Fabrication of GaAs nanowires and GaAs-Si axial heterostructure nanowires on Si (100) substrate for new applications

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Fabrication of GaAs nanowires and GaAs-Si axial heterostructure nanowires on Si (100) substrate for new applications

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Abstract— **The integration of III-V semiconductor nanowires on Si for nanoelectronics or nanophotonics devices is still a challenge. The monolithic integration of GaAs nanowires on silicon (100) by top-down approach enables new possibilities for the design and devices fabrication. We demonstrate the fabrication of GaAs-Si(100) nanowires array by plasma etching.**

I. Introduction

III-V nanowires-based devices represent a great interest for various applications including nanoelectronics [1], nanophotonics [2], biological sensors [3]. Integration of such nanostructures on the conventional silicon platform is a challenge. In order to make the bridge between fundamental studies on NW patterning and large scale device processing based on NWs new approaches should be developed. Traditionally, two complementary ways are used for nanowire fabrication: bottom-up growth and top-down patterning. The main advantage of bottom-up growth is the crystalline quality of nanowires and of the nanowires surface. However, the reproducibility and dimension control are difficult to reach, especially when selective area epitaxy approach is conducted to create localized NW array. Moreover, substrate orientation has an effect on nanowires orientation. In order to obtain vertical nanowires, Si (111) orientation is required [4], which is not the conventional substrate used in microelectronics (Si(100)).

The top-down approach allows nanowire patterning with better reproducibility, and dimension control accuracy. However, fine tuning of the nanowire etching is still a challenge together with the integration of III-V NW on silicon. Here, we will present for the first time a demonstration of III-V NW patterning on Si (100) based on a detail study of the nano-structuration.

II. Patterning for GaAs nanowires array

A. Process steps description

The starting wafer is composed a thin GaAs layer synthetized on Si (100) substrate by MOCVD without antiphase boundaries [5, 6]. The layer thickness is comprised between 200nm and 700nm. A top-down approach that couples Electron Beam Lithography (EBL) with anisotropic plasma etching was used to pattern the designed nanostructures. The EBL was carried out with a RAITH 150 writer at energy of 30 keV on a thin (90nm) negative-tone resist layer, namely hydrogen silsesquioxane (HSQ). After exposure, HSQ was developed by immersion in 25% tetramethylammonium hydroxide (TMAH) for 1 min (Fig.1-a) [7] to enhance the pattern contrast. HSQ patterns were subsequently transferred to the GaAs top layer by ICP-RIE (SPTS Omega 201, et Sentech SI500) in a Cl_2/N_2 plasma based chemistry down to the silicon substrate (Fig.1-b) [8].

In order to obtain axial heterostructure, a second step of plasma etching using SF_6/C_4F_8 chemistry was conducted (Fig.1-c).

The last step involves removing the resist and the passivation layer by wet etching with HF (Fig.1-d).

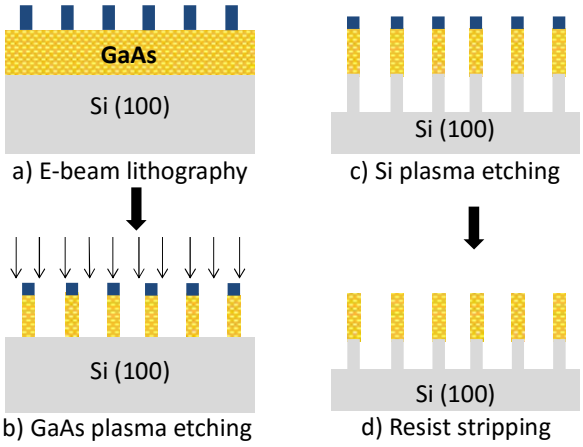

Figure 1. Process flow chart: a) First step is electron beam lithography with a negative resist (HSQ). b) ICP-RIE of GaAs thin layer by stopping on silicon substrate. c) ICP-RIE of silicon substrate. d) Last step is a wet etching to remove inorganic resist.

B. Patterning of GaAs by plasma

In order to determinate suitable parameters to obtain vertical nanowires, several parameters have been studied, shown in the Fig.2.

ICP power acts on plasma density (corresponding to the quantity of reactive species and ions). When the power increases, the increase of reactive species boosts the etch rate but also impacts the etching angle. At low ICP power, the dissociation energy is weak, promoting the reactive species formation to the ions formation. Therefore the chemical reaction is favored over the ionic bombardment. The chemical etching being isotropic, the etching profile is re-entering. It is necessary to apply a sufficient power level to obtain a good balance between chemical and physical etching, to tend towards vertical profiles (etching angle = 90°) as illustrated on Fig.2.

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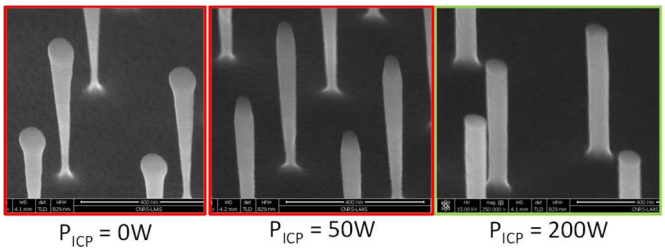

Figure 2. Influence of ICP power on etching angle and etch rate.

GaAs has been etched thanks to the combination of two gases: Cl_2 and N_2. Cl_2 is a reactive gas promoting the chemical etching. N_2 is a neutral gas favoring the physical etching (ions bombardment). By decreasing the Cl_2 / N_2 gas ratio, the reactive species quantity is reduced, therefore the etch rate decreases and the etching angle increases. In these conditions, etching profile is not vertical because physical etching is favored over chemical etching (Fig.3).

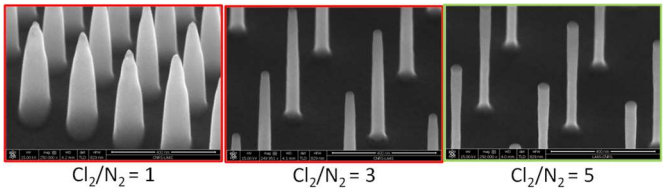

Figure 3. Influence of gas ratio on etching angle and etch rate.

All parameters are inter-dependant, the objective is to find right parameters to obtain a good balance between physical and chemical etching (Fig.4).

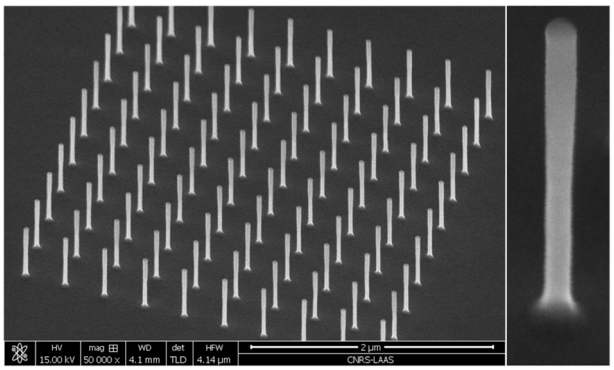

Figure 4. GaAs nanowires array (diameter = 40nm).

III. AXIAL HETEROSTRUCTURE NANOWIRES

To go further in the complexity of this work, we have also demonstrated the possibility to create GaAs/Si NW heterostructure based on this top-down approach.

After GaAs etching step, 50nm of HSQ resist is remaining on GaAs nanowires. The Si etching has to be selective compared to HSQ and not laterally etch the GaAs NWs. We used a process based on fluorine chemistry resulting on a Si/HSQ selectivity of 5. In this way, the top part of GaAs nanowires is not damaged (Fig.5).

For a perfect patterning of these hetero-structured nanowires, the challenge is to master the transition between the two etching chemistries in order to not degrade the Si/GaAs region. For that purpose, the end point detection during GaAs etching is critical. The over-etch of GaAs has to be less than 3 s, otherwise a lateral etching at the bottom of nanowires is accentuated resulting in mechanical fragility of the NWs and carrier mobility scattering.

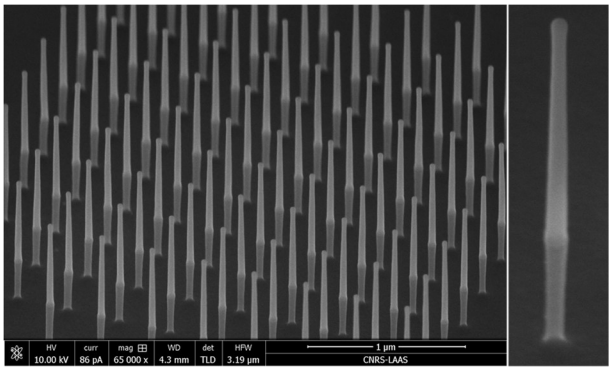

Figure 5. Heterostructured GaAs-Si nanowires array (diameter = 40nm) on Si(100) substrate.

IV. CONCLUSION

For the first time, we have demonstrated the fabrication of vertical GaAs nanowires array on Si (100) substrate. Moreover, this approach allows obtain axial heterostructure nanowires GaAs-Si. This technology opens the way to new integration schemes for nanoelectronics and nanophotonics applications.

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