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ABSTRACT

The purpose of this paper is to present an extensive study of three 1200 V silicon carbide (SiC) Power MOSFETs in non-destructive, but leading to degradations, short-circuit operation. Unusually, as compared with equivalent device built on silicon, the damage signature is a significant gate current increase but the components are still functional. In order to find the damage location, non-destructive and destructive methods have been carried out. The results converge to a local gate oxide breakdown caused by the important electrical and thermal stress during short-circuit operation leading to different failure mechanisms depending on the device design.

1. Introduction

Recently, several research efforts demonstrate that ruggedness of SiC power MOSFETs during short-circuit (SC) is, for most of devices, much lower than silicon (Si) devices, with similar rating [1]. Indeed, the weakness may be related to a higher short-circuit current density and a lower die area resulting in a higher temperature rising during SC leading to faster degradations.

During extensive testing in non-destructive SC operations of new commercial 1200 V SiC MOSFETs, some components have presented unusual degradations. Indeed, degraded components have shown an important gate-leakage current after few type-I SC tests but are still functional. During the SC tests, three recent planar components have been tested until degradation: two components (ST1 & ST2) manufactured by STMicroelectronics (SCT30N120, first generation) and one component (C1) manufactured by CREE (C2M0080120, second generation).

The aim of this paper is to investigate the electrical and physical degradations on the presented commercial SiC MOSFETs. In Section 2, the degradation scenario is described and analysed. In Section 3, a dedicated measurement methodology is proposed and applied in order to analyse the degradations and to propose physical explanations of the damage. In Section 4, experimental results are described and analysed. In Section 5, the experimental results on failure are correlated through physical study and damage analysis.

2. Degradation scenarios

The aim of the measurements was testing the components in an extreme mode but below destruction level. The device under test (DUT) is turned-on across a voltage source and through a polypropylene-capacitors tank providing the high- current pulse which is only limited by the device resistance. A step-by-step and careful increment of the short-circuit duration is realised. Fig. 1 shows the schematic of the proposed experimental set-up. The gate turn-on bias ($V_{buffer(ON)}$) is adjustable (18 V–21 V) as well as the blocking bias ($V_{buffer(OFF)}$) (−5 V–0 V) and the drain-source voltage (V_{DS}) (0 V–600 V). Measured data are saved and post-processed with MATLAB© and filtered (Gaussian filter $\sigma = 10$). The gate current is calculated with the voltage drop across the gate resistor.

The gate current and the drain saturation current over several SC tests on ST1 device are presented in Fig. 2(a). SC tests were performed, on this component, by increasing drain-source voltage (300 V to 500 V) and by increasing pulse duration (2 μs to 7 μs). The first permanent degradation occurred during the 19th short-circuit test within a short delay after turning off the device (permanent leakage current about −5 mA). Finally, a 20th pulse of a slightly shorter duration (6 μs) was performed after the degradation in order to evaluate its impact on the component. As a result, the component can still be operated and turned-on or off despite the high gate leakage current during the SC operation (Fig. 2). Moreover, the gate-source voltage drop into R_G caused by the gate current rise can explain the maximum saturation current decrease. However, the lower saturation current could also be explained by a decrease of the channel mobility [2] or a threshold voltage raise [3].

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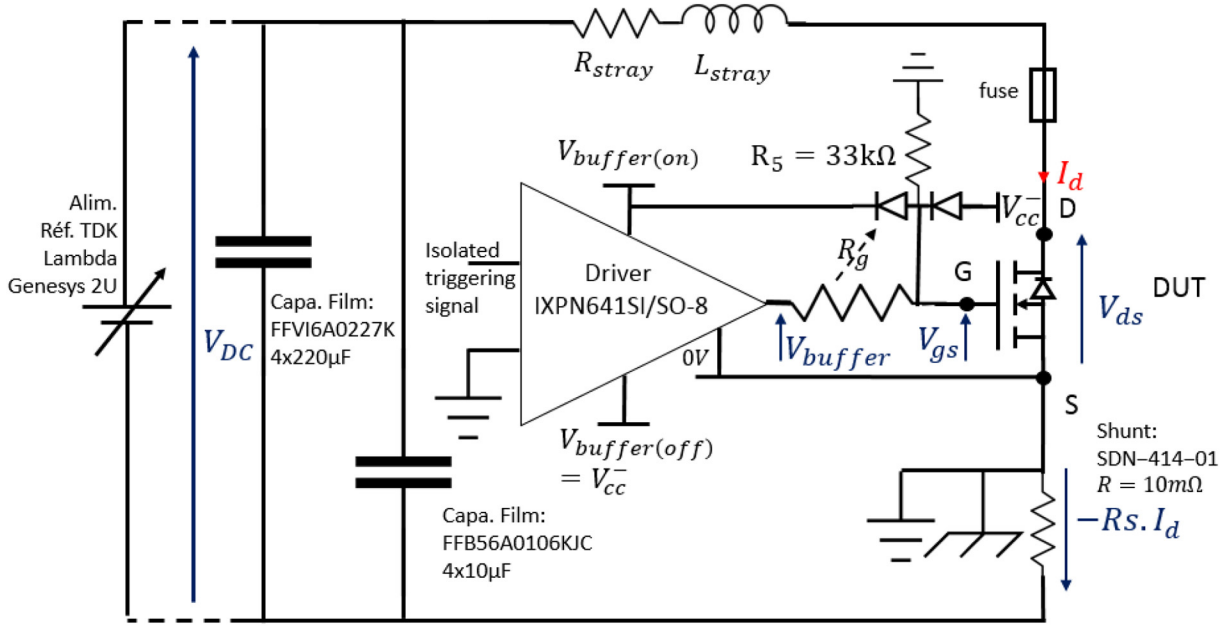

Fig. 1. Type 1 short-circuit test schematic. Oscillo.: Ref. Tektronix DPO4014B, BW 1GHz – 5 GS/s. Probes: 2 × Tek. TPP1000 300 V 1 GHz 3.9 pF, 1 × Tek.TPP0850 800 MHz 1000 V 1.8 pF — 300 mV offset compensation on V_{buffer} — L_{stray} = 52nH with fuse and DUT – Supply driver THB3-1215 – probes propagation time are compensated – aselfic coaxial shunt – CMS Schurter fuses.

In Fig. 3, component C1 was tested using the same protocol as ST1. However, a higher number of stress cycles were required in order to observe a significant evolution of the waveforms. From the 36th SC pulse at 5 µs, a decrease in the gate current is noticeable. At the 37th pulse, the gate current is lower than the previous pulse until 4 µs. For each following pulses, the leakage current increases step by step. As a result, maximum saturation current also decreases accordingly to the gate current variation as explained previously.

The aim of the following sections is to present a consistent theory about the particular degradation observed in Fig. 2 and Fig. 3.

3. Measurement methodology

In the studied MOSFET components, gate electrode is isolated from substrate with a thin layer of SiO_2 dielectric (typically 50 nm). After degradation, the gate is no longer isolated and the gate-leakage current is certainly caused by resistive paths through the SiO_2. The resistive paths are connected either to the N^- layer, the P-well, the N^+ layer or the top metal electrode (respectively named path-type n°1, 2, 3, 4). Fig. 4 depicts all possible damage locations and the impact of the applied gate-source voltage on the theoretical equivalent circuit.

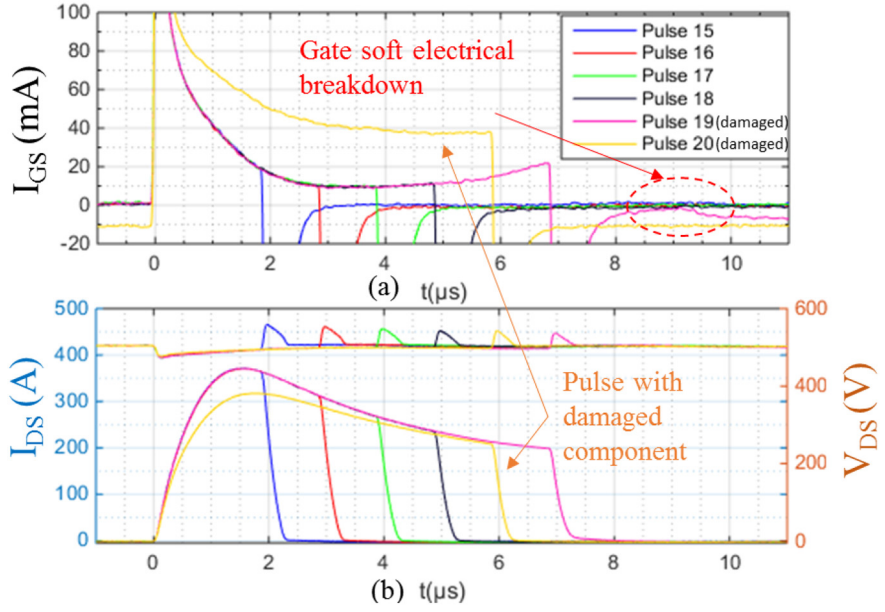

Fig. 2. ST1 device short-circuit waveforms. (a) Evolution of I_G, and (b) V_{DS}, I_D waveforms during the study. Each color represents a SC pulse with an increased on-time. (V_{DS} = 500V; $V_{buffer(ON/OFF)}$ = 18V/−5V; T_{case} = 25°C; R_G = 47Ω; ST1).

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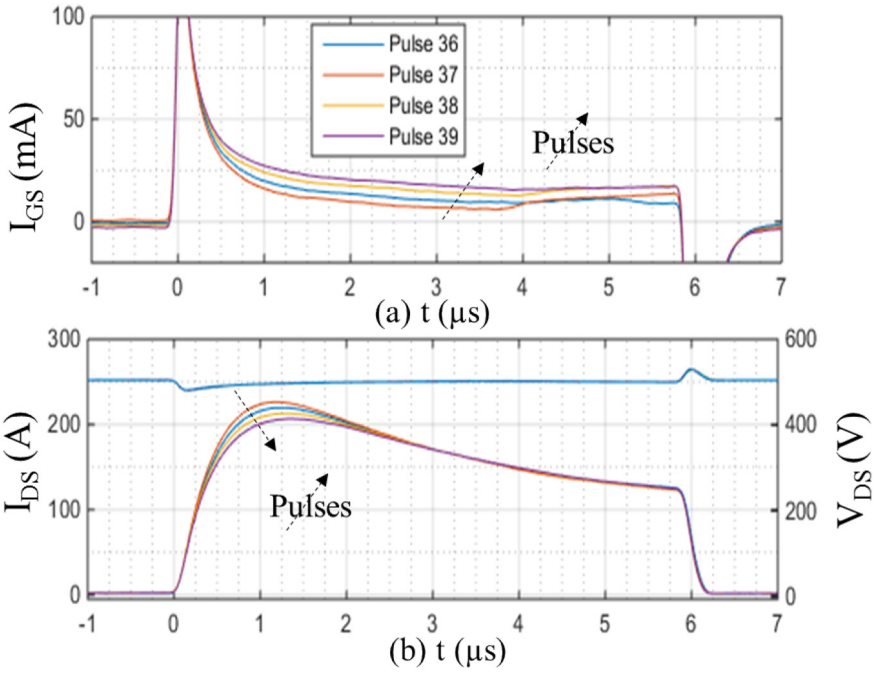

Fig. 3. C1 short-circuit waveforms. (a) Evolution of I_G, (b) V_{DS} and I_D during the study. Each color represents a SC. (V_{DS} = 500*V*; $V_{buffer(ON/OFF)}$ = 21*V*/−5*V*; T_{case} = 25°C; R_G = 100Ω; C1).

In order to determine which path-type exist and which one dominate, an electrical procedure, originaly adapted for planar Si CMOS [4], has been adjusted for SiC V-DMOSFET. The approach is based on the gate-source leakage current measurement for V_{DS} = 0 V and variable V_{GS} but also on the gate-drain leakage current measurement with variable V_{DS} and V_{GS} = 0 V. Moreover, this electrical method does not lead to further device degradation as long as the currents are kept at rather low levels.

In the first measurement, Fig. 5(a), a bias is applied on the gate while the drain and the source are short-circuited. The currents passing

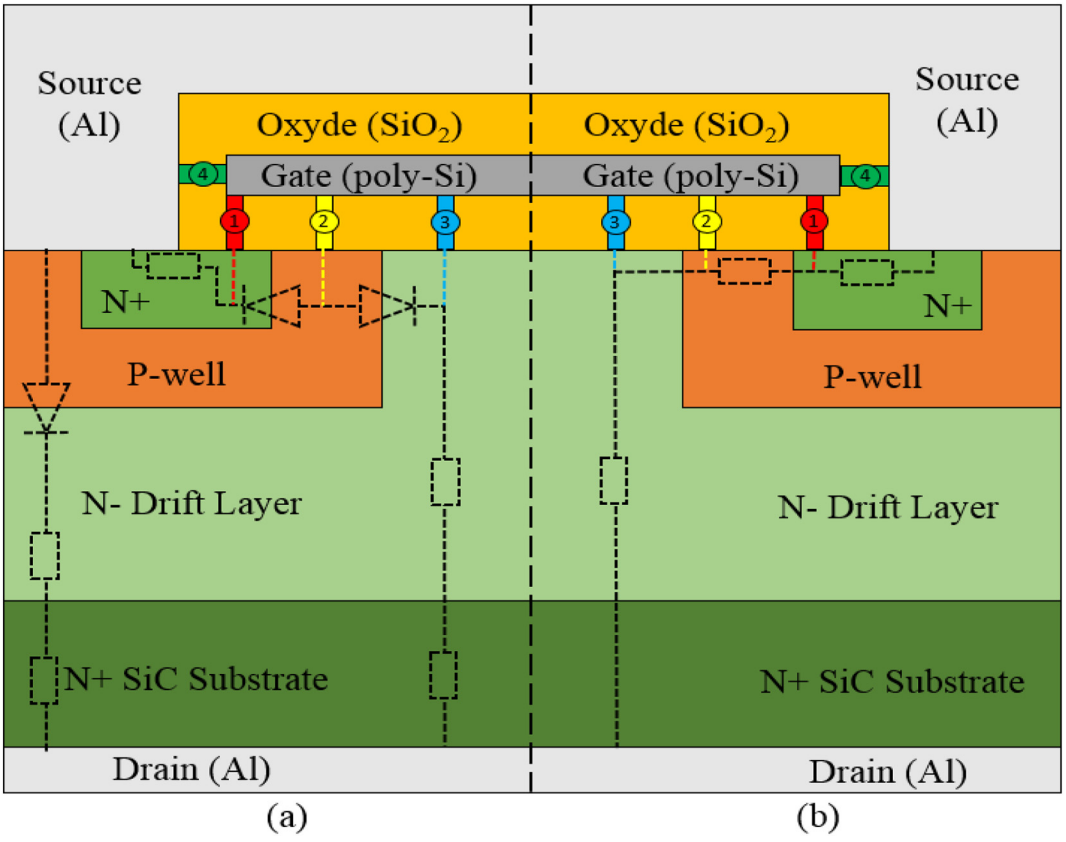

Fig. 4. Usual V-DMOSFET elementary cell. The local resistors named 1,2,3 and 4 models the damages in the oxide. (a) V_{GS}<$V_{GS(th)}$, the channel is non-conductive (b) V_{GS}>$V_{GS(th)}$, the channel is conductive.

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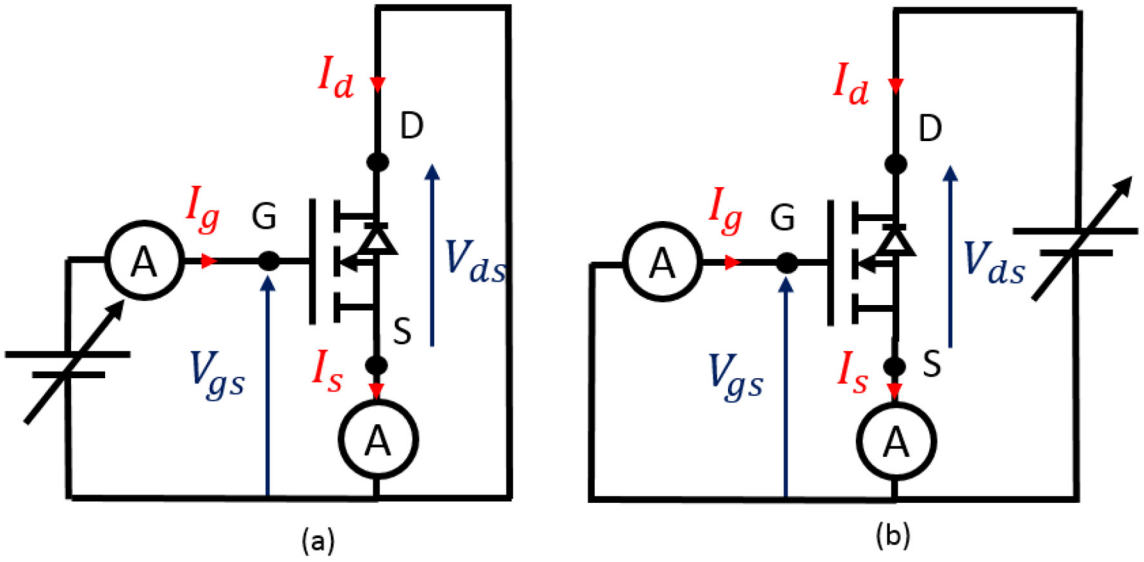

Fig. 5. Measurements performed with a SMU (Ref. Agilent B2902A 100fA 2ch.) and multimeter (Ref. Keithley 2700). (a) $I_G(V_{GS})$ Measurement (b) $I_G(V_{DS})$ Measurement.

through the gate and the source are measured. The currents passing through the gate and the source are measured. The current entering through the gate is going to come out either by the source or by the drain terminals depending on the least resistive path. The path resistivity depends on the gate polarization with respect to the threshold voltage (Fig. 3(a) or (b)) and the resistivity of each path-type damages.

If $V_{GS}<0V$, the channel is not formed and the intrinsic PN junctions (P-well/N^+, P-well/N^-) of the MOSFET are in the off state so that the path n°2 is inhibited. In that case, if $I_{GS}<0A$, the current is passing through the resistance constituted by damaged path n°1, n°3 or n°4. Make the difference between paths n°1 and n°4 is not possible. However, distinguish the paths n°1 or n°4 from path n°3 is performed by looking at the source current. Indeed, the more the source current is close to the gate current value, the more the paths n°1 or n°4 are prevailing upon path n°3.

Moreover, if the current I_G is zero for $V_{GS}<V_{bi}$ (where V_{bi} is the build-in voltage of one of the PN junction), and begins to increase when V_{GS}-V_{bi}, then the intrinsic diodes (P-Well/N^+ and P-Well/N^-) are in on state and the damage path n°2 is the dominant leakage path.

Furthermore, if damages n°1, 3 or 4 are existing according to the first test and if there is a change in the I_G slop for $V_{GS}>V_{bi}$, there is a competiton beween damage paths n°1, 3 or 4 and path n°2.

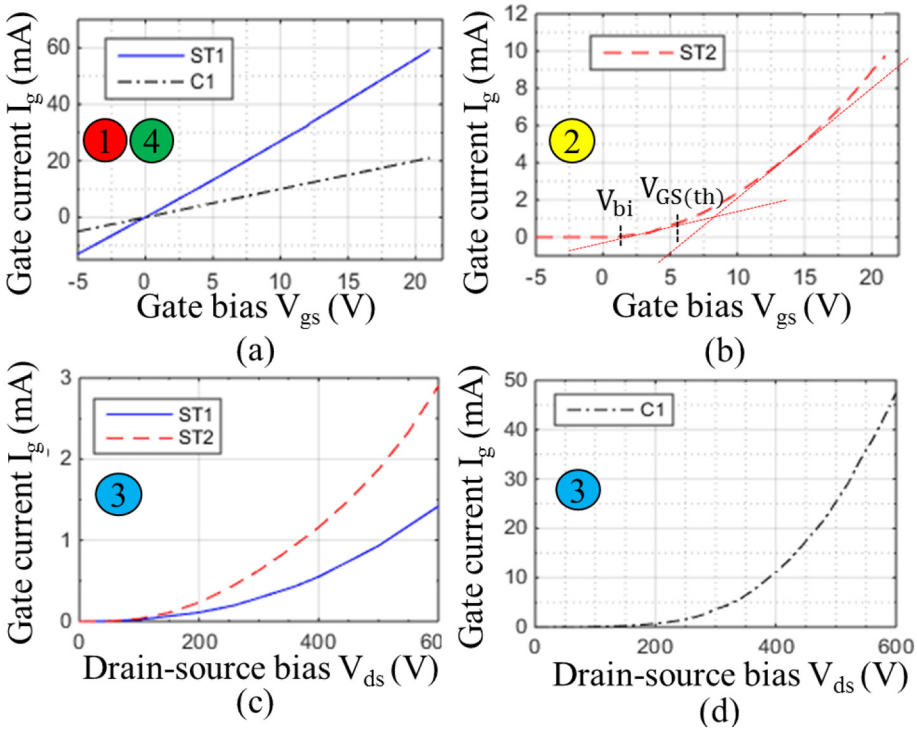

Fig. 6. Measurement results on damaged components. (a)&(b) $I_G(V_{GS})@V_{DS}=0V$. (c)&(d) $I_G(V_{DS})@V_{GS}=0V$.

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Finally, it happends that a path-type n°3 damage can exist even if other path are the dominant with the first measurement method. In order to find it, the component have to be polarized with $V_{DS}>0V$ and $V_{GS}=0V$. I_G and I_S are measured as depicted in Fig. 5(b). With this set-up, the path-type n°1, 2 and n°4 are disabled. If a gate current I_G is measured, this means that there is a path-type n°3.

4. Experimental results

Based on the analysis method described in the previous section and the measurement results presented in Fig. 6(a), (c) and (d), the damage paths n°1 or n°4 are clearly predominant in the components ST1 and C1 (source current not displayed here). However, a path-type n°3 exists for these two components and the damage is much more significant for ST1. The defects behaviour of these two components is very similar whereas they are from two different manufacturers. In Fig. 6(b) and (c), damages path n°2 and n°3 can clearly be identified for the component ST2.

Finally, it should be recalled that the actual component structure is constituted by a large number of cells similar to those shown in Fig. 3. Therefore, it is highly probable that the resistive paths identified by the proposed method will involve only a few cells.

5. Die analysis

5.1. Lock-in IR thermography (LIT)

In order to observe the damages and confirm the theory about resistive path-type developed in the previous sections, a physical study has been carried out on the degraded components ST1, ST2 and CREE. Indeed, in a first step, the resin on the top of the chip had been partially removed by laser machining followed by a chemical etching. In a second time, a very sensitive infrared thermography tool with a pulsed 25 Hz lock-in frequency is used to locate the hot spots, induced by the leakage currents of the transistors, on the chip surface [5]. Results are presented in Fig. 7. For all the components the hot spots are localised around the gate ring in the continuity of polysilicon gate fingers of the transistor interdigitated structure. For component C1, the defect seems to be localised at the interface between distributed gate metal and the source plan close to the source wire-bonding. Elsewhere, some defects could be under the remaining resin, close to the source wire-bonding. For all the components, no fusion has been observed on the top of the chip with optical microscopy analysis.

In conclusion, the thermal analysis localised damages but none are visible on the top of the dies so the damages are in the chip volume. As a result a study of the chip inside is needed.

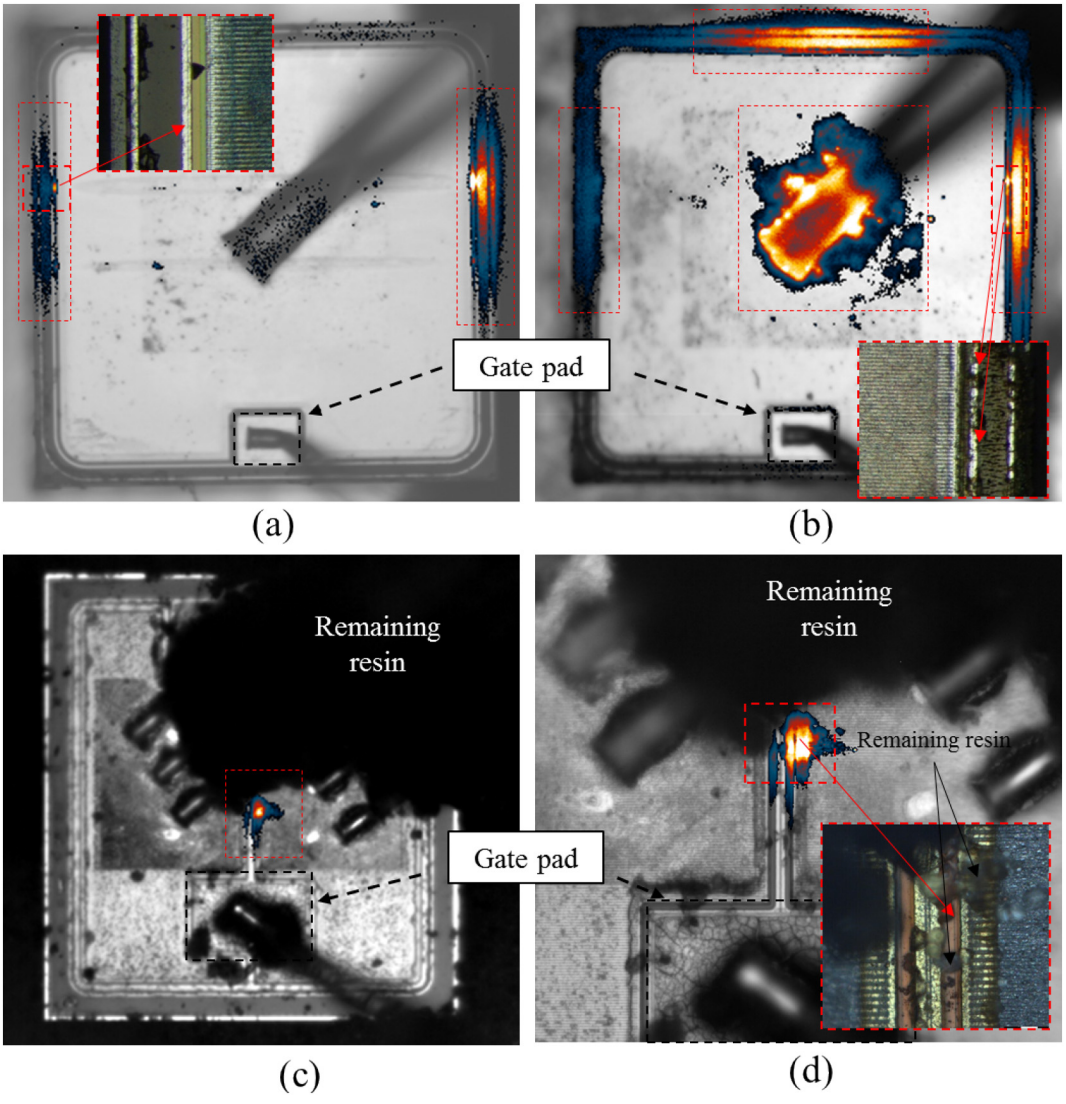

Fig. 7. Lock-in thermography: 25 Hz. Amplitude images. (a) ST1, (b) ST2, (c) C1, (d) C1 zoom.

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5.2. Focused ion beams (FIB)

For component C1, a focused ion beam (FIB) of Ga ions was used in the vicinity of the hot spot in order to obtain a microsection and to observe the oxide. In Fig. 8, the structure of the SiC V-DMOSFET is readily observable. The aluminium layer above the oxide, under the passivation appears to have melted and then migrated (Fig. 8(a)). Moreover, the dielectric around the polysilicon gate electrode, near its upper corners, has cracked with metal diffusion inside for some of them (Fig. 8(b)). Such metallic cracks may have been prior to the applied stresses, but they most likely were induced by the thermo-mechanical stress during the SC operation. The metal diffusion is most likely caused by the metal fusion (660 °C) or by aluminium migration into the SiO_2 oxide across the thin Titanium barrier layer. As a result, the path-type n°4 (Fig. 6(a)) measured on C1 is most likely caused by this metallic path. Unfortunately at this stage, FIB microsection limits SEM resolution. As a result, the oxide between the gate polysilicon and the SiC substrate (≅50 nm width) is not visible. Hence, the damage paths n°1, n°2 or n°3 cannot be seen. Moreover, paths n°2 and n°3 are more likely caused by percolation phenomena followed by very local dielectric fusions [6]. In that case, the damages position is very difficult to find for wide gate area because of the very low damage size. More investigations are in progress to analyse possible defects in the gate oxide and particularly by a scanning transmission electron microscope (STEM) analysis.

For ST2, a conventional microsection of the bare die with an allied multiprep polishing system (section axis perpendicular to the polygate fingers) was performed but no damage was clearly identified. Another microsection in the axis of the polysilicon gate fingers is in progress in order to try to better observe the hot spots zone.

5.3. Relations to literature

After extensive bibliographic researches, two papers presenting physical investigation on SiC power MOSFETs chips stressed by similar SC tests [2,7] have been found. The results, depicted in Fig. 9(a), confirm that the top aluminium is presenting signs of melting and migration due to the thermal stress applied during the SC operation. In [2], the component does not have a permanent gate leakage current but a saturation current decrease. At the opposite, results in Fig. 9(b), from [7], show cracks in the poly-Si gate for a component with a high and permanent gate leakage after an aging campaign in SC operations. According to the authors, the Poly-Silicon voids were formed from localised heat (high electric field and high temperature), leading to the gate oxide breakdown but the actual breakdown cannot be observed.

6. Conclusion

The paper attempts to provide a better understanding of the physical origin of the permanent gate-leakage current after few non-destructive (but leading to degradation) short-circuit operations of SiC power MOSFETs. As presented in Sections 2 and 3, a novel and consistent defect

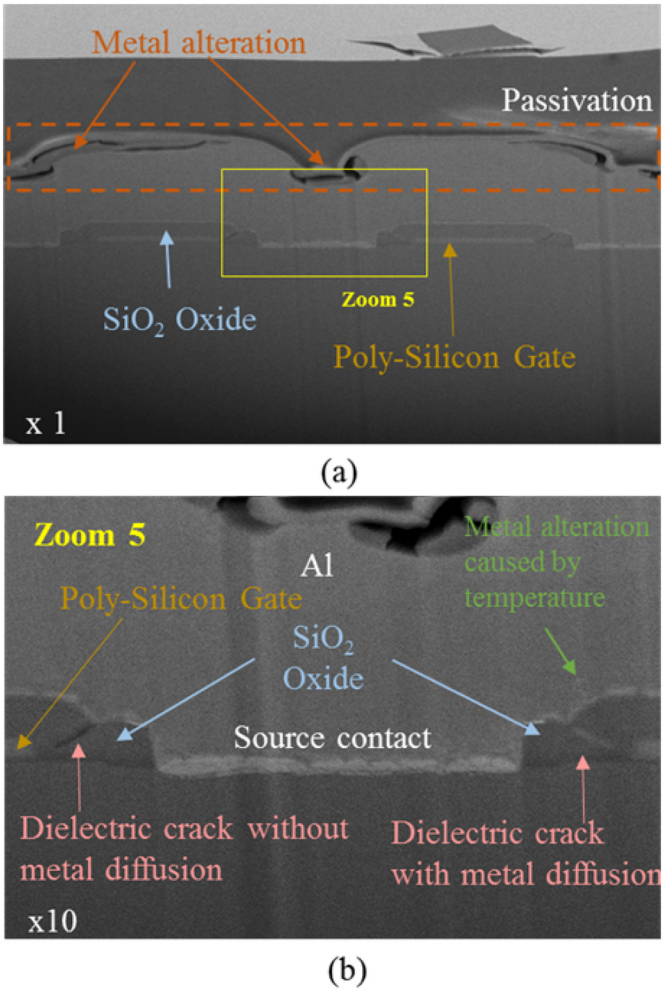

Fig. 8. Scanning electron microscope (SEM) images of the damaged area in C1. (a) image (b) zoom.

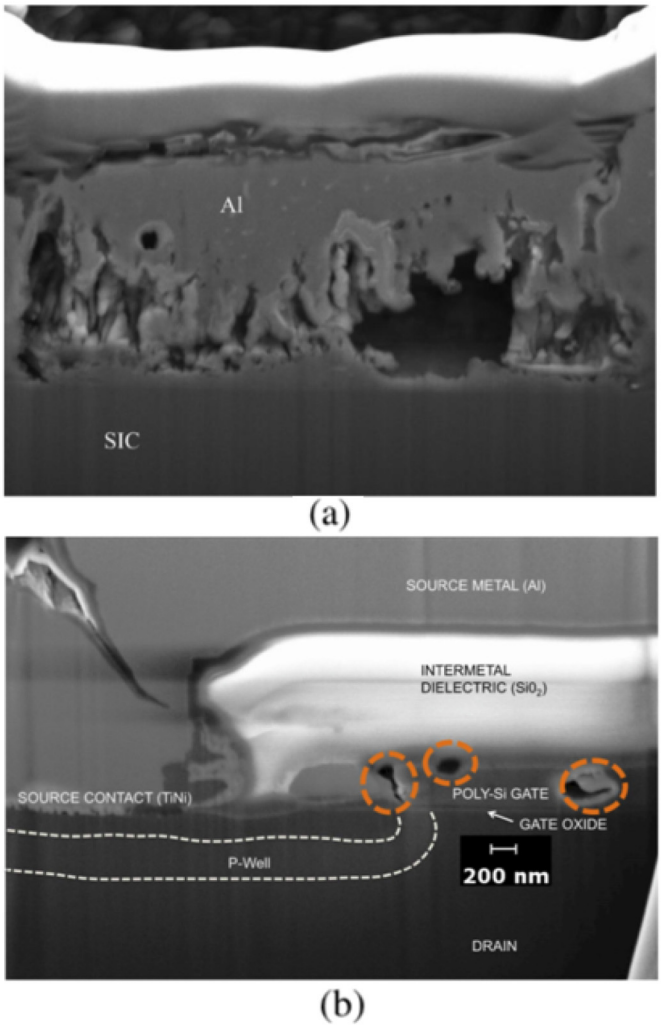

Fig. 9. (a) SEM image of degraded 10 kV 10 A 4H-SiC MOSFET, aluminium metallization at the source contact region between two cells [2]. (b) SEM image of the defect FIB cut localised by IR lock-in thermography. 1.2 kV 4H-SiC MOSFET [7].

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model made of four types of resistive paths was developed for vertical MOSFET. The model makes a link between electrical measurements and physical failure analysis. Indeed, FIB microsections and SEM investigations after LIT localisation on the chip confirm the path-type n°4 resistive damage with a crack followed by diffusion or migration of aluminium into the component C1. However, type n°2 and n°3 are not successfully observed using physical failure analysis, but electrical characterization tend to prove the degradation through these resistive paths, as reported in the literature. The STEM analysis, in progress, may confirm the presence of this type of defects in the gate oxide.

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