A power management system using reconfigurable storage scheme for batteryless wireless sensor nodes

Aris Siskos, Firdaous El Mahboubi, Vincent Boitier, Th Laopoulos, Marise
Bafleur

A power management system using reconfigurable storage scheme for batteryless wireless sensor nodes

A. Siskos[1,2], F. El Mahboubi[1], V. Boitier[1], Th. Laopoulos[2], M. Bafleur[1]

[1] LAAS-CNRS, Université de Toulouse, CNRS, UPS, Toulouse, France
[2] Aristotle University of Thessaloniki, Physics Department, Thessaloniki, Greece

Abstract—**The expanding network of wireless sensors nodes for IoT applications requires autonomous and low power systems. Supercapacitors (SCs) and energy harvesters manage to replace batteries, offering power autonomy and lifetime. In this work, it is presented a power management system that uses a reconfigurable SC scheme as storage media that is capable to store sufficient energy, while presenting a rapid initial charging. The system is implemented in CMOS 0.35µm AMS technology and consists of a reconfigurable bank of SCs, which is the power source of the node, a control unit and a LDO providing constant output voltage for the wireless sensor node (WSN).**

Keywords—energy autonomy; wireless sensors; energy harvesting; supercapacitors; smart storage; battery-free.

I. INTRODUCTION

Wireless sensor networks and applications or the so-called Internet of Things (IoT) are having an enormous impact on our daily lives. This technology aims at making the world more comfortable, safe, and environmentally friendly in many different applications such as the smart home, the factory of the future or the smart grid. One of the main roadblocks to the large deployment of wireless sensors is their energy autonomy. Predictions talk about 50 billions of connected objects meaning 50 billions of batteries with a limited lifetime that is not acceptable in terms of sustainability and cost. Low-power electronics and efficient power management of the node have allowed greatly extending the lifetime of batteries. However, they still need to be replaced at the end of their life. To cope with this issue, energy harvesting from the ambient environment is an interesting alternative. As the energy source may become temporarily unavailable or too weak, storage is still needed to allow for some buffering. Moreover, some applications in severe environment prohibit the use of primary batteries for safety issues or access difficulties.

To solve these issues, we have proposed to move to a battery-free wireless node using storage on supercapacitors [1]. Supercapacitors have many advantages such as an almost infinite lifetime, wide operating temperature range (particularly in the negative temperatures), high power density and being environment friendly. However, one of the main drawbacks is that its voltage is charge dependent and is zero when the supercapacitors are empty. As a result, powering a system with supercapacitor-based storage has two main issues: cold start (with empty storage), varying voltage and energy usage efficiency. Regarding the latter issue, the electronics generally stops working for a given voltage threshold although there is still plenty of energy stored in the supercapacitor. To cope with these issues, we have proposed a concept of smart or adaptive storage that can reconfigure according to the source availability and/or to the load demand. This concept was experimentally validated using FPGA for the control logic and external power supply for its powering [2]. The validation of the self-powering of such smart storage building block was experimentally carried out and exhibited an energy efficiency usage of 91% [3].

The next step is to build up a fully integrated smart storage block that could entirely replace a battery. To do so, integrated microstorage is needed and its feasibility has already been demonstrated with specific capacitance as high as 1000 mF/cm2 and a specific energy density of 49 µWh.cm-2 using porous gold/RuO2 electrodes [4]. This microstorage has to be integrated with its smart power management and a simple voltage regulation. This is the purpose of this work, which reports the design of the different blocks needed to build up this function. The full circuit was designed using 0.35µm CMOS C35B3L3 technology from AMS. In the following, we will describe the global architecture of this functional block and the main difficulties encountered within the different sub-blocks and how they were solved.

II. SYSTEM DESCRIPTION

A. Topology SC and configurations with switches

The system is based on the reconfiguration of a number of SCs from an all-series topology where the minimum energy is stored, changed to a partial series-parallel configuration and finally to an all-parallel configuration, where the maximum energy is stored (Fig. 1. (a)).
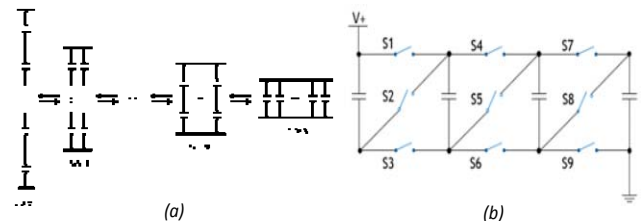

Fig. 1. (a) Arrangement of SCs. (b) Schematic of reconfigurable SCs architecture [2, 3].

The optimum number of SCs is $2^N=4$, where N is the order of discretization of the total capacitance [2]. The topology of the proposed system with four SCs needs N+1 stages and $3*(2^N-1)$ switches, as it is presented in the Fig.1. (b).

B. System description and Specifications

The system, which is indicated in Fig. 2, requires nine switches as mentioned above, a control unit circuit that produces the correct signals for driving the switches depending on the desired configuration of SCs and a regulator that feeds energy to the load. Additionally, the system has to be fully autonomous and generic.
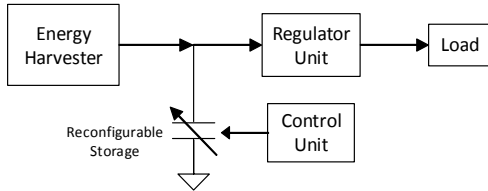

Fig. 2. Block diagram of the system of reconfigurable storage unit.

Considering that the system has to be fully autonomous and the energy is harvested from the environment, it is mandatory to consume low power. Since, the system is batteryless the control unit must be powered via the SCs. During the changes between SCs topologies, the voltage stored in the adaptive storage unit varies rapidly in a wide range of values, depending on the switching frequency. This implies that the control unit and the regulation unit should present high power supply ripple rejection (PSRR) to sustain the robustness of their function.

The most challenging block of the system is the design of switches. The switches need to be of low on-resistance and able to startup in all-series configuration and rapidly change configurations.

Finally, the regulation unit has to produce a regulated output voltage.

C. Proposed Solution

The proposed solution for the current configuration is the system depicted in Fig. 3. The system is implemented in the CMOS 0.35μm AMS technology using the flavor that includes low threshold voltage transistors, which are used to implement the switches. For the switches S1, S2, S4, S5, S7 and S8 are used PMOS and for the rest NMOS transistors. This choice gives the ability to self-start-up the system. The size of the switches is considerably large, so that they will be able to make the fast transition between the topologies and have low on-resistance to minimize losses.

The bank of SCs is made up of four commercial ones from AVX Bestcap with a rated voltage at 5.5V and a capacitance of 100mF. These SCs are modeled by adding characteristic series and parallel resistors (to take into account its leakage current).

The control unit is based on two comparators and a delay line for each one, which sets the switching frequency. The two comparators have the same voltage reference and different inputs, where low and high threshold voltage are applied. The input of the first comparator is changing the topology between

all-series (AS) to series-parallel (SP) and vice-versa and the second one is used to change the topology between series-parallel (SP) and all-parallel (AP) and vice-versa. The threshold voltages for two comparators are $V_{thL}=1.3V$ and $V_{thH}=2.6V$ respectively, provided by the fourth SC.

A low dropout regulator (LDO) has been decided for the regulation of the system output voltage and also it defines the threshold for the comparators. Because of the reconfigurable topologies, the LDO has the advantage to operate both for AP and for SP configurations till 2.6V. So, the use of the LDO provides the advantage of longer discharging time and therefore more energy to the load. Also, the LDO can manage to regulate an output voltage at 2.3V (the dropout voltage being 300mV), when both the variations of the voltage level of SCs and the variations of the load are occurring.

For the reference of the LDO and the control unit, we used a bandgap reference circuit.

The system does not integrate the voltage divider for setting the thresholds of comparators inputs. Also, feedback resistors and capacitor of the LDO are external. The reason for this choice is to make the system as generic as possible.
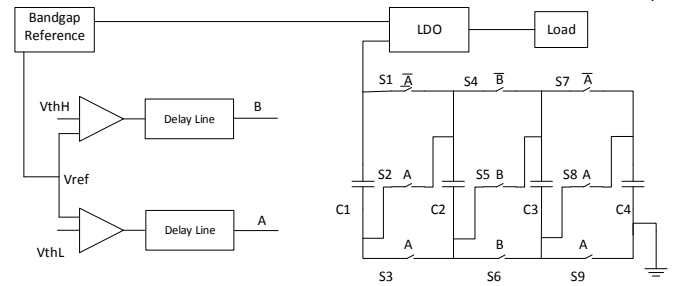

Fig. 3. Proposed architecture for the reconfigurable SCs bank

III. SYSTEM SUB-BLOCKS

A. Switches

As it is mentioned above, the switches are implemented with PMOS and NMOS with low threshold voltage transistors. For PMOS switches it is needed to implement a bulk regulation technique as in [5], because the supply voltage is not constant, but it is varying as the SCs charge or discharge. The switch transistors are very large (PMOS W/L = 60.000/0.5 and NMOS W/L=24000/0.5), to ensure fast transition between the different configurations of SCs.

B. Comparators and delay line

The architecture of the comparators consists of three stages and is illustrated in Fig. 4. The first stage is a differential amplifier, which is biased through cascode transistors for achieving high PSRR and stable output independent from the power supply fluctuations. The second stage is an inverter, with an additional PMOS in cascode configuration. The third stage is a simple inverter, which shapes the high and low level of its output voltage correctly. The voltage reference of the comparators was decided on 400mV.
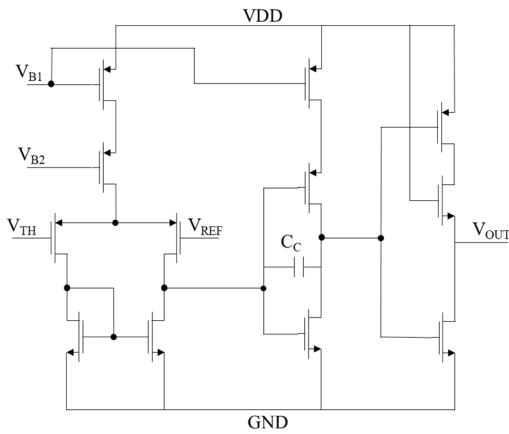
Fig. 4. Proposed comparator

The delay line at the output of each comparator is a cascade of three scaled inverters and four external capacitors, one at the output of the comparator and one at the output of each inverter respectively. The last two capacitors for each delay line set the switching frequency. For the proposed design, the switching frequency is 10kHz.

C. LDO

The LDO is a typical LDO architecture, shown in Fig. 5. The error amplifier, indicated in Fig. 6, is implemented using a modified OTA, as in [6]. The modification consists in the addition of (a) cascode transistors in order to enhance PSSR and (b) a source follower stage at its output to ensure fast switching of the pass element.
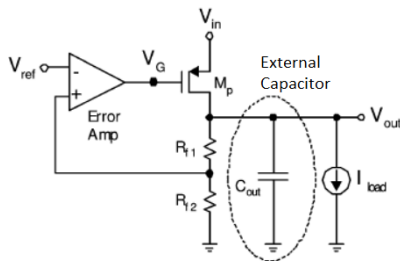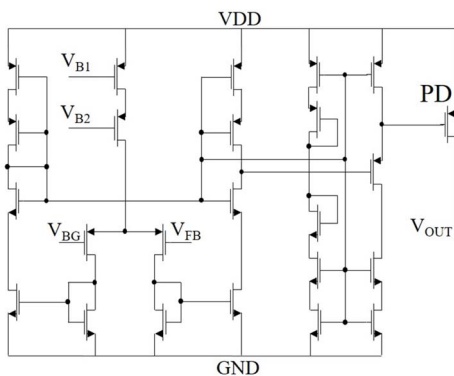

Fig. 5. LDO conceptual diagram.

Fig. 6. Error Amplifier and Pass Device of LDO.

D. Bandgap Reference and buffer

The architecture of the bandgap reference circuit was implemented as in [7], which has the advantage to feature an extremely high PSRR. The output voltage of the bandgap reference is 1.22V. A voltage divider implemented with transistors, was used to provide the voltage reference of the comparators. In order to maintain the output voltage of the bandgap reference at 1.22V a buffer was designed to isolate the bandgap reference and the voltage divider.

IV. SIMULATION RESULTS

The design of the integrated circuits was implemented in CMOS 035AMS (flavor C35B3L3), and the layout is presented in Fig. 7. The metal interconnections between the switches and SCs have to draw large currents, therefore they laid out using wide stacked metals, with the appropriate slots. In order to protect the rest of the circuits from substrate currents, local guard rings are implemented.

Considering that the power supply voltage for the circuits is the voltage provided from the SCs bank, which is changed each time the SCs are reconfigured, it was crucial to design all the circuits with high PSRR, as the voltage varies during the reconfiguration from 2.6V to 5.5V. Post-layout simulations showed that the comparator presents very high PSRR of -130dB (power supply range in 2–5.5V) and the bandgap reference presents PSRR of -100dB for the same power supply range. The PSRR of LDO is -35dB for 2.6V, which is the minimum input voltage, and -87dB for 4V and 5.5V and is illustrated in Fig. 8.

The temperature coefficients of bandgap reference at 2, 3.75, 5.5V supply voltage are 25ppm/ºC, as shown in Fig. 9.

Fig. 10 shows the transient analysis for the LDO, when the input voltage and load current are varying. For the input voltage was chosen a pulse of period of 5ms with a frequency of 100kHz from 2.6 to 5.5V. The load current is a pulse of period of 2.5ms with frequency of 100kHz from 0 to 50mA. The error in the output voltage is 0.25%.

The system is operating from 700 μA to 15mA charging current and from 0 to 50mA discharging current. The charging time of the system for 5mA current is 310s, indicated in Fig. 11. The discharging time of the system for 5mA current is 285s, indicated in Fig. 12. This time is considerably lower than in case of only one SC with value 400mF.

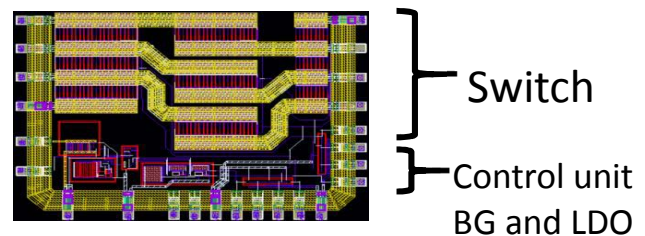The average power consumption of the total circuit is 185μW.
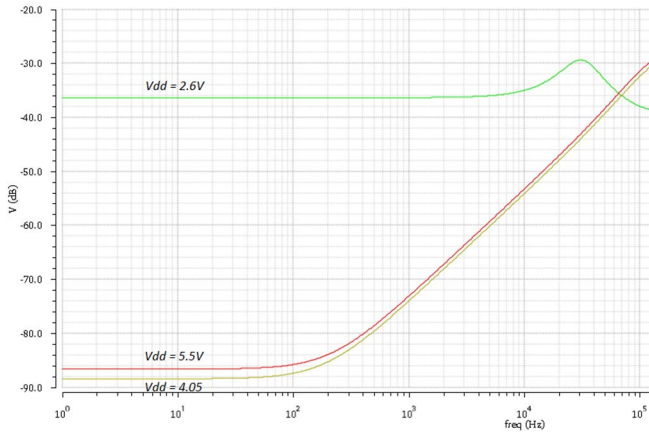

Fig. 7. Layout of the proposed system
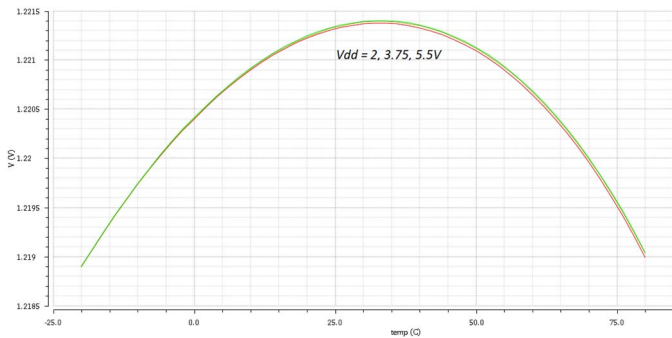
Fig. 8. PSRR of LDO for V_{IN} = 2.6, 4.05 and 5.5V

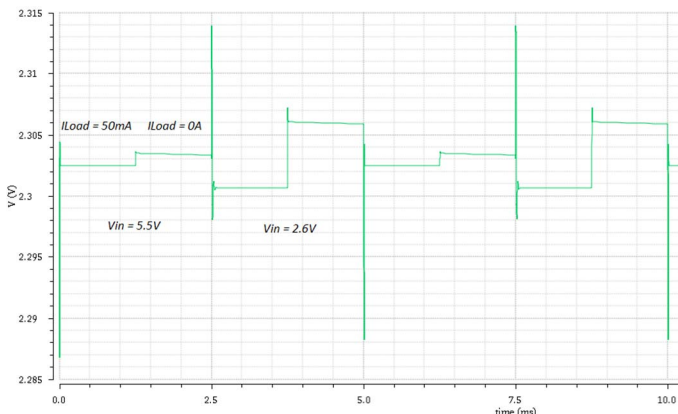Fig. 9. Temperature dependence of the bandgap reference for V_{DD} = 2, 3.75 and 5.5V

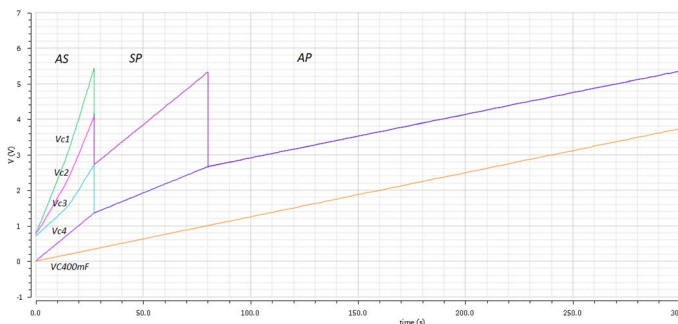Fig. 10. Transient analysis of LDO for VIN and ILOAD variations.

Fig. 11. Simulation results of the reconfigurable bank of SCs for the three phases of charging versus one equivalent capacitor (curve VC400mF)
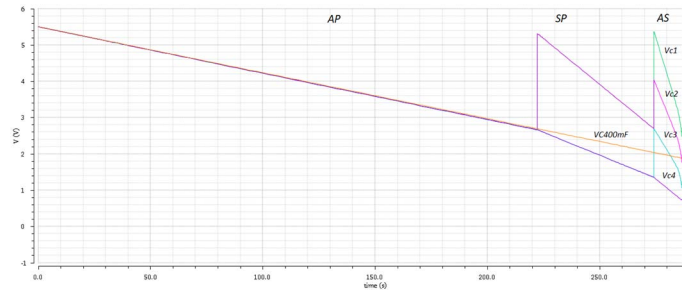

Fig. 12. Simulation results of the reconfigurable bank of SCs for the three phases of discharging versus one equivalent capacitor (curve VC400mF)

V.   CONCLUSIONS

In this work, it is proposed an integrated circuit for power and control management of a reconfigurable topology of SCs. Taking into consideration that the utilized technology is very mature, post-layout simulations demonstrate the feasibility of the proposed power management system using reconfigurable supercapacitors bank. Despite the challenges of such a design, the integrated circuit validates that the current topology of SCs can operate autonomously, without battery, with self-start-up and low power consumption. In the future it will be integrated the charging unit (i.e. harvester-DC/DC converter) to build a perpetual power supply unit for WSN and IoT.

REFERENCES

[1] J-M. Dilhac, M. Bafleur, "Energy Harvesting in Aeronautics for Battery-Free Wireless Sensor Networks," IEEE Aerospace & Electronic Systems Mag., Vol.29, Iss. 8, Aug. 2014, pp.18-22.

[2] R. Monthéard, M. Bafleur, V. Boitier, J-M. Dilhac and X. Lafontan, "Self-adaptive switched ultra-capacitors: a new concept for efficient energy harvesting and storage," PowerMEMS 2012, ATLANTA (USA), December 2-5, 2012, p. 283-286.

[3] F. El Mahboubi, M. Bafleur, V. Boitier, A. Alvarez, J. Colomer, P.Miribel and J-M. Dilhac, "Self-Powered Adaptive Switched Architecture Storage," 2016 J. Phys.: Conf. Ser. 773 012103, [PowerMEMS 2016, Paris (France), December 6-9, 2016].

[4] T.M. Dinh, A. Achour, S. Vizireanu, G. Dinescu, L. Nistor, K. Armstrong, D. Guay, D. Pech, Hydrous RuO2/carbon nanowalls hierarchical structures for all-solid-state ultra high-energy-density micro-supercapacitors, Nano Energy, Vol.10, pp.288-294, Nov. 2014.

[5] C.Peters, O.Kessling, F.Henrici, M.Ortmanns, and Y.Manoli, "CMOS Integrated Highly Efficient Full Wave Rectifier," Proc. IEEE international Symposium on Circuits and Systems (ISCAS 2007), pp. 2415-2123, 2007.

[6] R. J. Milliken, J. Silva-Martinez, E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," IEEE Trans. Circ. Syst.-I: Reg. Papers, Vol. 54, No. 9, pp. 1879 - 1890, Sept. 2007.

[7] W. Li, R. Yao, L. Guo, "A Low Power CMOS Bandgap Voltage Reference with Enhanced Power Supply Rejection," IEEE 8th Int. Conf. on ASIC, 2009. ASICON '09, Oct. 2009, Changsha, Hunan, Chin