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To cite this version:

Ahmet Lale, Auriane Grappin, Emmanuel Scheid, Jérôme Launay, Pierre Temple-Boyer. Design, realization and characterization of silicon nanowire ion sensitive field effect transistors. IEEE Nanotechnology Materials and Devices Conference, IEEE NMDC 2016, Oct 2016, Toulouse, France. 2p., 10.1109/NMDC.2016.7777159 . hal-01871410

HAL Id: hal-01871410

https://laas.hal.science/hal-01871410

Submitted on 10 Sep 2018

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Design, realization and characterization of silicon nanowire ion sensitive field effect transistors

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***Abstract*— The aim of our research project is to achieve a potentiometric multi-sensor platform, consisting of ion sensitive field effect transistors ISFET and MOSFET, which channel is a nanowire or a network of horizontal Silicon nanowires and whose gate insulator is alumina Al_2O_3 deposed by Atomic Layer deposition ALD. This microdevice will provide chemical and biological analyses in the liquid phase, in microfluidic channels.**

I. INTRODUCTION

Ion sensitive field effect transistors are microsensors derived by metal oxide semiconductor field effect transistors [1]. These are electronic microsensors designed to measure the pH. ISFETs have been functionalized for many applications such as the measurement of potassium [2], sodium [2], ammonium [3], urea [4], creatinine [5], lactate [6], glutamate [7] ...

Today, to open the door to new innovative applications, it is necessary to increase the sensitivity, decrease response times and detection limit of ISFET. To meet this challenge, the transistor based on silicon nanowires with surrounding gate seems to be the ideal candidate: low channel dimensions allow to work in micro-volume and thus to reduce the amount of analyte. But the biggest advantage lies in being able to work at the single living cell level. Moreover, the atomic layer deposition (ALD) now allows to achieve, for these nanoISFETs, controlled nanometric thickness gate insulators with adequate quality in terms of defects.

II. STUDY OF ALD ALUMINA

To achieve the gate insulator of our transistors, we have chosen to replace the silicon nitride Si_3N_4, previously used for the ISFETs in our past studies, by alumina Al_2O_3 which provides better sensitivity [8], which is a better insulator in liquid phase [8] and allows to be more selective against sodium and potassium than silicon nitride [8]. We chose to deposit the alumina through the ALD. The advantage of this technique is to deposit extremely compliant films and whose thicknesses are controlled close to the molecular monolayer [9]. The principle is to make successively reacting precursors, directly on the substrate's surface. A successive reaction of the precursors creates a molecular monolayer of alumina and this cycle is repeated n times according to the desired thickness. The first work was to make alumina films from 100 ALD cycles (~ 11nm) to 600 ALD cycles (~ 54nm) to study the deposition kinetic. Figure 1 shows the evolution of the average thickness (measured by ellipsometry) deposed by each ALD cycle to measure the deposition velocity. We compared the evolution of the refractive index of these deposits (figure 1) and we have highlighted a correlation between the refractive index and the deposition kinetic.

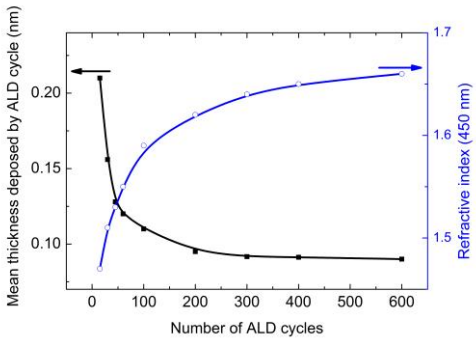

Figure 1 : evolution of refractive index and average thickness deposited by each ALD cycle based on the total number of completed ALD cycles.

Previously we obtained a 40nm deposit, with a refractive index of 1.65, a bit too low, the refractive index of the massive alumina being 1.78 without extinction coefficient [10]. To improve refractive index of our material, we did a thermal annealing campaign of 5 minutes under N_2/H_2 and we were significantly closer to the refractive index of the massive alumina (figure 2), on the other hand, we measured an extinction coefficient, that we explain by deficiencies in oxygen that appear in our material with the temperature rise. So, we decided to make our post-deposition annealing under O_2 and we have improved the index of refraction as previously (figure 2) while keeping a null extinction coefficient.

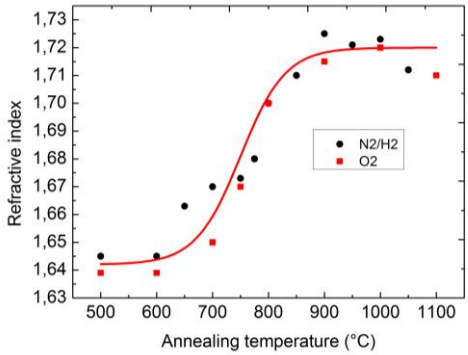

Figure 2 : changes in refractive index of alumina according to the post-deposition annealing temperature.

An X-ray diffraction study of ALD Al_2O_3 showed that alumina films are amorphous after deposition, but they crystallize when they are annealed up to 750°C. It shows that a structural modification of alumina induces the optical index improvement.

We have made MIS capacitors (metal insulator semiconductor) with the alumina as an insulator, to electrically characterize the ALD deposition. With C(V), we

noticed that the flat-band voltage decreases with annealing temperature, which means that it lowers the number of charges in insulator (figure 3). The accumulation capacity increases as well as the dielectric constant from 8.5 for non-annealed layers to 10 for layers annealed at 900°C (figure 4), conform to the literature of massive alumina [11].

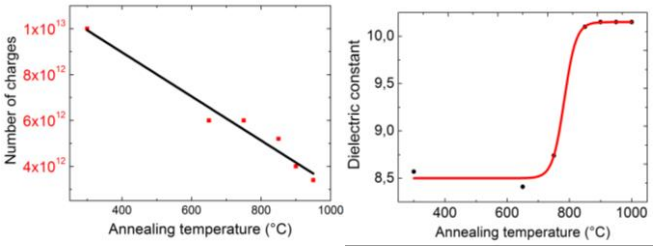

Figure 3 : left, number of charges in the insulator according to the annealing temperature under O_2.
Right, dielectric constant depending on the annealing temperature under O_2.

III. NANOISFET STRUCTURE

We used, on 6 inch SOI wafers, the projection photolithography with a resolution lower than 250nm, less than the maximum resolution of used Canon FPA-3000i4 stepper (350nm) and photoresist AZ ECI 3012, (400nm). After optimizations, we have managed to achieve on a single chip, with the same insolation parameters, transistors with a single nanowire as channel, next to transistors with 100 nanowires parallel network. The goal is to eventually compare in liquid phase, the pros and cons of each structure. We obtained reproducibly nanowires width less than 200nm. Once photoresist nanowires were optimized, we transferred them into silicon thanks to a reactive ion etching. Source and drain areas were N doped with arsenic. Then comes the realization of the gate insulator with alumina after RCA cleaning process (figure 4).

Once the transistors and interconnections ended (figures 4), we realized covered fluidic channels, using the SU8-3D technique [12], which has been optimized for 5 µm wide channels (figure 5).

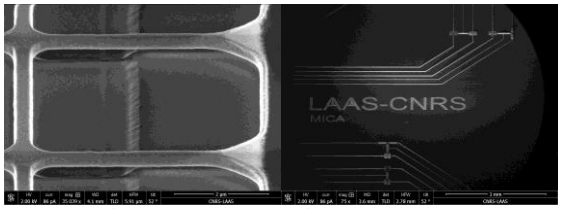

Figure 4 : left, silicon nanowires, after gate insulator completion. right nanoMOSFET and nanoISFET with interconnections.

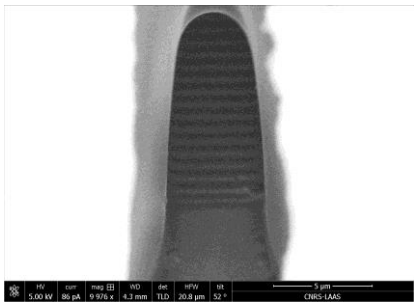

Figure 5 : dense nanowire network in a SU8 microfluidic channel, after removing the cover through a FIB etching.

Firstly, concerning MOSFET characterizations, we obtained very low subthreshold current: 10^{-14}A for Vg = 2V and low leakage currents through the gate (figure 6).

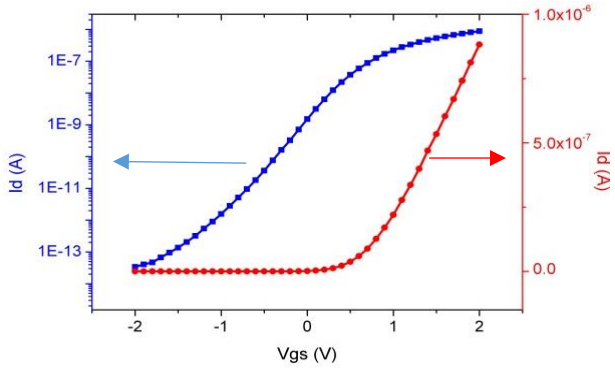

Figure 6 : I(V) characterization of a nanoMOSFET, red with a linear scale and blue with a semi-logarithmic scale. (V_{DS} = 0.1V)

We have then characterized nanoISFETs in liquid phase, and as for the MOS transistors, we got excellent characteristics, with extremely low leakage currents through gate insulator (10^{-12}A for Vg = 2V). Subthreshold Id current is also excellent. In addition, we have a good response to the pH variations (figure 7).

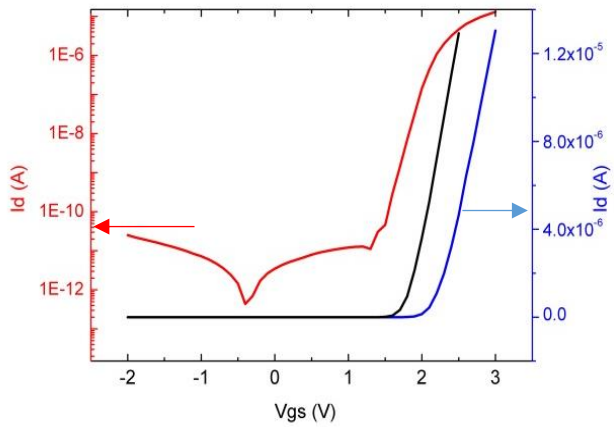

Figure 7 : I(V) characterization of a nanoISFET, in black pH 4, pH 7 in blue, red at pH 7 with a semi-logarithmic scale. (V_{DS} = 0.1V)

IV. CONCLUSION

We studied alumina deposed by ALD and we have demonstrated that it is possible to improve its physical and dielectric characteristics using thermal annealing under oxygen. We then realized nanoMOSFETs and nanoISFETs using alumina as gate dielectric. The first pH characterizations made in liquid medium are very encouraging for the future, with the perspective of the study of single living cells.

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