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Design Optimisation of the Deep Trench Termination for Superjunction Power Devices

Sylvain Noblecourt, Frédéric Morancho, Karine Isoird, Patrick Austin, and Josiane Tasselli

Abstract—Among the numerous solutions developed to improve the voltage handling capability of superjunction power devices, the Deep Trench Termination (DT²) is the most adapted thanks to its lower cost and size compared to other technologies using the multiple epitaxy technique, and an easier implementation in the fabrication process. This paper presents the optimization of the Deep Trench Termination by means of TCAD 2D and 3D-simulations allowing the realization of deep trench superjunction devices (diodes and MOS transistors) for 1200 V applications. The work is focused on the influence of the dielectric passivation layer thickness and the field plate length on the breakdown voltage of a DT-SJDiode.

Index Terms—deep trench termination; field plate; Superjunction; Breakdown voltage

I. INTRODUCTION

TODAY, the main IGBT competitor is the MOSFET. Indeed, the MOSFET exhibits many interesting properties for power applications: high switching speed, high input impedance and thermal stability. However, in high voltage range (600 V and above), conventional MOSFETs are limited by their very high specific on-resistance and, therefore, their high on-state voltage drop, which induces more on-state losses compared to bipolar devices. This on-resistance is inversely proportional to the doping concentration of the drift region, which must be low enough to sustain the off-state voltage: to find the best trade-off between these two parameters (specific on-resistance and breakdown voltage) is one of the major challenges in this voltage range. Recently, numerous researches have been done about the superjunction principle and about the way to realize it. Indeed, this principle allows to overcome the “breakdown voltage/on-state resistance” trade-off. This technology was chosen in particular by Infineon for the realization of COOLMOS™ transistors [1] and by STMicroelectronics for the realization of MDMESH™ devices [2]. However, the manufacturing cost of this technology can be very high because the process requires a multiple epitaxy technique, resulting in a significant number of masks. The deep trench technology [3] is a lower cost alternative with only one epitaxial step. Like all power devices, it needs an adapted junction termination technique to reach the highest breakdown voltage. Several junction termination techniques are available [4]-[6] but our attention

has stopped on the deep trench termination, which seems the most adapted termination for this technology. Indeed, one can notice that the junction termination area is dramatically decreased compared to conventional junction terminations in this voltage range.

This paper presents in a first part the structure of the Deep Trench SuperJunction Diode (DT-SJDiode) and its associated termination, the Deep Trench Termination (DT²). The second part is focused on the Deep Trench Termination parameters in order to obtain the best efficiency in terms of breakdown voltage. Finally, we will present an improvement of the termination that allows an electric field reduction at the critical point and consequently the increase in the breakdown voltage.

II. STRUCTURE DESCRIPTION

A cross-sectional view of the proposed DT-SJDiode is presented in Figure 1. It is based on elementary cells allowing the implementation of the superjunction principle [7], i.e. an alternation of N and P regions in the volume. To ensure the maximal breakdown voltage, the superjunction is protected in periphery of the active zone by means of a guarding technique developed in the laboratory. We use a dielectric filled wide and deep trench with a field plate on top. The use of deep trenches allows to avoid a multi-epitaxy technology. The P⁺ region is realized on the trench sidewalls from boron doping by Plasma-Immersion Ionic Implantation (PIII) [8]. The dielectric used is the BCB (Cyclotene 4026-46) [9] whose electrical parameters (critical field of 5.3 MV.cm⁻¹ and dielectric constant of 2.65) allow to ensure the efficiency of the junction termination.

The charge balance between N and P regions is important for the proper functioning of the superjunction and thus for the obtaining of an optimal breakdown voltage. Equation (1) recalls this balance in the case of constant doping profiles. Couples (W_N ; N_D) and (W_P ; N_A) represent the widths and the doping concentrations of N and P regions respectively:

$$W_N \cdot N_D = W_P \cdot N_A \quad (1)$$

To maintain the charge balance, the termination also needs to have a boron implantation on the trench sidewall as shown in Figure 1.

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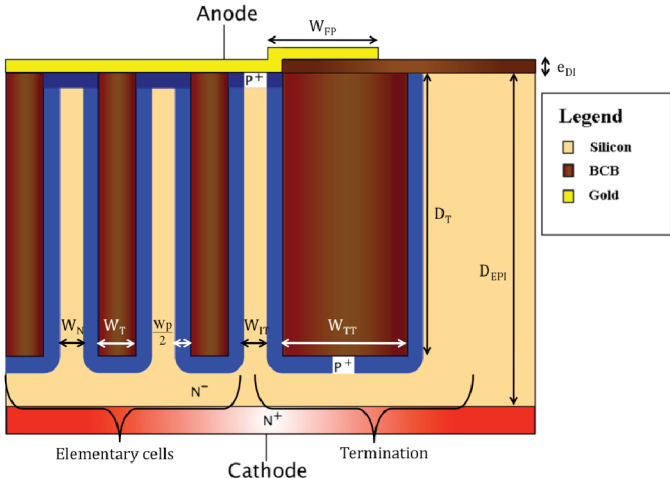


Fig. 1. Schematic cross-section of the DT-SJDiode with its Deep Trench Termination (DT²).

A single elementary cell of the DT-SJDiode exhibits a theoretical breakdown voltage of 1350 V. This value was obtained using the same methodology as the one presented in [10]. The corresponding parameters are listed in Table 1. We will use that breakdown voltage as a reference to evaluate the efficiency of the termination. Indeed, the termination efficiency is the ratio between the ideal breakdown voltage (1350 V in this case) and the breakdown voltage achieved with the termination.

TABLE I.
PARAMETERS OF THE SIMULATED STRUCTURE

Parameters	Symbols	Optimal values
N ⁻ epitaxial region doping concentration	N _D	3 × 10 ¹⁵ cm ⁻³
Implanted P-dose	P-Dose	10 ¹² cm ⁻²
Distance between two central trenches	W _N	6.5 μm
P-region width	W _P	1 μm
Central trench width	W _T	6 μm
Trench depth	D _T	80 μm
Distance between the last central cell and the termination	W _{TT}	6.5 μm
Breakdown voltage	BV	1350 V

III. ANALYSIS OF THE TERMINATION EFFICIENCY

A. Identification of simulation parameters

The deep trench termination is characterized by the following geometrical parameters: the depth D_T and the width W_{TT}, the length of the field plate W_{FP} and the thickness of the passivation layer e_{DI} (see Figure 1). D_T is imposed by the depth of the elementary cells trenches: a smaller D_T induces a charge unbalance, thus decreasing the breakdown voltage; a higher D_T is not useful because the termination efficiency does not increase. D_T is fixed to 80 μm. We focus on the influence

of the other geometrical parameters. For all the simulations, a 50 μm region of dielectric is added on the top of the structure. Indeed, it is important to study the electrical phenomena occurring on the top of the device for optimizing efficiently the design of the termination. Two limiting criteria are chosen: a leakage current of 10⁻⁷ A, corresponding to the avalanche breakdown, and an electrical field of 3 MV.cm⁻¹, above which value, arcing can occur between the field plate and the termination edges, leading to the destruction of the component.

B. Identification of critical points

There are two critical points in the structure as schematized on Figure 2. The first one is located at the edge of the field-plate (point A) where the potential lines shrink, inducing a maximal electric field, compared to the rest of the structure. The point B represents the place where the avalanche phenomenon appears, especially if the length of the field plate is small. Indeed, the purpose of the termination is to distribute the electrical potential lines in the dielectric in order to approach the ideal breakdown voltage. If the field plate is not long enough, the electrical potential lines are concentrated close to the silicon, thus increasing the electrical field and finally inducing a premature avalanche breakdown.

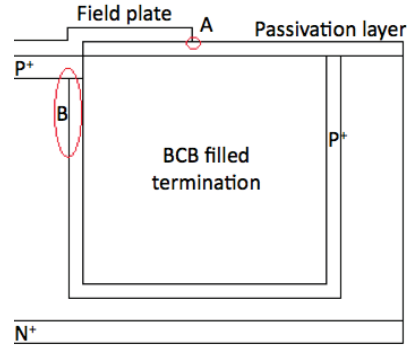


Fig. 2. Schematic view of the critical points for the breakdown.

C. Influence of the geometrical parameters

We have first studied the influence of the field-plate length on the breakdown voltage for various termination trench widths, as shown on Figure 3.

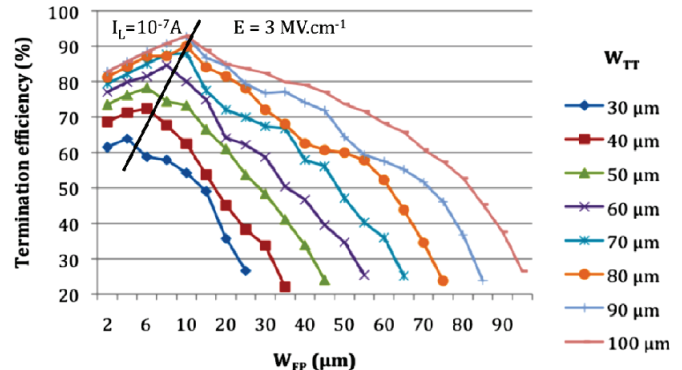


Fig. 3. Termination efficiency as a function of W_{FP} for various values of the termination trench width W_{TT}.

Increasing W_{TT} increases the breakdown voltage. For W_{FP} fixed at $10\ \mu\text{m}$ and for W_{TT} values varying from $30\ \mu\text{m}$ to $70\ \mu\text{m}$, the efficiency increases from 55 % to near 90 %. Above $80\ \mu\text{m}$, the termination efficiency can reach and exceed 90%. However the efficiency increase is not significant: so the optimal value for the termination width is $80\ \mu\text{m}$. We can also see on Figure 3 that there is an optimal value of W_{FP} , depending on W_{TT} . At first, increasing W_{FP} increases the breakdown voltage until an optimal value. More the edge of the field plate is close to the last central cell, more the breakdown is premature. However, increasing W_{FP} has a negative impact on the electric field because of the reduction of the potential lines spacing as shown on Figure 4.

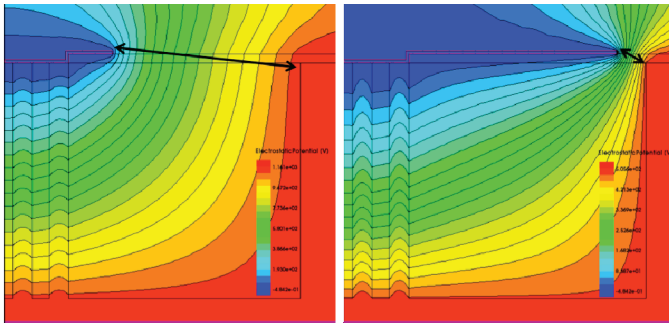


Fig. 4. 2D-simulated electrostatic potential distribution in the deep trench termination for $W_{FP} = 10\ \mu\text{m}$ (on the left) and $W_{FP} = 70\ \mu\text{m}$ (on the right).

The consequence is an increase in the electrical field at point A, as it can be seen on Figure 5. Indeed, all simulations here stop because the electric field at the end of the field plate reaches the limiting value of $3\ \text{MV}\cdot\text{cm}^{-1}$ which is destructive for the component.

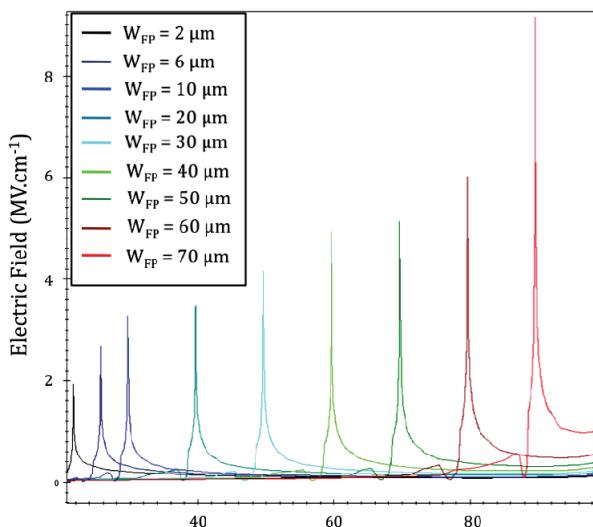


Fig. 5. Electric field at point A for various values of W_{FP} .

Figure 6 shows the influence of the dielectric thickness on the termination efficiency for $W_{TT} = 80\ \mu\text{m}$ and $W_{FP} = 10\ \mu\text{m}$. Increasing the BCB thickness does not permit an increase in the breakdown voltage because it decreases the electric field at point A and the limiting parameter is the leakage current for

this point. However, the presence of dielectric is necessary for preventing arcing between the field plate and the termination edges. It can be noticed that there is a slight drop of the efficiency when e_{DI} increases. Indeed, increasing e_{DI} strays the field plate and reduces its effect.

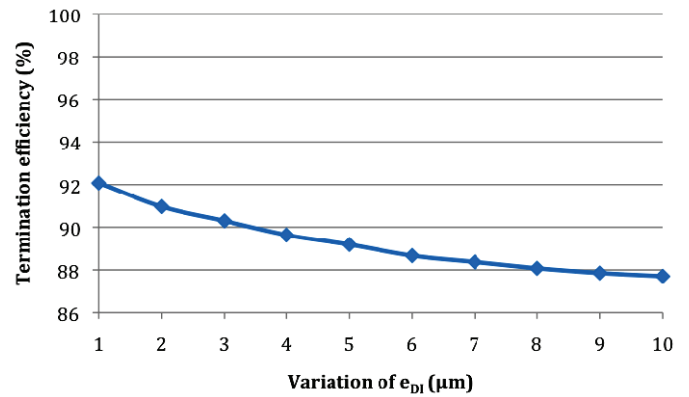


Fig. 6. Variation of the termination efficiency with the dielectric thickness e_{DI} for $W_{TT} = 80\ \mu\text{m}$ and $W_{FP} = 10\ \mu\text{m}$.

Finally, the geometrical parameters values that provide the best “efficiency/size” trade-off are $W_{TT} = 80\ \mu\text{m}$, $W_{FP} = 10\ \mu\text{m}$ (the field plate length depending on the termination trench width) and $e_{DI} = 1\ \mu\text{m}$.

IV. IMPROVEMENT OF THE TERMINATION

A. Description of the new design

In order to improve the efficiency of the termination and to decrease the electric field at point A, we propose to add a thickness of dielectric e_{DI-FP} only under the field plate as illustrated on Figure 7.

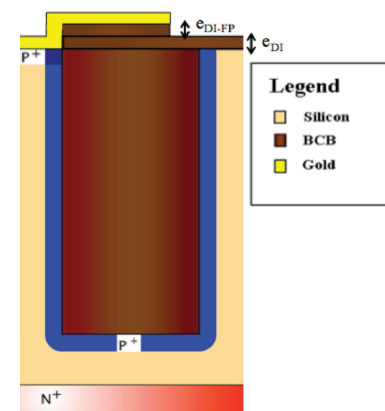


Fig. 7. Schematic cross-section of the improved termination.

Here, we use BCB for this layer because it can be easily integrated in the fabrication process. The stair-step allows a better potential distribution. Simulation results with only the electrical field as a limiting criteria are presented on Figure 8: with the new design, the electric field at point A is significantly reduced, from $4.2\ \text{MV}\cdot\text{cm}^{-1}$ to $2.5\ \text{MV}\cdot\text{cm}^{-1}$, thus preventing arcing.

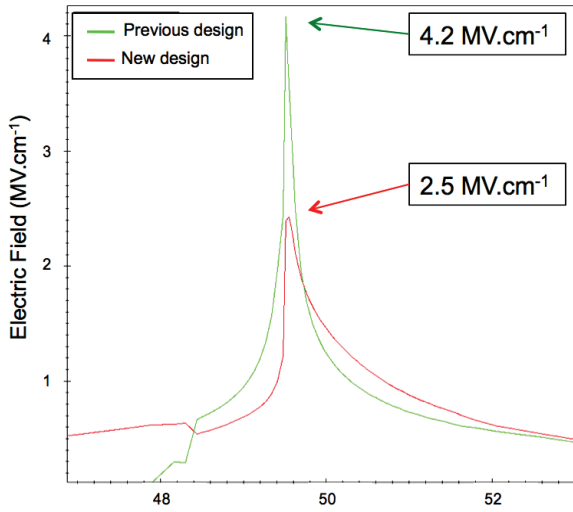


Fig. 8. Electric field at point A for the previous and the new design of the termination.

Figure 9 compares the evolution of the termination efficiency as a function of the field plate length W_{FP} for two structures: the one with dielectric above the whole junction termination as schematized on Figure 1 (previous design) and the other with an added BCB dielectric only under the field plate (new design shown on Figure 6). The BCB thicknesses ϵ_{DI} and ϵ_{DI-FP} are fixed at $1 \mu\text{m}$ and the termination width is fixed at $80 \mu\text{m}$.

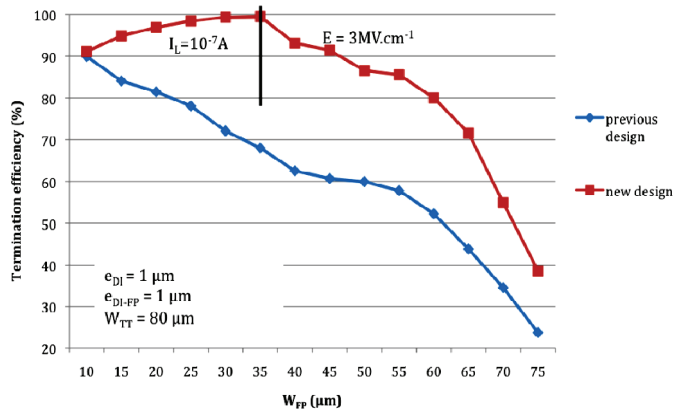


Fig. 9. Influence of the structure design on the termination efficiency as a function of the field plate length W_{FP} .

The new structure allows to reach almost 100 % of the termination efficiency. For $W_{FP} < 35 \mu\text{m}$, there is an avalanche breakdown occurring at point B which is not destructive for the device. For $W_{FP} > 35 \mu\text{m}$, the electrical field reaches 3 MV.cm^{-1} at point A before the avalanche phenomenon at point B. Thus, there is an optimal value of W_{FP} which is $35 \mu\text{m}$.

In this new design, the BCB thickness under the field plate, ϵ_{DI-FP} , has an impact on the electrostatic potential lines distribution. Indeed, increasing this layer extends the area of the potential distribution and reduces slightly the electric field at point A. However, it changes the electrostatic potential distribution in the corner of the last elementary cell, inducing

an increase in the electric field at point B and leading to a premature breakdown voltage. Figure 10 presents the electric field and electrostatic potential line distributions at points A and B for 2 values of ϵ_{DI-FP} : $1 \mu\text{m}$ and $5 \mu\text{m}$.

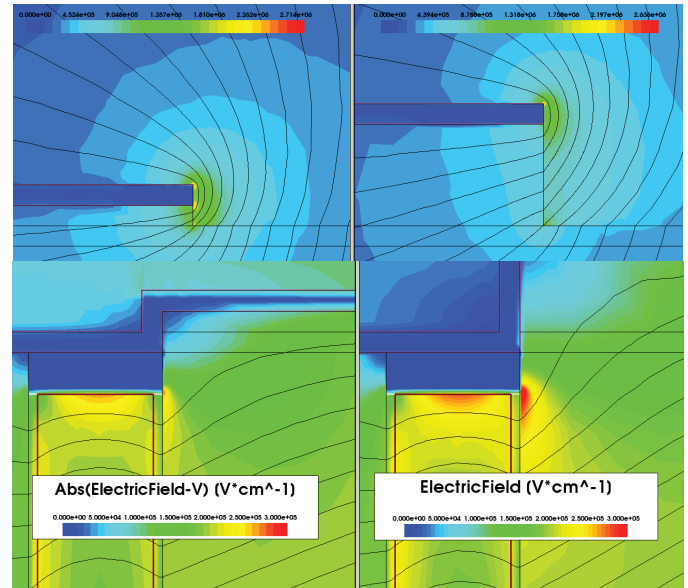


Fig. 10. Electric field at point A (on the top) and at point B (on the bottom) for $\epsilon_{DI-FP} = 1 \mu\text{m}$ (on the left) and $\epsilon_{DI-FP} = 5 \mu\text{m}$ (on the right)

Figure 11 represents the termination efficiency evolution as a function of W_{FP} for various values of ϵ_{DI-FP} : the maximum termination efficiency is the same whatever ϵ_{DI-FP} . Note that all the simulations stopped because of the leakage current. For each curve, increasing W_{FP} beyond the maximal value represented on Figure 9 means a drop of the efficiency due to the electric field reaching 3 MV.cm^{-1} .

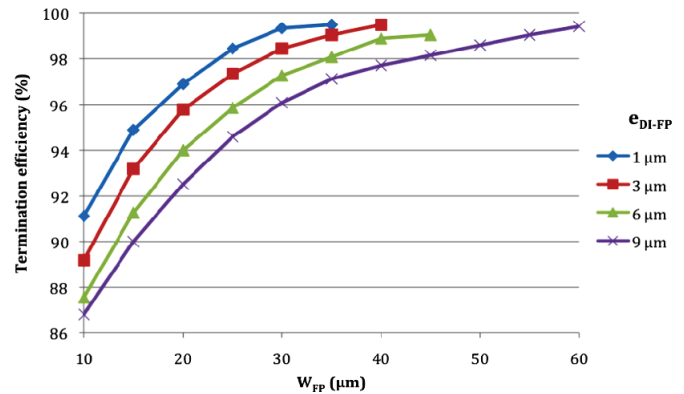


Fig. 11. Termination efficiency as a function of the field plate length W_{FP} for various values of ϵ_{DI-FP} .

B. 3D Simulations

3D simulations have been performed in order to verify the efficiency at the edges of the device. Indeed, it is well-known that cylindrical and spherical junctions induce premature breakdown [11]. A schematic top view and a 3D view of the simulated structure are reported on Figure 12.

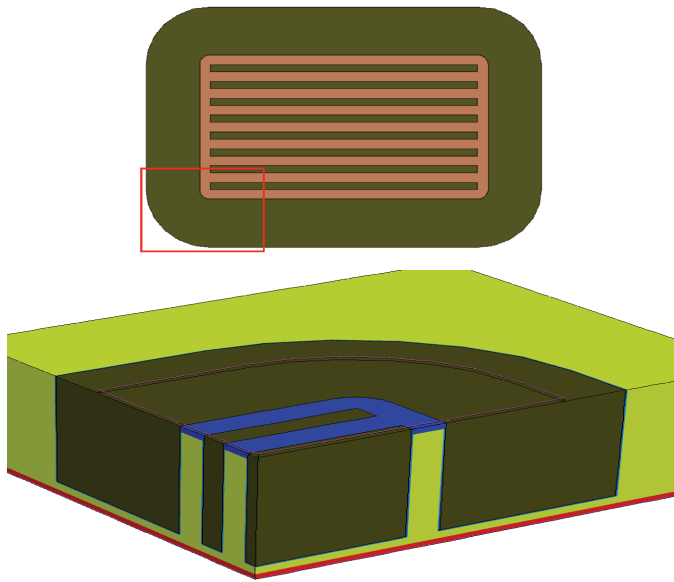


Fig. 12. Schematic top view and 3D view of the simulated structure.

In 2D, the distance between the termination and the last elementary cell must be equal to the distance between two elementary cells in order to maintain the charge balance. In the case of 3D simulations and with the optimized parameters reported in Table 1, a premature breakdown occurs because there is an unbalance charge in the regions located at the corners of the rectangular elementary cells. This phenomenon is illustrated on Figure 13 that shows the repartition of the impact ionization: in 3D, the equation (1) is no more valid because it is necessary to encompass the volume. The equation of the charge balance becomes the following one :

$$V_N \cdot N_D = V_P \cdot N_A \quad (2)$$

Couples $(V_N ; N_D)$ and $(V_P ; N_A)$ represent the volumes and the doping concentrations of N and P regions respectively.

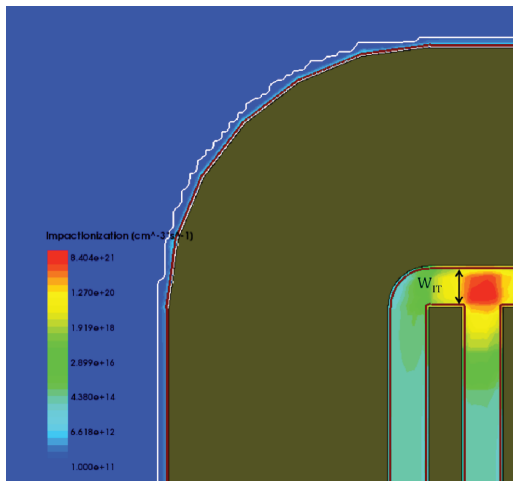


Fig. 13. Cross-section of the 3D simulated structure showing the point where the avalanche phenomenon occurs. The colors represent the impact ionisation distribution.

The 3D-simulated breakdown voltage is 71% of the maximal breakdown voltage related to central cells without correction. According to equation (2), the four parameters involved are key parameters for the charge balance. In our case, the P sidewall regions are realized by ionic implantation, so the term “ $V_P \times N_A$ ” can not be changed. In the same way, N_D can not be changed. The only parameter we can act on is W_{IT} , i.e. the spacing between the elementary cells and the termination at the corner side (see Figure 13), which parameter the V_N volume depends on. From equation (2), it results that the optimal W_{IT} value for obtaining the charge balance is approximately $4.5 \mu\text{m}$. In order to optimize W_{IT} , the leakage current is the only one limiting criterion used for the 3D simulations. Starting from a W_{IT} value of $6.5 \mu\text{m}$, we have studied the termination efficiency variations when reducing W_{IT} . It can be seen on Figure 14 that a W_{IT} decrease allows to approach the charge balance and so to obtain a better termination efficiency. However, a W_{IT} decrease unbalances the charge in the corner of the termination. Thus, there is an optimal value of W_{IT} to obtain the better termination efficiency. A $2 \mu\text{m}$ W_{IT} reduction improves the breakdown voltage and the termination efficiency becomes equal to 97 %.

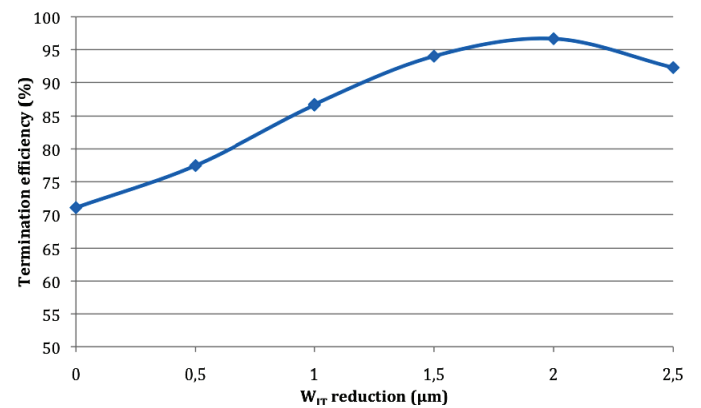


Fig. 14. Termination efficiency as a function of various values of W_{IT} reduction.

V. TECHNOLOGICAL PROGRESS

Before fabricating superjunction power devices with the new design, several critical technological steps were optimized as the control of trench verticality by dry etching, filling of the deep and wide termination trench with a dielectric (Figure 15) . L. Théolier [4] developed a process for trench BCB filling with two successive deposition steps. In a previous paper [10], we have presented an optimization of the trench filling with only one deposition step by spin coating as shown on Figure 15, thus simplifying the technological process. However, around $30 \mu\text{m}$ of BCB is still remaining on the top surface of the wafer. To eliminate this over-thickness, the use of Dry Reactive Ion Etching (DRIE) has been envisaged. To do that, it is first necessary to optimize the planarization of the BCB layer because of its non-uniform thickness over the wafer: a gap of $15 \mu\text{m}$ is observed between the thicknesses measured above the central cells and the termination. The planarization step development is still on going.

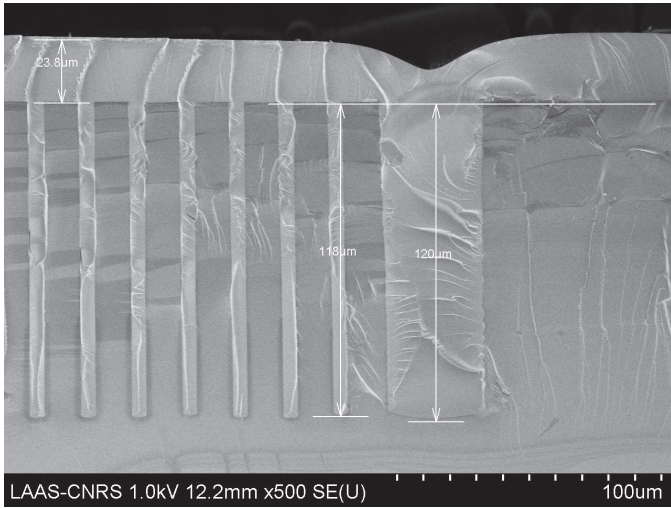


Fig. 15. Deep trenches fulfilled with only one BCB deposition whatever their width [10].

Another technological critical point is the alignment between the edge of the field plate and the dielectric stair-step. We have simulated its impact on the termination efficiency (Figure 16) for the optimal field plate length of 35 µm: positive values of the alignment variation correspond to a field plate length higher than the dielectric stair-step length. If the alignment is not perfect (i.e. different to zero), the termination efficiency is reduced and the new design is not efficient. The impact of the added dielectric layer is significant only near to the perfect alignment, between -1 µm and zero. Outside of this range, the distribution of the potential lines act as if there was not the dielectric stair-step.

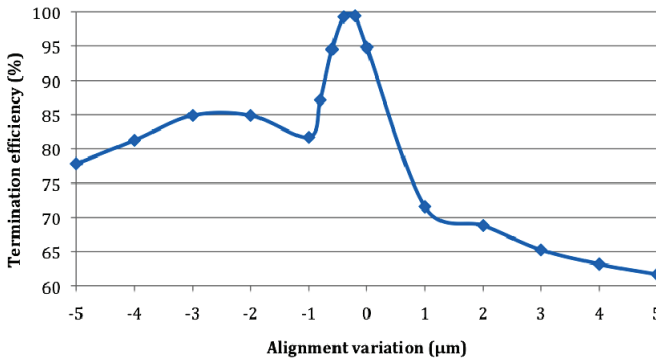


Fig. 16. Variation of the termination efficiency as a function of the alignment variation.

In order to obtain a perfect alignment, it will be necessary to etch both field plate metal and BCB layers successively using the same photoresist mask.

It is also interesting to study the influence of the dry etching anisotropy of the added BCB stair-step layer on the termination performances. We reported on Figure 17 the variations of the termination efficiency as a function of the BCB edge profile variations on both sides of the zero point, which corresponds to a perfect vertical profile: negative values correspond to a negative wall profile.

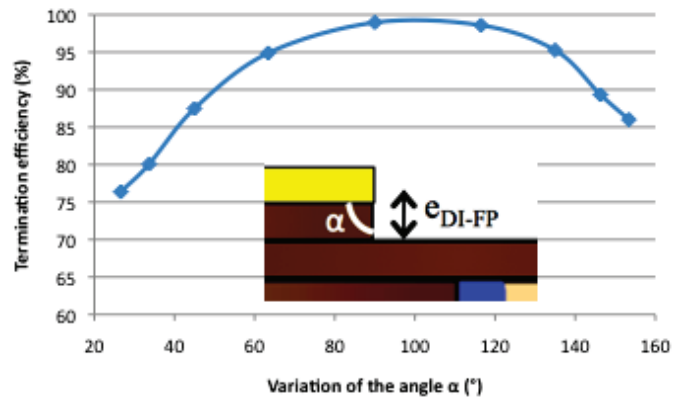


Fig. 17. Termination efficiency as a function of the stair-step edge profile.

The best termination efficiency is obtained when the stair-step edge is vertical. However, for a profile variation of +/- 0.5 µm (positive or negative wall profile respectively), the termination efficiency is still higher than 95% which is a satisfactory value: so it is not necessary to aim towards a perfect verticality for the BCB stair-step profile. First results for BCB dry etching with a SF₆/O₂ plasma are reported on Figure 18: etching is not anisotropic, leading to a positive BCB wall profile.

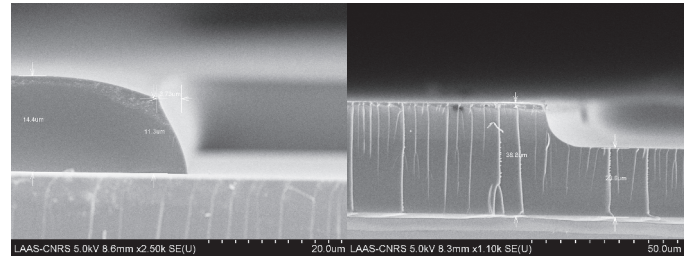


Fig. 18. Slope of the photoresist profile used as a mask (on the left) and BCB profile after plasma etching (on the right)

VI. CONCLUSION

In this work, we have proposed a new Deep Trench Termination design allowing the realization of deep trench superjunction devices (diodes and MOS transistors) for 1200 V applications. 2D and 3D simulations have permitted to evaluate the influence of the geometrical parameters on the termination efficiency. Increasing the field plate length W_{FP} has a negative impact on the breakdown voltage because it tightens the potential distribution: breakdown is always located at the end of the termination, which is destructive for the component. A modification of the structure was proposed to improve the efficiency until almost 100% and to allow a non destructive avalanche breakdown phenomenon.

The new design consists of the addition of a dielectric layer under the field plate thus allowing a better potential distribution. However, for the fabrication process, it is necessary to have a perfect alignment between the end of the field plate and the BCB stair-step. First technological studies have been presented. 3D simulations permit to highlight a charge balance issue at the corners of the elementary cells and to optimize the structure design. The realization of DT-SJDiode is on going.

ACKNOWLEDGMENT

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modeling, realization and characterization of silicon (VDMOSFETs, trench MOSFETs, Floating Islands MOSFETs and Deep Trench SuperJunction MOSFETs) and gallium nitride (MOSFETs and HEMTs) power devices. He has authored and coauthored 35 papers in scientific journals and over 70 papers in international conferences.

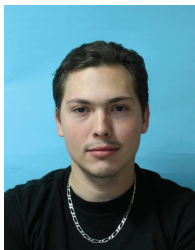


Josiane Tasselli received her Ph.D. degrees in electrical engineering in 1986 from the University of Toulouse, France. At LAAS-CNRS since 1988, her research concerned the fabrication of III/V heterojunction bipolar transistors for power applications, the design and fabrication of microfluidic devices for chemical engineering applications and the study of new 3D integration techniques. Since 2012 she is involved in the development of silicon and wide band-gap power devices for energy management.



Karine Isoird was born in Sète (France) in 1973. Her Ph.D. degree received in 2001, focused on the characterisation of high temperature and high voltage SiC power device. Since 2003, she is assistant professor at University Paul Sabatier of Toulouse and she has integrated ISGE team (Integration of Systems for Energy Management) within LAAS lab. Her activities research focus on the simulation, design and electrical characterisations of high voltage and high temperature power devices both in silicon, or wide band gap material. Indeed in recent years, she has

been involved in several projects for the design and realisation of devices dedicated to high voltage and high temperature applications, such as Thyristor, GaN HEMT or diamond Schottky diodes. She is co-authors of 27 publications in scientific journals and 20 in international conferences. Member expert to OMNT (Observatory for Micro and Nano Technology), on the topic Wide band gap Materials.



Sylvain Noblecourt was born in France in 1986. He received a Master of Science degree in Micro and Nano Systems from Paul Sabatier University in Toulouse (France) in 2011 and a second one in Training for higher education from the École Normale Supérieure in Cachan (France) in 2012. To date, he is pursuing his Ph.D. degree within the LAAS laboratory, in the field of power device electronics. His thesis is focused on the optimization and realization of deep trench superjunction power devices.



Patrick Austin received the Master degree and the Ph.D. degree in microelectronics engineering from the « Université de Toulouse » (Université Paul Sabatier), France, in 1988 and 1993 respectively. From September 1995 to August 2004, he was Assistant Professor at the « Université de Toulouse » and researcher at LAAS-CNRS. Since September 2004, he is Professor at the « Université de Toulouse ». His current research interests are in the modeling and conception of power semiconductor structures based on functional integration concept.