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Frank Torregrosa, Guillaume Sempere, Werner Schustereder, Philippe Godignon, Yohann Spiegel, et al.. Advantages and challenges of Plasma Immersion Ion Implantation for Power devices manufacturing on Si, SiC and GaN using PULSION<sup>®</sup> tool. 22nd International Conference on Ion Implantation Technology (IIT), Sep 2018, Würzburg, Germany. 5p., 10.1109/IIT.2018.8807978 . hal-01955688

**HAL Id: hal-01955688**

**<https://laas.hal.science/hal-01955688>**

Submitted on 14 Dec 2018

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# Advantages and challenges of Plasma Immersion Ion Implantation for Power devices manufacturing on Si, SiC and GaN using PULSION<sup>®</sup> tool

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**Abstract**—Thanks to its high throughput and low cost of ownership Plasma Immersion Ion Implantation (or Plasma Doping) has been widely used for Memory device fabrication. Its ability to implant very high doses in shallow layers, makes it a perfect tool for new material modification applications needed for advanced logic devices. Nevertheless, few works are reported for its uses in power device fabrication. The aim of this paper is to present several application cases where we studied the use of our PULSION<sup>®</sup> PIII tool for implantation in Silicon, Silicon Carbide and Gallium Nitride power devices. Benefits of PIII and challenges to overcome will be discussed for the following applications in silicon devices: High dose phosphorus and boron implantation for polysilicon gate doping and low dose doping of deep trench superjunction applications, contact plug doping for Silicon SFET devices and wall doping of deep shallow trenches for IGBTs. In addition possible applications for wide band gap materials will be discussed with an example of doping application for GaN HEMT, where PIII allowed to make the first demonstration of a normally-off device. Finally some doping and material modification applications on SiC are presented.

**Keywords**— Ion Implantation, Plasma Immersion Ion Implantation, Plasma Doping, Power devices

## I. INTRODUCTION

Thanks to its ability to implant high doses at low energy with a high throughput and no risk of high energy contamination, Plasma Immersion Ion Implantation (PIII) or Plasma Doping (PLAD) has been widely used, since 2005, in memory application for DRAM poly counter doping or contact doping [1-3]. The ability to also make 3D implant and to reach high surface concentration also opened new applications for logic devices fabrication (FinFET doping, Material modification application for Vth Tuning or etch stop

application) [4,5]. Despite all the advantages of PIII, nearly no work was reported in the literature for power devices applications. In this paper, thanks to the collaboration of several industrial and academic partners, we tested the efficiency of the PIII tool from IBS (named PULSION<sup>®</sup>) to address several challenging applications for Si power devices manufacturing where beam line tools were not technically or economically efficient:

## II. DOPING APPLICATION EXAMPLES FOR SILICON POWER DEVICES

### A. Poly doping for CoolMOS (INFINEON / IBS collaboration)

MOS and IGBT power devices are still using doped polysilicon for their gate stack. Initially doped using diffusion processes (PoCl<sub>3</sub> for N-Channel and BBr<sub>3</sub> for P-Channel MOSFETs), this process is progressively being replaced by Ion Implantation for a better homogeneity and reproducibility as well as for environment friendly considerations. But, the required doses are high (some E16/cm<sup>2</sup>) and even if the needed implantation energies are higher than for DRAM applications due to the thicker poly-Si thickness (generally around 400nm to 800 nm), throughput of the implantation process is still something to be improved.

As for DRAM or CMOS applications [1, 6], PIII, could be an efficient solution to benefit from the advantages of the ion implantation processes while keeping a high throughput and a low cost of ownership. But, due to its limitation in implantation energy (most of the available tools are limited to 10kV), the subsequent diffusion/activation process must be optimized to allow the dopants to diffuse through all the poly-Si and to reach a high enough concentration near the SiO<sub>2</sub> gate

interface to minimize depletion phenomena while avoiding dopant out-diffusion, implementing cap layers or oxidation steps in the thermal process.

Table 1 presents best results obtained on a 600 nm LPCVD PolySi deposited on SiO<sub>2</sub>, and submitted to PIII Implantation at 8 kV with doses ranging from 1E16 to 1E17/cm<sup>2</sup>, followed by a 30 min annealing step under argon, with and without oxidation steps. For Phosphorus doping PH<sub>3</sub> plasma was used, annealing temperature was ranging from 830°C to 1100°C. For Boron doping, BF<sub>3</sub> plasma was used and annealing temperature was ranging from 1050°C to 1140°C.

As can be seen, targeted values (about 10 Ω/sq for Phosphorus doping and 20 Ω/sq for boron doping) were nearly reached with respectively 11.1 Ω/sq and 23.4 Ω/sq.

TABLE I. Sheet resistance values obtained on a 600 nm Poly-Si on SiO<sub>2</sub> using PIII Phosphorus and Boron doping followed by optimized annealing process.

Poly Si Doping by PIII for CoolMOS devices		
PIII Implantation	Targeted sheet resistance (Ohm/sq)	Lowest obtained sheet resistance (Ohm/sq)
N type doping with Phosphorus PH <sub>3</sub> PULSION implantation + Annealing	≈ 10 Ω/sq	11.1 Ω/sq
P type doping with Boron BF <sub>3</sub> PULSION implantation + Annealing	≈ 20 Ω/sq	23.4 Ω/sq

We calculated that the use of PULSION Tool for this process could allow a reduction of the Cost of Ownership by a factor higher than 2 compared to the beam line process of record used at INFINEON.

#### B. Contact doping for SFET (INFINEON / IBS collaboration)

As for memory and logic devices, high surface concentration obtained using PIII is likely to reduce contact resistance and to be cost efficient compared to low energy BL implantation. [7]

New generations of SFET devices developed at INFINEON require an efficient p-type contact doping at the bottom of always narrower groove contact structures. In this study we compared PULSION doping using BF<sub>3</sub> plasma with Beam Line (BL) implantation using BF<sub>2</sub><sup>+</sup>. For BL implantation, energy was ranging from 10 to 25 keV and doses from 1E15 to 3E15 /cm<sup>2</sup>. For PIII, we used acceleration voltages from 5 to 10 kV and machine doses (including F<sup>+</sup> ions) from 2E15 to 6E15/cm<sup>2</sup>. The test was performed on different pitch size real devices without changing any other process steps. Electrical characteristics of the devices (V<sub>th</sub>, DiBL, conductance, body lateral resistance) were then measured and compared. Main conclusions were :

- Whatever the pitch size, PIII implantation gives electrical performance in the same range than the process of reference (using beam line) but with a clearly lower DiBL at the same V<sub>th</sub> (see fig 1)
- PIII allows less dispersion in electrical characteristics than BL

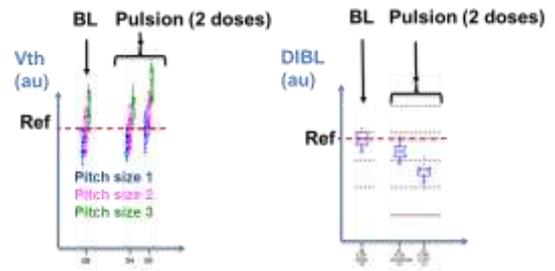


Fig. 1. V<sub>th</sub> and DiBL electrical results on SFET devices showing best performance (same V<sub>th</sub>, lower DiBL) on PIII implanted samples)

#### C. Trench doping for IGBT (INFINEON / IBS collaboration)

Thanks to its capability to do 3D doping, PIII process is likely to implant the wall of deep trenches needed for power device fabrication [7]

In order to reduce the R<sub>ds(on)</sub> of the MOSFET portion of the IGBT, a trench gate structure has been adopted 10 year ago by most of the suppliers: the gate oxide and conductive polysilicon gate electrode are formed in a deep (about 5μm) narrow trench below the chip surface and allow a higher cell current density while eliminating the “parasitic JFET effect” [8] , Development of new IGBT generations might require shallow trenches associated with uniform p-type doping within the trench. As this is likely impossible to be obtained using BL ion implantation, we checked the ability of PULSION tool to dope the walls of such trenches using BF<sub>3</sub> or B<sub>2</sub>H<sub>6</sub> plasma. Wall doping uniformity was checked using SSRM after annealing (see example on figure 3). Results validated the ability of PIII to be used to dope such trenches, work is still going on to optimize process parameters and process integration on real devices.

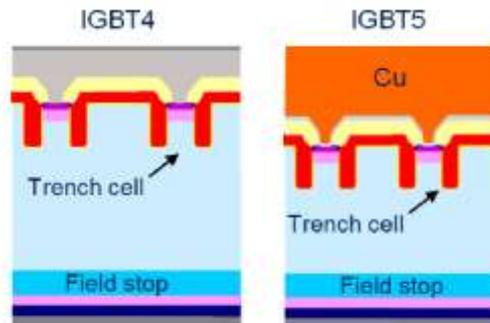


Fig. 2. Schematic of trench IGBTs

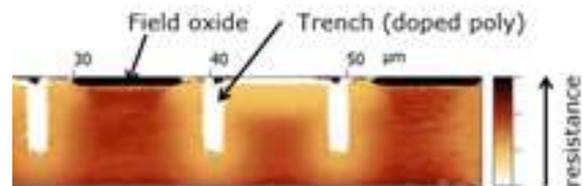
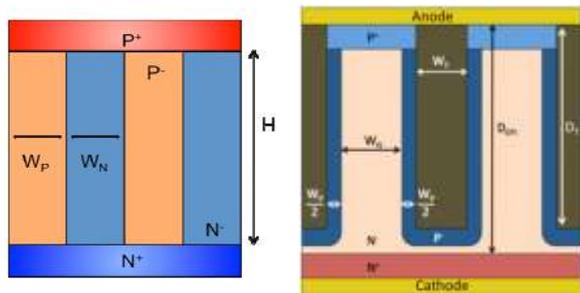


Fig. 3. SSRM of a trench-IGBT with PIII implanted trenches.

#### D. Low dose Trench doping for superjunctions (LAAS / IBS collaboration)

Superjunctions have been introduced by ST-MICROELECTRONICS and INFINEON few years ago to improve the ON state resistance of MOSFET devices. It consists in alternation of N and P vertical layers in the drift zone of the devices (see fig. 4). Nevertheless the fabrication of this structure is complex and requires multiple EPI steps. A proposed cost effective solution is to replace these multiple EPI layer by a single N type layer with deep trenches doped all around by P type implantation [10]. Breakdown Voltage depends on the size of the trenches as well as on the fine equilibrium between the N EPI and P implanted dopants. For 600V to 1200V devices, the depth of the trenches must be respectively around 30 $\mu\text{m}$  and 70 $\mu\text{m}$  with a form factor above 10:1. Doping these structures by BL implantation is thus a challenge and PIII appears to be a good candidate.



a-Schematic of a diode with standard EPI superjunction structure  
b-Schematic of diode with ion implanted deep trenches superjunction structure

Fig. 4. Schematic of standard and implanted trenches superjunction structures..

Thanks to a collaboration with LAAS/CNRS laboratory, we demonstrated that PULSION implantation of BF3 followed by thermal annealing was efficient to obtain a conformal junction of about 0.8  $\mu\text{m}$  deep around the deep trenches (see fig. 5).

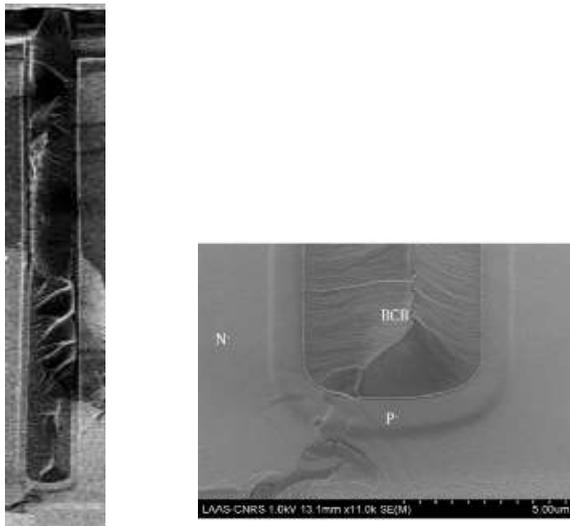


Fig. 5. Chemical staining of PULSION implanted P+ junction around a deep trench for superjunction application.

Nevertheless, the optimal boron dose to allow a good breakdown voltage is around  $1\text{E}12/\text{cm}^2$  and the breakdown voltage is really sensitive to any variation of this dose. To be

compatible with this application a dose reproducibility of few  $\text{E}10/\text{cm}^2$  is required, which still is a challenge for PIII tools.

### III. DOPING APPLICATION EXAMPLES FOR WIDE BAND GAP (SiC & GAN) POWER DEVICES

#### A. Channel mobility improvement on SiC MOSFET (IBS / CSIC)

SiC MOSFET devices are excellent power devices due to high breakdown electric field, high saturation velocity and high thermal conductivity. However, the excellent device characteristics expected from these physical properties have yet not been fully realized, due to the issues related to SiO<sub>2</sub>/SiC interface, leading in a poor channel effective mobility compared to the conventional crystal face (4H-SiC(0001)). [11]. To reduce the interface state density of SiC/SiO<sub>2</sub> interface, some specific treatment as N<sub>2</sub>O thermal oxidation or phosphorus oxide doping have been developed but some progress still need to be done.

In this study, we used PIII implantation of phosphorus to create a very thin and superficial layer of negative charges just below the gate to repulse the channel carriers from the SiC/SiO<sub>2</sub> interface and improve the carrier's mobility. Fig 6 show electrical results obtained on N-SiC MOSFET with N<sub>2</sub>O thermal gate oxide, with and without this PIII implantation. Phosphorus PIII implant allowed to significantly improve the effective channel mobility and increase the output current.

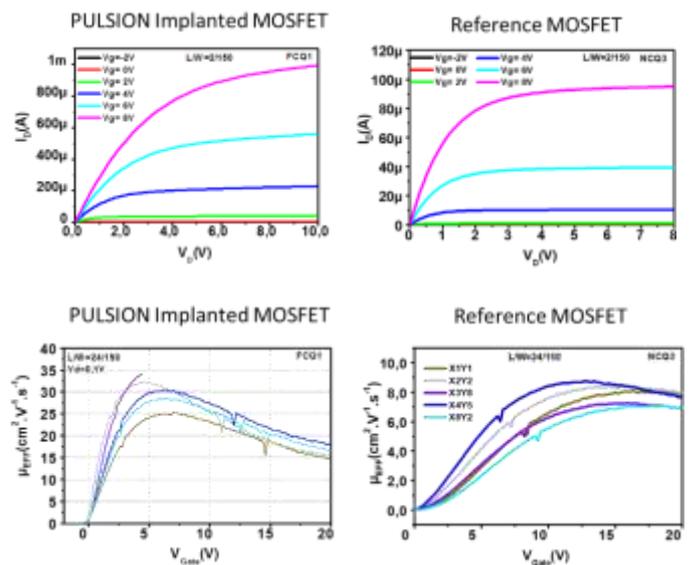


Fig. 6. Compared forward characteristics and extracted max. effective mobility of SiC MOSFET transistors with 2 $\mu\text{m}$  channel length : PIII implanted devices show a Drain current about 7x higher than reference devices for the same Drain and Gate voltages explained by a higher channel mobility.

#### B. Contact doping for SiC (IBS)

P-type doping in SiC is done using Aluminum ion implantation. As diffusion coefficient of Al in SiC is really small, multiple implantations at different energies are needed to obtain the desired doping profile. As the implanters used in SiC manufacturing are 150 mm medium current or high energy tools with limited capability in low energies, implanted profiles generally suffer from a reduced surface concentration

leading to a non-optimal contact resistance when surface concentration is lower than some  $E19/cm^3$  [12]. This situation can be efficiently improved by the use of an additional PIII implantation.

This is illustrated on fig 7 where we used PULSION tool to implant Al from TMA plasma on top of beam line multi energy implantations (from 30keV to 180 keV) a 3C-SiC. This allowed us to increase the surface concentration of Al from  $2E19/cm^3$  to  $1E20/cm^3$ .

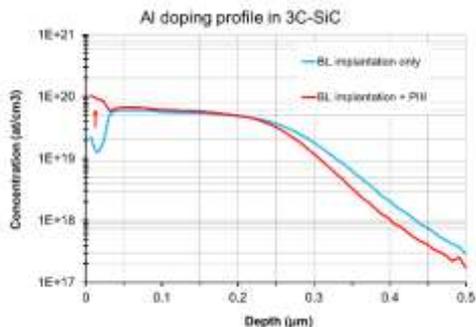


Fig. 7. SSRM of a trench-IGBT with PIII implanted trenches.

### C. PIII doping for normally-off GaN HEMT (LAAS/IBS)

Compared to silicon power devices, gallium nitride (GaN) High Electron Mobility Transistors (HEMTs) exhibit very interesting properties for power switching (reduced on-state resistance, operation at higher frequencies and temperatures), thus addressing the four difficulties of energy systems that are cooling, weight, bulk and efficiency. The major drawback of conventional HEMTs is that they are normally-on devices, exhibiting negative threshold voltages. However, many power applications require the use of normally-off switches, i.e. switches exhibiting positive threshold voltages.

A solution proposed by Hamady et al. [13] consists in introducing a P-doped GaN layer into the UnIntentionally Doped (UID) GaN layer, below the gate electrode, under the AlGaN / GaN interface (see fig. 8). One can note that the P-doping concentration of GaN has to be compensated on both sides of the gate region by incorporating N-types regions with a sufficiently high doping concentration to restore the electron current flow; without these N-GaN regions, the HEMT would be continuously blocked under the effect of the P-GaN region, whatever the voltage applied to the gate.

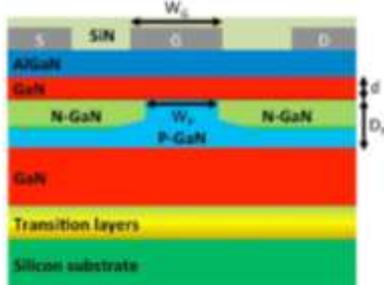


Fig. 8. Schematic cross-section of the new normally-off GaN HEMT proposed by Hamady et al. [13].

The fabrication technological process of this new device begins with the realization on a silicon substrate (111) of

successive epitaxies of the transition layers, the UID GaN layer and the P-GaN layer. Then comes the key step of the process which is the implantation of donors (silicon atoms) in order to realize the N-type regions. PIII appeared to be more suitable than conventional ion implantation since it allows high doses to be implanted at much lower energies, which reduces the depth of ion penetration and generates fewer defects. Thus, several PIII conditions combining different acceleration voltages (5 and 10 kV) and doses ( $10^{15}$  and  $10^{16} cm^{-2}$ ) were tested. The measurements confirmed the quality of PIII: the surface roughness remained stable and relatively low at around 1.8 nm RMS and the leakage currents of the devices appeared to be much lower than those of devices realized with conventional BL ion implantation whatever the implantation conditions.

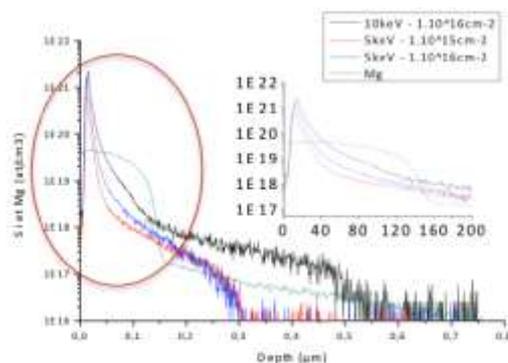


Fig. 9. SIMS profiles of silicon implanted GaN using PULSION allowing shallow and high concentration n-type layer above the p-type (Mg doped).

Fig. 10 shows the transfer characteristics  $I_d(V_{gs})$  on the reference GaN HEMT (conventional normally-on HEMT) and on the new GaN HEMT realized with PIII.

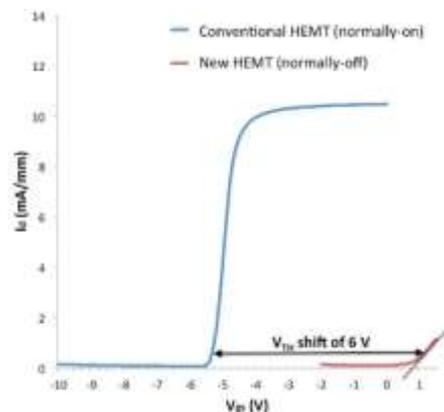


Fig. 10. Experimental transfer characteristics  $I_d(V_{gs}) @ V_{ds} = 1 V$  for the conventional normally-on HEMT and the new HEMT: 1st demonstration of a normally-off GaN HEMT thanks to PIII doping.

The measured threshold voltages of the two devices are respectively - 5.5 V for the reference and + 0.8 V for the new HEMT, which allows the experimental validation of the new concept proposed. Not only is the HEMT normally-off - even if the value of + 0.8 V would in practice be insufficient for power applications - but the offset of the threshold voltage, brought about by the introduction of the P-GaN region under the gate, is greater than 6 V, which is remarkable.

#### IV. MATERIAL MODIFICATION APPLICATION EXAMPLE FOR SiC EPI GROWTH IMPROVEMENT

The idea of using high dose carbon implantation into silicon crystal to form a compound semiconductor Silicon Carbide is present in the literature since early 70's [14]. Several potential advantages of ion implantation over other growth techniques were raised: high purity of crystal and implant; perfect control of implant dose and depth, finally relatively low process temperature. However, added to the fact that required doses were very high for BL implanters, even the most recent literature studies [15] report only about the formation of low structural quality, polycrystalline Silicon Carbide layers.

We investigated the possibility of using PULSION tool with a C<sub>2</sub>H<sub>2</sub> plasma to implant and/or deposit high dose of carbon (from 5E16/cm<sup>2</sup> to 5e17/cm<sup>2</sup>) on Si (100) substrate to form Si:C layer and convert it in a well oriented seed for epitaxial growth of 3C-SiC. The carbon treated samples were submitted to high temperature annealing in CVD reactor. Various annealing conditions were tested: atmosphere (flow of pure H<sub>2</sub>, H<sub>2</sub>/Ar or pure Ar), temperature (1250°C to 1400°C) and duration of annealing plateau (1min – 90min). Each annealing experiment was performed simultaneously on pieces of differently carbon treated substrates and on reference, bare Si (100) wafer. For epitaxy experiments a two-step growth process was applied. It was composed of annealing step followed directly by standard CVD step. The process didn't contain any carbonization (exposition to carbon precursor only) step. Epitaxy experiments were performed simultaneously on carbon treated samples, reference Si wafer and pieces of standard 3C-SiC/Si(100) template. Sample characterization by FTIR, SEM and XRD.

As illustrated on fig 10 and detailed in [16] we demonstrated that by combining PIII with high temperature annealing and by adjusting the annealing conditions we could tune the amount of created 3C-SiC. The formation of oriented seed under specific PIII / annealing conditions was confirmed by the fabrication of good quality 3C-SiC film on the seed.

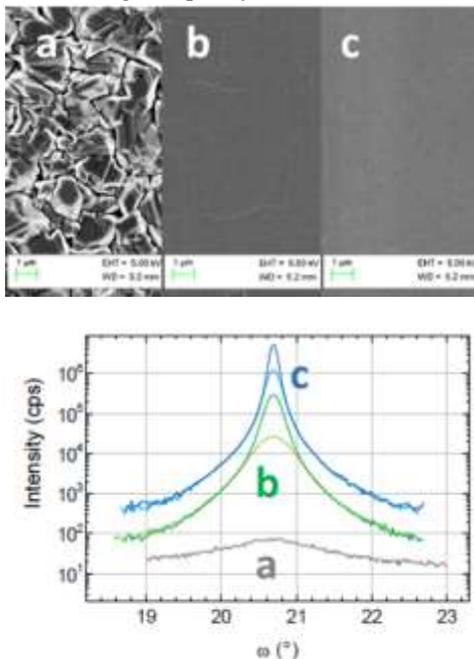


Fig. 11. SEM images and 3C-SiC(002) rocking curves of 1.3μm and 7μm thick EC-SiC epilayes grown on : a annealed Si(100) substrate, b-PIII treated sample, C 2μm 3C-SiC/Si template.

#### V. CONCLUSION

Thanks to its unique capability to implant high doses at low energy on planar or 3D structures and with high throughput PIII can offer unique and cost effective solutions to solve technical challenges encountered in advanced power devices fabrication. Using implantation of several species (B, P, Si, Al and C) on Si, SiC and GaN substrates, we demonstrated the efficiency PULSION® tool to improve characteristics of these power devices and to allow fabrication of new type of devices.

#### ACKNOWLEDGMENT (Heading 5)

The collaboration work between INFINEON and IBS on Si power devices has been done within the framework of European ENIAC and ECSEL projects EPPL and SEMI40.

The collaboration work between LAAS and IBS on superjunction doping has been performed with the support of the French ANR project SUPERSWITCH.

The collaboration work between NOVASIC and IBS on EPI growth improvement for 3C-SiC is supported by the European H2020 project CHALLENGE.

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