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Real-time Emulation of Boost Inverter Using the Systems Modeling Language and Petri Nets

A. Gutierrez¹⁻², M. Bressan¹, J.F. Jimenez¹⁻³, and C. Alonso²⁻³

¹*Universidad de los Andes, Department of Electrical and Electronic Engineering, Bogotá, Colombia*

²*Université de Toulouse III, UPS; Toulouse F-31400, France*

³*LAAS-CNRS, 7 Avenue du Colonel Roche, Toulouse F-31077, France*

Email: a.gutierrez75@uniandes.edu.co (A. Gutierrez), alonsoc@laas.fr (C. Alonso)

Abstract

A boost inverter is a versatile architecture able to supply DC or AC outputs from diverse alternative energy sources. The most relevant advantage of this multipurpose converter is to provide boosting and inversion in a single stage. The boost inverter has been studied from design and control perspectives with renewable energy sources. However, the real-time emulation of boost inverters is less widespread in literature. In this context, the main contribution of this paper is proposing an innovative methodology based on the Systems Modeling Language and Petri nets to emulate in real-time power converters using the boost inverter as a case of study. This approach develops real-time Hardware-in-the-Loop models using a graphical language and Petri nets. These graphical and Petri net features allow a formal validation of computational and time constraints before implementation in FPGA. The proposed methodology is also able to transform the developed models to the High Level Specification of Embedded Systems for automatic code generation. Comparison of real-time emulations and experimental results shows a suitable trade-off between the model accuracy and the computational time.

Keywords: Boost inverter, Hardware-in-the-Loop, SysML, Petri net, real-time emulation, FPGA.

1. Introduction

1 Nowadays, alternative energy sources have increased their integration in
2 power systems. As a result, innovative power converters are required to ac-
3 complish the power system conditions [1]. Modern power converters should
4 be robust architectures able to interact with intermittent energy sources and
5 electrical grids [2]. Currently, the boost inverter is a power converter able to
6 achieve these requirements which can be tested using real-time emulations [3].

7
8 The boost inverter shows interesting characteristics because provide both
9 boosting and inversion in a single stage [4]. These characteristics improve the
10 power system efficiency [5], decrease the harmonic distortion [6], and increase
11 the system reliability [7]. Authors in [8] introduce the boost inverter and pro-
12 pose a nonlinear control to take advantages of this converter. Also, further
13 studies present advanced control strategies to improve the boost inverter per-
14 formance as presented by [9][10][11]. Indeed, advanced controllers allow the
15 integration between renewable energy sources and the boost inverter [12][13].

16
17 According to [14], the integration of boost inverters and renewable en-
18 ergy sources requires innovative modeling approaches. For instance, authors
19 in [5] and [6] study the boost inverter interconnection with electrical grids
20 and PV modules. According to [15], the boost inverter can be modeled and
21 integrated in wind power systems. Other works also study the use of boost
22 inverters in hybrid architectures based on batteries, supercapacitors, and fuel
23 cells [16][17]. However, the boost inverter shows a highly nonlinear behavior
24 and control complexity which leads to unusual industrial applications despite
25 their remarkable advantages. As a consequence, the real-time emulation of
26 this power converter provides an interesting alternative for the control system
27 design to encourage their industrial application such as the current integra-
28 tion of renewable energies in power systems [18][19].

29
30 Real-time emulations provide several advantages for the study of power
31 converters [20]. Analyses based on real-time emulations allow evaluating
32 changes under different scenarios [21][22]. A relevant advantage of a real-
33 time approach is to test the safety operation of power converters closer to
34 working conditions using a Hardware-in-the-Loop method [23]. However, the
35 real-time emulation of boost inverters is less widespread in the literature de-
36 spite its powerful features.

37

38 In order to contribute in the fields of power electronics modeling and
39 real-time emulation, this study proposes an innovative modeling approach
40 using the graphical Systems Modeling Language (SysML)[24]. In this spe-
41 cific case, the boost inverter is modeled given its special characteristics and
42 potential range of applications in current renewable energy systems. Nev-
43 ertheless, the mathematical framework and the modeling methodology can
44 also be extended to other power converters.

45

46 The Systems Modeling Language (SysML) is a general-purpose modeling
47 language for specifying, analyzing, designing, and verifying complex systems
48 that may include hardware, software, information, and procedures [25][26].
49 SysML provides a systems engineering methodology able to model complex
50 systems and useful to describe systems based on power converters and re-
51 newable energies [27]. This study takes advantages of powerful modeling
52 possibilities of SysML to describe power electronics systems for further real-
53 time emulation in Field Programmable Gate Arrays (FPGAs) [28][29]. The
54 FPGA is selected as a processing device because of the characteristics of par-
55 allel processing, versatility, and adaptability [30][20].

56

57 The proposed methodology also employs the High Level Specification
58 of Embedded Systems (HiLeS) to transform automatically the developed
59 SysML models in Petri nets and VHDL code for model implementation in
60 FPGA [31][32]. This study contributes with the use of Petri nets in two
61 directions. First, the Petri nets are employed to verify the structural con-
62 sistency of the developed SysML models. Second, the analysis of generated
63 Petri nets allows identifying delays and defining the sequence of operations
64 to achieve the time constraints for real-time emulation of power converters
65 [33]. Fig.1 outlines the proposed modeling methodology through SysML and
66 Petri nets.

67

68 Section II introduces the boost inverter operation and their modeling us-
69 ing a component-based approach. Section III presents the concepts, current
70 state, and scope of real-time emulation methods for power converters. Sec-
71 tion IV presents the SysML and the HiLeS - Petri nets framework to emulate
72 in real-time power converters. Section V describes the experimental setup to
73 validate the proposed approach. Finally, emulated and experimental results
74 are discussed.

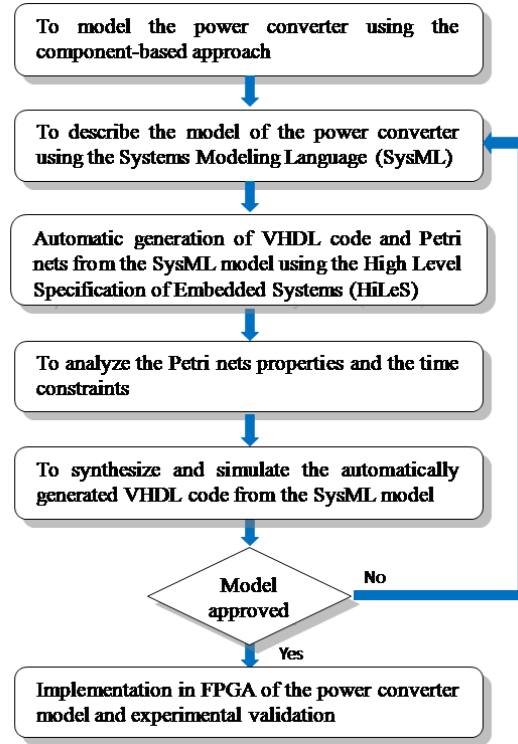


Figure 1: Modeling methodology based on SysML and Petri nets

76 2. Operation principle of boost inverter and modeling approach

77 This section introduces the operation principle and theoretical analysis
 78 of the boost inverter as a study case for further real-time emulation.

79 2.1. Operation principle

80 A boost inverter is a power converter build by two complementary bidi-
 81 rectional boost converters [4]. Fig.2 shows the operation principle of the
 82 boost converter. The output voltage of a boost inverter is given by eq.(1).
 83 When v_1 and v_2 are sinusoidal 180° phase-shifted and dc-biased signals, as
 84 shown in eq.(2) and eq.(3), the differential output of the boost inverter is
 85 given by eq.(4).

86

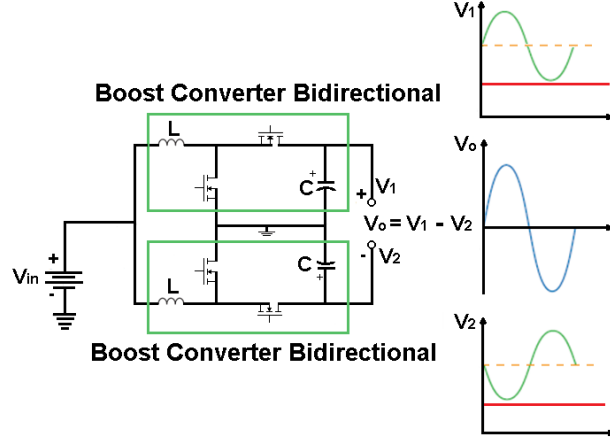


Figure 2: Operation principle of Boost inverter

$$v_o = v_1 - v_2 \quad (1)$$

$$v_1 = V_{dc} + \frac{1}{2}A_o \sin(\omega t) \quad (2)$$

$$v_2 = V_{dc} + \frac{1}{2}A_o \sin(\omega t - \pi) \quad (3)$$

$$v_o = A_o \sin(\omega t) \quad (4)$$

87 *2.2. Gain analysis*

88 The gain is the relation between the output and the input voltages of a
 89 power converter. The gain is one of the most important parameter for power
 90 converters. The ideal boost inverter gain is given by [4], where D is the duty
 91 cycle.

$$\frac{V_o}{V_{in}} = \frac{2D - 1}{D(1 - D)} \quad (5)$$

92 Taking into account the conductive losses, the boost inverter circuit is
 93 drawn in Fig.3. Where S_1 to S_4 are ideal switches, R_{on} represents the con-
 94 ductive losses of switching devices, and R_L are the conductive losses associ-
 95 ated to the inductors [34].

96

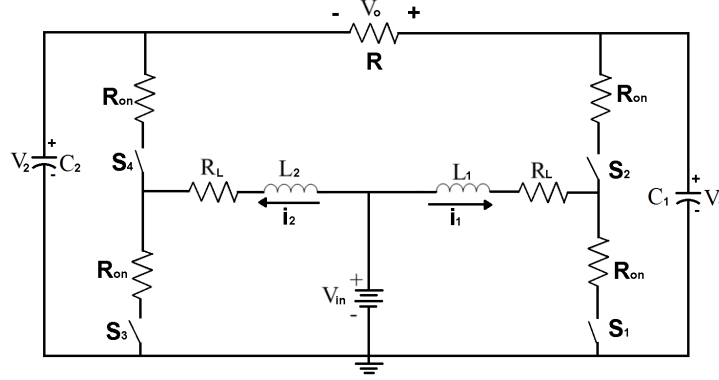


Figure 3: Boost inverter circuit with conductive losses

97 The boost inverter has two fundamental operation states. In the first
 98 operation state, $S_1 - S_4$ are active. In the second operation state, $S_2 - S_3$
 99 are active. For the first operation state,

$$v_{L1} = v_{in} - i_1 (R_L + R_{on}) \quad (6)$$

$$v_{L2} = v_{in} - i_2 (R_L + R_{on}) - v_2 \quad (7)$$

$$i_{c1} = \frac{v_2 - v_1}{R} \quad \text{and} \quad i_{c2} = i_2 + \frac{v_1 - v_2}{R} \quad (8)$$

100 In the second operation state,

$$v_{L1} = v_{in} - i_1 (R_L + R_{on}) - v_2 \quad (9)$$

$$v_{L2} = v_{in} - i_2 (R_L + R_{on}) \quad (10)$$

$$i_{c1} = i_1 + \frac{v_2 - v_1}{R} \quad \text{and} \quad i_{c2} = \frac{v_1 - v_2}{R} \quad (11)$$

101 Applying the principle of inductor volt-second balance and the capacitor
 102 charge balance to equations eq.(6) to eq.(11) [35]. Where $R_s = R_L + R_{on}$
 103 and $D_1 = 1 - D$,

$$\langle V_{L1} \rangle = D (V_{in} - I_1 (R_s)) + D' (V_{in} - I_1 (R_s) - V_1) = 0 \quad (12)$$

$$\langle V_{L2} \rangle = D (V_{in} - I_2 (R_s) - V_2) + D' (V_{in} - I_2 (R_s)) = 0 \quad (13)$$

$$\langle I_{c2} \rangle = D \left(\frac{V_2 - V_1}{R} \right) + D' \left(I_1 + \frac{V_2 - V_1}{R} \right) = 0 \quad (14)$$

$$\langle I_{c2} \rangle = D \left(I_2 + \frac{V_1 - V_2}{R} \right) + D' \left(I_1 + \frac{V_1 - V_2}{R} \right) = 0 \quad (15)$$

104 Solving the system of equations from eq.(12) to eq.(15), the boost inverter
 105 gain is given by eq.(16) [34].

$$\frac{V_o}{V_{in}} = \frac{2D - 1}{\frac{R_s}{R} \left(\frac{1}{D'} + \frac{D'}{D} - 1 \right) + DD'} \quad (16)$$

106 Fig. 4a shows the relationship between the output voltage and the input
 107 voltage given a series resistance R_s associated to conductive and inductance
 108 losses and a set of resistive loads R . As shown in Fig. 4a, the gain of a
 109 boost inverter can be affected by the load changes. Fig. 4a depicts that an
 110 AC voltage can be produced when the duty cycle oscillates around $D = 0.5$.
 111 Finally, eq.(16) determines that the factor R_s/R limits the boost inverter
 112 gain.

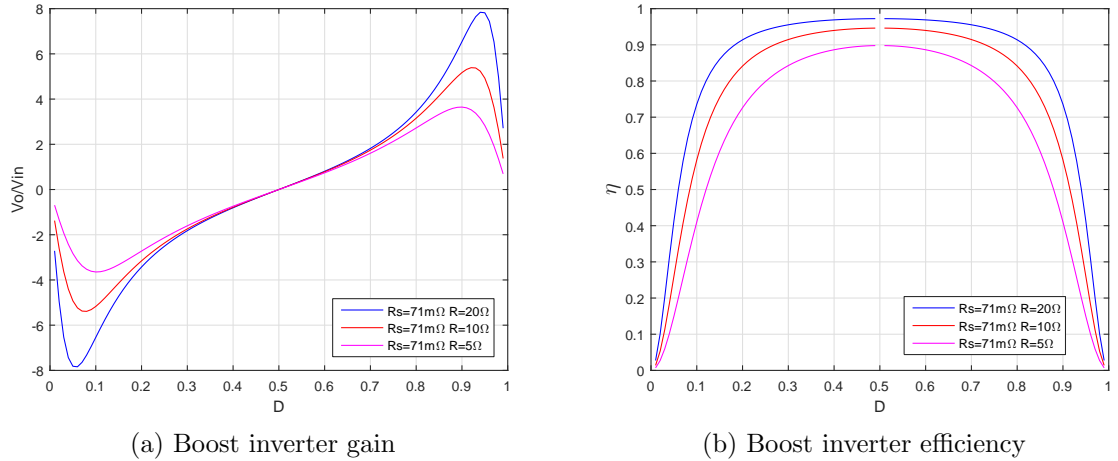


Figure 4: Boost inverter gain and efficiency

113 *2.3. Efficiency analysis*

114 The efficiency η is another important parameter of power converters. The
 115 efficiency is defined as a relation between the output power and the input
 116 power. Thus,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \left(\frac{V_{out}}{V_{in}}\right) \left(\frac{I_{out}}{I_{in}}\right) \quad (17)$$

117 Given the following relation for the boost inverter currents,

$$I_{in} = I_1 + I_2 = I_o \left(\frac{2D - 1}{DD'}\right) \quad (18)$$

118 Calculating the efficiency η from eq.(16) and eq.(18),

$$\eta = \left(\frac{2D - 1}{\frac{R_s}{R} \left(\frac{1}{D'} + \frac{D'}{D} - 1 \right) + DD'} \right) \left[\frac{1}{\frac{2D - 1}{DD'}} \right] \quad (19)$$

119 Fig.4b depicts the boost inverter efficiency η according to eq.(19). Fig.4b
 120 shows the influence of the duty cycle on the efficiency. As shown in Fig.4b,
 121 variations of $D \geq 0.8$ and $D \leq 0.2$ impact drastically in the converter effi-
 122 ciency [18]. Fig. 4a and Fig.4b also show the better operation range between
 123 $0.2 \leq D \leq 0.8$ where variation is more linear and efficiency is higher. Tak-
 124 ing into account previous results, it is clear that a well developed model
 125 is necessary to describe the nonlinear behavior of the boost inverter. Next
 126 section describes the component-based approach for boost inverter modeling.
 127

128 *2.4. Component-based approach to model the boost inverter*

129 The previous section showed the non-linearity and behavior of boost in-
 130 verter which requires innovative modeling approaches. This section intro-
 131 duces a component-based approach suitable to describe the complex behav-
 132 ior of power converters which is applied to the boost inverter a case study.
 133 This component-based approach is intended to model power converters as
 134 building blocks interacting with their environment. This methodology al-
 135 lows to model the power converter with a high degree of detail disregarding
 136 subsequent changes in the power source and load models.

137

138 The state of the art about modeling of boost inverter is focused on
139 oriented-control approaches [18]. Caceres *et .al* introduce the model pre-
140 sented in [8] and consider for analysis half boost inverter coupled with a
141 fixed source. Approach in [8] simplifies the analysis; however, the dynamic
142 of half boost inverter is disregarded. In [4] is proposed a model to design a
143 slide-mode control on each half boost inverter. According to authors in [4],
144 the output transfer function is evaluated to analyze the boost inverter sta-
145 bility. Flores-Bahamonde *et .al* in [36] assume the boost inverter operation
146 with complementary signals; therefore, two configurations are obtained. In
147 [36], the state equations are given and the second method of Lyapunov is
148 used for stability analysis. According to [37], the proposed model can ex-
149 press the converter behavior using a simplify average model. AC operation
150 is represented by a simplified model of the electrical grid [37]. The model is
151 intended to study the harmonic input current impact on the boost inverter
152 [37]. Finally, the boost inverter model in [15] introduces a converter bilinear
153 model from a state-space model considering the grid connection.

154
155 As aforementioned, most of proposed models in literature are intended to
156 control design. Additionally, proposed models simplify the boost inverter be-
157 havior, use linear approaches, and disregard the influence of conductive losses.
158 However, these characteristics have an important effect on the efficiency and
159 gain of actual power converters [35]. Another drawback of current models is
160 the lack of scalability and adaptability; therefore, most of these models should
161 be updated when the operation condition changes. For instant, changes in
162 either the type of load or the power source require significant changes in the
163 model. These drawbacks are a disadvantage for real-time emulations because
164 the study of versatile converters such as the boost inverter requires the test
165 under several scenarios.

166
167 In this context, an innovative component-based approach is presented.
168 This methodology explores characteristics of adaptability, scalability, and
169 model integration suitable for the study of power systems built by several
170 types of power sources, converters, and loads. In addition, this method is
171 intended to digital real-time emulations.

172
173 The component-based approach employs the concept of instantaneous
174 power conservation to analyze the power converter systems as structures
175 formed by functional components [18]. Fig.5 shows the general concept

176 about the component-based approach. In this case, the power converter
 177 is modeled independently of changes in the power source or the load. This
 178 modeling approach uses the flow of information between the power converter
 179 and its electrical neighborhood. To achieve this goal, the power converter is
 180 modeled with virtual sources able to maintain the equivalent instantaneous
 181 power at the input and output ports. The modeling procedure by using the
 182 component-based approach is described as follows:

Step 1: Substitution of the source power model by a virtual voltage source and
 184 the load model by a virtual current source. The aim of these changes is
 185 to formulate the power converter equations in terms of input and output
 186 voltages and currents independently of its electrical neighborhood.

Step 2: Formulation of the power converter equations in terms of inputs, out-
 188 puts, and internal parameters. These systems of equations are converted
 189 into the discrete domain because this method is intended to
 190 digital real-time emulations.

Step 3: Formulation of equations for describing the interaction between inputs
 192 and outputs with the electrical boundaries.

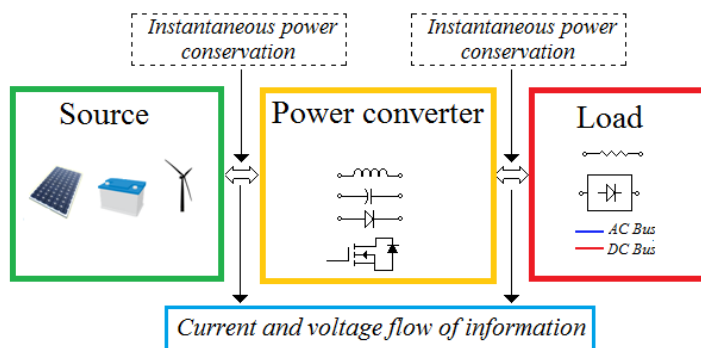


Figure 5: Component-based modeling approach

193 The boost inverter modeling applies the component-based approach. Four
 194 functional components are identified using this approach. The identified func-
 195 tional components are two bidirectional boost converters, the power source,
 196 and the load. Fig.6 shows the functional components of the boost inverter
 197 [18].

198

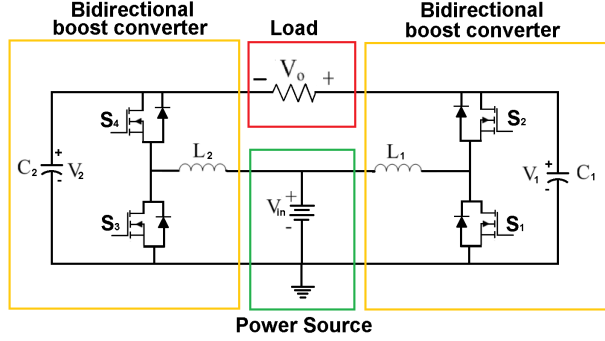


Figure 6: Boost inverter circuit and functional components

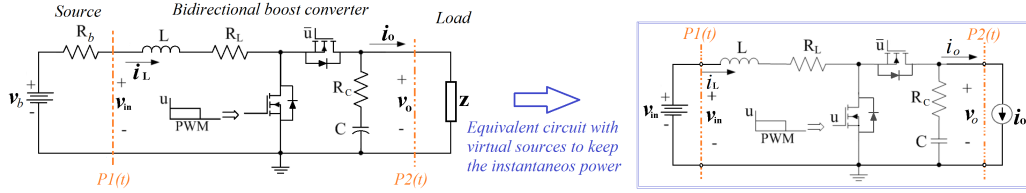


Figure 7: Operation states of bidirectional boost converter modeled with virtual sources

199 The boost inverter analysis takes as a start point the study of the bidi-
 200 rectional boost converters. In this case, the bidirectional boost converter is
 201 studied using the component-based approach and the instantaneous power
 202 conservation. Fig.7 represents the bidirectional boost converter but inter-
 203 connected to input and output virtual sources. These virtual sources are
 204 intended to keep the instantaneous power $p_n(t) = v_n(t)i_n(t)$ at the input
 205 and output ports. For this reason, the input power source is replaced by a
 206 voltage source keeping the input current, and the load is replace by a current
 207 source keeping the output voltage. The power conservation property allows
 208 to model the converter without considering changes in the power source or
 209 the load, but only taking into account the information flow with the electrical
 210 boundaries (see Fig.5) [18].

211

212 As shown in Fig.5, the bidirectional boost converter block should interact
 213 with the power source and load blocks through information flow. Then, in
 214 order to achieve this goal the following mathematical framework is proposed
 215 [34].

216

217 From circuit in Fig.7, the bidirectional boost converter behavior is given
 218 by two operation states represented by the control signal $u = \{0, 1\}$. Then,
 219 the converter behavior is given by,

$$\frac{di_L}{dt} = \frac{1}{L} [v_{in} - i_L(R_L + R_{on}) - (i_L R_c - i_o R_c + v_c)(1 - u)] \quad (20)$$

$$\frac{dv_c}{dt} = \frac{1}{C} [-i_o + i_L(1 - u)] \quad (21)$$

220 Given the discrete form with a sample time h , and let us consider $R_s =$
 221 $R_L + R_{on}$,

$$i_{L_{k+1}} = \frac{h}{L} [v_{in_k} - i_{L_k}(R_L + R_{on}) - (i_{L_k} R_c - i_{o_k} R_c + v_{c_k})(1 - u_k)] + i_{L_k} \quad (22)$$

$$V_{c_{k+1}} = \frac{h}{C} [-i_{o_k} + i_{L_k}(1 - u_k)] + v_{c_k} \quad (23)$$

222 Finally, the input and output interactions are defined. The output voltage
 223 interaction is then,

$$v_{o_k} = v_{c_k} + R_c [i_{L_k}(1 - u_k) - i_{o_k}] \quad (24)$$

224 Eq.(22) and eq.(24) are the output variables from the bidirectional boost
 225 converter block. The calculated $i_{L_{k+1}}$ can be sent to the power source block
 226 and v_{o_k} is able to be sent to the load block. Furthermore, eq.(22) to eq.(24)
 227 are expressed to variables v_i and i_{o_k} from associated power source and load
 228 blocks. Additional terms in eq.(22) to eq.(24) depend only of internal states
 229 and parameters. Then, any change in the power source and load models
 230 does not affect the developed converter model. Indeed, this is an advantage
 231 for real-time emulation because model operations and execution time can be
 232 well defined before model implementation.

233

234 Section IV will integrate the boost bidirectional model with the power
 235 source and the load models using the graphical language SysML. This model
 236 integration of section IV is proposed to develop real-time emulations. For
 237 this reason, before to model the boost inverter in real-time, the next section
 238 will introduce the currents state and the scope of real-time emulations in
 239 power electronics.

240 3. Real-time emulation of power converters

241 This section describes briefly the basic concepts about real-time emula-
242 tion, and its current state and scope in power electronics.

243
244 A real-time emulation of power electronics systems search to reproduce
245 accuracy voltage and current signals in a safety environment. These signals
246 represent the modeled systems and can be used to study control systems or
247 power interactions. This goal requires a fast digital real-time emulator able
248 to solve the equations that model the system [38]. Therefore, in discrete
249 time intervals are produced the output signals equivalent to the emulated
250 system [39]. Two situations can arise from the time constraints to evaluate
251 the model equations. First, the model execution time is shorter than the
252 required time-step. Then, the emulation is considered real-time. In contrast,
253 when emulation solves the equations after the time-step the emulation is con-
254 sidered non real-time or offline [39].

255
256 The real-time emulations are classified in two categories [38]. The first
257 category is a full digital real-time emulation. In this case, the emulation
258 occurs inside of the processing device without information interchange with
259 the environment. The second category is the Hardware-in-the-Loop. For this
260 category, an interchange of electrical signals occurs and digital-analog and
261 analog-digital conversion are required [23]. When the Hardware-in-the-Loop
262 system involves an actual controller, it is called a Controller Hardware-in-
263 the-Loop (CHIL). Our study is oriented toward Controller Hardware-in-the-
264 Loop. In contrast, the emulation that interacts with power transfer is known
265 as a Power Hardware-in-the-Loop (PHIL) [38].

266
267 According to Faruque et al. [39] a real-time emulator needs to solve an
268 electrical grid-scale model by roughly $50\mu s$ or a smaller time-step to repro-
269 duce electrical transients. Additionally, smaller time-steps are required in
270 power electronics systems because of the high switching frequency of power
271 converters [40]. For Controller Hardware-in-the-Loop, the internal clock of
272 microprocessors for the control system has speed periods of $1\mu s$ to 10ns.
273 Then, an emulation of these systems requires more computing capability
274 and the ability to emulate in the nanosecond scale [41].

275
276 Given these features of calculation speed and time constraints, the Field

277 Programmable Gate Arrays (FPGAs) arise as a suitable devices to achieve
 278 the requirements of real-time emulation in power electronics [21]. Fig.8 de-
 279 picts the frequency range versus simulation complexity [42]. In this figure,
 280 the frequency emulation above 100 KHz is feasible for FPGA and represents
 281 a research challenge [42]. However, Myaing *et .al* argue that the main draw-
 282 back of FPGAs is the complexity for developing code [43]. Indeed, Andina *et*
 283 *.al* highlight the potential of FPGAs for real-time emulations; however, tools
 284 to take more advantages of these devices are still required [44]. For these
 285 reasons, the next section describes the SysML and the HiLeS approaches to
 286 develop FPGA-based models to contribute with a structural methodology to
 287 emulate in real-time power converters.

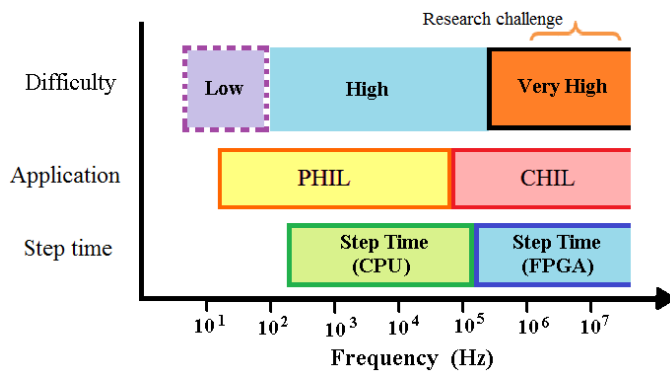


Figure 8: Range of applications and processing devices for real-time emulations

288 4. The SysML and Petri nets to emulate power converters

289 This section presents the Systems Modeling Language (SysML) [25], the
 290 High Level Specification of Embedded Systems (HiLeS) [31], and the Petri
 291 nets concepts [45] to develop FPGA-based real-time models of power con-
 292 verters. These models are developed using the component-based approach
 293 described in section II with the boost inverter as a study case.

294 4.1. SysML models

295 The Systems Modeling Language (SysML) is a general-purpose graphical
 296 modeling language for specifying, designing, and verifying of engineering sys-
 297 tems [25]. The SysML language uses international standardized diagrams to
 298 specify the system concepts and architectures. The main diagrams in SysML

299 are the Block Definition Diagrams, the Internal Block Diagrams, and the
 300 Activity Diagrams [25]. The Block Definition Diagrams define the structure
 301 and hierarchy of components in a system. The Internal Block Diagrams de-
 302 scribe the interaction between components. Finally, the Activity Diagrams
 303 are intended to model both computational and flow processes.

304

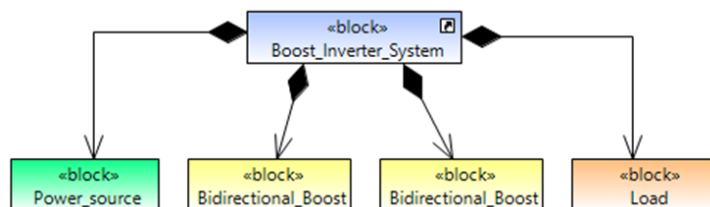


Figure 9: Block Definition Diagram for the boost inverter model

305 As described in section 2.4, the boost inverter was analyzed as a system
 306 built by four functional components. The SysML representation is shown
 307 in the Block Definition Diagram of Fig.9. This figure depicts the structural
 308 composition of the boost inverter. Fig.10 shows the interaction between the
 309 functional components of the boost inverter. This figure represents the Inter-
 310 nal Block Diagram with the specification of the information flow between the
 311 bidirectional converters, the power source, and the load [34]. In this case, the
 312 main components are the bidirectional boost converters which interchange
 313 current and voltage information with the load and the power source. Finally,
 314 the Activity Diagram of Fig.11 represents a simplified sequence of process
 315 to evaluate the boost inverter model. In this case, the Activity Diagram
 316 represents the operation flow and the concurrency of parallel process.

317

318 The proposed approach allows describing the behavior of each compo-
 319 nent in contrast with conventional modeling methodologies [18]. As a result,
 320 each functional component is modeled with independence of external mod-
 321 els. This approach is feasible for modeling current power converters because
 322 the interactions should be analyzed for the different types of power sources,
 323 converter topologies, and loads [34].

324 4.2. Model transformation from SysML to Petri nets and VHDL

325 The High Level Specification of Embedded Systems (HiLeS) framework is
 326 a free license tool able to transform automatically the SysML diagrams into

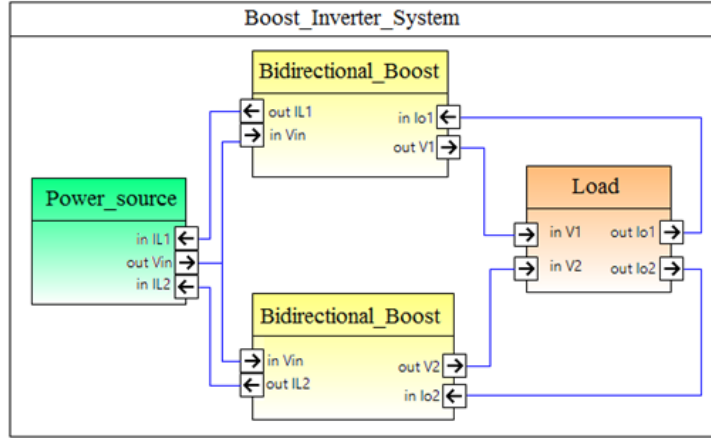


Figure 10: Internal Block Diagram for the boost inverter model

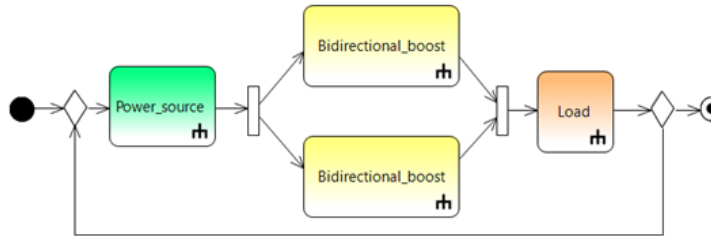


Figure 11: Activity Diagram for the boost inverter model

327 Petri nets and VHDL code [32]. The main advantages of this transformation
 328 are the structural and temporal verification of the developed models before
 329 implementation.

330

331 The HiLeS framework automatically transforms each element of the SysML
 332 model into an equivalent HiLeS formalism element [31]. The HiLeS formalism
 333 integrates in a Petri net representation the Internal Block Diagrams and the
 334 Activity Diagrams. Fig.12 depicts an illustrative example of these transfor-
 335 mations. First, the Internal Block Diagrams are represented by operational
 336 blocks which are controlled by a Petri net according to the Activity Dia-
 337 gram sequence. Then, the control Petri net and the operational blocks are
 338 described as a synthesizable VHDL code. At this transformation level, the
 339 control Petri net is synthesized in digital components and the operational
 340 blocks are represented in VHDL code by Entities and Signals. The transfor-

341 mation rules are presented in Reference [46].

342

343 The VHDL code automatically generated by the tool takes advantage
 344 of the Petri net features to provide a fully parallel architecture intended to
 345 decrease the processing time. However, the main constraints of the HiLeS
 346 tool are the needs of the algorithm complexity simplification, the code opti-
 347 mization, and the allocation control of the synthesized components. These
 348 aspects will be considered in further research on the tool development.

349

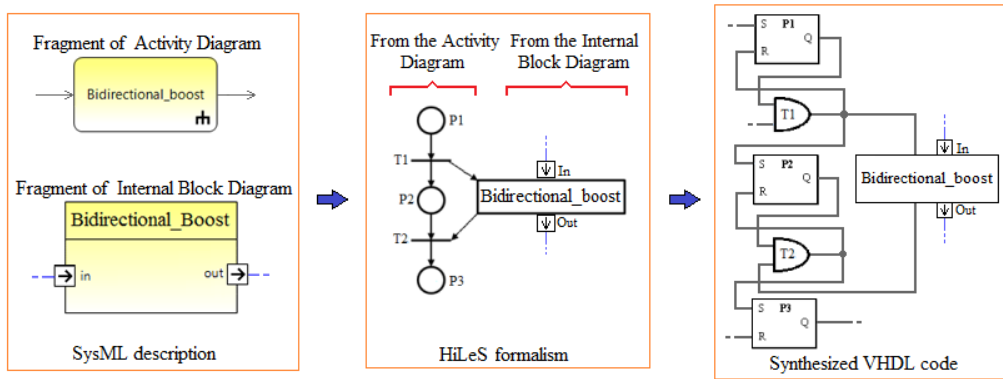


Figure 12: Illustrative example of SysML to VHDL code transformation

350 Fig.13 shows the SysML transformation chain used by the HiLeS frame-
 351 work. In Fig.13, T1 transforms SysML diagrams to the HiLeS formalism.
 352 Stage T2 extracts the Petri net representations from the HiLeS model. Fi-
 353 nally, transformation T3 is used to transform the HiLeS description in VHDL
 354 code for implementation in FPGA [33]. An illustrative example is described
 355 through this section using the bidirectional boost converter model developed
 356 in section 2.4.

357

358 In Fig.14, the Activity Diagram partially represents the flow of operations
 359 to calculate the bidirectional boost converter model from eq.(22) to eq.(24).
 360 Fig.14 shows the advantage of using Activity Diagrams because these dia-
 361 grams allow defining the concurrency and interdependency of operations to
 362 take advantage of the parallel processing and adaptability of FPGAs. Fur-
 363 thermore, the HiLeS framework transforms automatically the Activity Dia-
 364 grams in Petri nets according to the rules in [32].

365

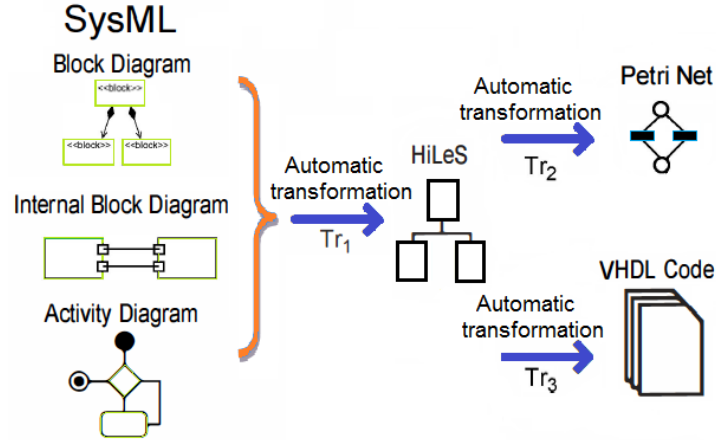


Figure 13: SysML transformations using the HiLeS framework

366 The Petri nets are a graphical and mathematical modeling language
 367 for the description of distributed systems. The Petri net elements are the
 368 places P_n (circles), transitions T_n (rectangles), and arcs (arrows) [45]. Places
 369 are connected to transitions by mean of arcs. According to [32], each ele-
 370 ment from the Activity Diagram is transformed to an equivalent Place-Arc-
 371 Transition branch. Fig.15a shows the associated Petri net of Fig.14. As
 372 example, the sequence of operations P_5 highlighted in the Activity Diagram
 373 is translated to a Petri net branch in Fig.15a. A repetitive loop with the
 374 transition T_6 is added to the Petri net of Fig.15a to analyze the iterative
 375 properties of the equivalent Petri net. Fig.15b shows a simplified version of
 376 the Petri net of Fig.15a to illustrate in the next section the formal mathe-
 377 matical validation.

378 4.2.1. Petri nets analysis

379 The Petri nets and the linear algebra theories allows analyzing the Petri
 380 net properties. The main properties of Petri nets are the boundedness, live-
 381 ness, invariance, and consistency. To accomplish these properties ensure the
 382 Petri net stability and the feasible use of computational resources to avoid
 383 unexpected behavior after implementation [45].

384

385 From the simplified Petri net of Fig.15b, the graph of markings is shown
 386 Fig.16a. In Petri nets, a change of state is denoted by the movement of to-
 387 kens or marks (\bullet) from one place to another. A graph of markings represents

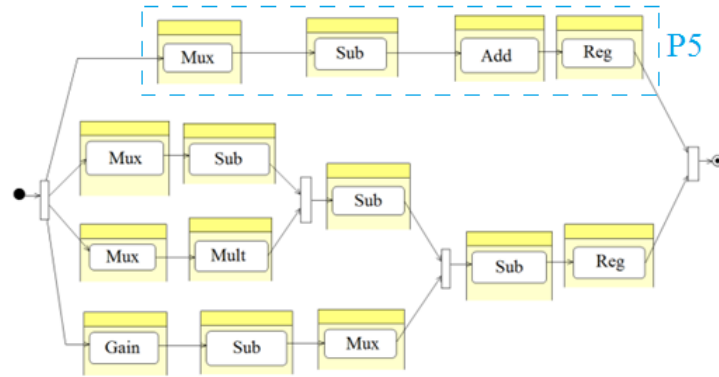


Figure 14: Partial Activity Diagram for calculation of the bidirectional boost model

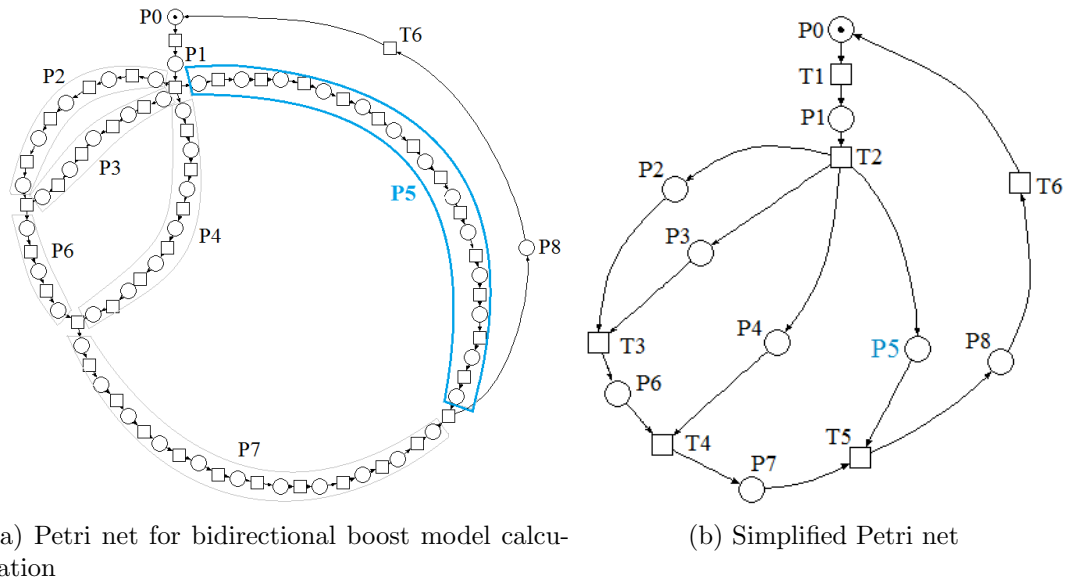


Figure 15: Petri net for the bidirectional boost converter model

388 the possible markings for the analyzed Petri net after transition firing [45]. A
 389 marking is a column vector whose components indicate the number of tokens
 390 or marks in each place (P_n). Fig.16a shows that each place has maximum
 391 one token. Then, the simplified Petri net is bounded because it has a limited
 392 number of tokens in each place. The interpretation of this property is that
 393 the Petri net requires a finite memory space and a finite use of hardware re-

394 sources. Furthermore, the graph of markings shows that is possible to reach
 395 any marking from any other marking; then, the Petri net is live without
 396 deadlocks [45]. An incident matrix \mathbf{W} denotes in columns the corresponding
 397 marking modification when a transition T_n is firing and to add (1) or remove
 398 (-1) tokens [45]. Fig.16b represents the incident matrix of the bidirectional
 399 boost converter model.

400

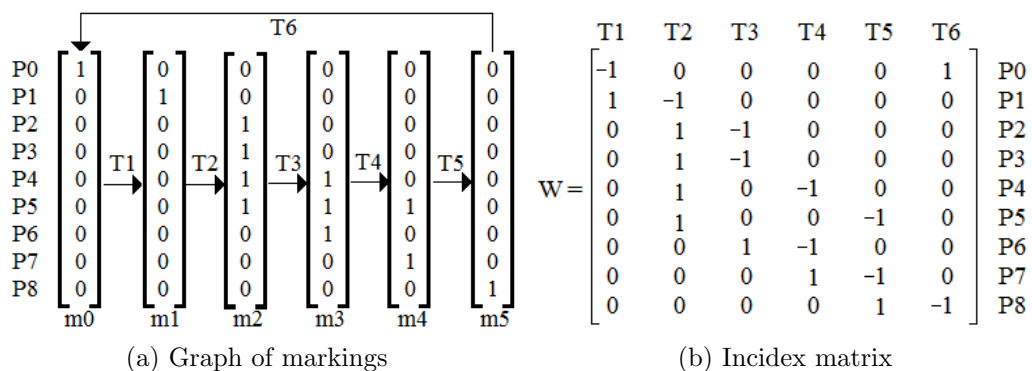


Figure 16: Petri net representation with linear algebra

401 A vector of places x , $x = (p_1, p_2, \dots, p_n)$ with $0 \leq p_i$, which is a solution
 402 of $x^T \cdot W = 0$ is known as a P-invariant and represents the invariant prop-
 403 erty of Petri nets [45]. Given the incidence matrix \mathbf{W} for the analyzed Petri
 404 net and the vector of places x , there is a finite solution for $x^T \cdot W = 0$ in
 405 $x^T = [4 \ 4 \ 1 \ 1 \ 1 \ 1 \ 2 \ 3 \ 4]$. Then, this Petri net is invariant [45].

406

407 A vector y associated with a firing sequence and solution of $W \cdot y = 0$
 408 is known as a T-invariant. y represents the consistent property of Petri nets
 409 [45]. Given the incidence matrix \mathbf{W} for the analyzed Petri net and the vector
 410 of transitions y , there is a finite solution for $W \cdot y = 0$ in $y = [1 \ 1 \ 1 \ 1 \ 1 \ 1]^T$.
 411 Then, this Petri net is consistent [45].

412

413 As a result, the Petri net for the bidirectional boost converter model is
 414 bounded, live, invariant, and consistent [45]. These properties ensure the
 415 structural and behavioral stability of the proposed model before implemen-
 416 tation in FPGA.

417



Figure 17: Time graph for the Petri net evolution

418 The formal validation of Petri nets by means of linear algebra methods is
 419 usually validated using computational tools [47]. The use of these automatic
 420 analysis tools, such as the integrated tool to HiLeS (TINA - Time Petri Net
 421 Analyzer), allows the formal validation of Petri nets with a large number
 422 of places and transitions [47]. Then, developed power converter models in
 423 SysML can be transformed to Petri nets for formal Petri net validation with-
 424 out constraint in the Petri net size.

425
 426 In addition, the HiLeS framework automatically transforms the developed
 427 models to VHDL code for FPGA implementation. Then, the Petri net of the
 428 bidirectional boost converter model is analyzed by simulating the generated
 429 VHDL code. Fig.17 shows the temporal evolution of the model operations.
 430 Results in this figure depict the Petri net temporal evolution and the de-
 431 lays cause by the calculus in each stage. The simulation of Fig.17 allows
 432 validating the real-time constraints for the model and identifying the delay
 433 problems. In this case, the step time for model calculation is suitable for
 434 real-time application given their range in nanoseconds. After validation of
 435 the bidirectional boost model characteristics, the entire boost inverter model
 436 is integrated and the simulation results are analyzed.

437
 438 Fig.18 depicts the simulation of the VHDL code for the inductor currents

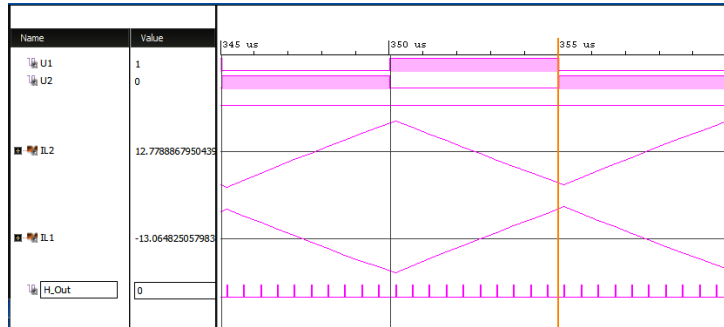


Figure 18: Simulation results for inductor current with time step around 500nS

439 (I_{L1}, I_{L2}) of the boost inverter model. Fig.18 shows that the step time for the
 440 boost inverter model is around 500nS (sampling signal H_Out). This step
 441 time is significantly lower than the expected switching time $U = 10\mu s$. Then,
 442 the developed model is able to emulate the boost inverter in real-time given
 443 this expected switching time U .

444

445 Furthermore, Fig.19 outlines the whole behavior for the boost inverter
 446 model driven by a control signal with a Sinusoidal Pulse Width Modulation
 447 (SPWM). Simulation of Fig.19 confirms that the developed real-time model
 448 is able to follow the dynamic and nonlinear behavior of the boost inverter
 449 given a sinusoidal reference. After this suitable results, the next section will
 450 describe the experimental setup to compare the developed emulation with
 451 an actual boost inverter prototype.

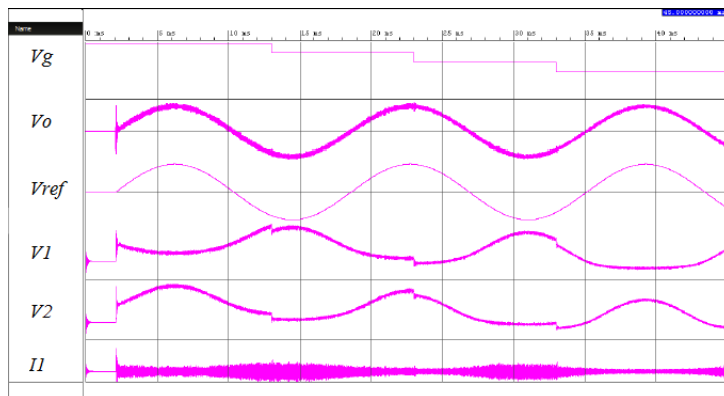


Figure 19: VHDL simulation of boost inverter real-time model

452 **5. Experimental test to validate the proposed approach**

453 The developed boost inverter model is implemented in FPGA and vali-
454 dated in real-time against the experimental test of a physical boost inverter
455 (Fig.20). For validation, a Sinusoidal Pulse Width Modulation (SPWM)
456 controls at the same time the boost inverter model and the boost inverter
457 prototype. The digital signals from the FPGA model are transformed in
458 analogical signals using high speed Digital-to-Analogical converters. Then,
459 the analogical signals are scaled and compared with the actual output sensor
460 signals. Table 1 lists the parameters for the experimental setup.

461

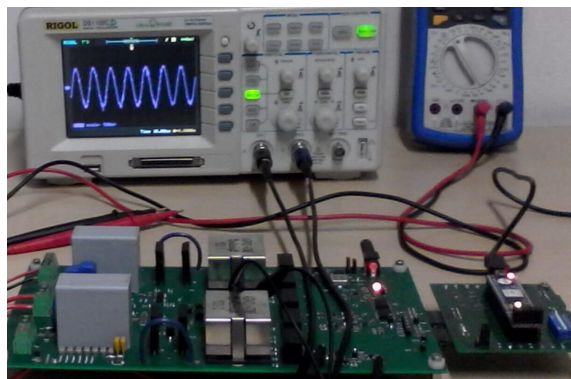


Figure 20: Experimental test of boost inverter prototype

462 The VHDL code automatically generated from the SysML models is syn-
463 thesized in FPGA. In this study, a Zynq-7Z020 - Artix7 series FPGA is used
464 to implement the developed model. The Vivado Design Suite WebPACK™
465 of Xilinx provides the VHDL synthesis, simulation, and configuration file for
466 model implementation in FPGA. Fig.21 summaries the resource utilization
467 after synthesis with an important use of the dedicated Digital Signal Pro-
468 cessors (DSPs) given the floating-point operations for high model accuracy.
469 Synthesis results also showed that the execution time is around 350ns which
470 agrees with the expected Petri net analysis. In addition, the ratio between
471 the execution time and the time step is approximately 70% where the differ-
472 ence is reserved to the high speed DAC communication.

473

474 Fig.22 depicts the DC comparison between the gain for the FPGA-based
475 emulation and actual boost inverter. Comparison of emulated and physi-

Table 1: Parameters for the experimental validation

Parameter	Value
$L_1 - L_2$	$47 \mu H$
R_L	$6 m\Omega$
$C_1 - C_2$	$10 \mu F$
R_c	$50 m\Omega$
$S_1 - S_4$	C3M0065090D - SiC MOSFET
R_{on}	$65 m\Omega$
DriverMOSFET	1EDI20N12AF
SPWM signal	$F_m = 50Hz$ $F_c = 100KHz$
DAC	High speed - AD5541
FPGA	Zynq-7Z020 - XC7Z020

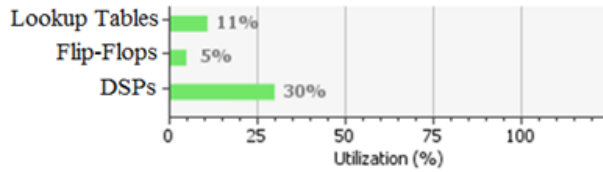


Figure 21: FPGA utilization after synthesis

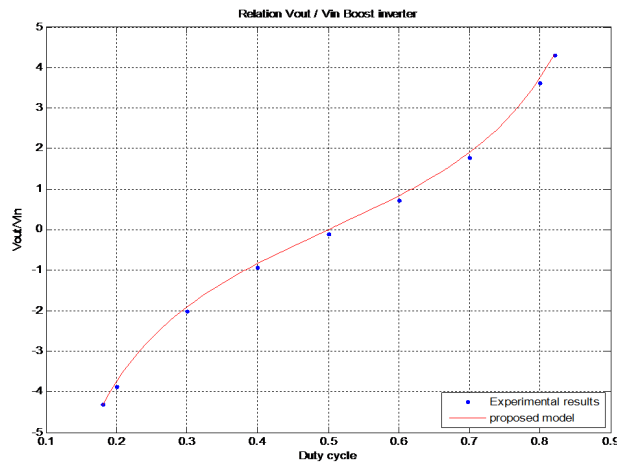


Figure 22: Boost inverter gain (red line - emulation, blue dot - prototype)

476 cal boost inverter gains shows the FPGA-based emulation accuracy. These

477 results also agree with the theoretical gain of eq.(16). Emulation results
 478 of Fig.23 allow verifying the experimental time step speed in comparison
 479 with the switching time for the emulated inductor currents. The boost in-
 480 verter power results are listed in Table 2 with suitable agreement between
 481 the emulation and the experimental results. Finally, results in Fig.24 show
 482 the synchronization between the emulated and the physical boost inverter
 483 for two percentages of modulation SPWM. In both cases, the results allow
 484 confirming the suitable performance of developed emulator to follow the non-
 485 linear and complex behavior of the boost inverter. In the next section, the
 486 results are discussed.

Table 2: Boost inverter power results

	SPWM Modulation 10%		SPWM Modulation 25%	
	Emulation	Experimental	Emulation	Experimental
Input power (W)	33.4	33.3	187.6	186.5
Output power (W)	30.8	30.3	167.0	164.1
Efficiency η	0.92	0.91	0.89	0.88

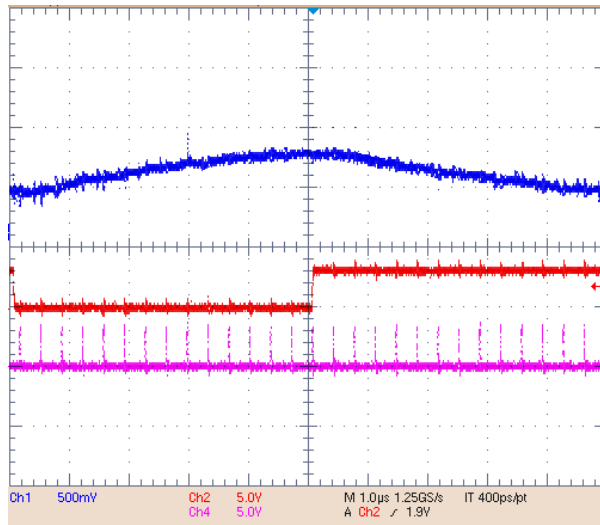


Figure 23: Time step for emulation of inductor current (blue - inductor current, red - control signal, magenta - time step)

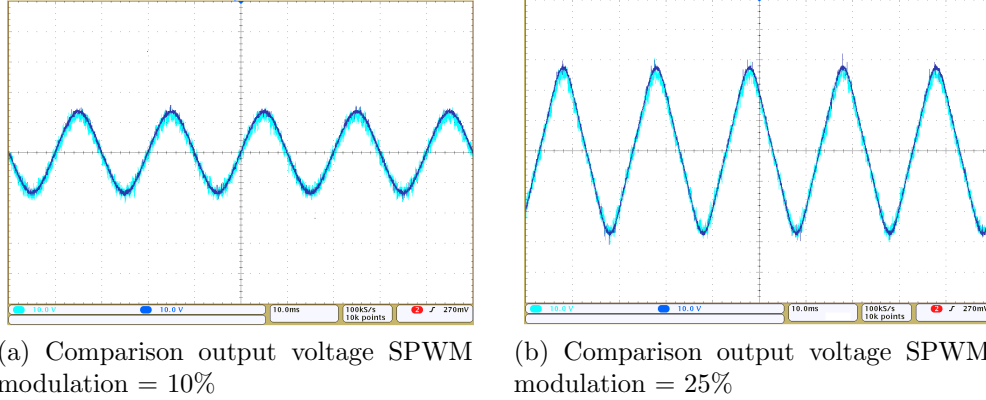


Figure 24: Comparison of emulated and experimental output voltages of the boost inverter

487 6. Results and discussion

488 Fig.22 shows the gain relation for the proposed emulation model and the
 489 actual boost inverter. For this gain comparison, the Medium Square Er-
 490 ror $MSE = (\sum_{i=1}^n (e_i)^2) / n$ is $MSE=0.01$. The Medium Absolute Error
 491 $MSE = (\sum_{i=1}^n |e_i|) / n$ is $MAE=0.093$. Then, the gain results validate the
 492 suitable accuracy of the real-time emulation model.

493
 494 Fig.23 depicts the inductor current, which is the faster signal, the control
 495 signal, and the model sampling signals. These results show that the time for
 496 the sampling signal allows calculating the model for the faster signal of the
 497 system. This case of study assumes a control signal with switching time of
 498 $10\mu S$ and a time step $500nS$ suitable to evaluate the model.

499
 500 In Fig.24 both emulated and physical signals are synchronized and com-
 501 pared. Fig.24a and Fig.24b show that the emulated signal is able to follow
 502 the behavior of the actual boost inverter in a wide range of SPWM variation.
 503 These results confirm that the proposed methodology is suitable to generate
 504 models for real-time emulation with a high degree of accuracy.

505
 506 These experimental and emulated results have shown that the proposed
 507 methodology based on SysML and Petri nets can contribute to the research
 508 challenges discussed in section 3. The time step and accuracy achieved in
 509 this study of case are in the expected region of research proposed by Lauss
 510 *et .al* [42] with suitable results. Finally, the proposed approach has shown

511 its potential to decrease the gap between the real-time modeling and the
512 complex implementation in FPGA as suggested by Andina *et .al* [44].

513

514 **7. Conclusion**

515 This paper has presented a modeling methodology based on SysML and
516 Petri nets able to model power converters. This study of case was focused on
517 the boost inverter with appropriate results. This methodology identified the
518 boost inverter functional components and their interactions by means of a
519 component-based approach. Furthermore, the bidirectional boost converter,
520 as main functional component of the boost inverter, was analyzed in detail
521 and subsequently integrated to the boost inverter for a real-time emulation.
522 The real-time emulation and experimental results provided a suitable model
523 accuracy and time performance. As a consequence, the proposed methodol-
524 ogy has shown its potential to model power converters. In future work, this
525 methodology can be applied to other power systems with different types of
526 energy resources, converter topologies, and nonlinear loads.

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