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A. Gutierrez[1−3], H.R. Chamorro[2], J.F. Jimenez[1], L.F.L. Villa[3−4], C. Alonso[3−4]
[1]Universidad de los Andes, Department of Electrical and Electronic Engineering, Bogotá, Colombia
[2]KTH Royal Institute of Technology, Stockholm, Sweden
[3]Univ. de Toulouse, Univ. Paul Sabatier, LAAS, F-31400, Toulouse, France
[4]CNRS; LAAS; 7 Avenue du Colonel Roche, F-31077, Toulouse, France
Email: {a.gutierrez75; fjimenez}@uniandes.edu.co, hr.chamo@ieee.org, {luiz.villa; alonsoc}@laas.fr

***Abstract*—This paper outlines a methodology for modeling photovoltaic systems in embedded hardware. This methodology uses the HiLeS platform to transform SysML models in Petri nets and generate VHDL code. The proposed methodology is intended for Hardware-in-the-Loop simulations of power converters and PV panels in microgrids. In addition, this methodology allows the design of MPPT controllers for their direct implementation in FPGA.**

***Index Terms*—Photovoltaic, Hardware-in-the-Loop, FPGA, SysML, Petri net, Boost converter, MPPT.**

I. Introduction

Currently, the extensive use of power electronics in micro-grids has increased their complexity [1] [2]. As a consequence, new strategies are needed for real-time simulation and control systems design in power electronics [3]. Indeed, high switching frequency of power converters increase the processing speed requirements of controllers [4] [5]. As a consequence, high performance devices are required to accomplish the performance requirements of these power electronics systems. Taking into account the previous reasons, FPGA is a suitable option to implement Hardware-in-the-Loop models of power electronics and control electronic systems in micro-grids [6]. However, designing and implementation of advanced micro-grids models requires a structural design methodology. In order to accomplish these design requirements, the HiLeS formalism (High Level Specification of Embedded Systems) is presented as a design methodology for developing Hardware-in-the-Loop simulations of power electronics in micro-grids. In addition, the HiLeS formalism through the HiLeS platform allows to validate and transform the SysML diagrams in Petri nets and VHDL code for implementations in FPGA [7]. This representation in Petri nets also allows a formal net structural analysis to avoid undesired computational behavior [8]. In addition, the automatic code generation provided by the HiLeS platform decreases the time of design and increase productivity.

In section II is presented a general description of the HiLeS platform. Section III shows the mathematical model of a PV panel used in this document. In section IV the numerical model of a Boost converter is analyzed. Section V presents a conventional MPPT controller, and section VI the control Petri net of the system is shown. Finally, simulations and experimental result are presented in section VII.

II. HiLeS Platform for HIL simulations of micro-grids

Hardware-in-the-Loop (HIL) emulations base on FPGA require tools to decrease the complexity through the design process. As a result, HiLeS platform provides a tool for designers to generate high level descriptions of embedded systems defining the functional composition, hierarchy and structure [9]. HiLeS platform is based on transformations from SysML to Petri nets and VHDL code for formal validation and hardware implementation.

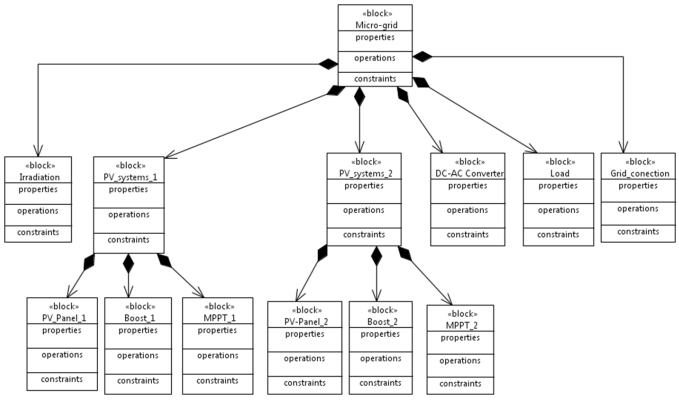

Fig. 1: Partial *Block Definition Diagram* of micro-grid based on PV systems.

1) SysML Models: SysML is an international standard language for modeling engineering systems [10]. Representative diagrams of SysML are Block Definition Diagrams, Internal Block Diagrams, and Activity Diagrams. SysML uses Block Definition Diagrams (BDD) to describe structural composition of systems, and Internal Block Diagram (IBD) to define the interconnections among the system components. Furthermore, SysML describe the system behavior by means of *Activity Diagrams*. Fig.1 shows the partial Block Definition Diagram (BDD) of a micro-grid based on PV systems. Fig.2 shows the partial Internal Block Diagram (IBD) for describing the interconnections among PV system components. The use of

SysML diagrams provides and structural design strategy which allows integrating several engineering fields in a common standard.

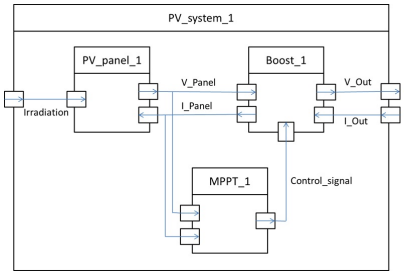

Fig. 2: Partial *Internal Block Diagram* of a PV system in a micro-grid.

2) From SysML Models to Petri nets: Main advantage of using *Activity Diagrams* in HiLeS platform is the representation in Petri nets according to the transformation rules defined in [11]. This representation based on Petri nets allows a formal net structural analysis in order to avoid undesired computational behavior. Furthermore, the transformation rules from SysML models to control Petri nets allows the automatic VHDL code generation for implementation in FPGA (Fig.3).

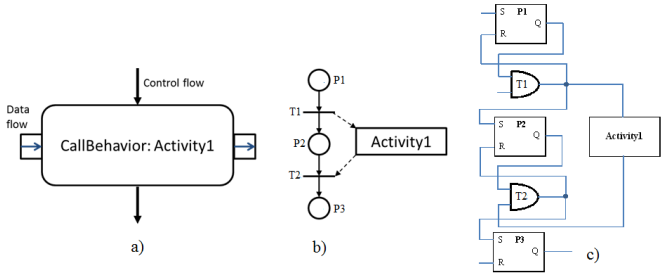

Fig. 3: a) Activity Diagram Component b) HiLeS Control Petri Net c) Equivalent synthesized VHDL code.

III. Mathematical model of PV panel

Photovoltaic panels can be modeled using the single diode circuit [12]. Let I_{ph} be the light generated current, under constant temperature conditions, the I_{ph} is proportional to the solar irradiance S_R where $I_{ph} = GS_R$. The characteristics of the PV cell with temperature constant are given by:

$$G\,S_R \;-\; I_0\,(e^{\frac{V_D}{V_t}} - 1) \;-\; \frac{V_D}{R_p} \;-\; I_{pv} \;=\; 0 \qquad (1)$$

A PV panel is built by *N* photovoltaic cells connected in series; therefore, the PV panel voltage is given by $V_{panel} = N\,(\,V_D \;-\; R_s I_{pv})$. From equation (1), V_D can be expressed as,

$$e^{\frac{V_D}{V_t}} \;=\; \frac{1}{I_0\;R_p}\,(G\;S_R\;R_p \;-\; I_{pv}\;R_p \;+\; I_0\;R_p \;-\; V_D) \quad (2)$$

Hardware implementation of analytical PV panel model from (2) is developed by a numerical method. Using the Newton-Raphson method [13], the term V_D in equation (3) can be found by iteration of:

$$V_{D_{n+1}} \;=\; V_{D_n} \;-\; \frac{V_t\;\left(I_{pv}\;R_p \;-\; G\;S_R\;R_p \;+\; I_0\;R_p\;e^{\frac{V_{D_n}}{V_t}} - I_0\;R_p + V_{D_n}\right)}{I_0\;R_p\,e^{\frac{V_{D_n}}{V_t}} \;+\; V_t} \qquad (3)$$

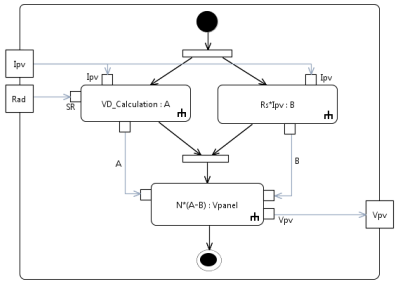

Fig. 4: Partial *Activity Diagram* of PV panel model.

Fig.4 describes the partial activity diagram for solving the PV panel model, and Fig.5 shows the associated control Petri net which is appropriate for implementation on FPGA.

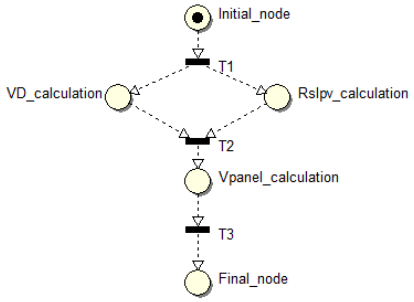

Fig. 5: Partial control Petri net of PV panel model.

IV. Numerical model of Boost converter

Boost converters are power converters of wide application in photovoltaic systems. Fig.6 shows a conventional boost converter circuit including losses. The behavior of a boost converter depends on the PWM signal. The inductor voltage and the capacitor current as function of the control signal *u* are given by eq.(4) and eq.(5).

$$\frac{di_L}{dt} = \frac{1}{L}[V_{in} - i_L R_L - (i_L R_{on})u - (V_d + i_L R_d + i_L R_c - i_o R_c + V_c)(1-u)] \quad (4)$$

$$\frac{dv_c}{dt} = \frac{1}{C}\,[-i_o + i_L(1-u)] \qquad (5)$$

Given the discrete form of (4) and (5) with a sample time *h*,

$$i_L(k+1) = \frac{h}{L}[V_{in}(k) - i_L(k)R_L - (i_L(k)R_{on})u(k) - (V_d + i_L(k)R_d + i_L(k)R_c - i_o(k)R_c + V_c(k))(1-u(k))] + i_L(k) \quad (6)$$

$$V_c(k+1) = \frac{h}{C}\left[-i_o(k) + i_L(k)(1-u(k))\right] + V_c(k) \quad (7)$$

Eq.(6) and eq.(7) are intended to use in circuits with impedance as load. However, in the specific case of PV systems, the boost converter load is associated to constant DC voltage source.

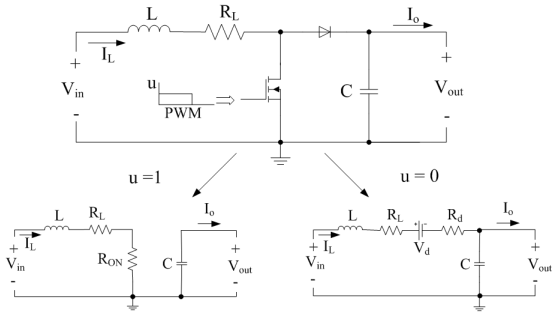

Fig. 6: Boost converter.

Therefore, boost converter control regulates the output current toward the constant DC voltage source. To model in SysML both situations with impedance and constant DC voltage source the following analysis is proposed. The output voltage is given by,

$$V_o(k) = V_c(k) + R_c\left[i_L(k)(1-u) - i_o(k)\right] \quad (8)$$

The model with impedance as load can be calculated from eq.(8) and eq.(9).

$$i_o(k) = \frac{V_o(k)}{Z} \quad (9)$$

On the other hand, the model with constant DC voltage source as load $V_o(k) = V_B$ is given by,

$$V_B = V_c(k) + R_c\left[i_L(k)(1-u) - i_o(k)\right] \quad (10)$$

Thus,

$$i_o(k) = i_L(k)(1-u) \; + \; \frac{V_c(k) - V_B}{R_c} \quad (11)$$

Fig.7 depicts the partial *Activity Diagram*, and Fig.8 presents the equivalent control Petri net of boost converter model to describe the calculation sequence.

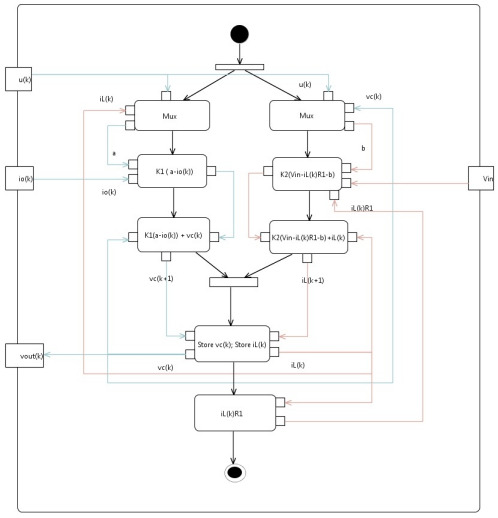

Fig. 7: Partial *Activity Diagram* of boost converter model.

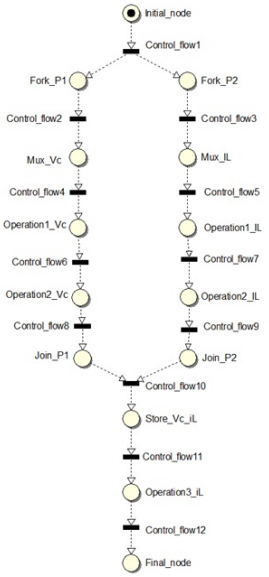

Fig. 8: Partial control Petri net of boost converter model.

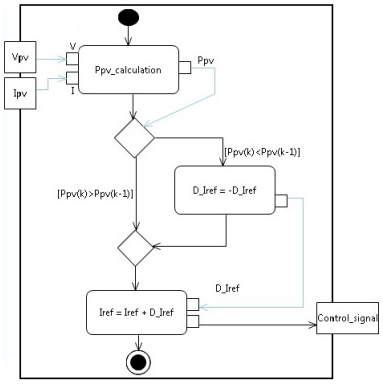

Fig. 9: Partial *Activity Diagram* of MPPT controller.

V. MPPT CONTROLLER

Currently, there are many different MPPT techniques [14] [15]; these are used in PV arrays to obtain the maximum power available from the system. The most popular algorithms is the Perturb and Observe method.

Fig.9 shows a partial MPPT based on the Perturb and Observe method modeled by means of *Activity Diagrams*, and Fig.10 shows the equivalent Petri net. Indeed, HiLeS methodology is focus on structural composition which allows assessing several MPPT methods for subsequent implementation in dedicated embedded hardware on FPGA.

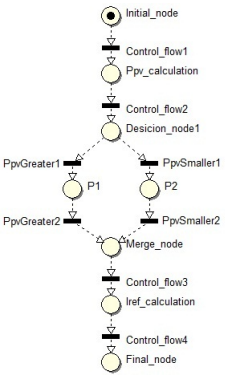

Fig. 10: Partial control Petri net of MPPT controller.

VI. CONTROL PETRI NET OF PV SYSTEM MODEL

According to the description of the PV system in Fig.2, the main system components are the PV panel, the boost converter, and the MPPT controller. The behavior of each components has been modeled by means of *Activity Diagrams* with their equivalent control Petri nets (Fig.5, Fig.8, Fig.10). As a consequence, a general control Petri net is proposed according to [11] in Fig.11. This general control Petri net describes in concurrent way the behavior of the PV system model. In fact, the proposed methodology allows taking advantage of the high performance and concurrent processing of FPGAs. Finally, description of PV system model in terms of Petri nets is suitable to verify theoretical properties of the associated Petri nets for structural and behavioral analysis before implementation. In this case, such analysis shows that the general Petri net of the PV system model is bounded, consistent, and live. As a result, the proposed control Petri net can be implemented in FPGA with low probability of undesired behavior.

VII. RESULTS

In order to validate the proposed methodology, VHDL simulations in the software Systen Vision are taken as reference. Fig.12 shows the calculation sequence of the inductor current simulation for a boost converter modeled by SysML and HiLeS platform.

Fig.13 shows the inductor current and the capacitor voltage simulations for the boost converter model; these results use math operations in float point format according to the IEEE 754 standard. Simulation results show coherence with theoretical models.

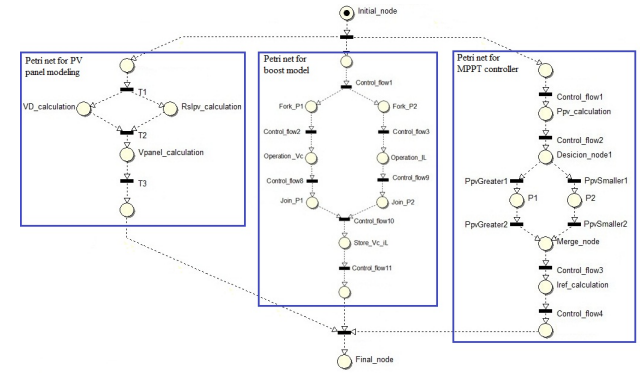

Fig. 11: Partial general control Petri net of the PV system model.

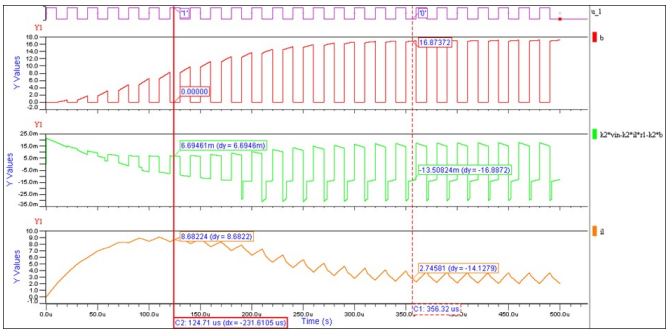

Fig. 12: Inductor current of boost converter model using VHDL code from HiLeS platform.

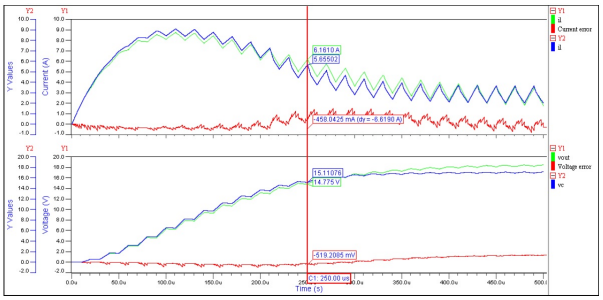

Fig. 13: Capacitor voltage of boost converter model using VHDL code from HiLeS platform.

In Fig.14, the result shows the Hardware-in-the-Loop implementation for Boost converter model. In addition, Fig.15 presents the suitable search action of the MPPT controller given as a reference a commercial PV panel under known irradiance.

VIII. CONCLUSION

This paper shows a methodology to implement PV system models in embedded hardware. The methodology is based on HiLeS platform, SysML diagrams and Petri nets. This methodology allows organizing the design process with adequate time

and appropriated hardware utilization. These characteristics are suitable for HIL modeling with high complexity level such as applications in micro-grids. Simulation results show consistency with theoretical models. Finally, description of PV system models in terms of Petri nets allows verifying properties for structural and behavioral analysis before implementation in FPGA.

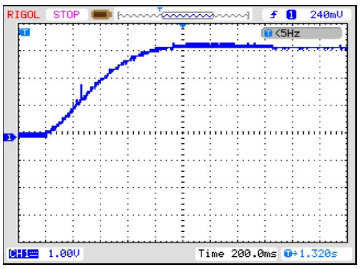

Fig. 14: Experimental result of boost converter model implemented in FPGA.

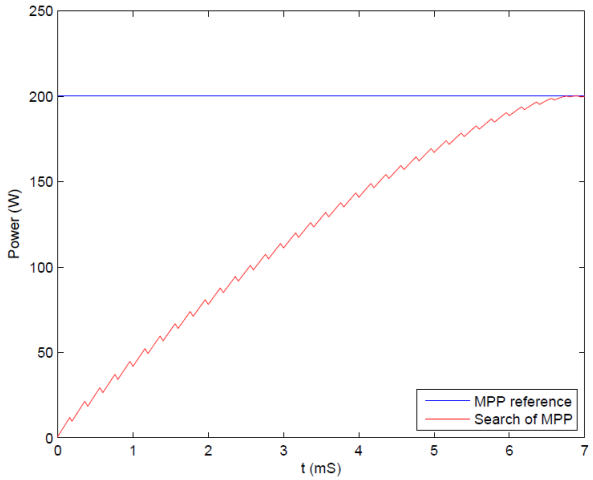

Fig. 15: Simulation of *Perturb and Observe* method for MPP search in PV model from HiLeS platform.

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