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# Development of Real-time Supervision HIL Emulator of Shaded PV Systems

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**Abstract**—This paper presents the development of a real-time Supervision Hardware-in-the-Loop (HIL) emulator of shaded PV systems. This study is focused on shaded conditions due to the impact of shadows in the final energy production and the global structural healthy. In this context, we propose a methodology to emulate in real-time the shaded PV system behavior. This proposed methodology is intended for evaluation of supervision and fault detection strategies using a Hardware-in-the-Loop approach. This study takes advantage of FPGAs given their features of adaptability and parallel processing suitable for emulation of complex shaded PV systems. The proposed methodology employs the High Level Specification of Embedded Systems (HiLeS) for automatic VHDL code generation, and the graphical Systems Modeling Language (SysML) to represent the PV system behavior. Experimental results show the emulation of current-voltage behavior of PV modules under normal and shaded conditions. Emulation results are compared with experimental and conventional computational approaches shown a high degree of accuracy.

**Keywords**—Photovoltaic, Shaded condition, Real-time Emulation, Hardware-in-the-Loop, FPGA, SysML.

## I. INTRODUCTION

Nowadays, photovoltaics (PV) systems play an important role in the recent tendency towards the use of distributed energy resources [1] due to their characteristics of modularity and easy installation. However, PV systems can be affected by several external factors such as shadows. PV plants influenced by shadows not only decrease the supplied energy from the power system. They can also increase the risk of structural failures because of the increase of temperature and the localized hot spot. As a consequence, the study and emulation of PV systems under shaded conditions represent an important concern for the current integration of PV generators in distributed energy resources [2] [3].

Currently, in the field of PV system a research challenge is associated with the development of real-time simulation methods for shaded PV systems [4] [5]. This challenge arises from the high non-linearity and complexity of PV systems and their interaction with power converters which operate with high switching speed [6], control systems for maximum power extraction [7], and supervision and fault detection strategies [8] [9]. According to [10], accurate and simplified methods are required to emulate and better understand the shadow impact on PV generation. Authors in [11] also argue that modeling approaches still need improvement, but without increasing the computational complexity.

Shaded PV emulators has been proposed in several studies [12]. These emulators reproduce the shaded PV behavior using different approaches from analog circuit until advanced computational platforms [12]. Simplified methods use Look-Up-Tables for a discrete and predefined set of data in shaded conditions, such as in [13]. Other approaches amplified the current-voltage characteristics from a photosensor output [14]. Third methods consider different environmental and partial shading conditions [15] [16]. Most recently, reconfigurable PV emulators under static partial shading conditions are presented [12]. These emulation methods show some limitations in modeling the partial shading conditions because of the complexity of the shadow phenomenon. This complexity also trends to the deterioration of the output performance and accuracy in the PV emulators [17]. To tackle such limitations, it is required to develop PV emulators able to reproduce the PV system behavior under partial shading conditions given working conditions influenced by the shadow parameters at level of PV cells.

For the aforementioned reasons, we propose a methodology to emulate in real-time the behavior of shaded PV systems using the PV cell model for supervision Hardware-in-Loop applications intended to design and validate supervision and fault detection methods. The proposed methodology in this paper search to contribute with a mathematical framework to decrease the computational effort and to increase the processing speed in order to achieve the performance and accuracy requirements of real-time emulations of shaded PV systems.

The proposed methodology for Hardware-In-the-Loop simulations provides a design framework using the graphical Systems Modeling Language (SysML) and the High Level Specification of Embedded Systems (HiLeS). This approach employs SysML and HiLeS to develop customized computational models of shaded PV systems suitable to be implemented in a Field Programmable Gate Array (FPGA) [18]. In this case, the FPGA is selected as a computational device because of their adaptability and high speed processing features [19]. The modeling of shaded PV systems in FPGAs decreases the computation time and allows developing computational units able to be adapted to the non-linearity of shaded PV models.

Section II presents the theoretical model for PV modules. Section III discusses the employed numerical methods. Section IV introduces the tool HiLeS to implement the PV models in FPGA. Finally, simulation and experimental results are discussed.

## II. MATHEMATICAL MODEL OF SHADED PV MODULES

A typical partially shaded situation is shown in Fig.1. Current-voltage (I-V) and power-voltage (P-V) curves of this PV module are shown in Fig.2. These figures allow concluding that a reduced portion of the shaded PV module has an important impact on the I-V and P-V characteristics. In addition, Fig. 3 shows that partially shaded PV cells can increase their temperature. In order to better describe this issue, this section presents the theoretical concepts about the shaded PV behavior.

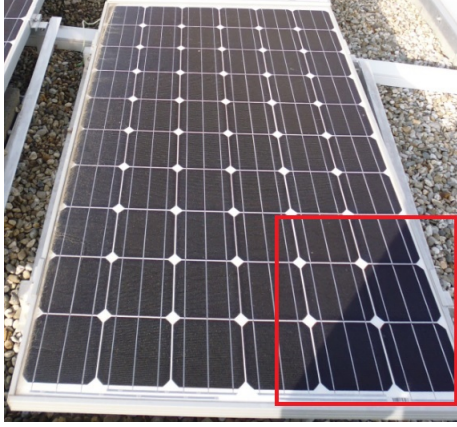


Fig. 1: Partially shaded PV module.

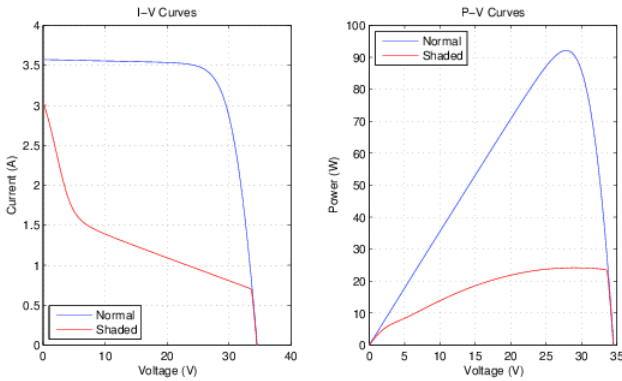


Fig. 2: I-V and P-V curves for a PV module under normal and shaded conditions.

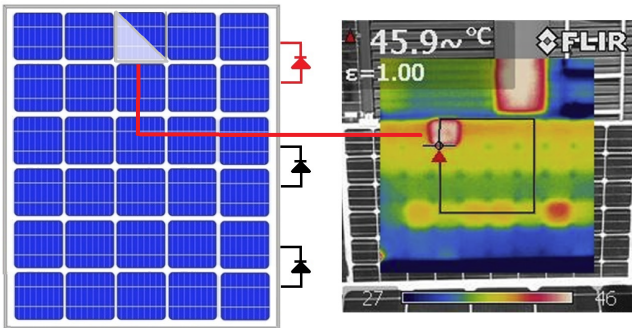


Fig. 3: Thermal impact of partially shaded PV cell.

### A. PV module behavior

PV modules are built by cell connected in series. As a result, the PV module voltage  $V_{pv}$  is given by the contribution of each PV cell,

$$V_{pv} = \sum_{i=1}^M V_{cn_i} + \sum_{j=1}^N V_{cs_j} + \sum_{k=1}^Q V_{cp_k} \quad (1)$$

where  $V_{cn}$  is the unshaded cell voltage,  $V_{cs}$  is the shaded cell voltage, and  $V_{cp}$  is the partially shaded cell voltage.  $M$ ,  $N$ , and  $Q$  specify the total number of each type of PV cell. Under shaded conditions, shaded cells can operate in reverse bias increasing the risk of structural failures [2]. Therefore, manufactures connect bypass diodes to group of cells in order to avoid cell damages as shown in Fig. 3. The group voltage  $V_G$  of PV cells connected to by-pass diodes is given by eq.(2),

$$V_{G_j} = \begin{cases} \sum_{i=1}^n V_{c_i} & \text{when } \sum_{i=1}^n V_{c_i} \geq 0 \\ V_{Bypass} & \text{when } \sum_{i=1}^n V_{c_i} < 0 \end{cases} \quad (2)$$

Then,  $V_{pv} = \sum_{j=1}^m V_{G_j}$  allows evaluating the voltage of a PV module with  $m$  groups

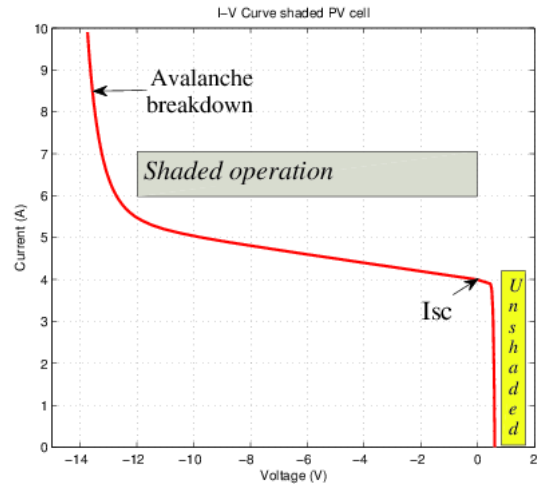


Fig. 4: I-V curve for a shaded PV cell.

### B. Shaded operation condition

Under shaded condition, the current through the shaded PV cell can be higher than the short-circuit current  $I_{sc}$ ; then, the PV cell is forced to operate in reverse bias, as shown in Fig. 4. According to Bishop [20], the reverse bias behavior can be modeled using eq. (3) where a non-linear multiplier factor  $M(V_d)$  is associated to the shunt resistor current (Fig. 5b).

$$0 = I_{ph} - I - I_0 \left[ e^{\left(\frac{V_d}{V_i}\right)} - 1 \right] - \frac{V_d}{R_p} \left[ 1 + k \left( 1 - \frac{V_d}{V_b} \right)^{-n} \right] \quad (3)$$

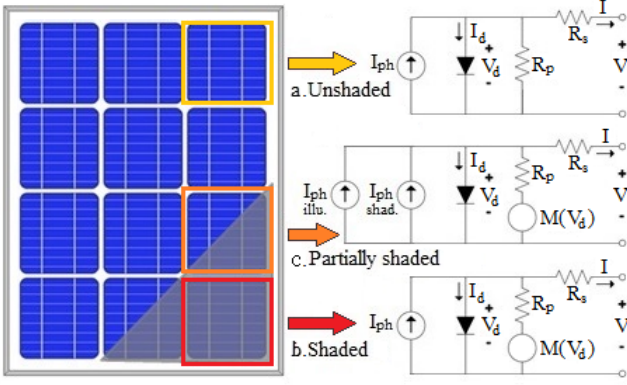


Fig. 5: PV cell characteristics according to shaded conditions.

Where  $k$  is the fraction of current involved in avalanche breakdown,  $V_b$  is the breakdown voltage, and  $n$  is the avalanche breakdown exponent.

### C. Proposed model for partially shaded condition

For this condition, we proposed a model taking into account the photo-induced current contributions from unshaded  $I_{ph_{ill}}$  and shaded  $I_{ph_{sh}}$  sides (Fig.5c).

$$I_{ph_{eq}} = I_{ph_{ill}} + I_{ph_{sh}} \quad (4)$$

In terms of current densities,

$$J_{ph_{eq}} A_{eq} = J_{ph_{ill}} A_{ill} + J_{ph_{sh}} A_{sh} \quad (5)$$

Experimental results show that photo-induced density current in a shaded PV cell is given by  $J_{ph_{sh}} = J_{ph_{ill}} \tau$ , where  $\tau$  is the shadow transmittance [21]. Thus,

$$J_{ph_{eq}} = (a_{ill} + a_{sh} \tau) J_{ph_{ill}} \quad (6)$$

where  $a_{sh}$  and  $a_{ill}$  are the percentage of shaded and illuminated areas. Let  $A = A_{eq}$  be the cell area, and  $I_{ph_{T}}$  the photo-induced current for the totally illuminated or shaded cell. Then,

$$I_{ph_{eq}} = (a_{ill} I_{ph_{T_i}} + a_{sh} I_{ph_{T_s}}) \quad (7)$$

### III. NUMERICAL APPROACH TO SIMULATE THE SHADED PV CELL MODEL

Emulation of shaded PV systems requires powerful processing devices such as FPGAs. However, the implementation in FPGAs of these complex models needs suitable numerical methods to accomplish with performance and design constraints for these devices. Therefore, this section explains the proposed numerical method to implemented shaded PV models in FPGA.

#### A. General PV cell equation

Solution of eq.(3) describes the behavior of shaded PV systems. The numerical method usually employs to solve this type of non-linear equations is the Newton-Raphson method [11]. This iterative numerical method is given by,

$$V_{dn+1} = V_{dn} - \frac{f(V_{dn})}{f'(V_{dn})} \quad (8)$$

Eq.(8) shows that implement the Newton-Raphson method requires a high degree of computational effort due to the evaluation of  $f'(V_{dn})$ . As a result, we proposed employing a modified Newton-Raphson method. This proposed method evaluates the discrete derivative of  $f(V_{dn})$  from,

$$f'(V_{dn}) = \lim_{h \rightarrow 0} \frac{f(V_{dn} + h) - f(V_{dn})}{h} \approx \frac{f(V_{dn} + \Delta V) - f(V_{dn})}{\Delta V} \quad (9)$$

figure

where  $\Delta V$  is selected to ensure the quadratic convergence for the proposed method. The modified Newton-Raphson method is then,

$$V_{dn+1} = V_{dn} - \frac{(\Delta V) f(V_{dn})}{f(V_{dn} + \Delta V) - f(V_{dn})} \quad (10)$$

Eq.(10) decrease the computational effort because the function  $f(V_d)$  is only evaluated and not  $f'(V_d)$ .

### IV. HiLES PLATFORM FOR SUPERVISION HARDWARE-IN-THE-LOOP (HIL) OF SHADED PV MODELS

This section presents the free license tool HiLeS for the designing and implementation of embedded systems. HiLeS is used through this study to develop a real-time Supervision HIL emulation of shaded PV systems in FPGA. This Supervision HIL system allows emulating the behavior of PV systems in normal and shaded condition to evaluate supervision and fault detection methods.

#### A. HiLeS platform

The HiLeS [22] uses the graphic SysML standard to represent structurally and behaviorally the system models to be implemented. The use of SysML diagrams provides and structural design strategy which allows integrating several engineering fields in a common standard [18]. Representative diagrams of SysML [23] are Block Definition Diagrams (BDD), Internal Block Diagrams (IBD), and Activity Diagrams. SysML uses Block Definition Diagrams to describe structural composition of systems, and Internal Block Diagram to define the interconnections among the system components. Furthermore, SysML describes the system behavior by means of Activity Diagrams.

The HiLeS platform can automatically transforms the SysML diagrams designed to described PV systems in the HiLeS formalism. This formalism is an extension of Petri nets which allows a formal structural analysis before implementation of Hardware-in-the-Loop PV models in order to avoid undesired computational behavior.

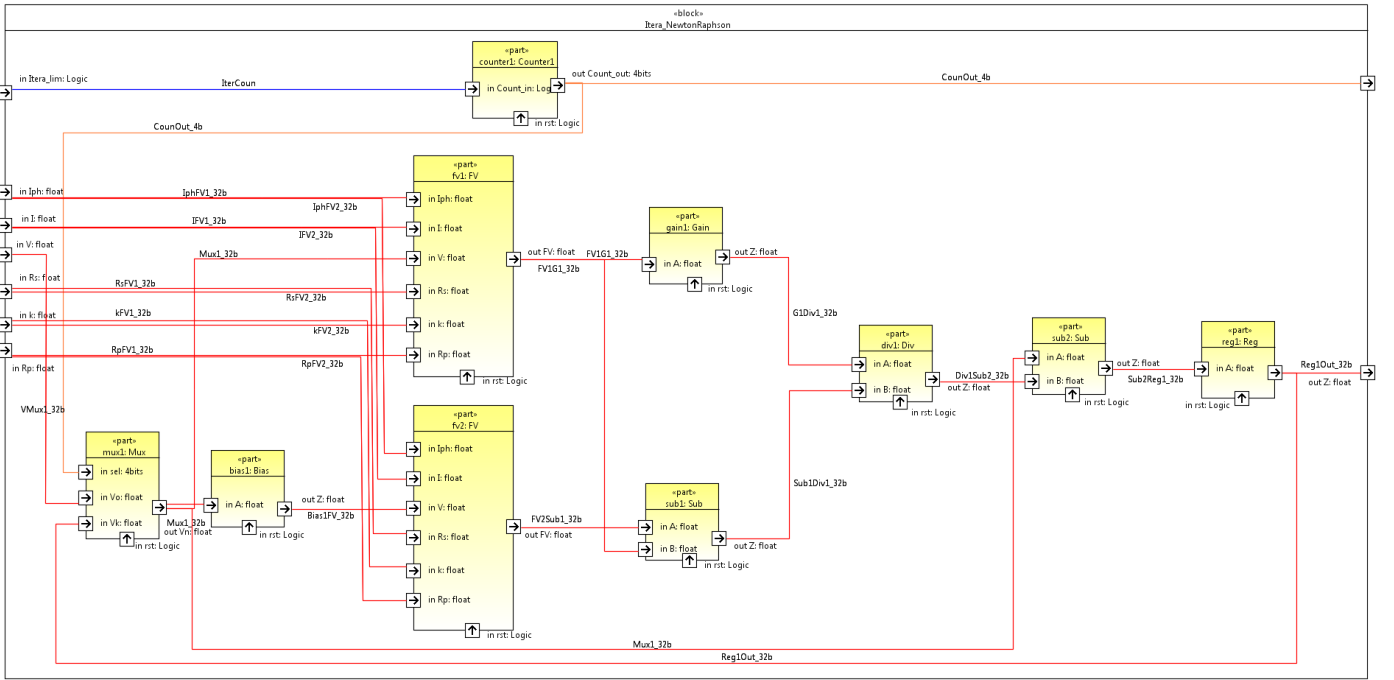


Fig. 6: IBD modified Newton-Raphson method.

Main advantage of using SysML diagrams in the HiLeS platform is their representation in Petri nets according to the transformation rules defined in [22]. This representation based on control Petri nets allows an automatic generation of VHDL code for HIL applications. In this platform, designers can define the FPGA resource use from SysML Internal Block Diagrams; additionally, users can describe the operation sequence and the suitable task distribution from Activity Diagrams.

### B. SysML representation of shaded PV systems

In this section is described the FPGA-based computational unit developed to emulate in real-time the behavior of shaded PV systems using HiLeS and the SysML diagrams.

Block Definition Diagrams (BDD) in SysML allows to describe the structure and hierarchy of systems. For PV system HIL modeling, this study proposes to use BDD to define the components that will be employed to implement the model in FPGA. Internal Block Diagrams (IBD) are used to describe the interaction among elements. Fig. 6 represents the IBD to implement the proposed numerical method from eq.(10). In Fig. 6 the yellow blocks represent the computational elements in the FPGA, and lines show the data flow with the data type.

Finally, Activity Diagrams are used in this approach to describe the operation sequence. Activity Diagrams allows to depict and take advantages of parallel processing in FPGA as shown in Fig. 7. Additionally, Activity Diagrams are useful to identify issues and delays in the execution of operations. Fig. 7 shows the Activity Diagram for the operation sequence to assess the modified Newton-Raphson method from eq. (10).

figure

## V. RESULTS

The developed supervision Hardware-in-the-Loop platform for emulation of shaded PV systems is shown in Fig. 8. In this platform, a digital patron for irradiance, temperature, and shadow profile is provided to the FPGA. As result, FPGA evaluates the shaded PV model and generates digital signals able to drive DACs or power devices to emulate the PV module behavior. Additionally, this platform stores the I-V resulting curves to further analysis of supervision and fault detection methods. Calculation results are compared with a conventional computational approach for a PV module with a single shaded cell as shown in Fig.9. The execution time for this shaded PV model is around  $8.3\mu S$  which is a suitable time for real-time applications. Table I summaries the used hardware and Table II presents the calculus error comparison with a conventional computational approach.

Fig.10 depicts the experimental results for a PV module in normal operation. Fig.11 represents the measurements for the emulation of a PV module with a shaded cell and by-pass activation. Finally, Fig.12 shows the results for a PV module with a shaded cell and by-pass diode in fault condition. These results allow validating the proposed approach to emulate PV modules in actual working conditions able to develop further supervision and fault detection strategies.

TABLE I: Hardware used for emulating the shaded PV systems

Device	Reference	Description
FPGA	XC7Z020	Look-Up Tables 15%; Flip-flops 5%; DSP 10%
DAC	AD5541A	High-speed 16-bit DAC.

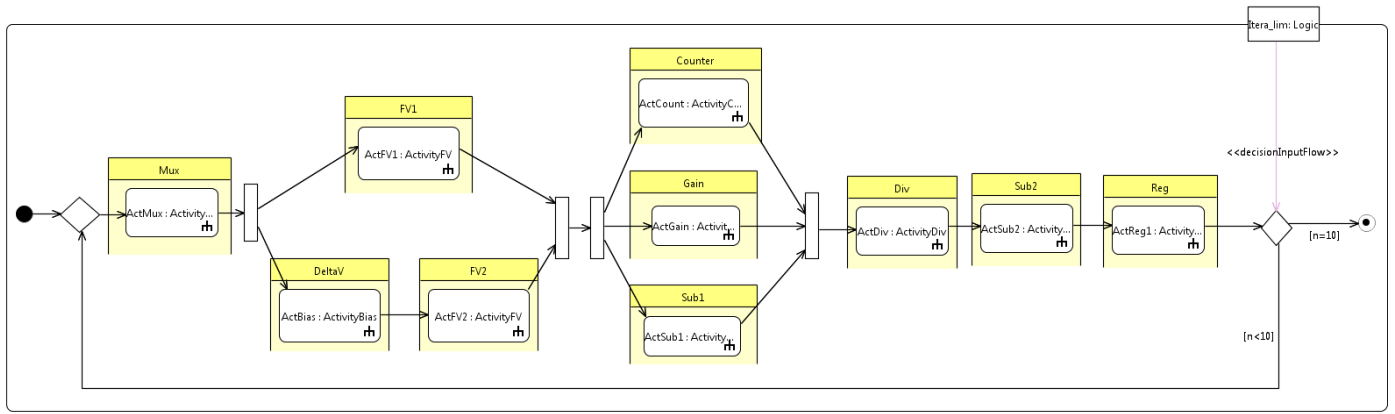


Fig. 7: Activity Diagram for modified Newton-Raphson.

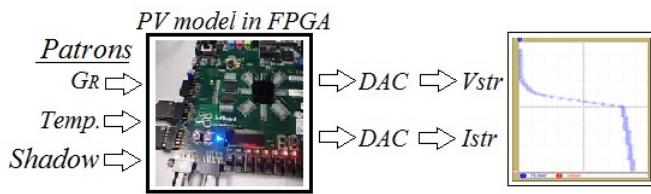


Fig. 8: Real-time FPGA-based platform for emulation of shaded PV systems.

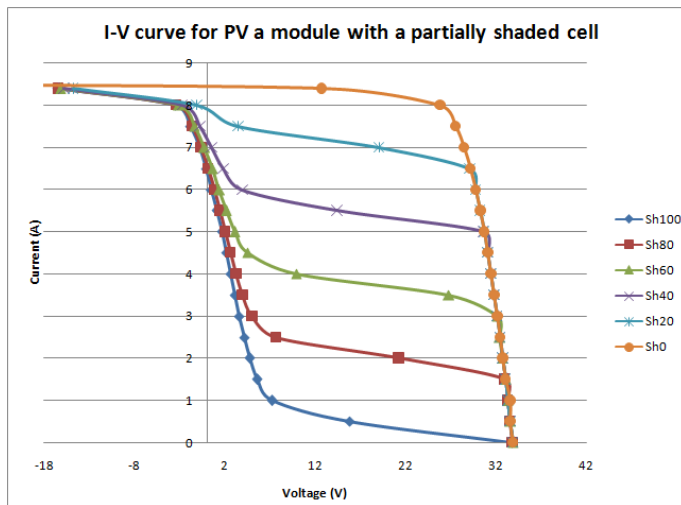


Fig. 9: Calculated I-V curve for a PV module with a single shaded cell and several partial shaded areas without by-pass diodes.

TABLE II: Comparison with calculus in a conventional computational approach

Shaded area	Mean Square Error	Mean Absolute Error
0%	$0.064 \times 10^{-8}$	$0.188 \times 10^{-4}$
20%	$0.123 \times 10^{-8}$	$0.264 \times 10^{-4}$
60%	$0.264 \times 10^{-4}$	$0.154 \times 10^{-4}$
100%	$0.096 \times 10^{-8}$	$0.264 \times 10^{-4}$

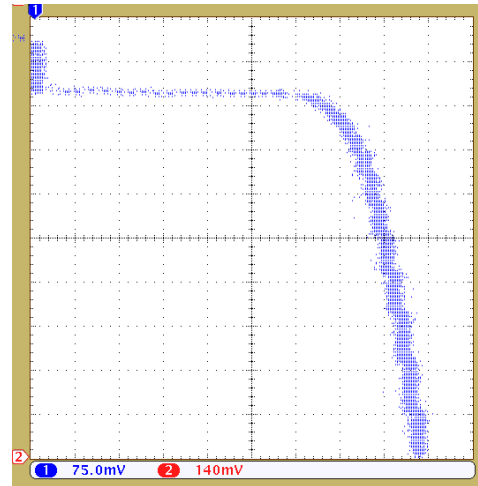


Fig. 10: I-V curve emulation of a PV module in normal operation.

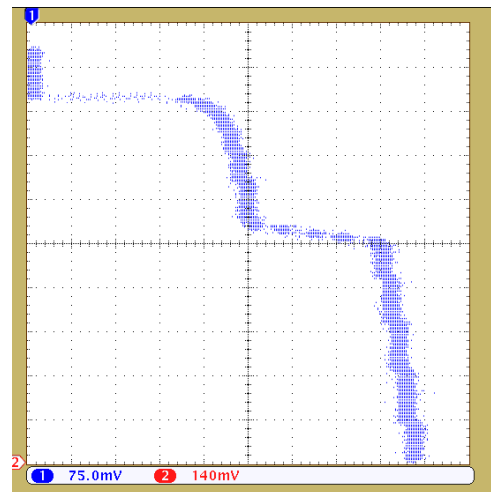


Fig. 11: I-V curve emulation of PV module with single shaded cell and activation of by-pass diode.

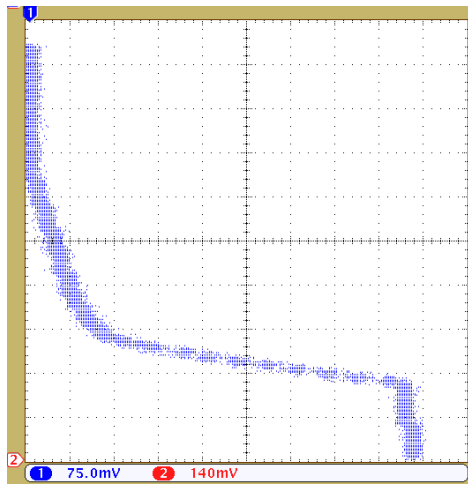


Fig. 12: I-V curve emulation of PV module with single shaded cell and fault in by-pass diode.

## VI. CONCLUSION

This paper presented an alternative methodology to implement shaded PV models in an emulation platform. Given the non-linearity and complexity of implemented PV models in FPGA, a modified Newton-Raphson numerical approach was proposed to simplify the computational effort. The proposed methodology based on the High Level Specification of Embedded Systems (HiLeS) and the System Modeling Languages (SysML) allowed emulating shaded PV systems in FPGA with high degree of accuracy. Further applications for the developed shaded PV emulation platform include the study of interactions with real-time supervision and fault detection strategies.

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