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Micro-strip slow wave line for phase shifting cells

M. Gastaldi, D.Dragomirescu, A.Takacs, V.Armengaud and S. Rochette

This paper addresses the design, simulation and measurements of microstrip slow wave lines implemented in a 0.25 µm SiGe BiCMOS process for Ku-band (10 GHz – 15 GHz) applications. The simulation results and the measurements show better performances for the proposed microstrip slow wave line compared to the classical microstrip transmission line. These lines present very low insertion losses and a high phase constant.

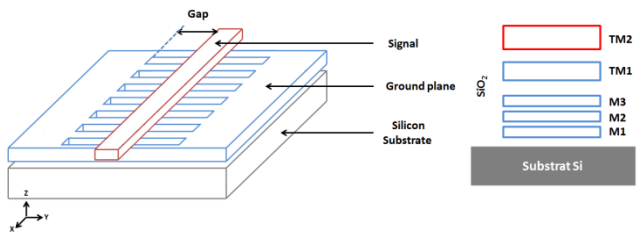
Introduction: Slow Wave Lines (SWL) are a specific topology of transmission lines that uses the slow wave phenomenon in order to miniaturize the physical length of a line [1, 2]. Nowadays, CMOS and BiCMOS (Bipolar CMOS) technologies are more and more used for microwave circuits [3] and become a promising candidate for core-chip circuits used in the satellite Beamforming Antenna Control Systems (BACS). Mainly for the phase shifter of BACS the use of microstrip lines require an important area on the chip. The SWL technology can be a valuable candidate for minimizing the occupied area on the chip by the microstrip lines used for interconnection or phase shifting [2],[4, 5].

The most common transmission lines implemented using SWL technology are the Shielded Coplanar Waveguide (S-CPW) [2]. Nevertheless Shielded MicroStrip Lines (S-MSL) can be designed. This particular type of SWL allows a very compact structure because a large gap is not required. This paper addresses the design the simulation and the experimental results of S-MSL implemented in a 0.25µm BiCMOS process from IHP.

Results:

The stack layers of the used BiCMOS process are represented in Fig. 1. The back end of this technology offers five metal layers: three thin aluminum layers and two thick layers fit for transmission lines and inductors design.

The position of the metal strips forming the ground plane varies for the two structures presented in this paper. The signal line is always located on the superior metal layer (TM2) while the periodic metal strips are located on the Top Metal 1 layer – TM1 (design 1) or, on the layer TM1 and M3 (design 2). The two thick metal layers TM2 and TM1 are separated by a 2 µm layer of SiO2. The capacitance per unit of length (C) is maximized by positioning the metal strips on the layers closest to the signal. However, even in this configuration, the value of the capacitance per unit of length is relatively small conducting to a poor quality factor.



a *b*

Fig. 1 *Proposed microstrip Slow Wave Line (S-MSL) in BiCMOS process*

a Simplified structure

b Cross-section of the 0.25µm BiCMOS process

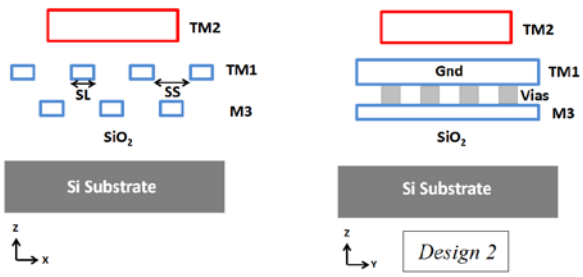


Fig. 2 *Cross-section view of the S-MSL structure*

The metal strips in the second design are connected by vias (Fig. 2). This disposition of these strips prevents more effectively the E-field from penetrating inside the substrate and thus improves the quality factor Q.

The metal strips are disposed orthogonally to the direction of propagation so the return currents cannot flow directly under the signal contrary to classical micro-strips lines. By making these currents flow far away from the signal line, it is then possible to artificially improve the inductance per unit of length (L). A diminution of the phase velocity for a transmission line can be achieved by controlling C and L.

$$v_p = c/\sqrt{\mu_r \varepsilon_r} = 1/\sqrt{LC} \qquad (1)$$

where L is series inductance per unit length and C denotes shunt capacitance per unit length.

The structures (S-MSL and MSL) implemented in 0.25µm SiGe BiCMOS process were electromagnetically simulated using HFSS software. Manufactured samples were also measured by using a VNA (Anritsu ME7808A VNA). The S-parameters, attenuation (α) and phase (β) constants were measured/extracted after de-embedding. A special designed Thru, Reflect, Line (TRL) calibration kit was manufactured on the die for de-embed the impact of the microstrip access lines (length: 150 µm) on the S-MSL.

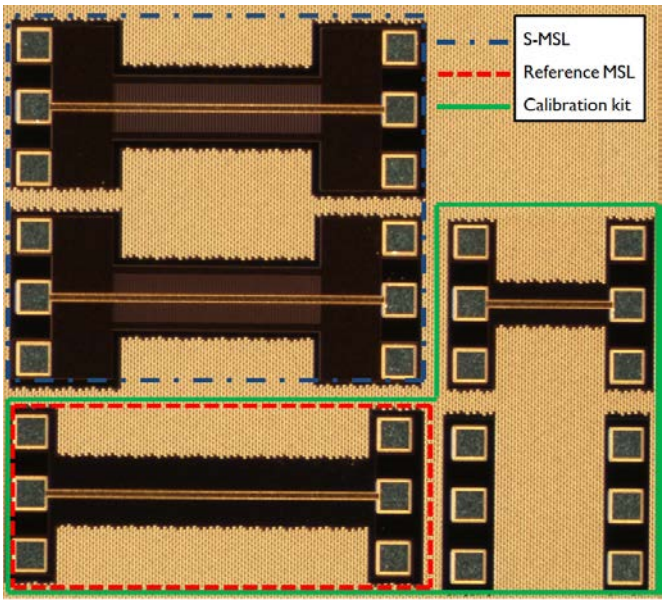
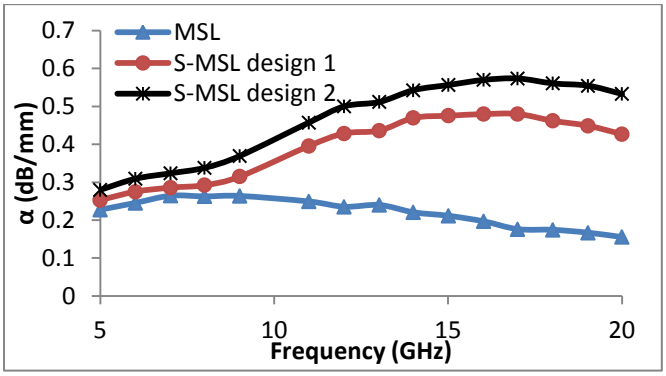


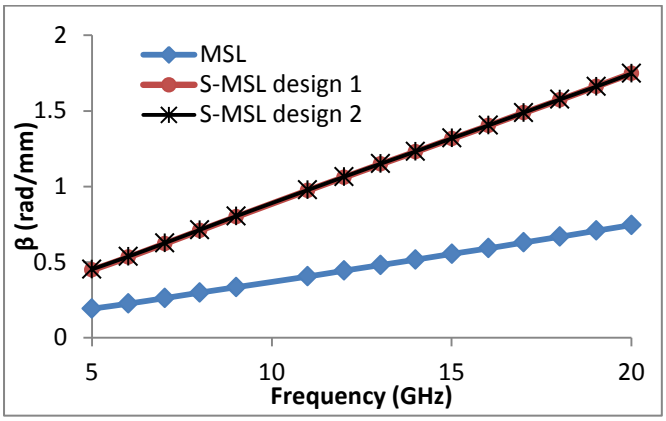
Fig. 3 *Layout photograph of the manufactured die including a reference microstrip line, S-MSL and the TRL calibration kit*

S-parameters measurements were performed with a VNA using a standard SOLT calibration procedure following by the TRL calibration. A layout view of the structures is shown on Fig. 3. The lines are 500 µm long (a minimum length of 300µm is required to avoid measurement errors due to the coupling between the probes). The reference MSL is also used as 'line element' in the TRL kit (Fig. 3 bottom left corner). The S-MSLs are preceded by a line length of Thru/2 that will be removed by de-embedding.

Fig. 4 shows the different measurements and the comparison between S-MSL and MS line. The width of the MSL signal line is w=15 µm conducting to a characteristic impedance of 50Ω for the reference MSL. The S-MSLs presented here were obtained after the optimization of three geometrical parameters: SL (the width of the metal strips shown Fig. 2), SS (the strip spacing Fig. 2) and the Gap (the distance between the signal line and the ground plane cf Fig.1). The strip spacing was chosen to minimize the eddy currents loss (SS = 6µm, SL = 2µm).



a



b

Fig. 4 *Comparison between MSL and S-MSL performances (measurements)*
a Attenuation constant (dB/mm)
b Phase constant (rad/mm)

The experimental results of the phase constant β show that the structures are working for Ku-band. However the attenuation of the first S-MSL is 0.42 dB/mm (0.5 dB/mm for design 2) at 12.5 GHz versus 0.24 dB/mm for the MSL. The reference MSL have a quality factor inferior to S-MSL structures. The differences between MSL and S-MSL appear also on Fig. 4 (a).

The simulations results (not detailed here) demonstrated that closer to the signal is the ground plane more α and β decreases. The gap must be sized as function of the system specifications (losses and capacity). According to this work, a reduction about of 58% can be expected for the length of the transmission line by using a M-SWL instead of a classical MSL for a targeted phase shift. A 1.78mm long conventional MSL is necessary to achieve a 45° phase shift (insertion loss of 0.3-0.4dB). For the same phase shift a length of only 740 µm is required with the S-MSL (insertion loss of 0.25-0.34dB). The gap of the fabricated S-MSL is 50 µm and is relatively small compared to other SWL at 12.5 GHz.

Conclusion: This paper presented two designs of S-MSL implemented in 0.25µm SiGe BiCMOS technology. The experimental results show an improvement of the phase constant by a factor 2.4 (β is improved by 2.4 at 12.5GHz) compared to the reference MSL while the attenuation constant is not strongly impacted. Thus the proposed S-MSLs are a very interesting candidate for phase shifting cells.

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