# High Current Ripple for Power Density and Efficiency Improvement in Wide Bandgap Transistor-Based Buck Converters

Bernardo Cougo, Henri Schneider, Thierry Meynard

# High Current Ripple for Power Density and Efficiency Improvement in Wide Bandgap Transistor-Based Buck Converters

Bernardo Cougo, Henri Schneider, and Thierry Meynard, *Senior Member, IEEE*

With the recent development and availability of wide bandgap devices in the market, more and more power converters are being designed with such devices. Given their fast commu-tation, when compared to their equivalent Si-based counterparts, these new devices allow increasing the converter's efficiency and/or power density. However, in order to fully avail these new devices, one should precisely know their switching characteristics and ex-ploit it the best way possible. This paper recalls our own precise method to measure separately turn-on and turn-off energies of wide bandgap devices. This method is applied to commercially available SiC and GaN transistors and results show that they present much lower turn-off than turn-on energies. For that reason, we show that a SiC-based buck converter must have high current ripple in the output filter inductor in order to decrease transistor losses. Anal-ysis of these losses as well as experimental results are presented. Finally, the precise design of a 2-kW SiC-based buck converter for aircraft applications is performed for different current ripples and switching frequencies. We show that current ripple higher than 250% of the dc load current significantly decreases the converter's losses, and consequently allows the increase of the switching fre-quency, which reduces the system volume and weight.

*Keywords*—Buck converter, converter design, silicon carbide MOSFET, switching losses, zero voltage switching.

## I. Introduction

WIDE bandgap (WBG) devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) transistors, are nowadays being used in different applications with the purpose of decreasing the converter losses and/or increasing the converter power density [1], [2]. When compared to silicon-based devices with the same on-state resistance, WBG devices can switch faster, resulting in lower switching losses. Also, they allow converters operating at higher switching frequencies, which generally reduces the volume of passive components placed in the converters and consequently increases the converter power density. Besides that, WBG devices may operate at higher junction temperature when compared to Si-based devices, with the consequent reduction of the cooling system volume [3], [4].

SiC devices are usually used in applications, where the switched voltage is higher than 500 V and the switched current is not higher than 60 A, since most of the SiC transistor manufacturers produce devices having 1200-V breakdown voltage [5] and on-state resistance from 25 to 450 mΩ. However, some high current applications, such as traction-related applications, develop modules having many SiC dies directly connected in parallel, achieving much higher current capabilities [6], [7]. In order to achieve higher switching voltage, one option is to series connect SiC transistors, as shown in [8], [9], where authors developed a 25-kW isolated dc/dc converter, switching 5 kV at 50 kHz. Each switch was composed of five series-connected normally-on SiC-JFET cascaded with a low-voltage normally-off silicon MOSFET. Also, high-voltage SiC components have been developed and evaluated, notably 12-kV IGBTs and 10-kV MOSFETs [10].

Most of the applications in power electronics using GaN devices have switching voltages in the range of 12–100 V. This is mainly due to the fact that the only commercially available GaN transistors have breakdown voltages from 40 to 200 V [11]. In order to achieve higher current capabilities, direct parallel connection of devices is possible, although switching performance is reduced when more than two devices are directly connected in parallel [12]. Thus, a solution is to connect commutation cells in parallel. This is done in [13], where a five-phase magnetically coupled and interleaved buck converter using EPC1001 GaN transistors was developed. Videau *et al.* achieved efficiency of up to 97% for a 1.8-kW 48-to-24 V conversion, switching at 300 kHz (output ripple at 1.5 MHz due to the interleaving technique). High-voltage applications depend on not-on-the-market components, such as the 600-V GaN HEMT in cascode structure presented in [14]. With this component, authors built a 1-MHz 300-W 400-to-12 V *LLC* converter. Due to the zero-voltage switching characteristic of the structure, the converter can achieve efficiency of 96%, which is 1% higher than that of a converter made with a silicon-based MOSFET.

Although, WBG devices have reduced losses when compared to their silicon-based counterparts, converters made with these components can have even lower losses if they are used in the best way possible, i.e., if the sum of the switching and conduction losses is minimized.

Reducing transistor losses can be achieved by the use of soft-switching techniques. Zero-voltage switching (ZVS) techniques are usually employed when converters are composed of

B. Cougo is with the LAAS Laboratory, Av. du Colonel Roche, 31031 Toulouse, France and also with the Laplace Laboratory, Rue Camichel, 31071 Toulouse, France (e-mail: cougo@laplace.univ-tlse.fr).

H. Schneider is with the LAAS Laboratory, Av. du Colonel Roche, 31031 Toulouse, France (e-mail: hschneid@laas.fr).

T. Meynard is with the LAPLACE Laboratory, Rue Camichel, 31071 Toulouse, France (e-mail: thierry.meynard@laplace.univ-tlse.fr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

MOSFETs, since the energy stored by the power switch in the parasitic capacitance can be restored to the system and not be dissipated in the switch channel [15].

ZVS can be achieved by the use of resonant circuits, which imposes a current in the switch such that the transistor is always switched ON when its body diode is conducting [16], [17]. ZVS operation is also possible by specific circuit topologies which naturally provide ZVS conditions (e.g., dual active bridge converters [18]), or by converters with auxiliary switches [19] and/or auxiliary components such as coupled inductors [20].

Techniques mentioned above to reduce switching losses either make use of extra passive and/or active devices, or are restricted to converter topologies which naturally provide ZVS conditions. Standard converters, such as a simple buck, can achieve ZVS operation without the use of extra components. This can be done if the transistor switching energies are precisely identified for the whole switched voltage and current ranges, and some adaptation in the converter parameters is realized so the transistors operate in the best possible condition. This is what we show in this paper for a buck converter realized with WBG transistors.

For that, a method to precisely determine turn-on and turn-off energies of WBG devices is recalled in Section II, where also some switching energy curves for different voltages and currents are shown for SiC and GaN devices.

Considering the switching energy curves related to SiC MOSFETs, Section III shows that there are specific high current ripple values in the output of SiC-based buck converter which minimize the transistor losses, for a given output load and switching frequency. This is experimentally verified in Section IV, where the losses of a buck converter using SiC MOSFET transistors are measured by means of the opposition method [21], [22].

High current ripple in the output of a bridge leg increases conduction losses in the transistor and also in the inductors and capacitors used in the output filter. Thus, Section V shows the design of a 2 kW 540-to-270-V buck converter and the calculation of losses in the bridge leg components as well as in the output filter inductor and capacitor, for different output current ripple values. Also, volume and weight of the filter and heatsink attached to the transistors are calculated. As a result, we show that there are different values of output current ripple which minimize the total converter losses, volume and weight, for a given switching frequency. The optimal output current ripple values are always high (from 250% to 280% of the output DC current), which is much higher than what is usually chosen in standard design of converters [23].

Note that analysis presented here can be also applied to converters with silicon-based transistors, which present much higher turn-on energies than turn-off energies, such as fast MOSFETs with breakdown voltage from 400 to 900 V.

## II. Switching Losses of WBG Devices

It is necessary to precisely measure switching energy of WBG devices in order to optimize the use of such devices in a given converter. The most common method to measure losses in transistor is frequently called the "double pulse" method [24], [25],

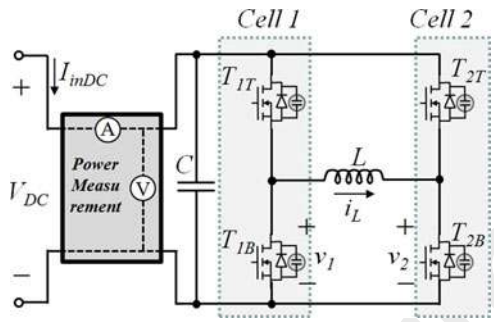



Fig. 1. Full bridge used to accurately measure switching energy of WBG transistors. Body diode and parasitic capacitance of transistor are represented.

where the transistor to be measured is inserted in a simple buck converter with a simple inductor load. A first pulse in the gate voltage of the transistor makes the current rise up to a chosen value. At this value, the transistor is turned OFF and then turned ON again. The current flowing through the transistor and the voltage over the transistor are measured using an oscilloscope at the switching instants and the instantaneous product of these two values is performed, to find the instantaneous power dissipated in the switch. The time integral from the beginning until the end of the commutation gives the turn-off and turn-on energies. However, this method has serious drawbacks, especially when WBG transistors are considered. The two most important of these drawbacks are listed below.

1) As explained in [21], when the transistor is turned ON, its parasitic capacitance is discharged through the transistor channel. The discharge current is not measured by the current sensor used to measure the transistor current during turn-on commutation and as a consequence the calculated switching energy may be inaccurate. Also, when the transistor is turned OFF, its parasitic capacitance is charged. The charge current is measured by the current sensor, but this energy is not lost during turn-off commutation.
2) In order to measure the current of a transistor, either a shunt resistor or a current transformer can be used. Both solutions change the resistance and inductance of the commutation loop. This changes the switching behavior of the transistor under test.

The method used in this paper to measure switching losses of SiC and GaN devices, and which was first presented in [21], includes the losses due to the parasitic capacitance discharge and it is applied to the transistor placed in a PCB with exactly the same conditions of the converter where the transistors will be used: same gate driver, same gate and commutation loops and same parasitic inductances and capacitances.

In this method, a PCB is conceived with four identical transistors which will be tested. A full bridge is designed with a gate driver and a PCB layout as close as possible to the final converter which will be designed with the tested devices. An inductor is connected between the outputs of each half-bridge, as shown in Fig. 1.

In order to measure turn-on and turn-off losses separately, measurements in two different modes must be done. In the first mode, an ac current at the switching frequency is imposed

through inductor $L$ (see Fig. 1). In this way, transistors will only present turn-off losses, which can be calculated by using the measured losses of the converter. In the second mode, a dc current is imposed through inductor $L$. Thus, transistors will present turn-on and turn-off losses. Since turn-off losses were already calculated by the measurements in the first mode, one can then calculate turn-on losses by using the measured losses of the second mode. Both modes are explained in detail in [21].

The same dc bus is connected to both commutation cells and different current waveforms can be imposed in the inductor by modifying the duty cycles of both cells and the phase-shift between them. As can be seen in Fig. 1, the power measured by the power measurement block (composed by a simple dc voltmeter and dc ammeter) is the total power dissipated by the system for a given operation point. In order to have an accurate measurement of switching losses, the other losses in the system must be negligible or at least well known to be able to be subtracted from the total losses. These other losses are listed below.

1) *Inductor losses:* they are usually divided between core and copper losses. A coreless inductor is usually enough to achieve the desired inductance value. Thus, only copper losses are observed in the inductor and they are usually low and can be easily calculated using a large cross-section litz wire.
2) *Transistor conduction losses:* the on-state resistance of each transistor in the experimental setup can be measured by regular static measurements, for different currents, gate-source voltages and temperatures, if necessary. Conduction losses can be calculated with these values and also with the RMS value of the current flowing through them.
3) *Connection losses:* These are mainly related to the copper on the PCB connecting the transistors and the passive components. These losses are very low when compared to the other losses and the resistance of these connections can be measured at different frequencies. The resistance of such connections at higher frequencies does not significantly increase since the copper thickness (typically 0.035 or 0.07 mm) is smaller than the skin depth of the copper at the desired switching frequencies (0.15 mm at 200 kHz, for example).
4) *Bus capacitor losses:* when designing a full bridge PCB, a high-dc bus capacitor value can be used. Thus, its series resistance is low and negligible losses on the capacitor are observed.

### A. Switching Energy of WBG Devices

The method explained above was used to measure switching energy of different WBG devices at different voltage and current levels. Both SiC and GaN devices tested with this method have body diodes, which present negligible reverse recovery energy, as stated by manufacturers. Fig. 2 illustrates the measured switching energy of the 1200-V SiC MOSFET CMF20120D from manufacturer CREE, which has on-state resistance of 80 mΩ. In this figure, the turn-on energies are shown in the left side of the graph (corresponding to negative values of current) and turn-off energies are shown in the right side of the graph (corresponding to positive values of current). This current sign convention (negative for turn-on and positive for turn-off) is convenient to explain the switching losses in a commutation cell as it will be seen in Section III.

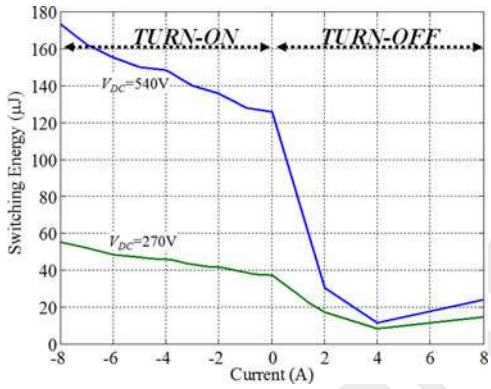



Fig. 2. Measured switching energy for different switched currents and voltages (270 and 540 V), for the 1200-V SiC MOSFET CMF20120D at 25 °C.

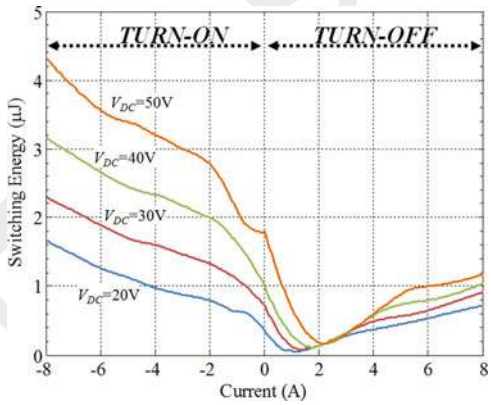



Fig. 3. Measured switching energy for different switched currents and voltages, for the 100-V eGaN FET EPC1001.

Measurements were performed for two different voltages typically used in the aeronautic environment (270 and 540 V), for dead time equal to 100 and 200 ns, respectively, for gate resistance of 1 Ω and for gate voltages of –2 and 20 V. The "dead time" is defined as the time between the gate signal which turns OFF one transistor of a commutation cell and the gate signal which turns ON the other transistor of the commutation cell. Results are shown for transistors at room temperature (25 °C) and for switched currents up to 8 A. Energies at higher currents grow quasi-linearly with current as shown in [25] and this consideration will be used in loss calculation of next section.

The same method was applied in [26] to measure the switching losses of the 100-V/25-A eGaN FET, reference EPC1001, from manufacturer EPC. Results are shown in Fig. 3 and were obtained for different switched voltages and currents, using a dead time of 26 ns, gate resistance of 1 Ω, and gate voltages of 0 and 5 V.

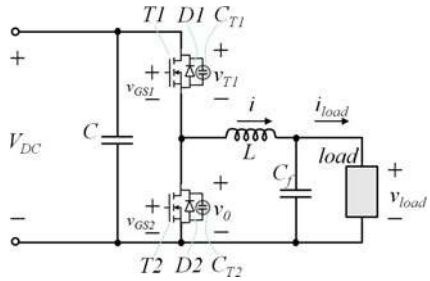



Fig. 4. Simple buck converter with output *LC* filter. Transistors *T1* and *T2* are represented with their body diode and parasitic output capacitance.

Regarding the results of both WBG components (see Figs. 2 and 3), turn-on energies are always higher than turn-off energies, for the same switched current and voltage. This is also valid for high-junction temperatures, as shown in [25]. Note that the higher the switched voltage, the higher the difference between turn-on and turn-off energies. For example, the SiC component (see Fig. 2) switching 8 A at 270 V has turn-on energy around three times higher than the turn-off energy while at 540 V the turn-on energy is around 7.5 times higher than the turn-off energy. This difference is mainly due to losses caused by the switch's parasitic capacitance.

As in standard silicon MOSFET, switching energy at zero current is mainly due to the charge and discharge of parasitic capacitance of transistors. Turn-off energy at low current is high given the fact the switch's parasitic capacitance is not completely charged/discharged by the load current during the dead time. Thus, curves in Figs. 2 and 3 may be different for different dead times, as explained in details in [21], [26].

It is interesting to observe that since the turn-off energy is much lower than turn-on energy, especially in the region of around 4 A for the SiC device (see Fig. 2) and around 2 A for the GaN device (see Fig. 3), high-efficiency converters using these devices should operate in such a way that they avoid switching ON current and as a result only switch OFF the current. This is usually the case in isolated dc/dc converters working in zero-voltage switching (ZVS) conditions [27], but this is not natural in regular buck converters. However, if extremely high current ripple (e.g., higher than the double of the output dc current) is allowed, only switch-off commutation will be observed in buck converters. This will be explained in the next section using the SiC MOSFET CMF20120D as the reference transistor.

## III. Losses of a Commutation Cell Using SiC MOSFET

A simple buck converter is composed of a bus capacitor, a commutation cell, and an *LC* filter in the output, as shown in Fig. 4. In this figure, $V_{\rm DC}$ is the voltage on the dc bus and $v_{\rm load}$ is the dc voltage across the output load. For a given duty cycle $D$ and switching frequency $f_s$ (and period $T_s$), if the capacitance $C_f$ is high enough so the load voltage has negligible ripple, the current ripple $\Delta I$ in the inductor is given by

$$\Delta I = D \cdot (1 - D) \cdot \frac{V_{\rm DC}}{L \cdot f_s} \qquad (1)$$

where $L$ is the value of the output filter inductance.

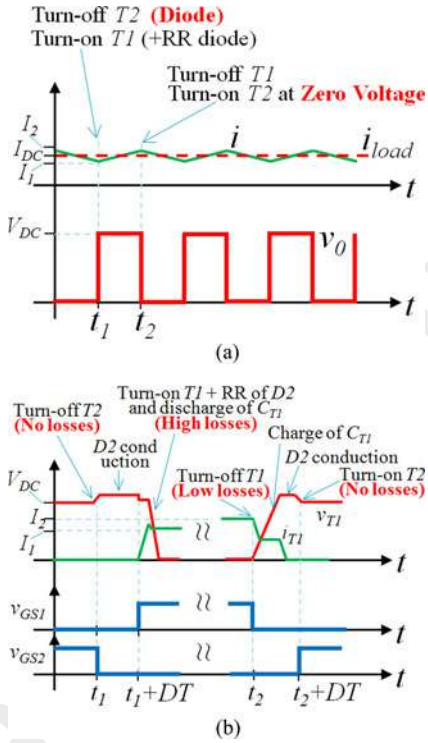



Fig. 5. (a) Load and inductor currents in a buck converter having low current ripple; (b) zoom on the commutation of transistor *T1*. When current ripple is low, the top transistor (*T1*) has turn-on and turn-off losses while the bottom transistor (*T2*) only switches at zero voltage.

Figs. 5 and 6 show the waveforms of the commutation cell voltage $v_0$, inductor current *i,* and load current $i_{\rm load}$, for a resistive load. The dc current in the load as well as in the inductor is equal to $I_{\rm DC}$. In Fig. 5, the filter inductance is high and the current ripple is low (about 20% of $i_{\rm load}$ in this example), while in Fig. 6, the filter inductance is low and, as a consequence, the current ripple is so high (about 250% of $i_{\rm load}$ in this example) that the converter switches a negative current (at instant $t_1$). These two modes will be discussed below.

### A. Low-Current Ripple Mode

Considering the low-current ripple mode [see Fig. 5(a)], at instant $t_1$, the commutation cell voltage $v_0$ goes from zero to $V_{\rm DC}$. This happens because first transistor *T2* is turned OFF and after the dead time *DT*, transistor *T1* is turned ON. When *T2* is turned OFF (and before *T1* is turned ON), the inductor current starts flowing through the body diode of *T2*. Thus, *T2* is turned OFF to a voltage close to zero (equal to the forward voltage of the body diode), resulting in negligible losses. After the dead time, *T1* is turned ON and its parasitic capacitance is discharged through the channel of *T1*. Note that at this instant the parasitic capacitance of *T2* is charged, and its "charging" current also flows through the channel of *T1*. In addition to that, *T1* also conducts the reverse recovery current of the body diode of *T2*, which is negligible in the WBG devices shown in Section II. As a result, at instant $t_1$, there is high turn-on energy loss in transistor *T1* and negligible turn-off energy loss in *T2*. Note that

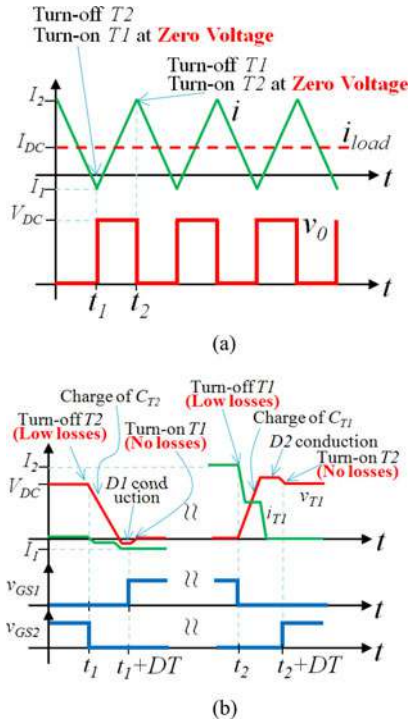



Fig. 6. (a) Load and inductor currents in a buck converter having high current ripple; (b) zoom on the commutation of transistor *T1*. When current ripple is high, the top transistor (*T1*) turns OFF at high current but turns ON at zero voltage while the bottom transistor (*T2*) turns OFF at low current and also turns on at zero voltage.

at instant $t_1$, turn-on losses in *T1* occur at a current

$$I_1 = I_{\rm DC} - \Delta I/2. \tag{2}$$

At instant $t_2$, the commutation cell voltage $v_{\rm o}$ goes from $V_{\rm DC}$ to zero. This happens because first transistor *T1* is turned OFF and after the dead time *DT*, transistor *T2* is turned ON. When *T1* is turned OFF (and before *T2* is turned ON), the inductor current discharges the parasitic capacitance of *T2* and charges the parasitic capacitance of *T1*. After that, the body diode of *T2* conducts the inductor current until the gate signal of *T2* goes high and the current starts flowing through the channel of *T2*. Thus, at instant $t_2$, there is turn-off energy loss in *T1,* but this energy is relatively low because the parasitic capacitances of *T1* and *T2* act as snubbers. At the same time, negligible turn-on energy is lost in *T2* since it turns ON after its body diode is conducting. This is usually called a zero-voltage switching (ZVS) commutation. The analysis shown above is illustrated by Fig. 5(b), where details on the voltage and current of transistor *T1* at instants $t_1$ and $t_2$ are given. Note that at instant $t_2$, turn-off losses in *T1* occur at a current

$$I_2 = I_{\rm DC} + \Delta I/2. \tag{3}$$

### *B. High-Current Ripple Mode*

Considering the mode where the current ripple is high [see Fig. 6(a)], at instant $t_2$, as it happens in the first mode, there is turn-off energy loss in *T1* and negligible turn-on energy loss in

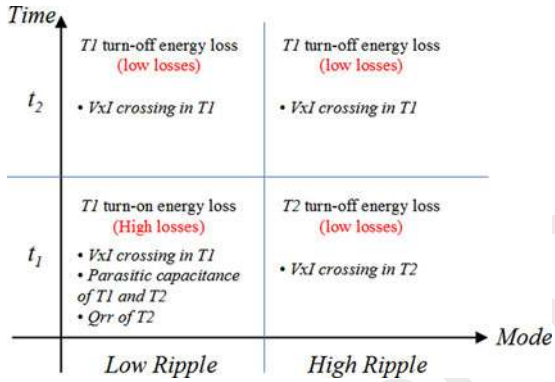



Fig. 7. Overview of switching losses in a buck converter operating in two different modes: low current ripple mode and high current ripple mode.

*T2*. However, at instant $t_1$, since the current changes the sign, something different occurs. At this instant, initially transistor *T2* is turned OFF and after the dead time *DT*, transistor *T1* is turned ON. When *T2* is turned OFF (and before *T1* is turned ON), the inductor current discharges the parasitic capacitance of *T1* and charges the parasitic capacitance of *T2*. After that, the body diode of *T1* conducts the inductor current until the gate signal of *T1* goes high and the current starts flowing through the channel of *T1*. Thus, at instant $t_1$, there is turn-off energy loss in *T2* and negligible turn-on energy loss in *T1* since it turns ON after its body diode is conducting (ZVS commutation). The analysis shown above is illustrated by Fig. 6(b) where details on the voltage and current of transistor *T1* at instants $t_1$ and $t_2$ are given.

In the first mode (low current ripple), during a switching period, there is turn-on energy loss in transistor *T1* (at instant $t_1$) and turn-off energy loss in the same transistor (at instant $t_2$). In the second mode (high current ripple), during a switching period, there is turn-off energy loss in transistor *T2* (at instant $t_1$) and turn-off energy loss in transistor *T1* (at instant $t_2$). This is schematically shown in Fig. 7. Thus, depending on the switching characteristics of the transistor used in the commutation cell, the sum of the turn-on and turn-off energies of the low-current ripple mode can be higher than the sum of the two turn-off energies of the high-current ripple mode. To illustrate that, an example is given for a buck converter using two CMF20120D SiC MOSFETs. The dc output current is equal to 4 A and three different current ripples are considered: 2, 6, and 14 A. These three inductor currents are shown in Fig. 8(a), where the different values of switched currents are marked with different markers. The switching energy corresponding to each switched current, for the CMF20120D SiC MOSFET, is shown in Fig. 8(b) (values experimentally obtained as shown in Fig. 2), for a switching voltage of 540 V. The sum of switching energies in one period, for the three cases is also shown in this figure. Note that the total switching energies per period ($E_{\rm total}$) for the current ripples of 2, 6, and 14 A are respectively 160, 150, and 52 $\mu$J. Hence, if $I_{\rm DC} = 4$ A, the switching losses are more than three times higher if the current ripple is equal to 2 A when compared to the case where the current ripple is equal to 14 A.

Increasing the current ripple leads to higher conduction losses in the transistors since the RMS current through them will

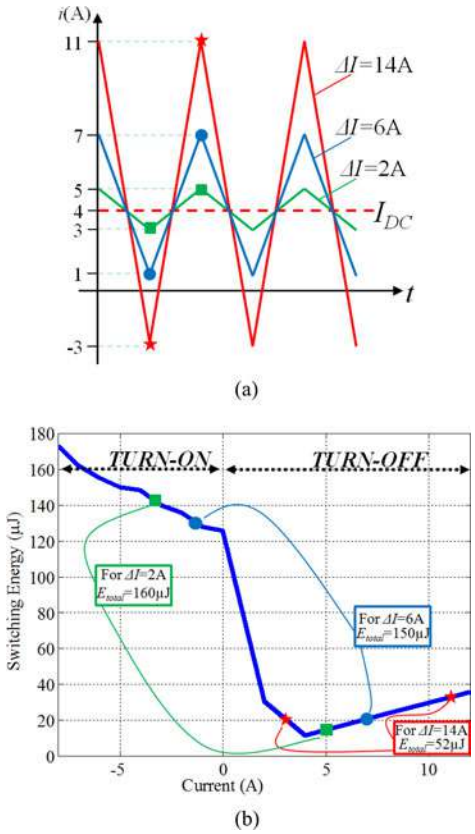



Fig. 8. (a) Inductor currents in a buck converter for different current ripples and (b) switching energy at 540 V for different switched currents, for the 1200 V SiC MOSFET CMF20120D. In (a) the switched currents are indicated with markers; these markers are used in (b) to show the corresponding switching energy. High current ripple results in lower total switching energy in a switching period ($E_{\mathrm{total}}$).

increase. The RMS value of the inductor current $I_{\mathrm{RMS}}$ for a given dc current $I_{\mathrm{DC}}$ and current ripple $\Delta I$ is

$$I_{\mathrm{RMS}} = \sqrt{I_{\mathrm{DC}}^2 + \Delta I^2/12}. \tag{4}$$

However, if the switching frequency is high, the increase in conduction losses in these transistors can be negligible when compared to the reduction of switching losses due to high current ripples. This can be seen in Fig. 9 for the specific case of a commutation cell containing two CMF20120D SiC MOSFET switching 540 V at a frequency of 50 kHz. Fig. 9(a) shows the total switching losses for different dc currents and different current ripple, while Fig. 9(b) shows the conduction losses of this SiC MOSFET (on-state resistance $R_{\mathrm{DSon}} = 80$ mW at 25 °C). Fig. 9(c) shows the total losses (switching + conduction) in the transistors. Note that the higher the dc current, the higher the optimal current ripple, which is the one minimizing the total losses. Optimal current ripple always corresponds to the case where there are two turn-off energies in a switching period (ZVS commutation), i.e., when the current ripple is higher than twice the dc current.

Also note that the higher the dc current, the smaller the difference between total losses at zero current ripple and at the optimal one. For example, if dc current is 2 A, total losses at

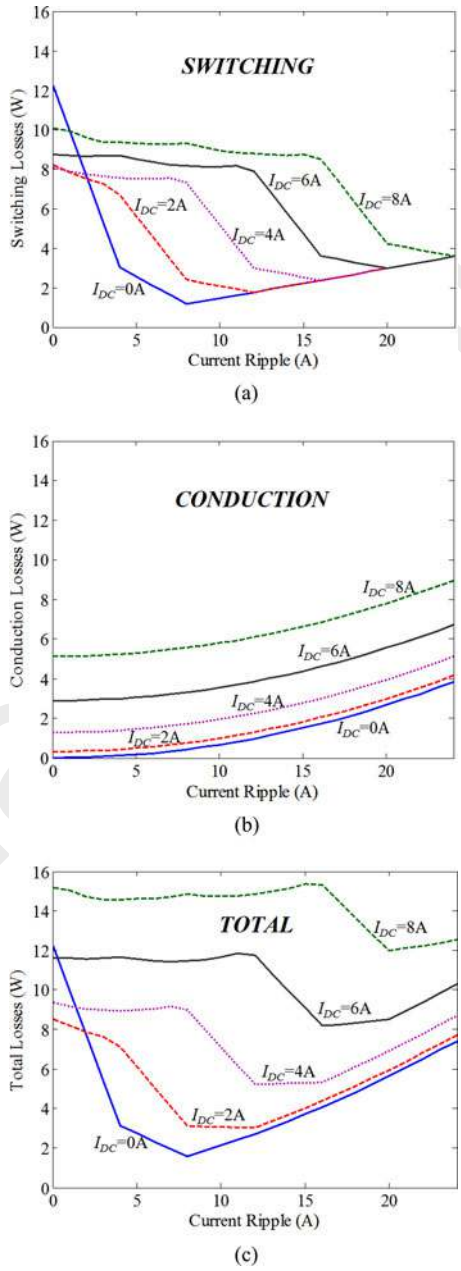



Fig. 9. (a) Switching losses, (b) conduction losses and (c) total losses (switching + conduction) in the bridge leg of a buck converter for different dc currents and different current ripples. Values were calculated using the SiC MOSFET CMF20120D switching 540 V at 50 kHz. High current ripples reduce total transistor losses although they increase the inductor RMS current.

zero current ripple are 8.4 W and at the optimal point, they are almost three times smaller (3 W). If dc current is 8 A, total losses at zero current ripple are 15.2 W and at the optimal point around 1.3 times smaller (12 W). Obviously, this difference can increase if the switching frequency is higher, as it is shown in Fig. 10, where the curves of total losses versus current ripple are plotted for two different dc currents (2 and 8 A), and for different switching frequencies. The concepts shown in this section will be experimentally verified in Section IV.

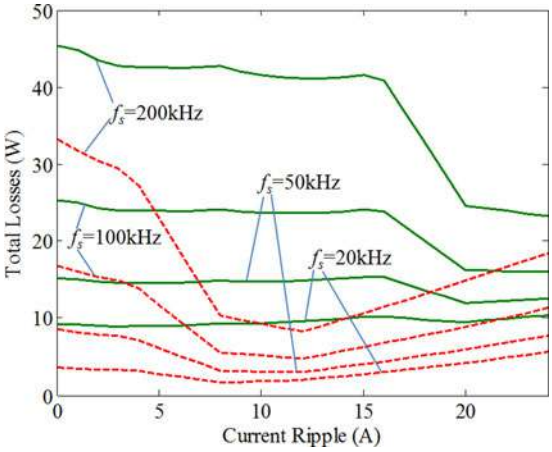



Fig. 10. Total losses (switching+conduction) in the bridge leg of a buck converter for different switching frequencies, for two different dc currents (dashed lines for 2 A and continuous lines for 8 A) and for different current ripples. Values were calculated using the SiC MOSFET CMF20120D switching 540 V. The higher the switching frequency, the higher the total loss reduction if optimal current ripple is chosen rather than no current ripple.

## IV. Experimental Setup and Results

### A. Loss Measurement Method

Measuring the total losses of a high-efficiency converter is a tricky task. One simple method is to measure the input and output power of the converter at a certain operation point and, then, subtract both measurements to find the converter losses. This is usually not accurate for high-efficiency converters. For example, if the converter losses are about 1% of the load power and if the voltage and current sensors have 0.1% of error, the error in the calculated converter losses can achieve 40%.

Using calorimetric measurement is usually more precise [28], however, it depends on a precise calibration of the calorimeter and the measurement for each operation point takes a long time (more than 3 h for each point as reported in [29]). Thus, this is not a practical method if the losses at many operation points need to be evaluated.

A more suitable method to measure losses of certain converter is called the "opposition method" [22]. This method is used to test the converter and its components at the nominal operation point, but only supplying the energy related to converter losses. This is mainly used in high-power converters when no load and no facilities are available for testing the converter at high-power levels [30], [31]. In [22], authors explain in detail the opposition method and show the advantages over regular calorimetric methods of the converter loss measurements. This method is used in [32] with the aim of testing the reliability of IGBTs operating at their rated power. In [33], this method is used to estimate losses of a dc–dc converter with a 12-phase monolithic Intercell Transformer and in [34] the same is done for an eight-phase 137-kW Intercell Transformer dedicated to multicell dc/dc stages in a modular UPS.

The opposition method consists of an association of two identical converters supplied by the same source, one operating as a generator, the other as a receptor. An inductive link connects

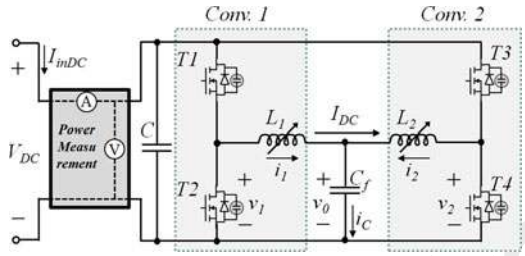



Fig. 11. Circuit of the opposition method applied to a buck converter.

both converters and the control of the current flowing from one converter to the other is made by small differences applied to the duty cycles of both converters. The opposition method applied to buck converter using SiC transistors, which is the converter of reference in this paper, can be represented by the circuit shown in Fig. 11. In this circuit, both buck converters (Conv. 1 and Conv. 2) are identical, having the same transistors and output filter inductor and capacitor. Since the capacitors of both converters are connected in parallel, they are represented by a single capacitor $C_f$ in Fig. 11. The dc voltage at the output capacitors ($V_0$) is equal to

$$V_0 = \frac{V_{1\mathrm{DC}} + V_{2\mathrm{DC}}}{2} = \frac{D_1 \cdot V_{\mathrm{DC}} + D_2 \cdot V_{\mathrm{DC}}}{2} \tag{5}$$

where $D_1$ and $D_2$ are, respectively, the duty cycles of Conv.1 and Conv. 2, and $V_{\mathrm{DC}}$ is the dc bus voltage. $V_{1\mathrm{DC}}$ and $V_{2\mathrm{DC}}$ are the dc values of voltages $v_1$ and $v_2$, respectively, in the output of each bridge leg.

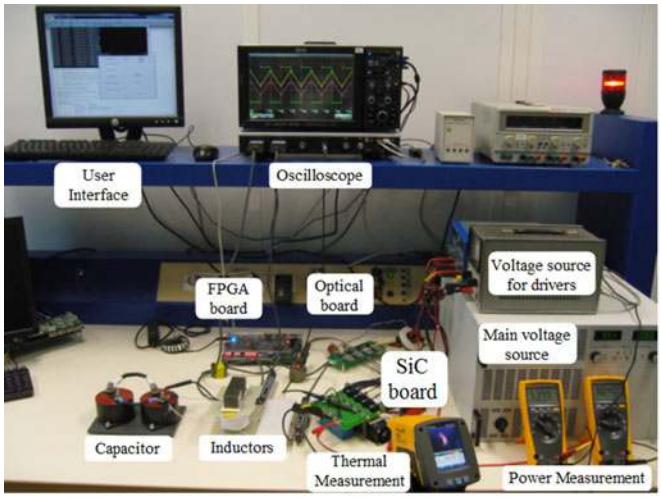
The dc current $I_{\mathrm{DC}}$ flowing from one converter to the other is given by

$$I_{\mathrm{DC}} = \frac{V_{1\mathrm{DC}} - V_{2\mathrm{DC}}}{R_L} = \frac{(D_1 - D_2) \cdot V_{\mathrm{DC}}}{R_L} \tag{6}$$

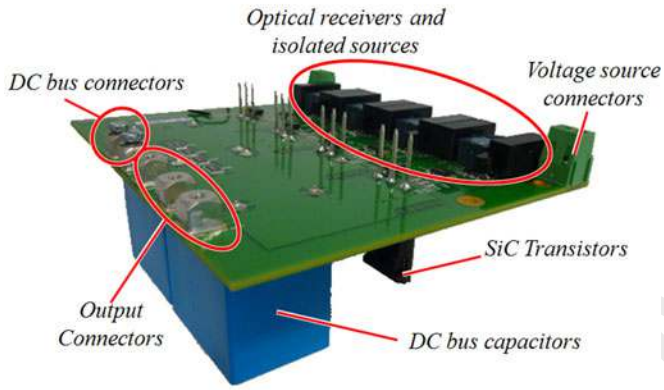
where $R_L$ is the sum of resistances of windings of inductors $L_1$ and $L_2$. This resistance is usually very small and thus small differences between the duty cycles of both sides are enough to impose the desired dc current in the inductor. Current ripple in both converters ($\Delta I_1$ and $\Delta I_2$) is calculated using (1).

### B. Experimental Setup

A four-layer PCB with 70-$\mu$m-thick copper was developed so four SiC transistors CMF20120D could be tested. These four transistors are arranged in two commutation cells and the drivers for each transistor use isolated sources, where the negative and positive voltage levels can be adjusted. The gate resistance of each transistor is equal to 10 $\Omega$. The developed board is shown in Fig. 12 as well as the entire experimental setup. The experimental setup is composed of a DE2-115 FPGA board, which is controlled by a personal computer. The switching signals from the FPGA board are sent to an interface board, which converts the electrical signals in optical signals transmitted by fiber optics to the SiC power board. Total losses of the entire converter are measured by simple dc voltmeter and ammeter. A FLUKE

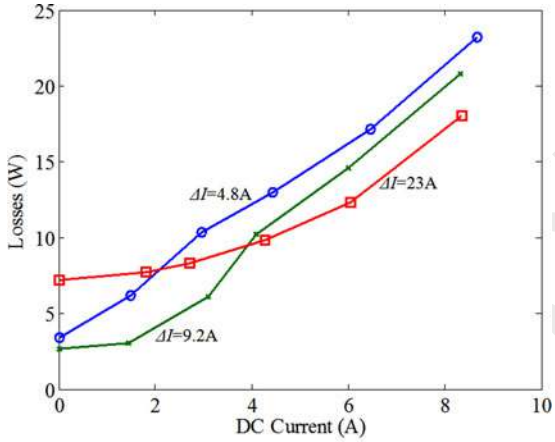



(a)

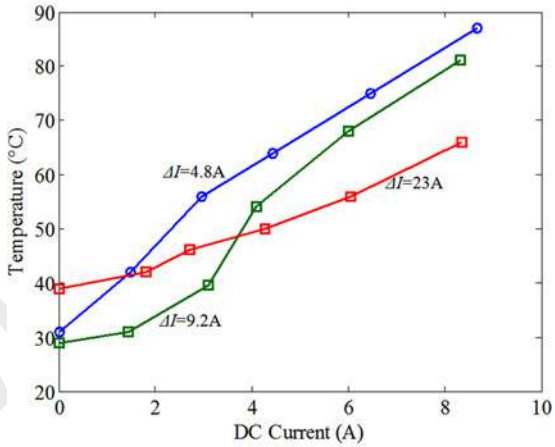



(b)

Fig. 12. (a) Experimental setup and (b) SiC board used in the opposition method to measure losses of a buck converter.




(a)




(b)

Fig. 13. (a) Total losses (switching+conduction) and (b) maximum transistor temperature in the bridge leg of a buck converter measured for a switching frequency of 50 kHz, for three different current ripples (4.8, 9.2 and 23 A) and for different dc currents. Experimental results show that high current ripples reduce transistor losses and temperature although they increase the inductor RMS current.

Ti20 Thermal Imager (accuracy of $\pm 2\%$) is used to measure the temperature of two SiC MOSFETs of the same bridge leg.

Both variable inductors of Fig. 11 are wound on the same core. A UI93/104/30 ferrite core, having material N87 from EPCOS, is used as well as two windings of 16 turns each. The airgap between the U and the I cores is variable in order to modify the inductance, and as a consequence the current ripple in the output of each bridge leg. The windings are made with litz wire having 20 thin wires (each of diameter 0.28 mm). The total cross section of the litz wire is 1.23 mm$^2$ and the dc resistance of each winding is 57 m$\Omega$ at 25 °C. At 50 kHz, each winding has a total equivalent resistance of 160 m$\Omega$. This value was calculated using FEM simulation for this frequency and for the first 51 harmonics, in order to precisely calculate losses for a triangular current, as shown in [35].

Concerning core losses, with $V_{\rm DC} = 540$ V and 16 turns in each winding, the peak flux density in the core is equal to 100 mT, for switching frequency of 50 kHz. This flux density induces losses of around 5.1 W (at 25 °C). Measurements of core losses were performed with this core beforehand.

Two 70 $\mu$F/900 V capacitors were connected in parallel to compose capacitor $C_f$ in Fig. 11. The total equivalent series resistance ($R_{\rm ESR}$) of the two capacitors in parallel is equal to 0.6 m$\Omega$ at 1 kHz and about 20% higher at 50 kHz. Thus, losses in these capacitors are negligible when compared to other losses of the system.

### C. SiC MOSFET Losses in Buck Converter

The experimental setup shown in Fig. 12 was used to measure losses under different conditions. The dc bus voltage is fixed to 540 V and tests were performed for a switching frequency of 50 kHz. The inductor airgap was adjusted so the current ripple was around 4.8, 9.2, and 23 A. The dc current was varied by slightly changing the duty cycles $D_1$ and $D_2$. The average duty cycle was 0.5 so the dc voltage in the output $V_0$ was maintained at 270 V.

Inductor and capacitor losses were calculated for each operation point and subtracted from the total losses in order to find only the losses in the transistors. These losses are shown in Fig. 13(a) for different dc currents and different current

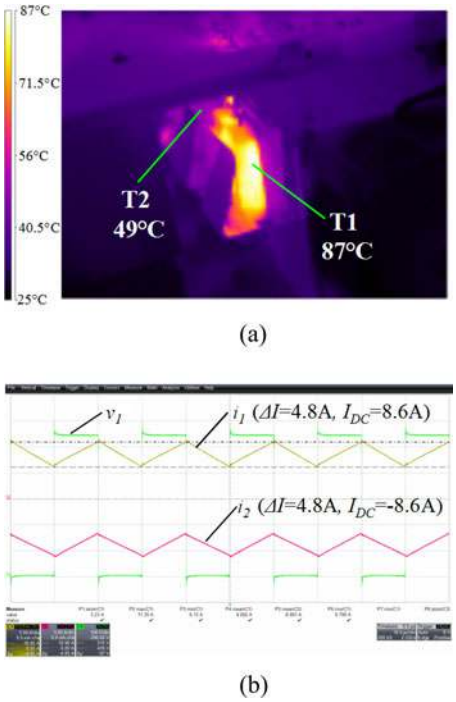



Fig. 14. (a) Thermal picture of two transistors of Conv. 1 of Fig. 11. (b) Experimental waveforms of voltage and current of Conv. 1 ($v_1$ and $i_1$) and current of Conv. 2 ($i_2$). Operation point has switching frequency equal to 50 kHz, dc current of 8.6 A and current ripple of 4.8 A. Low current ripple causes turn-on and turn-off losses in the top transistor (*T1*), and negligible switching losses in the bottom transistor (*T2*). Thus, *T1* attains much higher junction temperature than *T2*.

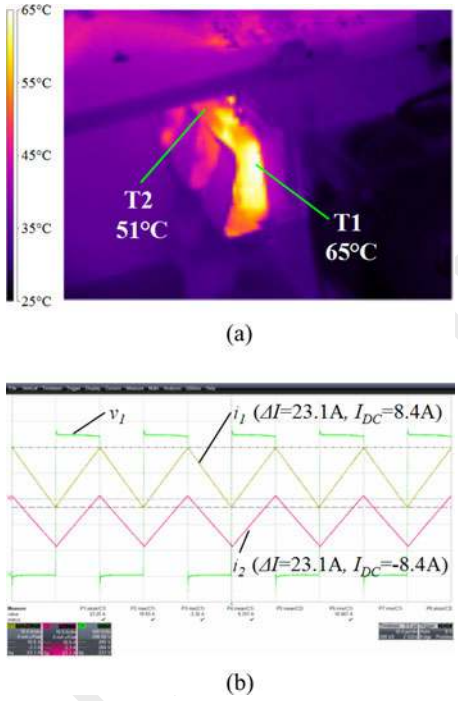



Fig. 15. (a) Thermal picture of two transistors of Conv. 1 of Fig. 11; (b) Experimental waveforms of voltage and current of Conv. 1 ($v_1$ and $i_1$) and current of Conv. 2 ($i_2$). Operation point has switching frequency equal to 50 kHz, DC current of 8.4 A and current ripple of 23.1 A. High current ripple causes turn-off losses in the top and bottom transistors, and negligible turn-on losses. Thus, *T1* attains much lower junction temperature than that in Fig. 14 where current ripple is low.

ripples. The higher the dc current, the higher the current ripple in order to allow transistor to only switch OFF current, with the consequent reduction of switching losses.

This reduction in transistor losses with increasing current ripple can be also confirmed by the temperature measured in both transistors of a bridge leg when the current ripple changes. Fig. 13(b) shows the case temperature of the hottest transistor (which is always transistor *T1* of Fig. 11) for the same dc currents and current ripples of Fig. 13(a). Note that higher current ripple decreases the transistor temperature when the dc current is high. The same thing can be seen in Figs. 14 and 15. Fig. 14(a) shows a thermal picture of both transistors of Conv. 1, for the experimental output current shown in Fig. 14(b). The dc current is equal to 8.6 A and the current ripple is 4.8 A. In this configuration, the top transistor (*T1*) switches OFF a current of about 11 A and switches ON 6.2 A. That is why, as shown in Fig. 14(a), *T1* has a temperature of 87 °C while *T2* (which has no switching losses) has a temperature of only 49 °C.

Fig. 15(a) shows a thermal picture of the same transistors, but now for the experimental output current shown in Fig. 15(b). The dc current is equal to 8.4 A and the current ripple is 23.1 A. Thus, the top transistor (*T1*) switches OFF a current of about 20 A and now the bottom transistor switches OFF a current of 3.1 A. With the increase in current ripple, *T1* does not switch ON current anymore, and that is why, as shown in Fig. 15(a), its temperature has dropped to 65 °C, while the temperature of *T2* only increased by 2 °C when compared to the first case. It is clear that, although higher current ripple increases the RMS current flowing through the transistors, it globally decreases total losses in the transistors and in particular it reduces the maximum temperature of hottest transistor in a buck converter.

## V. Optimal Buck Converter Design Considering High Current Ripple

In order to increase the current ripple in the output of a bridge leg of a buck converter, the output filter inductance must be reduced. However, the output filter capacitance must be increased with the purpose of maintaining the same filter cutoff frequency. Since the inductor is usually the most expensive, bulkiest and heaviest component of a filter, decreasing the inductance value is usually a good way to increase the power density of a converter. Nevertheless, higher current ripples increase copper losses in the inductor. For this reason, it is important to design the main components of a buck converter (transistors and associated heatsink, filter inductor, and capacitor) to verify that high current ripples not only decrease the losses in the transistors, but it also reduces total losses in the converter and increase the converter power density.

A 540-to-270-V buck converter, used in aircraft applications, will be designed for different allowed current ripples in the inductor and for different switching frequencies in order to find the optimal converter concerning efficiency and power density. Only the heatsink and the output *LC* filter will be designed. The input filter is not taken into account since it does not

TABLE I
PARAMETERS OF THE DESIGNED BUCK CONVERTER

| | |
|---|---|
| Output power, $P_{\mathrm{ref}}$ | 2 kW |
| DC bus voltage, $V_{\mathrm{DC}}$ | 540 V |
| Output voltage, $V_{\mathrm{load}}$ | 270 V |
| DC output current, $I_{\mathrm{load}}$ | 7.3 A |
| Output current ripple, $\Delta I$ | From 2 to 24 A |
| Switching frequency, $f_s$ | From 18 to 120 kHz |
| Ambient temperature, $T_{\mathrm{amb}}$ | 70 °C |

significantly change with the output current ripple and also because it is usually much smaller than the output filter for the voltage (540 V) and power (2 kW) levels considered in this paper. Specifications of the system are shown in Table I.

### A. Transistor Losses and Heatsink

The buck converter is composed of two SiC transistors CMF20120D attached to a natural convection heatsink. Conduction and switching losses are calculated the same way as losses calculated in Section III, i.e., switching losses depend on the switching frequency and total switching energy provided by the curve on Fig. 8(b) and conduction losses depend on the on-state resistance of transistors and the RMS current flowing through them, as shown in (4). Since transistors are assembled in a standard TO-247 package, a standard thermal resistance between the case and the heatsink $R_{\mathrm{thCH}}$ of 0.25 K/W is assumed. Having this value and total losses calculated in each transistor $P_{\mathrm{trx}}$ ($x = 1$ or 2, depending on the transistor), the junction temperature $T_{\mathrm{Jx}}$ in each transistor can be calculated as

$$T_{\mathrm{Jx}} = T_{\mathrm{amb}} + (P_{\mathrm{tr1}} + P_{\mathrm{tr2}}) \cdot R_{\mathrm{thHA}} + (P_{\mathrm{trx}}) \cdot (R_{\mathrm{thCH}} + R_{\mathrm{thJC}}) \quad (7)$$

where $R_{\mathrm{thJC}}$ is the thermal resistance between junction and case of the transistor and $R_{\mathrm{thHA}}$ is the thermal resistance of the heatsink. With this equation, two values of the heatsink thermal resistance can be calculated. One value for each transistor, since the two of them have different losses. The lowest calculated heatsink thermal resistance is the one which guarantees that none of transistors junction temperature will exceed the maximum temperature of 115 °C (which was chosen to be 10 °C below the maximum junction temperature allowed by the manufacturer).

Natural convection heatsink is chosen given that in a converter with forced air cooling system, the fan is usually one of the first devices to fail, and reliability is one of the main criteria in an aeronautic application. The best heatsink concerning the power dissipation per kg found in the market has flared aluminum pin fins. A side view of one of these heatsinks (50-mm-large model: 3–4220XXG) is shown in Fig. 16, as well as their weight and volume variation with thermal resistance, interpolated for different heatsink heights (dimension *H*) found in the manufacturer's datasheet [36]. These values were used to calculate the heatsink volume and weight for a given heatsink thermal resistance calculated with (7).

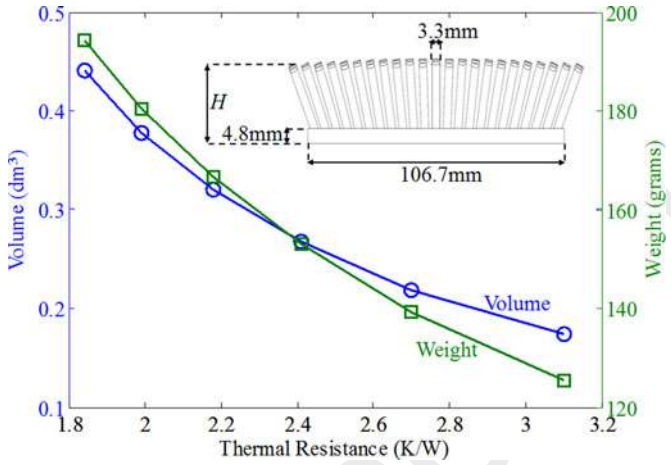



Fig. 16. Drawing of a flared pin fin heatsink used as reference for the converter design and variation of weight and volume of this heatsink with the thermal resistance. The heatsink thermal resistance is varied by changing the height "*H*".

### B. Inductance and Capacitance Calculation

The *LC* filter in the output of the buck converter has to limit the EMI injected into the load and the current ripple in the bridge legs. Measurement of voltage noise injected into the load is made using a line impedance stabilization network (LISN, defined in [37]), which is connected between the loads and the converter. The voltage measured at the LISN output, which is practically the high-frequency component of the filter capacitor voltage, is read by the EMI Test Receiver, which processes this noise according to [38]. The output of this circuit is compared to the limits defined by the standards.

The required inductance and capacitance such that the output of the EMI Receiver stays below the limits can be found by first calculating the required cutoff frequency of the *LC* filter. In a buck converter with duty cycle *D*, the *n*th harmonics ($V_{n,\mathrm{fs}}$) of the voltage in the output of the bridge leg ($v_0$ in Fig. 4) can be calculated as

$$V_{n,\mathrm{fs}} = \frac{2 \cdot V_{\mathrm{DC}}}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot D) \quad \text{for } n = 1, 2, 3, \ldots . \quad (8)$$

Assuming that the cutoff frequency $f_0$ of the filter is much lower than the switching frequency $f_s$, one can use the asymptotic response of the second-order filter to evaluate the harmonics after filtering

$$V_{n,\mathrm{fs}}^{\mathrm{filt}} = \left(\frac{f_0}{n \cdot f_{\mathrm{sw}}}\right)^2 \cdot \frac{2 \cdot V_{\mathrm{DC}}}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot D) \quad \text{for } n = 1, 2, 3, \ldots . \quad (9)$$

From this formula, it can be seen that the envelope of the harmonics of the output voltage is a straight line decreasing with a slope of –60 dB/decade when a second-order filter is used. The cutoff frequency of the output filter must be chosen so this envelope is below the limits provided by the standards [39].

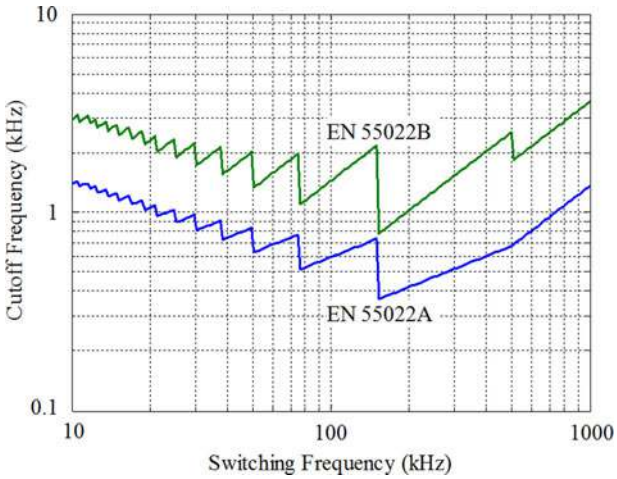



Fig. 17. Variation of the cutoff frequency of an *LC* filter in the output of a buck converter with the switching frequency of this converter. The cutoff frequency is calculated so the harmonics in the output voltage are below the limits imposed by standards EN 55022A and EN 55022B used in converters for aircrafts.

Considering a dc bus voltage ($V_{\rm DC}$) of 540 V and the standards EN 55022A and EN 55022B, the variation of the cutoff frequency with the switching frequency of the buck converter can be seen in Fig. 17. Note that the filter's cutoff frequency tends to decrease if the switching frequency increases, up to 150 kHz which is the starting frequency considered in the standards. It means that increasing the switching frequency results in larger output filters. The saw-tooth shape of the curves in Fig. 17 is due to the fact that the fundamental frequency of the switched voltage or its harmonics crosses the starting frequency considered in the standards, as explained in detail in [39].

Standard EN 55022B is chosen to design the 540-to-270-V buck converter in this paper. So for a given switching frequency, one can find the cutoff frequency of the required *LC* filter and the required capacitance can be calculated

$$C = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot L}. \tag{10}$$

Note that the inductance value *L* depends on the desired output current ripple and can be calculated using (1).

### C. Capacitor Volume, Weight, and Losses

As typically used in EMI filter design, MKP film capacitors from EPCOS with a dc rated voltage of 300 V were selected. The capacitor's volume, weight, and losses can be calculated using interpolation of values extracted from the manufacturer's datasheet. These values are shown in Fig. 18, where Fig. 18(b) shows the variation of the equivalent series resistance (*ESR*) value of the capacitors. These values are used to calculate capacitor losses $P_{\rm cap}$ as

$$P_{\rm cap} = \frac{ESR \cdot \Delta I^2}{12} \tag{11}$$

where $\Delta I$ is the peak-to-peak value of the triangular current ripple flowing through the capacitor. This current ripple is considered the same as the one in the inductor since very low current ripple is allowed in the load.

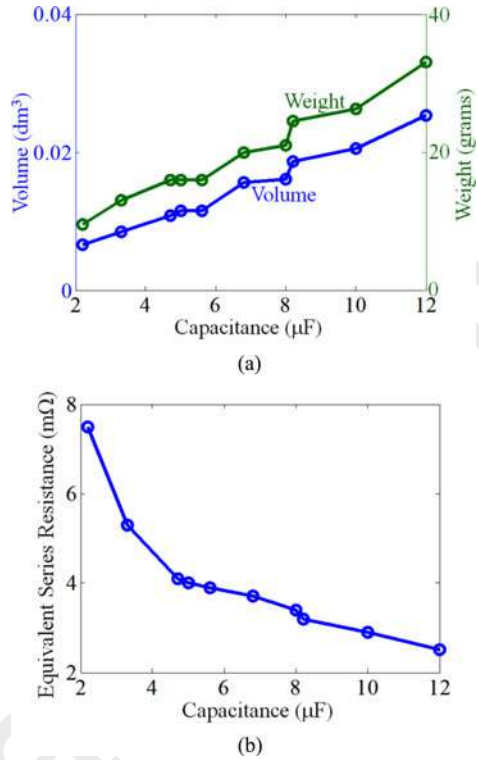



Fig. 18. (a) Volume, weight, and (b) ESR values of MKP film capacitors from EPCOS, dc-rated voltage of 300 V. Values were extracted from manufacturer's datasheet and are used to calculate the volume, weight, and losses of the output filter capacitor.

### D. Inductor Optimization

Inductors were optimized for minimum volume according to the procedure shown in the flowchart of Fig. 19. Since the main objective of the design is to reduce the boxed volume of the inductor, the structure of Fig. 20(a) was considered. Windings are composed of copper foil conductors which provide high utilization of the core window and low copper losses at higher frequencies. There are two windings (one around each core leg) connected in series, each having half the total number of turns. The inductor is composed of four cores of shape "I" and the core material is chosen to be ferrite 3F3 from manufacturer FERROXCUBE, given its low specific losses at high frequencies.

Geometric parameters which have their values changed during optimization are: conductor thickness ($e_c$) and width ($h_c$), core leg width ($e_{\rm li}$) and depth ($d_i$), and the number of turns (*N*). Other fixed parameters of the inductor are: distance between conductor and core leg ($e_{\rm wc}$), distance between two half windings ($e_{\rm ww}$), and insulation thickness around conductors ($e_{\rm ins}$). Some other dimensions are calculated from the fixed and variable parameters: core width ($e_i$), core height ($h_i$), and air gap length ($h_g$). Parameters are shown in Fig. 20(b).

Optimization constraints were defined as follows: maximum temperature rise ($T_{\rm lim}$) equal to 40 °C and maximum flux density

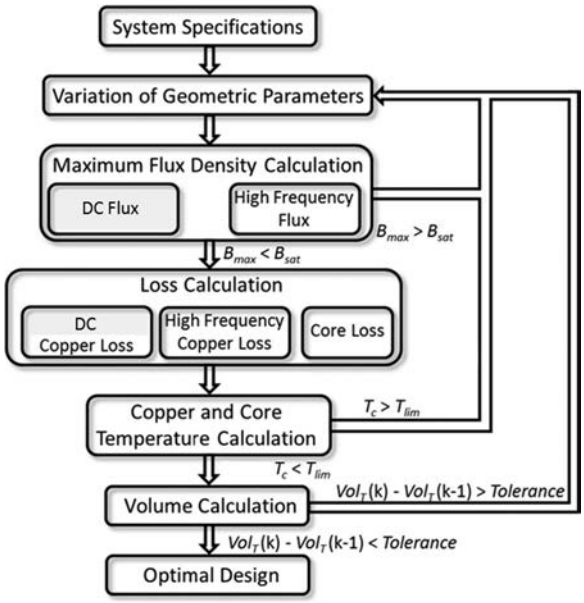



Fig. 19. Flowchart of the inductor design.

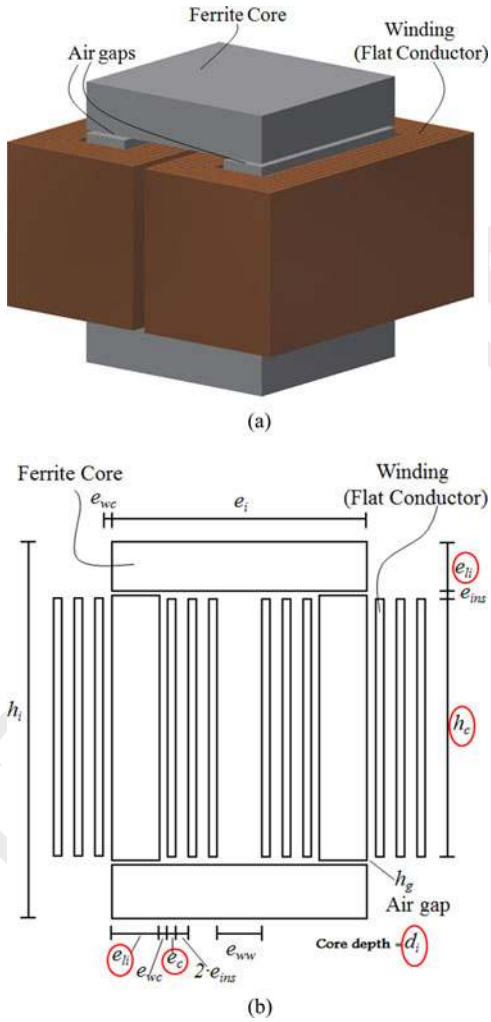



Fig. 20. (a) Structure of the inductor used in the optimization procedure and (b) geometrical parameters. Variable dimensions used in the optimization are marked with a circle.

($B_{\max}$) in the core equal to 0.3 T. The calculations performed in the optimization algorithm are briefly described below.

*1) Core Losses and Maximum Flux Density:* In an inductor, the flux density *B* inside the core is proportional to the current *i* flowing in the windings

$$B(t) = \frac{L \cdot i(t)}{A_c \cdot N} \tag{12}$$

where $A_c$ is the core cross section, *N* is the number of turns, and *L* is the inductance. With this equation, one can calculate the maximum flux density and the high-frequency flux together with (1) to estimate the core losses. An approximate calculation of the core losses in ferrite cores for nonsinusoidal flux can be based on the iGSE equation [40], which determines the core loss density $P_{\text{dens}}$

$$P_{\text{dens}} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{13}$$

where $k_i$ can be calculated as

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\zeta|^{\alpha} 2^{\beta-\alpha} d\zeta}. \tag{14}$$

In (13) and (14), coefficients $k$, $\alpha$, and $\beta$ are called the Steinmetz coefficients and they are specific for each magnetic material. They vary mainly with the frequency and temperature. These coefficients for the 3F3 ferrite material, at 100 °C and for high-frequency range, are $\alpha = 1.6$, $\beta = 2.5$, and $k = 2.5 \times 10^{-4}$. Calculated loss density is given in kW/m$^3$.

*2) Copper Losses:* Given the size of the magnetic devices, dc copper losses can be calculated using the dc resistance of the windings. However, the current ripple generates high-frequency copper losses which can only be approximated by analytical calculations. This paper has used formulas developed by Dowell [41] to calculate the ac resistance $R_{\text{AC}m}$ at a given frequency. FEM simulation is performed after optimization in order to precisely recalculate high-frequency copper losses of optimal inductor.

Since current ripple is triangular, it contains several harmonics. Each harmonic frequency has a corresponding ac resistance. Therefore, the ac resistance has to be calculated not only for the switching frequency, but also for all the important harmonics. Total copper losses can be calculated according to the following equation:

$$P_c = R_{\text{DC}} \cdot I_{\text{DC}}^2 + \sum_{m=1}^{\infty} R_{\text{AC}m} \cdot I_{m,\text{rms}}^2 \tag{15}$$

where $I_{\text{DC}}$ is the dc value of the inductor current and $I_{m,\text{rms}}$ is the rms value of the *m*th harmonic of the high-frequency current flowing through the windings.

*3) Thermal Calculation:* After calculating copper and core losses, the inductor temperature must be estimated. Since the components show a low volume (and thus have a high surface to volume ratio), no active cooling is necessary to achieve high

values of power density. A simple model considering a unique temperature for the whole magnetic component is used. The total heat exchange area ($S_{\text{exc}}$) of the magnetic component is calculated considering all copper and core surfaces which are in direct contact with air. This is used to calculate the overall temperature rise ($T_c$) of the magnetic component according to

$$T_c = \frac{P_t}{S_{\text{exc}} \cdot H_{\text{exc}}} \tag{16}$$

where $P_t$ is the total losses dissipated by the magnetic component and $H_{\text{exc}}$ is a thermal exchange coefficient which takes into account natural convection and radiation effects at high temperatures. This coefficient is usually between 5 and 15 $\text{W/m}^2 \cdot \text{K}$ [42] and here it is considered equal to 12 $\text{W/m}^2 \cdot \text{K}$ given the high core temperature.

### *E. Results*

A MATLAB algorithm was developed to calculate weight, volume, and losses of transistors with associated heatsink, filter inductor, and capacitor. This algorithm was run for different current ripples in the output inductor and for different fixed switching frequencies. Fig. 21 shows the losses, volume, and weight of different parts of the converter for different current ripples, at a fixed switching frequency of 50 kHz. Fig. 21(a) shows that since the filter has a high capacitance value, capacitor losses are negligible when compared to the other losses of the system. Also, there is an optimal current ripple which minimizes the inductor losses and another current ripple which minimizes the transistor losses. The current ripple value which reduces the total losses in the buck converter is around 20 A. This value allows ZVS operation of the converter since transistor *T1* would switch OFF a current of $7.3 + 10 = 17.3$ A and transistor *T2* would switch OFF a current of $10 - 7.3 = 2.7$ A, which is close to the minimum switching energy of the SiC MOSFET, as shown in Fig. 2.

Figs. 21(b) and 21(c) show that the higher the current ripple, the higher the volume and weight of the filter capacitor. The inductor and heatsink size and volume decrease with the augmentation of the current ripple, up to a certain point close to 20 A. For the specific switching frequency of 50 kHz, the heatsink is bulkier than the inductor although the inductor is heavier than the heatsink given its high mass density (inductor is composed of compact copper and ferrite material while heatsink is made of aluminum with a large amount of air between the fins in order to maximize the thermal exchange in natural convection). Nevertheless, the optimal current ripple which minimizes the converter weight and volume is close to 20 A, where the system is close to the ZVS operation. The volume and weight difference between high and low current ripple is more evident for higher switching frequencies. Also, this difference would be more evident if different filter criteria were considered. For example, for a buck used in a different application, EMI standards would not be the main filter criteria and most likely the cutoff frequency of the filter would be higher than those used to generate Fig. 21. Thus, the required filter capacitance would be significantly lower and, thus, the total converter weight and volume would be considerably lower for higher current ripples.

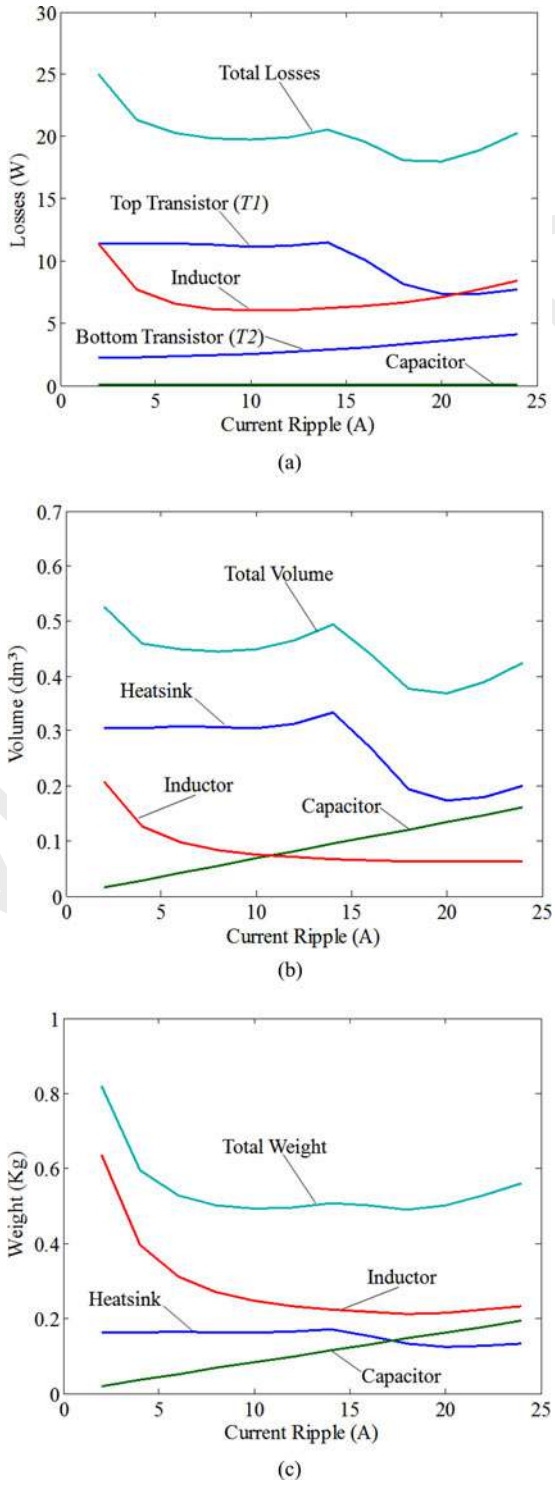



Fig. 21. (a) Losses, (b) volume, and (c) weight of different parts of the 540-to-270-V buck converter, for a fixed switching frequency of 50 kHz. High current ripples reduce total converter losses, volume, and weight although they increase the RMS current in all components.

The converter losses were used to calculate the converter efficiency and the converter volume is used to calculate the converter power density. This is made for different current ripples

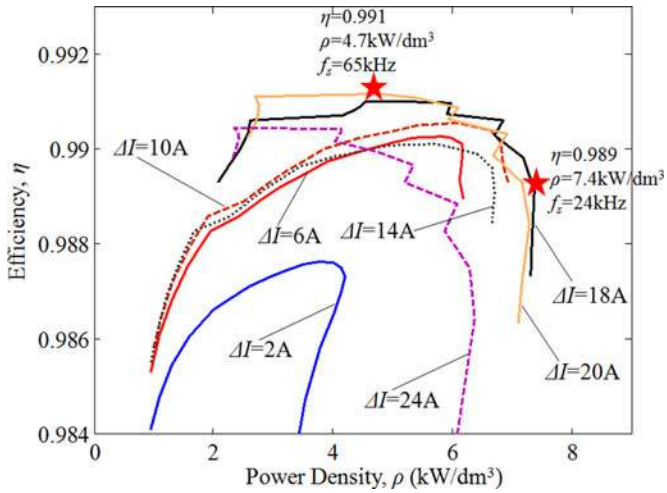



Fig. 22. Efficiency versus power density of the buck converter, for a frequency variation from 18 to 120 kHz and for different current ripples. The maximum power density is achieved for a current ripple of 18 A and frequency of 24 kHz while the maximum efficiency is achieved for a current ripple of 20 A and frequency of 65 kHz.

and for different switching frequencies. Thus, a Pareto front of the variation of converter's efficiency with its power density is shown in Fig. 22. Each curve corresponds to a different current ripple. Each point of a curve corresponds to a different switching frequency and the direction of the switching frequency increase within the curve is from the right to the left. The minimum and maximum switching frequencies are, respectively, 18 and 120 kHz.

Analyzing these curves, note that low current ripple result in poor efficiencies and power densities. The curve with the highest efficiencies and power densities corresponds to current ripples of 18 and 20 A. The highest power density (7.4 kW/dm$^3$) is achieved for a current ripple of 18 A and switching frequency of 24 kHz while the highest efficiency (99.1%) occurs at 65 kHz for a current ripple of 20 A. Both values are marked with a star in Fig. 22 and are achieved when the transistors operate in ZVS conditions.

## VI. Conclusion

New wide bandgap devices present much better performance than their equivalent silicon-based counterpart. However, in order to use these devices in the best way possible, their switching energies at different current and voltages must be precisely known. Classical switching loss measurement methods can be inaccurate when applied to WBG devices or simply unfeasible given the device dimensions. For that reason a specific method was developed in order to measure turn-on and turn-off energies of transistors without the use of current and voltage sensors on the transistor. Therefore, this method does not change the switching behavior of transistor and accurately measured switching energies.

The developed method was used to measure switching losses of SiC MOSFETs and a GaN FET. Results show that, in both transistors, turn-on energy is much higher than turn-off energy for a given switched current and voltage. This difference increases with the switched voltage given that turn-on energy is closely related to the parasitic capacitance charge. For the SiC MOSFET CMF20120D from manufacturer CREE at junction temperature of 25 °C, the turn-on energy at 540 V and 8 A is 7.5 times higher than the turn-off energy at the same voltage and current values.

Given these switching characteristics of WBG transistors, we showed that, in a buck converter, increasing the current ripple in the filter inductor to values higher than 200% of the dc current significantly decreases the transistor switching losses. In the specific case of SiC MOSFET CMF20120D, this value is between 250% and 280%. This is due to fact that with such a high current ripple, transistors of the commutation cell only turn-off current. Although high current ripple increases the RMS current flowing through the transistors, it globally decreases total transistors losses, especially if they switch at high frequencies.

Experimental results using SiC MOSFET CMF20120D in two buck converters connected in "opposition mode" showed a reduction of transistor losses with increasing current ripple in the output inductor. For a dc output current of 8.6 A and a dc bus voltage of 540 V, a buck converter switching at 50 kHz has the transistor losses reduced by 24% if the current ripple goes from 4.8 to 23 A. The temperature rise of the hottest transistor is reduced by 33%, showing that high current ripples have also the advantage of balancing the losses in both transistors of a commutation cell. This is explained by the fact that with low current ripple, one transistor of the commutation cell switches the current ON and OFF, while with current ripple higher than 200% of the dc current, both transistors of the commutation cell switch OFF current (although one transistor switches OFF a much higher current than the other).

The design of a 2-kW 540-to-270-V buck converter for aircraft applications was performed for different switching frequencies and current ripples. The characteristics of the SiC transistor tested in this paper were used to calculated transistor losses and the required natural convection heatsink volume and weight to limit the junction temperature of the transistors. The output differential-mode filter capacitor was designed using commercially available film capacitors and precise optimization taking into account high frequency effects and thermal aspects was developed to design the filter inductor.

Calculation for a fixed frequency of 50 kHz showed that the current ripple of around 20 A minimizes total losses, weight, and volume of the converter. This ripple value is much higher than the dc output current, which is equal to 7.3 A. The calculation of converter's efficiency and power density was performed for switching frequencies from 18 to 120 kHz and these values were plotted in a Pareto front for different current ripples. These curves show that current ripples from 18 to 20 A maximize the efficiency versus power density characteristic of the buck converter. The maximum power density is equal to 7.4 kW/dm$^3$ and is achieved at a switching frequency of 24 kHz, while the maximum efficiency is equal to 99.1% and is achieved at a switching frequency of 65 kHz.

High current ripples in buck converters using WBG devices reduce the converter's losses, volume, and weight. Although

not analyzed in this paper, high current ripples can also reduce the common-mode filter since they force the transistors only to switch OFF current. Turn-off commutation in these WBG devices constitutes soft switching, resulting in a much lower *dv*/*dt* than during a turn-on commutation.

The analysis presented here can be applied to converters with any power switch. However, high current ripple is only interesting if the switch characteristic shows much higher turn-on energy than turn-off energy, which is the case for fast transistors having high breakdown voltage. The higher the difference between turn-on and turn-off energies of a transistor (mainly due to parasitic capacitance of fast transistors), the more suitable the use of high current ripple in the converter.

## REFERENCES


[1] D. Reusch, D. Gilham, Y. Su, and F. C. Lee, "Gallium Nitride based 3D integrated non-isolated point of load module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 38–45.

[2] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si-evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[3] R. Wang, D. Boroyevich, P. Ning, Z. Wang, F. Wang, P. Mattavelli, K. Ngo, and K. Rajashekara, "A high-temperature SiC three-phase ac-dc converter design for $>100\,^{\circ}$C ambient temperature," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 555–572, Jan. 2013.

[4] J. Millan, "A review of WBG power semiconductor devices," in *Proc. Int. Semicond. Conf.*, vol. 1, Oct. 2012, pp. 57–66.

[5] C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli, "Characterization and comparison of 1.2 kV SiC power semiconductor devices," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[6] R. A. Wood and T. E. Salem, "Evaluation of a 1200-V, 800-A All-SiC Dual Module," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2504–2511, Sep. 2011.

[7] P. Ladoux, M. Mermet, J. Casarin, and J. Fabre, "Outlook for SiC devices in traction converters," in *Proc. Elect. Syst. Aircraft, Railway Ship Propulsion*, Oct. 2012, pp. 1–6.

[8] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SIC JFETs," presented at the IEEE Appl. Power Electron. Conf. Expo., Austin, TX, USA, Feb. 2008.

[9] D. Aggeler, F. Canales, J. Biela, and J. W. Kolar, "Dv/Dt control methods for the SiC JFET/Si MOSFET cascode," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4074–4082, Aug. 2013.

[10] S. Madhusoodhanan, K. Hatua, S. Bhattacharya, S. Leslie, Sei-Hyung Ryu, M. Das, A. Agarwal, and D. Grider, "Comparison study of 12kV n-type SiC IGBT with 10kV SiC MOSFET and 6.5kV Si IGBT based on 3L-NPC VSC applications," *IEEE Energy Convers. Congr. Expo.*, pp. 310–317, Sep. 2012.

[11] A. Lidow, J. Strydom, M. De Rooij, and Y. Ma, "GaN transistors for efficient power conversion," presented at the IEEE Power Convers. Publications, New York, NY, USA: Wiley, 2012.

[12] B. Cougo, J. Brandelero, H. Schneider, and T. Meynard, "Accurate switching energy estimation of parallel eGaN FETs for modern aircraft applications," in *Proc. IEEE* Wide Bandgap Power Devices Appl., 2013, pp. 108–111.

[13] N. Videau, J. Brandelero, T. Meynard, V. Bley, D. Flumian, G. Fontes, and E. Sarraute, "High switching frequency 5-phase interleaved buck converter with gallium nitride transistors," in *Proc. IEEE Wide Bandgap Power Devices Appl.*, 2013.

[14] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[15] L. Corradini, D. Seltzer, D. Bloomquist, R. Zane, D. Maksimovic, and B. Jacobson, "Zero voltage switching technique for bidirectional DC/DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1585–1594, Apr. 2014.

[16] Sung-Sae Lee, "Step-down converter with efficient ZVS operation with load variation," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 591–597, Jan. 2014.

[17] T. Mishima, C. Takami, and M. Nakaoka, "A new current phasor-controlled ZVS twin half-bridge high-frequency resonant inverter for induction heating," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2531–2545, May 2014.

[18] H. Qin and J. W. Kimball, "Solid-state transformer architecture using AC–AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.

[19] B.-R. Lin and C.-H. Chao, "A new ZVS DC/DC converter with three APWM circuits," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4351–4358, Oct. 2013.

[20] L. Jiang, C. C. Mi, S. Li, C. Yin, and J. Li, "An improved soft-switching buck converter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4885–4891, Nov. 2013.

[21] B. Cougo, H. Schneider, and T. Meynard, "Accurate switching energy estimation of wide bandgap devices used in converters for aircraft applications," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[22] F. Forest, J.-J. Huselstein, S. Faucher, M. Elghazouani, P. Ladoux, T. A. Meynard, F. Richardeau, and C. Turpin, "Use of opposition method in the test of high-power electronic converters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 530–541, Apr. 2006.

[23] H. Li-Gao and W. Jian, "Selection of the current ripple ratio of converters and optimal design of output inductor," in *Proc. IEEE Conf. Ind. Electron. Appl.*, Jun. 2010, pp. 1163–1167.

[24] J. Rabkowski, G. Tolstoy, D. Peftitsis, and H. Nee, "Low-loss high-performance base-drive unit for SiC BJTs," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2633–2643, May 2012.

[25] C. Zheng, Y. Yiying, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[26] J. Brandelero, B. Cougo, T. Meynard, and N. Videau, "A non-intrusive method for measuring switching losses of GaN power transistors," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, Nov. 2013, pp. 246–251.

[27] F. Krismer and J. W. Kolar, "Efficiency-optimized high current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[28] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Mühlethaler, T. Nussbaumer, and J. Miniböck, "Extreme efficiency power electronics," presented at the Int. Conf. Integr. Power Electron. Syst., Nuremberg, Germany, Mar. 2012.

[29] D. Christen, U. Badstübner, J. Biela, and J. W. Kolar, "Calorimetric power loss measurement for highly efficient converters," presented at the IEEE/IEEJ Int. Power Electron. Conf., Sapporo, Japan, Jun. 2010.

[30] P. Ladoux, J. M. Blaquiere, S. Alvarez, E. Carroll, and P. Streit, "Test bench for the characterisation of experimental low voltage IGCTs," in *Proc. IEEE Power Electron. Spec. Conf.*, vol. 4, 2004, pp. 2937–2942.

[31] J. Von Bloh and R. W. De Doncker, "Characterizing medium-voltage high-power devices under conventional and soft-switching conditions," in *Proc. IEEE Ind. Appl. Conf.*, 1999, pp. 373–378.

[32] J. Vallon, "Introduction à l'étude de la fiabilité des cellules de commutation à IGBT sous fortes contraintes," Ph.D. thesis, Institut National Polytechnique de Toulouse, Toulouse, France, 2003.

[33] B. Cougo, V. Costan, T. Meynard, F. Forest, and E. Laboure, "A new intercell transformer for interleaved converters," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2009, pp. 1–10.

[34] F. Forest, T. A. Meynard, J.-J. Huselstein, D. Flumian, C. Rizet, and A. Lacarnoy, "Design and characterization of an eight-phase-137-kW intercell transformer dedicated to multicell DC–DC stages in a modular UPS," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 45–55, Jan. 2014.

[35] T. Meynard, B. Cougo, F. Forest, and E. Laboure, "Parallel multicell converters for high current: Design of intercell transformers," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2010, pp. 1359–1364.

[36] Cooling Innovations, Heatsink model: 3-4220XXG. [Online]. Available: http://www.coolinnovations.com/

[37] Information technology equipment—radio disturbance characteristics—limits and methods of measurement—publication 22, CISPR, Geneva, Switzerland, 1997.

[38] J. Wang, W. G. Dunford, and K. Mauch, "Analysis of a ripple-free input current boost converter with discontinuous conduction characteristics," *IEEE Trans. Power Electron.*, vol. 12, n. 4, pp. 684–694, Jul. 1997.

[39] T. Meynard, B. Cougo, and J. Brandelero, "Design of differential mode filters for two-level and multicell converters", in *Proc. IEEE Int. Workshop Electron. Control Meas. Signals*, Toulouse, France, 2013, pp. 1–6.

[40] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.

[41] P. L. Dowell, "Effect of eddy currents in transformer windings," in *Proc. IEE*, vol. 113, no. 8, pp. 1387–1394, 1966.
[42] J. Biela and J. W. Kolar, "Cooling concepts for high power density magnetic devices," presented at the IEEJ/IEEE Power Conversion Conference (PCC), Nagoya, Japan, 2007.