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► **To cite this version:**

Alexandre Boyer, E. Sicard. A Case Study to apprehend RF Susceptibility of Operational Amplifiers. 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo 2019), Oct 2019, Haining, China. hal-02319469

HAL Id: hal-02319469

<https://laas.hal.science/hal-02319469>

Submitted on 18 Oct 2019

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A Case Study to apprehend RF Susceptibility of Operational Amplifiers

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Abstract— This paper describes the content of a practical training dedicated to the susceptibility of operational amplifiers to electromagnetic disturbances. The typical failure mechanisms of this type of device are characterized and compared on two commercial components. An analog behavioral model is then derived to predict the susceptibility of this device in various configurations.

Keywords—susceptibility, education, operational amplifier, IC EMC measurement, modeling

I. INTRODUCTION

Immunity to RF disturbances is an important requirement for electronic equipments to ensure a safe and reliable operation. It is strongly related to the susceptibility of the embedded integrated circuits (IC), whose operation can be disrupted by incoming electromagnetic (EM) disturbances. Among all the IC types, operational amplifier (op-amp) is often responsible of susceptibility. This circuit is not only usual in signal conditioning stage, but also within bandgap reference and linear voltage regulators. The nature of the failures induced by coupled EM disturbance has already been presented in numerous scientific papers and books, such as [1] [2]. Out-of-band EM disturbances coupled on differential-pair input terminals or power supply references may induce an offset which cannot be filtered anymore. Several papers address the modeling of the EMI-induced issue linked to the weak distortion of the incoming disturbance [3] [4] [5]. Many others propose design changes to improve its immunity [6] [7] [8].

In spite of the importance of this problem, it remains quite unknown or misunderstood by many electronic designers (not only IC designer, but also end-users). The origin of the problem is complex and understanding it requires good skills in analog design. However, learning EMC failure mechanisms and how evaluate them and how to correct them are very important to ensure EMI-proof electronic design. This paper aims at improving the understanding of EMC issues related to op-amp-based analog designs. For this purpose, a dedicated measurement and simulation lab has been developed, as part of a training dedicated to EMC of ICs [9]. It is based on a low-cost case-study and on modeling based on the freeware IC-EMC [10]. It aims at illustrating EMI-induced offset issue in analog ICs, measuring susceptibility of ICs, characterizing and observing the main EMI-induced failure mechanisms in op-

amp and building simple susceptibility model of op-amp.

The paper describes briefly the organization of this training, but focuses mainly on the observation of failures triggered on the tested devices and the description of a simple behavioral modeling approach based only on basic information and simple measurements. The paper is organized as follows: after a presentation of the case study, the measurement results are described and analyzed in the third part. Two major failure mechanisms are observed and characterized. From this analysis, an analog behavioral model is derived in the fourth part and its results are compared to measurements.

II. PRESENTATION OF THE CASE STUDY

The case study in this lab is representative of EM disturbance coupling on the input or output of conditioning signal stage placed after sensors, where amplification is required. The typical scenario is described in Fig. 1. Radiated EM disturbances may couple on cable harness, which can exist between the sensor and the amplification stage, or between the sensor and analog -to-digital conversion stage. This coupling of the EM disturbance induce RF voltage which may be conducted on op-amp differential inputs.

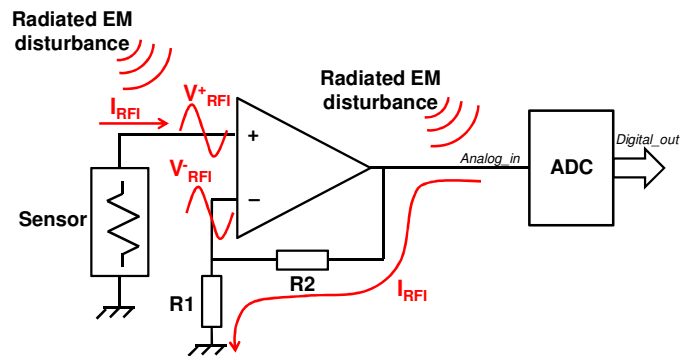


Fig. 1. Typical scenario of coupling EM disturbance on conditioning signal stage

In order to test the susceptibility of off-the-shelf op-amp, a low-cost evaluation board has been identified: the TI's universal op amp evaluation board 551012875 [11]. It aims at testing TI op-amp mounted in standard 6-lead SOT23 and SC70 packages. TI develops also EMI-hardened op-amps.

With TI's board 551012875, two op-amps can be mounted in parallel on the same board, with the same configuration and same power supply. It is an ideal situation to compare the susceptibility of two op-amp with similar characteristics, except their robustness to EM disturbances. Two op-amp references have been chosen with similar characteristics, summarized in Table I (EMI hardened and non-hardened op-amp do not have exactly the same characteristics). Most of them are familiar characteristics, except for EMIRR for Electromagnetic Interference Rejection Ratio which is the ratio between the peak-to-peak amplitude of the disturbance applied on the tested op-amp pin and the offset induced on its output, as given by (1).

$$EMIRR = \frac{\Delta V_{pp}}{V_{offset_out}} \quad (1)$$

TABLE I. CHARACTERISTICS OF TESTED OP-AMP

Characteristics	LMV651	LMV861 (EMI-hardened)
Power supply	+/- 2.5 V	+/- 2.5 V
Supply current	116 μ A	2.25 mA
Static gain	93 dB	110 dB
GBW product	12 MHz	30 MHz
Slew rate (+/- transition)	3.6 / -2.2 V/ μ s	21.2 / -24.2 V/ μ s
Max. input offset voltage	1.5 mV	1 mV
CMRR	100 dB	93 dB
PSRR	95 dB	93 dB
EMIRR	Not defined	70 - 110 dB (400-2400 MHz)

Both op-amps are mounted in non-inverting amplifier configuration with a gain of two. The populated board is shown in Fig. 2. SMA connectors are placed on non-inverting inputs and op-amp outputs to inject conducted disturbance to these pins. A symmetrical +/- 2.5 V power supply is applied on both devices.

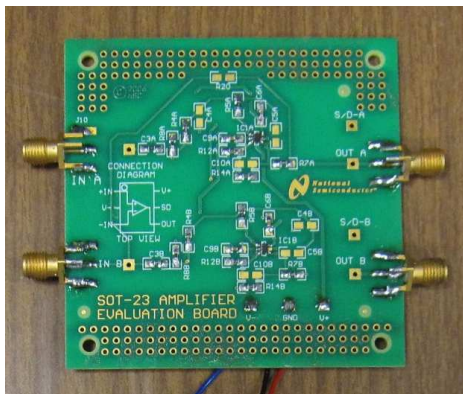


Fig. 2. Evaluation board to test and compare the susceptibility of EMI hardened and non-hardened op-amps

III. CHARACTERIZATION OF THE SUSCEPTIBILITY

A. Initial observation of EM disturbance effect

A significant part of the lab is dedicated to the characterization of the RF susceptibility of op-amp. An initial observation consists in coupling RF disturbances on op-amp terminals. A convenient approach consists in using a magnetic near-field probe excited by a RF signal, in order to identify the most susceptible pins and produce significant radiated disturbance without the need of TEM cell or anechoic chamber. In order to replicate a typical interference scenario, a 500 MHz RF disturbance is modulated by a 10 kHz square signal. The amplitude of the disturbance is set to 13 dBm. The worst case coupling is observed on the PCB trace connected to the non-inverting terminal of both op-amps. Fig. 3 shows the signal induced on the output of the LMV651. Only the envelop of the modulated signal is kept. The incoming disturbance has been rectified or demodulated due to the non-linear behavior of the op-amp to RF out-of-band disturbance. A similar effect is visible on the LMV861, but the amplitude of the induced signal on the output pin is negligible (< 10 mV).

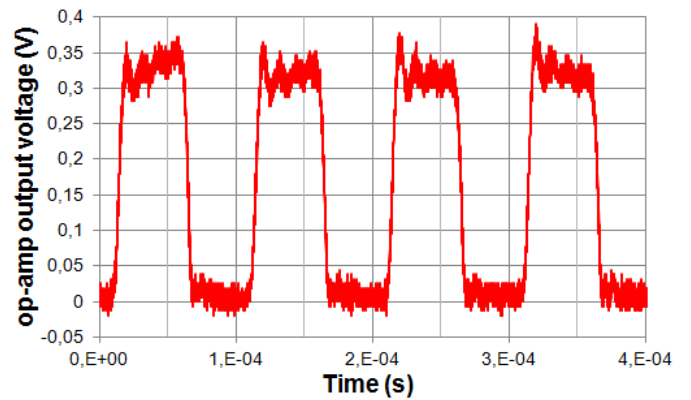


Fig. 3. Illustration of non-linear behavior of op-amp to EM disturbance: output signal measured on LMV651 when a 500 MHz amplitude-modulated perturbation is added is coupled on the non-inverting terminal

The modulation can then be suppressed. The demodulation of a low frequency is replaced by a parasitic offset related to the disturbance amplitude and frequency.

B. Conducted immunity characterization set-up

After this initial experiment, a better characterization set-up must be developed to characterize op-amp susceptibility properly. Due to its good reproducibility level, the standard conducted susceptibility test IEC62132-4 Direct Power Injection (DPI) can be proposed [12]. A presentation of the equipment, a clarification of the forward power and a discussion about the observation of the susceptibility criterion is done during the lab.

The test bench is described in Fig. 4. Continuous wave disturbance from 1 MHz to 1 GHz are generated by a frequency synthesizer and then amplified. The maximum forward power is limited to 25 dBm. The conducted disturbance is superimposed on non-inverting input or output through a bias tee. An oscilloscope probe is placed on the op-

amp output to control the EMI-induced offset. A failure is detected if the offset level exceeds ± 100 mV. High-frequency oscilloscope probes are also placed on inverting and non-inverting inputs to monitor the actual amplitude of the applied disturbance. From these measurements, the EMIRR of both tested op-amps will be extracted.

C. Conducted immunity measurement results

Fig. 5 presents the comparison of the immunity levels of both op-amps, for injection done on non-inverting input and output pins. This result shows clearly that the EMI-hardened version is more robust to EM disturbance, except between 25 and 60 MHz when EM disturbance is coupled either on non-inverting input pin or the output pin.

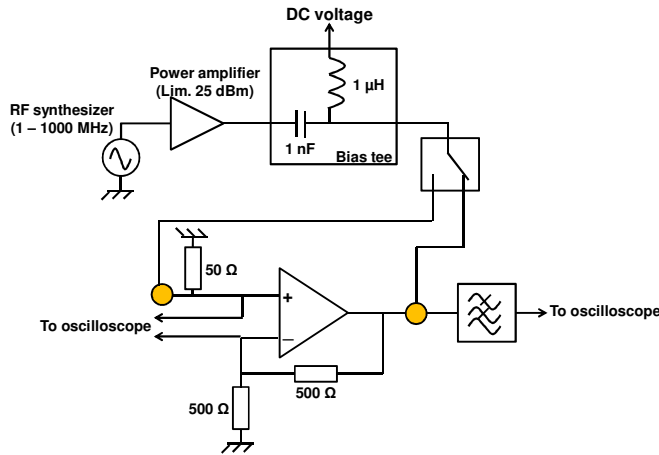


Fig. 4. Description of the conducted susceptibility test bench according to DPI standard [12]

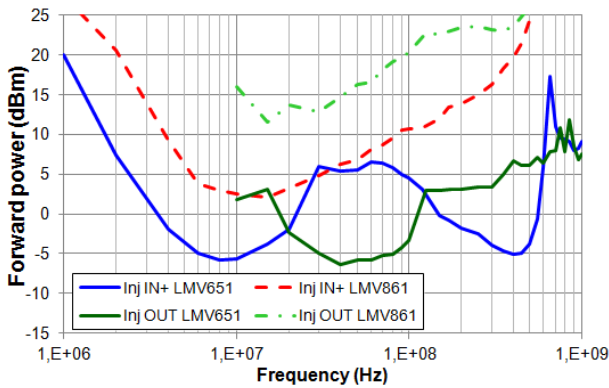


Fig. 5. Conducted immunity measurement results on both tested op-amps: injection on non-inverting input and output pins

The results of injection on input pin IN+ and output pin OUT are reported in Fig. 5 for both devices. It is interesting to observe the response of the op-amp at different frequencies and amplitude level in order to identify the failure mechanisms. Fig. 6. and 8 show the evolution of the offset measured on the LMV651 and LMV861 according to the disturbance amplitude, at four different frequencies. Fig. 7 illustrates the typical output waveform measured at low frequency. Up to some tens of MHz, the offset is essentially positive for the LMV651. Fig. 7 shows that the disturbance is not filtered on the output, but seriously distorted due to the

slew rate limit of the op-amp. However, this slew rate limit is not identical on rising and falling transition of the signal, which results in an offset. It corresponds to the first failure mechanism in op-amp, called asymmetrical slew rate. It is confirmed by Table I, where positive slew rate is nearly 60 % times larger than negative slew rate, resulting in a positive offset. This effect is less significant for the LMV861 because the asymmetry of slew rates on both transition is only 13 %. That's why the LMV861 is more immune than LMV651 below 30 MHz.

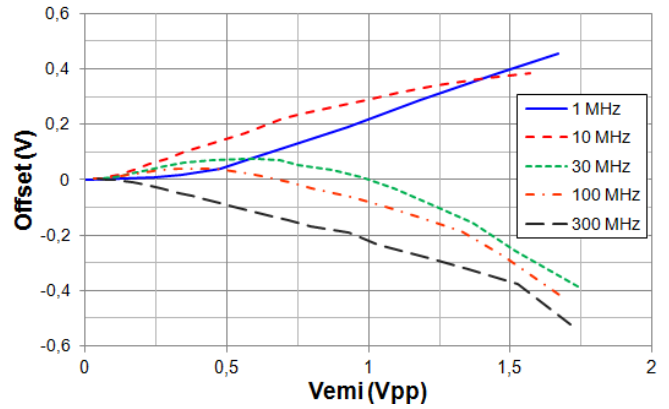


Fig. 6. Evolution of the offset measured on LMV651 (non EMI-hardened) output vs. EM disturbance amplitude and frequency

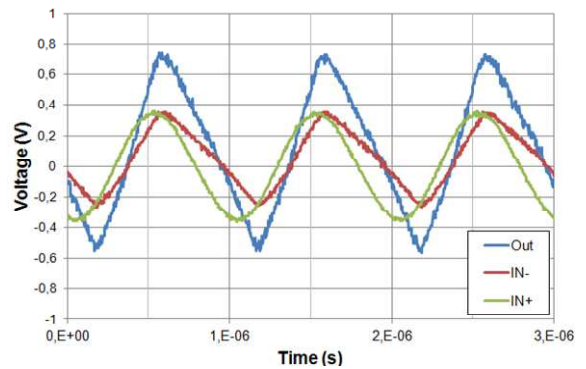


Fig. 7. Illustration of slew rate asymmetry: injection of a 1 MHz continuous wave disturbance on non-inverting input of LMV651

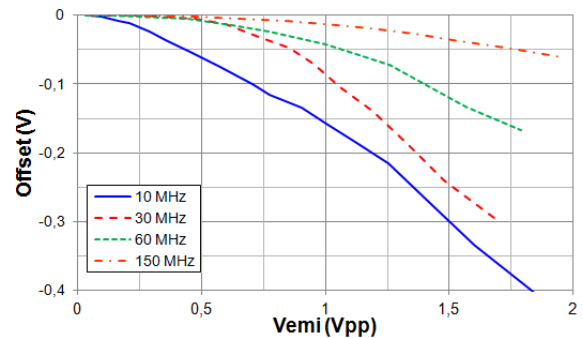


Fig. 8. Evolution of the offset measured on LMV861 (EMI-hardened) output vs. EM disturbance amplitude and frequency

This effect of slew rate asymmetry tends to disappear above several tens of MHz and a negative offset tends to increase rapidly with the disturbance amplitude according to a

non-linear relation. This effect is common to both op-amps and is due to the weak distortion of the disturbance coupled on differential pair inputs. This failure mechanism has been deeply studied in numerous research papers. The offset is related to the differential and common-mode voltages V_{DM} and V_{CM} coupled on op-amp inputs and the finite impedance of the differential pair current source. It results in an imbalance of the current flowing through the differential pair and thus an input related voltage offset V_{off_in} . For an harmonic injection, it is given by (2) theoretically [2] [5].

$$V_{off_in} = \frac{-1}{2|V_{gs} - V_T|} V_{DM} V_{CM} H_{CM} \cos(\phi + \theta) \quad (2)$$

where H_{CM} is related to the structure of the differential pair and parasitic impedance. The sign of the offset is related to the phase θ of differential and common-mode voltages and the phase ϕ of H_{CM} . Depending on the amount of coupling on both inputs, the sign of the offset may change with frequency, as it is observed on LMV651 above 600 MHz. When the amplitude applied on input terminals becomes large, a third failure mechanism appears which lead to a brutal change of the behavior: the offset can increase or decrease very rapidly. As described in [2], this phenomenon, called differential pair asymmetrical cut-off, results of disturbances with amplitude large enough to cut-off the conduction of one transistor of the differential pair. This effect appears when the induced offset exceeds several hundreds of mV, so that it can be discarded.

Both ICs are less sensitive to disturbance coupled on output pin. This situation is actually an indirect coupling on the inverting input pin. Depending on the frequency and the amount of disturbance coupled on inputs, the same type of failures arise. The next part of this paper will be focused on the susceptibility to disturbance coupling on non-inverting input.

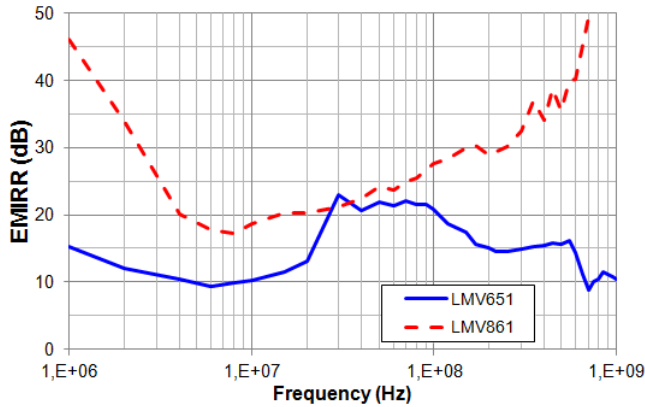


Fig. 9. Extraction of the EMIRR of both op-amps for injection on non-inverting input

D. Extraction of EMIRR

EMIRR is a convenient figure to characterize the susceptibility of a op-amp. Contrary to the forward power measured during DPI test, EMIRR is not affected by the parasitic impedances of PCB traces, external filter and tested

pin. It captures the intrinsic susceptibility of the IC more precisely. Fig. 9 compares the EMIRR of both op-amp for injection on non-inverting input. The EMIRR depends on the targeted offset, since the failure mechanism is non-linear. This result is only valid for an offset of 100 mV. Above 700 MHz, the EMIRR measurement of the LMV861 becomes inaccurate because of the induced offset becomes negligible. The differences in EMIRR trends are partially correlated with the difference in susceptibility levels shown in Fig. 5, since the susceptibility level depends also on the impedance of the IC under test. This result shows that both op-amps are extremely sensitive to RF noise around 10 MHz, just below their gain-bandwidth product, because of slow rate asymmetry. For LMV861, the EMIRR tends to increase rapidly above some tens of MHz. As explained in the datasheet, internal filtering has been added on inputs to increase the immunity of the device. This is not the case for LMV651, which tends to become susceptible above 100 MHz due to weak distortion.

IV. MODELING AND SIMULATION

In this part, a simple approach based on datasheet information and EMIRR measurement results is proposed to produce a first prediction model, which can be built and simulated by students rapidly.

A. Equivalent model of the op-amp

In literature, transistor-based models are used to simulate accurately the op-amp behavior to EM disturbance and propose design change to make it more robust. In practical situations, such a model is not available for end-users since it is not provided by manufacturers. Despite they usually propose equivalent SPICE models, they do not include slew rate asymmetry and weak distortion effects so that susceptibility simulation remains impossible. The only alternative consists in using available information in datasheet and simple measurements to extract parameters of a model dedicated to simulation of EMI-induced offset. From the previous analysis of measurement results, we propose to develop an analog behavioral model which simulates the slew rate asymmetry and the weak distortion effects. The proposed model is compatible with SPICE. It is built and simulated with the IC-EMC [10].

The overall structure of the proposed op-amp susceptibility model is described in Fig. 10. Only the slew rate asymmetry and weak distortion effects are included in this model. Asymmetrical cut-off is not taken into account since measurement results show that a significant offset voltage is induced even if this failure mechanism is not triggered.

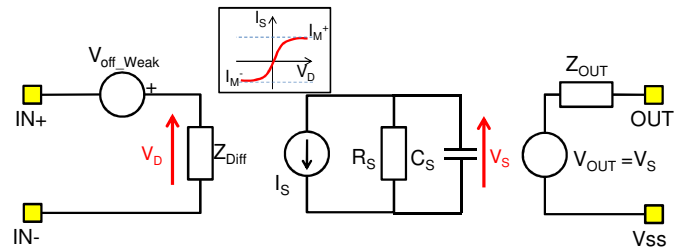


Fig. 10. Structure of the general analog behavioral model of op-amp

Two elements generate EMI-induced offset: the current source I_S which is related to slew rate limitation, and the voltage source V_{off_weak} which is associated to weak distortion effect. The slew rate limitation is modeled according to (3), which depends on several parameters defined by (4) to (6). They are related to the open-loop static gain A_0 and the gain-product bandwidth GBW of the op-amp, which is modeled by a simple RC circuit. All these values can be found in op-amp datasheet or extracted experimentally.

$$I_S = \text{Max}[I_M^+ \tanh(K^+ \cdot V_D), I_M^- \tanh(K^- \cdot V_D)] \quad (3)$$

$$I_M^+ = SR^+ \cdot C_{in} \quad I_M^- = SR^- \cdot C_{in} \quad (4)$$

$$R_{in} = \frac{A_0}{2\pi \cdot GBW \cdot C_{in}} \quad (5)$$

$$K^+ = \frac{A_0}{I_M^+ \cdot R_{in}} \quad K^- = \frac{A_0}{I_M^- \cdot R_{in}} \quad (6)$$

The offset due to weak distortion effect is determined from the theoretical expression (2), transformed in the more general form (7). V_{DM} and V_{CM} are the differential and common-mode voltages applied on op-amp differential inputs. The frequency dependent term H_{CM} relates the offset due to weak distortion and common-mode voltage applied on op-amp differential inputs. As weak distortion effect is not described by manufacturers, it has to be extracted experimentally. However, its extraction is the most complex step of the modeling process, because the measured offset is the superposition of two non-linear effects: slew rate asymmetry and weak distortion, which are not independent completely. The proposed set-up consists in measuring the evolution of the offset according to the amplitude of the voltages applied on differential inputs at several frequencies. Then the analog behavioral model is used to simulate the evolution of the offset. At each frequency, the value of H_{CM} is tuned to fit the measured evolution of the offset. A transfer function is adjusted and integrated in the model.

$$V_{off_weak} = \text{Average}(H_{CM}(f) V_{DM} V_{CM}) \quad (7)$$

The susceptibility of an IC is also dependent on the amount of disturbance coupled on its terminals, which is related to the interconnects and crossed devices. A precise susceptibility simulation requires equivalent impedance models of the interaction between IC terminals, but also external filtering and PCB interconnects. They can be extracted from S parameter measurement for example. As this step is quite long and tedious, a simplified model version is

tested with the students. It will be sufficient to illustrate the susceptibility simulation flow and determine the general susceptibility level of tested op-amp. It only includes the effect of the bias tee and the input impedance of the non inverting input. The couplings between input and output pins are neglected.

B. Validation of the model

Firstly, the EMIRR of both op-amp to EM disturbance coupled on the non-inverting input is simulated. It consists in determining the voltage of the disturbance to induce a given amount of offset. The complete models of the test board and DPI test bench are not taken into account. This simulation aims at verifying that the intrinsic behavior of the device to EM disturbance is correctly predicted. Comparisons between measurements and simulations for both op-amps are shown in Fig. 11. For both op-amps, a good agreement (difference less than 3 dB) between measured and simulated curves is obtained between 1 MHz and 550 MHz. The loss of accuracy around 10 MHz is related to the weakness of the slew rate limitation model, which is too simple to simulate precisely the exact waveform of the output signal. For the LMV651, above 550 MHz, the model underestimates the susceptibility of the op-amp. As discussed in III, the evolution of the offset is strongly influenced by the amount of disturbance coupled on both op-amp inputs. However, as an initial choice of our modeling approach was to neglect the coupling onto the inverting input, this effect cannot be correctly predicted. It would require measurement of the couplings between IC pins and extraction of an equivalent model. The gap observed between measurement and simulation result of LMV861 above 700 MHz is mainly related to measurement inaccuracies. Anyway, the model predicts correctly the strong robustness of this device to high frequency disturbance.

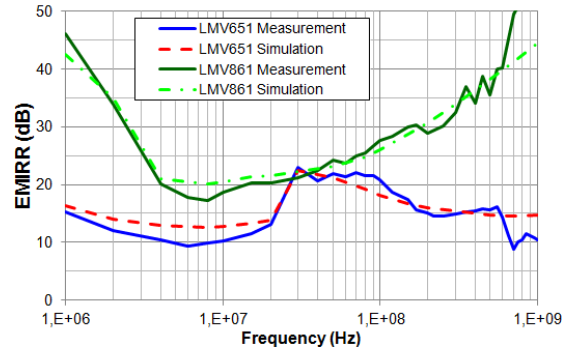


Fig. 11. Comparison between measurement and simulation of the EMIRR of the LMV651 and LMV861

In a second step, the models of the DPI test bench and test board are included in order to simulate the susceptibility level with DPI test. Measurement and simulation results are compared in Fig. 12. The general trend of the susceptibility level for both op-amps is simulated. For LMV861, except a maximum error of 3 dB in low frequency due to the weakness of the slew rate limitation model, the agreement with measurement is correct. The correlation between measurement and simulation is not as excellent for LMV651. In low frequency, the weakness of the slew rate model explains the gap between measurement and simulation results. The

agreement tends to degrade above some hundreds of MHz because of the weakness of the impedance model of the IC and PCB. However, it is interesting to underline that even a simple model is able to catch general trend and the global level of susceptibility of this IC up to several hundreds of MHz. To extend the model bandwidth and increase its accuracy, improvement of the impedance model must be brought.

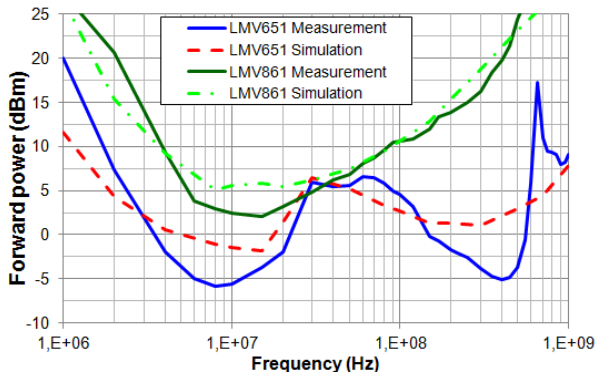


Fig. 12. Comparison between measurement and simulation of the susceptibility levels of the LMV651 and LMV861

C. Test of the model in another configuration

Modeling the susceptibility of an IC aims at predicting the susceptibility level, even in other configurations that those used to adjust the model. In this part, the LMV651 op-amp (non EMI-hardened version) is mounted in a voltage follower configuration. In order to improve the noise rejection, an external 15 MHz RC low-pass filter is also placed at the input. Measurements of EMIRR and DPI test are done in this configuration when EM disturbance is conducted on the non-inverting input. The model developed in the previous part is reused to simulate the susceptibility in this new configuration. The results are compared in Fig. 13. In low frequency, the op-amp in follower configuration is less susceptible than in amplifier configuration, because a larger disturbance is required on non inverting input to reach the slew rate limitation. Above 15 MHz, the low-pass filter rejects the noise coupled on the non-inverting input and contributes to improve the overall immunity. Up to 400 MHz, the proposed model is in good agreement with measurement results since it predicts correctly the correct trend of the susceptibility level. A loss of accuracy is observed above 60 MHz, where the gap between measurement and simulation reaches 5 dB. Above 400 MHz, simulation and measurement results diverge. This is not only due to the limitations of the model previously explained. During measurements, we observe that a sudden increase of the output offset arise when a given level of disturbance is applied. This effect is certainly related to differential pair asymmetrical cut-off mechanism, which is not taken into account in our model.

V. CONCLUSION

This paper has presented the content of a practical training dedicated to the susceptibility of op-amps to electromagnetic disturbances. It aims at illustrating typical failure mechanisms on a real case studies, comparing EMI robust and non-robust

device, and building prediction models. A large part of the paper was dedicated to the construction of an analog behavioral model of op-amp which can be constructed rapidly from non-confidential information, only obtained from datasheet and measurements. Results show that this simple model, even without a full impedance model of the IC and the surrounding PCB, is sufficient to determine the general trend of the susceptibility level of the op-amp mounted in various configurations up to several hundreds of MHz. It covers the needs of most IC end-users to predict potential electromagnetic interferences in their electronic equipments.

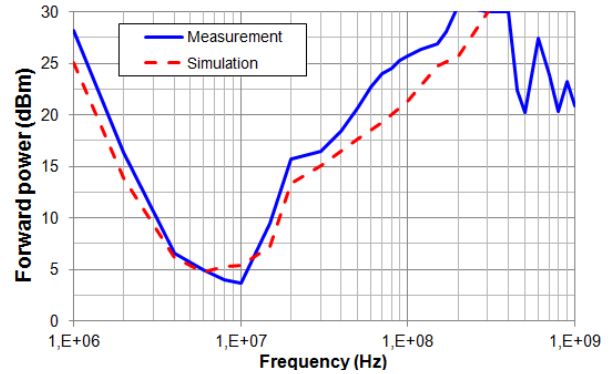


Fig. 13. Comparison between measurement and simulation of the susceptibility level of the LMV651 in another configuration (follower and external low-pass filter)

References

- [1] G. Masetti, S. Graffi, D. Golzio, ZS. M. Kovacs, "Failures induced on Analog Integrated Circuits by conveyed Electromagnetic Interferences: a Review", *Microelectronic Reliability*, vol. 36, no 7/8, pp. 955-972, 1996.
- [2] J. M. Redouté, M. Steyaert, *EMC of Analog Integrated Circuits*, Springer, 2010.
- [3] J. G. Tront, J. J. Whalen, C. E. Larson, J. M. Roe, "Computer-Aided Analysis of RFI Effects in Operational Amplifiers", *IEEE Trans. on Electromagnetic compatibility*, vol. 21, no 4, Nov. 1979.
- [4] D. Golzio, S. Graffi, G. Masetti, "New Circuit Modeling of Operational Amplifiers", *IEEE Int. Symposium on EMC, USA*, 1989.
- [5] F. Fiori, "A New Nonlinear Model of EMI-Induced Distortion Phenomena in Feedback CMOS Operational Amplifiers", *IEEE Trans on EMC*, vol. 44, no 4, pp. 495-502, Nov. 2002.
- [6] S. Graffi, G. Masetti, A. Piovaccari, "Criteria to Reduce Failures induced from conveyed Electromagnetic Interferences on CMOS Operational Amplifiers", *Microelectronic Reliability*, vol. 37, no 1, pp. 95-113, January 1997.
- [7] F. Fiori, "Design of an Operational Amplifier Input Stage Immune to EMI", *IEEE Trans. on EMC*, vol. 49, no 4, pp. 834 - 839, Nov. 2007.
- [8] A. Richelli, "EMI Susceptibility Issue in Analog Front-End for Sensor Applications - Review article", *Journal of Sensors*, 2016.
- [9] "A One-Week Training in Electromagnetic Compatibility of Integrated Circuits", more information on www.ic-emc.org.
- [10] IC-EMC v2.9, freeware available on www.ic-emc.org.
- [11] AN-1606 551012875, 551012922 Universal OpAmp Evaluation Boards (SOT-23 and SC-70), User's guide, Texas Instruments, May 2013.
- [12] IEC 62132-4 – edition 1.0: Integrated circuits - Measurement of electromagnetic immunity - Part 4: Direct RF power injection method, 2006-02-21.