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# Compact thermal modelling for fast simulating consequences of pump defect: application to power module with double efficient cooling

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## Abstract

Compact thermal modelling can provide useful tools for electronic systems designers. Indeed, the generation of simplified but accurate thermal models enables to reduce the number of 3D thermal simulations with high complexity and expensive computation time. Another benefit is the possibility for device manufacturers to provide systems suppliers with extended datasheets in the form of Compact Thermal Model (CTM) without revealing the device structure or used materials. The CTM can be applied to multi-chips systems and it is auto-adaptive to boundary conditions change.

In this paper, CTM methodology is defined for an efficient power module structure with double side cooling. The extracted CTM is used to investigate cooling pump defects in the design phase of the inverter. The results are compared with a 3D thermal model using Computational Fluid Dynamics software (6SigmaET).

## 1 Introduction

Thermal models one can find in CTM literature are generally defined for particular devices [1] [2] whereas our aim is to develop generic CTM for different power module topologies. The methodology of compact thermal modelling presented in this paper is applied to an efficient double cooling module intended for an automotive power electronics system. This module has been developed by the French Institute of Technology Antoine de Saint Exupéry in collaboration with aPSI<sup>3D</sup> [3]. This power module consists of an inverter leg (fig. 1) composed of two IGBTs and two diodes in configuration of High Side (HS) and Low Side (LS) switches (fig. 2). Notations used for the devices are T\_LS: LS IGBT, D\_LS: LS diode, T\_HS: HS IGBT and D\_HS: HS diode.

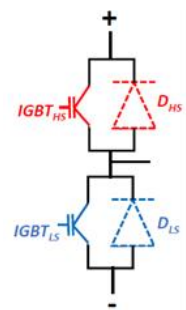


Figure 1: Inverter leg

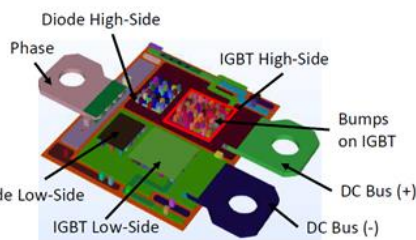


Figure 2: Power module

This module is double side cooled (fig.3) [4] using glycol water which flows through the cooling pipes. For test needs, the cooling efficiency can be changed as one wishes by adjusting the glycol water flow.

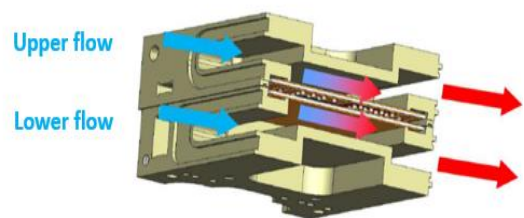


Figure 3: Illustration double cooling flow of the power module

The objective of this work is to provide electronic systems designers with accurate thermal models by extracting CTM from 3D thermal simulations using a Computational Fluid Dynamics software (6SigmaET). As these last can use these CTMs to investigate the consequences of cooling system default, the extracted models have to be auto-adaptive according to boundary conditions. As several chips are located on the same Active Metal Brazing (AMB) substrate, one has to consider the thermal coupling between these heat sources. The equivalent electrical network should also models physical phenomena as the spreading of 3D heat flux in the structure. To validate our thermal model, the results obtained with CTM will be compared with 3D thermal simulations.

## 2 Compact Thermal Model of the power module

### 2.1 Extraction of CTM

The objective of CTM is to determine a simplified representation of the thermal behaviour of an electronic system, compared to a 3D thermal model, with respect to the following requirements:

- Extraction of a simple electrical network with a limited number of elements RC, even for complex structures, to ensure a reduced computation time
- Auto-adaptation to boundary conditions
- Modelling the behaviour of 3D heat flux
- Sufficient accuracy (<10 %)

One main difficulty is to consider the heating between the chips due to their proximity on the substrate. The thermal coupling between heat sources is based on the Optimal Thermal Coupling Point (OTCP) [5].

As an example, regarding two heat sources HS1 and HS2, their thermal interactive effect is assessed with the following methodology: when HS1 dissipates power and HS2 is turned OFF, one isothermal surface, similar to a half-sphere, can be found at the same temperature than HS2. The same procedure is repeated when HS1 is turned OFF and HS2 is turned ON. The thermal coupling is defined with a particular point so-called OTCP located at the intersection of the two isothermal arcs previously defined. Hence, the steady state CTM can be defined (fig. 4). Knowing the dissipated powers of the component, thermal resistances are calculated according to the formula:

$$R_{th} = \frac{\Delta T}{P} \text{ [K.W}^{-1}\text{]} \quad (1)$$

With  $\Delta T$  : temperature difference [K], P : dissipated power [W]

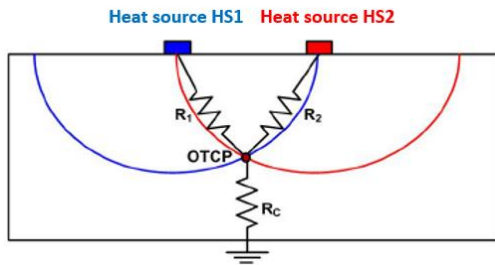


Figure 4: Illustration of the Optimal Thermal Coupling Point (OTCP)

In the case of our application, the CTM is extracted for the power module, with double side cooling, considering four heat sources (two IGBTs and two diodes) and two cooling paths as boundary conditions. A thermal model is defined for each heat source, from the junction to the cooling system, with resistances in series between each OTCP representing the thermal interaction between the active chip and the others

(fig. 5). For example, in the case where  $T_{LS}$  is the only active device thus the hottest inactive chip will be  $D_{LS}$ , followed by  $T_{HS}$  and  $D_{HS}$ . This descending order of temperatures defines the nodes of the equivalent electrical network. The resultant steady state CTM for the  $T_{LS}$  device is presented fig. 6.

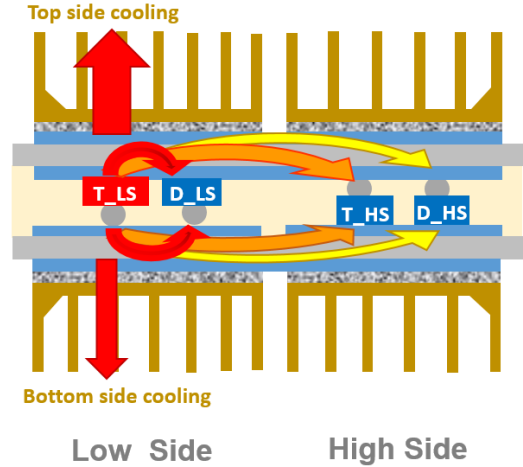


Figure 5: Schematic view of heat flux paths describing how  $T_{LS}$  powered ON thermally impacts the other chips

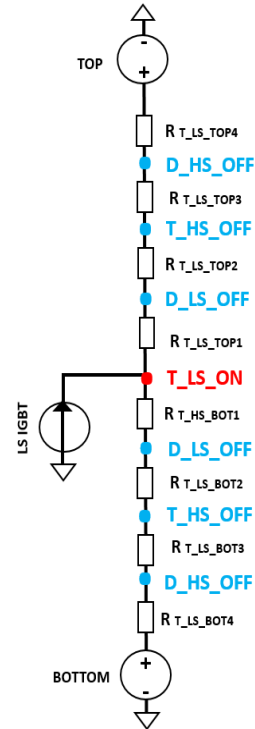


Figure 6: Compact Thermal Model of LS IGBT

Finally, the junction temperature of each source is calculated by adding the temperature due to the activation of the source itself and the temperature rise linked to the thermal coupling between heat sources [6]. For example, the junction temperature of the LS IGBT is equal to:

$$T_{jT\_LS} = T_{LS\_ON} + \sum_{i=3} T_{LS\_OFF}(i) \quad [^{\circ}\text{C}] \quad (2)$$

With  $T_{LS\_ON}$ : temperature of LS IGBT when it is the only device turned ON [ $^{\circ}\text{C}$ ],  $T_{LS\_OFF}$ : temperature of inactivate LS IGBT when another chip is switched ON [ $^{\circ}\text{C}$ ]

## 2.2 Variations of thermal resistances

3D thermal simulations have been performed using Computational Fluid Dynamics software (6SigmaET) for 5 cooling conditions, by adjusting the glycol water flow, to simulate operational to degraded cooling system modes i.e. the cooling liquid flow is significantly reduced in case of a pump defect.

The results data of the 3D thermal simulations are the temperatures of all devices for each cooling system configuration. These results are used to find a control law representing the dependence between thermal resistances and the heat flux through the two cooling paths. Knowing the temperature of the four chips in every case, the part of the heat flux going through the top ( $P_{top}$ ) and the bottom side ( $P_{bottom}$ ) of the module, thus thermal resistances can be calculated. As an example, here are expressions of some thermal resistances of fig. 6:

$$R_{T\_LS\_BOT1} = \frac{T(T_{LS\_ON}) - T(D_{LS\_OFF})}{P_{bottom}} \quad [\text{K}\cdot\text{W}^{-1}] \quad (3)$$

$$R_{T\_LS\_BOT2} = \frac{T(D_{LS\_OFF}) - T(T_{HS\_OFF})}{P_{bottom}} \quad [\text{K}\cdot\text{W}^{-1}] \quad (4)$$

$$R_{T\_LS\_TOP1} = \frac{T(T_{LS\_ON}) - T(D_{LS\_OFF})}{P_{top}} \quad [\text{K}\cdot\text{W}^{-1}] \quad (5)$$

A polynomial fitting is chosen to model the variations of thermal resistances as a representation of the transition from 3D thermal phenomena to an equivalent electrical network (fig.7 and fig.8).

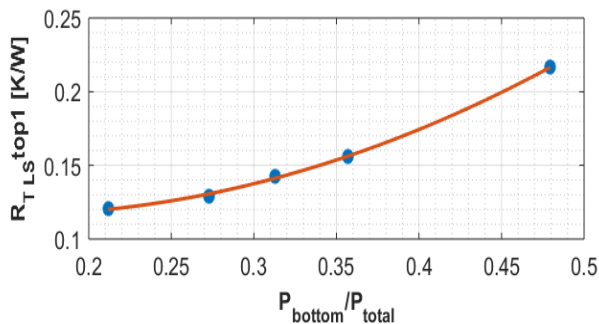


Figure 7: Variation law of thermal resistance  $R_{T\_LS\_top1}$

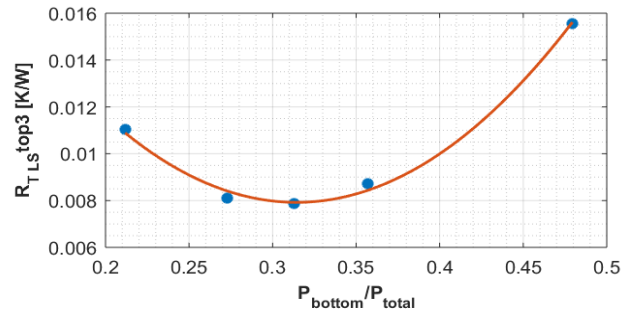


Figure 8: Variation law of thermal resistance  $R_{T\_LS\_top3}$

In case of a pump defect, the spreading of the heat flux in the structure is extended due to faulty cooling effects. Consequently, furthest chips from the heat source can be more heated which changes the order of the temperatures of the inactive devices.

Considering the CTM for LS IGBT such as the only chip turned ON (fig. 6), when the bottom side cooling is degraded i.e. the water glycol flow is set at 0,5l/min for 3D thermal simulation, the hottest inactive device becomes  $T_{HS}$ , then  $D_{LS}$  and  $D_{HS}$ . The order of the nodes of the CTM is changed compared to fig.6. Control laws of thermal resistances assigns negative sign to some resistances take into account this 3D thermal effect (fig.9).

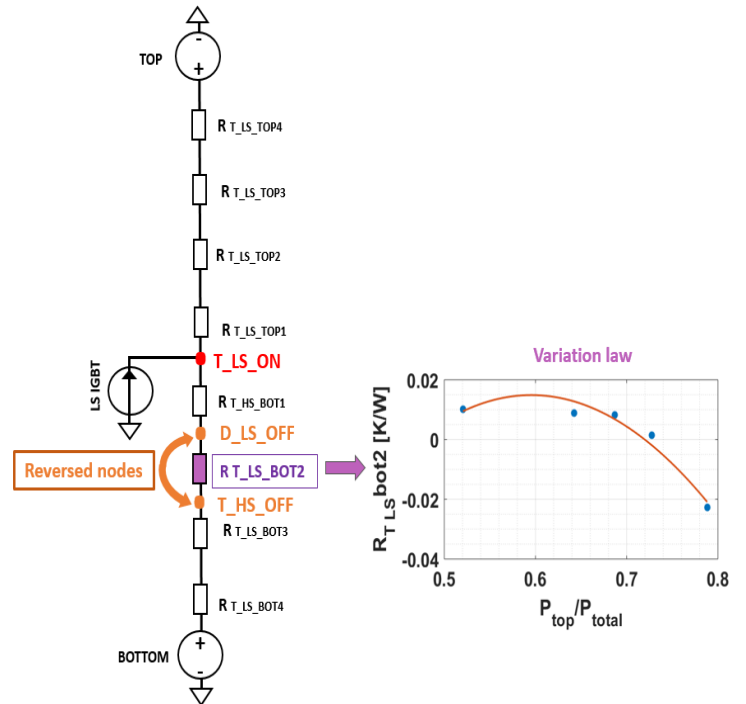


Figure 9: Illustration of CTM considering heat flux paths change

Therefore, the extracted CTM considers different paths of 3D heat flux depending on the cooling system configuration and it is auto-adaptive in respect of boundary conditions: the solver recalculates the values of thermal resistances for any change of the glycol water flow.

### 3 Comparison CTM - 3D thermal model

The extracted CTM will be compared with 3D thermal simulations using Computational Fluid Dynamics software (6SigmaET).

A 3D thermal simulation is performed with the following cooling configuration: upper glycol water flow is set at 4 l/min and lower flow is set at 4 l/min. The temperature of the glycol water is equal to  $T_{ref} = 65^\circ\text{C}$ .

The devices dissipate the following powers:

Heat sources	Dissipated power [W]
HS IGBT	682
HS diode	146
LS IGBT	682
LS diode	146

The junction temperature of each device will be calculated with their extracted CTM. The first step is to determine the ratio of the heat flux going through the top and the bottom side of the power module. An iteration procedure is defined to test ratios  $\frac{P_{top}}{P_{tot}}$  and  $\frac{P_{bottom}}{P_{tot}}$  with  $\frac{P_{bottom}}{P_{tot}} = 1 - \frac{P_{top}}{P_{tot}}$ . Once a ratio is chosen, the values of global thermal resistances  $R_{bot}$  and  $R_{top}$  are read on their respective control law graph (fig. 10).

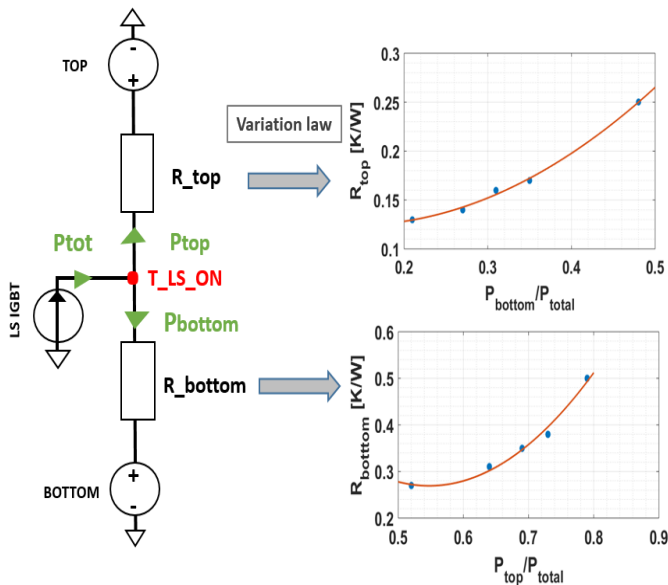


Figure 10: Determination of ratios of top and bottom heat flux

Then the temperature of the device, when it is the only one switched ON, is calculated with two expressions:

$$T_{j\ top} = R_{top} P_{top} + T_{ref} \quad (6)$$

$$T_{j\ bottom} = R_{bottom} P_{bottom} + T_{ref} \quad (7)$$

The iteration procedure ends when the following requirements are fulfilled:

$$\begin{cases} P_{bot} + P_{top} = P_{tot} \\ T_{j\ top} = T_{j\ bottom} \end{cases} \quad (8)$$

For the studied power module, heat flux ratio is estimated for HS devices resp. LS devices: top side cooling evacuates 30% resp. 70% of the total flux and 70% resp. 30% goes to bottom side cooling.

The junction temperatures calculated with CTM method are compared with 3D thermal simulations using the relative error criterion:

$$\epsilon_r = 100 \frac{|T_{j\ CTM} - T_{j\ 3D}|}{T_{j\ 3D} - T_{ref}} \quad [\%] \quad (9)$$

With  $T_{j\ CTM}$ : junction temperature with CTM [ $^\circ\text{C}$ ],  $T_{j\ 3D}$ : junction temperature with 3D model [ $^\circ\text{C}$ ],  $T_{ref}$ : cooling liquid temperature [ $^\circ\text{C}$ ]

Heat source	$T_{j\ CTM}$ [ $^\circ\text{C}$ ]	$T_{j\ 3D}$ [ $^\circ\text{C}$ ]	Relative error [%]
HS IGBT	151,1	150,3	0,94
HS diode	103,4	103,2	0,52
LS IGBT	141,46	142,46	1,29
LS diode	99,7	100,18	1,36

The achieved results by CTM method are validated with a satisfactory accuracy compared to 3D thermal simulations. For 3D model, it should be noticed that cooling liquid (glycol water) properties and silicon thermal conductivity are defined at  $20^\circ\text{C}$  and not at  $T_{ref} = 65^\circ\text{C}$  which can explain the values gap between the two models. Prospects to improve compact thermal modelling will be to consider the temperature dependence of silicon thermal conductivity.

### 4 Conclusion

The presented methodology of a Compact Thermal Model provides with satisfactory accuracy the same results then those given by 3D thermal simulations. Indeed, CTMs are relevant solutions to simplify the representation of complex power electronics systems and to reduce the number of 3D thermal simulations. These simplified models present lower

computation time, take into account the thermal coupling between several heat sources while being auto-adaptive for any boundary conditions change.

In this paper, a static Compact Thermal Model is extracted for the simulation of a power module with four chips on the same AMB substrate with a double side cooling. This power module is difficult to model due to multiple thermal flux paths that totally change according to boundary conditions. In this way, CTM methodology developed at LAAS-CNRS has been improved to adapt to complex structures that are frequently encountered nowadays. The extracted CTM remains valid for extreme boundary conditions allowing investigation of the consequences of cooling system defects. Resistances variation laws take into account the 3D thermal phenomena as the heat flux spreading and its multiple paths while changing. Future work will deal with the evolution in time of the junction temperatures using a transient compact thermal model.

### Acknowledgements

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