Degradation indicators of power-GaN-HEMT under switching power-cycling

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Abstract

This paper describes the design of a power-cycling test bench to study the reliability of power-GaN-HEMT power switches. The aim of the presented paper is to study the measurable electrical consequences of internal degradation with aging. The shift of these measured parameters can be considered as reliability indicators. With the aim to decorrelate thermomechanical effects from internal GaN-specific degradation, the temperature was limited by choosing the stress parameters with the use of an infrared camera. The power-cycling test was designed with GaN-specific gate drivers to consider the pGaN-gate requirements. Thorough the power-cycling test we have tracked the evolution of electrical parameters that have been identified as degradation indicators. Finally, we have studied the link between the stress parameters and the degradation, as well as the correlation between different degradation indicators.

1. Introduction

Gallium nitride (GaN) has come to be a very promising material for the fabrication of power transistors. Power-GaN-HEMT (High-Electron Mobility Transistor) in Al_xGaN_{1-x}/GaN heterojunction is the up-and-coming device for energy management in space applications. GaN tolerates higher operational temperatures than silicon, and it is an inherently radiation-hard semiconductor material. In addition, GaN-based transistors offer remarkable performances for power switching energy converters like low on-resistance and high power densities compared to silicon-based devices (MOSFET, IGBT). Furthermore, due to its higher switching frequency, smaller and lighter power converters can be conceived, in as much the value of passive devices can be reduced (inductors and capacitors) when operating at higher frequencies.

Nonetheless, extensive utilization of power-GaN-HEMT remains limited because of lack of knowledge in the aging and reliability. The comprehension of the GaN-specific failure mechanisms is necessary to achieve a large-scale deployment of GaN devices. Conventional test procedures used to test silicon devices [1] do not cover the reliability requirements for GaN, especially regarding trapping effects.

New degradation indicators have been proposed to study the aging of power GaN HEMTS in [2]. In [3] is studied the effect of traps in the threshold voltage V_{TH} in GaN HEMT for RF applications (normally-on devices) showing that the traps beneath the gate can cause V_{TH} shift. Other authors [4] studied the role of traps in MOS-HEMTs by using the C(V) hysteresis measurement. Nevertheless, the role of traps in commercial power GaN-HEMTs (normally-on enhancement-mode devices with pGaN gate) have to be studied.

With the aim of obtaining reliability data of power GaN devices, we apply a power-cycling test on discrete commercial devices from different manufacturers. The selected devices are enhancement-mode transistors with pGaN-gate and low-drain-to source blocking voltage (100 V - 200 V), because are the usual values used in space energy management. The power-cycling test is described in section 2, the degradation indicators measured to track the devices evolution are shown in section 3

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and the results are presented in section 4.

2. Power-cycling test

2.1. Power-cycling purpose

The aim of this active power-cycling procedure is to obtain reliability data in a short period of time, accelerating the stress that the device would undergo in a power-switching converter.

The activation of failure mechanisms changes on each stage of the switching cycle in power-switching converters [5]:

- During the OFF state (V_{GS} = 0 V, V_{DS} = V_{in}) the GaN device is under a high electric field. In this phase, trapping effects can degrade the On-Resistance, which will be observed just after the turn-on. This transient phenomenon known as Dynamic On-Resistance is a GaN-HEMT specific drift effect. [6]
- In the switching phase, both a high electric field and a high current will be present in hard-switching operation. In addition, an eventual overshoot in the gate could damage the gate stack (V_{GS} > V_{GSMAX}) generating a shift in the threshold voltage V_{TH} and increasing the gate leakage current I_G.
- During ON state (V_{GS} > V_{GSTH}), we can observe the Dynamic On-Resistance effect. Depending on the trapped charge, ON-state-losses can be noteworthy, compromising the efficiency of power-switching converters.

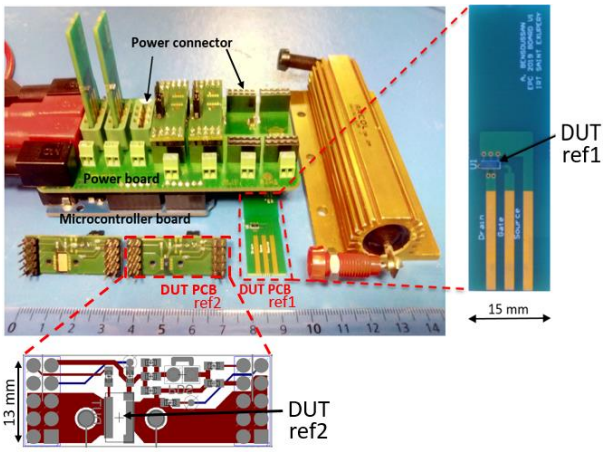


Fig. 1. Power-cycling boards, DUTs and connectors

It is needed to characterize the device under test throughout the power-cycling. That is the reason why the device is not soldered in the power-cycling board, but soldered in a small PCB which is plugged by connectors in order to plug and unplug the device in the power-cycling bench (see fig.1) and in the curve tracer. It allow us to take out the DUT track how the electrical parameters are affected by the aging. In the curve tracer HP4142B we extract the $I_D(V_{DS})$ curve for several V_G values the $I_D(V_{GS})$ curve –from witch V_{TH} is deduced– and the $I_G(V_{GS})$ leakage current.

2.2. Choosing the stress parameters

The purpose of this test is to control all the electrical parameters causing stress in a power-switching converter. Two main causes of stress during the power-cycling are controlled: the gate voltage and the power parameters A microcontroller board connected to the power-cycling board gives the gate voltage. By programming the microcontroller, we can regulate the frequency, the duty cycle and the gate voltage for each device under test. The microcontroller outputs are pulse-width modulation channels (PWM) associated to GaN-compatible drivers, connected with pull-up and pull-down resistors as suggested by manufacturers in order to protect the pGaN gate [7]. The power parameters are the drain voltage V_{DS} and the drain current I_D which is fixed by the power resistor connected to the load connector.

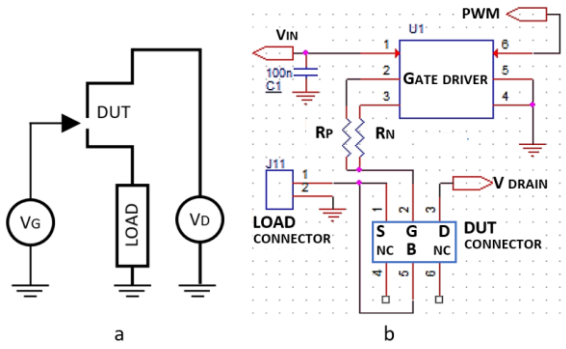


Fig. 2. Simplified electric circuit (a), and electric schematic of the power-cycling board (b)

We apply a step-stress consisting of incremental values of drain current with the purpose of finding the parameters that causes a gradual degradation, avoiding a fast burnout of the device. Each step of the power-cycling is a two-day stress. The power parameters for the first step (S1) consist of I_D 1A and V_D 10V; S2 parameters are I_D 2A and V_D 20V; S2 parameters are I_D 4A and V_D 40V, being each stress the double of the previous one.

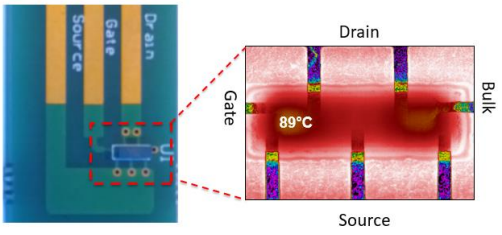


Fig. 3. DUT PCB and infrared image

To choose the stress parameters, thermomechanical effects have been considered. In [8] the author has demonstrated that high temperature swings can produce mechanical degradation due to coefficient of thermal expansion (CTE) mismatch between the device and the board, combined with high power densities in power GaN HEMTs. The aim of this paper is to study internal GaN-specific degradation mechanisms such as the trapping effects in the gate region, not solder or packaging issues.

With the purpose of being sure thermo-mechanical failure mechanisms such as delamination of solder due to high temperature fluctuations are not triggered, we measure the temperature with an infrared (IR) camera (see fig.3) and the Normalized Thermal Impedance Z_θ given by manufacturers. We make sure that the chosen stress parameters do not heat the devices at more than 100°C and $\Delta T<25°C$. The switching frequency, an important parameter that determines ΔT, is fixed to 1 kHz after the IR camera tests. This frequency is high enough to limit the temperature fluctuation and, at the same time, allow us measure properly the temperature with the IR camera (note that the sampling frequency of the camera is limited).

3. Measurements

A set of tests are prepared in order to track the evolution of the devices under test during the power cycling. To trace the I(V) curves we use the curve tracer HP4142B, with which we can measure up to 10 A. The C(V) curves are measured using the Agilent B1505 Power Device Analyzer. Each measurement has the objective of studying one drift effect, which is associated with its physical origin, as shown in table 1.

Drift effect	Physical origin	Measurement
Dynamic R_{DSON} increase	Trapping in GaN buffer and surface trapping between drain and gate	$C_G(V_G)$ hysteresis measurement
Time-Dependent degradation	Generation of drain-source, gate-channel paths and vertical breakdown	Leakage current measurement
V_{TH} shift	Electron trapping beneath the gate	$I_D(V_{GS})$ curve, $I_D(V_{DS})$ for several V_{GS} values
I_G leakage current	Path creation in the gate, Trap-assisted tunnelling	$C_G(V_G)$ hysteresis, $I_G(V_{GS})$ curve

Table. 1. Measurements realized to study each drift effect and its physical origin, based in [9]

In this work, we want to study the evolution of the trapping effects causing V_{TH} shift and Dynamic On-Resistance (also known under the name "current collapse" for RF GaN HEMT [10]). This drift effect produces extra losses in ON state and reduces the efficiency in power-switching converters. Dynamic On-Resistance is a transient effect generated by trapped electrons (see fig.4). The On-Resistance just after the turn-on is higher than the steady On-Resistance value (or static R_{DSON}), which is given in the datasheet (see fig.5). The trapped electrons nearby the channel create a local electric field that increases the resistance in the channel [11].

Trapped electrons have to be released to reach the steady On-Resistance value. These electrons can be trapped in impurities in the GaN buffer layer, the Al_xGaN_{1-x} layer, the SiN passivation layer or dislocations produced by the lattice mismatch between the silicon substrate and GaN buffer, even if the transition layer attempts to reduce this mismatch progressively.

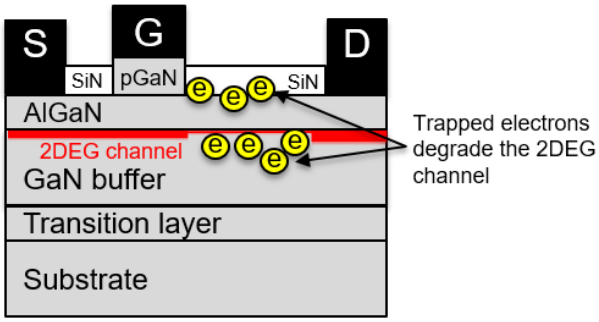
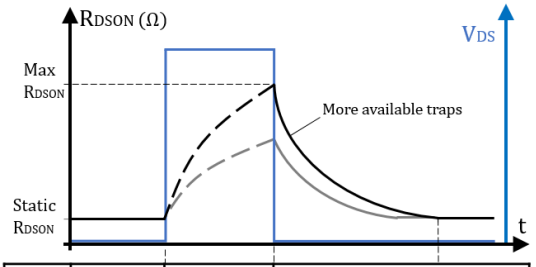


Fig 4. Trapped electrons in the GaN HEMT structure, based in [12].

A high electric field during off-state (high V_{DS}) and a long the time in off-state increases the On-Resistance value after the turn-on [13], because more electrons can be trapped (as they have more time and more energy to be trapped). Trapped electrons are nearby the sharp edges of the drain and gate electrodes, where the electric field is higher. When the OFF-time is long enough to fill all the avaiable traps, the R_{DSON} will not increase anymore, Dynamic On-Resistance is saturated.



State	ON	OFF	ON	
Traps	Empty traps	Trapping time	Detrapping time	Empty traps
RDSON	Static	Increasing	Decreasing	Static

Fig 5. Evolution of the On-Resistance in a switching cycle, based in [13].

It is known that traps in GaN devices can be found because of impurities, native defects in the fabrication [14]. In this work we want to investigate if new traps can be created with the aging in a switching power-cycling.

To investigate this phenomena we realize $C_G(V)$ curves with up and down sweeps in V_G, as shown in [11]. The arrow close to each curve in fig.6 marks sweep directions.

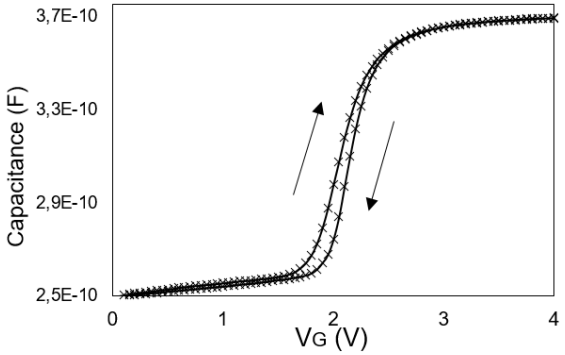


Fig 6. $C_G(V)$ curve of a GaN HEMT before the aging

This curve is extracted with the Agilent B1505 Power Device analyser at 300K, at 1MHz and with a step of 50 mV. We have measured the surface hysteresis at different temperatures in order to find the surface maximum, which we have found at around 300K. In this curve, it is identified a hysteresis in the capacitance revealed by a shift during the return sweep. The inner surface encircled in the hysteresis curve can be explained as electrons injection and electron trapping [15]. Note that the surface enclosed is an electrical charge: capacitance (in farads) multiplied by a voltage (in volts).

In [11] (page 129), the author has shown that $C_G(V)$ hysteresis measurement can be coupled to gate leakage current. We realize two different tests side by side with different gate voltages: 4V and 5V. The hypothesis is that the devices will age differently. Knowing that gate traps could be responsible of V_{TH} shift and gate leakage current [7], if we report a similar degradation in this parameters we can validate that the traps responsible of this phenomenon are also responsible of the evolution of $C_G(V)$ hysteresis curves.

4. Results and analysis

Figure 7 recapitulates the threshold voltage V_{TH} shift throughout the power-cycling steps (S0 –non-stressed device–, S1, S2, S3). Note that DUT4 and DUT5 broke down after stress S2 (see figure 7 and figure 8). V_{TH} is extracted from $I_D(V_{GS})$ curves traced with the HP4142B.

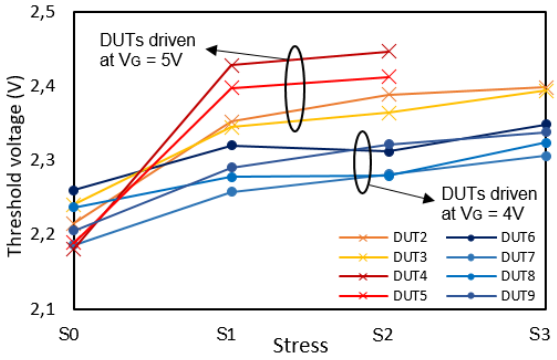


Fig. 7. Threshold voltage evolution throughout the test.

Figure 8 summarizes the evolution of the gate leakage current I_G during the power-cycling steps. Note that the degradation of the devices under test aged at V_G=5 V is major that those at V_G=4 V.

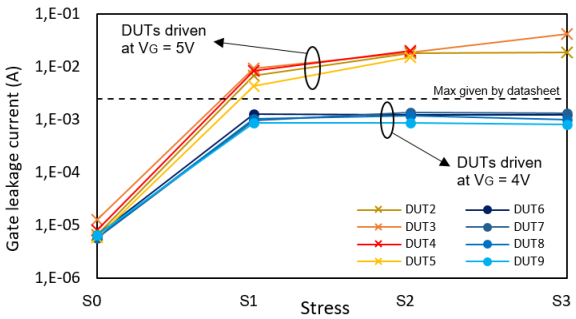


Fig. 8. Gate leakage current evolution throughout the test.

In figure 9 we observe the evolution of the $C_G(V)$ hysteresis curves in power GaN HEMTs driven at 4 V in the gate (V_G = 4 V); and in figure 10 the devices are driven at 5 V in the gate (V_G = 5 V)

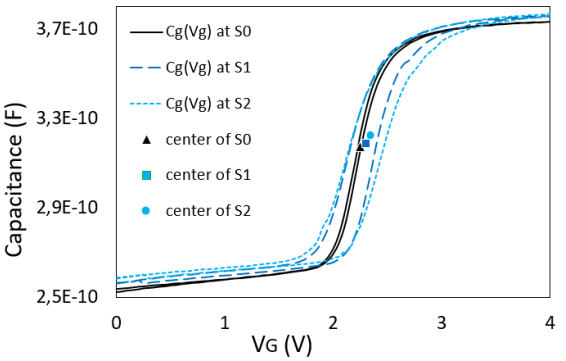


Fig. 9. $C_G(V)$ hysteresis curve evolution for the devices aged at V_G=4V

Note that in figure 10 we can observe a higher hysteresis surface enclosed in figure 9.

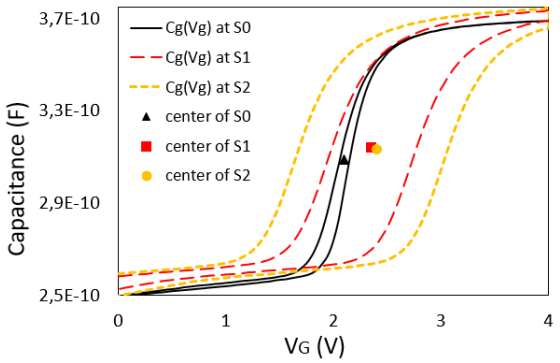


Fig. 10. $C_G(V)$ hysteresis curve evolution for the devices aged at V_G=5V

In figure 11 we can observe the hysteresis surface in coulombs enclosed between the up and down sweeps for the devices aged at V_G=4V and V_G=5V. It is calculated by integrating the $C_G(V)$ curves. Note that the unit is an electrical charge in coulombs: capacitance (F) multiplied by a voltage (V)

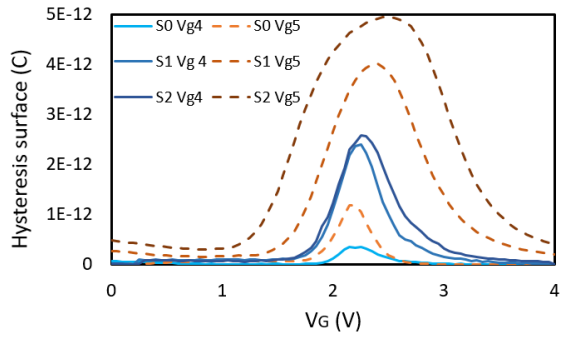


Fig. 11. Hysteresis curve evolution for the devices aged at V_G=4V (blue) and at V_G=5V (dashed brown)

In figure 12 we can observe center of the hysteresis surface versus the threshold voltage in order to evaluate the correlation between these two parameters.

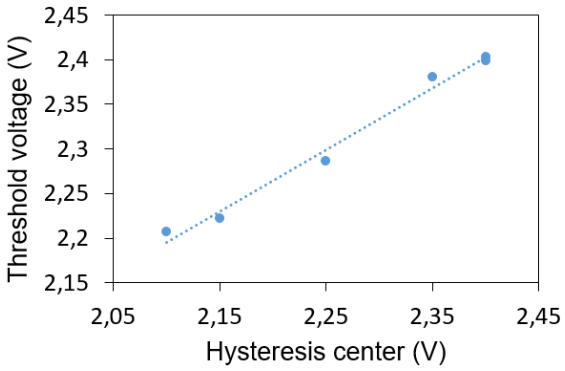


Fig. 12. Threshold voltage versus hysteresis surface center

5. Conclusion and future work

We have presented a power-cycling test bench dedicated to study the degradation of power-GaN devices. When designing the power-cycling stress parameters, we had to avoid the thermomechanical effects that have been presented in other works studying these devices under power-cycling [6]. Furthermore, we took into account the GaN-specific gate requirements using pGaN compatible drivers.

We carried out a set of tests in order to evaluate the relation between trapping effects in the gate region, the threshold voltage V_{TH} and gate leakage current I_G in power-cycling tests with different gate voltage V_G during the aging.

The $C_G(V)$ evolution curves show that the hysteresis capacitance measurement is a good indicator to study the degradation of power-GaN-HEMTs.

We have demonstrated a correlation between the hysteresis evolution and the threshold voltage shift (see fig 12). We suggest that the electric charge trapped in the gate region creates a local electric field that results in a virtual gate. In order to create the channel, we need to compensate this trapped negative charge increasing the gate threshold voltage V_{GSTH}, causing V_{TH} shift.

Further work will be forthcoming with new power-cycling tests studying the relation between the hysteresis surface in the $C_G(V)$ curve and Dynamic On-Resistance measurements. This test will allow us to prove if the traps measured in $C_G(V)$ hysteresis curves are responsible for Dynamic On-Resistance.

Acknowledgements

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