Transmission Line Approach for the PCB Gate Interconnection Design in GaN-Based High-Frequency Power Converters

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Transmission-Line Approach for the Gate PCB-trace Design in GaN-Based High-Frequency Power Converters

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Abstract

GaN-HEMTs allow power converters to achieve high switching frequencies. Therefore, novel design challenges arise in both power and frequency. In this context, this work aims to contribute with the integration of design concepts inspired both from power electronics and radio-frequency methods by using transmission-line approach. The developed study presented here focuses on the gate signal. Nevertheless, this methodology can be extended to any other power converter signals. The explored methodology associates coplanar transmission lines with the IPC9592B PCB design standard for the design of the gate PCB-trace layout. Experimentally, a Vector Network Analyzer verifies the transmission line parameters of the designed gate layout . Additionally, the gate signals are compared for different power levels in a high-frequency boost converter. Study results provide insights about the transmission line methodology for the development of high-frequency power converters based on GaN-HEMT.

1 Introduction

Progress in Gallium Nitride - High Electron Mobility Transistors (GaN-HEMT) has enabled switching frequency of power converters up to megahertz-level [1]. Therefore , promising perspectives forecast a new generation of power converters with significant increase of power density and switching frequency [2]. However, high-frequency power converters should overcome challenging design constraints in both power and frequency domains[1]. Given this perspective, we aim to contribute with an innovative design approach using transmission line concepts for the development of high-frequency power converters. The goal of this approach is to complement the usual power-electronics methodologies with a radio-frequency concepts to facilitate the design of high-frequency power converters based on wide-band-gap devices.

Conventionally, reported works about the Printed Circuit Board (PCB) impact on the GaN-HEMT performance are mainly focused on the parasitic inductance of the power and driver loops [3]. Studies based on the parasitic inductance have significantly contributed to understand PCB phenomena around the GaN-HEMT devices. However, approaches based only on the parasitic inductance could be limited in scope to describe some PCB phenomena that arise at megahertz-level. Indeed, some authors argue that high-frequency phenomena in power converters need additional analysis tools [4].

This work describes the impact of PCB traces on high-frequency power converters using usual transmission-line parameters like characteristic impedance Z_0 and propagation time T_d . These two parameters depend on the PCB-traces geometry and the PCB-substrate features [5]. Therefore, the integration of these parameters in a preliminary design and simulation stage can provide valuable information for further PCB manufacturing. A case study is developed through the gate layout design of a high-frequency boost converter based on GaN-HEMT. A demonstrator experimentally validates the proposed design methodology.

This paper is organized as follows. Section two describes the PCB trace modeling using transmission lines. Section three presents the integration of the coplanar transmission lines

and the IPC9592B standard for the gate layout design. Finally, section four describes the experimental setup and results to validate the proposed approach.

2 PCB trace modeling using transmission lines

The transmission line modeling considers the PCB trace as a means of propagation for electromagnetic waves (see Fig.1). As shown in Fig.2, the PCB geometry and substrate material are the main aspects to consider for calculating the characteristic impedance Z_0 and the propagation time T_d. The characteristic impedance Z_0 represents the own opposition to the alternative current flow given by the relation voltage / current on the PCB trace. The propagation time T_d is the time required for a signal to travel through a PCB trace of a given length ℓ.

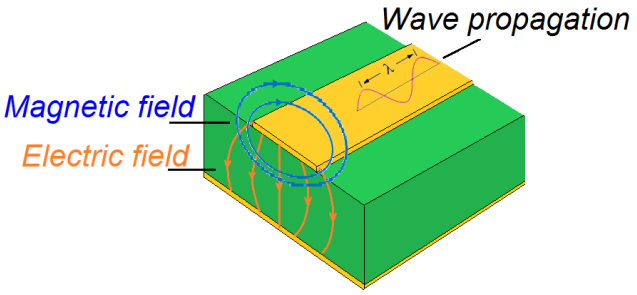
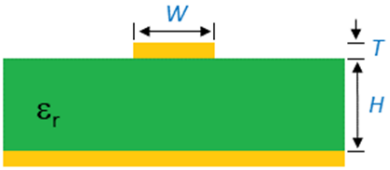


Fig. 1: Transmission line model of a PCB trace.

In Fig.3, a designed boost converter of 400V/400W/30MHz considers the Spice model of a PCB trace in the gate-signal path. The PCB characteristics are set to typical values of $T = 35\mu m$, $H = 1.6mm$, $\epsilon_r = 4.2$. The parameters W and ℓ are adjusted to get several values of Z_0 with T_d constant(i.e. equal track length). Fig.4 shows the gate voltage signals for several values of Z_0 while keeping T_d unchanged. Simulation results of Fig.4 show that lower Z_0 improves the signal quality and decrease the risk of hazard oscillations. Next section describes the proposed methodology for designing the PCB gate trace.



$$L_0(nH/cm) = 2\ \ln\left(\frac{5.98H}{0.8W+T}\right)$$

$$C_0(pF/cm) = \frac{0.26\,(\varepsilon_r+1.41)}{\ln\left(\frac{5.98H}{0.8W+T}\right)}\varepsilon_0$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad T_d = \ell\sqrt{L_0C_0}$$

Fig. 2: Characteristic impedance Z_0 and propagation time T_d from PCB parameters.

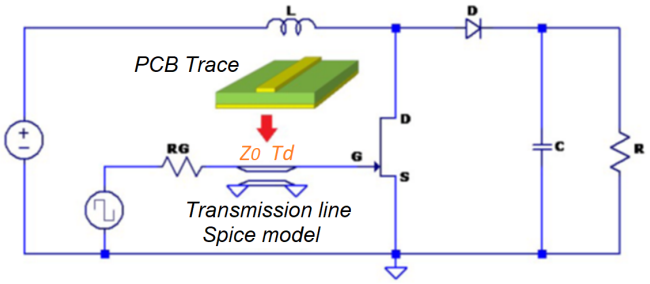


Fig. 3: High-frequency boost converter with transmission line model.

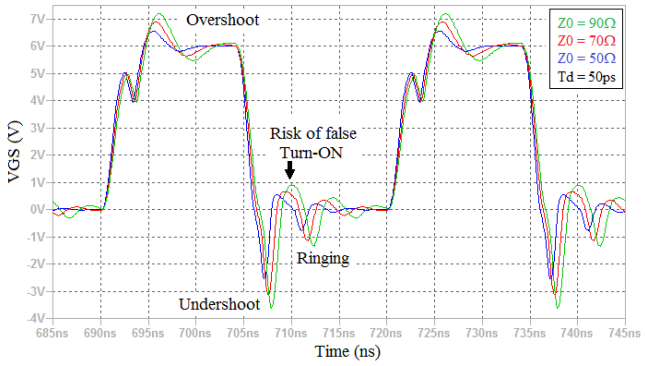


Fig. 4: Simulations results of boost converter with transmission line model in the gate path.

3 Coplanar transmission lines and IPC9592B standard for gate layout design

As describe in previous section, lower values of Z_0 improves the gate signal quality. However, Fig.5 shows that achieving lower Z_0 values requires increasing the PCB trace width. This condition

is highly restrictive given the current size of high-frequency gate drivers which have pitch at micrometer-level (see example in Fig.6).

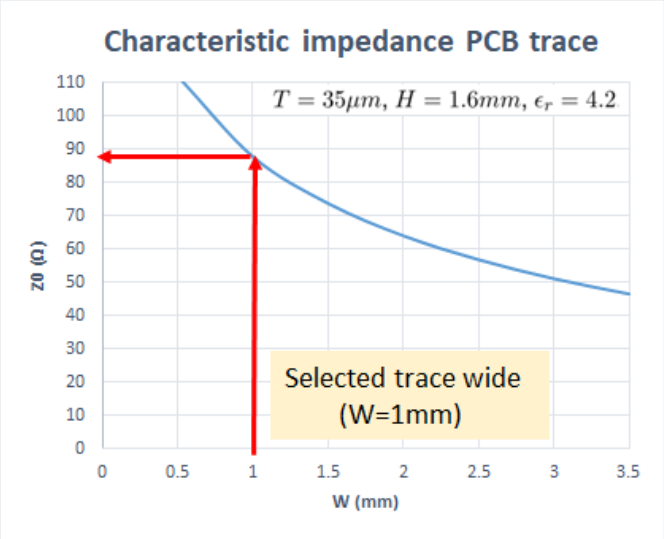


Fig. 5: Characteristic impedance of a PCB trace in terms of the trace width.

Therefore, a coplanar transmission line, depicted in Fig.7, seems more suitable to overcome this space constrain. This transmission line topology provides an electromagnetic field distribution that allows to lower the characteristic impedance Z_0 by decreasing the space between the signal trace and the coplanar ground plane (S in Fig.8).

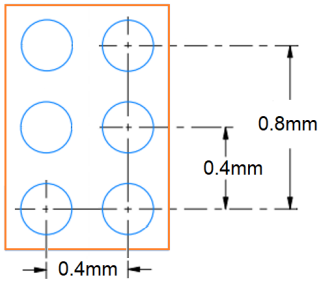


Fig. 6: Example of gate-driver-package pitch for GaN devices at the Mhz level.

Fig.9 describes the variation of the characteristic impedance given the clearance decreasing between the trace and the ground plane. The gate layout design considers a PCB trace width $W = 1mm$. This trace width provides a characteristic impedance $Z_0 \approx 90\Omega$. To decrease this characteristic impedance, the IPC9592B PCB design standard is selected as minimum spacing parameter for the trace distance S. As shown

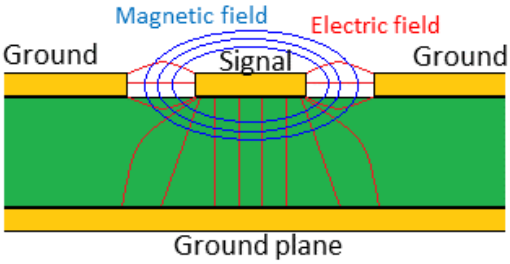


Fig. 7: Magnetic and electric fields in coplanar transmission line.

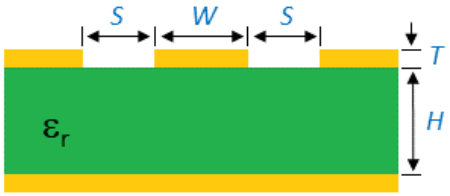


Fig. 8: Parameters of coplanar transmission line.

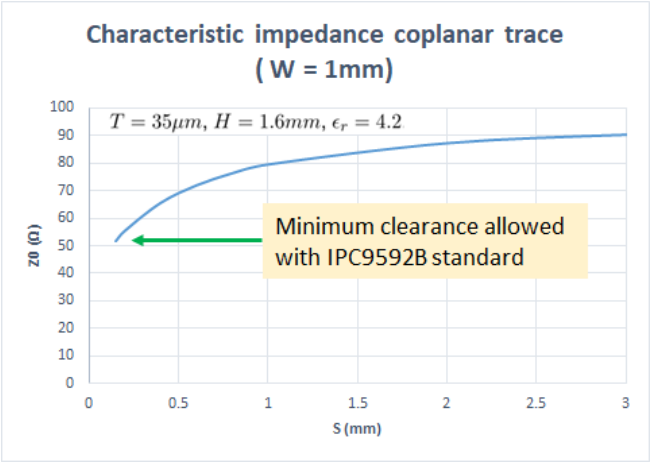


Fig. 9: Characteristic impedance of coplanar transmission line.

in Fig.10, this standard recommends a minimum spacing of 0.13mm for withstanding voltage below 15V. Therefore, a characteristic impedance $Z_0 \approx 50\Omega$ can be achieved as shown in Fig.9. Next section describes the experimental setup implemented to validate the proposed approach.

4 Experimental results

A GaN-based boost converter of 400V/400W/30MHz is implemented with a high-frequency gate driver and PCB gate layout design following the proposed approach. Details of implemented PCB around the gate driver are shown in Fig.11.

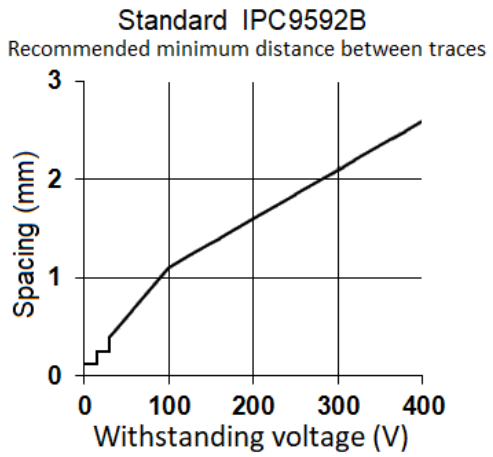


Fig. 10: Minimum trace spacing according to IPC9592B

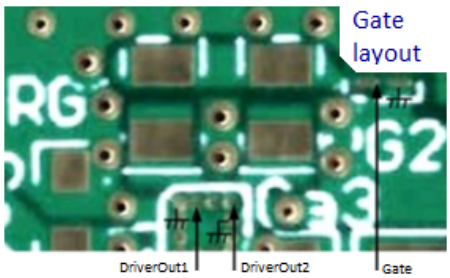


Fig. 11: PCB layout around the gate driver.

Fig.12 illustrates the experimental setup based on the Vector Network Analyzer Keysight Technologies N5247A to measure and validate the designed characteristic impedance Z_0 around the PCB gate layout. This PCB characterization employs the S-parameters extraction to evaluate the transmission line parameters in a wide range of frequencies.

Experimental results depicted in Fig.13 show that the characteristic impedance of the output driver and the GaN gate input are close to the expected value of $Z_0 \approx 50\Omega$. Therefore, these results validate the proposed approach to design coplanar transmission lines in the PCB gate interconnections to achieve a given characteristic impedance.

Considering the power converter behavior, Fig.14 shows that the gate signal has a suitable performance in relative low voltage and power (90V/20W/30MHz). However, the increase of voltage and power requirements (400V/400W/30MHz) impacts drastically the measured signal quality as shown in Fig.15. Therefore, other phenomena such as electromagnetic induction (radiated emissions

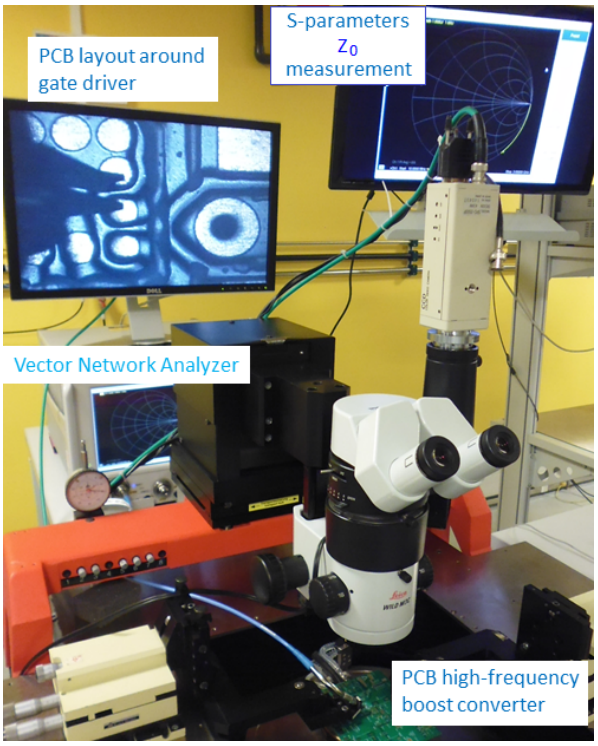


Fig. 12: Experimental setup based of a Vector Network Analyzer to measure Z_0 of PCB gate trace.

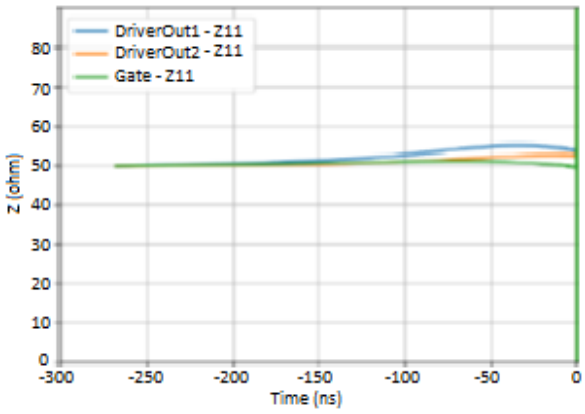


Fig. 13: Characteristic impedance measurement of PCB gate layout. Negative time corresponds to reflected measure signals.

at high dV/dt) and its impact on the measurement setup should be considered to better understand this distortion at high level and complement the proposed design methodology.

5 Conclusion

This paper described the PCB gate-layout design for GaN-based high-frequency power converters using a complementary approach based on transmission

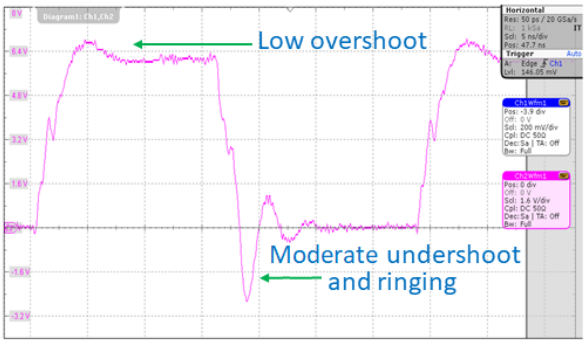


Fig. 14: Gate signal at low output power. Vert_scale:1.6V/div, Horiz_scale: 5ns/div

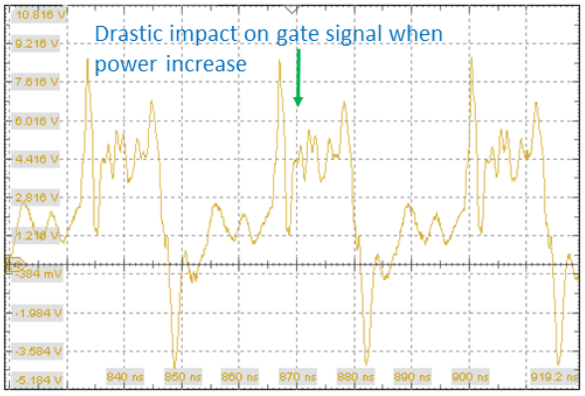


Fig. 15: Gate signal at high output power. Vert_scale:1.6V/div, Horiz_scale: 10ns/div

lines. Simulation and analysis results was employed for the PCB manufacturing of a 400V/400W/30Mhz boost demonstrator. Experimental results showed that the expected characteristic impedance was achieved using coplanar transmission lines and the IPC9592B standard. The measured gate signal quality at relative low voltage and power was suitable. However, the voltage and power increase impacted drastically the signal behavior. Future works will consider aspects such as the electromagnetic analysis to avoid hazard disturbances on the gate signal.

Acknowledgements

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References

[1] A. Hariya, K. Matsuura, H. Yanagi, S. Tomioka, Y. Ishizuka, and T. Ninomiya, “Five-Megahertz PWM-Controlled Current-Mode Resonant DC-DC Step-Down Converter Using GaN-HEMTs”, *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3263–3272, 2015. DOI: 10.1109/TIA.2015.2391439.

[2] H. A. et al, “The 2018 GaN power electronics roadmap”, *Journal of Physics D: Applied Physics*, vol. 51, 2018.

[3] D. Reusch and J. Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter”, *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2008–2015, 2014. DOI: 10 . 1109 / TPEL . 2013 . 2266103.

[4] J. Kashiwagi, A. Yamaguchi, Y. Moriyama, and K. Nakahara, “Hysteretic Control Embedded Boost Converter Operating at 25-MHz Switching”, *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 1, pp. 101–105, 2019. DOI: 10.1109/TCSII.2018.2834571.

[5] *Standard IPC-2141A, Controlled Impedance Circuit Boards and High Speed Logic Design*, Institute for Interconnection and Packaging Electronic Circuits, 2004, Institute for Interconnection and Packaging Electronic Circuits.