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# Frequency Based Method Investigation to Extract an ESD Protection Dynamic SPICE Model from TLP Measurements

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**Abstract**—In order to ensure reliability of systems early in the design phase, it is becoming crucial to have models able to predict the behavior of systems exposed to ElectroStatic Discharge (ESD). This is an increasing necessity since the number of embedded electronic products is growing and since they are employed in applications where people’s safety is a requirement, such as automotive and aeronautic applications. Until now, quasi-static models of protection devices have succeeded in providing fairly good results in failure predictions (mainly hard failures). Today, the increased frequency range of such devices requires dynamic models able to reproduce their transient behavior. In this paper, we investigate if conventional methods for modeling linear devices, generally used in the frequency domain, could be used to obtain an equivalent frequency model for ESD protection devices, which exhibit non-linear behavior. A methodology to extract an ESD protection SPICE model from Transmission Line Pulse (TLP) measurements to address transient and frequency simulation is proposed and detailed. We demonstrate that, in well-defined conditions, such frequency models can give accurate results to predict overshoots related to protection device triggering delays. Validation of the models is performed under TLP and Human Metal Model (HMM) conditions on three off-the-shelf devices.

**Index Terms**— System ESD modeling, ESD reliability, frequency modeling.

## I. INTRODUCTION

The reduced dimensions available through shrinking technology have increased the capabilities of devices and resulted in the development of so-called “embedded” systems. The devices embedded in these systems are weak and exposed to harsh environmental conditions such as ElectroStatic Discharges (ESD). They constitute powerful sources of interference able to destroy electronic devices. On-chip protection structures are commonly used to ensure that devices fulfill HBM [1], MM [2], or CDM [3] standards. However, nowadays, such devices have to survive much more severe stresses as defined in the IEC 61000-4-2 standard [4] for system level applications. In some fields, this is even more crucial since electronic systems have to ensure people’s safety,

as in transportation applications. As a result, the demand for robustness against system-level ESD, as defined by the IEC61000-4-2 standard, is increasingly shifted to the component level itself [5][6][7]. One of the key issues is the ability to predict, during the design phase, if the system will operate well in any test conditions using models.

Predicting system level reliability against ESD stresses remains a very challenging topic because safety constraints require protecting systems from hard and soft failures. Being able to do so could bring further improvements to existing protection approaches [8], while reducing costs. In most cases, the lack of available transient integrated circuit (IC) models makes this task difficult. Stress waveforms at the device inputs have to be predicted to evaluate the failure risk. For digital circuits, IBIS files [9], dedicated to Signal Integrity (SI) simulations, could provide the beginning of an answer but are not entirely suitable [10] [11]. Dedicated ESD protection models need to be added to SI models to consider high power transient events.

Such models have now been studied for around ten years and behavioral descriptions were first proposed in [10][12]. The models are extracted from Transmission Line Pulse (TLP) quasi-static measurements [13][14][15]. A piecewise linear I(V) curve is built and used in simulation. Different model descriptions can be generated, as described in the recent standards [16][17]. These models are able to reproduce the system behavior in most cases, as presented in papers [18][19][20] and also [21],[22],[23],[24],[25],[26]. All these publications show how behavioral models proposed by [10] can give good results to predict hard failures (destructions) of the ICs but also (in some cases) functional failures. In most of these papers, the failure level is determined through the time to failure as described by Wunch & Bell [27], [28]. Some compact modeling approaches to predict thermal effects have been proposed in [29],[30],[31],[32] where equivalent Spice models are used to reproduce thermal effects. The proposed models of these articles are able to represent the transient behavior of self-heating. This is particularly useful for the prediction of destruction for long pulse durations. In a different way, hard failure can be related to oxide breakdown when an overvoltage

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appears. Some models to take into account these transient stresses have been proposed in [31],[32],[34]. When failure is not related to a thermal effect and is due to a voltage overshoot, methods based on a quasi-static measurement show some limits. The protection turn-on delay may not be reproduced accurately and, thus, the over-voltage is not correctly determined in simulation, thereby inducing prediction errors [35],[36]. Some works have proposed SPICE modeling approaches to build models that take into account such events, such as [33],[35],[36]. However, these models are not so easy to build because the parameters enabling transient behavior to be considered could be difficult to fit. The proposed models are able to predict overshoot in the dynamic regime. The model proposed in this article is based on observation of the time responses of protection devices from article [33]. When the protection devices are exposed to a very fast rise time, the behavior response looks like a 2<sup>nd</sup> order filter, such as the one reported in Fig.1, where  $Z_{dyn}$  represents the turn-on delay constraints. If the turn-on of the switch could be neglected, then this 2<sup>nd</sup> order filter could be estimated using frequency propagation wave methods such as S Matrix [38]. After detailing the impact of the triggering conditions, frequency measurement methods will be used to get an equivalent frequency model of protection devices using a TLP generator. This model does not provide the failure level, but it makes it possible to simulate the transient response of the device under ESD stress condition using time simulators such as SPICE, or frequency simulators. (NdT: The end of this sentence is not clear. Is "...OR frequency simulators" meant?) Failure criteria could be added as described in paper [37].

The present document is set out as follows: following this introduction, the second section discusses the consideration of using frequency parameters to reproduce ESD protection behavior, even if such devices are non-linear. The third section presents the theory of reflectometry in the frequency and time domain and describes the existing link between both domains that will allow us to get frequency parameters from TLP measurements. An RLC example shows that frequency parameters could be obtained from TLP measurements. This section is completed by a discussion demonstrating how such a frequency approach could be used to address protection devices in well-defined conditions. The fourth section considers a real case of application by building frequency models of LIN devices and measurements and simulations are compared using TLP injection and GUN injection. The paper ends with some conclusions.

## II. BASIS OF THE PRESENT WORK

In this paper, the objective is to investigate a model considering the transient behavior of the protection mainly caused by on-chip structure triggering. This is becoming crucial as devices go to higher working frequencies.

During a previous study [33], it was demonstrated that ESD protection transient behavior could be represented by the non-linear IV quasi-static curve of the protection with an additional dynamic model based on an equivalent RLC network ( $L_{dyn}$ ,

$R_{dyn}$ ,  $C_p$ ). The equivalent electrical schematic of the protection device is shown in Fig. 1. The model device takes into account all the parasitic elements of the package, represented by its inductances ( $L_{pack}$  – on the input and ground pin), the equivalent quasi-static model of the protection (represented by  $E_p$  and  $R_{stat}$  –  $E_p$  representing the voltage while the protection is triggered at 0 amps, to get the I(V) characteristic) and a dynamic contribution  $Z_{dyn}$ .

$Z_{dyn}$  includes the equivalent capacitance of the protection ( $C_p$ ), a dynamic resistance ( $R_{dyn}$ ) and an inductance ( $L_{dyn}$ ). The switch (which represents the turn-on of the protection) is activated when the voltage through the protection ( $V_p$ ), measured across  $C_p$ , reaches the quasi-static triggering value of the protection. At the very beginning of the pulse, the inductance  $L_{dyn}$  acts as a high impedance (like an open circuit).  $R_{dyn}$  is a high impedance that is progressively shorted by  $L_{dyn}$  after a small delay corresponding to the turn-on delay of the protection. Then only the  $R_{stat}$  (a low impedance) is seen. The validation of such a model in real conditions is detailed in paper [33]. This model clearly shows that an RLC network can reproduce the behavior of an ESD protection.

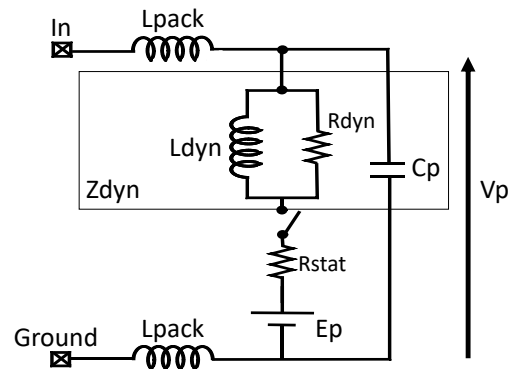


Fig. 1: Equivalent electrical schematic of the protection when it turns on.

This model is composed of two parts. A quasi-static part obtained with TLP measurements and a dynamic part with parameters obtained using VF-TLP measurements. As described in papers [33], [35], [36], the model is computed from the  $V(t)$  and  $I(t)$  curves during a TLP injection with a 300 ps rise time. Extracting such a model from measurements directly in the time domain is not an easy task since it requires a high frequency bandwidth voltage and current probes (>1 GHz) which withstand high power injection (several kilovolts and some tens of Amps). This extraction process may be easier in the frequency domain due to the large bandwidth offered by this type of measurement equipment. However, until now, there has been no set-up that allows a protection to be triggered with high voltage injection and, at the same time, allows the possibility of making voltage and current frequency measurements.

This paper aims to evaluate if an IC internal ESD protection could be considered as a linear device. The RLC network provided in [33] is able to reproduce a transition from high to low impedance in a nanosecond range. The remaining question is to define under what conditions, which also means that: could the switch be neglected? If the assumption is borne out,

an equivalent linear model can be extracted from frequency-domain methods to model the dynamic behavior of the protection. This assumption will be discussed and demonstrated in section III.

In spite of a loss of accuracy, such an approach will simplify the modeling process of ESD protection devices.

This analysis will lead to the proposal of an equivalent "S-parameter" model that could be obtained using TLP measurement systems. The approximations allowing us to consider the non-linear behavior of the protection device as a linear network are presented and discussed. The mathematical approach to obtain such "[S] matrix" from VF-TLP measurements is described. It is validated first on a basic RLC circuit and then on three protection devices integrated in three commercial circuits (LIN (Local Interconnect Network) transceivers).

The SPICE models extracted from this "[S] parameters" approximation are introduced into simulations to compare system level measurement scenarios under TLP and HMM (Human Metal Model) [43] conditions.

### III. FROM TLP MEASUREMENT TO FREQUENCY MODEL

#### A. From TLP measurement to S11 parameter – Theory

The S frequency parameters are mostly extracted using a Vector Network Analyzer (VNA). It applies a small sine wave signal at each port of the Device Under Test (DUT) and according to the device's behavior it creates a matrix of  $S_{jk}$  parameters. The S(f) matrix is directly related to the impedance of the DUT. For linear devices, the reflection coefficient at port 1 of the DUT is  $S_{11}$ , obtained by the formula:

$$S_{11}(f) = \frac{b_1(f)}{a_1(f)} \quad (1)$$

Where  $a_1$  is the forward wave and  $b_1$  the reflected wave for one injection frequency. To get the full [S] matrix, the operation is repeated for each frequency.

VNA is often used to get the DUT input impedance for small signal analysis. ESD protection devices are non-linear elements, and VNA cannot be used for such components because the non-linearities introduce harmonics. Moreover, the VNA output power is not sufficient to reach the triggering voltage or current of most ESD protections. It is not able to maintain sufficient power on an impedance close to zero when the ESD device turns on. Even if it could be possible, applying a powerful continuous sine wave would damage the DUT.

Transmission Line Pulse coupled to the Time Domain Reflection (TLP-TDR) method is preferred. The TLP delivers a rectangular pulse of 1 ns rise time (or less) and 100 ns duration, which is enough to characterize a protection device without damaging it. This pulse can reach dozens of Amps, which is enough to trigger any ESD protection device. As shown in Fig. 2, the set-up is quite similar to the VNA

measurement set-up, except the measurement is made in the time domain. The 500  $\Omega$  resistor and the 50  $\Omega$  transmission line impedance form a voltage divider to pick a part of the voltage across the DUT.

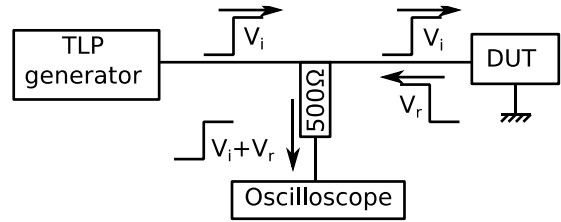


Fig. 2: Set-up for a TLP measurement of ESD protection

For a linear DUT, the power transmitted to the DUT is linked to the forward voltage signal ( $V_i$ ) and to the reflected signal from the DUT ( $V_r$ ), by the following relationship:

$$VDUT(t) = V_i(t) + V_r(t) \quad (2)$$

The DUT reflection coefficient using this measurement method is given by:

$$\Gamma(t) = \frac{V_r(t)}{V_i(t)} \quad (3)$$

This relationship is similar to equation (1) except  $\Gamma$  is in the time domain. It also works in the frequency domain by using a Fast Fourier Transform (FFT) of the reflected and incident voltages, assuming the DUT is linear. This means that TLP combined with reflectometry methods in the time domain can provide the reflection coefficient  $S_{11}$  as mentioned in (4).

$$S_{11}(f_1 \dots f_n) = \frac{b_1(f_1 \dots f_n)}{a_1(f_1 \dots f_n)} = \frac{V_r(f_1 \dots f_n)}{V_i(f_1 \dots f_n)} = \Gamma(f_1 \dots f_n) \quad (4)$$

The computing method has been coded in a Matlab script, the principle of which is summarized in Fig. 3.

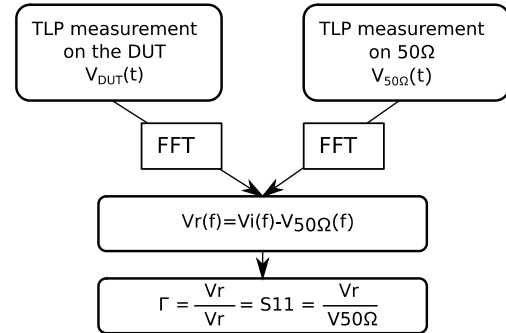


Fig. 3: TLP Diagram to extract S11 parameter from TLP measurement

The first voltage measured with TLP is  $V_{50\Omega}$ , obtained by calibration on a 50  $\Omega$  resistor ( $V_{50\Omega}(t)$ ), and the second voltage is the voltage across the DUT ( $V_{DUT}(t)$ ). An FFT is applied to both of them and they are introduced into eq (2) to obtain the reflected pulse in the frequency domain. The computation finally gives us the reflected coefficient,  $\Gamma$ , which is also the  $S_{11}$  parameter in the frequency domain. Using such a computational method, only a voltage probe is needed, which usually has a larger bandwidth than current probes - referring to the method proposed in [33].

In the applications presented in the current paper, the DUT is soldered on a dedicated board with a 50  $\Omega$  access line

through SMA connectors. The voltage probe is made of a high frequency  $500\ \Omega$  resistor placed on the PCB closed (*NdT*: “closed to” or “close to”?) to the component and connected to a 12 GHz oscilloscope. The voltage probe has an equivalent bandwidth of 6 GHz.

With such a measurement set-up, high power injection can be reached using TLP generators to obtain the equivalent  $S_{11}$  parameter (up to 1 kV). The TLP rise time will define the upper frequency limit of the computed  $S_{11}$ . The smaller the rise time, the higher the frequency bandwidth of the pulse.

To validate the mathematical approach, a transient simulation with ADS software (ADS 2017) is first performed on the RLC circuit, shown in Fig. 4. This passive network was proposed in [33] for the linear part (without the triggering condition) of an ESD protection. A TLP pulse of 800 V amplitude, 100 ns duration and 1 ns rise time is applied and the script shown in Fig.3 is executed.

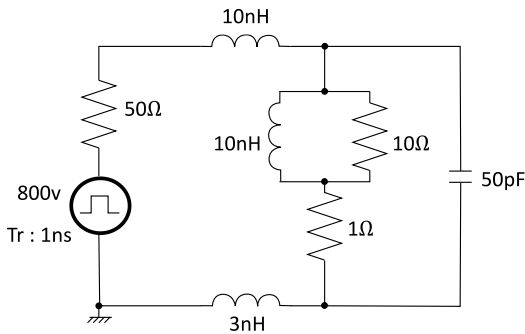


Fig. 4: TLP simulation set-up used to validate the mathematical approach

The result designated “ $S_{11}$  from TLP” is compared to the S-parameter simulated with ADS directly on the RLC network. As shown in Fig. 5, the  $S_{11}$  obtained from the time domain simulation using TLP pulse injection and the Matlab Script fits perfectly with the equivalent  $S_{11}$  matrix of the RLC provided by ADS up to 1GHz. At higher frequency, the impact of the TLP rise time is clearly visible. As the spectrum of TLP pulse exhibits zeroes at multiple frequencies of the inverse of the rise time, the accuracy of the operation performed in (4) is degraded at these frequencies. To increase the frequency validity range, a short rise time could be preferred to move the computing noise of the division  $V_r/V_{50\Omega}$  to higher frequencies. Another way could be to have a more robust computing algorithm to avoid the division by zero that introduces high magnitudes.

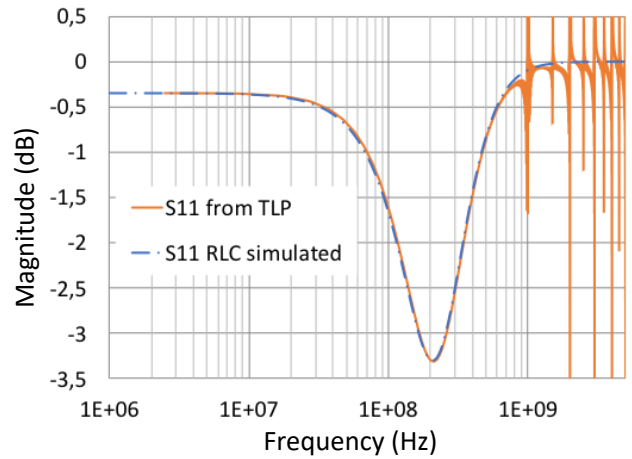


Fig. 5: Comparison of the magnitude for both  $S_{11}$  from TLP computation and from S-parameter simulation. (*NdT*: if possible, replace decimal commas by decimal points here and in other figures)

A SPICE model from the  $S_{11}$  parameter can be built using an automatic tool designated “broadband SPICE model generator” in the ADS software (Fig 6).

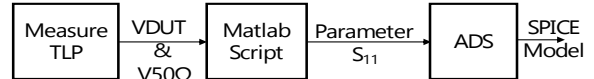


Fig. 6: Diagram of the methodologies used to extract a SPICE model from the TLP measurement.

The input is the  $S_{11}$  file extracted from Matlab (red curve) and the tool is able to provide a SPICE model (green curve) that fits the red curve depending on the user’s constraints (frequency min/max, tolerance, average, etc.). As shown in Fig. 7, the SPICE model fixes the mathematical errors introduced by the Matlab code in the high frequency region. The green and red curves are superimposed.

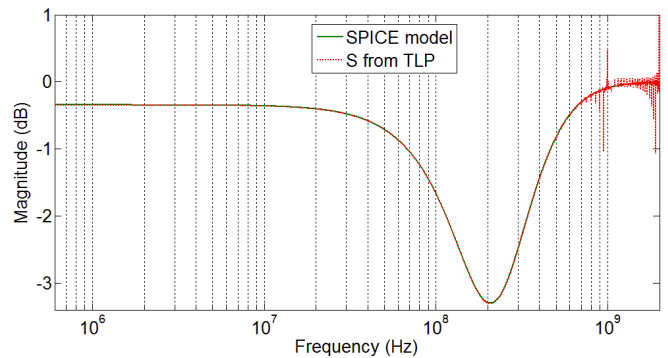


Fig. 7: Comparison of the magnitude for both  $S_{11}$  from TLP simulation (S from TLP) and from the broadband SPICE model generated (SPICE model).

The SPICE model generated is used in a transient simulation. TLP injections are simulated on the RLC network shown in Fig. 4 and on the broadband SPICE model. Both results are compared in Fig. 8. The TLP is set at 800 V with 1 ns rise time. Both simulation results match well, proving the validity of the approach in the case of a purely linear device.

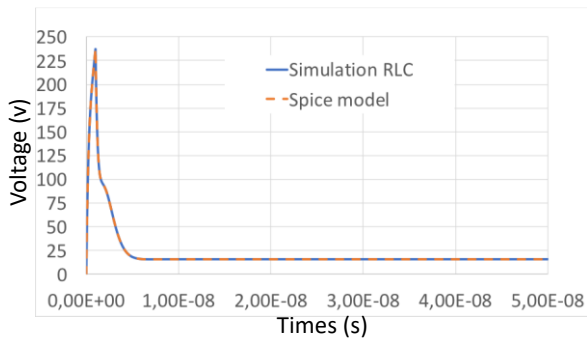


Fig. 8: Comparison of the voltage for the TLP simulation on the RLC device (Simulation RLC) and the TLP simulation on the SPICE model generated (Spice model)

### B. Measurement validation on RLC network:

In this section, the methodology to extract an S-parameter from TLP measurements is validated on the RLC circuit described in Fig. 9.b. Each step is reproduced and the measurement results are compared with the simulation. The TLP is set at 400 V and 1 ns for the rise time.

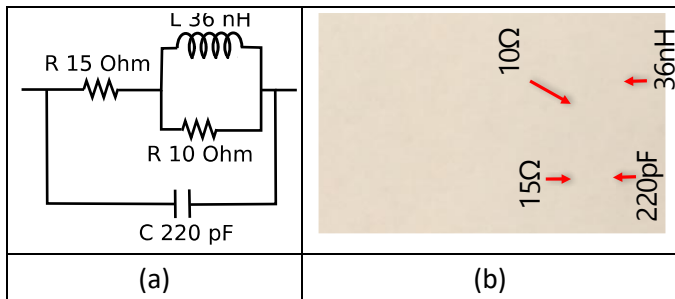


Fig. 9: (a) Schematic of the tested RLC circuit. (b) RLC components mounted on the test board.

Voltage measurements made on the RLC circuit and on a 50  $\Omega$  load are reported in Fig. 10, (a) and (b) respectively. A peak on the rising edge and another one on the falling edge are observed on the voltage measurement of the RLC structure (V DUT). This is mainly due to the delay between the forward and reflected waveforms related to the short transmission line between the measurement probe and the RLC circuit (for a 50  $\Omega$  configuration, the load is placed at the probe). In simulation, an ideal set-up is used, meaning that the delay introduced by a small line between the voltage probe and the RCL network is not considered. Both simulations and measurements are quite similar.

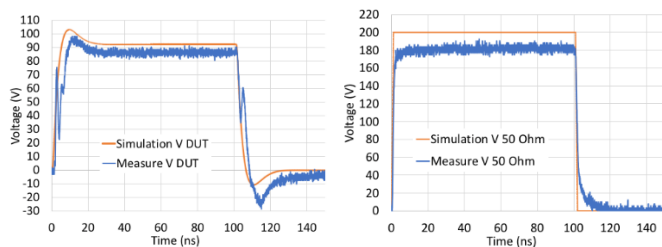


Fig. 10: Left side, comparison between measurement and simulation of the RLC circuit under 400V injection TLP. Right side, comparison between measurement and simulation of the 50 Ohm resistor under 400 V injection TLP.

These transient measurement curves are used in our Matlab Script to extract the S-parameters. Fig. 11 shows the parameters for measurements and simulation together with standard  $S_{11}$  ( $NdT$ : both  $S_{11}$  and  $S_{11}$  appear in the script. If the same thing, only one should be used) parameters extracted by a VNA, and also  $S_{11}$  parameters simulated in the ADS software. It can be noticed that the S-parameters obtained from simulation are both (VNA and TLP simulated) exactly the same. The S-parameters obtained from measurements with VNA are quite similar and show a small attenuation at high frequency (above 100 MHz) due to the impact of the parasitic elements of all the interconnects, which are ignored in simulation. The S-parameters extracted from the TLP measurement are close to the simulated one with 1 dB attenuation. Up to 300 MHz, VNA measurements and TLP give similar results confirming the use of the TLP TDR system to obtain the dipole's frequency parameter.

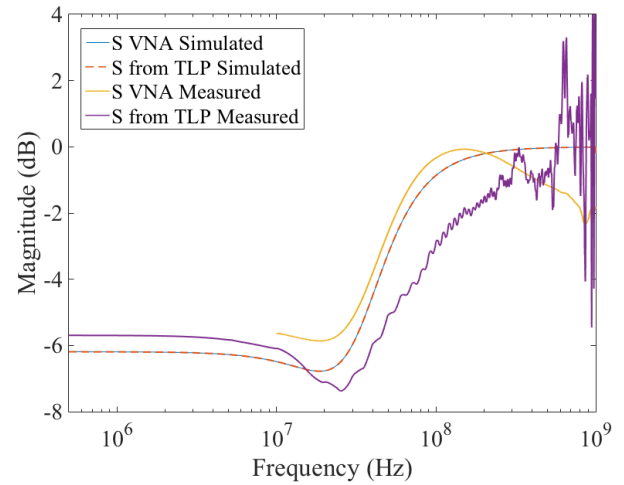


Fig. 11: Simulation and measurement comparison of the S-parameters extracted from VNA and using our methodology from TLP curves.

A SPICE model is generated from the S-parameter extracted by TLP measurements. Simulation is performed considering all the measurement set-ups. Fig. 12 compares the transient voltage measured across the RLC circuit and the voltage simulated by the SPICE model under 400 V TLP injection.

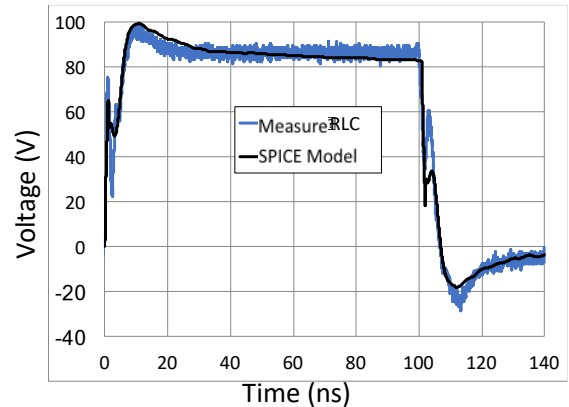


Fig. 12: Comparison between the voltage measured and simulation of the extracted SPICE model under 400 V TLP injection.

The simulation with the SPICE model fits well with the measurement. The first peak here reports the incident pulse due to the real distance between the voltage probe and the DUT. Following these results, the methodology used to build a model of a linear component from the TLP response could be validated. In the next section, we will discuss the possibility of using a similar approach to model a non-linear element.

### C. Application to a non-linear circuit.

We decided to apply this method to an ESD protection used in the LIN transceiver studied in [33]. In a linear circuit, S-parameters are the ratio between the amplitudes of the scattered power wave and the forward power wave at one frequency. The S-parameters remain the same whatever the input power because of its linear behavior. For a non-linear circuit, these rules are not true. Applying a sine wave to a non-linear component input generates multiple harmonics on the output. Moreover, the amplitude of the fundamental frequency and its harmonics depend on the input power. In this case S-parameters cannot be used to model the component precisely and an alternative description such as X-parameters [35] should be used. They are commonly used to characterize high frequency components in small signals [39][40][41][42]. Unfortunately, X-parameter measurement systems cannot reach the triggering level of most ESD protections. Even if such measurement systems could reach high power capabilities, the time needed to sweep the frequency and obtain all the harmonics is too long to prevent the device's destruction. Regarding all these drawbacks, transient measurement systems such as TLP or VF-TLP are preferred. The TLP generator creates multiple harmonics (square pulse definition). Using a TLP generator combined with something like "S-parameters" computation should provide an approximation of the response of a protection device as long as its behavior is nearly linear. This last sentence is heavy with consequences and has to be taken into account with care.

Regarding previous works [33], the model obtained of the ESD protection of the studied LIN transceiver is reported in Fig 1. To determine if it may behave quasi-linearly or not, the main question is about the effect of the switch, which is the main contributor to non-linearity. During an ESD event, strong  $dv/dt$  up to several kilovolts per nano-second are observed and the triggering voltage can be reached so quickly that the non-linear effect of the triggering is masked by the equivalent passive components of the device. Based on the approximation that passive components of the model (Fig. 1) hide the effect of the switch, we could neglect it. In the following section, this will be demonstrated and the required validity conditions of this approximation will be defined. Simulation makes it possible to investigate how all the passive elements act, and what is the impact of the ESD event waveform on the switching effect.

In our model, the parasitic package inductance ( $L_{pack}$ ) and the internal capacitance of the component ( $C_p$ ) of Figure 1 define the passive device network (PDN) before triggering. Its frequency response is simulated according to the electrical

model shown in Fig.13. The main goal is to evaluate the bandwidth of this equivalent low-pass filter and then to determine the rise time upper limit. If the incoming pulse has a significant spectral content above the cut-off frequency of the package, the parasitic capacitance  $C_p$  shorts the switch. Thus, the device operates quasi-linearly above this frequency.

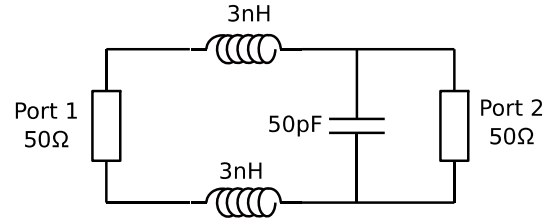


Fig. 13: Passive device network of the LIN component used in the dynamic model.

The S-parameter simulation results of this circuit are shown in Fig.14. The 3-dB cut-off frequency of the transmission parameter  $S_{21}$  (from Port 1 to Port 2), is obtained at  $F_{C-3dB} = 132.7MHz$ . For higher frequencies, the parasitic elements of the package attenuate the signal, which also means that a signal with a rise time with higher equivalent frequency than 132 MHz is stopped by the package. The maximum rise time to ensure quasi-linear conditions can be derived from the approximation formula.

$$(T_r = \frac{0.35}{Bandwidth}) \quad (5)$$

For the studied protection, the maximum rise time is equal to 2.63ns.

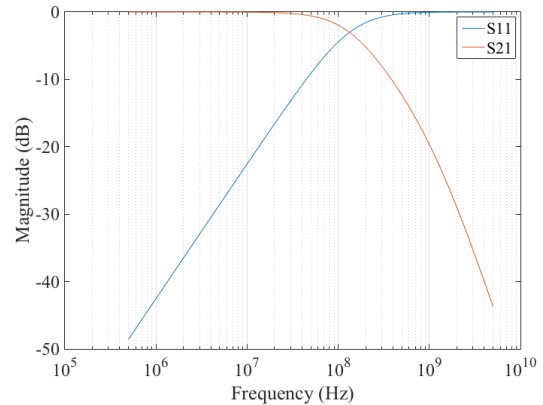


Fig. 14: S-parameters of the passive network of protection.

In order to validate this condition, the impact of the switch is simulated according to the rise time of the incoming pulse. The equivalent dynamic model of the LIN to GND protection extracted in [33] (Fig. 15) is used. In this model, a switch represents the ESD protection triggering when the voltage across the protection reaches 40 V. Details of the LIN device used as reference in this paper are given in paper [33]. A transient simulation is realized on two circuits, with and without the switch under 800 V TLP injection for two different rise times: 1ns and 5ns.

As shown in Fig.16, the impact of the switch is not significant when the rise time is set at 1ns. The spectral content of the pulse is significantly above the cut-off frequency of the protection package. This means that the linear part of the

model drives the behavior of the protection turn-on. In such conditions, the protection device behaves like a linear component, and our frequency methods can be considered. As was expected, with a rise time set at 5ns (Fig. 17), the impact of the ESD protection triggering could not be neglected. In this case, the component is strongly non-linear and linear frequency methods cannot be applied.

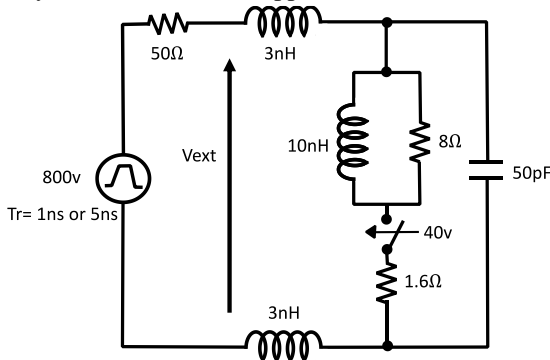


Fig. 15: Dynamic model with the switch that triggers at 40 V.

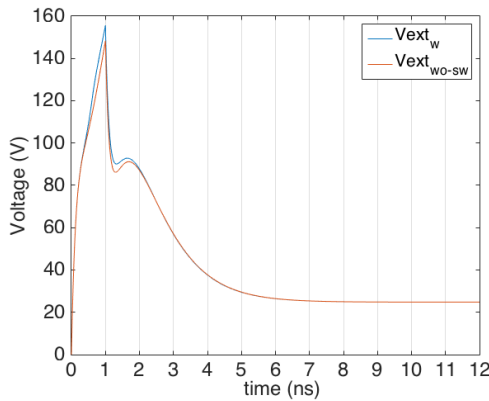


Fig. 16: Comparison of the voltage obtained for the simulated circuit with 40 V triggering switch ( $V_{extw}$ ) and the voltage without the switch ( $V_{extwo-sw}$ ) for 800 V TLP injection and 1ns rise time.

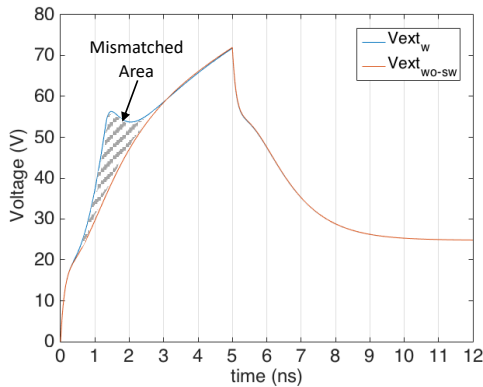


Fig. 17: Comparison of the voltage obtained for the simulated circuit with 40 V triggering switch ( $V_{extw}$ ) and the voltage without the switch ( $V_{extwo-sw}$ ) for 800 V TLP injection and 5ns rise time.

Non-linear effects could be hidden by the RLC equivalent filter of the PDN when the stress rise time is faster than the

filter cut-off frequency. According to equation (5), in our application, for rise times faster than 2.6ns the trigger is masked by the passive elements. In this particular condition, which is also the rise time of IEC 61000-4-2 stress, it is possible to extract a "S-parameters" equivalent circuit of the protection device considering that it behaves as a linear component. But the voltage amplitude of the stress has also to be considered, because the equivalent RLC network reproducing the behavior of the protection will change according to the stress power. This effect needs to be quantified depending on the protection structure. If the voltage is set just above the triggering voltage, even if the rise time is under the maximum  $T_r$  calculated according to equation (5), some non-linear effects may appear. This is mainly due to the fact that close to the triggering voltage, the semiconductors are not fully supplied to have a quick release. (*NdT: this phrase is not clear. Is this what is meant?*) The amplitude has to be set higher, arbitrarily two times the triggering voltage, which is generally a low ESD stress level that generally does not cause any defect. This defines the rise time and the voltage amplitude to ensure the validity of the proposed frequency model.

#### IV. APPLICATION OF FREQUENCY PARAMETER MEASUREMENTS TO THE MODELING OF A LIN PROTECTION DEVICE

##### A. TLP test

We applied the methodology to three different LIN transceivers designated A, B and C. Their quasi-static I(V) curves extracted by TLP measurements are plotted in Fig.18. Components A and B exhibit strong snapback behavior while component C is a diode. The components have the same package.

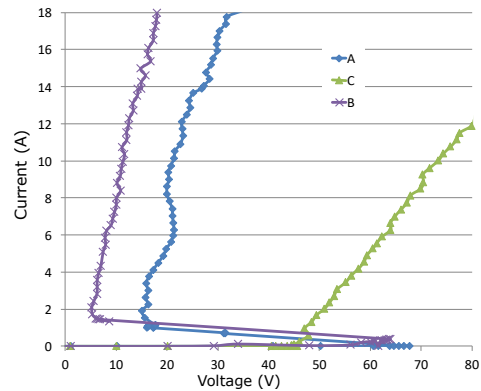


Fig. 18: Quasi-static I(V) curves of the three LIN components for positive pulse across LIN to GND pins.

Following the methodology described previously, the magnitude and phase of the S11 parameter, calculated from 800V TLP measurements, of the three devices are represented in red in Fig. 19 while the SPICE model generated by ADS is represented in blue. The model fits well until 200MHz. ADS

is not able to give a model that fits with our specifications for higher frequencies. This is mainly due to strong oscillations of the S11 phase (from  $180^\circ$  to  $-180^\circ$ ) which foils (*NdT: this is not clear. Is "foils" or "falsifies" meant?*) the model extraction algorithm. The SPICE models obtained from S-parameter measurements for the three LIN components are compared with the transient measurements on the device for 800 V TLP and 1 ns rise time injection in Fig. 19. The quasi-static level matches for all the devices. The transient behavior is also well reproduced, even if the initial voltage peak is overestimated for the component B in simulation (20%). Moreover, the frequency SPICE model is limited to 200MHz. This explains why the simulated voltage waveforms are smoothly comparable to measurements.

### B. Human Metal Model test

The S-parameters model extracted with the proposed methodology has been validated for transient ESD simulation under TLP injection, which is a  $50 \Omega$  testing system. In this section, we compare the S-parameters model with an ESD "gun" measurement in HMM configuration. The stress waveform has a 700 ps rise time and an amplitude of several

kilovolts. The validity conditions of the proposed frequency model are fulfilled in these conditions.

Two components, a CMS resistor of  $2.2 \Omega$  and a LIN transceiver (type A), are tested successively on the same PCB board. The CMS resistor is used to calibrate our measurement set-up. It is soldered on the PCB in place of the transceiver, between the LIN bus I/O and ground pads. The ESD gun is pre-charged at 2 kV. Its ground is connected to the board and plated to the metallic table (Fig. 20). The voltage across the component terminals is measured using a  $500 \Omega$  resistor placed as close as possible to the component under test. An additional 20dB attenuator is placed at the scope input.

In simulation, the entire measurement set-up is taken into account (SMA connector [44], PCB, coaxial line, etc.), as shown in Fig. 20. The ESD gun is modeled according to Chiu's gun model [45]. The values of the capacitor C1 and the resistor R2 are adjusted to fit measurement and simulation of the injection on the  $2.2\Omega$  resistor.

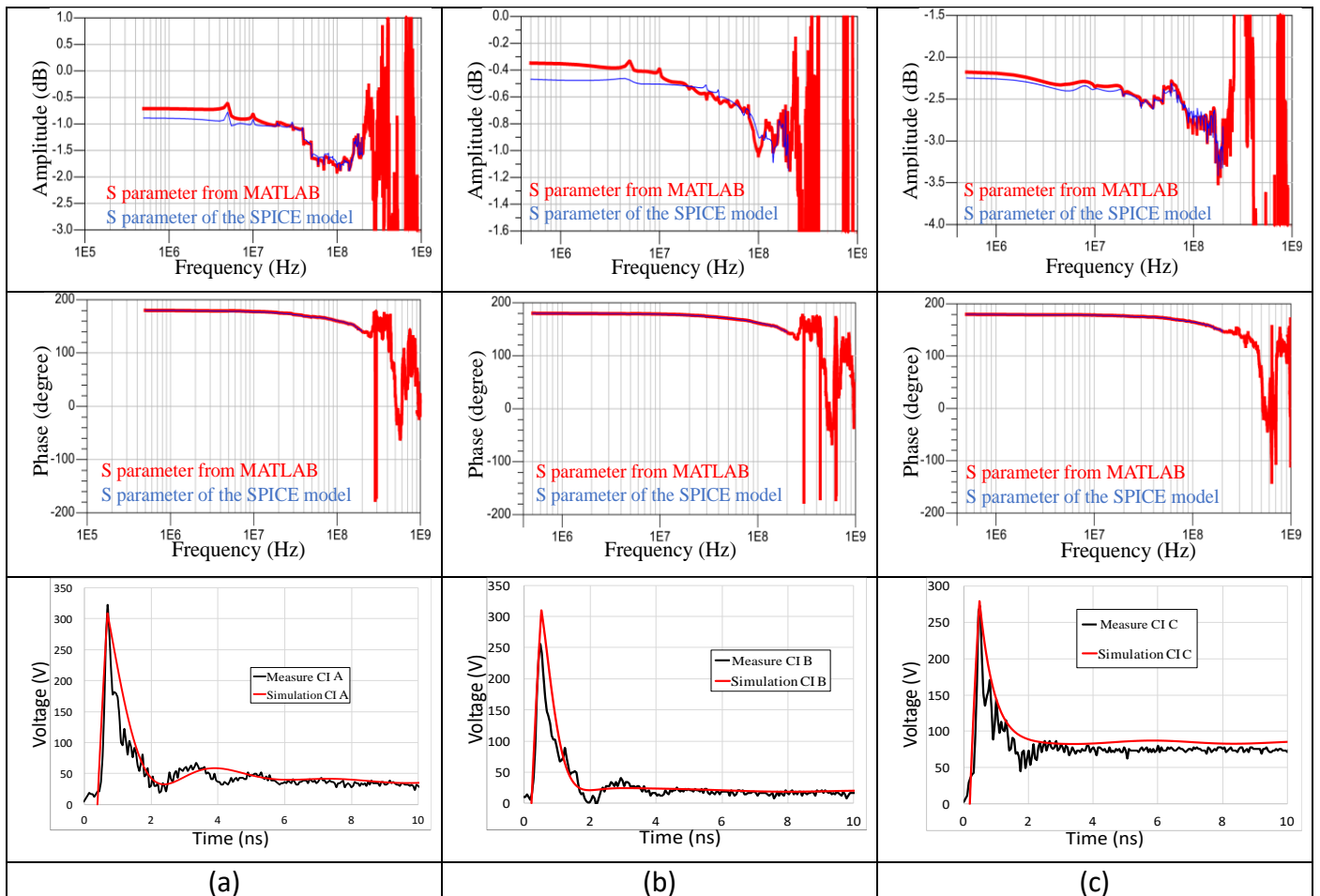


Fig. 19: SPICE model fitted curve (blue) on the S-parameter extracted from TLP measurements (red) in amplitude and phase, and Voltage comparison between the TLP measurements on the LIN-GND protections (black curve) and the generated SPICE model (red curve) on the three LIN devices

The voltage comparisons between measurement and simulation for a 2kV ESD gun injection, on the 2.2 Ω resistor and on the LIN device, are shown in Figs. 21 and 22 respectively. In Fig. 21, the measurement shows that the amplitude of the initial overshoot is correctly estimated by the model. However, all the mismatch impedances between the gun (330 Ω), the PCB line (50 Ω) and any other possible connections (such as probes and LIN bus connections) create strong oscillations not perfectly reproduced in the simulation. We did not succeed in explaining why the negative oscillation is very attenuated in the

measurements. It could be related to some attenuator in the gun to avoid reflections not considered in our simulation. PCB reflections seem to increase the oscillations. Nevertheless, if we focus on the first peak, the amplitude is well reproduced.

Fig 22 compares measurement and simulation when the stress is injected between the LIN and ground pins of the LIN transceiver. The S-parameters used in simulation with the same set-up conditions are able to reproduce the first peak very well. As for the 2.2 Ω load, the negative oscillations are attenuated in the measurement.

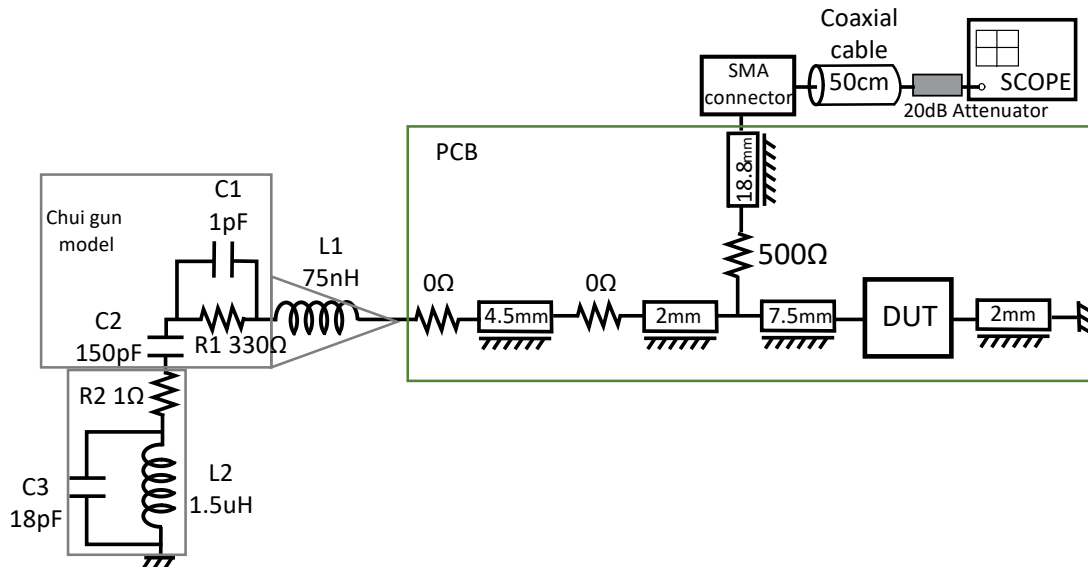


Fig. 20: ESD gun measurement and simulation set-up. The DUT are the LIN-GND component, S-parameter model in simulation, or the 2.2Ω resistor.

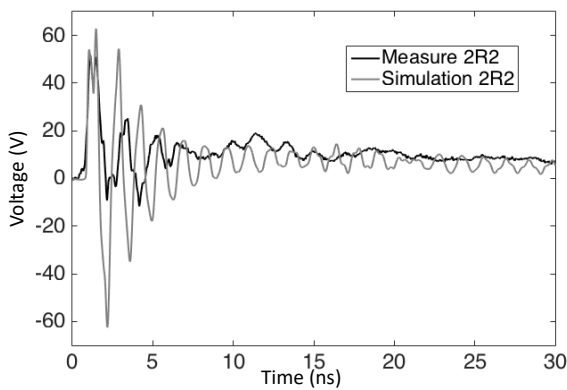


Fig. 21: Voltage comparison of the simulation (grey curve) and the measurement (black curve) on the 2.2Ω resistor under 2 kV ESD gun

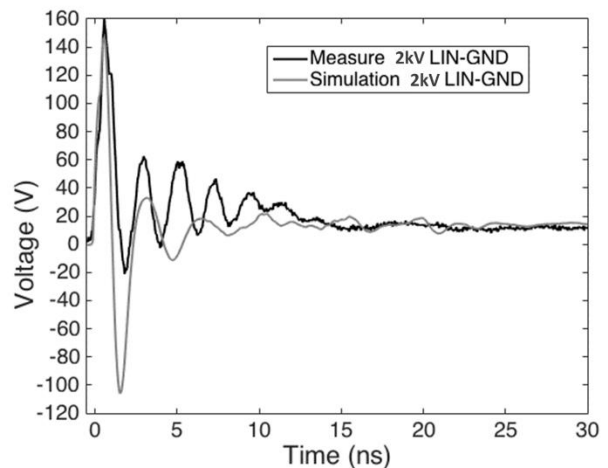


Fig. 22: Voltage comparison of the simulation (grey curve) and the measurement (black curve) on the LIN-GND (b) under 2 kV ESD gun

## V. CONCLUSIONS

This paper investigates if a non-linear ESD protection could be considered as a linear device while the stress rise time is in the range of 1ns, which is the rise time range of a typical ESD gun stress. We demonstrate that this supposition is correct for well-defined stress injections constrained by the  $dv/dt$ . This is mainly because the passive device network and the equivalent RLC dynamic elements of the ESD protection hide the non-linear behavior generally modeled by a switch in simulation. Starting from the approximation that an ESD protection device can be considered as a linear device, we assume that a "frequency-parameter" could be used to simulate its behavior. Obtaining the frequency parameter of an ESD protection from conventional VNA is not possible due to the power limitations of such equipment and the damage caused by a continuous wave on an ESD protection device. Consequently, a mathematical approach has been developed to obtain the equivalent S-parameters from TLP measurements.

This TDR method using a TLP was validated on passive and active devices. The limitations of this measurement equipment and the required validity conditions have also been given. The extracted frequency parameter is used to obtain an equivalent SPICE model of an ESD protection which can work in both transient and frequency simulations. The simulation results using such a model provided good results when the devices are exposed to Gun stresses in HMM conditions. Some power dependency that could appear on certain protection devices is under study and more investigations are underway to define frequency parameters that consider this effect.

One of the main advantages of the modeling method proposed in this paper is that it could be used to investigate system level ESD as well as electromagnetic compatibility in high injection regime. Further work will investigate how to acquire more than a 2 pins frequency description like the multiport frequency S parameter does. Some more studies have to be performed to set the validity of such a model for high frequency devices.

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