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Fabrication and characterization of Si₃N₄-MIS structures on p-type diamond

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With its wide bandgap and interesting electronic properties, diamond is a promising material for high power applications. However, several technological obstacles have to be overcome to develop MOS diamond devices. In this context, we study the fabrication of MIS structures based on the deposition of a Si₃N₄-dielectric layer. The C(V) measurements are presented and the interface between diamond and Si₃N₄ is analyzed.

MIS structures are fabricated on a P⁻/P⁺ stack on (100) diamond at LSPM laboratory with doping estimated to be [B] = 1x10¹⁷ at.cm⁻³/[B] = 1x10²⁰ at.cm⁻³ for 4μm/10μm thicknesses respectively.

The diamond layers surface is chemically cleaned and treated using Ozone UV to ensure the elimination of contaminants and C-H bonds in order to limit the number of traps at the interface between diamond and the dielectric layer.

A 30nm-Si₃N₄ layer is deposited by LPCVD at 770°C. Ohmic contacts using Ti/Pt/Au are fabricated on the P+ layer and Al contacts (of a diameter of 300μm, 200μm and 100μm) were deposited on the dielectric layer.

The module and argument variations of the impedance are then measured. These characteristics show the capacitive behavior of the structures over a wide frequency range, from 1 kHz to 100 kHz. The influence of the diamond p- layer resistivity is therefore negligible. A two-element model (capacitance and resistance in parallel representing leaks) is therefore used hereafter.

C(V) measurements show the different modes of accumulation, depletion and deep depletion. Comparison between measurement and to the theoretical curve calculated from the model of the ideal MIS device highlights the presence of a significant number of traps.

The development of these functional MIS structures opens the way to the manufacturing of diamond power MOS devices, even if a limitation of the traps is still necessary.