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***Abstract* — Dense integration and high operating frequencies associated with increased number of I/O buffers of FPGAs are factors contributing to electromagnetic emission (EME) increase. Consequently, the radiation issue that used to be discussed at PCB level has nowadays shifted to component level. Thus it is of high interest and challenging to investigate chip EME performance. This paper presents an analysis about the impact of the placement and routing (P&R) process of logic inside the FPGA on the chip EME level. With this purpose, a softcore processor was placed and routed based on three different strategies in the configurable logic block (CLB) array of a commercial FPGA and executed an application code running over an operating system (OS). One of these P&R strategies is performed automatically by a commercial CAD tool, whose results are compared against the other two manually P&R processes of the FPGA. Two experiments have been performed. The obtained results indicate that the EME level can be affected up to 21.8% by the way the processor is placed and routed inside the FPGA. Moreover, we propose a few recommendations to improve the efficiency of the commercial CAD tool to execute the P&R process having in mind the FPGA EME.**

Keywords — Commercial Field-Programmable Gate Array (FPGA), Logic place and route process, Electromagnetic emission (EME), GTEM Cell Test Method, Surface Scan Test Method.

I. INTRODUCTION

As semiconductor technologies have been shrinking, integrated circuit (IC) parameters such as operating frequency, integration density, and the number of I/O interfaces have been significantly increased. As consequence, electromagnetic emission (EME) became a paramount issue in the IC design. In this scenario, engineers must guarantee the ability of electronic components to operate safely in an increasingly hostile electromagnetic environment. Therefore, dealing to better understand the relationship between ICs and EME, several studies have been found in the literature dealing to define measurement procedures and standards, laboratory setup and countermeasures to understand and minimize EME from ICs. Among the most prominent works, it is worth mentioning the following ones: King Lee Chua *at al.* [1], Van Toan Nguyen *at al.* [2], Mohamed Ramdani *at al.* [3], Jan Mocha *et al.* [4], J. Szczęsny, *et al.* [5], Juliano Benfica *et al.* [6,7].

Nevertheless, from the best of our knowledge it is worth noting that none of the previous works found in the literature was dedicated to study the effect of logic placement and routing (P&R) on the EME level of FPGA. Dealing to minimize this gap, this paper analyzes the impact of the P&R process of logic inside the FPGA on the emission level of such component. Though, a softcore version of the processor Hellfire RISC [8,9] was placed and routed in three different ways in a commercial FPGA (Xilinx/Spartan 3E, part number XC3S500E-4PQ208). In order to measure EME of such embedded system, two experiments were performed. The first experiment measured the far-field emission from voltage raw measurements at GTEM cell terminal [10]. The second experiment was based on the so-called Surface Scan Method [11]. This measurement technique enables the visualization of the near magnetic field directly at the surface of an IC package or microchip. In this case an H-field probe is automatically moved step by step over the surface of the IC. At each position, the magnetic field is measured with the help of e.g. a spectrum analyzer in a certain frequency position or range.

II. CASE-STUDY: HW, SW AND PLACE & ROUTE STRATEGIES

The case-study was based on a Spartan 3E FPGA (part number XC3S500E-4PQ208), from Xilinx, which was mounted on a dedicated board specially designed to support EMC test [6]. The board design and software development were carried out by the Catholic University – PUCRS. In order to analyze the effect of the P&R algorithm on the FPGA emission level, a softcore processor: Hellfire RISC running a Bubble-Sort program over an operating system (HF-OS) [8,9] was placed and routed in three different configurations in the Spartan 3E FPGA. Fig. 1a depicts the basic block diagram of the embedded system instantiated in the FPGA and mounted on board. Fig. 1b presents a photo of the test board.

In the first configuration, the processor was placed and routed automatically by the Xilinx ISE-EDK Design Tool without designer assistance (let us say this is the "Automated" P&R version). In the second and third configurations, the processor was completely and intentionally sat in the periphery region ("Center" version) and in the left-hand side ("Right" version) of the configurable logic block (CLB) array of the FPGA. With this purpose, the designer prevented the ISE-EDK Tool from instantiating the processor core in the center of the CLB array (i.e., the "Center" version) and in the right side of the CLB array (i.e., "Right" version). Fig. 2 depicts the three P&R strategies.

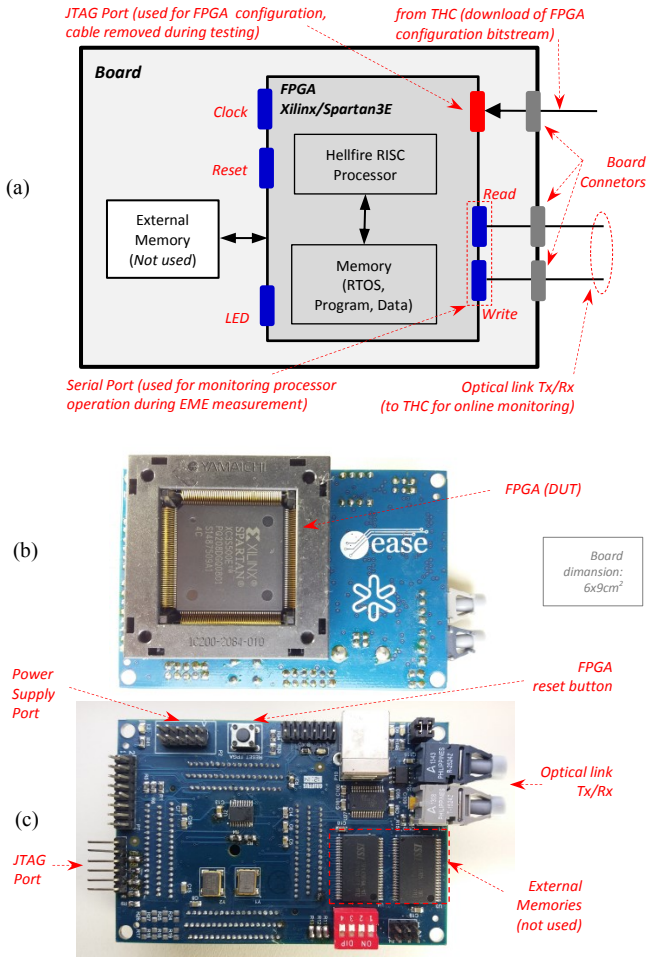

Fig. 1. Test board: Embedded system overview (a); Photo of the board: FPGA side (b); control side (c).

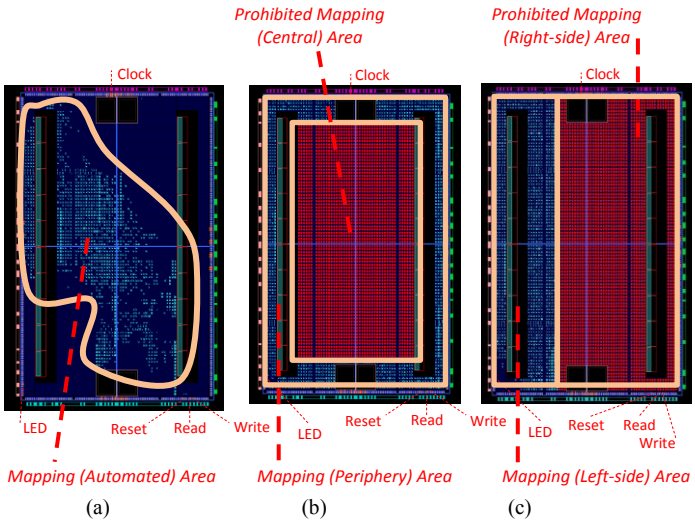

Fig. 2. Three P&R strategies to instantiate the processor core inside the CLB array of the FPGA: (a) "Automated", (b) "Center", (c) "Right".

In order to prevent board-level signals from jeopardizing FPGA EME measurements, the whole system (i.e., processor and memory containing operating system, program and data) was mapped inside the FPGA. The only signals flowing on and outside board during EM emission measurement were those associated to the serial communication connecting the FPGA to the user test host computer (THC). This serial port was used to monitor processor operation in real time during the experiments. In order to prevent communication from being disrupted by electromagnetic interference during the experiments, the serial communication was implemented by means of a two-module optic fiber link (Tx/Rx). Figs. 1 and 2 depict the five pin positions configured around the FPGA CLB: "*Read*" and "*Write*" (for the serial communication), "*LED*" (to monitor FPGA operation), "*Clock*" and "*Reset*". The pin positions were fixed for all three P&R strategies. Additionally, a JTAG connection was used to configure the FPGA (Fig. 1, red connector). Once the configuration was complete, this cable was removed before starting EME measurements.

III. Performed Experiments

In order to observe the effect of the place and route (P&R) algorithm on the FPGA emission level, three experiments were performed as described in the sequence.

A. GTEM Cell Test Method

The first experiment, based on the GTEM Cell Test Method [14,15], was performed at the LAAS-CNRS and is depicted in Fig. 3.

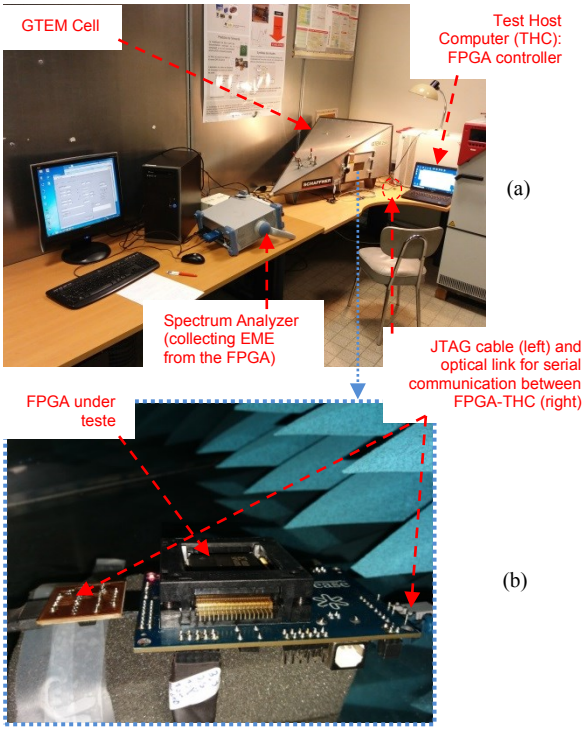

Fig. 3. GTEM Cell Test Method experiment: (a) general overview; (b) detail of the FPGA under test.

Normally, to characterize only the EM emission of the FPGA, one would build a standardized EMC test board according to the requirements of IEC61967-1 and IEC61967-2 [10]. With this particular test board, only the FPGA is allowed on one side of the test board and all other components needed

to operate the FPGA should be on the opposite side of the board. This board would then be inserted into the opening of the GTEM cell in such a way that only the FPGA would look inside the cell. In this case, however, even though the FPGA is sitting alone in one side of the test board, the requirements of IEC61967-1 and IEC61967-2 were partially attended and the existing test board was fully placed in a fixed position directly inside the GTEM cell. In order to achieve reproducible results, the position of the test board was not changed during the whole experiment, for the comparison measurements. The FPGA activity was controlled by a Test Host Computer (THC) placed outside the GTEM cell. The voltage induced at the GTEM cell terminal by the FPGA radiation was measured with a spectrum analyzer. If the FPGA board is assumed to be electrically small and equivalent to an elementary electric dipole, the far-field emission from the FPGA board can be estimated at any distance (in this experiment, at 1m) [12]. In spite of these assumptions, the results can be compared with typical radiated emission requirements at electronic equipment level.

The GTEM cell estimates the far-field emission of the FPGA including the emission generated by the whole PCB on which the IC is mounted on (including tracks, connectors and other components such the serial/optical converter IC sitting nearby the FPGA). In contrast to that, the near field measurement technique presented in *Section B* is mainly focused on the precise localization of the near magnetic field distribution over the die surface by using a very sensitive and small, moving near field probe, which offered a high local resolution. These two methods constitute effective methodologies to characterize ICs in terms of EME.

B. Surface Scan Method with a Moving Near-Field Probe

The second experiment, based on the Surface Scan Method [11,13,16], was performed at the TU Graz University (Fig. 4).

This method constitutes an effective methodology to characterize printed circuit boards and ICs in terms of electromagnetic emission (and immunity as well). It is a useful technique to locate areas of critical radiation, which could influence the performance of devices placed nearby or the device under test itself.

Fig. 4 depicts a photo of the test set-up. The equipment seen in this figure consists of a micromanipulation (wafer probing) that is equipped with stepper motors to control the probe movement in XYZ directions (in our experiment, Z was fixed at a constant distance of 2mm from the IC package). Note that while the GTEM Cell Test Method experiment measured emission from the whole board based on a fixed probe position with respect to the FPGA package, this experiment scanned 4,000 points above the surface of the package with a moving near field probe where the die is located, hence adding a much higher precision and sensitivity to the emission measurement.

IV. Obtained Results

Fig. 5 summarizes the EME measurements. Fig. 5a depicts results for the GTEM Cell Test Method experiment, whereas Fig. 5b presents results for the Surface Scan Method. Table I summarizes the ambient noise values measured for both experiments. The ambient noise was measured by disconnecting the board under test from power supply lines and then, the Spectrum Analyzer captured the remaining noise around the FPGA.

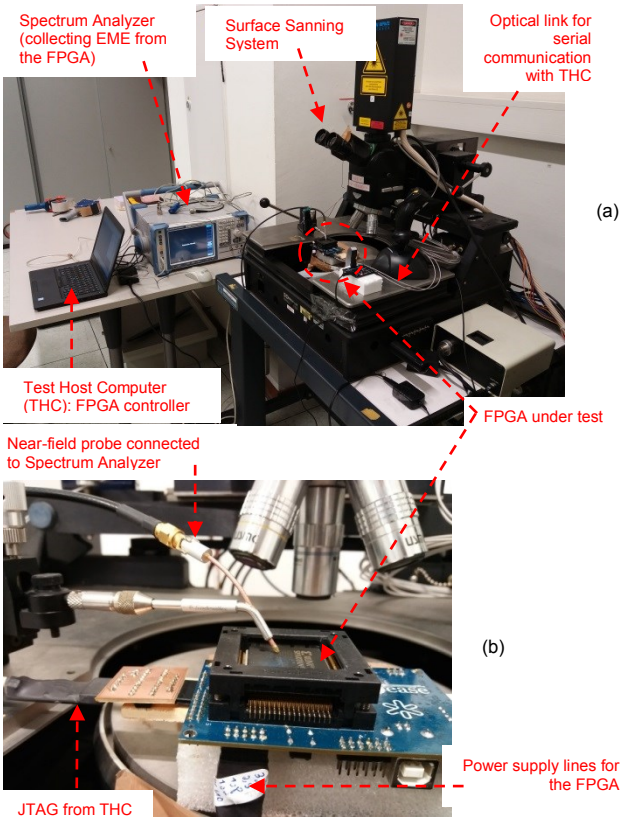

Fig. 4. Surface Scan Method experiment: (a) general overview; (b) detail of the FPGA under test.

By observing Table I and Fig. 5, the following conclusions can be taken:

a) In Fig. 5a, the emission level of the "Automated" place and route version is **21.8%** higher than the average of the other two configurations ("Centered" and "Right" versions). Note that the GTEM Cell Test Method measures EM emission from the whole system, i.e., not only from the FPGA but also from the board (including tracks and other components such the serial/optical converter logic sitting around the FPGA).

b) In Fig. 5b, the EM emission level of the "Automated" P&R strategy is **8.4%** higher than the other two configurations ("Centered" and "Right" versions). Since this method scanned 4,000 points right above the package surface with a moving near field probe, it is expected a much higher precision and sensitivity to the emission measurement as compared to the GTEM Cell Test Method.

Table I. Ambient Noise Measured for the Experiments

Experiment	Ambient Noise
Surface Scan (Moving Near-Field Probe) Method	3.297 x 10-3 (V)
GTEM Cell Test Method	8.938 x 10-4 (V/m)

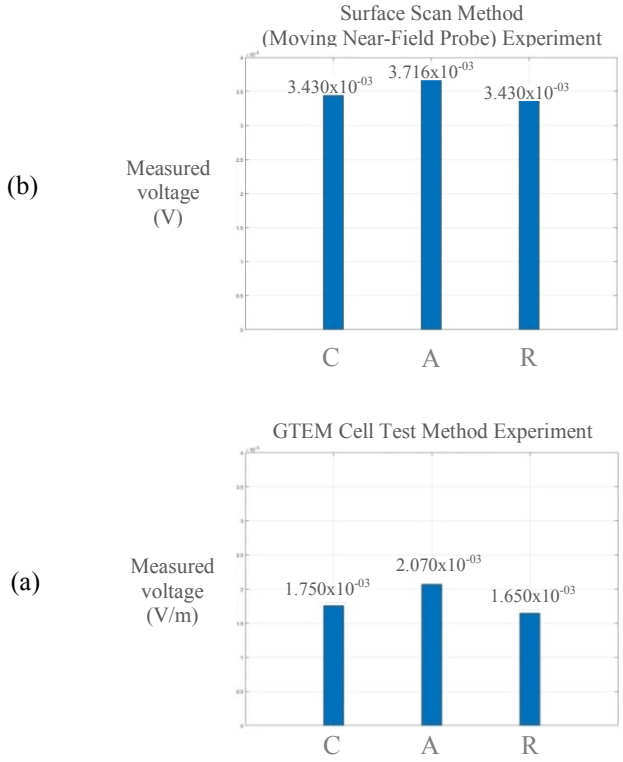

Fig. 5. EME measurements for the three FPGA P&R strategies (C: "Center", A: "Automated", R: "Right"), performed during the experiments: (a) GTEM Cell Test Method; (b) Surface Scan Method (Moving Near-Field Probe).

TABLE I. AMBIENT NOISE MEASURED FOR THE EXPERIMENTS

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V. HARDWARE, DELAY AND POWER ISSUES

In this section, the following topics will be discussed:

A. Hardware required to instantiate the processor in the FPGA

This topic discusses the impact of the size of the hardware required to implement the processor for each of the three P&R strategies, on the FPGA EME level. Even though it is not a rule of thumb, there is a tendency that the larger the circuit hardware, the higher EM emission from the circuit.

Table II presents data extracted from the post P&R report (*Map_Report* file), generated from the Xilinx ISE-EDK Design Tool. This table depicts the hardware required to implement the "Logic", i.e., the Hellfire RISC processor into the FPGA, in terms of Flip-Flops (FF) and Look-Up Tables (LUTs). These are the same hardware resources required for any of the three P&R strategies, since the number of LUTs and FFs is the same to instantiate the processor no matter is the place where it is mapped into the device. Note that the above hardware resources are those required only for *instantiating* the processor, but not for *routing* it into the FPGA (e.g., routing the processor with memory). Therefore, it is not possible to explain why the "Automated" version emits more radiation then the other two strategies only by analyzing the hardware required instantiate the Hellfire processor into the FPGA.

TABLE II. HARDWARE REQUIRED TO INSTANTIATE THE PROCESSOR ("LOGIC") IN THE FPGA

Place & Route Strategy	Look-Up Tables (LUTs): 2,304 (100%)		Flip-Flops (FF)
	Used as "Logic"	Used for "Dual-Port RAMs"	Used for "Dual-Port RAMs"
Automated	2,048 (88.89%)	256 (11.11%)	610
Right			
Center			

B. Data path delay in the FPGA

This section analyzes the impact of the delay induced by routing the processor in the configurable logic block (CLB) on the FPGA EME level, for each of the three P&R strategies. Note that increased routing delay suggests that *longer routing paths* are used to connect the processor logic along with the FPGA CLB. A hypothesis is that long interconnects demand the use of strong signal buffers to guarantee strict signal propagation timing. These routing resources (i.e., buffers) would produce large dynamic currents, which might result in high EME level.

Data in Table III were extracted from the post P&R report (*Post_PAR* file) generated by the Xilinx Timing Analyzer Tool. As depicted in Table II, since the number and types of LUTs and FFs required to implement the Hellfire RISC processor (the "Logic") is the same for any of the three strategies, the *same* intrinsic delay was estimated by the Timing Analyzer Tool for the strategies: 1.553ns (see Table III).

However, the delay induced by the routing ("Route") of the logic is *not* the same for all strategies, since it depends directly on the assumed P&R approach and their respective routing paths. In this case we observe that the "Automated" version presented the largest total delay (2.975ns, compared to 2.521ns and 2.412ns). This is consequence of the largest "Route" delay: 1.422ns (resp. 0.968ns and 0.859 for the "Right" and "Center" strategies, respectively).

Note that the increased "Route" delay suggests that *longer routing paths* are used to connect the logic spread around the floor planning "Automated" when compared to the other strategies. A hypothesis is that long interconnects demand the use of a large number of strong signal buffers to guarantee strict signal propagation timing. These routing resources (i.e., buffers) produce large dynamic current, which might result in high EM emission level.

As seen in Table III, the total delay difference between "A" and "C" strategies is 23.4% (2.975ns against 2.412ns) with respect to the "C" strategy. Also, the total delay difference between "A" and "R" is 18.0% (2.975ns against 2.521ns) with respect to "R" strategy.

On the other hand, the difference between "R" and "C" strategies is rather smaller: 4.5% (2.521ns against 2.412ns). This small difference could explain the fact that the EM emission level of "R" and "C" strategies is the same in Fig. 6c and quite close in Fig. 6a (around 5% difference on their emission level).

In opposite, the "A" strategy total delay is much larger than the ones from "R" or "C", which made it easier for Surface Scan and GTEM Cell measurement methods to discriminate the "A" strategy as the one issuing the highest EM emission level (Figs. 6c and 6a).

However, it is important to note that there is no guarantee that such a P&R strategy with long interconnects will always produce higher EM emission than other P&R strategy, implemented with small routing delays due to short interconnects (and so, dissipating less power), because the actual EM emission level depends also on the *coupling degree between the layout of the routed tracks* and the *signal switching activity along these tracks*.

Fig. 5 and Tables III and IV support this reasoning: "A" strategy produces the highest EM emission, presents the largest data path delay, but it is not the one dissipating more power among the three P&R strategies. "R" strategy produces the lowest EM emission, but it is not the one presenting the smallest data path delay and the smallest power supply dissipation. Similarly, "C" strategy dissipates the largest power supply among the three strategies, but it is not the one yielding the highest EM emission level and it is not the one presenting the largest data path delay. Some of these concerns have also been addressed in some extent in [14,17,18].

TABLE III. DATA PATH DELAYS IN THE FPGA

Place & Route Strategy	Data Path Delay (ns)		
	Logic	Route	Total
Automated	1.553 (52.2%)	1.422 (47.8%)	2.975 (100%)
Right	1.553 (61.6%)	0.968 (38.4%)	2.521 (100%)
Center	1.553 (64.4%)	0.859 (35.6%)	2.412 (100%)

C. System power consumption

This section analyzes the influence of the power dissipation on the EME level of the FPGA for the three P&R strategies. The hypothesis is that the greater the power dissipation, the higher the EME level.

Assume Table IV. Data in this table were generated in two steps: *a)* first, power dissipation of the logic was estimated by the Xilinx XPower Analyzer Tool *after* the P&R process; then, *b)* while running the Hellfire processor with the Bubble Sort program under the control of the operating system, the voltage drop over a 4 ohms resistor placed in series with the V_{DD} input power pins of the FPGA was measured by means of an oscilloscope. Then, the RMS power dissipated by the FPGA was computed for the three P&R strategies, as depicted in Table IV. XPower Analyzer estimated the dissipated power based on a *.vcd* (**v**alue **c**harge **d**ump) file containing data collected from a ModelSim simulation run which took around 2 hours and 30 mins to complete. This simulation represented a HellFire processor execution of 33,201,543,766 pico-seconds, which corresponded to one complete execution of the Bubble Sort program to reorder a 20-position vector. A *.vcd* file was generated for each P&R strategy and the size of a single *.vcd* file was in the order of 140 GBytes.

As observed in Table IV, the "Automated" strategy issued the smallest estimated dissipated power, followed by the "Right" and "Center" strategies. Nevertheless, the "Automated" and "Right" strategies issued roughly the same measured power dissipation. The Center strategy revealed the highest dissipated power in both cases (estimated and measured).

TABLE IV. SYSTEM POWER CONSUMPTION

R&R Strategy	Power Supply Summary (mW)			
	XPower Analyzer Tool Estimation			Measured
	Static	Dynamic	Total	RMS
Automated	81.85	26.96	108.81	28.11
Right	81.92	30.56	112.48	28.79
Center	82.10	40.99	123.09	32.35

Fig. 6 summarizes the design flow, the used tools and generated reports to build-up Tables I to IV and Fig. 5. The design environment was installed in a computer hosting an Intel Core i7 – 4700MQ CPU @ 2.40 GHz, with 8 GBytes of RAM and Windows 7 operating system. Several data files were generated during the design process. For instance the *.ncd* (**n**ative **c**ircuit **d**escription) file, generated during the *Design Capture*, is updated at the output of the *Post P&R Simulation* and grouped with files *.pcf* (**p**hysical **c**onstraints **f**ile) and *.ucf* (**u**ser **c**onstraints **f**ile) to serve as inputs to the Timing Analyzer Tool (to build-up Table III). The *.ncd* file is also combined with files *.vcd* or *.saif* and *.pcf* (**p**hysical **c**onstraints **f**ile) to serve as inputs to the XPower Analyzer Tool (to construct Table IV). The *.saif* file extension stands for **s**witching **a**ctivity **i**nterchange **f**ormat. The*.vcd* and *.saif* files describe circuit simulation activity by including specific switching information such as toggle rates, signal rates and frequency information; these files give the best accurate for power estimation.

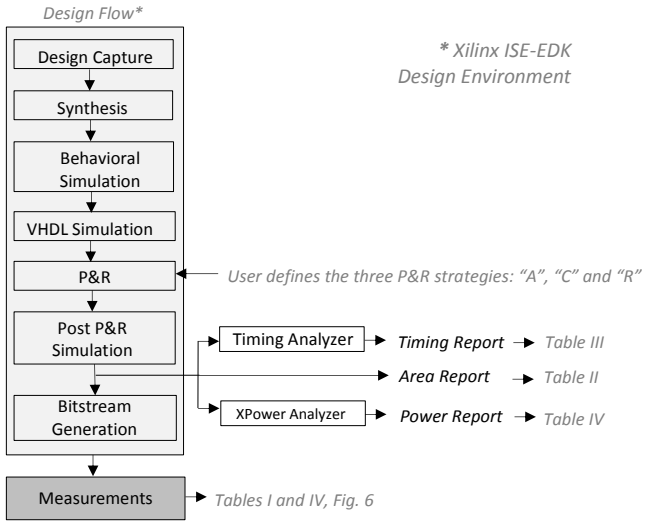

Fig. 6. Design flow and information collection for analysis.

VI. DISCUSSIONS

We observed in our experiment that:

i) For different P&R strategies, the FPGA emitted different EM emission levels (Fig. 6);

ii) The ISE-EDK Design Tool generated the same hardware resources for any of the three P&R strategies, since the same number of Look-Up Tables (LUTs) and Flip-Flops (FFs) was

used to instantiate the processor no matter is the place where it is mapped into the device (Table II).

iii) The Xilinx Timing Report indicated different data path ("logic" + "route") delays, for each of the P&R strategies (Table III). Since the "logic" delay was the same for any of the strategies, the differences in the data path delay are attributed to different "route" delays estimated by the Timing Analyzer Tool.

iv) The XPower Analyzer estimated different system power consumption for each of the P&R strategies (Table IV).

From the above considerations one might conclude that, for a given P&R strategy, large "route" delays are the result of *long routing paths* that are used to connect the logic spread around the FPGA CLB. These long interconnects demand the use of a large number of strong signal buffers to guarantee proper signal propagation timing. These resources (i.e., buffers) produce large dynamic current, which in turn might result in high EM emission level. However, it is worth noting that there is no guarantee that such a P&R strategy with long interconnects will always produce higher EM emission than other P&R strategy, implemented with small routing delays due to short interconnects (and so, dissipating less power), because the actual EM emission level depends also on the *coupling degree between the layout of the routed tracks* and the *signal switching activity along with these tracks*.

v) It seems that the ISE-EDK Design Tool performs the P&R procedure having in mind circuit optimization to power. From the best of our knowledge, we do not have official information from Xilinx on how the tool has been implemented and to which parameter it optimizes the P&R process. But if this reasoning is true, then it would be a great improvement to this tool if it could optimize the P&R process by having in mind a second parameter, in addition to power dissipation: the EM emission. During times when edge computing embedded systems for IoT applications and critical applications are spreading around us everyday, this could be of high interest to engineers committed with the design for EMC topic.

VII. CONCLUSIONS

This work presented a study about the influence of the place and route (P&R) strategy on the electromagnetic emission (EME) level of a commercial FPGA. The considered device was a Xilinx Spartan 3E, part number XC3S500E-4PQ208, which was configured with the Hellfire softcore RISC processor available in the *github* public domain. The FPGA was mapped by three different strategies: "Automated", in which the processor was placed and routed automatically by the Xilinx ISE-EDK Design Tool. In the second and third versions, the processor was completely and intentionally placed in the left-hand side ("Right" strategy), and in the periphery region ("Center" strategy) of the configurable logic block (CLB) array of the FPGA. The processor executed a Bubble-Sort program running under the control of an operating system (OS).

The obtained results suggest that the P&R strategy can affect the FPGA emission level. For the developed experiments, the influence was in the order of **21.8%** (GTEM Cell Test Method) and **8.4%** (Surface Scan Method).

As far as we understand, results suggest that the Xilinx ISE-EDK Design Tool **does not** take into account circuit EM emission issue during the P&R process of the FPGA. To counteract this drawback, it is strongly suggested that the designer takes an accurate procedure to measure EM emission of different P&R strategies directly "*in circuit*" before finalizing the design process. Moreover, it would be useful to select more than one measurement approach, e.g., the GTEM Cell Test Method, which measures not only the emission from the FPGA but also from the whole system mounted on board (e.g., other nearby ICs, tracks, connectors and cables directly affected by the code running in the FPGA) and the Surface Scan Method, which measures with high precision the emission only from the FPGA die.

In this work we were focused on analyzing the influence of the P&R strategy on the emission level of the FPGA configurable logic block (CLB) array. For future work, we have two goals:

i) study in more detail the relationship among the following parameters: (1) number of hardware resources (LUTs and FFs), (2) data (logic and route) path delay, (3) signal switching activity, (4) dynamic power dissipation and (5) the respective EM emission level;

ii) place the (program and data) memory outside the FPGA, at the board level. This will allow us to analyze the IO pins influence on the FPGA emission level, for different P&R configurations.

iii) The differences in emissions are within a few dBuV. So, maybe it is useful to confirm the measurements on more FPGA samples. With this purpose, we are redesigning the test board to host a socket for the FPGA, so that this device can be replaced a couple of times during the experiment.

ACKNOWLEDGEMENT

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