Extraction of compact transient thermal models for a global optimization of a power system based on SiC MOSFETs switches

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This paper deals with the interest of compact transient thermal models in the optimization of power converting system. These models have to take into account thermal coupling effects between the different chips of a power module based on SiC MOSFETs. The developed models are easily implementable within simulation tools such as Modelica. We will show that for applications operating at low duty cycle or with fast varying power demand, the consideration of transient models could improve a global optimal design by lightening the system. This approach also ensures that the junction temperatures do not exceed their limit values.

1 Introduction

Compact thermal modelling is a powerful simulation tool for the design and thermal management of power converting systems. These models are developed to have a reduced calculation time and an accuracy comparable to 3D thermal simulators. In this paper, we will show that for the intended transient mission profile, the transient thermal study enables to reduce weight and size, as compared to steady state considerations based on the worst case point. This is especially important in the cooling system design.

The application example[1] taken in this study is an electrical bus with an ultra-fast recharging system to power the bus on its route with low pollutant emissions. In the bus, a battery pack and supercapacitors pack are associated with an electric power train. The studied power module is used as a buck DC-DC converter during the charging of a supercapacitor and a boost DC-DC converter during the power train supply (fig.1).

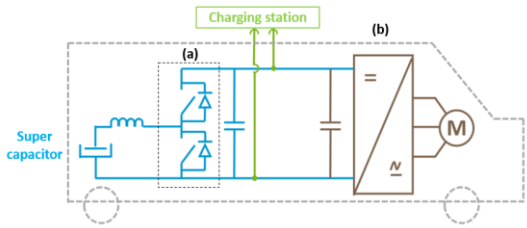

Figure 1. Illustration of the application (a) DC-DC converter (b) power train inverter

The charging operation takes approximately 30 seconds, and is repeated every 200s. For this type of mission profile, where the power dissipation does not last enough time to induce the steady state temperature of the components, to reach the optimum, it is very important to take into account the transient thermal behavior of the whole module and thus to extract transient models. It should also be considered that during the charging and discharging phases of the supercapacitors the module will alternately activate the transistors and body diodes. Thus, the sizing of the converter and in particular of its cooling system needs to consider the transient rise in junction temperatures during the MOSFETs operation. Unfortunately, a global multi-parameter optimization is quite complex and time consuming if it is based directly on 3D transient thermal modeling. We have therefore developed a methodology for extracting transient compact thermal models to fit precisely the thermal responses and to take into account thermal coupling between chips in the module.

2 Power converting system design

2.1 Steady state optimization

The purpose is to minimize the size and weight of the power converting system [1] [2] with the best compromise between the cooling system, here a forced convection heatsink, and filter sizes and with respect of thermal constraints of the chips. The weight of the cooling system, which is a major part of the power system, depends mainly on the losses of the converter in the worst case.

In this application, the worst case happens during the fast charging phase of the supercapacitors. A global optimization of the power converting system is performed on the maximum dissipation point in steady state. The self-heating of each chip is only taken into account. Thus the thermal resistance between the chip junction and the module base plate is considered with Rth=0.75 K/W. This value was extracted from 3D thermal simulation when one chip is activated. These considerations are generally used for a first step of power converting system design.

The optimization variables are the switching frequency, the heat sink size and characteristics of the filter components such as their width, height and admissible current ripple. The constraints are the junction, capacitor and inductor temperature limits. The thermal constraints for the

[1] http://pvi.nouveauxterritoires.fr/

optimization are defined so that junction temperatures do not exceed 175°C. The optimization method is based on the SLSQP algorithm of Scipy Python package. The results of the optimization are the dimensions of the heatsink, inductor and capacitor. The sized heatsink is then integrated into the 3D thermal model (fig.3). The fins are represented by an equivalent convection coefficient. A compact thermal model of the power module and the heat sink is extracted in order to study the possible improvements of the design result.

Table 1: Optimization results

Global mass	2.89 kg
Power	11.20 kW
Efficiency	92.20 %
Inductor	11 µH
Capacitor	3.08e-04 F
MOS power loss	507.25 W
Diode power loss	371.95 W
Heatsink	L250mmxW241.01mmxH24.10mm h equivalent = 203.81 W/K/m^2
Switching frequency	8.63e+04 Hz

2.2 Thermal coupling consideration

The compact thermal model should be able to take into account the thermal coupling due to the proximity of the chips on the power module and to ensure the respect of the thermal constraint.

thThe power module used in this study was designed and produced as a prototype by IRT Saint Exupéry. It consists of 12 SiC MOSFETs (fig.2) divided in 6 switching cells and body diodes are used to avoid additional diodes. A 3D modelling of the power module is realized using COMSOL Multiphysics. The considered cooling is a heat sink optimized for steady state operation. It is represented in simulation by its base only and the equivalent convective coefficient is applied at the bottom surface. Sides and top face are considered adiabatic (fig.3).

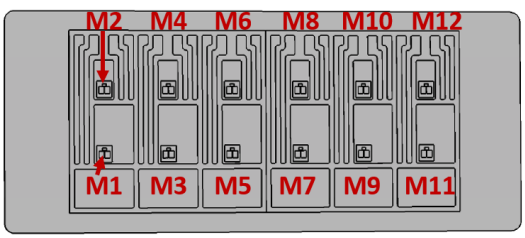

Figure 2. Power module with 12 SiC MOSFETs M1 to M12

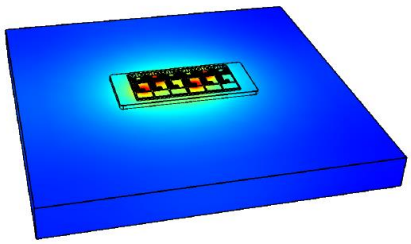

Figure 3. Simulation of the power module with optimized equivalent heatsink

An equivalent electrical network is defined for each component taking into account its self-heating and its thermal impact on the nearby chips. In order to take into account this thermal coupling, the static model is defined using the methodology of the optimal thermal coupling point [3] [4]. The basic principle of the methodology is based on the characterization of the isotherms of the structure. When a chip is activated, it is then possible to find isotherms at the same temperature as switched off chips. By activating the chips one by one, the thermal coupling points are located at the intersection of the considered isotherms (fig.4). Chips temperature data are extracted from COMSOL Multiphysics 3D thermal simulations.

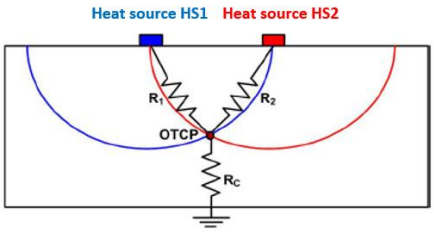

Figure 4: Illustration of the Optimal Thermal Coupling Point (OTCP)

For the studied power module, the chips with close temperatures i.e. on an equivalent isotherm are grouped. A coupling criterion is defined so that the difference temperature of the considered chip with reference to the ambient does not exceed 10% of the cluster average temperature. Consequently, this makes it possible to reduce the number of elements of the equivalent network depending on the intended target. For example, when M1 is activated, the clusters formed are shown fig.5 and the extracted static compact model with coupling points fig.6. A thermal model is associated to each chip. 3D simulation results show that only the models for M1, M3 and M5 need to be extracted and the others can be deduced by the symmetry of the module. For example, the models of M1, M2, M11 and M12 have the same RC elements with different coupling points.

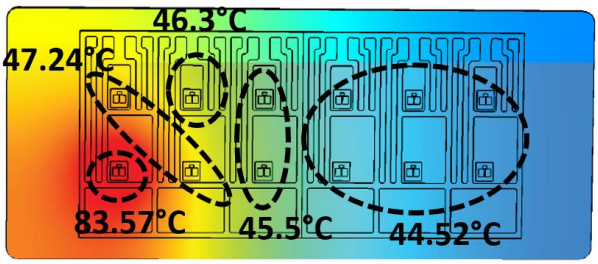

Figure 5. Illustrations of clusters for M1 ON P=50W and ambient temperature T_{amb}=40°C

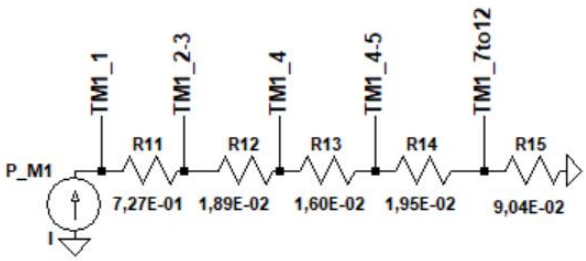

Figure 6. Static compact thermal model for M1 with self-heating TM1-1 and coupling points

Thermal resistances are calculated knowing the dissipated power, self-heating temperatures and coupling points temperatures:

$$R_{th} = \frac{\Delta T}{P} \ [\mathrm{K.W^{-1}}] \quad (1)$$

with ΔT: temperature difference [K], P: dissipated power [W]

When more than a single chip is on, the junction temperatures are calculated according to the superposition principle by considering the self-heating temperature and the coupling temperature for each chip:

$$\mathrm{Tj_{M1}} = \mathrm{TM1\_1} + \sum_{i=1}^{12} \mathrm{TMi\_1} \ [°C] \quad (2)$$

with $\mathrm{Tj_{M1}}$: junction temperature of M1 [°C], TM1_1 : self-heating of M1 [°C], TMi_1: coupling terms [°C]

3 Dynamic compact thermal model

The consideration of electrical and thermal time constants of the application leads to the development of a dynamic compact thermal model. Indeed, the charging of the super-capacitors lasts 30 seconds while the thermal settling time of the module is about ten minutes. Thus, the temporal simulation of the temperatures could avoid an oversizing of the power converting system.

The extension to the dynamic model consists in determining the equivalent network capacitances while keeping the resistances values of the static model. The objective is to find an analytical model to represent self-heating and coupling between chips during the transient phase.

Dynamic models in literature are often based on multi exponential fitting and deconvolution operations [5] [6]. The functions used can be quite complex and the processing to obtain the spectrum of time constants is not always obvious. A type of representation generally used is the Cauer model for its physical representation of the 1D diffusion effect in multiple layers structures. However the major limitation concerns its analytical formulation because time constants cannot be calculated directly as they depend on each of the other elements of the circuit [7]-[9]. As our focus is on the generation of an analytical behavioral model, a Foster-type network is used for its easier time constants identification and reduced calculation time. The extracted model simulates the different time constants of temperature rises of each chip during the mission profile.

The defined algorithm to extract thermal capacitances is described in fig.7. The steps for calculating cell elements from 3D thermal simulations are described below :

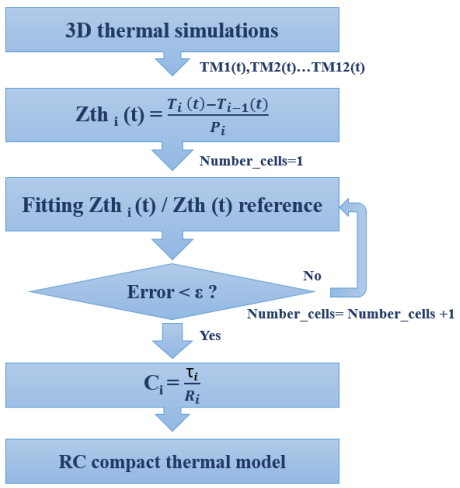

Figure 7. Schematic diagram for RC model extraction

Step 1: COMSOL 3D thetherrmal simulations are performed for one component activated to create the temperatures database. The results are the transient temperature response of each device.

Step 2: Considering the activated chip, a Foster network is defined with a number of cells equal to the number of defined coupling points. The thermal response of each cell is calculated as follows:

$$Zth_i(t) = \frac{T_i(t) - T_{i-1}(t)}{P_i} \quad [\mathrm{K.W^{-1}}] \quad (3)$$

Step 3: the thermal response of a cell is fitted using simplex algorithm to minimize the norm between reference thermal response and Foster cell response. Cells are added to improve

the fitting accuracy if the average relative error exceeds 10%. This process is repeated for each network cell.

Step 4: the thermal capacitances are determined using the time constant and the resistance of each Foster cell as follows:

$$C_i = \frac{\tau_i}{R_i} \quad [\mathrm{F}] \quad (4)$$

The extracted compact RC thermal models of each chip (fig.8) are used to calculate the transient junction temperatures in an electrothermal simulator of the bus converter.

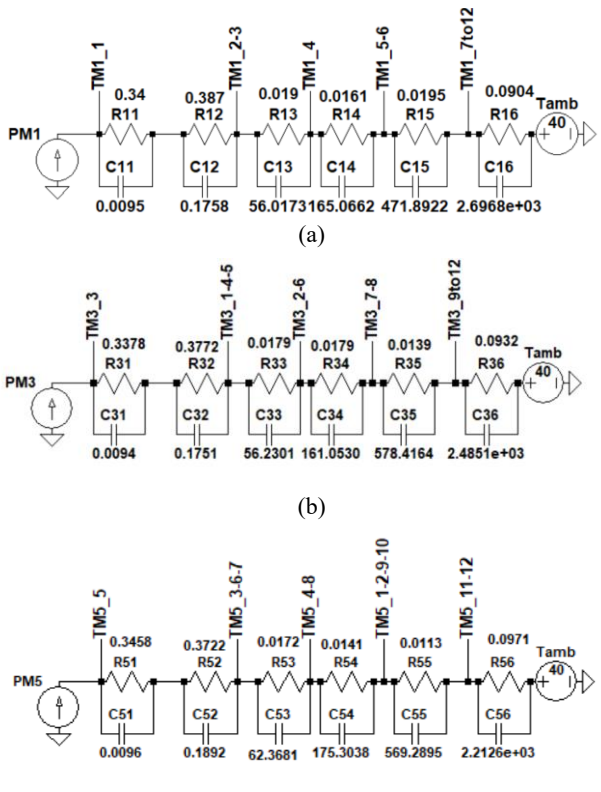

Figure 8. Dynamic compact thermal models of (a) M1 (b) M3 (c) M5

4 Model integration

4.1 Electro thermal simulator

The extracted compact thermal models are implemented in an electrical and mechanical modeling of the bus using Modelica (fig.9) [10]. The vehicle's velocity is adjusted by control loop. The supercapacitor is connected to the DC-DC converter which manages the charge and discharge phases during the bus operation.

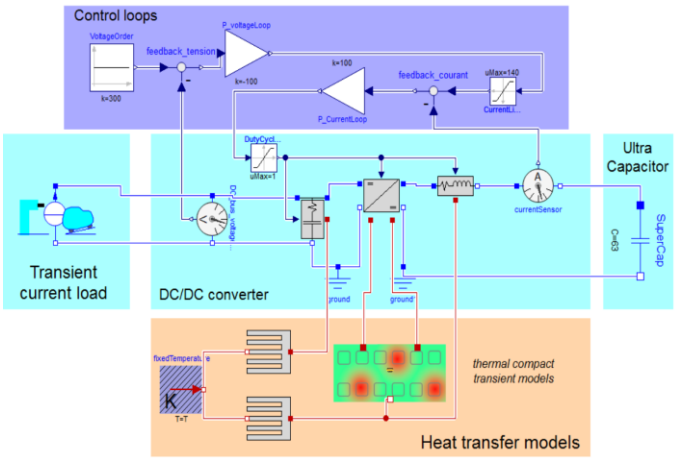

Figure 9. Modelica modelling of the electrical bus

The electrical model of the DC-DC converter is implemented and used to also calculate the thermal losses. Conduction losses P_{cond} and switching losses P_{sw} are taken into account (fig.11):

K1 MOSFET : $P_{cond\_K1m} = I_{out}^2 R_{DSON} \frac{V_{out}}{V_{in}}$ [W] (5)

K2 MOSFET : $P_{cond\_K2m} = I_{out}^2 R_{DSON}(1 - \frac{V_{out}}{V_{in}})$ [W] (6)

K1 diode : $P_{cond\_K1d} = V_F I_{out}(1 - \frac{V_{out}}{V_{in}})$ [W] (7)

K2 diode : $P_{cond\_K2d} = V_F I_{out} \frac{V_{out}}{V_{in}}$ [W] (8)

$$P_{sw} = \frac{V_{in} V_{out}}{2} \left(t_{rise} + t_{fall}\right) f_{sw} \quad [\mathrm{W}] \quad (9)$$

with I_{out} : DC output current [A], R_{DSON} : MOSFET drain-to-source resistance in the on state [Ω], V_{out} : DC output voltage [V], V_{in}: DC input voltage [V], V_F: diode forward voltage, t_{rise} : turn-on transition (s), t_{fall}: turn-off transition (s), f_{sw}: switching frequency [Hz]

Conduction and switching losses are calculated as inputs for the thermal model from the given mission profile (fig.10).

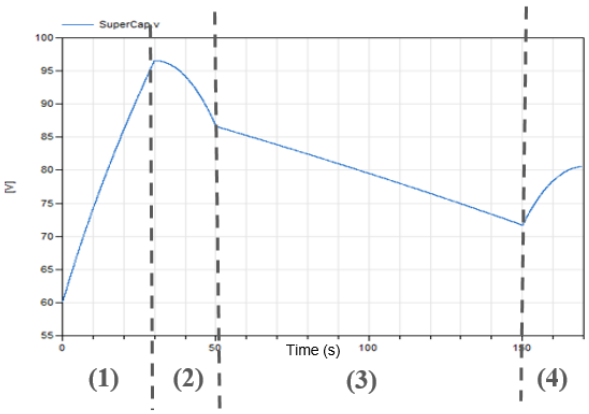

Figure 10. Supercapacitor voltage variation during the mission profile (1) supercapacitor charge (0-30s) (2) bus acceleration (30s-50s) (3) constant speed phase (50s-150s) (4) braking phase (150s-170s)

The power module chips are used to simulate the high side switch K1 and the low side switch K2 of the DC-DC converter (fig.11). Thus 6 MOSFETS in parallel are associated with a switch and work in direct mode or diode depending on the operating phase of the converter. A staggered configuration of the switches is chosen for a better repartition of the dissipated power (fig.12).

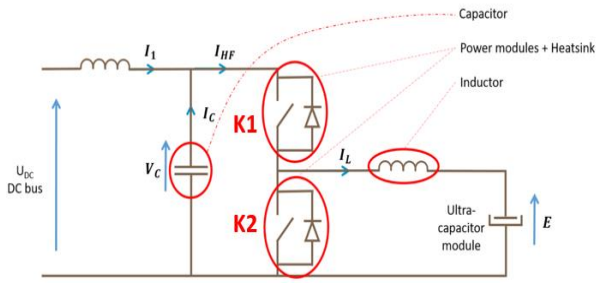

Figure 11. DC-DC converter diagram

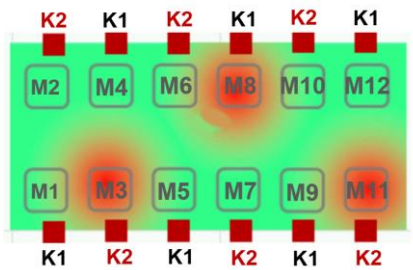

Figure 12. Switches configuration

4.2 Results

Considering the mission profile fig.10, Modelica simulations are performed to extract the junction temperatures of the components. In order to highlight the benefits of the proposed thermal model, two comparisons are conducted. First, the temperatures obtained by the uncoupled static model are compared with those obtained with a static coupled model. This comparison will highlight the impact of thermal coupling between the chips. Second, the temperatures obtained with the static coupled model are compared with those of the transient thermal coupled model to highlight the impact of the thermal inertia.

The first step is the comparison between the static compact thermal model with and without thermal couplings between the chips. Thus, a first simulation is achieved taking into account only the thermal resistance of the chips self-heating. A second simulation is performed using the static compact model with coupling points (fig.13).

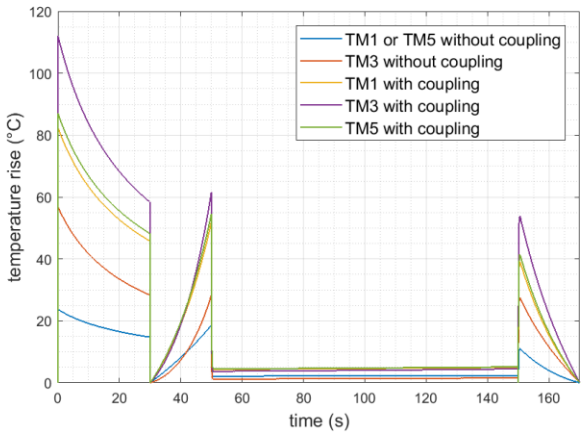

Figure 13. Junction temperatures comparison with and without coupling

The obtained temperatures show the important part of the mutual coupling between chips. Indeed the junction temperature of M1 reaches a maximum of 23.7°C without considering coupling while it rises to 82.4°C with coupling. These results show an increase of components temperature of about 60°C during the charging phase due to the coupling of nearby components and for a staggered configuration. The chips position on the module is also an important parameter to take into account. The optimization of components layout for a given application could be considered with this type of thermal modelling.

The second point of interest is the comparison of the results between the static and dynamic models with coupling (fig.14).

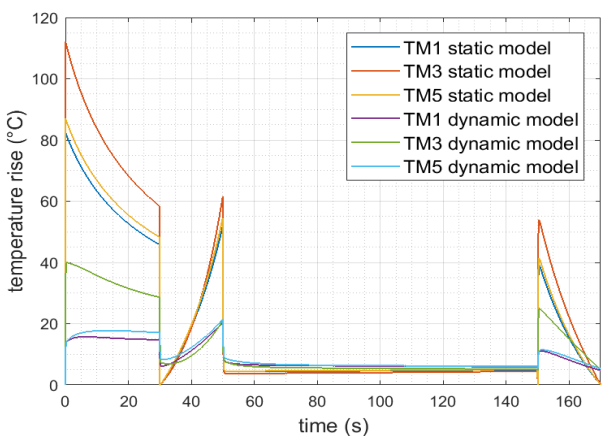

Figure 14. Junction temperatures comparison between static and dynamic model

The comparison of the junction temperatures for the static and dynamic models show the relevance to take into account the transient phase for short time operations. As an example, the the average overestimation error of the static model compared to the transient model for the junction temperature of M1 is about 70% and for M3 about 60% during the charging phase. In this case, it appears necessary to implement a dynamic

thermal modelling to avoid the oversizing of the power converter and in particular the heatsink. The prospects to improve the power converting system design should focus on the integration of the transient thermal modelling.

5 Conclusion

Considering a DC-DC power converter for supercapacitors to power an electric bus, the control of the junction temperatures is essential during transient phases of the charging of the supercapacitors. Taking into account this maximum power as steady state should lead to an oversizing of the cooling system. In this paper, a compact thermal model of the power module is extracted to fit the thermal responses of the chips and to ensure a satisfactory accuracy by taking into account their thermal coupling. The transient thermal model with a reduced number of elements and low computation time is designed to be implemented in an electro thermal simulator of the power converting system. Future works will concern the compact thermal model integration in the optimization to take benefit of thermal capacities and thus minimize the size and weight of the power converting system.

Acknowledgements

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