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TOP-DOWN FABRICATION OF VERTICAL NANOSTRUCTURED CHANNEL ARRAYS ON SIGE FOR FUTURE NANOELECTRONICS APPLICATIONS

J. Müller ^a, A. Lecestre ^a, R. Demoulin ^a, F. Cristiano ^a, J.-M. Hartmann ^b and G. Larrieu ^a

^a LAAS-CNRS, CNRS, Université de Toulouse, INP Toulouse, Toulouse, 31031, France.

^b CEA, LETI, Université Grenoble Alpes, Grenoble, 38000, France.

e-mail: jonas.mueller@laas.fr, guilhem.larrieu@laas.fr

In order to improve the performances of FET transistor devices, current designs are being scaled down. The top-down fabrication of vertical nanostructured channel array (VNCA) based devices is another option for a highly dense device integration, however [1]. With such a scheme, vertical nanowires or nanosheets can be integrated with a gate all around configuration, in order to enhance the immunity against short channel effects when the gate length is ultimately scaled [2]. A shift from Si substrates towards higher hole mobility SiGe, in order to boost the performances of pMOS devices, is also being considered [3].

Fabrication strategies for SiGe nanostructures mostly rely on reactive ion etching (RIE) with halogens e.g. F, Cl or Br [4]. A fluorine chemistry is best suited to have highly anisotropic etching profiles. While the etching of low Ge content ($x < 0.25$) $\text{Si}_{1-x}\text{Ge}_x$ nanowires has already been demonstrated [5], the fabrication of highly dense Ge-rich VNCAs remains challenging due to etch rate and anisotropy increases because of strong chemical interactions between SiGe and the etching gas. Here, we present progresses on the top-down fabrication of highly anisotropic and ultra-dense $\text{Si}_{0.8}\text{Ge}_{0.2}$ and Ge-rich $\text{Si}_{0.5}\text{Ge}_{0.5}$ VNCAs, compatible with wafer scale processing.

Dense arrays of nanowires (NW) and nanosheets (NS) were fabricated thanks to negative-tone resist hydrogen silsesquioxane (HSQ) masks and electron beam lithography with a Raith-150 system at 30 kV. Being mature for silicon [1], resist patterning remains challenging for high Ge contents as proximity effects limit the achievable NW density. By adjusting the nanostructure design, a common process window has been demonstrated independently of the Ge content. The resulting patterns were transferred onto the $\text{Si}_{1-x}\text{Ge}_x$ ($x = 0, 0.2, 0.5$) substrates by anisotropic RIE with a fluorine-based chemistry. While the HSQ mask provided a good chemical stability and high etching selectivity, the substrate's etch rate and form anisotropy depended on the Ge content and on the gases used (SF_6 and C_4F_8), as shown in Fig.1. By optimizing gas ratios, we succeeded in obtaining perfectly vertical nanowire profiles whatever the Ge content considered. Dense $\text{Si}_{1-x}\text{Ge}_x$ nanowire arrays (Fig.2) 200 nm high with densities of 331 $\text{NW}/\mu\text{m}^2$ for ($x = 0, 0.2$) and 83 $\text{NW}/\mu\text{m}^2$ for ($x = 0.5$) were achieved.

Dense Si nanosheet arrays with a line density of 17 $\text{NS}/\mu\text{m}$ (Fig.3a) were otherwise obtained. Nanosheets as thin as 14 nm were fabricated with a 54 nm spacing and a line density of 14 $\text{NS}/\mu\text{m}$ (Fig.3b). Equally thin nanosheets could be obtained on SiGe, as shown for $\text{Si}_{0.5}\text{Ge}_{0.5}$ in Fig.3c with a width as low as 16 nm.

Finally, a thermal oxidation step was used on these nanostructures, resulting in oxide shell/SiGe core heterostructures, either to create a thin gate oxide or to be used as sacrificial oxidation, scaling the NW dimensions and improving the surface quality by removing process-induced defects. First, oxidation growth rates have been investigated for various Ge contents. A wet-thermal oxidation at 850°C has been selected in order to obtain the same oxide thickness whatever the Ge content. These conditions have been used on VNCAs in order to investigate the impact of the nanostructured shape (NW or NS), size and Ge content on the oxide growth on $\text{Si}_{1-x}\text{Ge}_x$ VNCAs.

Results on the lithography, etching and oxidation of Si, $\text{Si}_{0.8}\text{Ge}_{0.2}$ and $\text{Si}_{0.5}\text{Ge}_{0.5}$ nanostructures as well as the structural characterization by transmission electron microscopy and by energy dispersive X-ray spectroscopy will be detailed.

- [1] Y. Guerfi, F. Carcenac and G. Larrieu, *Microelectronic Engineering* 110 (2013) 173-176.
- [2] G. Larrieu, Y. Guerfi, X. Han and N. Clement, *Solid-State Electronics* 130, pp. 9–14 (2017).
- [3] International Roadmap for Devices and Systems (IRDS), “More Moore”, IEEE (2021).
- [4] G. S. Oehrlein, Y. Zhang, G. M. W. Kroesen, E. de E. de Frésart and T. D. Bestwick, *Appl. Phys. Lett.* 58 (1991) 2252.
- [5] E. van Drift, T. Zijlstra, R. Cheung, K. Werner and S. Radelaar, *Microelec. Eng.* 23 (1994) 343-348.

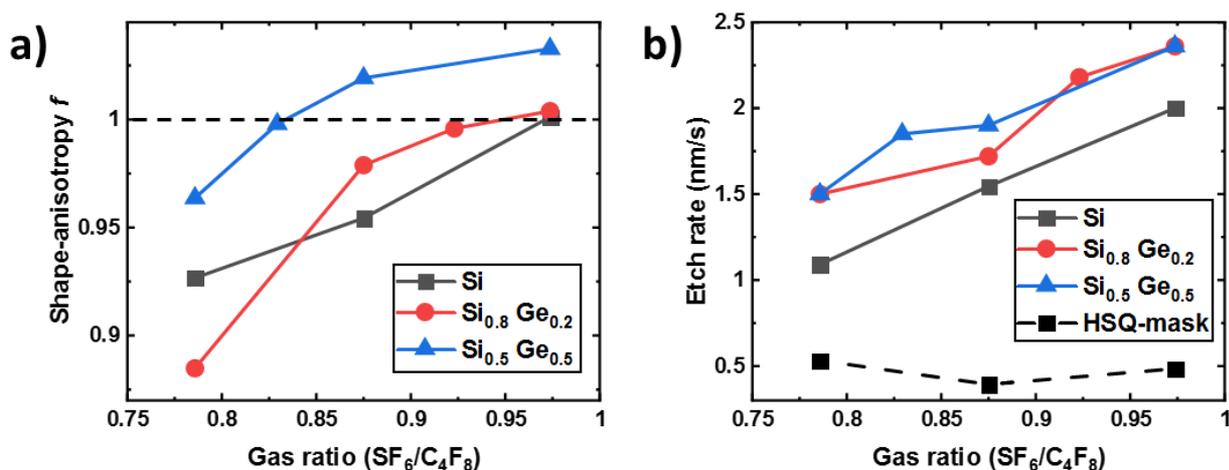


Figure 1. To achieve nanowires with perfectly straight sidewalls the fluorine-based gas mixture of the RIE etching process has been optimized to achieve shape-anisotropy factors f of 1 ($f = 1 - (d_{\text{etch,rel}}/2 h_{\text{etch}})$, h_{etch} being the nanowire height and $d_{\text{etch,rel}}$ the relative change of the nanowire diameter from top to bottom). $\text{Si}_{1-x}\text{Ge}_x$ form-anisotropy factors together with $\text{Si}_{1-x}\text{Ge}_x$ and HSQ mask etch rates are plotted against the (SF_6/CF_4) mass-flow ratio in (a) and (b), respectively.

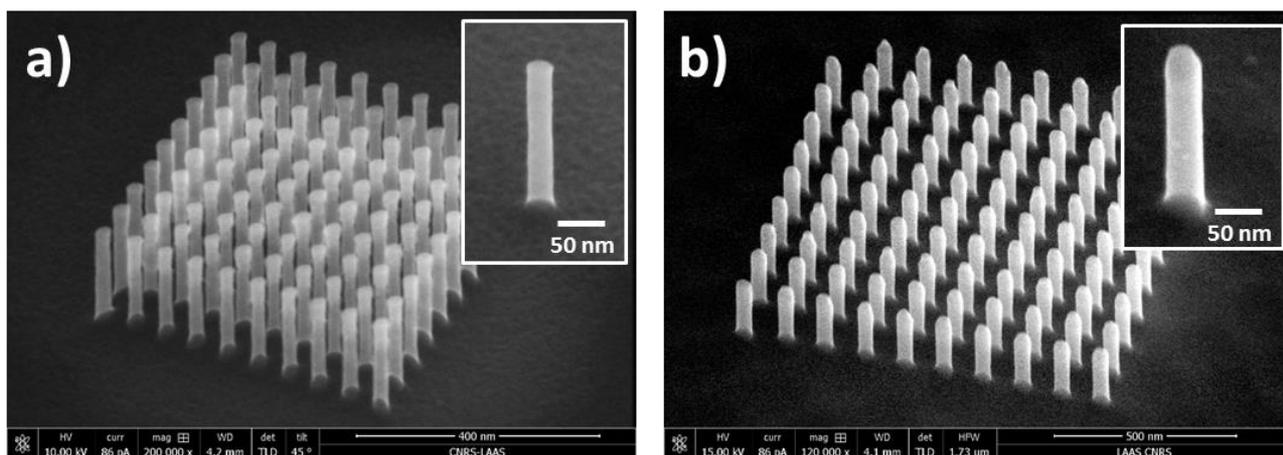


Figure 2. SEM images of dense and highly anisotropic ($f = 1$) Si & SiGe nanowire arrays fabricated thanks to a top-down approach and optimized RIE, resulting in 25 nm diameter silicon nanowires with a 20 nm spacing (a) and 45 nm diameter $\text{Si}_{0.5}\text{Ge}_{0.5}$ nanowires with a 65 nm spacing (b).

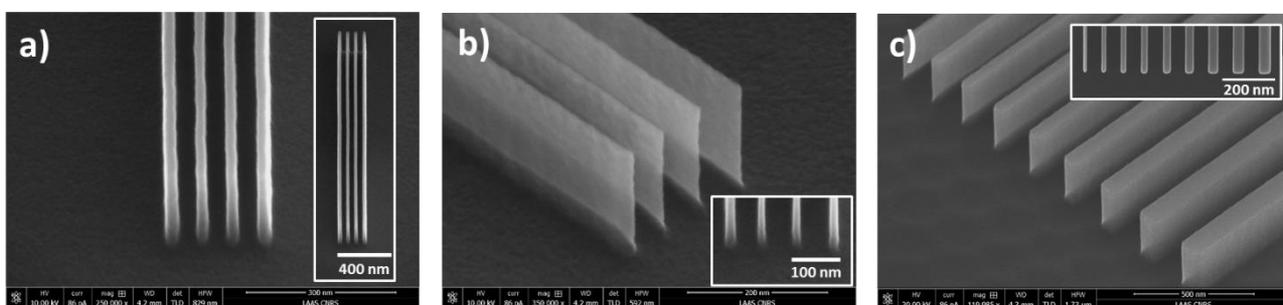


Figure 3. SEM images of highly anisotropic ($f = 1$) Si & SiGe nanosheets, 200 nm high and 2.1 μm long, fabricated thanks to a top-down approach and optimized RIE. Dense Si nanosheet arrays were achieved: 21 nm wide nanosheets with a spacing of 37 nm (a) and 14 nm wide nanosheets (14 nm) with a more relaxed spacing of 54 nm (b). Similar nanosheet widths (as low as 16 nm) were demonstrated on $\text{Si}_{0.5}\text{Ge}_{0.5}$ (c)