ADVANCES IN TOP-DOWN FABRICATION AND PROCESSING OF VERTICAL SIGE NANOWIRE ARRAYS FOR FUTURE NANOELECTRONICS APPLICATIONS

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In order to improve the performance of FET transistor devices current designs are being scaled down whereas vertical nanowire array (VNA) based devices, fabricated through a top-down approach, present a straightforward option for a highly dense device integration [1]. In addition, especially for CMOS devices, technology is shifted from using Si-substrates towards the higher mobility SiGe, which is needed to enhance their performance [2]. Here, we present the current progress on the top-down fabrication of ultra-scale dense VNAs on SiGe as demonstrated on commonly used Si_{0.8}Ge_{0.2} and Gerich Si_{0.5}Ge_{0.5}. Highly dense arrays of nanowires and nanosheets have been created as a negative-tone resist masks of hydrogen silsesquioxane through electron beam lithography using a Raith-150 system at 30 kV. Being well-established for silicon [1], the fabrication remains challenging for higher Gecontents as proximity effects limit the achievable NW density. By adjusting the nanostructure design, a common process window has been demonstrated independently of the Ge-content. The obtained patterns were transferred onto the $Si_{1-x}Ge_x$ (x = 0, 0.2, 0.5) substrates by anisotropic reactive ion etching (RIE) with fluorine-based chemistry. By tuning the gas mixture's ratio, we demonstrated the generic approach of the process to achieve a perfectly vertical nanowire profile whatever the Ge-content considered. Dense Si_{1-x}Ge_x nanowire arrays (Fig.1) of 200 nm height with densities of 331 NW/ μ m² for (x = 0, 0.2) and 83 NW/µm² for (x = 0.5) were achieved. Finally, a thermal oxidation step has been introduced to these nanostructures, forming an oxide shell/SiGe core heterostructure, either to create a thin gate oxide or to be used as sacrificial oxidation, scaling the NW dimension and improving the surface quality by removing process-induced defects. Results on the lithography, etching and oxidation of Si, Si_{0.8}Ge_{0.2} and Si_{0.5}Ge_{0.5} nanostructures as well as the structural characterization by transmission electron microscopy and by energy dispersive X-ray spectroscopy will be discussed in detail.



Figure 1: SEM images of highly dense Si- & SiGe-nanowire arrays fabricated by a top-down approach resulting in a 20 nm spacing as presented for silicon nanowires with 25 nm diameter (a) and 65 nm spacing for 45 nm Si_{0.5}Ge_{0.5} nanowires (b). To achieve nanowires with perfectly straight sidewalls the fluorine-based gas mixture of the RIE etching process has been optimized to achieve form-anisotropy factors of f = 1, corresponding data is shown in (c).

References:

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