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A fast and efficient Model Extraction Method to predict the transient Response of ESD Protection Devices

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Abstract— *ElectroStatic discharge (ESD) protection devices have non-linear and complex behavior that makes system level design robustness predictions complex. To obtain a precise simulation, a model reproducing the turn-on behavior is needed. In this paper we propose a complete measurement and computation setup to get access to an equivalent frequency model of devices under strong pulse injection. To validate our proposed frequency model a comparison of measurements and simulations is performed on passive and linear components first, then on a protection device (TVS).*

Keywords—*S parameter, TLP, system level ESD, modelling, EFT, protection device*

I. INTRODUCTION

Embedded systems are using more and more computations and high-frequency communications. All these electronics products are constituted by complex integrated circuits (IC) that have to survive harsh environments, which induced Fast Electrical Transient (EFT) like electrostatic Discharge (ESD). System designers have to consider security requirements to ensure that systems survive any stress that occurs. Designers must predict the robustness against system level ESD up to some kV as defined by [1].

Building accurate models for system level ESD is not an easy task [2]. One of the most related problem is to have correct models that take into account the dynamic behavior, such as the protection device's triggering behavior to obtain a good estimation of the over-voltages [3] [4].

Passive components and protection devices mounted on Printed Circuit Board (PCB) exhibit strong non linearities when they are exposed to EFT reaching kVs. To build accurate models, we need dedicated parameters extracted from measurements with high frequency bandwidth (up to few GHz) and high-power injection (in the order of some kV and tens of Amps). A conventional measurement technique to characterize protection devices without damaging the devices, is the Transmission Line Pulse (TLP) [5]. Using this generator, some authors have proposed dynamic models for protection devices [4,6,7], but the models are based on measurement using both voltage and current probes, which are frequency limited, and can be used only in time domain. The models are generally SPICE models, which could be difficult to build and implement. In this paper, we propose a black box model that can be used both in time and frequency domains

based on the response of the Device Under Test (DUT) to a strong pulse injection. The method is based on the use of TLP generator to reach high power injection combined with Time Domain Reflectometry (TDR) (Fig1), as introduced in [8] In this paper, we propose a different measurement and calibration set-up. The proposed set-up uses only one voltage probe and no current probe, which may have bandwidth limitation, as suggested in [8,9]. From TLP-based TDR measurements TLP an equivalent S parameter model is obtained assuming a Linear Temporal Invariance (LTI). This assumption has been addressed in paper [9] for protection devices.

The whole setup as well as dedicated calibration technique and computation to obtain the frequency model is presented in section II. In section III, the method is validated on linear devices, and comparisons are performed. S11 parameters obtained with our TLP-based TDR method are compared with VNA measurements under low-level injections. For higher level pulse injections, simulations are performed into the time domain using the S11 obtained with the proposed method, and compared to transient measured waveforms to validate the relevance of the extracted model. In Section IV, a frequency model with non-linearities depending on the power injection is presented to build the model of a Transient Suppressor Voltage (TVS). Time domain simulations are performed showing a good agreement between the time domain measurement and the simulation using our frequency models. Finally, Section V is dedicated to the conclusion and presents some perspectives for better prediction results.

II. PRINCIPLES OF MODEL EXTRACTION METHOD

A. TLP-based TDR measurement method

The aim of this method is to obtain a frequency model of a two-terminal protection device (e.g. filtering capacitor, TVS). Here, a black-box modelling is used, based on the measurement of the reflection coefficient of a load impedance through TDR method [10].

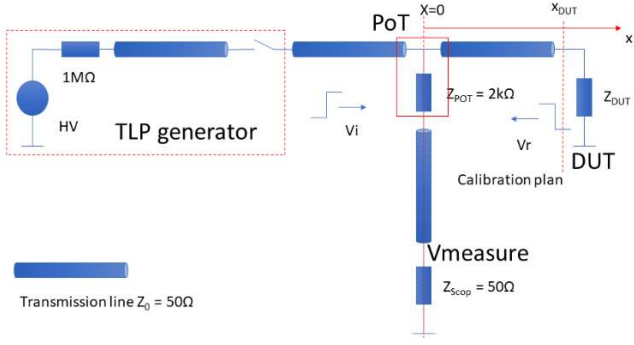


Fig. 1. Schema of TDR measurement method

The TDR method principle, illustrated in Fig 1. is based on the injection of a forward voltage V_i , which is reflected as V_r , by the terminal load impedance Z_{DUT} . The measurements of V_i and V_r allow to compute the transient impedance (1), where Z_0 is the characteristic impedance of the cable that drives V_i .

$$\Gamma(x_{DUT}, t) = \frac{Z_{DUT}(t) - Z_0}{Z_{DUT}(t) + Z_0} = \frac{V_r(x_{DUT}, t)}{V_i(x_{DUT}, t)} \quad (1)$$

The pulse is generated by a TLP generator [5]. A Pick-off Tee (PoT), linked to an oscilloscope, is used to measure the voltage on one point of the line ($x=0$). All the lines between the different elements are 50Ω adapted. Forward and reflected voltages overlap in the transmission lines as reported in Fig.1. The measured voltage V_m at a given distance x is defined by (2).

$$V_m(x, t) = V_i(x, t) + V_r(x, t) \quad (2)$$

The time delay between V_r and V_i is computed in relation with the distance between DUT and the PoT, and the propagation speed in lines. This delay leads to a complex transient waveform for an unmatched load as shown in Fig. 2.

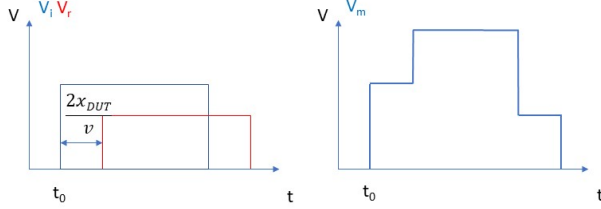


Fig. 2. Example of TDR waveform for an unmatched load

Having V_m , one has to separate V_i and V_r to be able to compute the reflection coefficient. A calibration method is needed to extract V_i independently of the connected load, at the output of the TDR. A matched load Z_0 is used instead of Z_{DUT} to cancel V_r and ensure that $V_m = V_i$. Setup parameters and the charge voltage level of the TLP are the same than those used to measure V_m on Z_{DUT} . As shown in (2), V_i and V_r are separated, to obtain a measurement of the impedance.

The TDR gives either the transient reflected coefficient or impedance of the DUT. The spectrum of V_i and V_r are computed from a Fourier transform, in order to obtain the reflection coefficient or S parameter in frequency domain (3).

$$S_{11}(x_{DUT}, f) = \frac{Z_{DUT}(f) - Z_0}{Z_{DUT}(f) + Z_0} = \frac{V_r(x_{DUT}, f)}{V_i(x_{DUT}, f)} \quad (3)$$

B. Calibration method

The aim of calibration is used for de-embedding the S parameter measured at the PoT level (4) to move the calibration plane at the DUT (3) input. This calibration process also compensates all the imperfections and error sources (e.g. imperfect TLP output matching, cable and PoT attenuation, ...). This method is detailed in [11].

$$\begin{cases} V_{PoT} = V_i(0, f) + V_r(0, f) \\ S_{PoT}(0, f) = \frac{V_r(0, f)}{V_i(0, f)} \end{cases} \quad (4)$$

S_{11} is seen through a quadrupole error. It can be extracted from S_{PoT} through (5) and (6). The terms e_{xx} are the elements of an error coefficient matrix [E], which are extracted by a series of three measurements on reference loads. The error coefficient matrix [E] is computed according to (7).

$$S_{11} = \frac{S_{PoT} - e_{00}}{\Delta e - e_{11}S_{PoT}} \quad (5)$$

$$\Delta e = e_{10}e_{01} - e_{00}e_{11} \quad (6)$$

$$[S] = [M][E] \quad (7)$$

Where [S] (8) contains the S parameters obtained by TLP-based TDR measurement done at the PoT. [E] (9) is error coefficient matrix and [M] a matrix shown in (10). [E] is obtained by solving (7).

$$[S] = \begin{pmatrix} S_{PoT 50\Omega} \\ S_{PoT open} \\ S_{PoT short} \end{pmatrix} \quad (8)$$

$$[E] = \begin{pmatrix} \Delta e \\ e_{00} \\ e_{11} \end{pmatrix} \quad (9)$$

$$[M] = \begin{pmatrix} S_{VNA 50\Omega} & 1 & S_{PoT 50\Omega}S_{VNA 50\Omega} \\ S_{VNA open} & 1 & S_{PoT open}S_{VNA open} \\ S_{VNA short} & 1 & S_{PoT short}S_{VNA short} \end{pmatrix} \quad (10)$$

C. Model extraction method algorithm

The method presented above was implemented with an algorithm coded with the software Matlab. Its principle is described in Fig. 3.

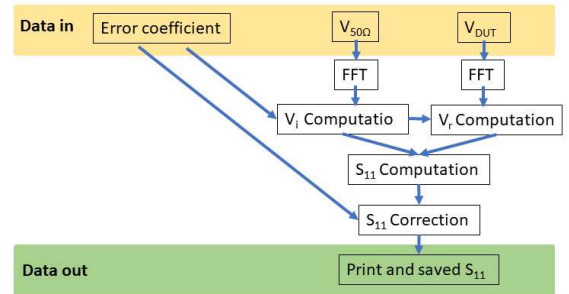


Fig. 3. Flow diagram of the model extraction method

The algorithm has two types of data inputs. The first type consists in error coefficients, as computed in the previous part. The second type is a series of two voltage measurements, one on a matched load (to extract V_i), and the second on the DUT

load (Z_{DUT}). The output is the S parameter of the load, eventually converted in impedance Z_{DUT} , given as a Touchstone. s1p file, which can be directly imported as black-box model in electrical simulator such as ADS.

IV. VALIDATION OF THE PROPOSED APPROACH ON PASSIVE LINEAR LOADS

A. Experimental set-up

To validate the method, the impedance of several passive loads, whose component specifications are listed in Table II. The whole component setup of the TLP-based TDR is listed in Table I. The duration of the pulse generated by the TLP is 100 ns and the rise time is equal to 100 ps. For linear components, impedance is measured by a Vector Network Analyzer (VNA), so as to get a reference impedance.

TABLE I. MATERIAL SPECIFICATIONS

Material	Reference	Specification
TLP	HPPI TLP8010C	$V_{max}=4kV$ $I_{max}=80A$ $t_r=100ps$ Adapter 50Ω
PoT	PT-45A	$Z_{PoT}=2.2k\Omega$ BW=18GHz
Oscilloscope	Tektronix DPO71254C	100GS/s BW=12GHz

TABLE II. TESTED COMPONENT SPECIFICATIONS

Component	Reference	Specification
Resistor 2R	Yageo RC0805FR-072RL	2Ω , 0.125W
Resistor 470R	TE Connectivity CRG0805F470R	470 Ω , 0.125W
COG capacitor	Vishay VJ0805A102JXBAT	1 nF, $V_{max} = 100V$
TVS	Nexperia PESD5V0L1BA 115	$V_t=7V$ $P_{max}=500W$

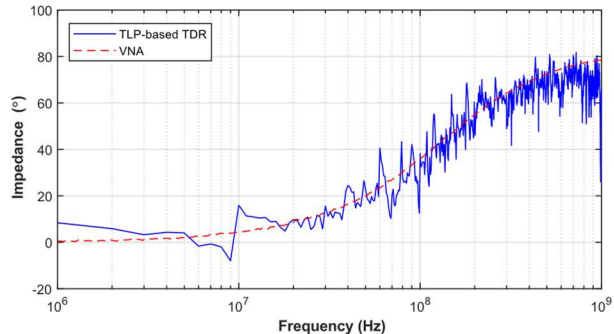
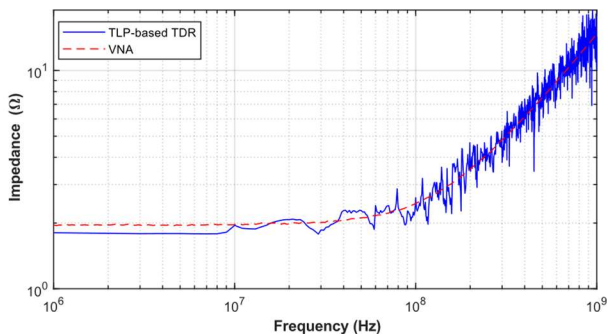
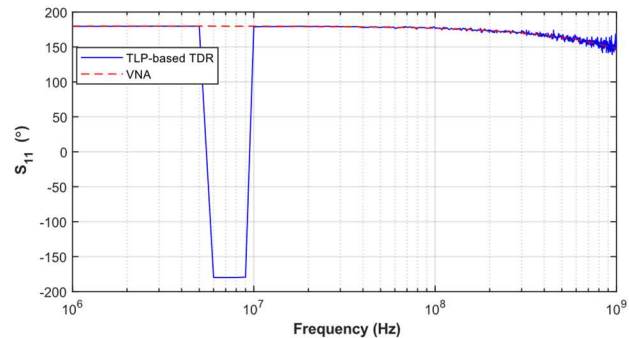
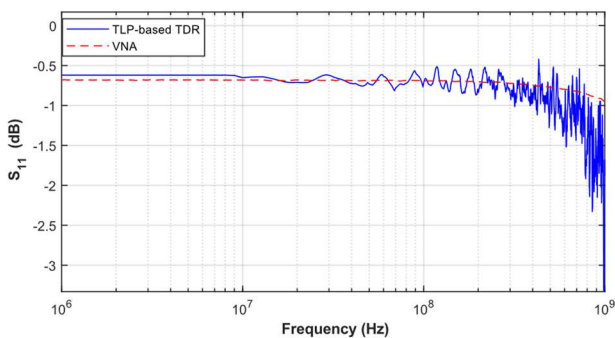


Fig. 4. Comparison between VNA and TLP-based TDR measurements on the 2Ω load

In a first step, components were tested to determine their breakdown voltage. The limit is set so as to have a perfect linear regime and prevent any drift of characteristics due to accelerated aging. The limit is set at 500 V.

B. Results

1) 2Ω load

The 2R resistance is a good representation of an activated ESD protection. Fig. 4 shows the module and phase of S parameter and the impedance extracted with the TLP-based TDR at 100V measurement, and the VNA measurements.

The impedance of the 2R extracted by TLP-based TDR measurement fits well with VNA measurement up to 1 GHz. Above that level, frequency noise appears. This noise is largely due to the large bandwidth of the oscilloscope and also by the limited time rise. Considering a trapezoidal pulse form, the time rise being 100 ps, the spectrum extends up to 3.5 GHz. The extension of the bandwidth needs a faster pulse. A part of the noise is also due to calibration errors.

2) 470Ω load

The 470R resistance behaves as a non-activated or beginning-activated protection. Fig. 5 presents only the module of the impedance under 100 V pulse. For all the next measurements presented only the resulted impedance from computation will be presented.

As in the previous case, the TLP-based TDR fits well with VNA measurement. The main difference is the frequency noise at high frequency. We'll discuss about this noise effect in the next part.

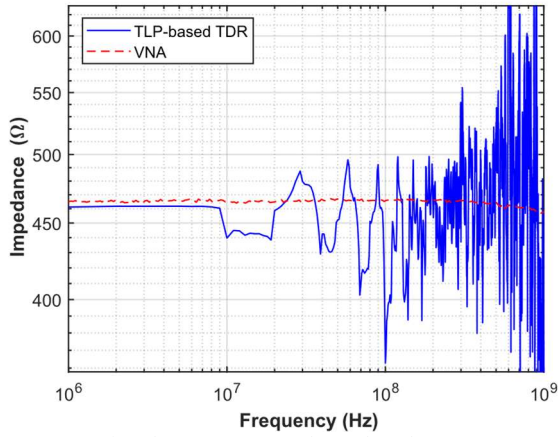


Fig. 5. Comparison between VNA and TLP-based TDR measurements on the 470Ω load

3) COG dielectric capacitance

COG dielectric is an extremely stable capacitor, leading to a linear behavior. Its properties do not vary with voltage.

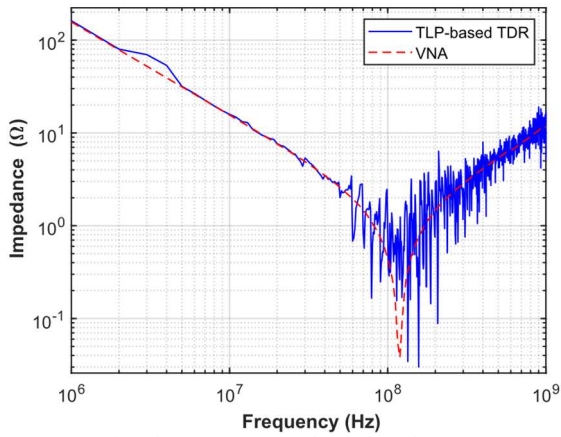


Fig. 6. Comparison between VNA and TLP-based TDR measurements on the 1 nF COG capacitor

As well as for the previous resistive loads, TLP-based TDR measurements, in Fig. 6, fits very well with VNA measurements. Between 1MHz and 1GHz, the gap is under 1%. The resonance peak is different between TDR-based TLP (ESR is 200 mΩ) and the VNA (ESR is 40 mΩ). The frequency noise is significant in this part.

C. Validation of the simulated transient behavior

A second step of validation is to compare transient measurements and simulations issued from the component model extracted from TLP-based TDR. The simulations were made with Advanced Design System (ADS) software. For linear devices, two parallel simulations were also made using S parameter from TLP-based TDR measurement and from VNA measurement. These measurements are loaded in a « S1P » box. The TLP electrical model is provided by the TLP manufacturer and has been validated through comparison with measurement on calibration loads. The schematic simulation including the TLP, the PoT and the load under test is described in Fig. 7

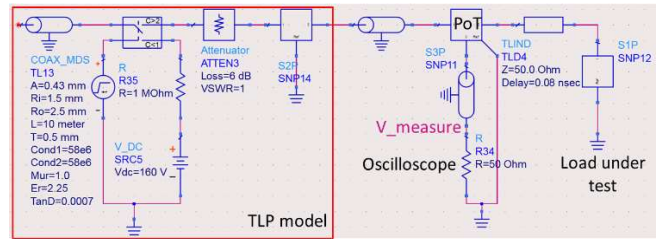


Fig. 7. Schema of electrical simulation

In Fig. 8, the measurement of the voltage under 100 V pulse for 470R load is compared to the simulations based on the models extracted either with TLP-based TDR or VNA.

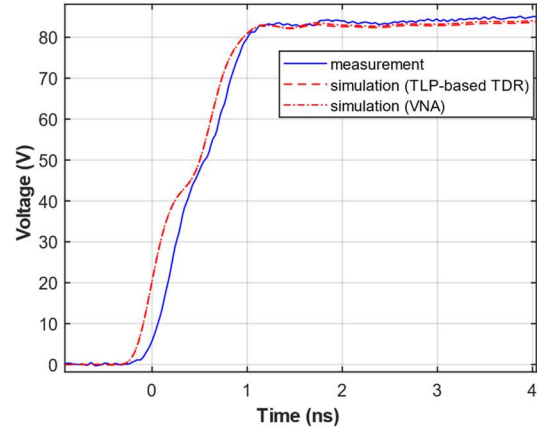


Fig. 8. Transient measurement vs two simulation with the tow model for 470Ω load

The measured and simulated voltages in steady-state regime are identical. During the transient regime, the first part of the rising transition is modeled correctly. The gap in the transient part is 3% for both TLP-based and VNA extracted models. The plateau at 50V is equal to V_i and its duration is due to the time delay introduced by the connector and the short PCB trace. The estimated overshoot with both models is in excellent agreement with the measured one. The influence of the frequency noise is not seen in this case.

The second case study concerns the COG capacitor. The measured and simulated transient waveforms are shown in Fig. 9. A good match appears between the measurement and the simulation results obtained from TLP-based TDR and VNA extracted models. The maximum gap between the measured and simulated waveforms is 11%. One can notice that the gap between measurement and simulation is larger with the component model extracted with the VNA.

In spite of a larger noise on the extracted impedance in the frequency domain, the measurement of the TLP-based TDR measurement enables one to simulate correctly the transient response of linear load under a high voltage pulse.

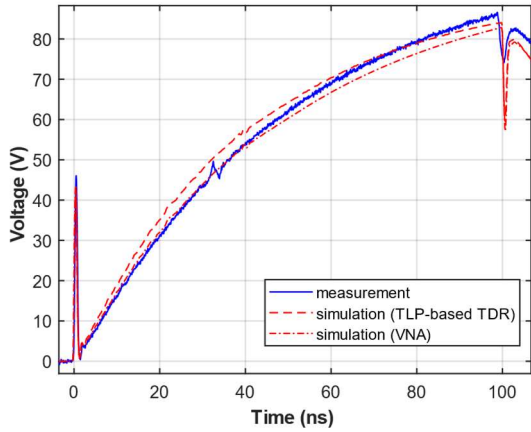


Fig. 9. Transient measurement vs simulation for C0G capacitor load

V. CHARACTERIZATION AND MODELLING OF NON-LINEAR PASSIVE LOAD

In this part, a passive non-linear load (i.e. its behavior changes with the applied voltage) is characterized with TLP-based TDR in order to extract a model for the transient simulation. The TVS whose characteristics are given in Table II is used as case study. In this part, the relevance of the linear assumption on which the proposed modeling approach relies is tested. Because of its non-linear behavior the VNA measurement cannot be used as a reference. To have a first understanding of its behavior, a quasi-static I(V) curve is necessary (Fig. 10).

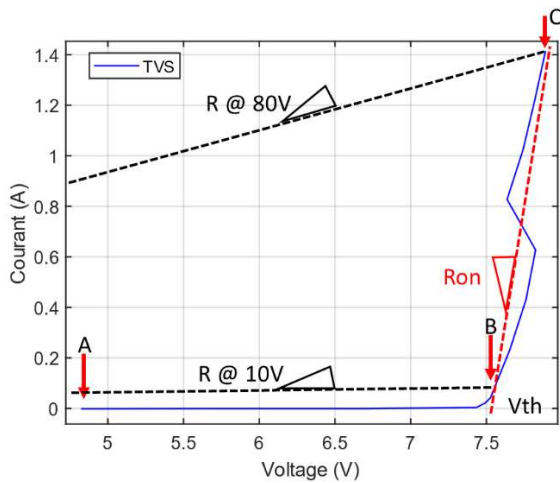


Fig. 10. I(V) curve for the TVS

A. Extraction of the impedance of the TVS

Below the triggering voltage $V_{th} = 7.5$ V, the protection is not activated leading to a very high impedance (Open). Above V_{th} , the protection is activated and its equivalent impedance R_{on} is 0.35Ω .

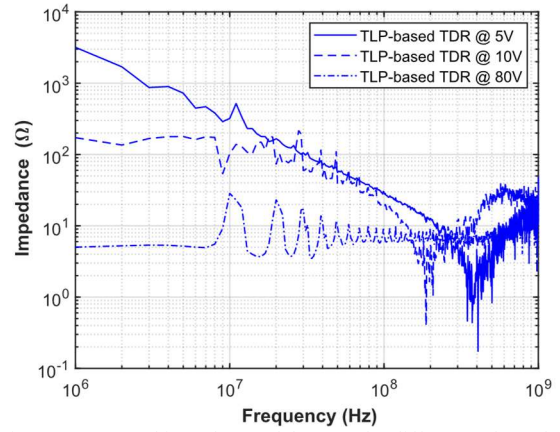


Fig. 11. Measured impedance of the TVS for different pulse voltage

Three measurements of the TVS impedance are given in Fig. 11.

- The measurement at 5 V is done below V_{th}
- The measurement at 10 V is done, just above V_{th}
- The measurement at 80 V is done when the protection is fully activated

The three impedance curves are different below 600 MHz. For pulse voltage less than V_{th} , TDR@5V, the measurement shows that the TVS has a capacitive behavior, with an equivalent capacitance of 63 pF. It is consistent with the value of 70 pF given by the datasheet. For pulse amplitude close to V_{th} , TDR@10V, the precision in low frequency seems better. B the operating point (reported in Fig. 10), obtained for 10 V injection, is given at 7,6V with 0.05 A. This exhibits an equivalent quasi-static resistance of 160Ω , while the estimation from the quasi-static I(V) curve (Fig. 10) is around 152Ω , resulting in an error of only 5%. For 80V injection, following the same way of thinking, the operation point (C) is at 7,8V for 1.4A. It leads to equivalent quasi-static resistance of 5.6Ω , versus 5.3Ω obtained with our TLP-based TDR measurement.

A last interesting observation can be done from the results shown in Fig. 11. Above 600 MHz, the measured impedance profiles are identical whatever the TLP pulse amplitude. The impedance is dominated by the TVS parasitic inductance which is constant whatever the pulse amplitude. We can expect that the initial transient response of the TVS to a fast pulse will be dominated by this parasitic inductance. Moreover, the linear assumption on which relies the proposed modeling approach should be acceptable to model the first nanosecond of the transient response.

B. Comparison measurement vs simulation of the transient behaviour

The first step consists in simulating the behavior of the TVS before the triggering voltage. Fig. 12 shows the comparison between the measured TVS response at 5 V and the simulation from the TLP-based TDR extracted model.

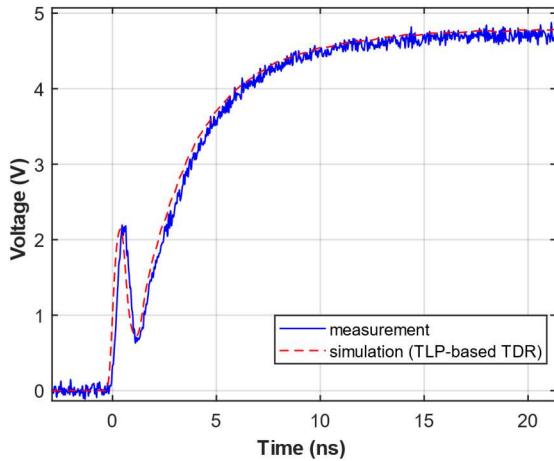


Fig. 12. Transient measurement vs simulation of TVS for 5V TLP pulse

The curve given by the simulation is similar to the measured curve. The quasi-static level is exact at more or less 1%. The charge time is reproduced correctly.

Fig. 13 shows the comparison between measurement and simulation of the TVS transient response for 80 V TLP pulse. Fig. 13 shows a good fit between measurement and simulation. First, the quasi-static level merges with the measurement. The simulated and measured initial transient behaviors are similar. In spite of the linear assumption behind the extracted TVS model, the dynamic response of the transient trigger TVS is correctly represented, especially the magnitude of the initial overshoot.

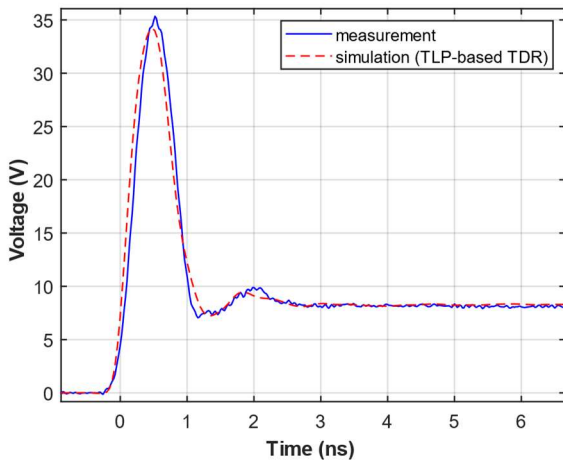


Fig. 13. Transient measurement vs simulation of TVS for 80V TLP pulse

VI. CONCLUSION

This paper has presented a TLP-based TDR method to facilitate the construction of ESD protection device models, in order to simulate their transient response to high voltage fast pulses. The proposed model is based on S-parameter black-

box macromodels that can be directly imported in SPICE simulator, without any tedious and time-consuming model fitting phase. The method has been validated on several passive linear loads. Although the proposed method relies on the LTI assumption, a validation case study on a TVS confirms that the transient response of such a non-linear device can be simulated with an acceptable precision.

Further works are necessary to confirm the validity of the approach on other protection components with non-linear behavior under large injection regime (e.g. X7R ceramic capacitor, choke). Moreover, the presented work was only focused on two-terminal devices and should be extended to devices with a larger number of terminals, in order to cover integrated circuit or common-mode chokes. Finally, a complete validation of the method requires to simulate a complex filter made of several devices modeled according to the proposed approach.

REFERENCES

- [1] "IEC 61000-4-2:1995, Electromagnetic compatibility (EMC), Part 4-2: Testing and measurement techniques, Electrostatic discharge immunity test," 1995.
- [2] White Paper 3, System Level ESD, Part 1, Industry Concil ESD Target Levels, 2011
- [3] M. P. J. Mergens, M. T. Mayerhofer, J. A. Willems, and M. Stecher, "ESD protection considerations in advanced high-voltage technologies for automotive," in *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, 2006.
- [4] F. Escudié, F. Caignet, N. Nolhier, and M. Bafleur, "From quasi-static to transient system level ESD simulation: Extraction of turn-on elements," *Electr. Overstress/Electrostatic Disch. Symp. Proc.*, vol. 2016-October, no. 1, 2016
- [5] ANSI/ESD STM5.5.1, ESD Association Standard, "Test Method for Electrostatic Discharge (ESD) Sensitivity Testing - Transmission Line Pulse (TLP) - Component Level" ANSI/ESD STM5.5.1-2016.
- [6] G. Notermans, H.-M. Ritter, S. Holland, ; D. Pogany, "Dynamic Voltage Overshoot During Triggering of an SCR-Type ESD Protection", *IEEE Transactions on Device and Materials Reliability*, Vol 19, I 4, pp 583-590, Dec 2019.
- [7] J. S. Meiguni et al., "Transient Analysis of ESD Protection Circuits for High-Speed ICs," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 63, no. 5, pp. 1312-1321, Oct. 2021.
- [8] R. Gillon, M. Vanden Bossche, F. Verbeyst, "The application of large-signal calibration technique yields unprecedented insight during TLP and ESD testing", 2009 31st EOS/ESD Symposium, 2009, pp 1-7.
- [9] F. Escudié, F. Caignet, N. Nolhier, A. Boyer, "Frequency Based Method Investigation to Extract an ESD Protection Dynamic SPICE Model From TLP Measurement", *IEEE Transactions on Electromagnetic Compatibility*, Early Access, pp. 1-11, October 4th 2021, 10.1109/TEM.2021.3106770
- [10] H. Fellner-Feldegg, « Measurement of dielectrics in the time domain », *J. Phys. Chem.*, vol. 73, no 3, p. 616-623, mars 1969, doi: 10.1021/j100723a023.
- [11] « Uncertainty analysis of the weighted least squares VNA calibration ». <https://ieeexplore-ieee-org-s.docadis.univ-tlse3.fr/document/1427566/>.