

Chip or Wafer – Small quantity fabrication

Shun Yasunaga^{1*}, David Bourrier², Naonobu Shimamoto¹,
Ayako Mizushima¹, Hugues Granier², and Yoshio Mita^{1,c}

¹The University of Tokyo, 7-3-1 Hongo, Bunkyo-city, Tokyo, Japan

²LAAS-CNRS, Université de Toulouse, CNRS, Toulouse, France

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Abstract:

In the academic research activities in the cleanroom, where mass production is rarely required or substrate to be processed is sometimes limited in size, devices are often fabricated using diced chips rather than wafers. However, such fabrication often struggles to maintain quality, in part because of inhomogeneity on the small chip and the different chip size among users, which requires process optimization for each. One possible solution is to standardize processing chips attached to or embedded in a dummy wafer.

Electroplating is one of the processes whose homogeneity is affected by the sample's geometry [1,2]. To see the feasibility of electroplating on chip using a wafer, we tested copper electroplating on a chip attached on 4" wafer. We prepared 20 mm square silicon chips, on which copper was sputtered by 50 nm as seed layer and positive tone photoresist JSR7790G (thickness = 1 μm) was patterned. Then we affixed the chip on a gold-sputtered 4" silicon wafer using conductive tape. After process optimization, we obtained the results shown in Fig. 1. The result that the whole wafer surface was plated implies more parallel current near the chip during the process, resulting to a better homogeneity.

Practically, other factors must be considered for agile development and smooth administrative operations, such as cost and maintenance frequency. The preparation of the dummy substrate must also be carefully done for the processes. Still, using on-wafer process of chips as standard can be effective for quality, efficiency, and reproducibility in the fabrication of test devices of small quantity.

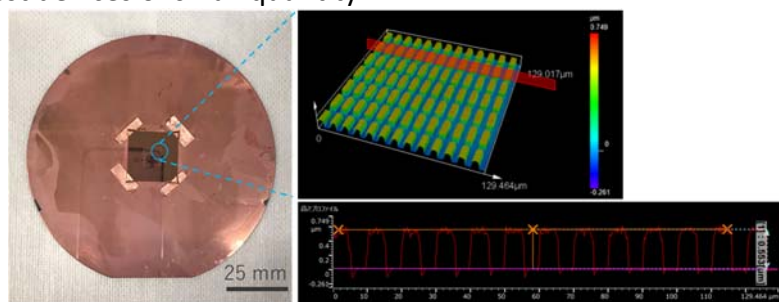


Fig. 1. Results of copper electroplating using 4" wafer

References:

- [1] N. Obaid, R. Sivakumaran, J. Lui, and A. Okunade, Proceedings of the 2013 COMSOL Conference, Boston, (2013)
- [2] D. Chen, et al., Surface and Coating Technology, vol. 455, article no. 129178, (2023)

*Presenting Author: S. Yasunaga.

^c**Corresponding author:** Yoshio Mita (MEMS@if.t.u-tokyo.ac.jp); 7-3-1 Hongo, Bunkyo-city, Tokyo, Japan

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