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Investigation of BV_{dss} instability in trench power MOSFET through DLTS, electrical characterization and TCAD simulations

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Abstract— In this paper, we investigated the drain to source breakdown voltage (BV_{dss}) instability during avalanche current drain stress of Shielded Gate MOSFET (SG-MOSFET) structure and we propose a new methodology to correlate electrical results to TCAD simulations. The presence of positive charged states at the Field Plate (FP) oxide/Si interface was confirmed by Capacitance-Deep Level Transient Spectroscopy (C-DLTS). Thus, it was implemented in TCAD simulations that predict the experimental behavior of two architectures. Thanks to these results, walk-in contributors were discriminated to suggest a pathway to increase device robustness with a slight R_{on} impact.

Keywords—Shielded Gate MOSFET, BV_{dss} walk-in, DLTS, TCAD

I. INTRODUCTION

The constant performance improvement in power applications lead to the Shielded Gate MOSFET (SG-MOSFET) structure (Fig. 1(a)) which allows to reach unprecedented specific ON-state resistance (R_{on}) vs. drain to source breakdown voltage (BV_{dss}) [1]. This structure exploits the Field Plate (FP) electrode to obtain a uniform distribution of the electric field along the drift region that can be less resistive for the same sustained BV_{dss} (Fig. 1(b)) [1]. However, this structure suffers from BV_{dss} instability also known as walk-in phenomenon during avalanche current drain stress [2]. This device exhibits a

BV_{dss} lowering when the structure reaches the avalanche regime. This is a major product reliability issue as they must keep their characteristics for several years. This phenomenon has been studied by several research groups and attributed to a dynamic process of hot holes injection during avalanche current stress which destabilizes the sensitive charge balance of the SG-MOSFET structure [2], [3].

In this paper, we present the C-DLTS results as evidence of positive charged states at the FP oxide/Si interface after manufacturing process. From those results, the simulations set-up allows us to predict the behavior of the device at two different stages: primarily at the first electrical BV_{dss} characterization (from now on called virgin state); secondly during the following ones (from now on called degraded state). Following this study, we propose to examine the influence of FP polarization and gate depth. To conclude, we list few actions to increase device robustness with reduced impact on R_{on} .

II. C-DLTS ANALYSIS

Capacitance deep level transient spectroscopy is a powerful characterization method to show the presence of deep trap levels in the forbidden energy band gap. The analysis was performed with a PhysTech FT 1230 HERA-DLTS equipment on an n-type trench MOS capacitance (Fig. 2(a)). The sample has been attached to its holder with a special ceramic paste to assure a homogeneous thermic contact in a cryostat chamber. The latter was connected to a liquid nitrogen pump that allowed to decrease the temperature down to 85 K. The resulting spectrum of first order Fourier sine coefficient (b_1) vs. T showed two peaks around 285 K and 310 K (Fig. 2(b)). According to [4], a positive peak behavior during a temperature sweep is distinctive of a trap deep level for majority carriers at the SiO_2/Si interface. The equipment allowed to collect a capacitance transient at each temperature and, for each transient, it extracted the emission time constant (τ). The emission rate e , i.e. the inverse of τ , is linked to the activation energy of the deep level through eq. (1) [4]:

$$e \propto T^2 \exp(-E_a/K_B T) \quad (1)$$

Therefore, the activation energies E_a of the deep levels have been extracted from the slopes of the Arrhenius plot and correspond to 0.6 eV and 0.3 eV. According to [5], these states in the forbidden energy band gap correspond to Si dangling

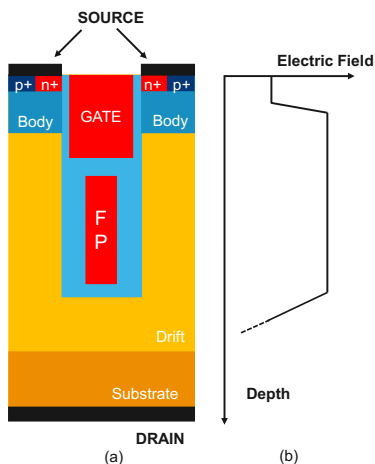


Fig.1: (a) SG-MOSFET structure; (b) inter trenches electric field.

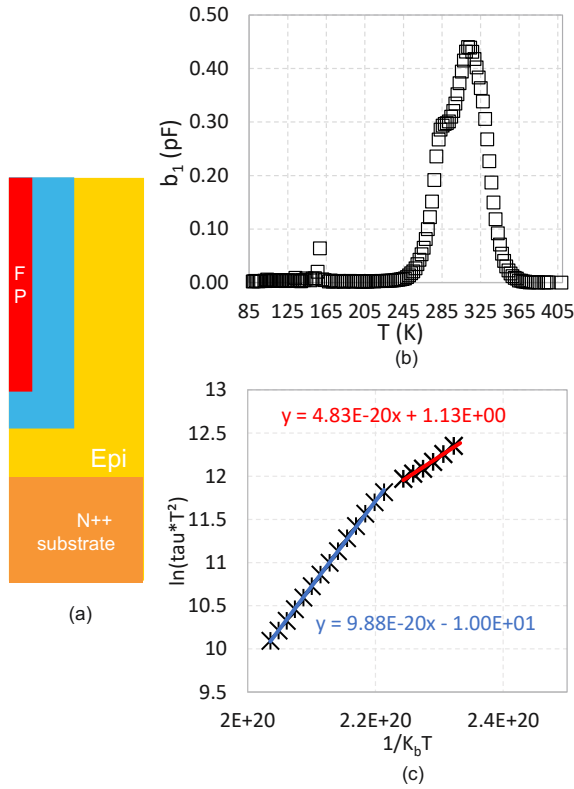


Fig. 2: (a) C-DLTS characterization was performed on a MOS structure; (b) the resulting spectrum; (c) deep levels activation energies are extracted from the slopes of the straight lines displayed in the Arrhenius plot [$\ln(\tau \cdot T^2)$ vs. $1/K_b T$].

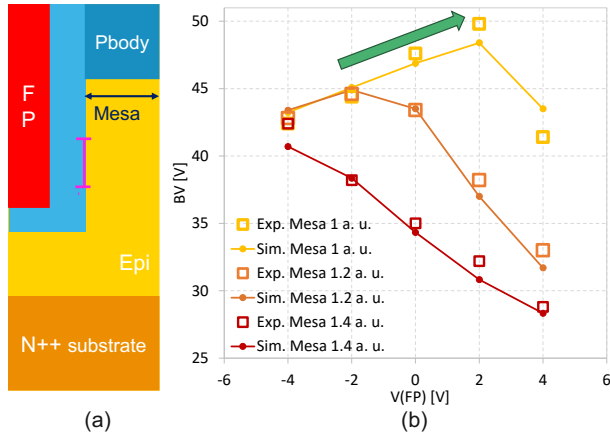


Fig. 3: (a) Single polysilicon filled trench structure with positive charges density of $1.5 \times 10^{12} \text{ cm}^{-2}$ located at the pink interface; (b) BV_{dss} vs. $V(\text{FP})$ curves for devices with mesa = 1 a. u., mesa = 1.2 a. u. and mesa = 1.4 a. u. As we reduce the mesa dimension, we shift the bell curve (green arrow).

bonds configurations called Pb0 and Pb1 centers. This means that positive charged states are at the SiO_2/Si interface.

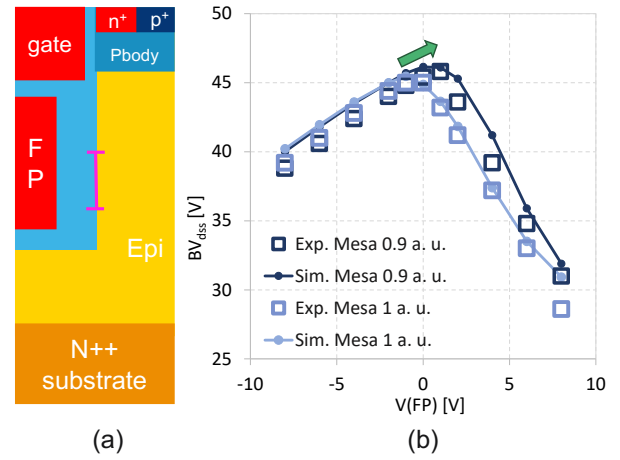


Fig. 4: (a) SG-MOSFET structure with positive charges density of $1.5 \times 10^{12} \text{ cm}^{-2}$ located at the pink interface; (b) BV_{dss} vs. $V(\text{FP})$ curves for devices with mesa = 0.9 a. u. and mesa = 1 a. u. We can notice a shift in the bell maximum as we reduce the mesa dimension (green arrow).

III. ELECTRICAL CHARACTERIZATION AND SIMULATIONS

Starting from the evidence found in DLTS, positive fixed charges at the FP-oxide/Si wall were implemented in Synopsys Sentaurus Device TCAD simulation tool. Then to correlate our simulations with experimental data, electrical characterization was performed to obtain BV_{dss} values at different FP polarizations. Measurement method used was to polarize the backside of the wafer through the chuck by imposing a voltage sweep from 0 to 50 V. The compliance value used for the drain current was fixed at 100 nA/mm^2 . This compliance allowed to stop the measurement in the BV region with a low current density to control the stress in the avalanche region during the measurement. All experimental points were done on virgin sites except when contrary is specified.

A. Single polysilicon filled trench structure

The first structure tested is represented in Fig. 3(a). A particular extension and concentration of the charged interface allowed to predict the behavior of BV vs. $V(\text{FP})$ bell curves (Fig. 3 (b)) for structures with three different inter-trenches distances. The latter is also known as mesa dimension, and it is one of the most important factors to consider when designing the charge balance of the structure. The pink segment shows the extension of the charged interface used in simulations. Due to structure topology, the hypothesis is that the defectivity evidenced by the C-DLTS is localized deep down the trench walls. As highlighted in Fig. 3 by the green arrow, the bell shape curve is shifted towards up-right direction due to the charge balance between the mesa region and the polarization of FP electrode and its effect on electric field distribution. TCAD simulations precisely fit the electrical characterization. Considering as a reference the FP polarization at 0 V, for the BV we notice that the values decrease of approximately 12 V for a mesa increase of 40 %. This is expected because, as we increase the distance between trenches, we lose the beneficial effect of the FP electrode, thus moving the BV towards the intrinsic p-body/n-epi junction value.

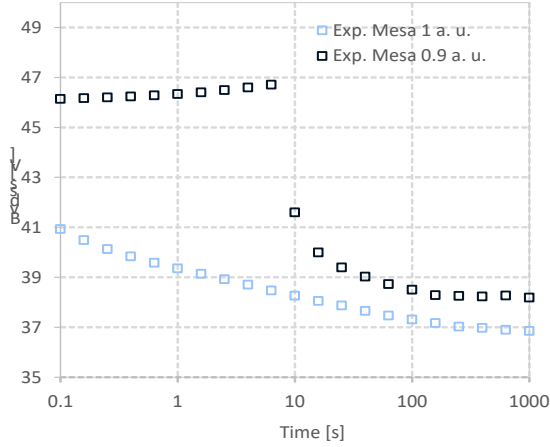


Fig. 5: BV_{dss} of SG-MOSFET structures with different mesas monitored during 1 mA/mm^2 avalanche current drain stress.

B. SG-MOSFET structure

The same simulation approach was used for the more complex structure of SG-MOSFET. Two structures with 10 % difference in mesa dimensions were electrically tested. As reported in Fig. 4(a), there is a good match between simulations and experimental characterization proving that the critical interface defectivity is limited to the FP oxide walls where positive fixed charges are located. The green arrow in Fig. 4 (b) highlights the shift in the bell curve induced by the reduction of mesa of 10 %.

C. Avalanche current drain stress

The SG-MOSFET structures were tested during avalanche current drain stress to obtain the experimental data reported in Fig. 5. At each point of the curve, the continuous current drain stress was interrupted and the BV_{dss} was obtained in parametric

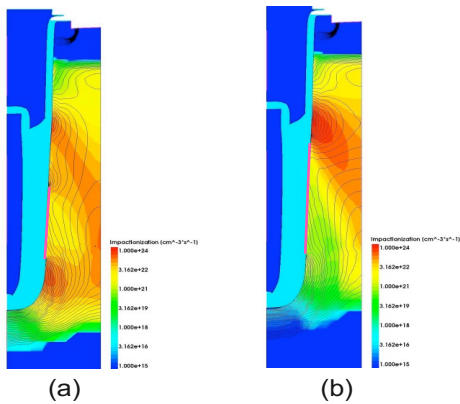


Fig. 6: Impact ionization view and electric field lines of SG-MOSFET at breakdown. Pink line shows the position of positive charges used in BV_{dss} simulations: (a) electric field with two hot spots in virgin structure; (b) for degraded structure, the high ionization spot is located in the upper portion of the trench, causing the BV_{dss} drop due to FP effect loss.

test mode imposing a pulse of 100 nA/mm^2 on drain contact to read the voltage value. As reported in the graph, the structure with the reduced mesa dimension seems to be more robust, leading to a walk-out phenomenon of the BV_{dss} before the degradation. Moreover, also in the degraded state, it represents the more favorable solution with a stable plateau behavior and higher absolute BV_{dss} value.

IV. DISCUSSION

The walk-in phenomenon is due to the evolution of electric field during the avalanche stress and the consequential displacement of impact ionization peak from the bottom to the p-body/n-epi junction [6]. As shown in Fig. 6(a), the virgin state structure can withstand a higher BV_{dss} value because it has two ionization spots that share the avalanche stress. The latter introduces further interface defectivity due to hot-hole injection degradation mechanism [3]. Therefore, in TCAD simulations of the degraded state, the charged FP oxide/silicon interface was extended. This induces the concentration of only one high ionization spot next to the junction (Fig. 6(b)).

In agreement with electrical current drain stress results, the BV_{dss} TCAD calibration for reduced mesa structure in the degraded state requires an increase in overall charge density from 1.5×10^{12} to $1.7 \times 10^{12} \text{ cm}^{-2}$ with respect to the larger mesa (Fig. 7). It is supposed that the higher charge density required for degradation is a signal of increased robustness. For this simulation set-up, we used fixed charged density at the interface in the degraded state while changing the FP polarization. The correlation is perfect at $V(\text{FP}) = 0 \text{ V}$ whereas it is slightly misaligned in positive and negative FP polarizations (Fig. 7). This is explained by the fact that holes are moving in the oxide and, depending on the polarization sign, are attracted or pushed from the interface. Therefore, depending on FP polarization, the extension of the charged interface is variable.

To study the influence of gate depth, three different polysilicon recession times were used during manufacturing, this resulted in different gate depths. These trials were tested after degradation in the same conditions previously described and the BV_{dss} vs. $V(\text{FP})$ bell curves do not show any important gain in the walk-in phenomenon. At $V(\text{FP}) = 0 \text{ V}$, the BV_{dss}

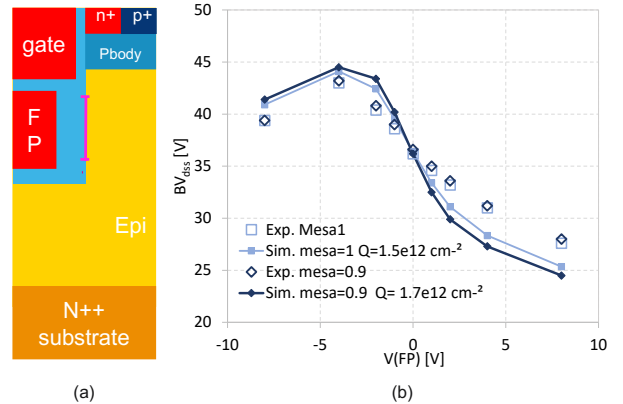


Fig. 7: (a) SG-MOSFET structure with positive charge density located at pink interface; (b) BV_{dss} vs. $V(\text{FP})$ curves after degradation of SG-MOSFET structure with different mesa dimensions.

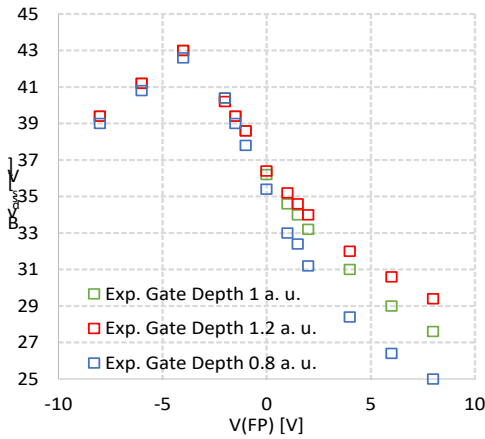


Fig. 8: BV_{dss} vs. $V(FP)$ experimental characterization after degradation of SG-MOSFET structures with different gate depths.

values for the three structures stand next to each other between 35 V and 37 V. This agrees with the fact that positive charges are located at FP oxide walls and that the degradation phenomenon is not influenced by the gate depth, meaning that there is only one high ionization spot in the degraded state next to the p-body/n-epi junction for all the three structures.

Following the characterizations, acting on gate depth or mesa dimension is not sufficient to solve BV_{dss} walk-in issue. Therefore, we used the degraded simulation set-up (Fig. 6(b)) to analyze the effect of modifications in epitaxy recipe, always paying attention to its impact on R_{on} . A fine tuning of the epitaxy recipe in the drift region allows us to obtain a remarkable improvement in the device behavior (Fig. 9). When focusing on the $V(FP) = 0$ V polarization, it is possible to have 28% increase in BV_{dss} with less than 6% of total R_{on} increase for the adjusted epitaxy recipe (green arrow in Fig. 9).

Fig. 10 shows that the increased BV_{dss} sustained by the structure is due to the second ionization spot appearing at the bottom of the trench thanks to the modified charge balance.

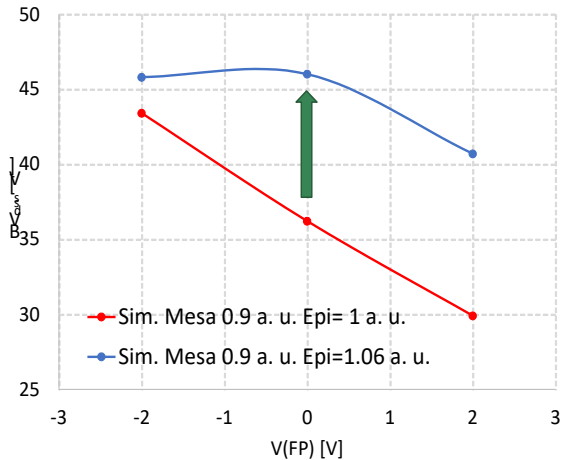


Fig. 9: BV_{dss} vs. $V(FP)$ of SG-MOS FET with two epitaxy recipes predicting an increased robustness in degraded structure simulation set-up as in Fig. 6 (b).

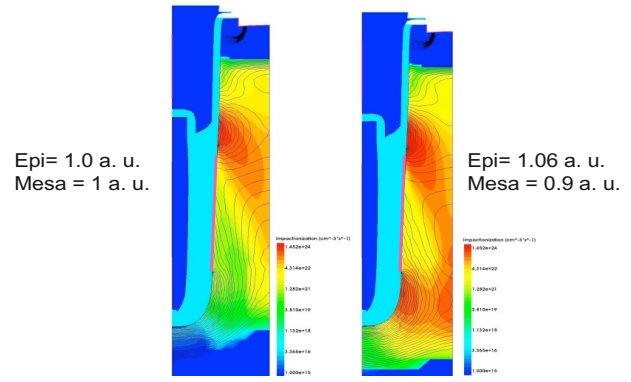


Fig. 10: Comparison between non-optimized (on the left) and optimized structure (on the right). Impact ionization view and electric field lines of SG-MOSFET at breakdown. Pink line shows the position of positive charges used in BV_{dss} simulations.

V. CONCLUSIONS

In conclusion, to increase the robustness of the SG-MOSFET structure, it is necessary to pin the electric field enhancement at the bottom of the trench. Experiments and simulations proved that reducing the mesa dimension can help this mechanism. Through this work, it was possible to prove that to adjust the gate depth is not sufficient to solve this issue. Therefore, modifications in the epitaxy recipe and in the charge balance of the drift region were analyzed. The simulations predict that, combining a reduced mesa with an adapted epitaxy recipe solve the issue with a reduced R_{on} impact.

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