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► To cite this version:

Guilhem Larrieu, Jonas Müller, Sylvain Pelloquin, Abhishek Kumar, Konstantinos Moustakas, et al. Advanced contacts on 3D nanostructured channels for vertical transport gate-all-around transistors. 21st International Workshop on Junction Technology (IWJT 2023), Jun 2023, Kyoto, Japan. pp.1-4, <10.23919/IWJT59028.2023.10175172>. <hal-04189319>

HAL Id: hal-04189319

<https://laas.hal.science/hal-04189319v1>

Submitted on 31 Aug 2023

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Advanced contacts on 3D nanostructured channels for vertical transport gate-all-around transistors

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1. Introduction

Gate-all-around (GAA) transistors are anticipated to have a substantial impact in achieving logic scaling in the nanometer technology node range, serving as a substitute for the current FinFET technology which lacks acceptable immunity against short channel effect at such miniaturization. GAA transistors offer several advantages over older transistor designs, such as better performance, lower leakage, and reduced energy consumption. This makes them a more sustainable and environmentally friendly alternative to current architectures. In term of integration, vertical gate-all-around devices offer extreme density capability, surpassing equivalent planar technologies. Nevertheless, the development of vertical technology requires rethinking the entire development chain from design to technology. Here, we will present an overview of this technology with a particular focus on the engineering of 3D nanostructured channels and on the integration of S/D contacts on such vertical channels.

2. Vertical channel engineering

Vertical nanostructures of Si and SiGe are realized by a top-down fabrication process with three main steps as demonstrated for the creation of nanowires on highly doped p-type silicon substrates is presented in Fig. 1. Different structures such as nanowires (NW) and Nanosheets (NS) can be created and are firstly patterned as negative resist mask of Hydrogen Silyloxyane (HSQ) by e-beam lithography that, operated at low acceleration voltage of 30 kV and using dedicated star-shaped exposure paths for NW writing, benefits from an over-all reduction in writing time making it wafer-scale applicable. The developed HSQ patterns are then transferred onto the substrates by reactive ion etching (RIE) based on fluorine chemistry and the remaining HSQ is removed in diluted hydrofluoric acid. This process yields perfectly vertical nanostructures for the correct gas ratios of SF₆ and C₄F₈ (see Fig. 2a) which can be adjusted to achieve optimal results for any Si_{1-x}Ge_x (x = [0,1]) substrate composition as demonstrated in [1]. Lastly, the so achievable feature sizes of 25-30 nm can be reduced further through the creation and removal of a sacrificial oxide layer. For Si, a thick oxide is grown through wet-thermal oxidation at 850°C during several minutes and the resulting oxide layer is

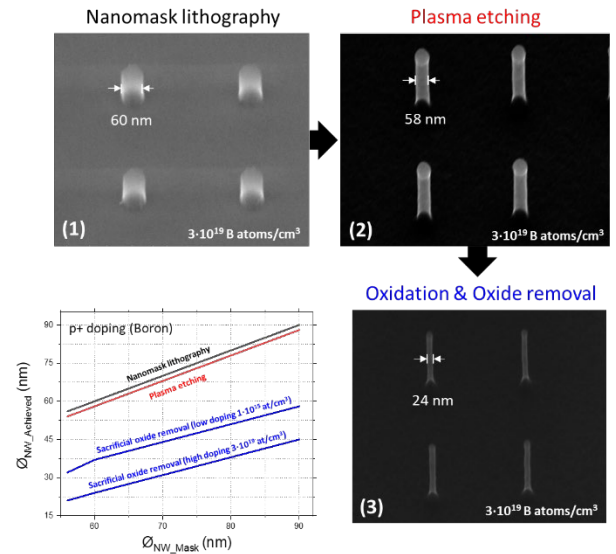


Fig. 1: Scanning electronbeam microscopy images of the top-down fabrication of vertical nanostructures as shown for nanowires on highly doped p-type Si. The measured NW diameter after the different processing steps are plotted over the initial electron beam mask sizes.

stripped in a buffered oxide etchant (BOE) solution. For SiGe structures, slower oxidation processes, such as dry-thermal oxidation, are required as increased Ge contents lead to an oxide growth rate enhancement (GRE). This is similar to the effect of high dopant concentrations in silicon substrates which have no impact on the patterning, the dimensions of the nanostructures after lithography and etching are identical for any doping concentration, but also increases the oxidation rate. Consequently the oxidation process has to be adjusted to the substrate's doping level.

This fabrication process can also be extended to other materials such as III/V semiconductors as demonstrated for epitaxial GaAs or GaSb layers on Si substrates [2]. Following the same lithography step, the transfer etching of vertical GaAs structures is achieved through chlorine-based plasma etching. Similar to the fluorine gas mixture used for Si_{1-x}Ge_x substrates, the anisotropy of the GaAs etching can be precisely tuned by optimizing the Cl₂/N₂ gas ratio (see Fig. 2b). Further, by implementing protective layers, it is possible to sequentially conduct both etching processes to fabricate vertical GaAs-Si nanostructures with an axial

hetero structure [2]. Consequently, it becomes possible to realize different heterostructures using III/V and $\text{Si}_{1-x}\text{Ge}_x$ materials.

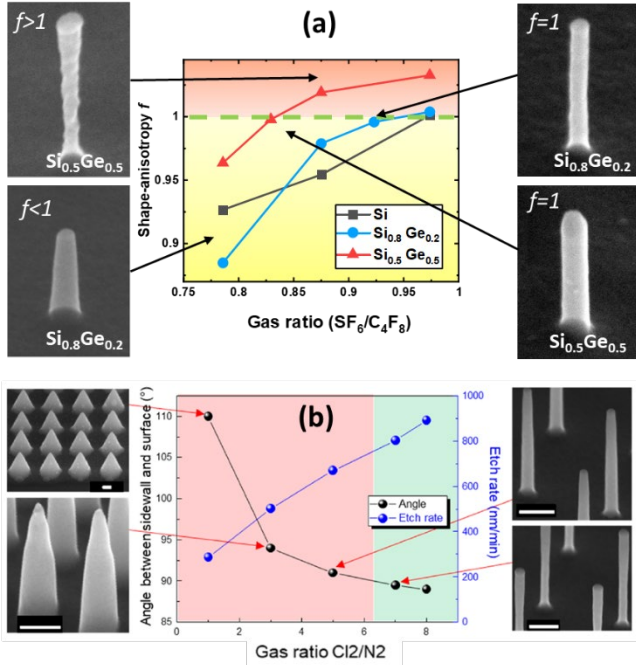


Fig. 2: Impact of the RIE plasma gas ratio of (a) $\text{SF}_6/\text{C}_4\text{F}_8$ on the nanowire sidewall anisotropy for Si, $\text{Si}_{0.8}\text{Ge}_{0.2}$ and $\text{Si}_{0.5}\text{Ge}_{0.5}$ adapted from [1] and (b) Cl_2/N_2 on the nanowire sidewall anisotropy and GaAs etch rate adapted from [2].

3. Advanced contacts on vertical nanoscale channels.

The fabrication of reliable contacts using metal silicon alloys (silicides) is a crucial technological component for the realization junctionless VNW-FETs and more complex future CMOS or other 3D structured devices. Particularly for CMOS-NW applications, it is necessary to locally implant a high concentration of n- and p- type dopants in NWs which consequently require different low-resistive silicide alloys, Ni- or Pt-silicides respectively, to achieve optimal performance [3]. The change in geometry from conventional planar/bulk devices to 3D vertical nanostructures however, greatly impacts the dopant segregation and silicidation reaction due to the different geometrical constraints of e.g. nanowires and their respective dimensions.

Oxidation processes used during VNW-FET fabrication, either to create sacrificial oxide layers or dielectric gate oxides, cause a depletion of the initial doping level as dopants segregate into the formed oxide layer. Recently realized measurements of the dopant concentration of boron doped NWs using high incident Secondary Ion Mass Spectrometry (SIMS) [4] firstly allowed for the precise evaluation of the enhanced dopant segregation and the change of the dopant level in nanostructures as compared to planar samples. The results presented in Fig. 3 correspond to the Boron profiles obtained after the RIE etching of highly

doped nanowires, sacrificial oxidation by either dry or wet thermal oxidation, tuned to achieve equal oxide thickness, after the combined process of wet sacrificial and short dry-thermal oxidation used for the creation of thin gate oxides (“gate”).

Similarly, the silicidation process in vertical nanostructures also differs from the commonly observed reactions in bulk

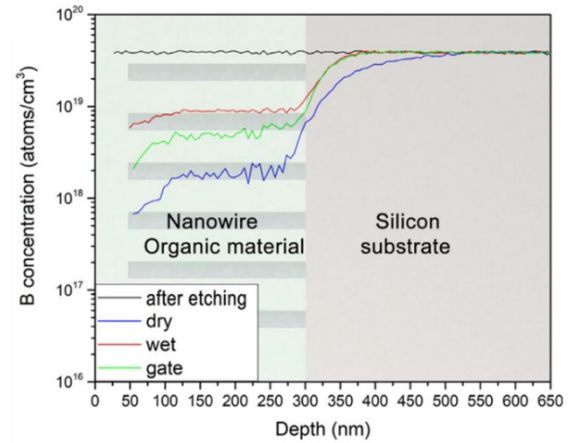


Fig. 3: Comparison of the depletion in boron concentration due to dopant segregation into silicon oxide as measured by high incident angle SIMS measurements for NW samples after RIE etching and different oxidation processes with subsequent oxide removal. Figure adapted from [4].

samples as shown in Fig. 4 for Ni-silicide. While the Pt-silicide reaction is well understood and successfully implemented on vertical nanostructures, Ni-silicide fabrication is more challenging due to the added complexity of the Ni-Si phase transformation and its dependence on the thermal annealing process triggering the silicidation reaction. Up to now, plenty of reports on the bulk transformation sequence are available while the few considering the silicidation in nanostructures are so far limited to large nanometric dimensions. The investigation of Ni-silicidation in nanostructures with high geometrical constraints (20-30 nm) as required for JL-VNWs devices is thus crucial for the optimization of VNW-FET contacts. Notably, the goal is to obtain the low-resistive NiSi phase while avoiding high resistive NiSi_2 or Ni-rich phases. For comparison Ni-silicide was created on Si-NWs, fabricated following the fabrication process described in section 3, and characterized by Energy Dispersive X-ray (EDX) microanalysis as depicted in Fig.3b demonstrating the impact of high geometrical constraints in smallest nanostructures shifting the transition temperature of NiSi-NiSi₂ towards lower temperatures as observed for the bulk [5].

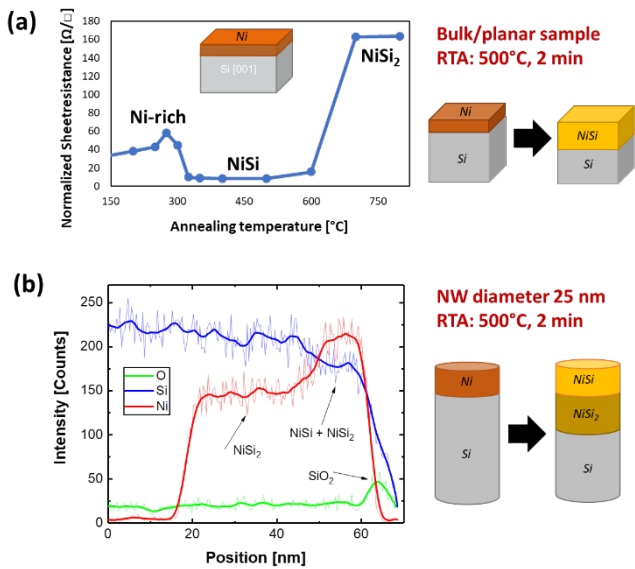


Fig. 4: Comparison of the Ni-silicidation of bulk and nanowire samples obtained after rapid thermal annealing (RTA) of 10 nm thick Ni layers at 500°C. (a) Based on sheet resistance measurements, the low resistive NiSi phase is found for bulk samples while the EDX measurement along the NW axis (b) reveals a partial transformation into NiSi₂ indicating a shift of the transformation in small nanostructures.

In the same manner, the formation of silicide-like contacts for III/V materials can be implemented as for example in the case of the Ni-GaAs system, forming Ni₃GaAs (Fig. 5). In both cases, the formation and size of the alloyed contact strongly depends on the nanostructure's diameter, requiring a precise adjustment of the processing parameters to achieve reliable NW contacts.

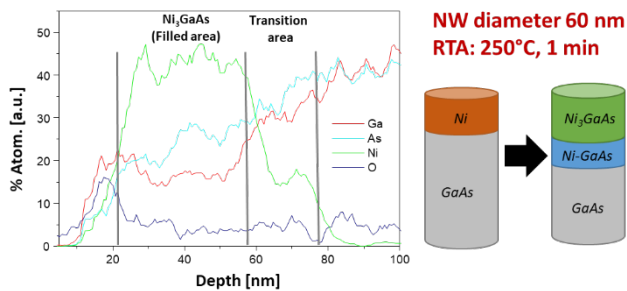


Fig. 5: EDX profile of the formed Ni₃GaAs alloy on a nanowire sample obtained after rapid thermal annealing (RTA) of a 15 nm thick Ni layer at 250°C.

4. Vertical Junction-less field effect transistors

In contrast to the traditional fabrication method for planar transistors using a gate first approach, we have introduced a gate last approach for the creation of nanoscale gate-all-around (GAA) transistors in a vertical configuration. This involves processing the gate contact after the formation of the source and drain, which allows for precise definition of

the length of the metal gate in extremely miniaturized dimensions. The main steps involved in the fabrication process of vertical GAA transistors include patterning of the vertical nano-structured channel and of gate-all-around material, engineering of the source/drain contacts and vertical spacer technology. The aforementioned fabrication steps have been integrated to produce highly dense ultra-scale vertical transistors [6][7][8] (Fig. 6). The use of highly doped silicon substrates in the fabrication of nanowires [9] allows for the creation of junctionless transistors, simplifying the overall fabrication process by avoiding the need for dopant gradients required for conventional junctions.

Junctionless transistors exhibit high immunity against short

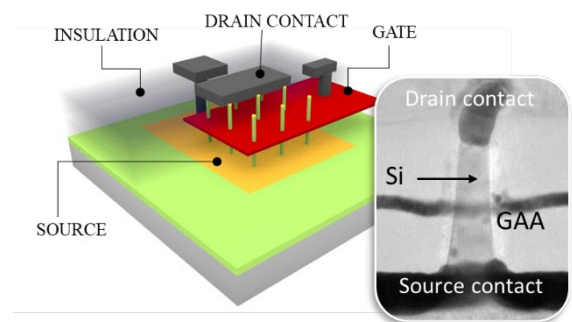


Fig. 6: Schematic representation of the vertical gate-all-around transistor with a TEM cross-section features Pt-silicided source/drain contacts and an 18 nm Lg.

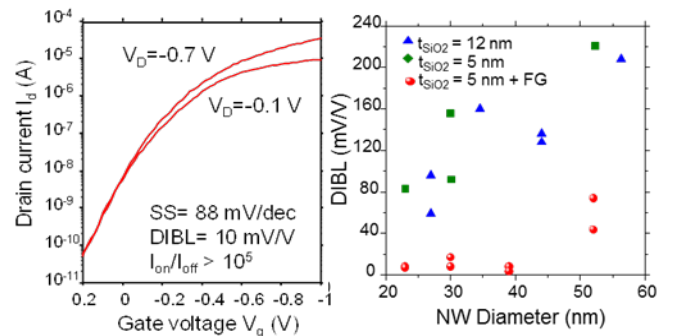


Fig. 7: (left) Static characteristics of a 15 nm gate-all-around vertical junctionless transistor on nanowires with 30 nm of diameter and (right) drain induced barrier lowering as a function of nanowire diameter measured on a 14 nm GAA architecture showing the impact of the gate oxide thickness and the post forming gas annealing [8]

channel effects. Electrostatic control of the channel can be maintained for sub-15 nm gate dimensions with nanowire diameters up to 40 nm [6][7], offering a wide design window for these devices. Consequently, excellent electrical properties are achieved, with small drain-induced barrier lowering (10 mV/V), good subthreshold swing (88 mV/dec), and high on/off ratios on the order of 5 magnitudes achieved for an ultra-thin gate oxide [6]. The electrical properties scale with the nanowire dimension, as the drive current is proportional to the nanowire's cross-sectional area, while the

electrostatic control of the gate is increased for smaller nanowires. Junctionless contacts are less sensitive to defects near the gate oxide because the conduction occurs mainly in the heart of the channel [10]. Vertical junctionless transistors are highly versatile in their application, as the threshold voltage for a given configuration can be adjusted simply by designing the nanowire diameter. Vertical nanowire arrays thus offer a multi-threshold voltage platform that can be tailored for either low-power or high-performance applications using the same fabrication process [8].

5. Conclusions

The recent achievements in nanostructure fabrication of different semiconducting materials (Si, SiGe, GaAs) and alloyed contact formation using Ni or Pt, required for the creation of novel and more performant junctionless Vertical gate-all-around devices have been presented. With optimized RIE etching processes it is possible to fabricate smallest nanostructures on high mobility substrates such as SiGe that achieve even higher device performance when implemented in JL-VNWFET devices. Further, the possibility of creating axial heterostructures including III/V materials gives way to the fabrication of more complex NW based devices. Recent advances in the characterization techniques for dopant concentration and studies on silicidation of nanostructured S/D contacts on these 3D nanostructured channels have shed new light on the complex segregation and silicidation mechanisms in nanostructures. Due to the high geometric constraints in VNW-FET scale structures, dopant segregation and silicidation differ from what is observed in planar devices, thus requiring a precise adjustment of the processing parameters to achieve optimal contact and device performance.

Acknowledgements

This work was supported by European Union's H2020 program through the FVLLMONTI project (N°101016776) and MUNDFAB project (N°871813) and by the LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech french national network.

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