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Thermal consideration in nanoscale gate-all-around vertical transistors

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Abstract — *Development of high-performance logic application in sub-20 nm technology node has gained significant attention due to their improved electrostatic and thermal control. In this work, we investigate electro-thermal transport in vertical junctionless nanowire transistors (VNWFET) at cryogenic temperatures to understand thermal effects in nanoscale regime. It highlights that heat dissipation and thermal stability are more efficient compared to planar Finfet configuration.*

Keywords: Semiconductor, junctionless nanowire transistors, nanoscale thermal transport, thermal conductivity, cryogenic.

I. INTRODUCTION:

In the present era, transistors have attained a state of high miniaturization, with technology nodes such as N5 possessing physical gate lengths less than 20 nm. At these scales, classical physical principles confront competing mechanisms and configurations intrinsic to the nanoscale. Additionally, in short channel lengths thermal management poses significant challenges, encompassing low thermal stability and leakage current due to self-heating effects and hot-spot formation [1]. This paper presents an investigation of the thermal properties of a vertical conduction sub-20 nm gate-all-around (GAA) junctionless transistor technology, a promising candidate for future technology nodes due to its ability to support denser architectures through a compact device layout. Given its highly miniaturized design and unconventional layout of metallic and insulating layers, this architecture is particularly intriguing for addressing thermal challenges of highly advanced devices. In this scope, it has thus become crucial that design considerations include renewed focus on electrothermal optimizations to satisfy Moore's law trends [2]. Thermal conduction is governed by phonon transport in sub-10 nm devices that include (1) ballistic, (2) boundary scattering and (3) confinement regimes [3]. Guyer and Krumhansl equation (GKE) has recently been demonstrated to capture non-diffusive heat transport in nanoscale regime beyond the classical Fourier's law, offering understanding of non-local thermal effects [4]. Based on the GKE formulation, this work investigates for the first time electrothermal behavior of nanoscale GAA junctionless transistors.

II. DEVICE AND TEMPERATURE CHARACTERIZATION

Fig.1 present a schematic view of the vertical junction-less device with a metallic GAA of 18 nm and symmetrical PtSi contacts, as described in [5]. The measured I_D - V_G curves are plotted in Fig. 2 for different temperatures ranging between 100 K $\leq T \leq$ 400 K, for p-Type JL GAA MOSFETs (Fig. 2) with a NW diameter 23 nm. The drive current increases monotonically with the temperature both at low and high V_D , in accordance with the behavior observed for junctionless FETs [6]. The decrease in drain current at lower temperatures can be attributed to the suppression of the thermally-activated conducting currents at the contact which is not compensated by the improvement of mobility at low temperature. A

transition between low and high temperature regimes for V_{th} (reflected by a change of slope of the V_{th} -T plot in Fig. 3) at around 200-300 K, exhibit a NW size-dependent transition of the dominant scattering mechanisms in the nanostructures. The subthreshold slope evolution with the temperature for different NW diameters (Fig. 4) is compared to a theoretical prediction for MOSFET devices ($\ln 10 \cdot (kT/q)$).

III. THERMAL ANALYSIS

Through cryogenic static characterizations and finite element modeling, we studied heat accumulation in a single nanowire using COMSOL Multiphysics [7] based on GKE formulation. Unlike the linear temperature gradient in classical regimes, non-Fourier transport can accurately describe nonequilibrium states in both steady and transient ultrafast nanoscale thermal transport based on GKE and energy conservation. Non-local response of phonon destination is used for the prediction of the effective thermal conductivity in nanowires as shown in Fig. 5, illustrating that the present GKE matches well with the reported data [8]. Thermal conductivity reduces significantly below the 10-nm regime. Distribution of thermal conductivity and temperature along the nanowire, shown in Figs. 6 and 7, respectively, indicate a degradation of thermal performances near the drain region due to the dominance of resistive phonon transport. However, beyond the point of heat accumulation near the drain, especially at $V_D = -1.1V$, device temperature drops rapidly towards the drain contact (Fig. 7), indicating an efficient heat evacuation that further improves with more parallel nanowires. In terms of electrical performance under temperature, a key parameter for the junctionless device is its threshold voltage, which shows two distinct temperature coefficients between two heat conductive regimes separated around 250K (Fig. 3). The VNWFET compact model [9] has been adapted to incorporate this effect through temperature dependence of key parameters such as V_{th} , Schottky barrier, R_{access} , V_{sat} and SS. Following model calibration against room temperature data (Fig. 8), good model accuracy was achieved for drain current temperature dependence (Fig. 9), highlighting the need for better understanding of nanoscale thermal transport for accurate electro-thermal modelling. Finally, Table 1 demonstrates that the extracted thermal conductivity in JLNTs is higher than FinFETs technologies. The structure of GAA JLNTs guarantee less confinement effects and therefore higher effective thermal conductivity. In technological point of view, JLNT is more thermally stable.

CONCLUSIONS

We investigated nanoscale electrothermal transport in sub 20 nm GAA vertical nanowire junctionless transistors. Results indicate two distinct heat conduction regimes at low and high temperature ranges that were taken into account to model its electrical characteristics. Efficient heat dissipation and better thermal stability justify the benefits of this technology as a beyond CMOS alternative.

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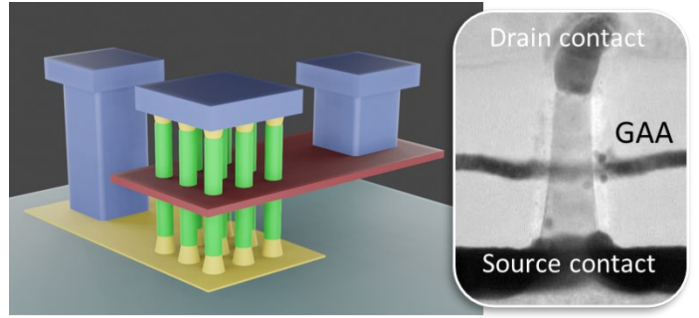


Fig. 1: Schematic and TEM cross section view of the vertical junction-less GAA devices. The metallic GAA features 18nm gate length. The channel is p-type homogeneous doping ($3E19 \text{ at.cm}^{-3}$) and have symmetrical Pt-silicided contacts.

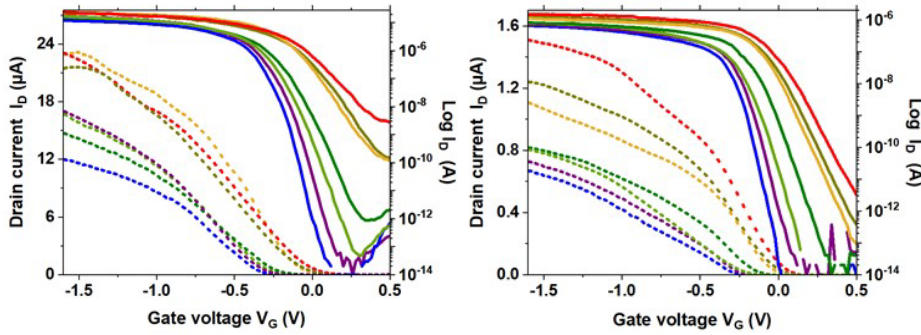


Fig. 2: I_d - V_g of 18 nm GAA VFET from 100K to 400K (step 50K) at a) $V_D = -0.1V$ and b) $V_D = -1.1V$

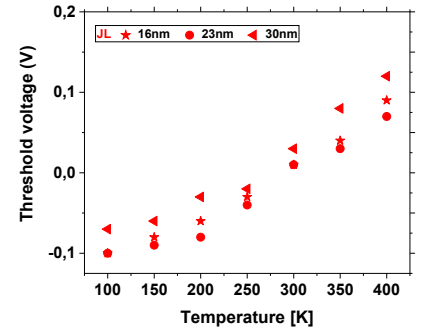


Fig. 3: Evolution of V_{th} as a function of temperature

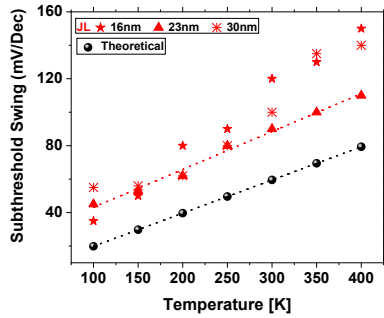


Fig. 4: Evolution of SS as a function of temperature

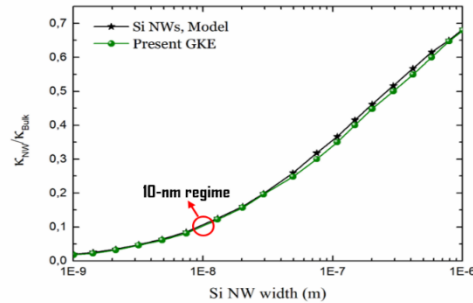


Fig. 5: Comparison of effective thermal conductivity for silicon nanowire at room temperature

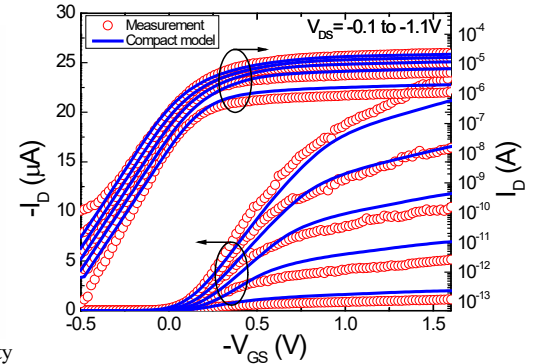


Fig. 8: Compact model validation at room temperature

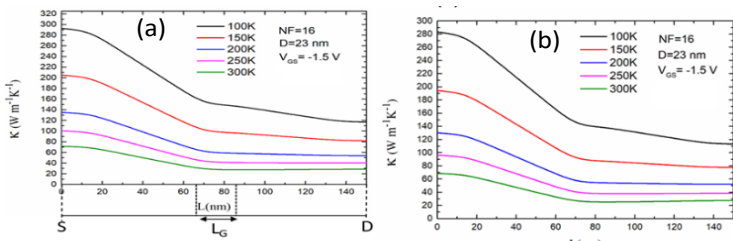


Fig. 6: Effective thermal conductivity along the nanowire for (a) $V_{DS} = -0.1V$. (b) $V_{DS} = -1.1V$

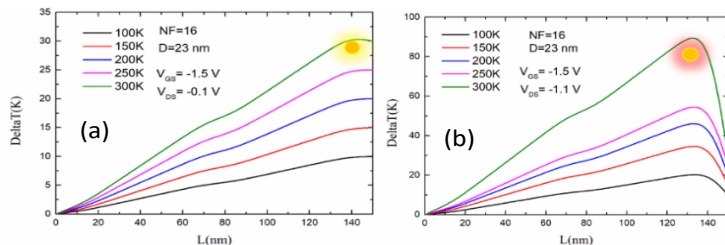


Fig. 7: The temperature distribution within the nanowire for (a) $V_{DS} = -0.1V$. (b) $V_{DS} = -1.1V$

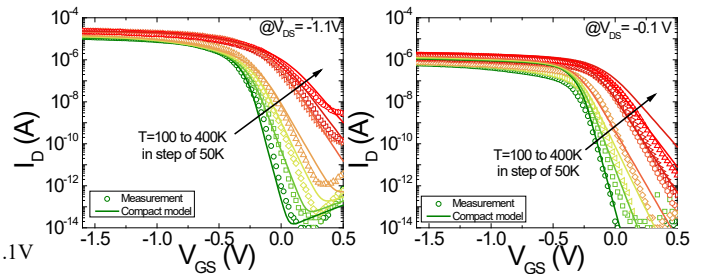


Fig. 9: Compact model validation against temperature data at $V_{DS} = -1.1V$ and $-0.1V$.

	JLNTs	FinFET
23-nm L_g	18 (W/m/K)	12 (W/m/K)
18-nm L_g	10 (W/m/K)	8.2 (W/m/K)

Table 1: The extracted thermal conductivity in SOI FinFETs [10] and JLNTs (present work)