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Analytical Approach of The High Susceptibility Frequencies of a Battery Management System During Direct Power Injection. Methods of Improvement

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Abstract— When it comes to the electromagnetic interference (EMI) immunity of a Battery Management System Integrated Circuit (BMS IC), Printed Circuit Board (PCB) traces and external components (ECs) arrangement define the high susceptibility frequencies (HSF) of the IC during Direct Power Injection (DPI) tests. This work first aims at defining the root causes of those HSF in a realistic and measurement correlated environment, then, formulating them in order to provide a realistic prediction in the early design stages. Moreover, the configuration of the ECs raises a crucial tradeoff between the overall price of the system and the immunity of the IC. This work, then, also aims at analyzing this tradeoff and proposing alternative configurations of the ECs that reduce the overall price but also lead to lower injection levels during DPI.

Keywords— BMS; PCB; Battery; Immunity; DPI; Resonance; Noise levels; EMC; Ladder Networks.

I. INTRODUCTION

Lithium Ion (Li-Ion) batteries as well as BMS [1] have been subject to extensive research to pave the way for the new generation of Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV). One major aspect of development, for example, is the characterization of the conducted EMI coming from the drive inverter which is one of the noise sources that can act as an aggressor to the BMS IC. In this noise path the cables, PCB traces and ECs highly contribute to the immunity of the BMS IC. The ECs of interest are automotive high voltage rated capacitors that are placed for electromagnetic compatibility (EMC) purposes and protection against electrostatic discharges (ESD). As shown in previous work [2], the cheapest configuration of these ECs is a differential connection across the battery cell. However, this leads to a number of HSF in both low and high frequencies of the considered DPI [3] frequency range ([150 kHz; 1 GHz]). Therefore, this work builds a measurement correlated model of the BMS IC environment to be used in DPI simulations. Then, this work elaborates an analytical model to predict the main HSF of the BMS IC in the early design stages in order to both provide design guidelines of the BMS environment and accelerate the time to market by taking appropriate measures in the early stages. Moreover, this analysis also determines the exact elements in the BMS IC environment that cause the HSF which in this case are resonances. Additionally, while this cheapest configuration of ECs [2] causes many HSF, the proposed analytical approach is pushed even further to analyze the addition of an extra capacitor to the ground and

evaluate its impact on the HSF in order to approach a more optimized configuration of ECs in terms of cost and immunity level. In parallel, the general approach of cost reduction of the overall EV system on the BMS ICs side is to increase the number of cells that the IC can monitor to have a reduced number of ICs for the same EV battery pack. However, the number of external components is rather cell related and thus stays the same. Moreover, since the new generations of BMS ICs handle a higher voltage (>80V), these ECs and more specifically automotive rated capacitors need to be rated for a higher voltage. Therefore, not only the price of these capacitors is greatly increased but also a bottleneck arises in terms of the voltage that they can handle. When including the EMC and ESD aspects, the best case scenario is to connect the capacitors to the ground to achieve optimum common-mode (CM) filtering and leaving only the variability of the capacitors with the DC voltage as source of asymmetry on one hand. Therefore, the high voltage rating issue is more pronounced in this case. On the other hand, achieving the cheapest cost is done by placing all the capacitors differentially, thus, not having to handle a 100V. However, a number of HSF is introduced and the IC immunity is compromised. Therefore, this work analyzes this problematic from a cost and DPI injection levels perspectives and proposes new ECs architectures that enable a better compromise between overall cost and EMC performance during DPI. These configurations are then compared in terms of EMC performance and overall price. Finally, the goals of this article can be summarized as follows:

- Build a measurement correlated model of the BMS IC environment to be used in DPI simulations. Propose a numerical model to understand and predict the HSF (resonances) in the cheapest configuration of ECs in the early design stages. Theoretically evaluate the impact of adding an extra capacitor to the cheap configuration on the EMC performance.
- Analyze how symmetrical placement of traces and ECs has an impact on EMC performance during DPI. Then, propose and compare optimized ECs configurations for EMC performance and low cost.

This paper is organized as follows: First, the measurement correlated modeling of the BMS IC environment is presented. Secondly, the on-hand analytical model to formulate the HSF is presented as well as the analysis of the impact of adding an

extra capacitor. Thirdly, the analysis of symmetry mechanisms with respect to EMC performance is elaborated. Then, optimized ECs configurations are proposed and compared in terms of DPI injection levels and cost.

II. MODELING OF THE BMS IC ENVIRONMENT

The main purpose of a BMS is to ensure the optimum and safe operation of the battery even under a harsh EMI environment. Some of the main functions of a BMS IC are to perform accurate cell voltage measurement and passive cell balancing [1] to prevent cell degradation and enable optimum power extraction from the battery pack. In order to characterize the ability of the IC to perform those tasks in a harsh EMI environment, DPI tests are performed where 30 dBm is coupled in a CM way onto all the IC's inputs that connect to the battery cells. Fig.1 shows the DPI setup used in this work with a BMS IC product that monitors up to 18 battery cells. In this setup, ultra-capacitors are introduced to be able to use 12 V batteries to build the pack (>80 V) and also provide a stabilization of the impedance seen on the pack's side.

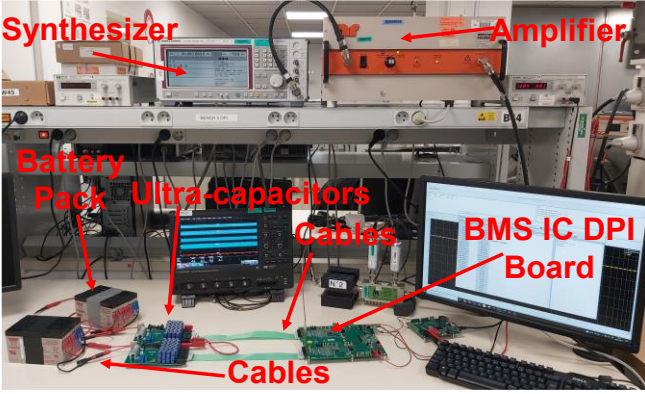


Fig. 1. BMS DPI test bench.

From Fig. 1, the elements of interest in this on-hand modeling approach are the following: the cables (30 cm both on the battery pack and PCB sides), the ultra-capacitors, the connectors, the PCB traces (both on the ultra-capacitors board and BMS IC board), the ECs on the BMS IC board and finally the impedance presented by the BMS itself. The goals of this measurement and modeling are to firstly confirm the resonances (HSF) in [2] and secondly build a realistic and measurement correlated simulation setup to be used in the comparisons of this work. From Fig. 2, the BMS IC input is

modeled by capacitors C_L (30pF) representing the internal passive cell balancing switches [1]. The capacitors C_d (47nF) are the ECs of interest which are placed for ESD and EMC purposes in the cheapest configuration [2]. C_{d1} (47nF) and C_{d0} (47nF) serve the same purpose ($C_d=C_{d1}=C_{d0}$) however C_{d1} is a 100V rated capacitor. The parasitic resistance and inductance of C_d and C_{d1} are also included in the model. In fact, since these parasitics are more pronounced in high frequencies, the parasitic resistance R_d of C_d and C_{d1} is taken at 100MHz and above. In a similar way, the parasitic behaviors of the injection capacitor C_i (330pF) are also considered. When it comes to the cables and PCB traces, their capacitive effect is not taken into account due to the presence of relatively higher value capacitors (C_d and C_{d1}). The following table associates each parameter on Fig. 2 with the elements on Fig. 1.

TABLE 1. Parameters of BMS IC environment Model during DPI

Parameter (Fig. 2)	Modeled Element (Fig. 1)
R_c, L_c	Cables between pack and Ultra-caps ($R_c=0.2 \Omega, L_c=300n$)
C, ESR, ESL, R_{leak}	Ultra-caps (10F), parasitic resistance ($ESR=0.1 \Omega$), parasitic inductance ($ESL=60 nH$) and leakage resistance (100 k Ω)
R_u, L_u	Traces on the ultra-caps PCB ($R_u=0.05 \Omega, L_u=12 nH$)
R_0, L_0	Cables between ultra-caps PCB and BMS PCB and 2 connectors ($R_0=0.3 \Omega, L_0=318nH$)
R_a, L_a	Traces from connector to injection point on BMS IC PCB. ($R_a=0.04 \Omega, L_a=20nH$)
L_1	Traces between injection point and capacitor C_d ($L_1=1nH$)
R_i, L_i	Traces between C_i and the injection point ($R_i=0.013 \Omega, L_i=1.62nH$)
R_d, L_d, L_{d1}	The parasitic resistance and inductance of C_d (not represented in Fig. 2). And L_{d1} the parasitic inductances of C_{d1} ($R_d=0.07 \Omega, L_d=0.68 nH, L_{d1}=0.82 nH$)
L_2, L_3	The traces between C_d and the BMS IC. ($L_2=21 nH, L_3=46 nH$)
R_b	Passive cell balancing resistor (11 Ω)

Moreover, the battery is modeled by an ideal voltage source as the pack and cables are shorted by the ultra-

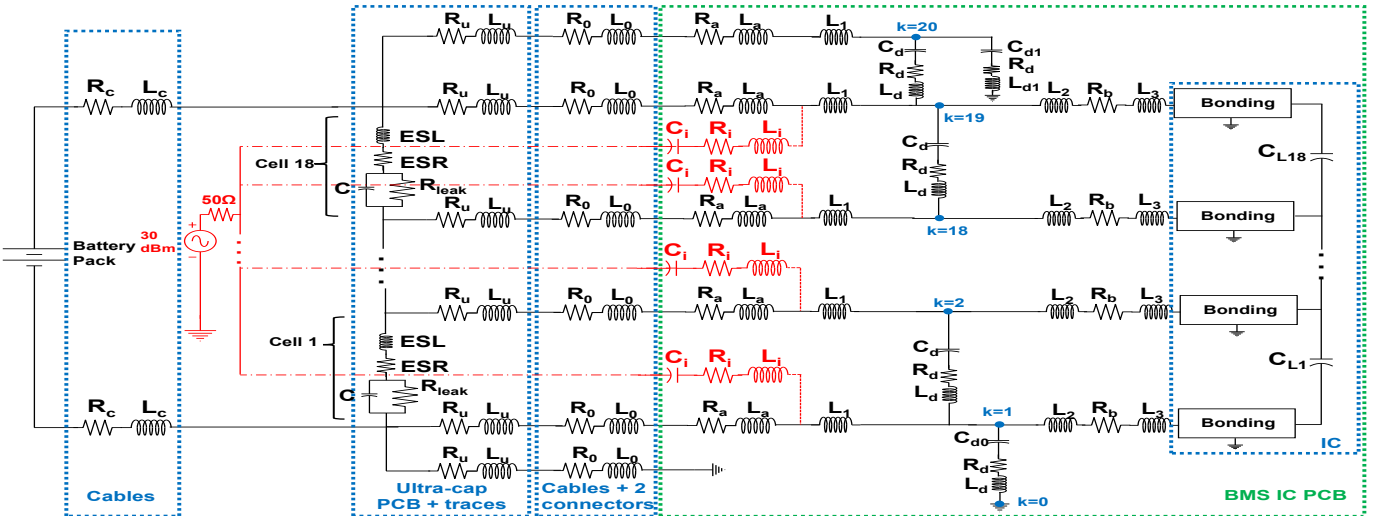


Fig. 2. Modeling of the BMS IC environment during DPI tests

capacitors. From Fig. 2, all the parameters are similar for the 18 cells neglecting the mismatches on the distances from each cell to the IC pins. The peak-to-peak voltage generated across C_{L1} (noted $V_{pk2pk}(C_{L1})$) is used to correlate between the measurements (Fig. 1) and the simulated model (Fig. 2) as the main goal here is to reproduce the main injection and HSF tendencies realistically by simulation. In the measurements, $V_{pk2pk}(C_{L1})$ was extracted using an oscilloscope passive probe (resistance of $10M\Omega$ and capacitance of 10 pF) with at least 100 points per decades in terms of injected frequencies at a constant power of 30 dBm . These probes were also accounted for in the simulation of the model (Fig.2). Furthermore, in order to extract $V_{pk2pk}(C_{L1})$ in a spice environment, transient simulations were performed where:

- Enough periods were given to the signals to settle (above 500 periods) before extracting any data.
- $V_{pk2pk}(C_{L1})$, is extracted as an average on the peak-to-peak voltage over the last 50 periods of the signal for each injected frequency.
- A sufficient number of points per decades were taken in the range of $[150\text{ kHz}; 400\text{ MHz}]$ (500 pts/decades).

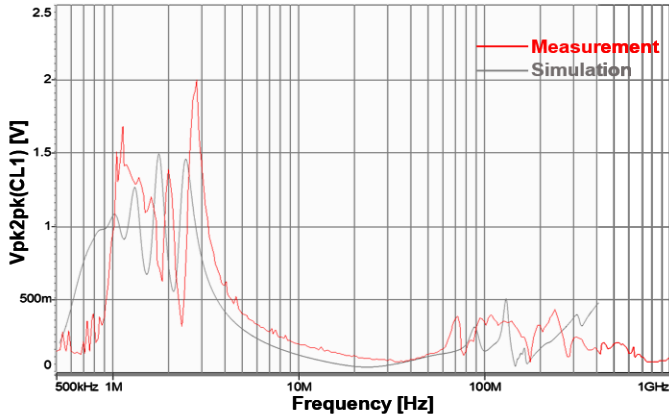


Fig. 3. Correlation between DPI measurement and simulation in terms of $V_{pk2pk}(C_{L1})$

Fig. 3 shows the correlation between the model and measurements where the simulation was stopped at the frequency of 400 MHz after which great mismatch occur due to unmodeled cables and traces behaviors that come into play. However, the main HSF were captured by the model in both high and low frequencies. Indeed, the measurement confirms the existence of the simulated resonances in [2], and the simulation manages to reproduce them realistically with a certain acceptable frequency and amplitude shifts. The frequency and amplitude shifts in low frequencies between the measurement and simulation are due to the non-considered mismatches in lengths of the traces that connect the cells to the BMS IC pins. The frequency and amplitude shifts in high frequencies between the measurement and simulation are due to the skin effect (traces, capacitors ...) and parasitic capacitances of cables and traces which are not considered in this model (Fig. 2). As opposed to previous work [2], not as many resonances are observed in low frequencies for example, and this is due to the resistivity of the PCB traces and cables. In fact, this resistive aspect compensate some of the 18 ideal resonances with anti-resonance counter parts. This leaves the resonances with the highest quality factor seen in Fig. 1. Finally, with a relatively simple model (Fig. 2), the main HSF and realistic injection levels can be obtained. Indeed, faster DPI simulations can be performed with the model without having to consider every single aspect of the system.

Moreover, it has also been shown that this cheapest configuration of C_d leads to a set of HSF. In the next section, the source of these HSF will be analyzed along with giving a numerical model.

III. ANALYTICAL APPROACH OF THE HSF OF THE BMS IC DURING DPI

Understanding the origins of the main HSF of the BMS IC during DPI is crucial in the first design stages for the correct definition of the ECs and the necessary design measures (IC, filters ...) for optimal EMC performance. In this section, the HSF of the BMS during DPI are investigated and formulated by an analytical approach for both high and low frequencies. Additionally, the possibility to counter those HSF with one additional capacitor arrangement is investigated.

A. Low Frequency Resonances ($<10\text{MHz}$)

The low frequency resonances are caused by the C-L ladder network generated by the differentially placed capacitors C_d and the parasitic inductance of the PCB traces and especially the cables between the ultra-capacitors and the BMS IC PCB. In order to approach a closed form expression of the HSF, no resistive effect is considered to visualize all of the generated resonances. Furthermore, a first approximation is to neglect any element present after capacitor C_d in Fig. 2 ($L_d, R_d, L_2, R_b, L_3, C_L \dots$) due to the high ratio between C_d and C_L especially in the considered range of frequency. With the previous consideration, the obtained model is shown in Fig. 4a with $L_T = L_u + L_0 + L_a$ (Fig. 2).

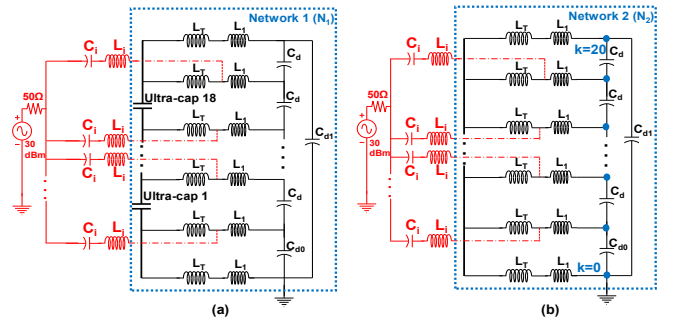


Fig. 4. Simplifying the model in Fig. 2 to ease the analytical approach. (a) Removing C_L . (b) Neglecting the ultra-capacitors

Next, the ultra-capacitors are approximated as very low impedance due to the high value of C (10F) and value of ESL especially in the considered range of frequencies ($[150\text{ KHz}; 10\text{ MHz}]$). The latter point leads to N_2 in Fig. 4b. N_2 is now a n -cells C-L ladder network composed of $(L_T + L_1)$ and C_d with an external load C_{d1} where ' n ' in this case is 20. Using [4], one can define the impedance of N_2 , however, no closed form of resonances is obtained due to the complexity of the equations. In this section, the previously proposed formula of resonances [2] is adapted for the case of N_2 as a more realistic case is considered now for the BMS IC environment. For now, we will analyze the impact of having an external load C_{d1} in N_2 in terms of resonances by considering an example of a 4 cells C-L ladder network with an external load C_{x5} in Fig. 5a.

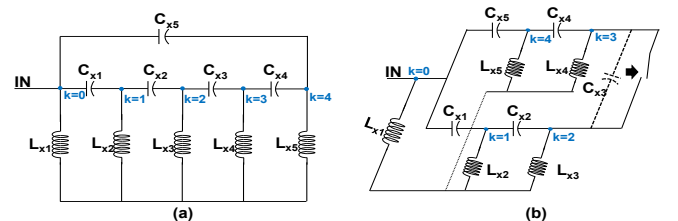


Fig. 5. 4 cells ladder network with external load C_{x6} (a) and its equivalent (b)

In Fig. 5, $C_{x1}=C_{x2}=C_{x3}=C_{x4}=C_{x5}$ and $L_{x1}=L_{x2}=L_{x3}=L_{x4}=L_{x5}$ with V_k the voltage on L_{xk} . From fig. 5b, which is a another representation of the network in Fig. 5a, V_1 and V_2 are symmetrical (or equivalent) with V_4 and V_3 respectively because there isn't any mismatch between the different components. Therefore, V_2 and V_3 follow the same variations thus no current flows through C_{x3} (Fig. 5b). The remaining network is composed of two identical C-L networks, thus, presenting 2 resonances and 2 antiresonances. In other words, without C_{x5} in Fig 5a 4 resonances and 4 anti-resonances would be presented. Thus by adding C_{x5} , the number of resonances and anti-resonances is divided by 2. While, it is assumed here that all the capacitors and inductances have the same value, it is mostly the case in reality in Fig. 2 where capacitors C_d are placed with the same value as not to create any asymmetries in the traces that lead to an increased injection levels during DPI. Furthermore, since node 1 and 4 (Fig.5b) have the same variations, Fig. 5b is equivalent to a 2 cells ladder network as shown in Fig. 6a where the value of L_{x1} in Fig.5b is doubled.

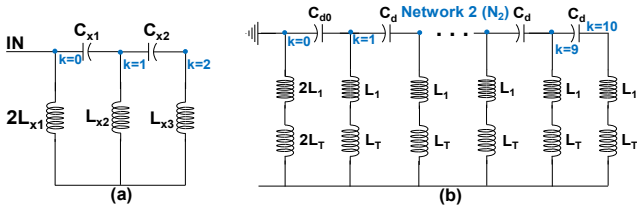


Fig. 6. (a) Equivalent to a 4 cells Ladder network with external load. (b) Equivalent to the network N_2 show in Fig. 4b.

In fact, the same approach can be applied for the case of the BMS IC environment leading to the equivalent network in Fig. 6b. Furthermore, it can be deduced that C_{d1} (Fig. 2) reduces the number of potential HSF of the BMS IC by half. From Fig. 6b, finding the resonances now amounts to extracting the input impedance Z_{IN} . Let us introduce the following notation for the companion polynomial in [5]:

$$P_a^n(K(s)) = \sum_{k=1}^n \frac{2n-1}{2k-1} \binom{n+k-2}{n-k} K(s)^{k-1} \quad (1)$$

Where $K(s)$ is defined as in [6] i.e. $K(s) = \frac{1}{s^2(L_T+L_1)C_d}$ in the case of N_2 (Fig. 4b). From [7], one can formulate the impedance seen from node 1 to the output. Then, by calculations extract Z_{IN} by taking into account C_{d0} ($C_{d0}=C_d$) and $(2L_T + 2L_1)$. Z_{IN} can be written as follows:

$$Z_{IN}(K(s)) = \frac{2Z_1 P_b^{n/2}(K(s))}{K P_a^{n/2+1}(K(s))} \quad (2)$$

Where $Z_1 = \frac{1}{sC_d}$, $P_b^n(K(s))$ is the morgan-voyce polynomial defined in [6] and 'n' is the total number of cell of the N_2 in Fig. 4b. The HSF are, thus, the roots of the polynomial $P_a^{n/2+1}(K(s))$. From [4], P_a^n is expressed as a function of Chebyshev polynomials of the second kind $U_n(x)$, and is orthogonal in the interval $[-4,0]$ with respect to the weight function $\sqrt{-\frac{x}{x+4}}$. Moreover, the roots of $P_a^n(K(s))$ are all real and can be written as follows [5]:

$$y_{j,n} = -4 \sin^2 \left(\frac{2j}{2n-1} \frac{\pi}{2} \right) \quad (3)$$

$$j = 1, \dots, n-1$$

Then, the HSF based on Fig. 4b can be written as follows:

$$f_{HSF,n}^{(j)} = \frac{1}{4\pi\sqrt{(L_1 + L_T)C_d} \sin \left(\frac{2j}{\left(\frac{2n}{2} + 1\right)} \frac{\pi}{2} \right)} \quad (4)$$

$$j = 1, \dots, \frac{n}{2} = 1, \dots, 10$$

In parallel, the resonance frequencies of the voltage generated across C_d i.e., the BMS IC side are extracted by simulating the setup of Fig. 4b. The resonances of the voltage across C_L generated in Fig. 2 while considering no resistive aspect in the model are also extracted by SPICE simulation. These values are then compared to their calculated counterparts from equation 4.

TABLE 2. Comparison of the values of equation (4) to their simulated counterparts in Fig. 4b and Fig. 2.

$f_{HSF,n}^{(j)}$	Equation (4)	Simulation Fig. 4b	Simulation Fig. 2 With no resistive behavior
$f_{HSF,n}^{(10)}$	622 KHz	615 KHz	601 KHz
$f_{HSF,n}^{(9)}$	636 KHz	626 KHz	615 KHz
$f_{HSF,n}^{(8)}$	666 KHz	659 KHz	644 KHz
$f_{HSF,n}^{(7)}$	716 KHz	706 KHz	693 KHz
$f_{HSF,n}^{(6)}$	793 KHz	785 KHz	767 KHz
$f_{HSF,n}^{(5)}$	912 KHz	901 KHz	825 KHz
$f_{HSF,n}^{(4)}$	1.1 MHz	1.1 MHz	1 MHz
$f_{HSF,n}^{(3)}$	1.4 MHz	1.4 MHz	1.29 MHz
$f_{HSF,n}^{(2)}$	2.1 MHz	2.07 MHz	1.7 MHz
$f_{HSF,n}^{(1)}$	4.1 MHz	4 MHz	2.37 MHz

From Table 2, the calculated resonances accurately fit the simulated resonances of the approximated setup of Fig. 4b, thus validating the analytical approach. Moreover, when considering an ideal version of Fig. 2 i.e. with no resistive behavior in the model, the calculated resonances fit reasonably well with the simulated ones up to $f_{HSF,n}^{(3)}$. However, an a deviance is noticed for $f_{HSF,n}^{(2)}$ and $f_{HSF,n}^{(1)}$. This is due to the ESL of the ultra-capacitors that now comes into play especially when frequencies get higher. Moreover, from Fig. 3, only $f_{HSF,n}^{(5)}$, $f_{HSF,n}^{(4)}$, $f_{HSF,n}^{(3)}$, $f_{HSF,n}^{(2)}$ and $f_{HSF,n}^{(1)}$ are present due to the resistive behavior of the model that drastically attenuate the resonances below $f_{HSF,n}^{(5)}$. All in all, the proposed closed form expression of the HSF remains a reasonable approximation of the frequencies and the range of frequencies for which the BMS IC is susceptible during DPI. Now, to consider the resistive behavior in Fig. 2, let us define $R_T = R_u + R_0 + R_a$. R_T would then be in series with L_T and L_1 (Fig. 4b). By re-applying the same analytical approach used previously, the HSF could be expressed as follows:

$$f_{HSF,n}^{(j)} = \frac{1}{2(L_T + L_1)} \sqrt{\frac{4(L_T + L_1) + R_T^2 y_{j,\frac{n}{2}+1} C_d}{-y_{j,\frac{n}{2}+1} C_d}} \quad (5)$$

$$j = 1, \dots, \frac{n}{2} = 1, \dots, 10$$

In this work, R_T is in the order of 0.39Ω thus it does not drastically contribute to the value of the calculated HSF. However, it can be the case in other DPI setups where longer cables are used.

B. Impact of Adding an Extra External Load C_{d2} ($<10\text{MHz}$)

From the previous section, without C_{d1} (Fig. 2) the number of presented HSF is doubled. One can then wonder if by adding an additional external load to N_2 (Fig. 4b), the number of HSF can be further reduced or some of them canceled. The following figure displays the addition of an external load C_{d2} to N_2 on a specific node 'x' where $C_{d2}=C_{d1}=C_{d0}=C_d=47\text{nF}$.

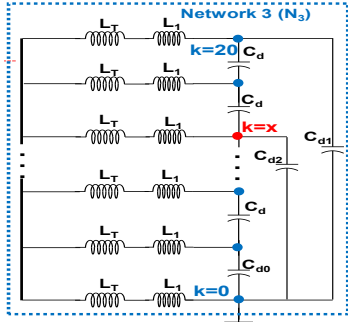


Fig. 7. Adding an extra external load C_{d2} in the BMS IC environment.

The approach in [4] has been adapted for an additional external load and the total impedance of N_3 (Fig. 7) has been calculated for an arbitrary node 'x' in [2;18]. The following 3-D graph displays $\text{dB}(Z_{IN})$ of N_3 as a function of frequency and C_{d2} placement node 'x'.

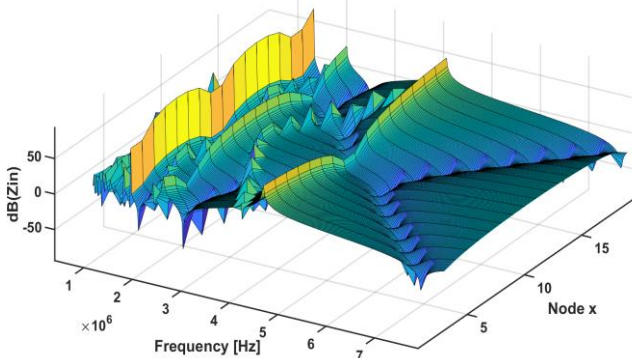


Fig. 8. The input impedance of N_3 as a function of frequency and placement of capacitor C_{d2} .

The goal here is to evaluate if there is an optimum node 'x' at which C_{d2} would limit the most of the HSF. From Fig. 8, it can be seen that for any 'x', some resonances can be shifted and controlled while others are fixed. Moreover, the number of resonances stays the same regardless of 'x'. Therefore, while adding C_{d2} may reduce the amplitude of the resonances it does not necessarily eliminate the issue of the HSF.

C. High Frequency Resonances ($>10\text{MHz}$)

In order to assess the origin of the high frequency resonances in Fig. 3, DPI measurements were performed with and without the BMS IC mounted to the PCB. From Fig. 9, it can be deduced that the high frequency resonances are not caused by the impedance of the BMS IC. In fact, the observed resonances are caused by the ladder network in Fig. 10. In other words, the resonances are due to a coupling between the injection capacitors and the capacitors C_d .

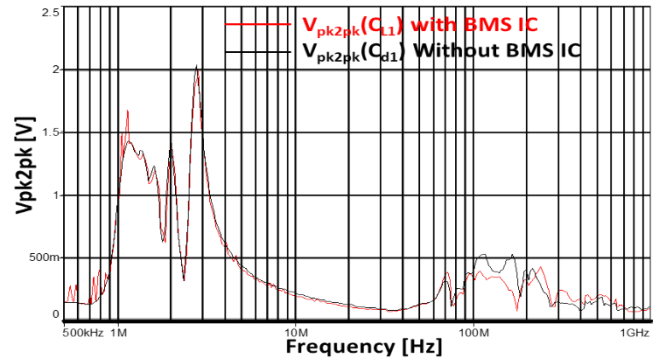


Fig. 9. Impact of the BMS IC on the high frequency resonances.

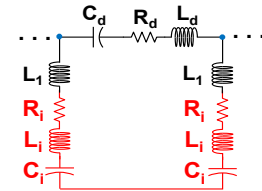


Fig. 10. The ladder network behind the high frequency resonances.

The resonances can be formulated similarly to the approach of previous work [2]. All in all, the choice of capacitor C_d packaging as well as the layout of the DPI injection traces on the PCB of the BMS IC directly impacts the immunity of the IC in high frequency during DPI.

IV. NEW PROPOSED ECs CONFIGURATION FOR EMC PERFORMANCE

The reason behind the relatively high injection levels in Fig. 2 is that for each node $k = i$ and $k = i + 1$, the path from 'i' to C_{d0} and the path from 'i + 1' to C_{d1} are asymmetrical. Thus making the first and last cells subjected to the highest injections and cell 9 to the lowest during DPI. In fact, the only best case is cell 9 and all the other cells are subjected to high injection levels thus increasing the numbers of cells for which the BMS IC could fail. To solve this issue, each C_d in Fig. 2 should be connected to ground for maximum symmetry, however, the cost is drastically increased as they would need to be rated for a larger voltage (100 V). Fig. 11 shows some solutions ((a), (b), (c), (d)) for the latter tradeoff. The proposed architectures are compared in terms of injection levels on the worst case and best case cells. In solution (a), the asymmetrical cells are cell 1, 9, 10 and 18. In fact the worst case cells are either cell 1 or cell 18. Cell 1 is chosen as worst case for solution (a). Moreover, in the exception of the aforementioned cells, all the others are symmetrical unlike Fig. 2, with no need of 100V rated capacitors. In solution (b), the asymmetrical cells are cell 1, 6, 7, 12, 13 and 18. In fact, for solution (b), the worst case cell is cell 1. Moreover, the solution (b) shares the same advantages as solution (a) with the exception of a slight increase in the number of asymmetrical cells. And, it allows using even lower voltage rated capacitors. Alternatively, solution (c) offers a middle ground between a perfect symmetry when all capacitors are connected to ground and Fig. 2. The goal of solution (d) is to evaluate if adding two capacitors to ground to Fig. 2 (cost limited) would lead to reasonable injection levels compared to the other architectures. In parallel, the injection levels on the best case cell in terms of symmetry of its traces and maximum level injected are presented for each architecture to assess their

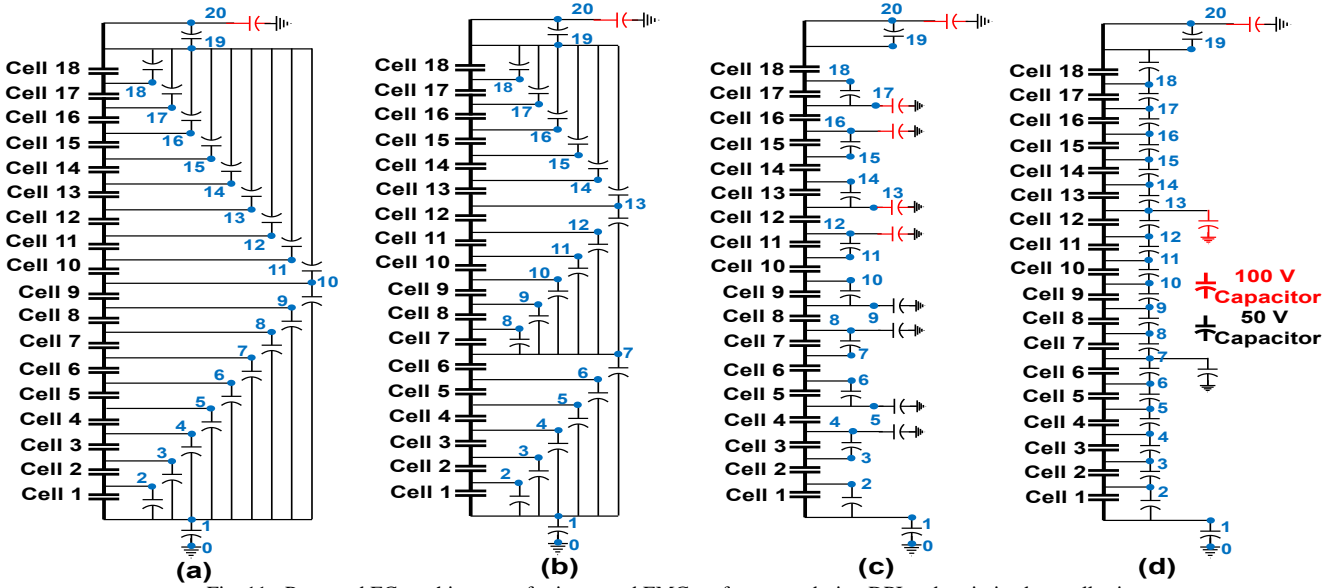


Fig. 11. Proposed ECs architectures for improved EMC performance during DPI and optimized overall price.

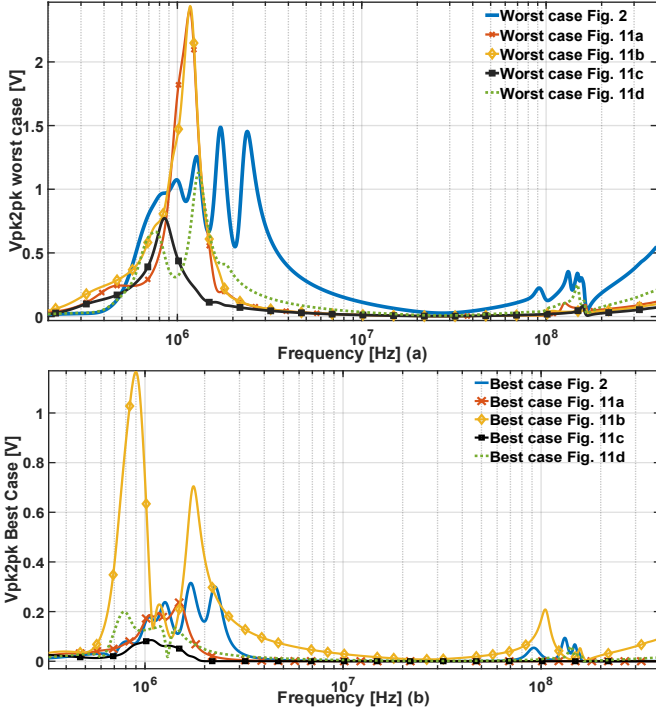


Fig. 12. Comparison of the architectures in Fig. 11 in terms of worst case and best case cells. (a) Worst case. (b) Best case.

potential. At last, to compare the architectures in Fig. 11, they were simulated in the same environment as Fig. 2. From Fig. 12a, solution (a) and (b) display a resonance at low frequencies. However, it is present only in the worst case cells while the others are relatively more symmetrical with considerably lower injections similarly to the best cases of solutions (a) and (b) in Fig. 12b as opposed to the case of Fig. 2 where nearly all the cells are compromised. Furthermore, from Fig. 12, solutions (c) and (d) have similar performances. In addition, they show better performance compared to the others. While the asymmetry of the traces in Fig. 2 has been alleviated with the proposed architectures, the ultra-capacitors now come into play in terms of the asymmetry. Concerning the cost, capacitors C_d in Fig. 2 or Fig. 11 handle up to 50V and still are cheaper than the 100V rated ones. If one assumes that each ultra-capacitors is around 5V, then solutions (a) and

(b) are as cheap as the ECs configuration of Fig. 2. Moreover, with respect to Fig. 2, better EMC performance can be obtained at the cost of adding one 100V capacitor and one 50V capacitor to ground (Fig. 11d) and an even more optimized performance with 4 additional 100V capacitors (Fig. 11c).

V. CONCLUSION

In this work, a measurement correlated model of the BMS IC is presented to be used for realistic DPI simulations. With respect to the cheapest configuration of the ECs, the root causes of the HSF are elaborated both in low and high frequencies. Moreover, an analytical approach on those frequencies is presented in order to predict them in the early definition stages, thus, guiding the design for an optimum EMC performance. Finally, alternative architectures are proposed to optimize the EMC during DPI with a consideration of the cost of the ECs. In future work, more architectures could be proposed and the impact of some functions of the BMS on the EMC performance will be analyzed.

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