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Performance Characterisation of the Decoupling Capacitor Network using the Near-Field Measurement

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Abstract — This paper describes a contactless method for evaluating the performance of a decoupling capacitor network and diagnose power integrity issues. A performance indicator is extracted for each capacitor from the near-field measurements (based on Z_{21} impedance measurement). Quantitative performance indicators extracted can provide in-depth analysis of the effect of the design of power network. The influence of each capacitor on the overall network impedance can be clearly identified and the impact of other contributors in the power network (PCB, IC and regulator) can also be analyzed. Using the near-field measurement allows to have a relevant approach (contactless, accurate and very wide band) to analyze decoupling capacitance network.

Keywords — Power Integrity, decoupling capacitor, power distribution network, Near-Field measurement.

I. INTRODUCTION

The demand for ever more functional, smaller and less consuming electronic devices requires the development of ever more innovative technologies. This one drives the development of the advanced System-on-Chips (SoC) that dramatically increase component density in an ever-shrinking space. The switching frequency increases with the data rate of signal (UCB-C Thunderbolt V3.0 @ 40 Gbit/s). Also driven by the environmental recommendations, the power supply voltage is decreased to limit power consumption and thermal issues.

In this context, the management of Power Integrity (PI) and Signal Integrity (SI) performance must be a challenge in order to limit electromagnetic interference (EMI) problems (noise propagation along power supply, edge radiation, eye pattern degradation, etc.). The power distribution network (PDN) delivers the supply voltage to the integrated circuits (IC). Due to the high frequency switching noise generated by the digital circuits and the complexity of the PDN, the loop inductors (traces, vias, pads, perforated planes) of Printed Circuit Board (PCB) interconnects can induce critical voltage variations on PDN. In order to limit the voltage variation, the PDN must have the lowest possible impedance.

To reduce the impact of PCB interconnect inductances, a large number of capacitors are added around the IC on the PDN. The Multi-layer Ceramic Capacitor (MLCC) technology provides short interconnect and small form factor packaging. This technology is widely used in the field of digital component decoupling. Usually, at least one capacitor per IC power supply pair is recommended.

During the design phase, a wide variety of commercial tools can help the designer to optimize the placement and routing of decoupling capacitors. However, it is more difficult to assess the performance of a given decoupling capacitor

network on a physical electronic board. All measurement approaches (such as the PDN impedance measurement [1][2], ripple voltage or eye diagram) require high frequency (HF) connections to the PDN. Implementing these HF connectors is not always easy on an industrial board and needs a complex de-embedding process for accurate HF measurements. These measurement methods are relevant to check performance constraints regarding PDN impedance target, maximum ripple voltage or the closing of eye diagram. However, in the event of non-compliance, these measurements do not provide enough information to quickly identify the real root cause.

The Near-Field Scan in emission (NFSe) is a well-known and contactless measurement to characterize and locate the emission sources. In this paper, the near-field probe coupling with MLCC capacitor package is used as a HF connector to capture impedance on the PDN. A performance factor is extracted for each decoupling capacitor using Z_{21} -parameter measurement (called Z_{21} NFSe). The quality of placement and routing, the choice of technology/package of the decoupling capacitors and the power/ground planes design efficiency can be assessed from the extracted performance factors.

The section II describes the Z_{21} NFSe measurement approach that is experimentally evaluating in the section IV. The section III presents the calibration process necessary to extract all performance indicators.

II. DEFINITION OF THE Z_{21} NFSE APPROACH

A. General Description

As shown by Fig. 1, the Z_{21} NFSe measurement approach, initially introduced by [3], uses two magnetic tangential (H_{xy}) probes connected to a Vector Network Analyzer (VNA). The first probe is located above a reference capacitor. The second probe is moved above the other decoupling capacitors. From the VNA, the Z_{21} -parameter is captured for each position of the second probe above the capacitors.

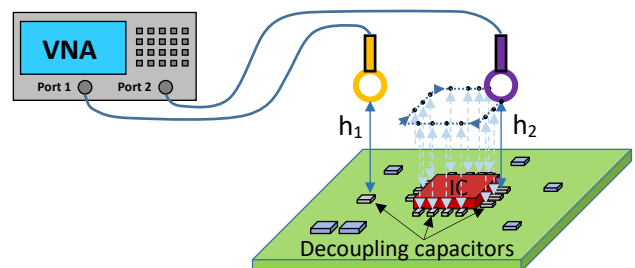


Fig. 1. Definition of the Z_{21} NFSe measurement setup.

A measurement, following the Z_{21} NFSe approach, was performed on the B-8a-2a1 demonstrator board implementing

a STM32H7 microcontroller with its decoupling capacitors network. The microcontroller is powered by a 3.3 V power supply through a SMA connector.

The measured Z_{21} transfer impedance depends on probe coupling to the capacitors and PDN impedance, given an indirect method to measure the impedance of the PDN. As the impedance provided by the decoupling capacitors and power planes is not dependent on bias voltage, the Z_{21} NFSe measurement does not need that the tested board is powered.

Fig. 2 shows the result of the mapping of the Z_{21} -impedance coupling between both probes through the decoupling capacitors captured during the measurement. First “static” probe is located under decoupling capacitor on the bottom side of PCB. The second probe is moved over the Top surface of PCB on each point to process the mapping shown on Fig. 2. The height of the two Langer “RF-R 0.3-3” magnetic tangential probes (with a loop diameter of 1 mm) has been set to 1mm above the decoupling capacitors.

These results show that, depending on the second probe orientation, the probe coupling on each capacitor can be localized. The Z_{21} -impedance coupling is highest when the second probe is centered above the capacitor. Moreover, the Z_{21} -impedance coupling gradient is high between two close capacitors. This validates that parasitic coupling with neighboring capacitors can be neglected.

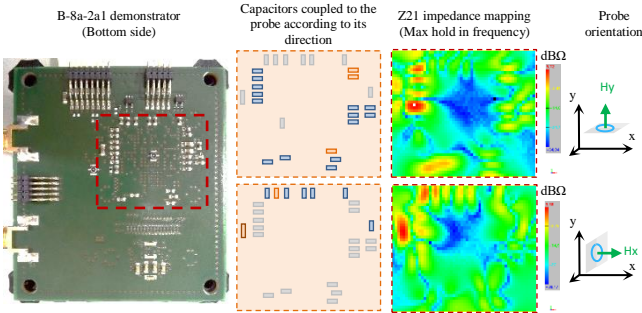


Fig. 2. Mapping of Z_{21} -Impedance coupling between probe and capacitor.

B. Modeling of the probe coupling to the PDN

Fig. 3 shows the equivalent circuit of the probe coupling to a MLCC capacitor. The coupling between the probe and the capacitor is bijective. Two modes can be observed:

- In emission mode, the current flowing through the probe loop induces a coupling on the capacitor, which can be modeled by an equivalent current generator in parallel of the Equivalent Serial Inductance (ESL) of the decoupling capacitor.
- In reception mode, the current flowing through the capacitor induces a coupling on the probe, which can be modeled by an equivalent current generator in parallel of the probe inductance.

In Z_{21} NFSe measurement approach, the first NF probe located above the reference capacitor (named C_k) is in emission mode. The port-1 of VNA injects a power through the NF probe-1. The excitation of the first probe leads to the generation of an equivalent current in parallel of the ESL inductance of the decoupling capacitor. The second NF probe is in reception mode. The current on the second decoupling capacitor induces an equivalent current generator in parallel of the probe-2 inductance. The coupling between the probes

and the capacitors can be seen as an input or output connector located between the V_{dd} and V_{ss} traces.

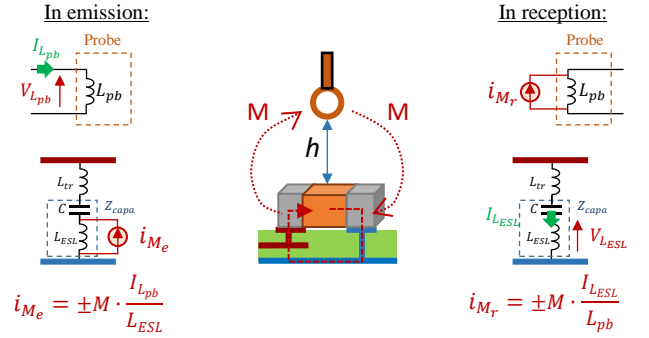


Fig. 3. Definition of the H_{xy} probe coupling on MLCC capacitor

As shown in Fig. 4, a series of parallel impedances can model each part of the power distribution network between V_{dd} and V_{ss} traces. Each part of the PDN is presented below:

- Z_{VRM} is the impedance of voltage regulator module and associated components.
- Z_{Cplan} defines all PCB interconnects as traces, pads, vias, ground/power planes (except those related to decoupling capacitor routing).
- $Z_{tr_i} = \{Z_{tr_k}, Z_{tr_{j=1..N}}\}$ defines the interconnect impedance (traces, pads, vias) to route the capacitor “i”.
- $Z_i = \{Z_k, Z_{j=1..N}\}$ defines the model of the capacitor “i”.
- $Z_{F_i} = \{Z_{F_k}, Z_{F_{j=1..N}}\} = Z_i + Z_{tr_i}$
- $\{\{Z_{Probe_1}\}; L_{pb_1}\}$ & $\{\{Z_{Probe_2}\}; L_{pb_2}\}$ defines the models of both used near-field probes.
- K_1 & K_2 defined the coupling factor between probe and capacitor.
- $L_{pkV_{dd}}, L_{pkV_{ss}}, C_{IC}$ et I_A defines the model of decoupled IC [4][5].
- P_1, R_{p1} and R_{p2} defined the two ports of the VNA

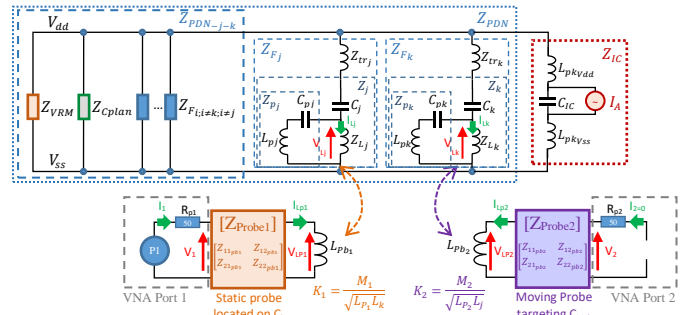


Fig. 4. Equivalent electrical model of the full PDN including both NF probes coupling.

In this model, it is assumed that V_{dd} and V_{ss} are a virtual equipotential. All interconnects of the decoupling capacitors (Z_{tr_i}) are defined in the Z_{F_i} impedances. The “K” mutual coupling models the coupling between the probe and the capacitor.

The expression (1) of the Z_{21} measurement provided the VNA, can be extracted from this model. Two identical terms, (2) and (3), can be identified in equation (1). The equations Z_{21_j} (2) and Z_{21_k} (3) represent the coupling between the

MLCC decoupling capacitor “ j ” and “ k ” with both respective NF probes.

$$Z_{21k,j; j=1..N} = \pm Z_{21j} \cdot Z_{21k} \frac{Z_{PDN}}{Z_{Fk} \cdot Z_{Fj}} \quad (1)$$

With:

$$Z_{21j} = \pm j\omega M_1 \frac{Z_{21Probe1}}{Z_{11Probe1} + Z_{Lpb1}} \left[\frac{Z_{pj}}{Z_{Lj} + Z_{pj}} \right] \quad (2)$$

$$Z_{21k} = \pm j\omega M_2 \frac{Z_{21Probe2}}{Z_{11Probe2} + Z_{Lpb2}} \left[\frac{Z_{pk}}{Z_{Lk} + Z_{pk}} \right] \quad (3)$$

The first part of these equations is related to the probe impedance itself and the height of measurement ‘ h ’ through the M parameter: the mutual inductance between the probe and the MLCC. The last part of these equations, between square bracket, is related to the technology and package of the decoupling capacitor. These both impedance parameters (2) and (3) can be extracted from calibration process described in section III.

The calibration process allows extracting both calibration impedance Z_{21j} (2) and Z_{21k} (3). With the knowledge of the first decoupling capacitor impedance (Z_{Fk}) targeted by the probe-1, the performance factor of each decoupling capacitor “ j ”, given by (4), can be extracted from (1).

$$K_{Z21j; j=1..N} = Z_{Fk} \cdot \left[\frac{Z_{21k,j; j=1..N}}{Z_{21j} \cdot Z_{21k}} \right] = \frac{Z_{PDN}}{Z_{Fj}} \quad (4)$$

The performance factor K_{Z21j} allows evaluating the influence of any decoupling capacitor “ j ” on the global impedance Z_{PDN} . If the factor K_{Z21j} tends to one, the decoupling capacitor “ j ” strongly influences the global impedance Z_{PDN} . Else if K_{Z21j} tends to zero, the capacitor “ j ” does not have a significant influence on Z_{PDN} .

According to the topology of the full PDN model presented in Fig. 4, (5) gives the expression of the global PDN impedance.

$$\frac{1}{Z_{PDN}} = \left(\frac{1}{Z_{VRM}} + \frac{1}{Z_{Cplan}} + \frac{1}{Z_{IC}} \right) + \frac{1}{Z_{Fk}} + \sum_{j=1}^N \frac{1}{Z_{Fj}} \quad (5)$$

With:

$$Z_{IC} = Z_{LpkVdd} + Z_{LpkVss} + Z_{CIC} \quad (6)$$

Merging (4) and (5) leads to the definition of a new performance indicator given by (8).

$$K_{Z21Net} = \frac{Z_{PDN}}{Z_{VRM}} + \frac{Z_{PDN}}{Z_{Cplan}} + \frac{Z_{PDN}}{Z_{IC}} \quad (7)$$

$$K_{Z21Net} = 1 - \left(\frac{Z_{PDN}}{Z_{Fk}} + \sum_{j=1}^N K_{Z21j} \right) \quad (8)$$

The performance factor K_{Z21Net} allows evaluating the influence on Z_{PDN} of all the other contributors of the power distribution network (except the decoupling capacitors) such as PCB, IC and regulator module.

The performance factors for each decoupling capacitor K_{Z21j} completed with K_{Z21Net} provide quantitative indicators to evaluate the quality of the PDN (routing and choice of technology/package of the decoupling capacitors and the power/ground planes design efficiency).

III. CALIBRATION PROCESS OF Z_{21} NFSE APPROACH

The calibration process requires developing a specific demonstrator in order to extract $Z_{21i} = \{Z_{21j}; Z_{21k}\}$. As shown in Fig. 5, the decoupling capacitors are mounted on a specific demonstrator. The capacitors are connected, by a calibrated trace, through an SMA connector link to the port-1 of the VNA. The probe is connected to the port-2 of the VNA.

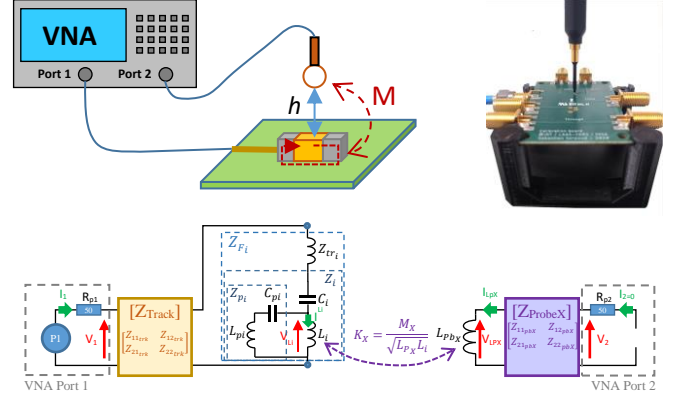


Fig. 5. Definition of “the probe/capacitor coupling” calibration process based on a specific demonstrator.

As is described in section II, Z_{21i} is related to the probe impedance (link to the design of probe), the height of measurement ‘ h ’ and the technology and package of the decoupling capacitor used. Therefore, a parameter Z_{21i} must be extracted for each couple capacitor technology and probe used. Two types of decoupling capacitor are used on the B-8a-2a1 demonstrator:

- C_{100nF_0402} : 100 nF MLCC capacitor mounted in 0402 package
- $C_{2.2\mu F_0603}$: 2.2 μ F MLCC capacitor mounted in 0603 package

The Z_{21} NFSe measurement approach requires using two probes. In our application, the probe-2 is located on the capacitor $C_{2.2\mu F_0603}$. The probe-1 moves to target all others decoupling capacitors (C_{100nF_0402} or $C_{2.2\mu F_0603}$). In this context, three calibration impedances are needed ($Z_{21i} = \{Z_{21Probe2-C_{2.2\mu F_0603}}; Z_{21Probe1-C_{2.2\mu F_0603}}; Z_{21Probe1-C_{100nF_0402}}\}$).

According to the model of the calibration process presented in Fig. 5, (9) gives the expression of Z_{21} -parameter measurement captured by the VNA.

$$Z_{21cal_i} = \pm j\omega M_x \frac{Z_{21ProbeX}}{Z_{LpbX} + Z_{11ProbeX}} \left[\frac{Z_{pi}}{Z_{Li} + Z_{pi}} \right] \frac{Z_{21track}}{Z_{Fi} + Z_{22track}} \quad (9)$$

The first part of (9) is equal to Z_{21i} . The last part of (9), $\frac{Z_{21track}}{Z_{Fi} + Z_{22track}}$, represents the effect of the calibrated trace (connected between the SMA connector and the decoupling capacitor). With the knowledge of the calibrated trace model, it is possible to de-embed [7] this last part of (9) to extract Z_{21i} from Z_{21cal_i} .

Z_{21cal_i} depends of the height “ h ” of the measurement between the bottom of probe loop and the top of the decoupling capacitor. Fig. 6 shows Z_{21cal_i} for several “ h ” ($h = \{0; 0.5; 1; 1.5; 2; 3; 4; 5; 7.5; 10\} [mm]$).

As it is visible in Fig. 6, to ensure good measurement sensitivity, the height must be as lower as possible. The height “ h ” is fixed to the same value ($h = 0.5 \text{ mm}$) during all measurements.

Note: using a low noise amplifier (LNA) (not done here) can improve the sensibility of the measurement.

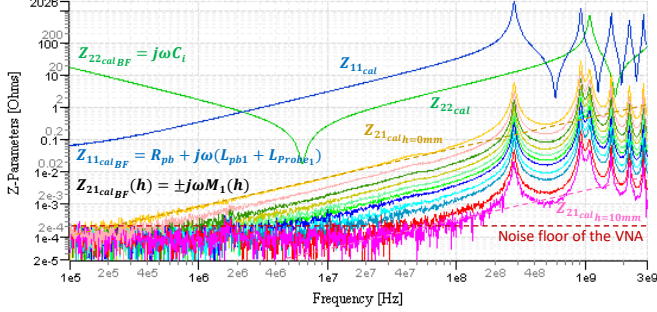


Fig. 6. Z-parameters measurement on a calibration demonstrator.

From the full Z-parameters measurements made on the calibration board, shown in Fig. 6, some other interesting information can be extracted:

- M_X : defined the mutual coupling between the capacitor and the NF probe. M_X can be extracted from $Z_{21_{cal_i}}$ in low frequency $\rightarrow M_X = \frac{|Z_{21_{cal_iBF}}|}{\omega}$.
- The C_i value of the capacitor can be extracted from the $Z_{11_{cal_i}}$ parameter in low frequency $\rightarrow C_i = \frac{|Z_{11_{cal_iBF}}|}{\omega}$.
- The DC probe resistance R_{pb_1} as well as the probe loop inductance and the access inductance $L_{pb_1} + L_{Probe_1}$ can be extracted from $Z_{22_{cal_i}}$ at low frequency.

IV. EXPERIMENTAL VALIDATION OF PROPOSED APPROACH

A. Definition of the demonstrator

An experimental validation has been done on the B-8a-2a1 demonstrator. In this version, the microcontroller is not mounted and only five capacitors was mounted as described in Fig. 7. These five capacitors have been scattered around the microcontroller pattern, with one capacitor ($C_k = C_{2.2\mu F_0603}$) on the top side and four capacitors ($C_a = C_{2.2\mu F_0603}$ and $\{C_b; C_c; C_d\} = C_{100nF_0402}$) on the bottom side.

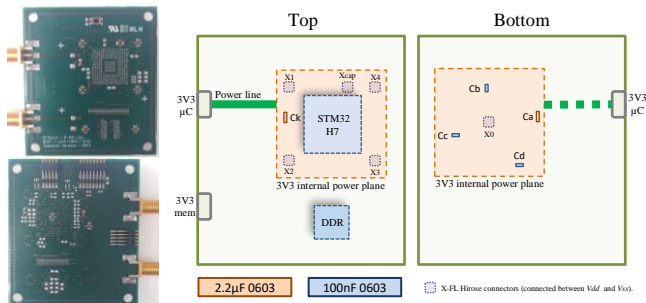


Fig. 7. Definition of the « B-8at-2a1-PCB+5xCapas » demonstrator.

In order to simplify the analysis of the results, the power supply and the microcontroller are not present on « PI B-8at-2a1-PCB+5xCapas » demonstrator ($\rightarrow Z_{VRM} = Z_{IC} = \infty$). In this context, the $K_{Z21_{Net}}$ performance factor is only related to

the performance of all PCB interconnects as traces, pads, vias, and ground/power planes represented by the Z_{Cplan} impedance.

B. Preliminary analysis of the PDN impedance

In order to process a first performance analysis of the PDN impedance, including its decoupling capacitors, the impedances of each capacitor and the impedance Z_{Cplan} of the PCB were modeled from the impedance measurement according to the Z_{21} -method [6]. The impedance of decoupling capacitor is measured from specific extraction board implemented each type of decoupling capacitor. Z_{Cplan} is extracted from measurement on specific version of « B-8at-2a1-PCB » demonstrator, where only all “X-FL Hirose” connectors (X_0, X_1, X_2, X_3, X_4) are soldered. From (5), Z_{PDN} impedance was extracted as shown in Fig. 8.

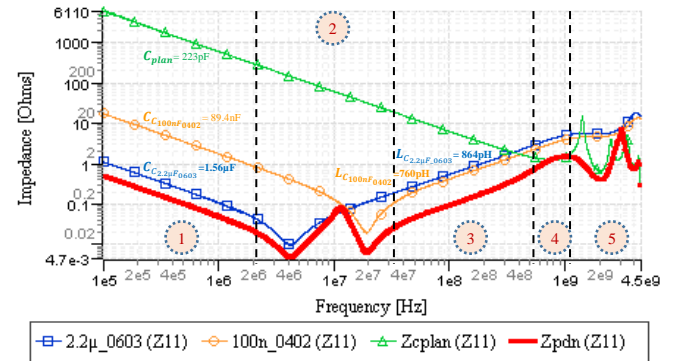


Fig. 8. Impedance of the decoupling capacitors.

A short analysis allows defining five ranges according to the influence of each contributor of the PDN. Following the range, the PDN impedance is driven by:

- Range (1): high influence of the intrinsic value of the decoupling capacitors: $C_i = \{C_k, C_j; j=1..N\}$.
- Range (2): resonance between the parasitic inductance and the intrinsic value of the decoupling capacitors.
- Range (3): high influence of the parasitic inductance of the decoupling capacitors.
- Range (4): resonance between the parasitic inductance of the decoupling capacitors and Z_{Cplan} . Remark: Here this resonance is not very marked because the access inductance (routing) of the decoupling capacitors is not taken into account.
- Range (5): high influence of Z_{Cplan} (PCB plans resonances).

C. Analysis of the proposed performance indicators

The test bench setup presented in Fig. 9 is used to capture Z-Parameters on the « B-8at-2a1-PCB+5xCapas » demonstrator. A robot is used to move the probe-1 at 0.5 mm above the center of each decoupling capacitor. The static probe-2 is centered at 0.5 mm above the C_k capacitor located of the bottom of board.

The proposed method does not require capturing a mapping of Z_{21} -Impedance measurement as presented on Fig. 2. Only “ j ” measurements are necessary. The normal orientation of probe is perpendicular to the length of the

capacitor package. Therefore, measurements on the "j" capacitors can be carried out in less than 5 minutes.

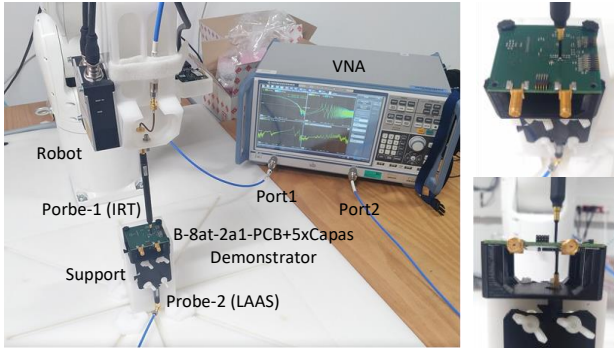


Fig. 9. $Z_{21}NFSe$ measurement setup on « B-8at-2a1-PCB+5xCapas » demonstrator.

Fig. 10 shows the Z-Parameters measurement results performed on all "j" decoupling capacitors. In low frequency, below 10 MHz, a limitation of this approach due to the sensibility of de NF probe coupled to the VNA. As already mentioned in the previous section, a LNA could be used to increase the sensitivity and extend the method bandwidth in low frequency. However, it is not here a hard limitation. In general, optimizing PI integrity below 10 MHz does not present a problem. The main field of interest is above 100 MHz.

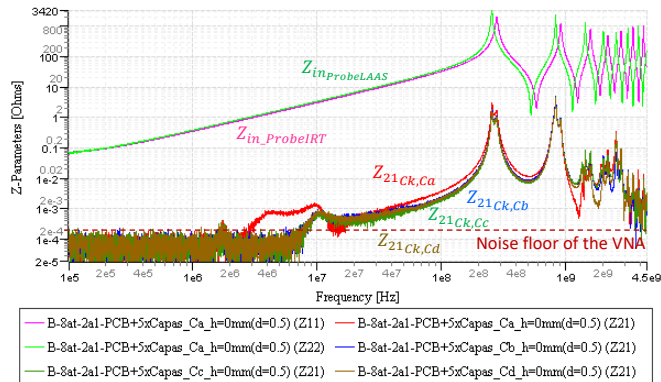


Fig. 10. Z-Parameters measurement on « B-8at-2a1-PCB+5xCapas » demonstrator.

According to equation (4) and after de-embedding by Z_{21_i} , the performance factors $K_{Z21_j; j=1..N}$ can be extracted as shown on Fig. 11. In order to help analysis of the performance factors $K_{Z21_j; j=1..N}$, a color line on the top of Fig. 11, sets the color of the curve, which has a higher value than the others.

In range 2, the performance factors $K_{Z21_j; j=1..N}$ show resonance of the PDN impedance ($Z_{21_i} > 0$) visible in Fig. 8. The paralleling of the decoupling capacitors generates resonance that decrease performance of the global decoupling capacitor network. The performance indicators highlight the Ca capacitor as the main contributor of this resonance ($K_{Z21_1} \gg \{K_{Z21_2}, K_{Z21_3}, K_{Z21_4}\}$).

In range 3, the performance factors show that the capacitor Ca mainly drives the global impedance of the PDN (Z_{PDN}). This result may seem strange if we look at the value of the parasitic inductance of the different capacitors (C_{100nF_0402} and $C_{2.2\mu F_0603}$) presented in Fig. 8. Measurement on these

decoupling capacitors shows that the capacitor $C_{2.2\mu F_0603}$ has a parasitic inductance $L_{ESL_{Ca}} = 864pH$ while the capacitor C_{100nF_0402} have a parasitic inductance $L_{ESL_{Cb}} = L_{ESL_{Cc}} = L_{ESL_{Cd}} = 760pH$. Thus, the decoupling capacitors C_{100nF_0402} should contribute more strongly to reduce Z_{PDN} than $C_{2.2\mu F_0603}$ which has a larger parasitic inductance value.

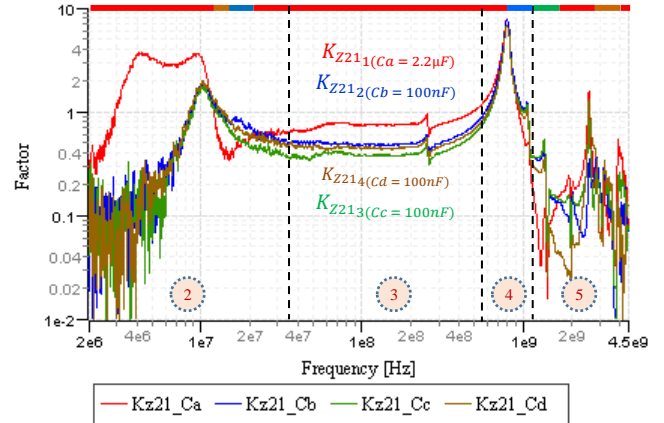


Fig. 11. The performance factors $K_{Z21_j; j=1..N}$.

Fig. 12 shows an overview of the decoupling capacitors routing. All C_{100nF_0402} capacitors are routing using two vias to connect them to the power and ground planes. Both $C_{2.2\mu F_0603}$ are routing using four vias. Consequently, the access impedance Z_{tr_k} is half for the capacitors $C_{2.2\mu F_0603}$ compared to the capacitors C_{100nF_0402} .

In range 4, the performance factors are well above the value one. This identifies the presence of a resonance, in this frequency range, between the parasitic inductance of the decoupling capacitors and $Z_{C_{plan}}$. This resonance has a significant impact on the power supply instability. Therefore, it is important to identify the possible resonances and in the present case to identify their origins. Here, the fact that all $K_{Z21_j; j=1..N}$ performance factors are equal means that all capacitors contribute equally to this resonance.

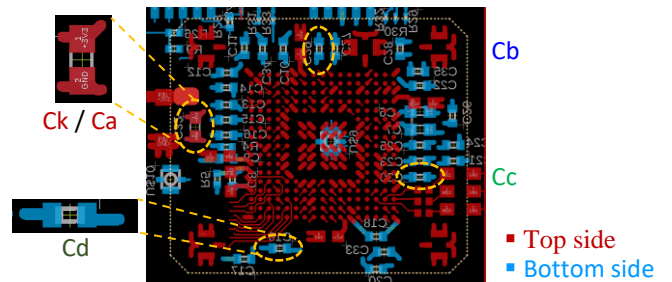


Fig. 12. Overview of the decoupling capacitors routing.

In range 5, all performance factors $K_{Z21_j; j=1..N}$ are much less than one. This means that all decoupling capacitors have very little influence on the Z_{PDN} impedance. In this range, the impedance of PCB defined by $Z_{C_{plan}}$ (here $Z_{VRM} = \infty$ and $Z_{IC} = \infty$) drives chiefly the global Z_{PDN} impedance.

Fig. 13 presents an extract of the performance factors $K_{Z21_j; j=1..N}$ from Fig. 11 for the specific frequency range 5. A resonance around 2.58 GHz can be observed. From the performance factors, the capacitors Ca and Cd are mainly at the origin of this resonance.

The PI analysis on the « B-8at-2a1-PCB+5xCapas » demonstrator is easy due to the low complexity of the design. It would certainly not be same on an industrial application, using a powerful microprocessor with several supply voltages and dozens of decoupling capacitors using different technologies and packages. Nevertheless, the short measurement and processing time ensures a quick deep analysis without any knowledge about PCB routing and decoupling capacitors.

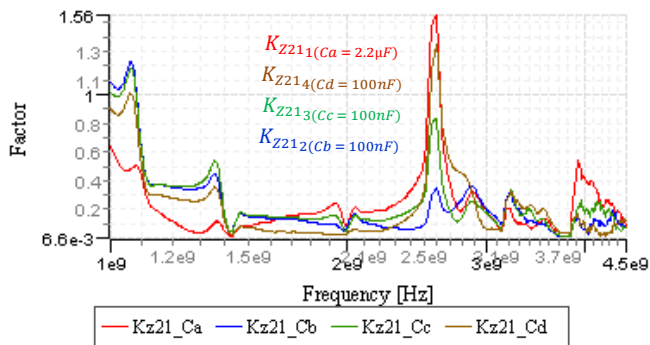


Fig. 13. The performance factors K_{Z21j} ; $j=1..N$ – Frequency range 5

V. CONCLUSION

This article proposes a novel approach to evaluate quickly the performance of the power distribution network of a digital device over a wide frequency range. This approach is based on the near-field scan method using the Z_{21} -parameter measurement. Two NF probes are used to access the PDN through the MLCC decoupling capacitors, which are equivalent to two virtual RF connectors connected in parallel to the MLCC. This contact-less measurement can be easily applied on any industrial application without the limitation of implementing RF connectors on the design.

The definition of quantitative performance factors for each decoupling capacitor greatly facilitates the analysis of a bad routing or choice of decoupling capacitors without any knowledge on the design. Where common approaches are

only dedicated to the PI conformity checking, the performance factors extracted from the Z_{21} NFSe measurement approach allow to precisely identifying the real root cause of PI issues in order to fix them.

The definition of the performance factor K_{Z21Net} completes the analysis of the impact of the other contributors of the power distribution network (PCB, IC and regulator).

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