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Passive Cell Balancing Impact On Injection Levels During Direct Power injection on Battery Management System

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Abstract— When it comes to the electromagnetic interference (EMI) immunity of a Battery Management System Integrated Circuit (BMS IC), Printed Circuit Board (PCB) traces and external components (ECs) arrangement are crucial. The impedance presented by the BMS IC is also a key factor. In fact, such impedance is greatly altered by the cell balancing function of the BMS IC. More specifically, the integrated passive cell balancing function in most commercially available BMS ICs greatly reduces the impedance presented by the BMS IC. This work aims at investigating the impact of different passive cell balancing approaches on the immunity level of the BMS IC. Then a new BMS IC architecture is presented that not only reduces the number of ECs but also allows the passive cell balancing to have the most impact on the immunity of IC, i.e. the injections levels during DPI tests. Thus, the IC can maintain a high voltage measurement accuracy in noisy environments.

Keywords— BMS; PCB; Battery; Immunity; DPI; Resonance; Noise levels; EMC; Ladder Networks.

I. INTRODUCTION

Lithium Ion (Li-Ion) batteries as well as BMS [1] have been subject to extensive research to pave the way for the new generation of Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV). One major aspect of development, for example, is the characterization of the conducted EMI coming from the drive inverter which is one of the noise sources that can act as an aggressor to the BMS IC. In this noise path the cables, PCB traces and ECs highly contribute to the immunity of the BMS IC. The ECs of interest are automotive high voltage rated capacitors that are placed for protection against electrostatic discharges (ESD). As shown in previous work [2], the cheapest configuration of these ECs is a differential connection across the battery cell. However, this leads to an increase of injection levels due to introduced resonances in the DPI [3] frequency range ([150 kHz; 1 GHz]). As shown in [2], the resonances are due to the constructed C-L ladder network. In this case, the passive cell balancing, when activated, places the cell balancing resistor as well as some parasitics in parallel with the ESD capacitor which can alter the attenuation level of those resonances. In this work, two cell balancing approaches are considered. The first approach consists on shorting all the cells that can be shorted in the exception of the cell that the BMS IC is currently measuring. The injected levels during DPI on the measured cells are then extracted to evaluate the impact of this approach on the Immunity of the IC. Moreover, this work compares two architectures with this first balancing approach where the main difference between them is the number of cells that can be balanced

simultaneously. The second balancing approach consists on shorting the same cell that is currently being measured by the IC in a specifically proposed architecture. Furthermore, the proposed architecture turns the ESD capacitor into a filter thanks to a new placement of the balancing resistors. This enables the balancing to drastically reduce the impedance seen on the BMS IS side, thus reducing the injection levels. Additionally, to evaluate the impact of the parasitic inductances, the impact of the cell balancing is evaluated with different distances between the ESD capacitor and the IC. Finally, this paper is organized as follows: First, the modeling of the BMS IC environment is presented. Secondly, using a first cell balancing approach, two BMS IC architectures are compared in terms of the balancing impact on injection levels during DPI. Thirdly, the proposed architecture is presented and the balancing impact on the injection levels during DPI is evaluated with a second balancing approach.

II. MODELING OF THE BMS IC ENVIRONMENT

The main purpose of a BMS is to ensure the optimum and safe operation of the battery even under a harsh EMI environment. Some of the main functions of a BMS IC are to perform accurate cell voltage measurement and passive cell balancing [1] to prevent battery cell degradation and enable optimum power extraction from the battery pack. To characterize the ability of the IC to perform those tasks in a harsh EMI environment, DPI tests are performed where 30 dBm is coupled in a CM way onto all the IC's inputs that connect to the battery cells. Fig.1 shows the DPI setup used in this work with a BMS IC product that monitors up to 18 battery cells. In this setup, ultra-capacitors are introduced to be able to use 12 V batteries to build the pack (>80 V) and also provide a stabilization of the impedance seen on the pack's side.

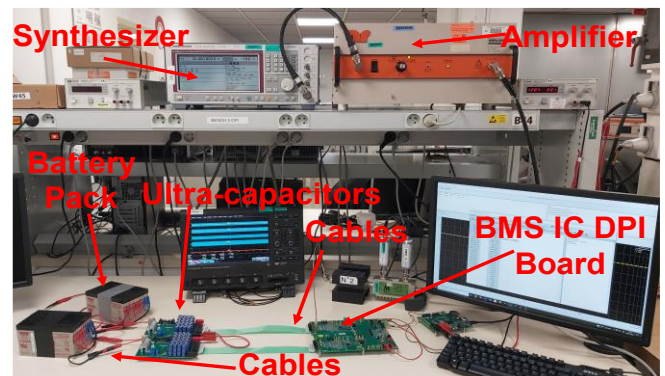


Fig. 1. BMS DPI test bench.

From Fig. 1, the elements of interest in this on-hand modeling approach are the following: the cables (30 cm both on the battery pack and PCB sides), the ultra-capacitors, the connectors, the PCB traces (both on the ultra-capacitors board and BMS IC board), the ECs on the BMS IC board and finally the impedance presented by the BMS itself. The goal of this section is to model the BMS environment in order to build a realistic simulation setup to be used in the comparisons of this work. From Fig. 2, the BMS IC input is modeled by capacitors C_L (30pF) representing the internal passive cell balancing switches [1]. The ON resistance of these switch is $R_{on} = 0.25 \Omega$. The capacitors C_d (47nF) are the ECs of interest which are placed for ESD purposes in the cheapest configuration [2]. The parasitic resistance and inductance of C_d are also included in the model. In fact, since these parasitics are more pronounced in high frequencies, the parasitic resistance R_d of C_d is taken at 100MHz and above. In a similar way, the parasitic behaviors of the injection capacitor C_i (330pF) are also considered. When it comes to the cables and PCB traces, their capacitive effect is not taken into account due to the presence of relatively higher value capacitors (C_d). Table 1 associates each parameter on Fig. 2 with the elements on Fig. 1. Furthermore, the battery is modeled by an ideal voltage source as the pack and cables are shorted by the ultra-capacitors. From Fig. 2, all the parameters are similar for the 18 cells neglecting the mismatches on the distances from each cell to the IC pins. Finally, this model is taken as valid in the range of [150kHz, 200 MHz].

Concerning the IC pins, the architecture 1 has C_{Bx} pins destined for cell voltage measurement and passive cell balancing. And, C_{Tx} pins are only destined for a redundant voltage measurement of the cells. In fact, measurements through C_{Tx} are performed by a discrete time (DT) analog to digital converter (ADC), thus, the need of an anti-aliasing filter (AAF), i.e., R_f and C_f . Measurements through C_{Bx} pins are performed by a continuous time (CT) ADC, thus, not needing any AAFs. Finally, in the next section the architecture 2 will be presented as well as the first balancing approach used in this work in order to improve the immunity of the BMS IC. Additionally, Architectures 1 and 2 will be compared in terms of the attenuation of injection levels that the first approach of

passive cell balancing brings. Additionally, when balancing is activated in this work, it is supposed to last for a few hundred microseconds, i.e., long enough to perform voltage measurement on the cell of interest, thus, not greatly impacting the state of charge of balanced cells.

TABLE 1. Parameters of BMS IC environment model during DPI.

Parameter (Fig. 2)	Modeled Element (Fig. 1)
R_c, L_c	Cables between pack and Ultra-caps ($R_c=0.2 \Omega, L_c=300n$)
C, ESR, ESL, R_{leak}	Ultra-caps (10F), parasitic resistance ($ESR=0.1 \Omega$), parasitic inductance ($ESL=60 nH$) and leakage resistance (100 k Ω)
R_u, L_u	Traces on the ultra-caps PCB ($R_u=0.05 \Omega, L_u=12 nH$)
R_0, L_0	Cables between ultra-caps PCB and BMS PCB (30cm) and 2 connectors ($R_0=0.3 \Omega, L_0=318nH$)
R_a, L_a	Traces from connector to injection point on BMS IC PCB. ($R_a=0.04 \Omega, L_a=20nH$)
L_1	Traces between injection point and capacitor C_d ($L_1=1nH$)
R_i, L_i	Traces between C_i and the injection point ($R_i=0.013 \Omega, L_i=1.62nH$)
R_d, L_d, L_{d1}	The parasitic resistance and inductance of C_d (not represented in Fig. 2). And L_{d1} the parasitic inductances of C_{d1} ($R_d=0.07 \Omega, L_d=0.68 nH, L_{d1}=0.82 nH$)
L_2, L_3	L_2 is the traces between C_d and the Node split. L_3 is the distance between R_b or C_f to the IC. ($L_2=21 nH, L_3=46 nH$)
R_b	Passive cell balancing resistor (11 Ω)
C_f, R_f	They make up the anti-aliasing filter ($R_f=10 k\Omega, C_f=47 nF$).

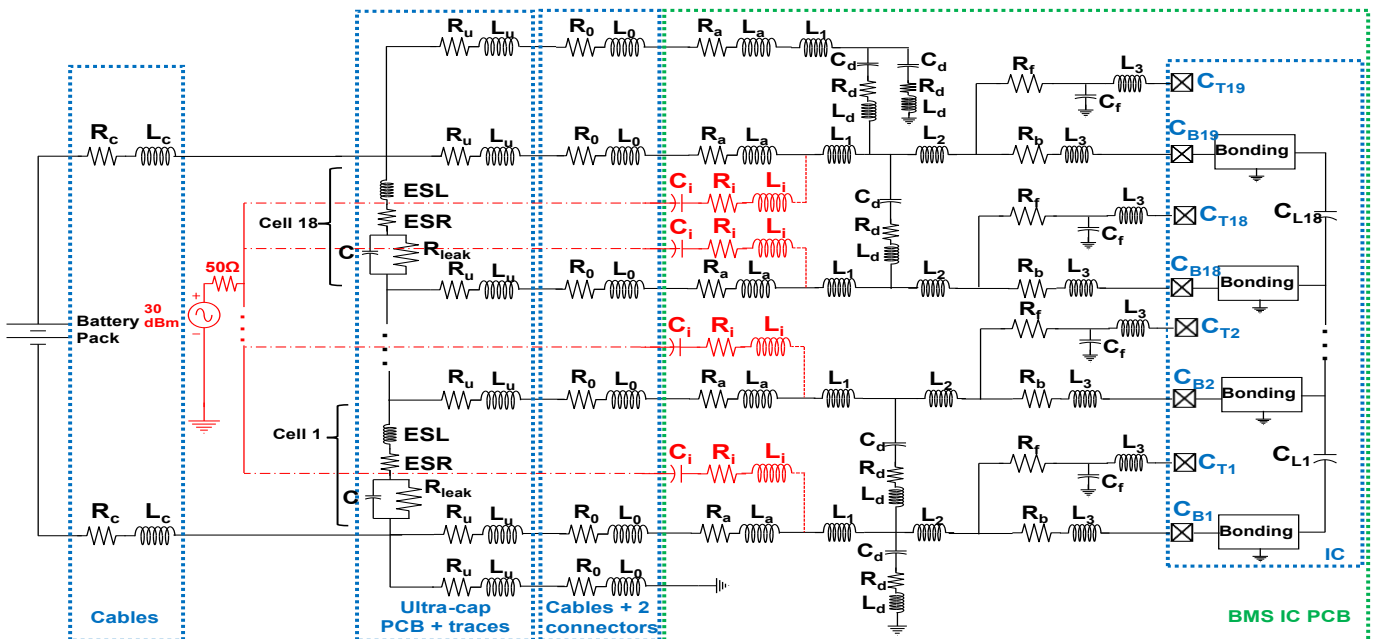


Fig. 2. Modeling of Architecture 1 of the BMS IC and its environment during DPI tests.

III. FIRST PASSIVE CELL BALANCING APPROACH IMPACT ON DPI INJECTED LEVELS

The architecture of the BMS IC in terms of Pinout, number and types of used ADCs directly impacts the outside components. Indeed, in the architecture 1 (Fig. 2), each C_{Bx} pin is shared among two cells in the exception of C_{B0} and C_{B19} . Since R_b needs to be present on each PCB trace leading to a C_{Bx} pin to limit the common mode (CM) to differential mode (DM) conversion during DPI tests, two adjacent cells cannot be balanced simultaneously. Therefore, the odd and even cells are balanced in different cycles. Alternatively, architecture 2 (Fig. 3) has extra C_{Bx_H} pin that allows the balancing of two adjacent cells. However, this increases IC die size, number of pins and external components (R_b).

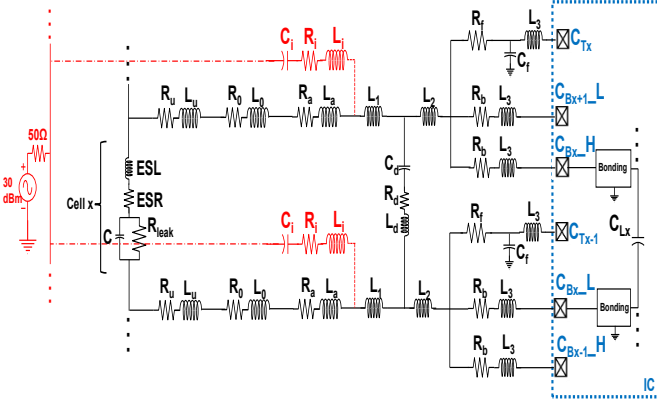


Fig. 3. Modeling of Architecture 2 of the BMS IC and its environment during DPI tests.

As shown in [2], the C-L ladder network composed of $L_T = L_u + L_0 + L_a$ (Fig. 2) and C_d is causing a number of resonances. These resonances are placed in relatively low frequencies (under 10 MHz) which makes them costly to filter. In fact, in realistic applications, the cables connecting the BMS IC to the battery pack can extend up to 2 meters thus not only pushing these resonances even lower in frequency but also increasing their quality factor. While the presence of $R_T = R_u + R_0 + R_a$ does attenuate somewhat the resonances, it is still not sufficient. One aspect of this work is, then, to investigate other methods to introduce more attenuation to the low frequency resonances without having to add more external components. A second aspect of this work is also to analyze the impact of such approaches on the high frequency resonances and injection levels. When cell balancing is not activated, L_2 , R_b and L_3 can be neglected due to the fact that $C_d \gg C_L$ and that the resonances are sufficiently lower in frequencies. Therefore, R_b doesn't interfere in the attenuation of the resonances. However, when cell balancing is activated C_L is replaced by R_{on} (0.25Ω), i.e., R_b as well as inductive parasitics are now in parallel with C_d . R_b is now helping attenuating the resonances.

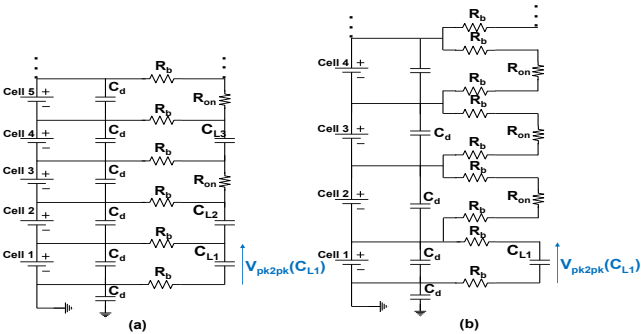


Fig. 4. First balancing approach on architecture 1 and architecture 2.

The first balancing approach considered in this work consists on extracting the peak-to-peak voltage on the first cell (C_{L1}) during DPI simulations while the other cells are being balanced. In the case of the first architecture, only the odd cells are balanced in the exception of cell 1 (Fig. 4a). Balancing the even cells starting from cell 2 hasn't been considered in this case because the DC on cell 1 would change, thus, not reflecting a realistic measurement scenario of cell 1. Concerning the second architecture, since it enables the balancing of adjacent cells, all the cells in the exception of cell 1 are balanced. Furthermore, in order to extract $V_{pk2pk}(C_{L1})$ in a spice environment, transient simulations were performed where:

- Enough periods were given to the signals to settle (above 500 periods) before extracting any data.
- $V_{pk2pk}(C_{L1})$, is extracted as an average on the peak-to-peak voltage over the last 50 periods of the signal for each injected frequency.
- A sufficient number of points per decades were taken in the range of [150 kHz; 200 MHz] (200 pts/decades).

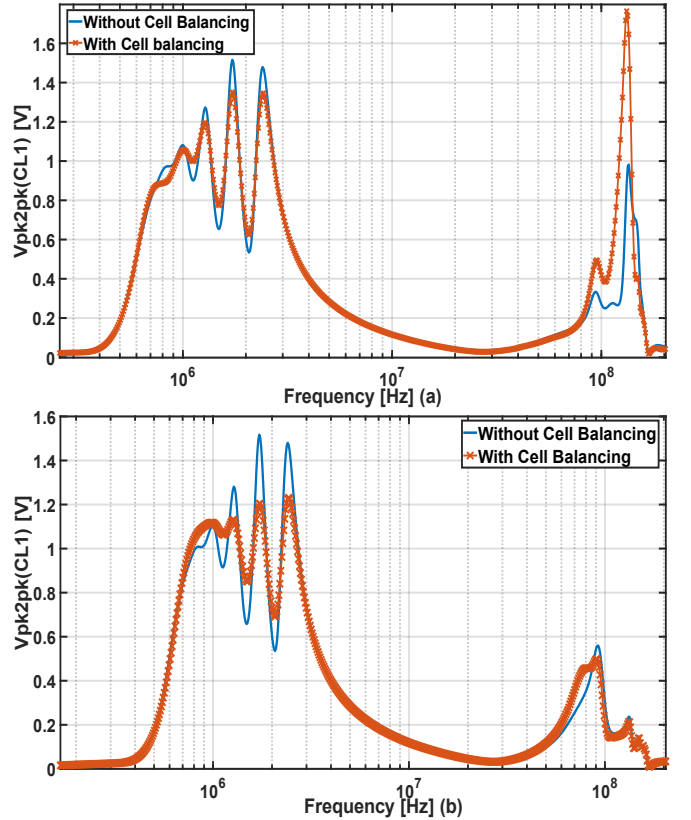


Fig. 5. First cell balancing approach impact on injection levels during DPI with architectures 1 and 2 with $R_b = 11 \Omega$. (a) Architecture 1. (b) Architecture 2.

From Fig. 5a, passive cell balancing does indeed reduce the amplitude of the resonances in low frequencies as expected. However, an increase in injection levels is noticed in high frequencies (around 150 MHz). From [2], one of the major contributors to high frequency resonances is the C-L ladder network constituted of $\{L_2, L_3, R_b\}$ and C_L in architecture 1. And since the architecture 1 can't balance all the cells simultaneously by construction, then the balancing doesn't entirely remove the ladder network composed of $\{L_2, L_3, R_b\}$ and C_L . When it comes to the architecture 2, Fig. 5b shows that the cell balancing has a higher impact in the

injection levels at low frequencies compared to architecture 1 (Fig. 5a). This can be explained by the fact that more cells are able to be balanced simultaneously by the architecture 2. Thus, introducing more damping. Concerning higher frequencies, it can be seen that the architecture 2 inherently shows lower injection levels at high frequencies without activating the cell balancing. This is because R_b is placed in the path between C_{L_x} and $C_{L_{x+1}}$ (Fig. 3). With the cell balancing activated, only a slight improvement is noticed in high frequencies (Fig. 5b). Clearly, the architecture 2 enables the cell balancing to have a better impact of injection levels in both high and low frequencies compared to the first architecture. Furthermore, this balancing approach seems not to greatly impact the resonances caused by the parasitics on the cell that is currently being measured by the BMS IC (C_{L1}). One may wonder about the impact of the cell balancing resistor value on the cell balancing impact on injection levels. Indeed, passive cell balancing does introduce a damping on the low frequency resonances, however, it can be easily deduced that if R_b is too high then it won't be greatly impacting C_d when cell balancing is activated.

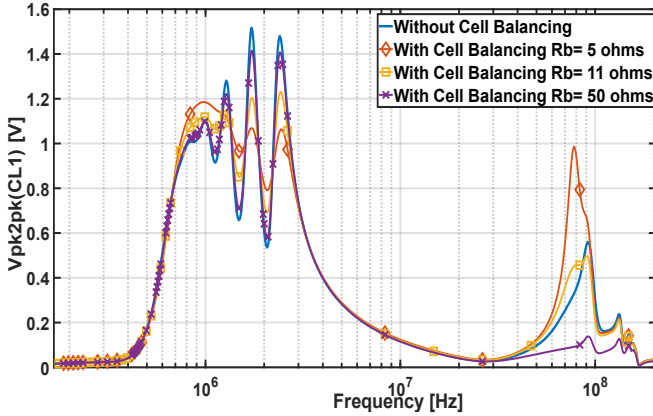


Fig. 6. Cell Balancing impact on injection levels during DPI with architecture 2 and different values of R_b .

From Fig. 6, lowering R_b leads to greater attenuation of some low frequency resonances that are introduced because of the ladder network compared to the case of $R_b=11 \Omega$. However, this leads to a lower attenuation of the high frequency resonances caused by $\{L_2, L_3, R_b\}$ and C_L on the currently being measured cell by the BMS IC. Thus an increase of injection levels in high frequencies as seen in Fig. 6 for $R_b = 5 \Omega$ compared to when the cell balancing is not activated. Alternatively when R_b is increased, lower attenuation of the low frequency resonances is observed as R_b of 50Ω has less impact on C_d than $R_b = 11 \Omega$. However, the high frequency resonances are now better attenuated. Therefore, the value of R_b raises a trade-off between the attenuation of the low and high frequency resonances when it comes to this first balancing approach.

IV. SECOND PASSIVE CELL BALANCING APPROACH IMPACT ON DPI INJECTION LEVELS WITH NEW PROPOSED BMS IC ARCHITECTURE

In the previous section, a first cell balancing approach showed some attenuation levels when it comes to the low frequency resonances during DPI which can be the most expensive and hardest to filter. However, the observed attenuations are not drastic. The first goal of this section is to, evaluate the balancing impact on the low frequency resonances from an analytical prospective in a simplistic scenario that will lead to an improved architecture. The second

goal is to evaluate the cell balancing impact of the proposed architecture on the DPI injection levels. In order to understand the impact of the passive cell balancing on the injection levels, an ideal and simplistic scenario is analyzed to understand some mechanisms.

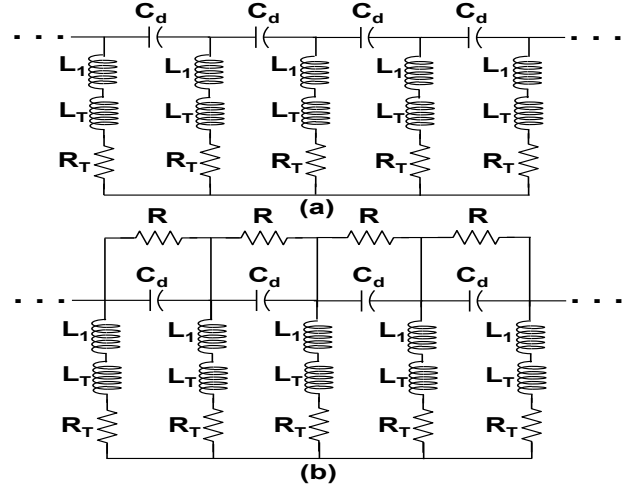


Fig. 7. Considered scenarios to analyze the impact of cell balancing on injection levels. (a) without balancing. (b) with balancing.

Let us consider Fig. 7a, it greatly resembles the case of architecture 1 (Fig. 2) with some simplifications. First, under 5 MHz, the ultracapacitors display a low impedance due to their high value (10 F) and their parasitics (ESR, ESL) are still low in these ranges. Thus they can be considered as a short. Secondly, since we are considering the low frequency resonances, C_L can be neglected as explained in the previous section. And thirdly, a simple ladder network is considered with no external loading to ease the approach. Fig. 7b shows a simplistic implementation of the passive cell balancing on the scenario of Fig. 7a. Indeed, R is placed in such manner to represent passive balancing and to ease the analytical approach. In addition, all the potential inductive parasitic elements between C_d and R are not considered to represent a case where C_d is very close to the BMS IC and to visualize a maximum impact of R on the resonances. In the case of Fig. 7a, the total impedance can be written as follows [2]:

$$Z_{eq}(K(s)) = \frac{\sum_{j=0}^{n-1} b_{n-1,j}(K(s))^j}{\sum_{j=0}^n c_{n,j}(K(s))^{j+1}} \quad (1)$$

Where $K(s)$ in the case of Fig. 7a is expressed as $K(s) = \frac{1}{sC_d(R_T + sL_T)}$, 'n' is the number of cells in the ladder network (considered here to be 18 for example) and $c_{n,j}$ and $b_{n,j}$ are a function of the binomial coefficients. Based on the approach in [2], extracting the resonances frequencies amounts to solving the following polynomial:

$$1 - C_d R_T v_{n,j} s - C_d (L_T + L_1) v_{n,j} s^2 \quad (2)$$

Where "j" is the resonances frequency index in [1, 18] and $v_{n,j} = 4 \sin\left(\frac{j}{2(n+1)}\pi\right)^2$. For the considered values of $R_T = 0.39 \Omega$, $L_T = 350 \text{ nH}$ and $L_1 = 1 \text{ nH}$, the discriminant of equation 2 is negative for all the values of "j". In other words, equation (2) has two imaginary roots where the real part reflects the attenuation of the resonances (pseudo-periodic regime). The real part can be written as follows:

$$|\lambda|_{No_Balancing} = \frac{R_T}{2(L_T + L_1)} \quad (3)$$

When taking the same approach on Fig. 7b, extracting the resonances amounts to solving the following polynomial:

$$(R - v_{n,j}R_T) - v_{n,j}(L_T + L_1 + RR_T C_d)s - v_{n,j}RC_d(L_T + L_1)s^2 \quad (4)$$

In this case, placing R as low as possible leads to the discriminant of equation (4) being positive for more number of resonance indexes. Thus, greatly damping those resonance frequencies. However, the pseudo-periodic regime remain the case for some resonances and their attenuation factor can be written as follows:

$$|\lambda|_{With_Balancing} = |\lambda|_{No_Balancing} + \frac{1}{RC_d} \quad (5)$$

From equation (5), cell balancing could potentially greatly impact the injection levels if R can be placed sufficiently low. One could also increase the value of R_T by adding an extra resistor. However, this is not possible for the case of architecture 1 (Fig.2) or 2 (Fig. 3) as it will drastically degrade the measurement accuracy on C_{Tx} pins when cell balancing is activated for that cell. With the previous remarks, the following architecture is proposed:

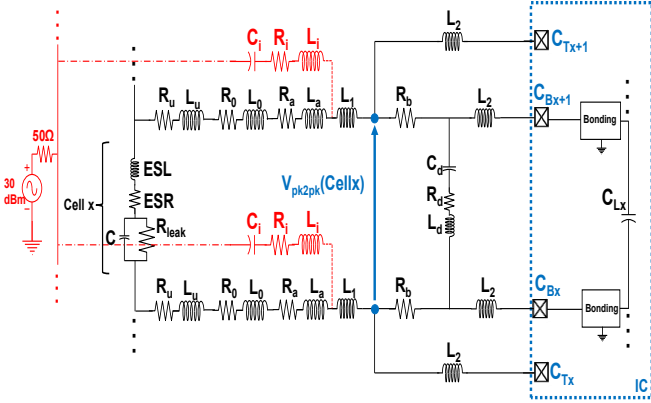


Fig. 8. Proposed BMS IC architecture for maximizing the cell balancing impact on injection levels.

Previously, in architecture 1 or 2, measurements through C_{Tx} pins are performed with a DTADC, thus, the need of an AAF (R_f , C_f) and measurements through C_{Bx} pins are performed with a CTADC. Now, in the proposed architecture (Fig. 8), measurements through C_{Tx} pins are done with a CTADC, thus, no need for R_f and C_f . And, measurements through C_{Bx} are done by a DTADC. In order to provide an AAF for the CBX pins the balancing resistor R_b is moved before the ESD Capacitor C_d . Therefore, not only the AAF previously present on C_{Tx} pins was removed but also greater attenuation of low frequency resonances will be obtained by the new placement of R_b . Moreover, to prevent any measurement error when cell balancing is activated, C_{Tx} measurements are performed before R_b . When it comes to the balancing impact on injection levels, the second balancing approach consists on balancing the same cell that is being measured by the ADC. In other words, the goal is to balance cell x (Fig. 8) in order to reduce the injection level on C_{Tx} pins. The proposed architecture also enables the balancing to have a maximum impact on the DPI injection levels by placing R_b before C_d and placing C_d as close as possible to the IC. The quantity of interest in this second balancing approach is $V_{pk2pk}(cellx)$. In fact, the proposed architecture is simulated in the same environment and conditions as architectures 1 and 2. Indeed, $V_{pk2pk}(cell1)$ is extracted for the proposed architecture in the same manner as $V_{pk2pk}(C_{L1})$ for architectures 1 and 2. In Fig. 9, the injection levels at low frequencies without cell balancing are independent of the

value of L_2 . It only comes into play when cell balancing is activated. As expected from the previous calculations, the proposed architecture inherently offers lower injection level without activating the cell balancing compared to architectures 1 and 2 (Fig. 5).

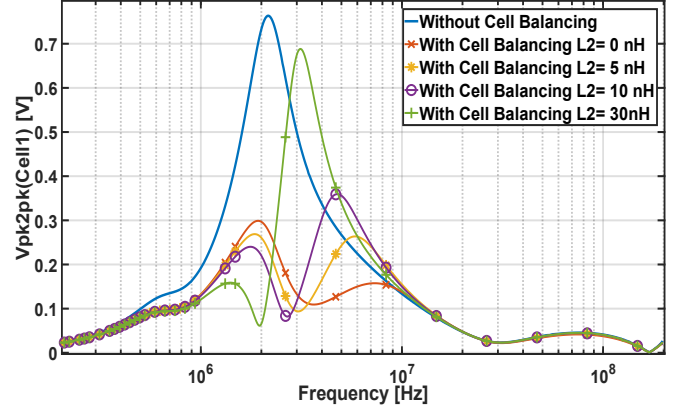


Fig. 9. The impact of the second balancing approach on injection levels during DPI with the proposed architecture and different values of L_2 .

From Fig. 9, it can be seen that important attenuation is obtained when capacitor C_d is placed at reasonable distances from the IC 0.5cm ($L_2= 5$ n) or 1cm ($L_2=10$ n). While the proposed architecture does lead to lower injection levels, saves 19 resistors and capacitors and enables the cell balancing to have an important impact on the injection levels, it raises some trade-offs with the ESD performance. Usually, when an ESD event happens at the connector of BMS IC PCB, C_d offers a low impedance path to the ground in the case of architectures 1 and 2. Thus, pins C_{Bx} and C_{Tx} are subjected to lower voltages. In the case of the proposed architecture (Fig. 8), placing one resistor R_b in that path will put C_{Tx} pins at risk of high voltages. In fact, depending on the value of R_b and incoming current, the voltage seen by C_{Tx} pins can vary. R_b should be chosen high enough for reasonable balancing currents and also low enough to minimize the voltage seen between C_{Tx} and C_{Tx+1} . Alternatively, placing an internal clamping device on the C_{Tx} loosen this trade-off. Other minimum cost approaches could lead to improve the ESD performance of the proposed architecture which will be one of the main focus point of upcoming works.

V. CONCLUSION

In this work, a model of the BMS IC is presented to be used for realistic DPI simulations. A first balancing approach to reduce the injection levels during DPI is proposed and two architectures are compared. Moreover, a simple analytical model of the cell balancing impact on the attenuation levels of low resonance frequencies is presented to identify a strategy to reduce the important noise coupling recorded in low frequencies. A new architecture is proposed to minimize outside components and injection levels which also enables the cell balancing to have a more important impact on the immunity of the IC. Finally, the proposed architecture raises some trade-offs that are related to the ESD performance. Future work will focus on evaluating the ESD performance of the proposed architecture and possible improvements without excessively increasing the number of outside components.

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