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ADIABATIC LOGIC GATES FOR ULTRA-LOW-POWER OPERATION USING CONTACTLESS CAPACITIVE MEMS

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ABSTRACT

We propose a concept of ultra-low-power logic gates based on flexural capacitive MEMS. Contactless operation avoids reliability issues faced by micro-electromechanical relays and allows for elimination of static losses. Furthermore, capacitive information encoding allows recovery of the invested charges, which makes adiabatic operation possible. This new paradigm is thus expected to be much more energy efficient than any CMOS logics that inherently presents static and dynamic losses. The design of an inverter (NOT) gate based on a complementary architecture of combdrives is detailed. They operate in the unconventional configuration where the initial overlap of the comb fingers is zero for the sake of a minimum usage of energy of the gate. Fabrication of proof-of-concept devices is presented using a silicon-on-insulator technology with 0.5 μm critical dimensions.

KEYWORDS

Adiabatic logic, ultra-low-power computing, combdrive actuators, variable capacitor.

INTRODUCTION

Electrical consumption of electronic circuits is increasing with the rise of digital services, which has a growing impact on global energy demand. On a smaller scale, power consumption impacts the battery time of many applications encompassing mobile devices, IoT, and autonomous sensors. The energy efficiency of information processing is thus a major challenge. These last decades have seen important efforts and tremendous progress in CMOS technology on which almost all digital processing circuits are based, such as CPUs. These circuits basically consist of logic gates that manipulate binary states, 0 and 1, to perform combinatory and sequential logic operations. The state-of-the-art CMOS logics achieve around 1000 $k_B T$ dissipation while performing an operation on one bit [1], which is three orders of magnitude above the Landauer limit $k_B T \ln 2$ [2]. Any further reduction of energy dissipation is restricted by the trade-off between dynamic and static losses and primarily by the finite transistor I-V subthreshold slope that is inherent to the CMOS technology itself. To overcome this limitation, a change in the paradigm is necessary. With this aim in mind, and leaving the transistors aside, previous works have exploited nano/micro-electromechanical relays [3-5]. These relays physically break the connection between the power source and the ground in the "OFF" state, thus preventing leakage currents and therefore static losses. However, their operation involves a physical contact leading to mechanical irreversibility and energy dissipation, and to poor

mechanical reliability. This latter point limits their use in digital circuits that require high amounts of switching, much higher than 10M cycles presented in literature [5].

Recently, we have shown that a logic state can be coded in the displacement of capacitive and contactless MEMS [6,7]. Combdrive actuators were used for the proof of concept. With this approach, leakage currents and losses due to mechanical irreversibility are eliminated while reliability is dramatically increased compared to micro/nano relays. Moreover, capacitive transduction allows implementation of the concepts of adiabatic logic [7] where the invested electromechanical energy is recovered through charge transfer with the reversible power supply. In such a configuration, slowing down the speed theoretically enables operation with near-zero dissipation. Indeed, residual dynamic losses due to mechanical dissipation in materials and in air and to non-infinite conductivity of the materials, scale down linearly with the operation frequency [7]. Calculations show that the energy required to process a bit of information is then orders of magnitude below the dissipation floor of the CMOS logics. Building on [6], we present here the implementation of an inverter (NOT) gate based on our approach called complementary adiabatic capacitive logic (CACL). The following sections describe architecture design, operation analysis, fabrication and actuation results of the gate.

ADIABATIC CAPACITIVE LOGIC

Figure 1 shows the system-level schematic of the elementary component of the complementary adiabatic capacitive logic (CACL) approach [1]. The working principle is relying on two variable electromechanical capacitors C_A and $C_{\bar{A}}$ sharing the same grounded electrode.

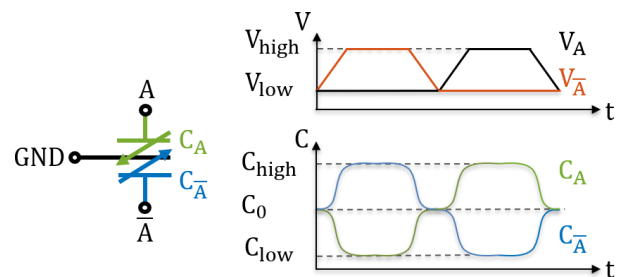


Figure 1. Schematic and characteristics of an elementary component based on two complementary variable capacitors (VC) C_A – between A and ground, and $C_{\bar{A}}$ between \bar{A} and ground.

Complementary voltages V_A and $V_{\bar{A}}$ are applied simultaneously to two independent gate terminals A and \bar{A} , respectively. If V_A is set to high and $V_{\bar{A}}$ to low, the capacitor

value C_A will increase whereas the one corresponding to $C_{\bar{A}}$ will decrease, as shown in Figure 1. The variation is the opposite if the voltage $V_{\bar{A}}$ is set to high and V_A to low.

The key challenge for implementing the elementary CACL devices is being able to define a robust, contactless hardware technology for realization of VC components. Viable candidates for VC implementation are combdrive actuators (Figure 2).

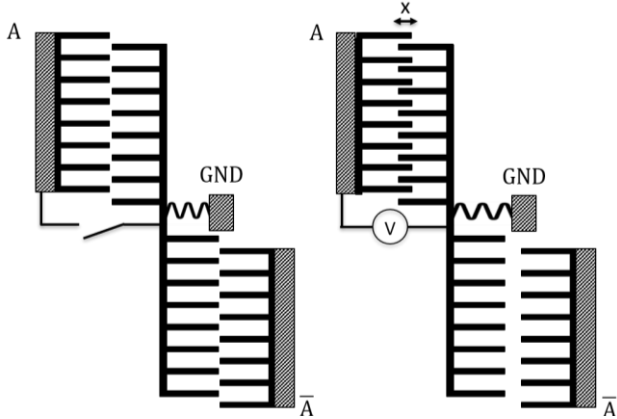


Figure 2. Combdrive actuators as variable capacitors in complementary configuration.

Combdrive structures have been massively employed in MEMS devices since the 1990's as actuators, sensors and resonators, and have proven their usability for applications like inertial sensors [9,10], micro-opto-electromechanical systems [11], or microgrippers [12] among many others. They are basically composed of two interdigitated sets of fingers, with one set being fixed while the other is connected to a flexible suspension. Combdrive capacitance depends on distance between the two sets of fingers. It is regulated by a balance between the electrostatic force, dependent on the applied voltage, and the mechanical restoring force of the flexible suspension, influenced by the stiffness of the springs. In our ACL approach, the logic state representation depends on the displacement of the moveable comb and the energy dissipation depends on the supplied voltage. So, it is crucial to identify suspensions that are as soft as possible, allowing large deflections at low actuation voltage.

Building on the elementary component from Figure 1, with VCs being implemented with combdrive structures, the inverter gate can be realized as shown in Figure 3. Note that input and output variable capacitors share the same moveable grounded electrode as a mechanical link.

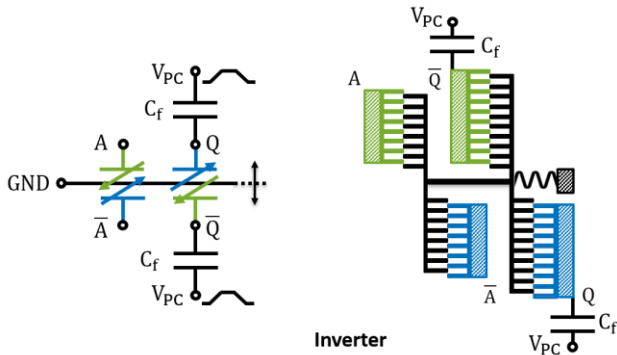


Figure 3. Simplified electromechanical model of an ACL inverter gate and the MEMS implementation.

The input signals A and \bar{A} determine the capacitor values C_A and $C_{\bar{A}}$. The established input capacitances further set the displacement of the movable grounded electrode and the values of the complementary output capacitors C_Q and $C_{\bar{Q}}$. C_f is a fixed capacitance forming a capacitive bridge. The power clock signal V_{PC} , a variable power supply capable of energy recovery, is applied over the bridge, yielding the complementary output electrical signals Q and \bar{Q} of the gate. The timing sequence is similar to the one of adiabatic logic where the power supply V_{PC} is a trapezoidal voltage divided in four phases [1].

As previously discussed in [6], the operating conditions that allow for the minimum usage of energy for the logic state encoding are the ones where the overlap between the fixed and moveable fingers of the combs is near zero in the resting state. Connection in a differential architecture of the comb-pairs in both input and output stages allows indeed for a larger range of motion between the two logic states. In such configuration with zero overlap, fringing fields have a substantial effect on the capacitance versus displacement characteristics of the combdrive actuators. As there is no reliable model of fringe effects that could we could apply, we first simulated these behavior characteristics by FEM using COMSOL Multiphysics before any system-level modeling.

DEVICE DYNAMICS

In this section, we present and analyze the simulations of CACL inverter logic gate using the MEMS components presented previously. These simulations allowed us to determine a set of parameters that makes operation with enough logical differentiation (distinguishing between two logic states) and cascability (the output voltages of a gate can be used to drive the following one) [6]. The physical and geometrical features of the proposed implementations are given in Table 1.

Table 1. Physical and geometric parameters used in simulations

Parameter	Description	Value	Unit
E	Young's modulus of silicon	$170 \cdot 10^9$	N/m ²
ϵ	Permittivity of air	$8.854 \cdot 10^{-12}$	F/m ³
h	Thickness of the capacitors	4.5	μm
h_{box}	Thickness of the BOX layer	2	μm
l	Length of the fingers	10	μm
d	Width of the fingers	0.5	μm
k	Spring constant in the direction \vec{x}	1.6	N/m
x_{re}	Overlap between the fingers	0	μm
N_A	Number of fingers in the input pairs	60	
N_Q	Number of fingers in the output pairs	480	
	Gate size	0.3	mm ²

This information was then processed with the goal of simulating the displacement of the moveable electrode within the inverter logic gate, calculating the generated output voltages and thereby demonstrating the inversion of the input logic states. We also looked at the energy consumed during these operations and showed that the inverter gate can generate output voltages suitable for driving subsequent gates. The dimensions presented above are carefully chosen in order to ensure the operation of the logic gate.

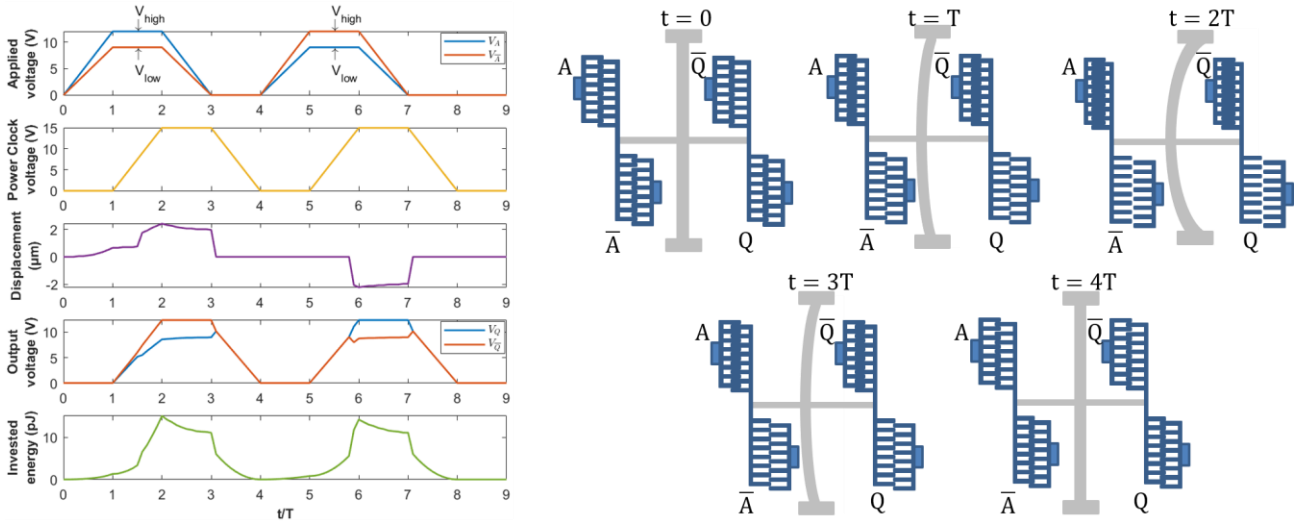


Figure 5. Left: Dynamic behavior of the inverter MEMS gate: Signals applied to the input comb-pairs; PC signal applied to the output comb-pairs (via capacitive bridge) with a time delay T ; Induced displacement of the moveable MEMS part; Generated signals on the output comb-pairs; Energy invested by the PC in the operation; Right: Corresponding displacement for the logic state 1 for the period $0 < t \leq 4T$.

Figure 5 shows the inverter behavior of the MEMS comb-drive gate and the propagation of the state 1 from the input to the output stage of the buffer logic gate. The information encoding and reading is done in 4 phases governed by the power clock which allows recovery of the electrical charges.

In the **phase 1** ($0 < t < T$) the input voltages cause the disbalance between the forces acting on the electrodes within comb-pairs A and \bar{A} . This disbalance puts the moveable combs into motion towards the electrode experiencing greater force (here A), further inducing the initial disbalance, within the output comb-pairs, corresponding to *pre-actuation*. In the **phase 2** ($T < t < 2T$) power clock signal V_{PC} is progressively applied to the output stage via capacitive bridge formed with the fixed capacitances C_f , establishing the output voltages (V_Q , $V_{\bar{Q}}$). If the design parameters are carefully chosen, this additional voltage amplifies the initial movement established by the inputs. In the **phase 3** ($2T < t < 3T$) signals A and \bar{A} are lowered to the ground. As $N_A \ll N_Q$ the logic state is kept coded in the position through the force generated by the output comb-pair and the power clock. During this phase the established voltages V_Q and $V_{\bar{Q}}$ serve as the input voltages to evaluate the next logic gate of the circuit. In the **phase 4** ($3T < t < 4T$) V_{PC} signal is reduced to 0, returning the moveable parts to their initial position.

Trapezoidal waveform of the signals (inputs and PC) eliminates any abrupt transitions, allowing for optimal charge of the capacitors and energy recovery by the power clock, therefore enabling very low dissipation and even adiabatic operation. The energy invested into logic state encoding E_{in} corresponds to the sum of electrical energies stored in the four VCs and the mechanical energy stored in the spring:

$$E_{in} = \frac{C_A V_A^2}{2} + \frac{C_{\bar{A}} V_{\bar{A}}^2}{2} + \frac{C_Q V_Q^2}{2} + \frac{C_{\bar{Q}} V_{\bar{Q}}^2}{2} + \frac{kx^2}{2} \quad (1)$$

With k being the spring constant and x the displacement of the moveable combs. During the phase when V_{PC} is

lowered to 0 ($3T < t < 4T$ and $7T < t < 8T$) the invested energy is recovered by the power supply.

FABRICATION & CHARACTERIZATION

MEMS gates are fabricated on (100) SOI wafers with device thickness of $4.5 \mu\text{m}$ and BOX thickness of $2 \mu\text{m}$. Top silicon layer and the handle are highly doped with low resistivity ($0.001\text{-}0.005 \Omega\text{cm}$). Fabrication steps included photolithography (Canon Stepper I Line), DRIE (Alcatel AMS4200) and wet etching (BOE). The realized comb-finger width is $0.4 \mu\text{m}$, the gap between them is $0.6 \mu\text{m}$. The whole logic gate has a surface of about 0.3mm^2 .

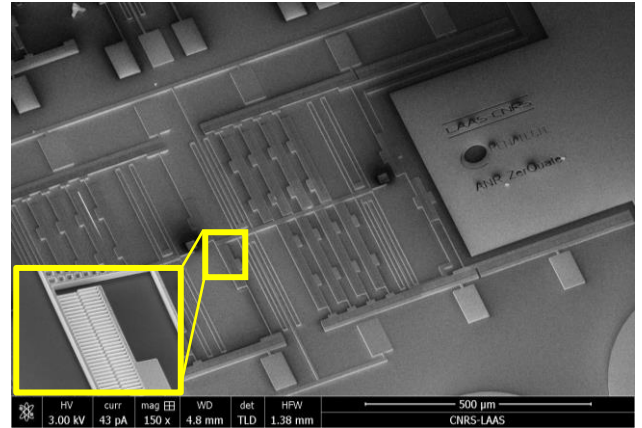


Figure 7. SEM image of the inverter logic gate.

Devices were successfully activated on a probe station causing movement governed by the activation voltages (Figure 8). The voltage signal was applied on terminal A , while the \bar{A} and the moveable electrodes were grounded, to encode logic state 1. In order to encode logic state 0, the voltage signal was applied on terminal \bar{A} , keeping A and the moveable electrodes grounded.

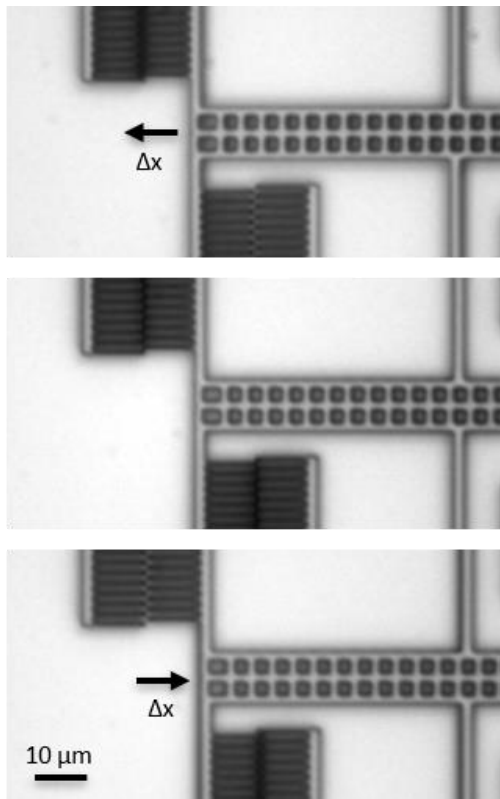


Figure 8. Coding of the logic states in the physical position of the moveable comb – logic state 1 (top), resting position (middle) and logic state 0 (bottom).

Application of the DC voltage on terminal A resulted in an electrostatic force acting on the moveable electrodes and causing them to shift to the left (Figure 8 - top). By our chosen convention this corresponds to logic state 1. Analogous to that, the application of the signal to terminal \bar{A} resulted in the movement to the right (Figure 8 - bottom), encoding logic state 0. Keeping all the terminals at the ground potential corresponds to the resting state (Figure 8 - middle). These experiments confirmed the FEM simulation and expectations given in [6]. Even though the initial state of the combdrives is with zero overlap between the electrode fingers, fringe effect allows for a displacement. Application of 15V to the terminals resulted in a displacement of 2 μm .

CONCLUSION

We have implemented a new paradigm of logic gates by using a flexural structure and variable MEMS capacitors in a complementary configuration. Combdrive actuators were identified as robust candidates for the purpose of proof-of-concept devices. They were operated in a regime of a zero-initial overlap between the comb fingers for the sake of a minimum usage of energy during operation of the gate. We performed FEM analysis in order to obtain a fine knowledge of the capacitance versus displacement of the combdrives which is a key point for the accuracy of the further system-level modeling and design. We derived optimal geometrical parameters for an elementary variable capacitor. Building on this elementary component, we have developed an inverter logic gate and have simulated the inversion of the input logic states. The amount of energy invested during operation of the gate is 13 pJ maximum and

it can be fully recovered by a reversible power supply. Furthermore, we have shown that the inverter gate can generate output voltages suitable for driving subsequent gates. And finally, we have fabricated the inverter gate and demonstrated the encoding of the logic states in the position of the moveable electrodes.

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