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Abstract

A 4×4 Butler matrix for millimeter-wave communications is presented in this paper. The circuit takes advantage of a new 3-D Integrated Passive Devices (IPD) process to achieve a performance/compactness trade-off substantially higher than conventional IPD designs. A footprint of 0.84 mm^2 is reached by using 3-D transformers and solenoids for designing couplers and phase shifters. Couplers are optimized to maximize the bandwidth of the Butler matrix. Phase variations with frequency are also tuned between phase shifters and crossover for the same purpose. The resulting experimental bandwidth, defined by reflection coefficients at −10 dB, is from 20 GHz to 30.1 GHz, and from 22.1 to 27.5 GHz considering a maximum phase error of 10° for the four states −45°, 135°, −135° and 45°, while insertion losses are measured close to 1.3 dB. Matchings and isolations remain below −17 dB and −12 dB, respectively.

Keywords: Integrated Passive Devices (IPD), 3-D technology, Solenoid, Transformer, Metal-Insulator-Metal (MIM) capacitor, Millimeter waves, 5G, Quadrature hybrid Coupler, Phase Shifter, Crossover, Butler matrix. keyword one, keyword two

1. Introduction

Using large bandwidths in the millimeter-wave spectrum may significantly increase data rates of the next generation of wireless communication applications. However, short wavelengths bring about new challenges to radio architectures that have to overcome high propagation losses and fast fading effects. One of these challenges is the integration of high gain antennas with adaptive spatial filtering to mitigate high path losses and to provide cost-effective and reliable coverage. Among strategies available for beamforming, the most versatile is the phased array system [1]. While this approach is well-suited to base stations, it is hardly compliant with mobile handsets which face additional constraints in terms of cost, energy efficiency and size limitations [2]. For the latter handset, the implementation of phase-switched networks using passive circuits, such as Rothman lenses and Blass or Butler matrices, is more relevant [3, 4]. Compared to phased-array systems, such a solution dissipates much less DC power but features less discrete beam directions.

Among these passive networks, the Butler matrix has been extensively researched owing to its low complexity. A $n \times n$ Butler matrix produces n phase-shifted replicas with equal magnitude of a single signal applied to one of its n inputs. The phase relationship between outputs is set from the selected input. Connecting outputs to an antenna array makes it easy to create a switched multi-beam system. In the targeted frequency range of 24 to 29 GHz, the literature reports very different ideas and technologies. The most compact circuits are based on CMOS back end of line (BEOL)[5, 6]. However, this technology is not really suitable because of the complexity and cost of manufacturing, and the average performances achieved. On the other hand, low-cost and low-complexity printed circuit board (PCB) technologies support the implementation of very different design techniques such as microstrip lines [7, 8, 9], substrate integrated waveguides (SIW) [10, 11, 12, 13] or suspended lines (SISL) [14]. The resulting dimensions are quite large, but SIW butler matrices offer by far the best performance today. Finally, integrated passive device technologies (IPD) provide intermediate dimensions, low manufacturing costs and complexity [15, 16]. Conventional IPD technologies are suitable for the integration of semi-distributed planar devices, as in [15, 16], using MIM capacitors and spiral inductors with improved Q-factors compared to CMOS technology [17, 18]. In order to increase integration densities of IPD circuits without compromising losses and overcoming the previous apparent trade-off, the use of the third dimension is proposed in this paper. Based on a dedicated and innovative 3-D technology process, a family of compact, high-performance devices derived from solenoids is designed and used for the integration of a 4×4 Butler matrix.

The paper is organized as follows. Section 2 discusses the design of each component of the Butler Matrix. The technological process for the fabrication of 3-D circuits is described in Section 3. Section 4 deals with Butler matrix measurements and a comparison is made with simulated data. Finally, these results are assessed in relation to other works published at similar frequencies in Section 5.

2. Butler Matrix Design

The 4×4 Butler matrix presented consists of four quadrature hybrid couplers, one crossover and two phase shifters (Fig-

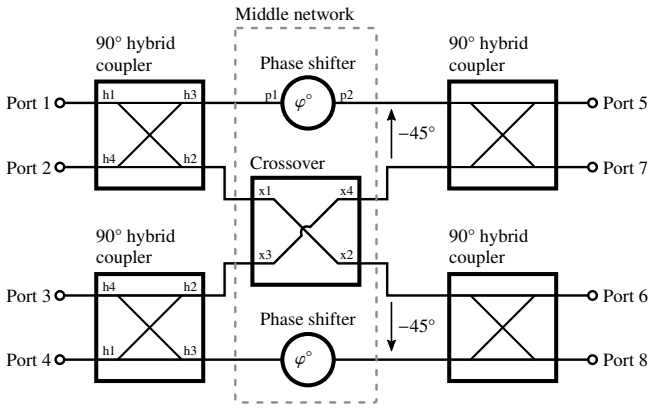

Figure 1: Block diagram of the proposed 4×4 Butler matrix.

ure 1). The main contribution of this work lies in the design of each of the components constituting the Butler matrix. The hybrid coupler and the phase shifter generalize the use of solenoids to take full advantage of the technological process employed, to maximize the compactness and minimize the losses while the crossover is simply the intersection of two lines.

As seen in Figure 1, the phase shift value φ introduced by each phase shifter is adjusted in order to obtain a phase difference of -45° between transmissions of the phase shifter and the crossover. In this configuration, the phase difference observed between the adjacent outputs 5 to 8 of the Butler Matrix is −45°, 135°, −135° and 45° when excitation is applied from port 1 to 4, respectively. The signal applied to one of the inputs 1 to 4 is distributed equally between the four outputs 5 to 8, and a transmission coefficient theoretically equal to −6 dB is then expected whatever the excited input.

The following sections present the design of the hybrid quadrature coupler, the crossover and the phase shifter. The latter two components make up the middle network (Figure 1). These are optimized simultaneously, as it is essential to keep the phase shift observed constant between their respective transmissions over a widest frequency range.

2.1. Quadrature Hybrid Coupler

Branch-line, Lange and basic coupled-line couplers are used extensively in microwave and millimeter-wave circuits to create 90° phase shifts. All these circuits occupy large chip area due to the long transmission line sections required for their implementation, but this problem can be mitigated by adopting a semi-distributed or lumped element design approach. The basic coupled-line coupler topology is of particular interest here because the coupled lines can be replaced by an ultra-compact 3-D transformer made by combining two solenoids. It is formed by winding two turns of two parallel strips around an insulating core of SU8 resin, as illustrated in Figure 2a.

The design of a 50 Ω-matched quadrature hybrid coupler from a transformer requires to match the even and odd mode ABCD matrices of its lumped equivalent model (see black parts of Figure 2b) with those of an ideal coupled-line hybrid coupler. Each element of the model is then expressed according to the characteristics of the coupled-line coupler: $Z_{0o} = 20.7\,\Omega$, $Z_{0e} = 120.7\,\Omega$, $\theta = 90°$, $k = 0.707$ [19], Z_{0o}, Z_{0e}, θ and k being the odd and even mode characteristic impedances, the electrical length and the coupling factor, respectively. To achieve a quadrature hybrid coupler operating at 27 GHz, the following values are calculated [20]: $L = 417$ pH, $k = 0.71$, $C_g = 49$ fF and $C_c = 118$ fF. These values define a starting point for the circuit design. The inductance value L is determined by adjusting the number of turns and the aspect ratio of the vertical section of the 3-D transformer's dielectric core. As its aspect ratio must remain close the square shape to minimize the proximity induced losses in the conductors, the best compromise leads to an inductance of 460 pH. The coupling factor k is technology limited as it depends on the spacing between turns. By reducing it to the minimum possible, a value close to 0.6 is obtained. Finally, two external capacitors C_m and C_c (in gray in Figure 2b) are added to provide an extra degree of freedom and bring the equivalent characteristic impedances Z_{0o} and Z_{0e} and the coupling factor k of the circuit in Figure 2 close to the target values. C_m compensates the excess impedance brought by the inductance L while C_c increases the coupling factor. The performance tuning is performed using an electrical simulator (Keysight ADS) based on the 3-D electromagnetic model of the transformer (ANSYS HFSS).

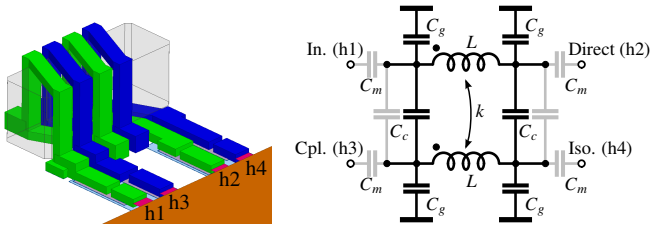

Figure 2: (a) 3-D model of the 90° hybrid coupler and (b) equivalent network highlighting fabricated transformer in black and added MIM capacitors in gray.

In practice, solenoids are integrated around a 110 µm-thick SU8 resist core and the area of the coupler is 340 µm×280 µm (0.095 mm^2). The concept and design of this coupler was first described in [21]. However, in this version, capacitors C_c and C_m have been rearranged and placed under the lower metallization of the solenoids to improve compactness. Values of capacitors C_c and C_m are set to 55 fF and 325 fF for a performance alignment on the targeted center frequency of 27 GHz. To minimize imbalances and achieve a good electrical symmetry, ports are designed such the ports $h1$ and $h3$ (ports $h2$ and $h4$ respectively) are kept in close proximity.

Results of the coupler's S-parameter simulation along with magnitude imbalance and phase difference between transmissions are shown in Figure 3. At 27 GHz, insertion losses extracted from S_{h21} or S_{h31} (Figure 3a) come to approximately 0.3 dB. Reflection S_{h11} and isolation S_{h41} coefficients remain below −17 dB over the 24 GHz to 29 GHz range. From Figure 3b, it can be noticed that the phase difference between outputs $h2$ and $h3$ is 90° and the magnitude imbalance is −0.22 dB

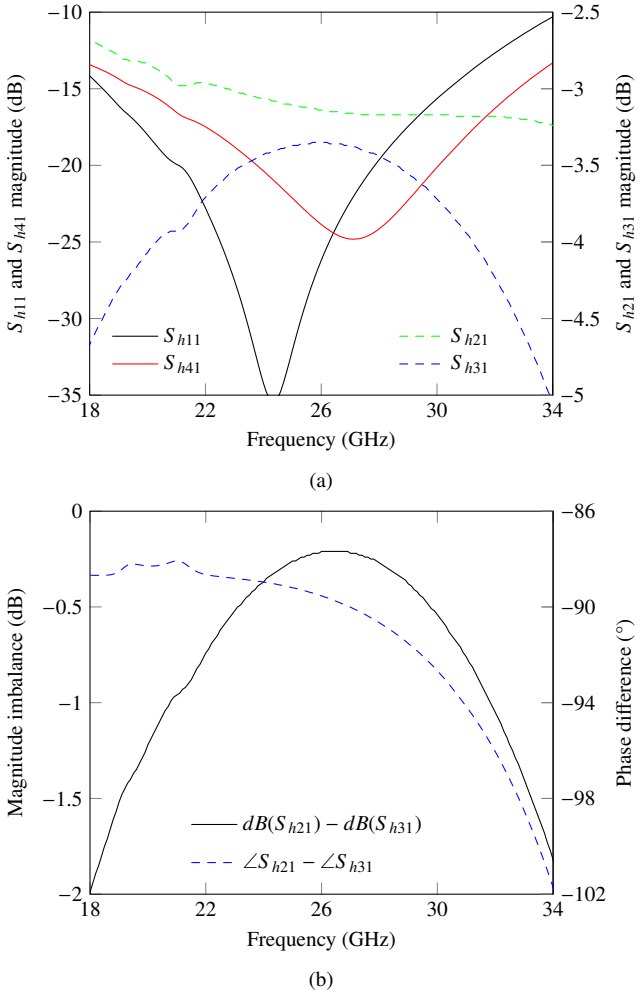

Figure 3: 90° hybrid coupler simulated characteristics, (a) S-parameters and (b) amplitude imbalances and phase difference.

at 27 GHz. Within the 24 GHz to 29 GHz frequency band, coupling imbalances are maintained below 0.4 dB and ±1.5° around 90°.

2.2. Crossover

The crossover enables a signal transmission from port $x1$ to port $x2$ (resp. $x3$ to $x4$) while the other two ports remain isolated (Figure 1). This function is carried out via a bridge that allows the crossing of two transmission lines, when the required number of metal layers is technologically available [5, 15, 16]. Otherwise, it can be obtained by cascading two 90° hybrid couplers [10, 11, 12]. Here, the first solution is preferred owing to better compactness and a broader frequency bandwidth.

The top view and the 3-D model of the designed crossover are presented in Figure 4. Despite the lack of geometric symmetry, the two paths are drawn to exhibit the same electrical length. In addition to the bridge, two long parallel strips are drawn to connect the input couplers to the output couplers. Such a design is prone to radiation losses, but not desirable. A third strip integrated on top of 110 µm-thick SU8 pillars and connected to ground mitigates these effects as much as possible. The whole creates a slightly frequency dispersive high-impedance grounded coplanar strips waveguide (CPS). Four identical capacitors, named C_x, are added in series with the ends of the lines to improve the impedance matching of the crossover with the couplers it connects to.

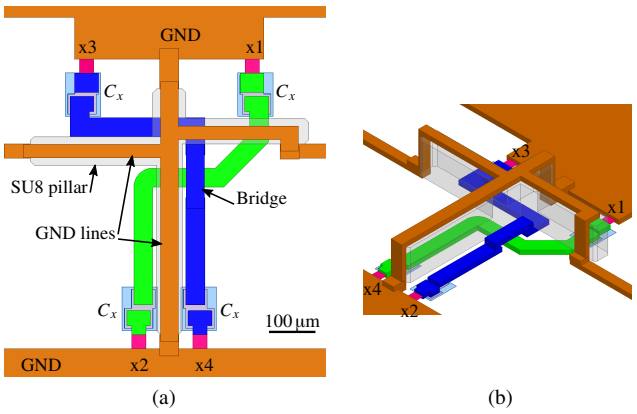

Figure 4: (a) Top view and (b) 3-D model of the crossover. Signal lines are drawn in green and blue. Orange parts are connected to ground.

The first design steps are performed using multi-level microstrip line models usually available in RF CAD software to define the main line dimensions (length, width and spacing). Circuit dimensions are then refined by using electromagnetic simulation. The final simulated characteristics are shown in Figure 5. The insertion losses are comprised between 0.6 dB and 0.9 dB in the 24 GHz to 29 GHz range, and the S_{x31} and S_{x41} isolations are under 10 dB and 26 dB, respectively. The electrical symmetry of the crossover is estimated by measuring the imbalances between S_{x21} and S_{x43} parameters, on magnitudes and phases (Figure 6). Values less than 0.05 dB and 0.2°, respectively, are reported in the same frequency band.

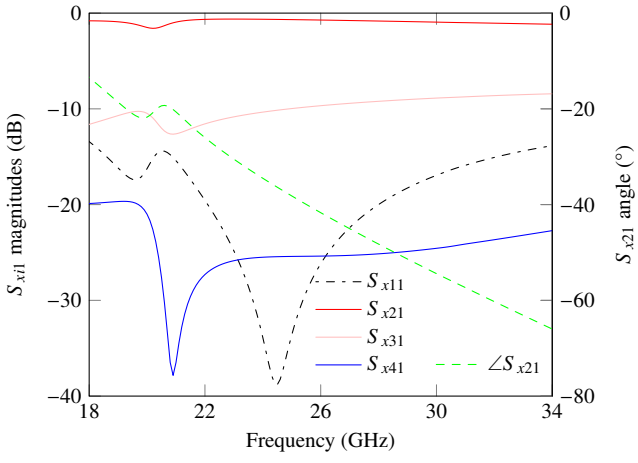

Figure 5: Crossover simulated S-parameters from port 1 and with C_x = 300 fF.

2.3. Phase Shifter

The phase shifter presented in Fig. 7 consists of a 3-D coil wrapped around the 110 µm-thick SU8 core in association with

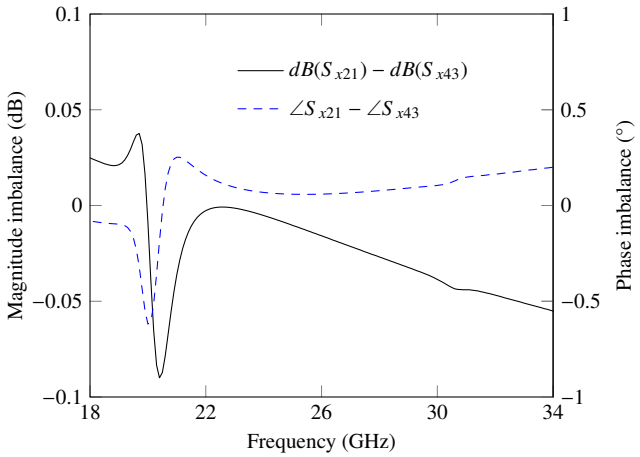

Figure 6: Simulated magnitude (——) and phase (---) imbalances between crossover paths, with C_x = 300 fF.

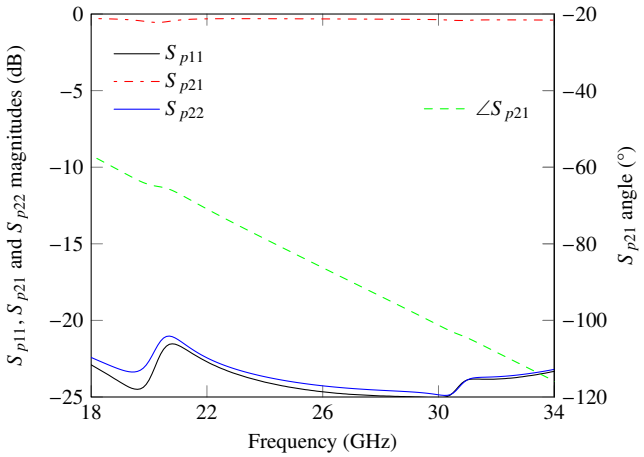

Figure 8: Simulated characteristics of the phase shifter with C_p = 1.6 pF.

input/output series capacitors C_p. This circuit acts as a section of transmission line whose phase slope and attenuation are matched to those of the crossover. The 3D coil consists of two turns of 50 µm-wide strips. The inductance/capacitance ratio of this structure is initially too high due to the strong inter-turn mutual positive coupling and the low capacitance to ground. This problem is solved by interposing a 30 µm-wide grounded line with 15 µm line spacing. The C_p capacitor is used to fine-tune the phase difference observed with the crossover. It also adjusts the transmission's phase slope in the lower frequency range. As for the crossover, the first design steps rely on electrical simulations using models of coupled microstrip lines. Electromagnetic simulations are then used to determine the final dimensions. The footprint of the circuit shown in Fig. 7 is 635 µm×330 µm (0.21 mm^2).

Simulated data of the device (Figure 8) exhibit a broadband behavior. Return losses remain less than −24 dB and insertion losses are better than 0.35 dB in the frequency range 24 GHz to 29 GHz.

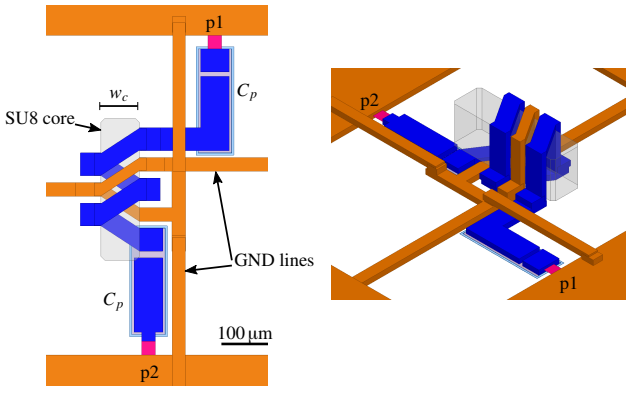

Figure 7: (a) Top view and (b) 3-D model of the phase shifter. The signal strip is in blue and orange parts are connected to ground.

2.4. *Bandwidth Optimization of the Middle Network*

Several conditions must be met to achieve broadband operation of the middle network. First, a phase difference of −45° between phase shifter and crossover transmissions must be reached at the center frequency. Second, this difference must be kept for the largest possible frequency band, while both magnitudes are kept as close as possible to each other. As the crossover introduces a phase shift of −45° at the center frequency of 27 GHz, φ has to be adjusted to −90° to reach the phase difference of −45° between phase shifter and crossover transmission parameters, as highlighted in Figure 1. φ depends on the width w_c of the SU8 core of phase shifter (Figure 7a). Therefore, phase adjustment is very easily carried out by choosing the optimal width w_c at 27 GHz. Here, the result is a w_c set to 84 µm.

Once w_c is set, capacitors C_x and C_p are tuned to keep this phase difference close to −45° at 27 GHz but also within the whole frequency range, by matching the slopes of phase variations versus frequency between transmissions of both the phase sifter and the crossover. This optimization has almost no effect on transmission magnitudes as long as components remain impedance-matched. The transmission angles of the crossover (S_{x21}) and phase shifter (S_{p21}) are shown in Figure 9 for several C_x and C_p values and for w_c set to 84 µm. The best trade-off with respect to the aforementioned requirements is obtained for capacitors C_x and C_p of 300 fF and 1.6 pF, respectively.

The resulting magnitude and phase differences observed between the transmission parameters of the phase shifter and the crossover are given in Figure 10. From 24 GHz to 29 GHz, the magnitude difference is kept within the range 0.3 dB to 0.5 dB while phase difference varies from −44.1° to −46°.

3. 3-D IPD Fabrication Process

3-D IPD processes have emerged with the potential to enhance performance and integration densities when compared to conventional planar IPD technologies [22, 23, 24, 25, 26]. The key innovation lies in leveraging the third dimension to design 3-D structures, including 3-D solenoid inductors rather

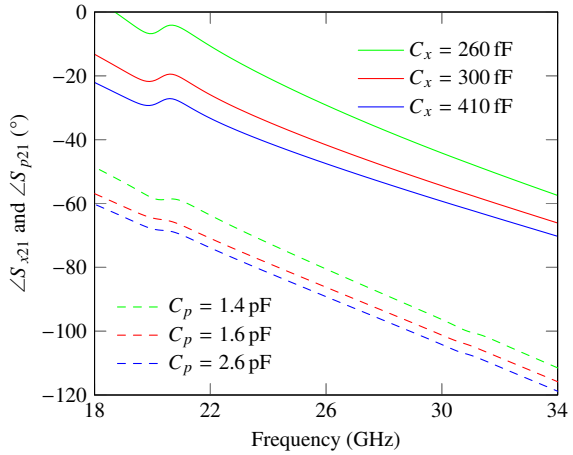

Figure 9: Crossover S_{x21} angle versus C_x (——) and phase shifter S_{p21} angle versus C_p (---) for phase difference and phase slope adjustments over frequency of the middle network. w_c is set to 84 µm.

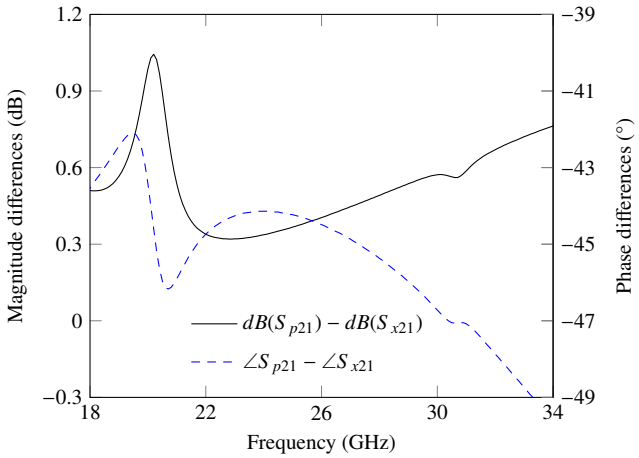

Figure 10: Simulated magnitude (——) and phase differences (---) observed between S_{p21} (phase shifter) and S_{x21} (crossover) transmissions of the middle network.

than planar spiral inductors, resulting in improved Q-factors. These processes typically involve metalizing both sides of a silicon or glass substrate ranging from 50 to 250 µm in thickness. Unlike silicon [22, 25], glass offers the advantage of producing solenoids with notably high Q-factors. Inductance densities have, however, remained in the range of 3 to 17 nH/mm^2, comparable to those achieved by conventional planar IPD technologies using spiral inductors. This is due to the manufacturing of Through Glass Via (TGV), which require large diameters and pitches, limiting device scalability and adaptability to increasing operational frequencies. These technologies are also complex to implement and involve numerous technological steps.

The proposed 3-D IPD technology aims to address these limitations in achieving significantly higher inductance densities, up to 60 nH/mm^2 [18], along with high Q-factors and resonant frequencies. This makes it a strong candidate to accommodate millimeter-wave frequencies, distinguishing it from other 3-D IPD technologies. The technology detailed in [18] for the integration of the solenoids is supplemented by additional steps

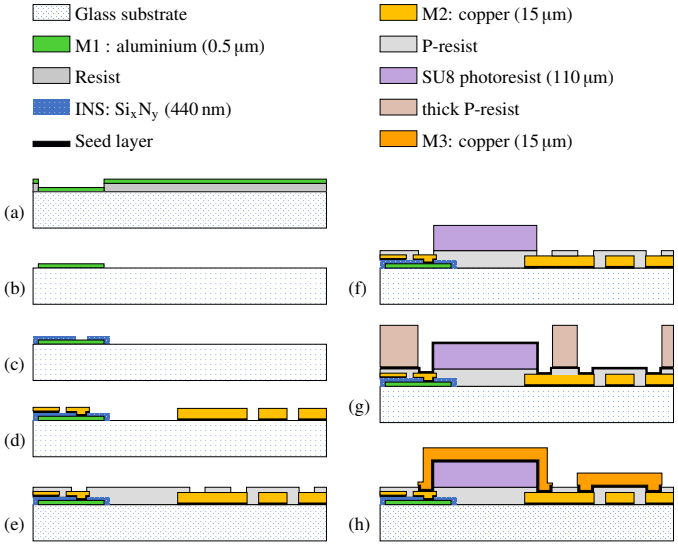

Figure 11: Sectional view of the main steps for the integration of a capacitor, a solenoid and a bridge (from left to right) using the 3-D IPD process.

for the implementation of MIM capacitors. The overall process flow is depicted in Figure 11.

MIM capacitors are manufactured first. The bottom electrode, referred to as M1 in Figure 11, is obtained from the evaporation of a 0.5 µm-thick aluminum layer on a resist mold (Figure 11a). This resist is removed using a lift-off process (Figure 11b). The insulating layer INS is made up of a 440 nm thin layer of silicon nitride Si_xN_y, deposited by an Inductively Coupled Plasma Chemical Vapor Deposition (ICPCVD) process at a temperature under 100 °C (Figure 11c). The top electrode is formed along with the first level of the solenoid in a single copper electroplating step named M2 (Figure 11d). The copper thickness is set to 15 µm. A photoresist (P-resist) is added to protect M2 layer against oxidation and etching that can occur during the following steps and vias are opened for further electrical connections to M2 (Figure 11e).

All steps required for the manufacture of 3-D metallization are described below. A 110 µm-thick SU8 photoresist layer is deposited and patterned to form the cores of solenoids and the stands for strips required within the upper metal (Figure 11f). A thick P-resist layer is applied and openings are made to create the mold for the upper metallization M3 growth (Figure 11g). Both vertical and upper sections of the M3 layer are electroplated simultaneously using a single 3-D seed layer, and a copper thickness of 15 µm is processed for this M3 level (Figure 11h). The latter step can also be used for the manufacture of metal bridges if required for line crossovers or coplanar waveguides (CPW). In this case, the P-resist layer located under the metal strip is not removed.

The whole manufacturing process requires six masks, which is comparable to conventional IPD technology. The maximum temperature of 100 °C reached during fabrication makes this process compliant with a large variety of substrate materials, both mineral and polymer-based. For the application considered here, the process is developed on a glass substrate.

4. Butler Matrix Simulation and Measurement

The fabricated Butler Matrix is shown in Figure 12. The four hybrid couplers, the two phase shifters on each branch, the grounded upper structure, all CPW and pads of matrix ports can be seen on this picture. Thanks to the grounded lines in and around the components of the Butler matrix, a very low degradation of their individual performance can be observed when close to each other. Thus, a very compact Butler matrix is obtained. Except for measurement pads and CPW accesses, the circuit footprint is 700 µm × 1200 µm (0.84 mm^2) for a height of 145 µm.

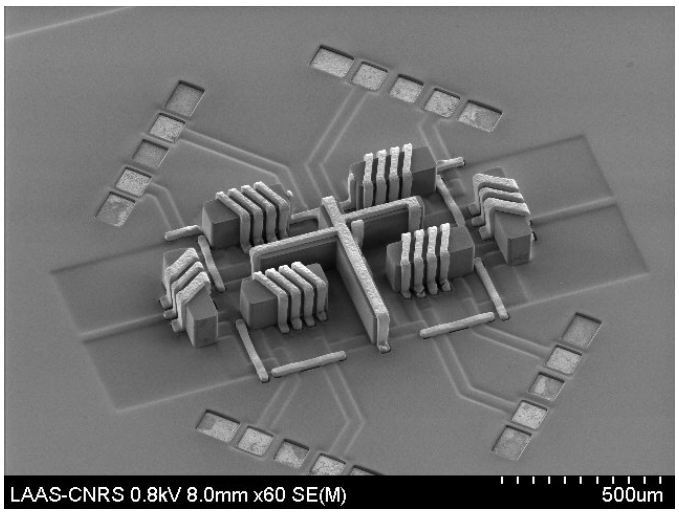

Figure 12: Scanning Electron Microscopy (SEM) picture of the fabricated 4×4 Butler matrix.

The characterization of the 4×4 Butler matrix ideally requires an 8-port Vector Network Analyser (VNA). To circumvent this need, which is quite difficult to achieve given the number of ports and the high frequencies involved, a 4-port VNA is used in conjunction with matched loads placed on unused ports. This approach requires six partial measurements which are processed to recover the 8×8 scattering matrix of the Butler matrix. Two additional CPW transmission lines of different lengths, with the same geometry as the CPW access lines, are also used to calculate and de-embed the contribution of the access pads and CPWs. The method used for this operation is described in [27]. The on-wafer characterization has been performed on a PM-8 Suss Microtec probe station and a Keysight N5247A PNA-X 4-port VNA. Four Cascade Infinity RF probes are used, as well, with a GSGSG configuration (G for Ground and S for Signal) and a pitch of 150 µm.

The deembedded experimental S-parameter magnitudes of the Butler matrix when the input signal is applied to port 1 are shown in Figure 13, and compared with simulated ones. Input reflection magnitudes (S_{11}, S_{22}) and magnitudes of isolations with other inputs (S_{21}, S_{31} and S_{41}) are plotted in Figure 13a while transmission magnitudes toward ports 5 to 8 (S_{51}, S_{61}, S_{71} and S_{81}) are given in Figure 13b. Phase differences between outputs are reported in Figure 14. Simulations and measurements are in fairly good agreement knowing that two sources of uncertainty affect the experimental data: mismatch-induced errors due to impedances connected to unused DUT ports that changes from one partial measurement to another [27, 28], and the access de-embedding process. In Figure 13a, the −10 dB bandwidth, extracted from S_{11} and S_{22} parameters, is from 20 GHz to 30.1 GHz. Within this range, isolations are less than −17 dB after 22.4 GHz except for S_{41} which is limited by S_{x31} crossover isolation. Alleviating the crossover's compactness constraints should easily improve this. With respect to transmissions (Figure 13b), average losses resulting from the Butler matrix are less than 2 dB between 21 GHz and 30.3 GHz. The observed inter-channel dispersion is primarily caused by over-coupling in the input couplers of the Butler matrix, implemented from initial version [21] while the output couplers benefit from the improvements discussed in section 2.1. For the phases plotted in Figure 14, a good agreement is also obtained between simulations and measurements. Phase errors are minimal (7°) around 25 GHz and remain below 8° between 23.3 GHz and 26.5 GHz and below 10° from 22.1 GHz to 27.5 GHz. At the highest frequencies, the discrepancies observed between simulation and measurements could be the result of the aforementioned measurement errors but also of the post-layout electromagnetic model of the circuit which considers rectangular sections for the metallization whereas these are more complex in practice.

5. Comparison and Discussion

The measured performances of the butler matrix are summarized in Table 1 and compared to similar works reported in the literature operating in the same frequency bands. The discussion focuses on the electrical performances obtained with respect to the dimensions obtained using different technologies. To be able to compare this work with other reported Butler matrices, the available data have been re-processed on the basis of common criteria. For example, to highlight the phase shift optimization work done between the components of the proposed butler matrix, we have chosen to define a bandwidth based on a maximum phase error arbitrarily fixed at 10°.Worst-case data are also extracted within this band for the isolation (Iso.), the return-loss (RL) and the average insertion losses (aIL), when available. The averaged insertion losses enable an assessment of the inherent loss associated with each technology without being disturbed by inter-channel dispersion of transmissions.

The best insertion losses, around 0.5 dB, are obtained from SIW technologies that benefit from the absence of radiative losses, copper metallization and very low loss angle substrates [10, 12]. Unsurprisingly, these matrices present the largest dimensions of this comparison. IPD and particularly CMOS technologies offer a much better compactness but this advantage comes at a performance cost, with insertion losses around 2 dB for CMOS [5] and 3 dB for IPD [15]. In [15], the authors favored compactness by using very narrow (3 µm-width strips) high-impedance transmission lines at the expense of insertion losses. However, IPD technologies usually improve Q-factors compared to their CMOS silicon-based counterparts thanks to their much thicker and better conducing materials

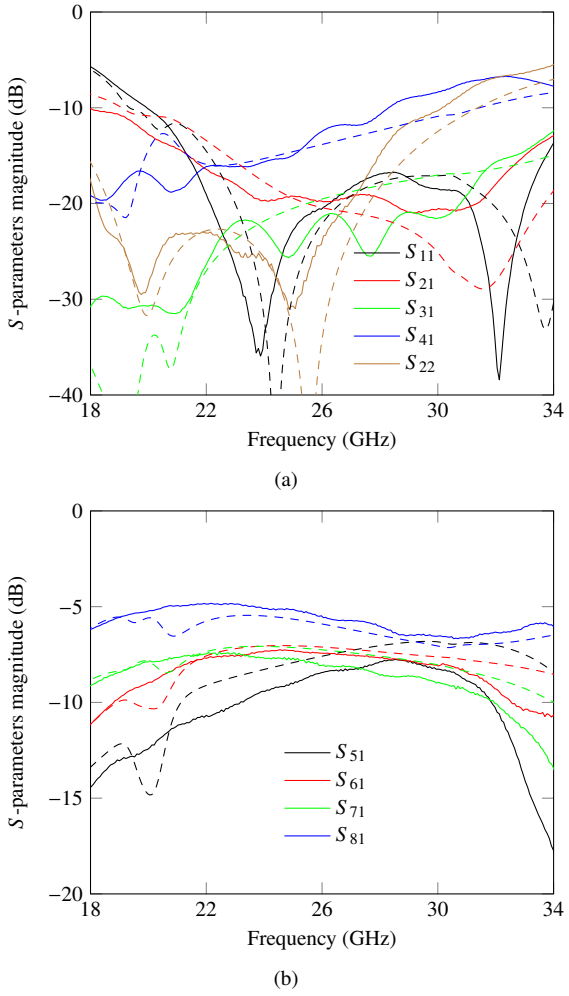

Figure 13: Simulated (---) and measured (——) S-parameters magnitudes of the Butler matrix with excitation at port 1. (a) return loss and isolations and (b) transmissions from input 1 toward outputs 5 to 8.

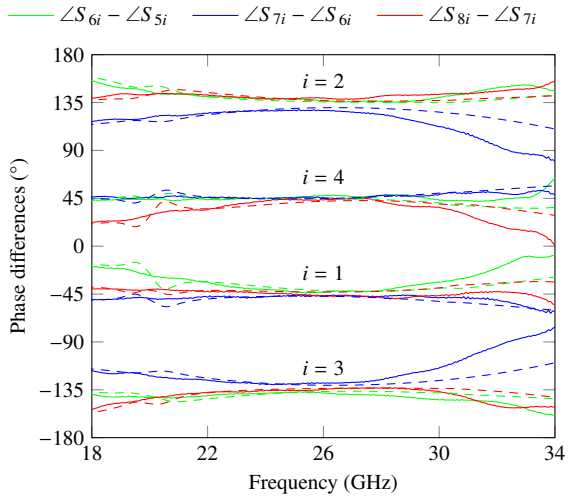

Figure 14: Simulated (---) and measured (——) phase differences between adjacent outputs for excitation successively applied to port i, with i from 1 to 4.

used for metal layers (Cu vs. Al) placed on insulating substrates (i.e. glass) [18, 29]. But these characteristics make the circuits manufactured in IPD technologies more bulky than their CMOS counterparts.

Table 1: Performance comparison between Butler Matrices in K and KA bands.

Reference	[5]	[15]	[16]	[10]	[12]	[14]	This work
Technology	CMOS	IPD	IPD	SIW	SIW	SISL	3-D IPD
Area (mm^2)	0.41	4	7.5	1520	684	1190	0.84
BW (GHz)	21–26.5	25.9–29.9	29.7–29.9	29.5–31.7	29.1–31	24.5–26.4	22.1–27.5
BW (%)	23	14.3	0.7	7.3	6.3	7.5	22
Iso. (dB)	n.c	n.c.	n.c.	−18	−21	−14	−12
RL (dB)	n.c	n.c.	n.c.	−18	−21	−11	−17.5
aIL (dB)	2.1–2.3	2.9–3.2	n.c.	0.3–1.1	0.3–0.42	1.1–2.1	1.3–1.7

By offering thick and wide metallizations, the 3-D technology presented in this paper reduces resistive losses compared to conventional IPD technologies while offering a much better integration density thanks to the exploitation of the third dimension. These features help to significantly improve performance and reduce manufacturing costs compared to traditional IPD technology, without increasing manufacturing complexity. The proposed 3-D Butler matrix combines relatively low insertion losses of at best 1.3 dB, thus coming close to the performance achieved by SIW technologies, with a footprint only twice as large as that of CMOS integrated matrices and five to ten times lower than IPD.

For applications where bandwidth is of great importance, SIW technology does not appear to be the best option. With a waveguide height and length driven by technology and crossover respectively, the few remaining degrees of freedom lead to a difficult trade-off between phase shifter return loss, bandwidth and phase difference with respect to the crossover [7, 8]. In addition, as the antennas are connected directly to the output of the Butler matrix, practical routing constraints require the addition of a crossover and a pair of phase shifters to cross the signals from ports 6 and 7 in Figure 1 and properly feed the antenna array. IPD technologies enable larger bandwidths but the design remains limited given the small number of metal layers most often available. The highest relative bandwidth of Table 1 (23 %) is achieved by the CMOS Butler matrix in [5] which takes advantage of the high number of metal layers to miniaturize each component and to adjust their characteristics relative to each other. The 3-D implementation of the Butler matrix, as proposed in this paper, relies on a large number of geometrical parameters that allowed us to reach the best performance trade-off and a 22 %-large bandwidth (Table 1).

Finally, when the Butler matrix operates in transmission, power handling must be considered. Qualitatively, when comparing metallization characteristics, it can be stated that the proposed 3-D Butler matrix can handle more power than CMOS solutions, but less than SIW technology.

6. Conclusion

A 4×4 Butler matrix is presented which meets requirements of beamforming for millimeter-wave 5G or other communication systems. The circuit has been implemented with a 3-D IPD technology based on three metallic levels, a thin Si_xN_y dielectric deposited at a low temperature for MIM capacitors, and a 110 µm-thick SU8 photoresist for the shaping of solenoids. The surface area of the fabricated matrix is less than 1 mm^2, while performances tend to peak as in the case of transmission losses at almost 1.3 dB. So, the trade-off between size and performances is much better compared to other published solutions. Also, the relative bandwidth of 22 % ranks this Butler matrix among the best published works in the 20–30 GHz frequency band. To summarize, this 3-D Butler matrix comes close to the compactness offered by solutions using the BEOL of CMOS technologies with performances close to SIW solutions.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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