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ITEC+EATS 2022 Short Course

Software-Defined Power Electronics: Theory and Study Cases

Matthias Preindl, Columbia University
Luiz Villa, University of Toulouse
Liwei Zhou, Columbia University
Matthew Jahnes, Columbia University
Jean Alinei, University of Toulouse

- I. Introduction (Luiz 9min, Matthias 12min, Luiz 9min).
- II. Software-Defined Control Techniques (Liwei 15min)
- III. Software-Defined Hardware Design (Matthew 30min)
- IV. Design case of Transformerless Converter (Liwei 15min)
- V. Zephyr-Based Implementation (Luiz 60min)
- VI. Design case of Multi-Level Converters (Matthias 15min)
- VII. Conclusion (Matthias 8min, Luiz 7min)

Introduction

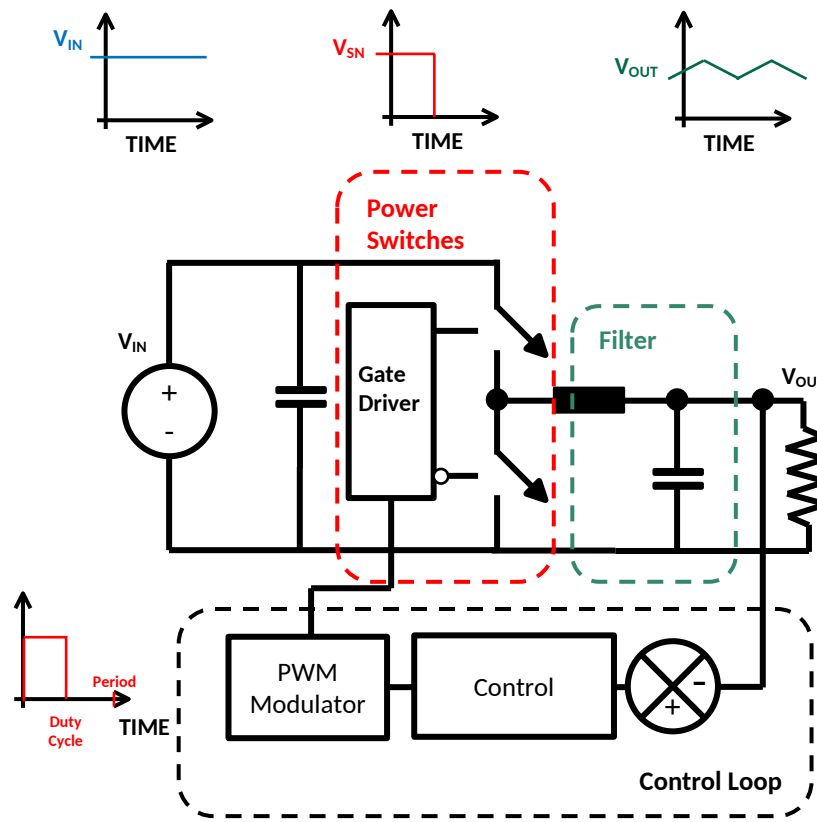
Matthias Preindl, Luiz Villa



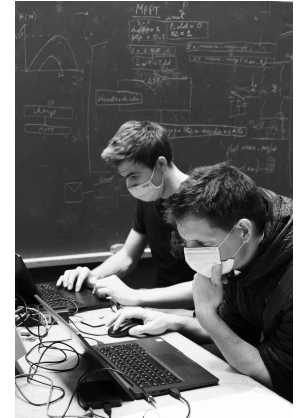
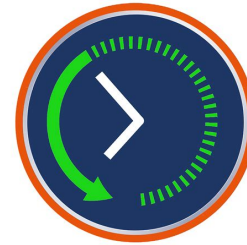
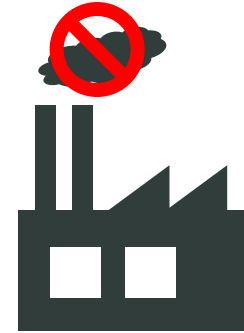
- Is a branch of electrical engineering
- Electronics that is made to handle power flows
 - Goes from mW to MW
 - DC-DC and DC-AC (1 or 3 phase)
- **Application-oriented design**
 - **Battery charging**
 - **Energy management**
 - **Motor control**
 - **Grid connection of renewables**



- Power converters regulate voltages and/or currents in either DC or AC
- Regulation is done through control loops
- Control loops use measurements to regulate power flow
- Power flow is controlled via PWM signals sent to the power switches via gate driver circuits
- Output filters smooth out the output voltage and current
- **Real-Time is critical for stability**
- **The P.E. community is very analog solution oriented**
- **We believe the time is ripe for digitalizing power electronics**



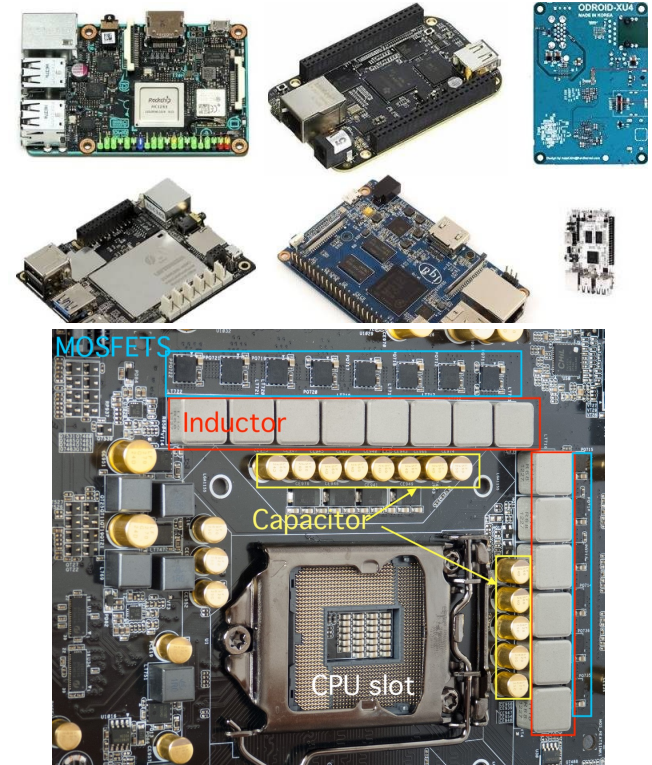
- Decarbonizing the economy will require more electricity
- More electricity will require more power electronics
- Digitalization has emerged as a means to reduce time-to-market and standardize the development of solutions
- **Energy transition will be greatly accelerated if power electronics becomes more standardized, modular and digital**



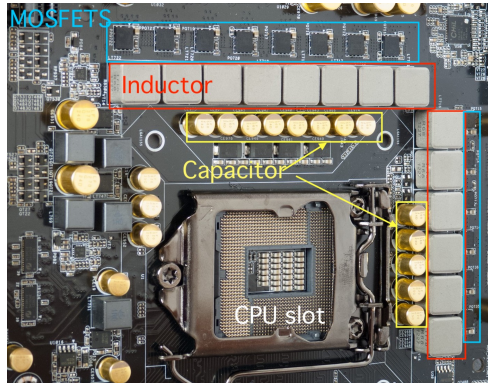
Two examples give a good idea of the state of the art of digitalization

- IoT
 - Fully integrated software stack
 - No more bare metal
- Digital Power controllers
 - Bare metal
 - Ultra-flexible micro-controllers with specialized peripherals
 - High integration between peripherals
 - Specialized for real-time control
 - Integrated fault-management and telemetry protocols

The Problem: On which target can we combine the abstraction API approach of IoT with the performance of dedicated analog peripherals ?

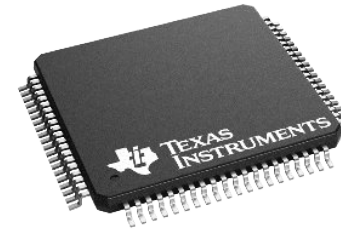


- Multiple silicon vendors have Digital power SoC in their portfolios
- Some are Function defined
 - Multiphase converters for CPU power delivery






- Provide Telemetry
- Optimize control laws
- Tied to a specific use case

- Some are reprogrammable as they can cover multiple power topologies.

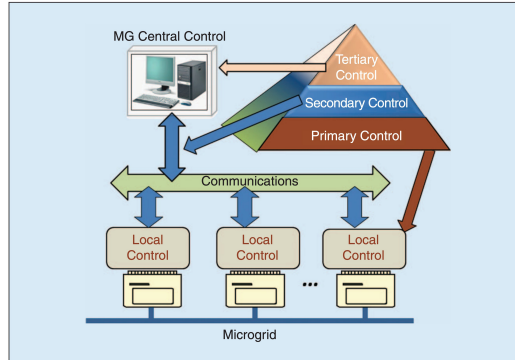


- Digital power SoC do have
 - Dedicated High Resolution PWM generators
 - Dedicated Fast Analog peripheral
 - ADC, DAC and comparators
 - Dedicated Hardware for fast control computation
- Some require vendor specific languages and libraries

Wind Turbine	Generator Set	Fuel Cell
PM1000 provides power flow control of the wind turbine's output.	2MW gen-set converter for UK MOD naval applications.	PM1000 used to provide a regulated output voltage from the fuel cell.
		

Power Electronics Building Blocks (PEBB):

- Power component.
- Control card.
- Cooling system.
- Communication system.



Microgrid Hierarchical Control Structure:

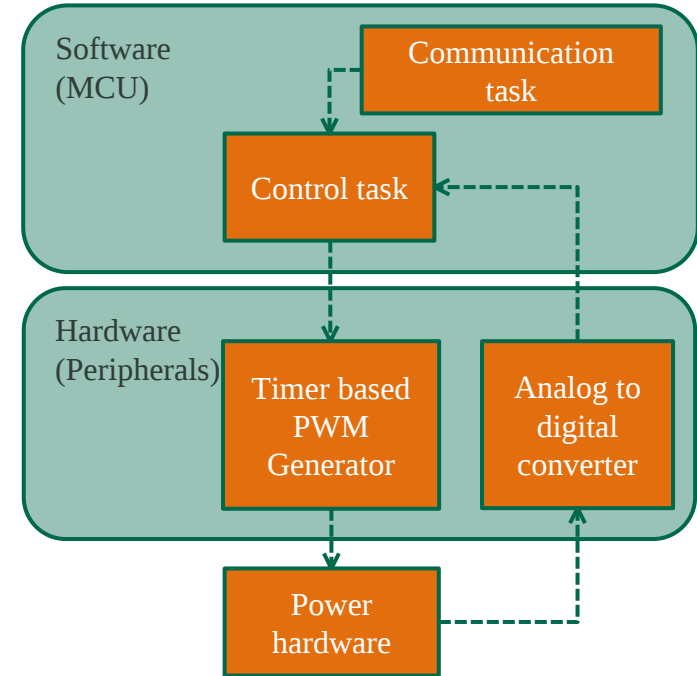
- Grid level central control.
- Distributed resource level local control.
- Communication system.
- Multi-layer control structure.

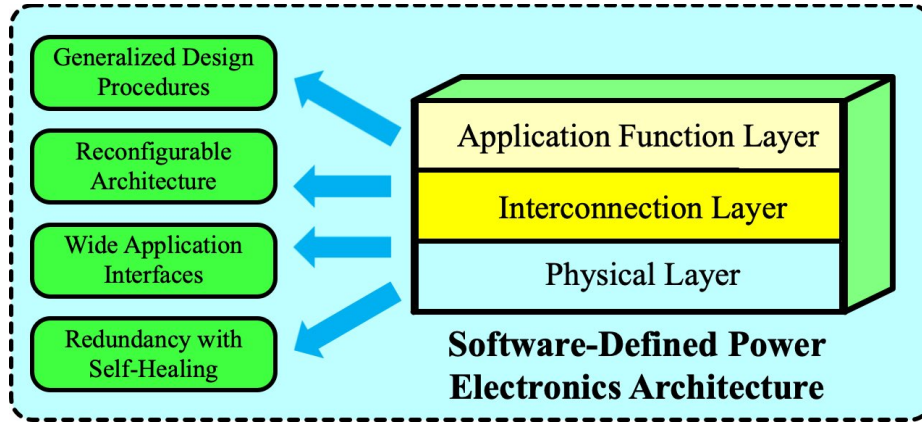
The digital power electronics stack has two parts: Software and Hardware Peripherals

- Software handles communication tasks and control
- Hardware comprises PWM Generation and ADC operation

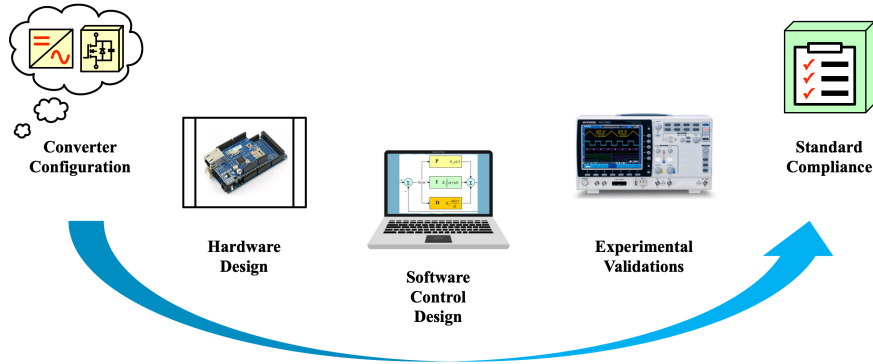
Low level loop

- The power hardware sends data to the ADC and receives the PWM from the Timer
- The control task drives the PWM





- **Application Layer:** Interfaced with Different load/source applications, e.g., EV battery, single/three-phase grid, solar, motor.
- **Interconnection Layer:** Manage power converters from module to integrated circuit; central power/voltage/current control functions.
- **Physical Layer:** Voltage/current source types of module; local voltage/current stabilization; PWM modulation.

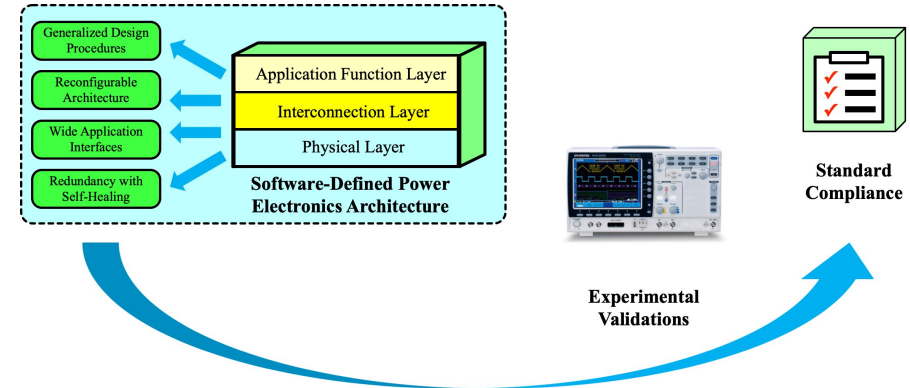


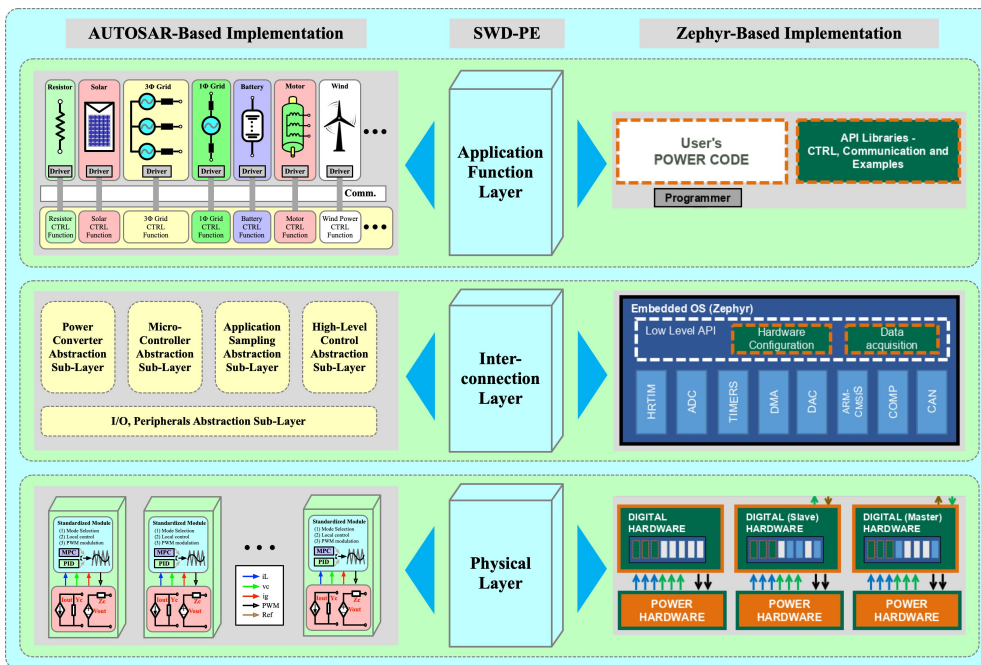
Conventional Power Electronics Design:

- Various interfaced applications.
- Different power ratings.
- Hardware design.
- Software design.

Software-Defined Power Electronics:

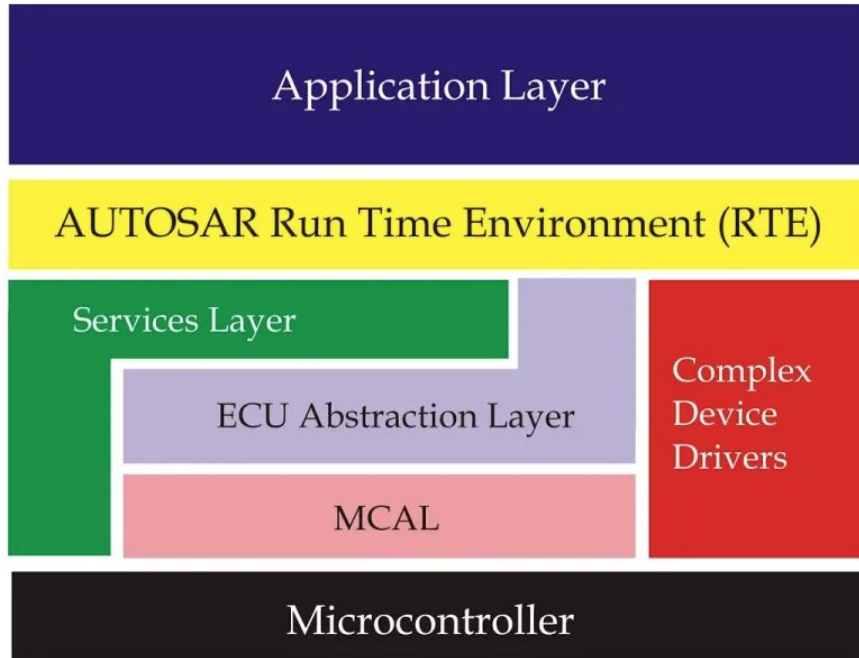
- Generalized design procedures.
- Reconfigurable architecture.
- Wide application interfaces.
- Redundancy with self-healing.





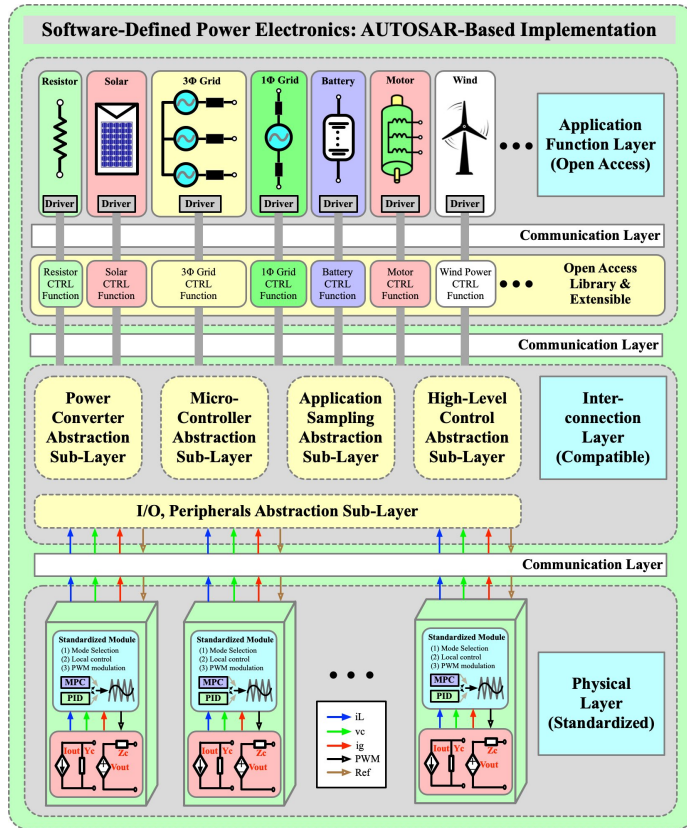
Two Multi-Layer Implementations:

- AUTOSAR-based implementation.
- Zephyr-based implementation.



AUTOSAR Structure:

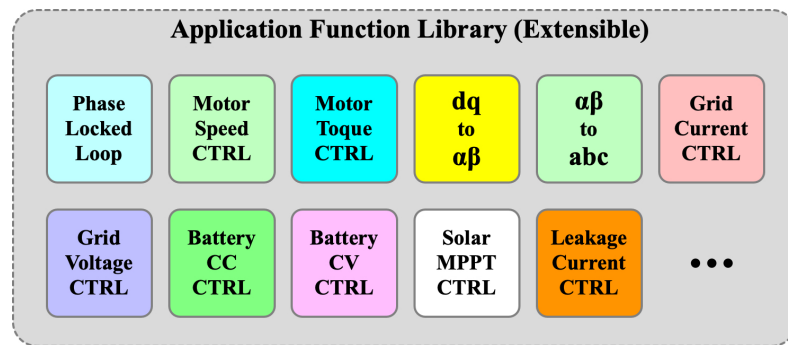
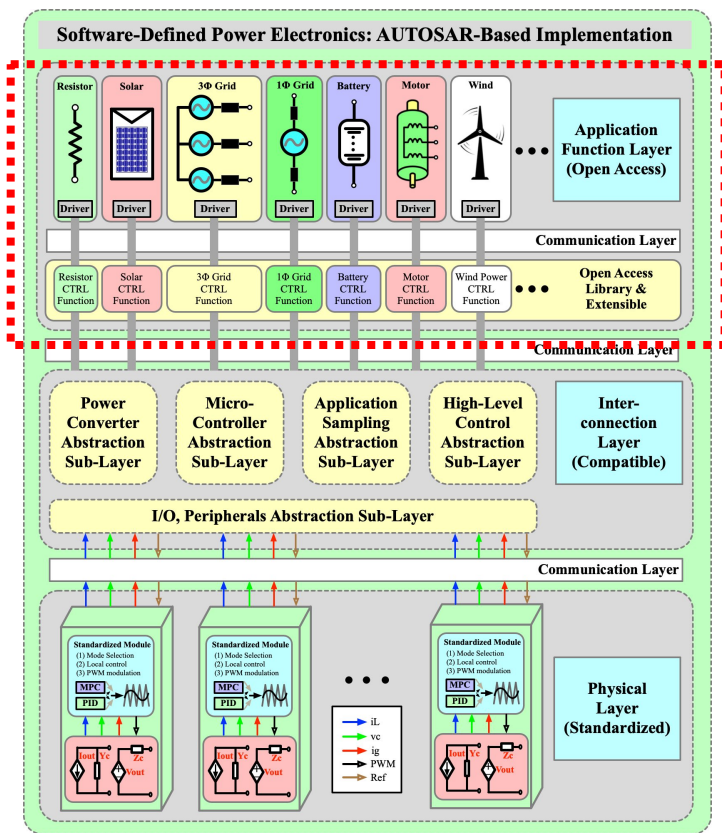
- Application Layer: application code.
- AUTOSAR RTE: Running time environment.
- Service Layer: application services.
- ECU Abstraction Layer: I/O, hardware.
- MCAL: micro-controller system.

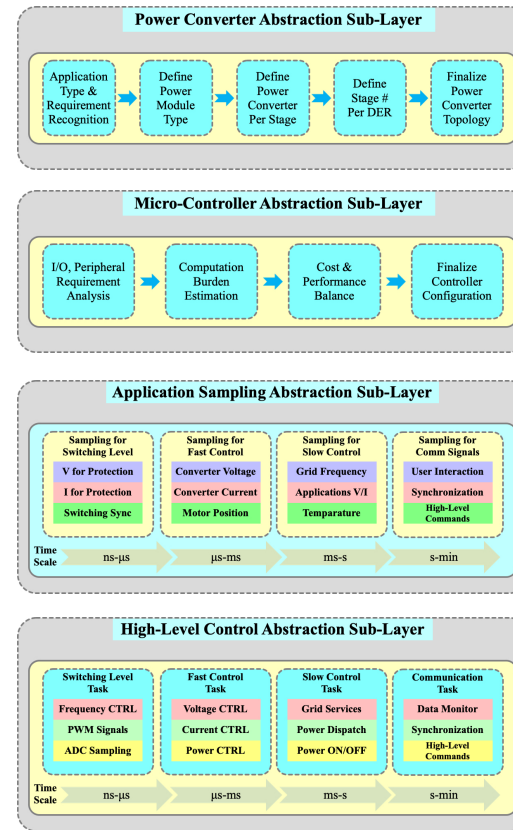
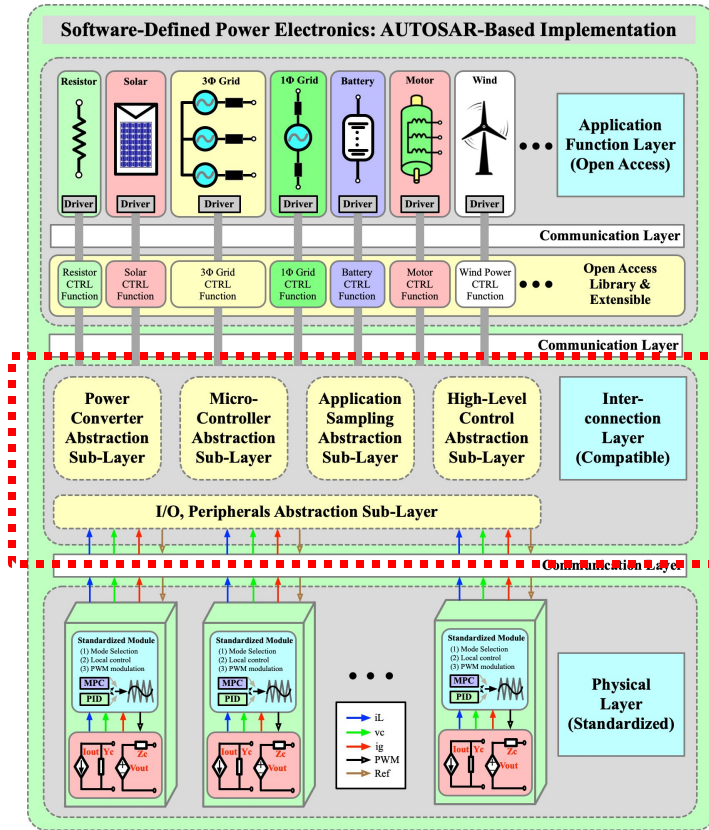


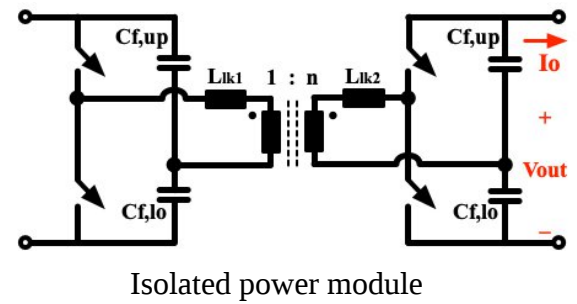
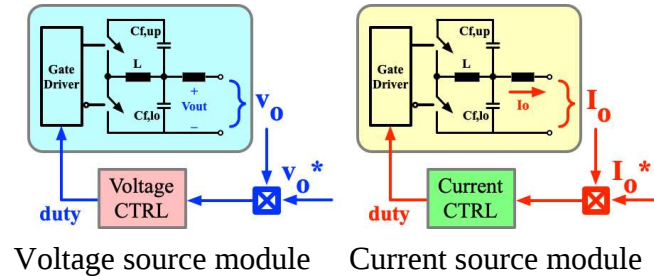
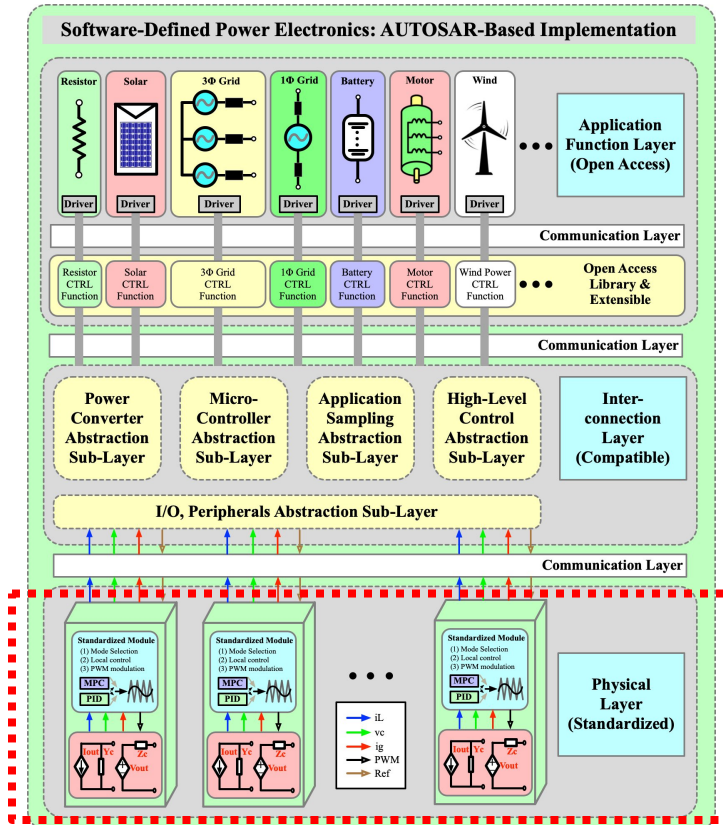
➤ **Application Layer:** Interfaces and functions with different load/source applications, e.g., EV battery, single/three-phase grid, solar, motor.

➤ **Interconnection Layer:** Link between application and physical layers; manage power converters from module to integrated system; central power/voltage/current control functions.

➤ **Physical Layer:** Voltage/current source types of module; local voltage/current stabilization; PWM modulation.







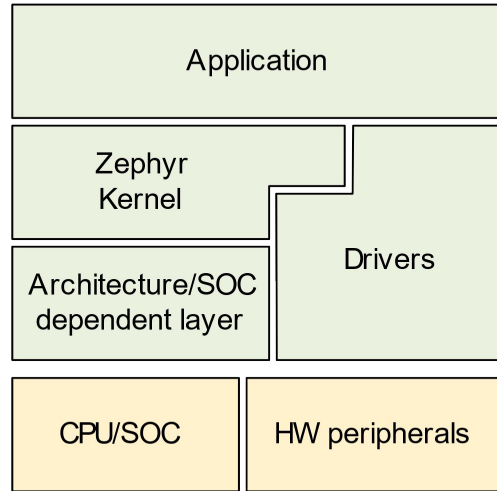
Module Configuration:

- Upper/lower power switches.
- Upper/lower output capacitors.
- Switch side inductor (optimized).

Communications:

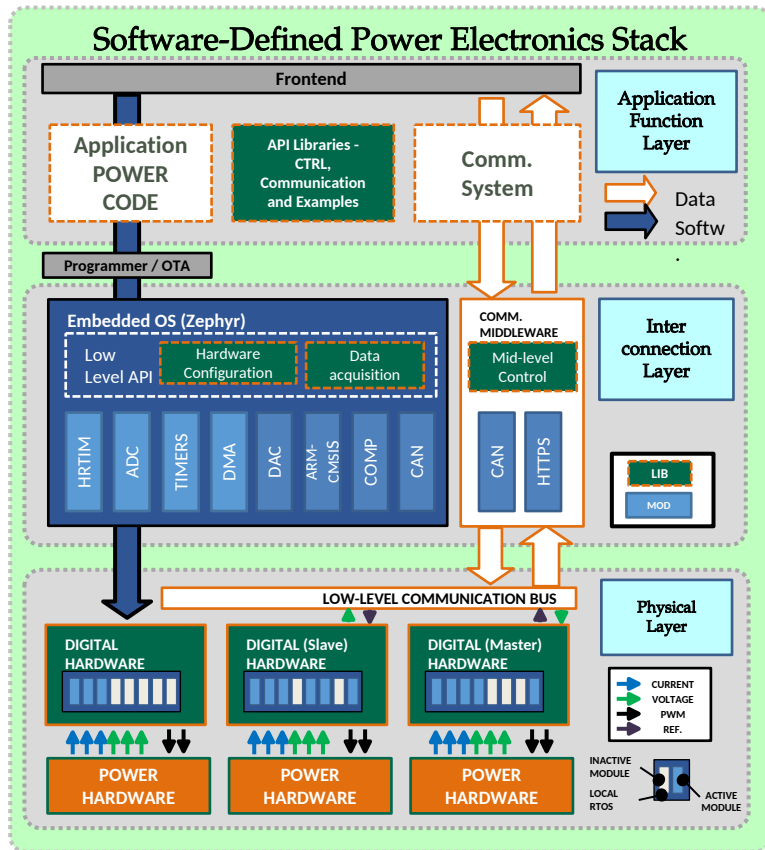
- CAN: Controller Area Network.
- FSI: Fast Serial Interface from TI.
- Ethernet.

Normal Zephyr layering

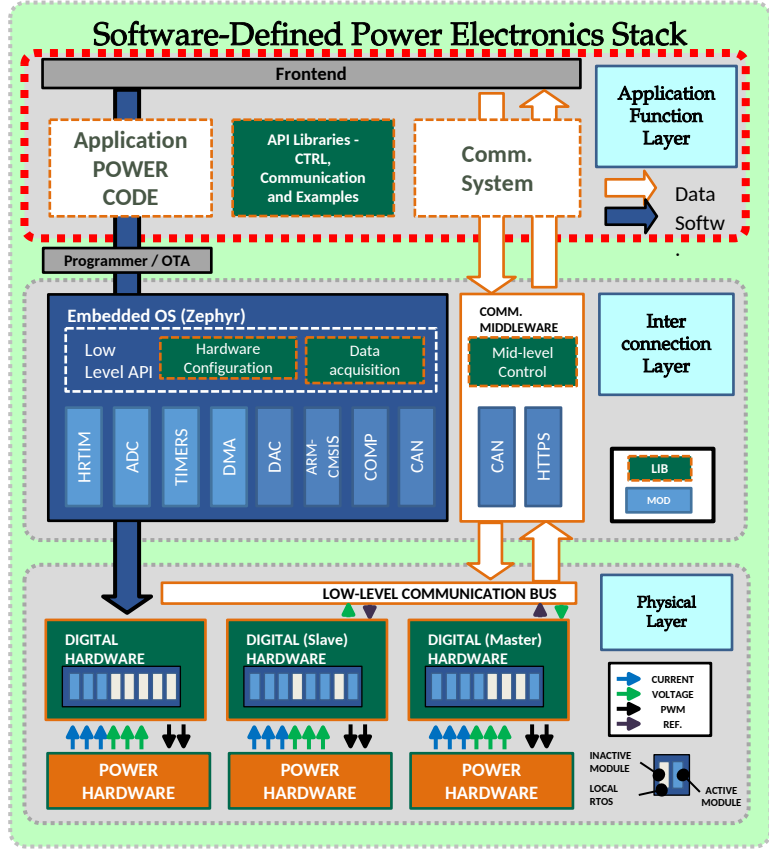


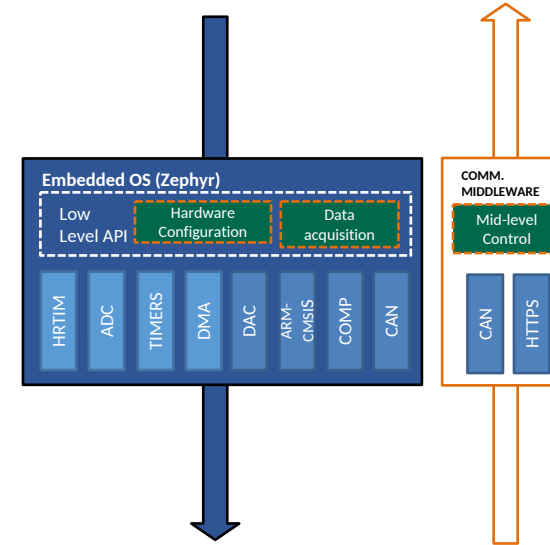
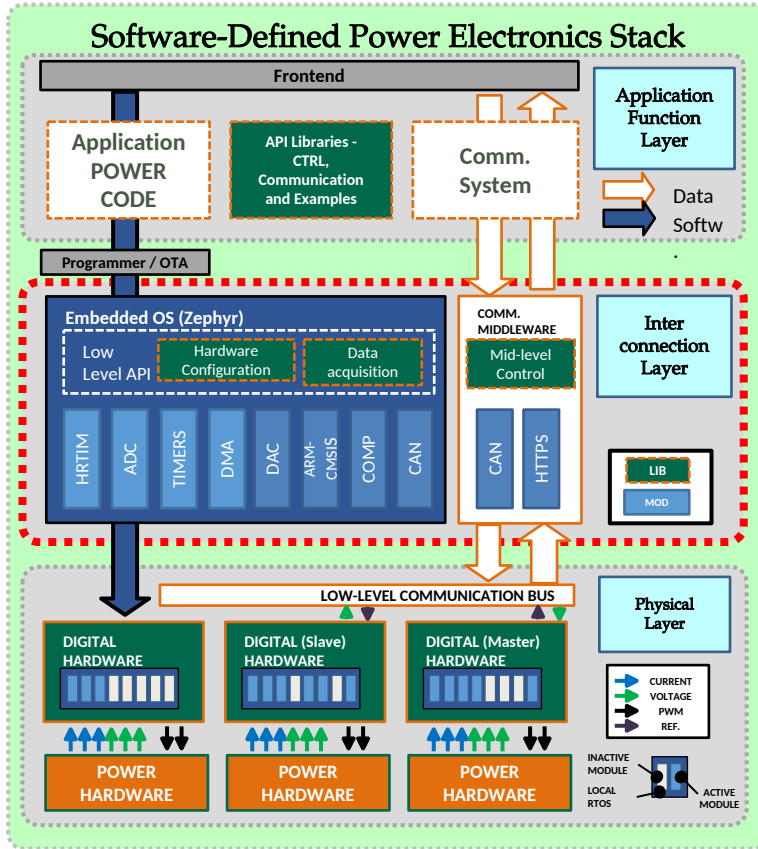
Zephyr Structure:

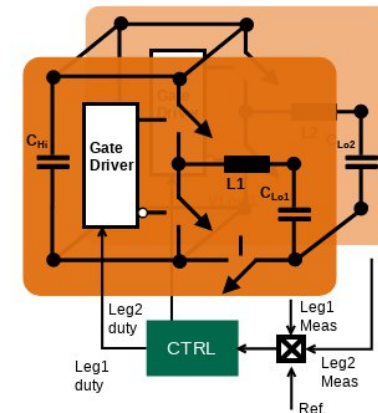
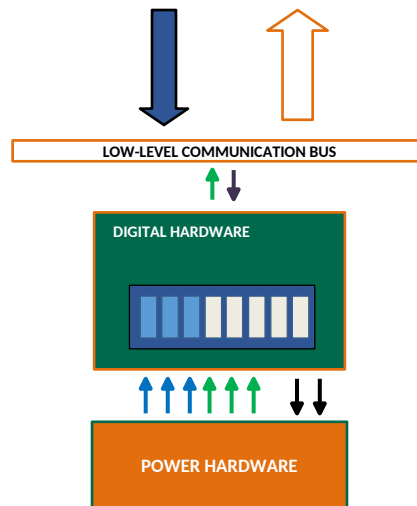
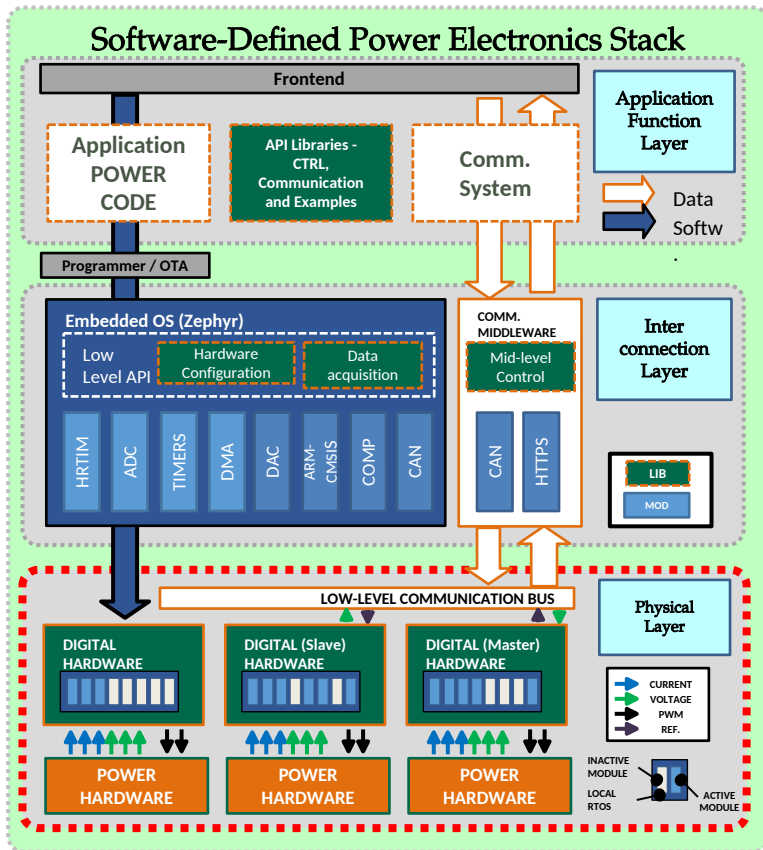
- Application Layer: application code.
- ZEPHYR KERNEL: Running time environment
- Architecture/SOC dependent layer: peripherals unique to the target SOC
- Drivers Layer: Hardware agnostic drivers for SOC and peripherals
- SOC-HW peripherals: micro-controller system.

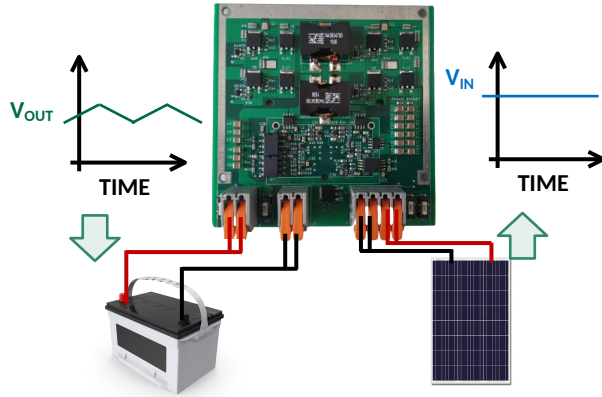


- **Application Layer:**
 - A frontend for data visualization and firmware update
 - Libraries provide functions for power and data
- **Interconnection Layer:**
 - A programmer/over the air links the application to the Zephyr based system for code compiling and update
 - A communication middleware provides bi-directional data flow and mid-layer control
- **Physical Layer:**
 - Each module is composed of a digital and power hardware connected to a low-level communication bus
 - Multiple control schemes can be implemented: Decentralized, Mid-level or frontend based
- **Downlink and Uplink**
 - The downlink flashes onto the digital hardware
 - The uplink is done from a low-level bus to a communication system via a middleware







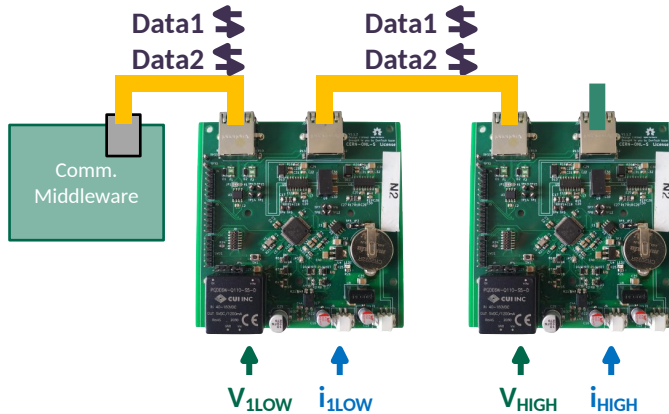


Power Module Configuration:

- Two legs and a NGND switch
- Bi-directional DC-DC Buck/Boost
- Single phase DC-AC

Digital Module Configuration:

- CAN: Controller Area Network.
- USB: Bootloader Programming and Over the Air capabilities
- Serial and other extensions possible



Software-Defined Control Techniques

Liwei Zhou

- **Goal:** find the best control sequence over a future horizon of N steps

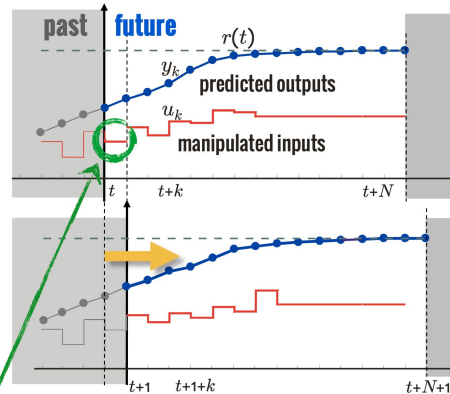
$$\min \sum_{k=0}^{N-1} \|W^y(y_k - r(t))\|_2^2 + \|W^u(u_k - u_r(t))\|_2^2$$

s.t. $x_{k+1} = f(x_k, u_k)$ prediction model
 $y_k = g(x_k, u_k)$

$u_{\min} \leq u_k \leq u_{\max}$ constraints
 $y_{\min} \leq y_k \leq y_{\max}$

$x_0 = x(t)$ state feedback

→ optimization problem

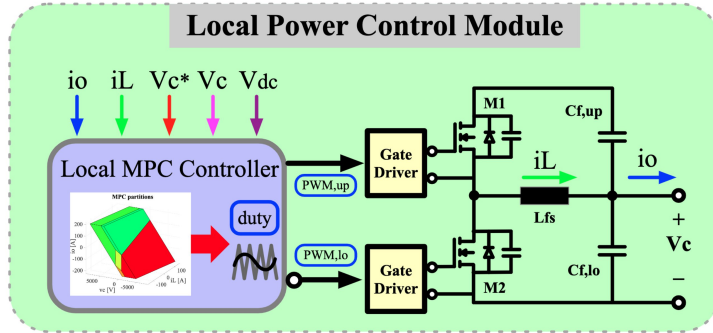


Advantages of MPC:

- Better dynamic performance.
 - Multi-objective optimization.
 - Optimize current timeslot with future timeslots in account.
- **At each time t :**
 - get new measurements to update the estimate of the current state $x(t)$
 - solve the optimization problem with respect to $\{u_0, \dots, u_{N-1}\}$
 - apply only the first optimal move $u(t) = u_0^*$, discard the remaining samples

[1] 2019 A. Bemporad - "Model Predictive Control"

Model Predictive Control for Modular Power Converters



Discrete State Space Equations:

$$i_{Lfs}(k+1) = i_{Lfs}(k) - \frac{T_s}{L_{fs}} v_{Cf}(k) + \frac{V_{dc} T_s}{L_{fs}} d(k)$$

$$v_{Cf}(k+1) = \frac{T_s}{C_f} i_{Lfs}(k) + v_{Cf}(k) - \frac{T_s}{C_f} i_{Lfg}(k).$$

Standardized Format:

$$X_{k+1} = AX_k + Bu_k + Ee_k$$

$$A = \begin{bmatrix} 1 - \frac{R_{Lfs}}{L_{fs}} & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix},$$

$$X_k = \begin{bmatrix} i_{Lfs}(k) \\ v_{Cf}(k) \end{bmatrix}, u_k = [V_{dc} d(k)], e_k = [i_{Lfg}(k)].$$

Cost Function:

$$\min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^T R \Delta u_k.$$

Constraints:

$$\tilde{X}_{k+1} = A\tilde{X}_k + Bu_k + Ee_k \in \mathcal{X}$$

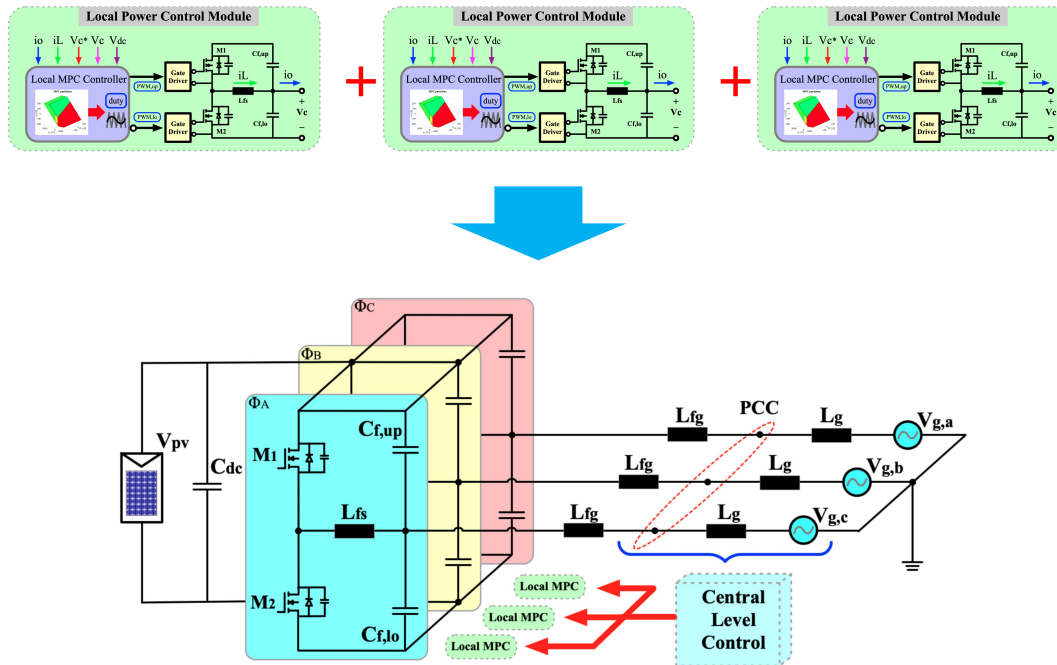
$$\Delta u_k = u_k - u_{k-1} \in \mathcal{U}$$

$$\begin{bmatrix} -I_{Lfs,max} \\ 0 \end{bmatrix} \leq X_k \leq \begin{bmatrix} I_{Lfs,max} \\ V_{dc} \end{bmatrix}$$

$$[0] \leq u_k \leq [V_{dc}]$$

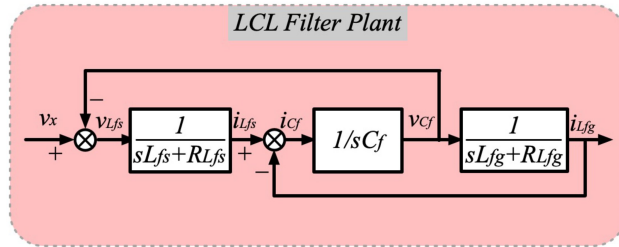
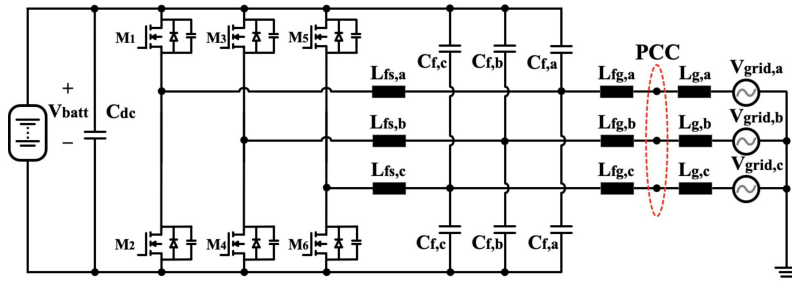
$$[-I_{Lfg,max}] \leq e_k \leq [I_{Lfg,max}].$$

Model Predictive Control for Modular Power Converters

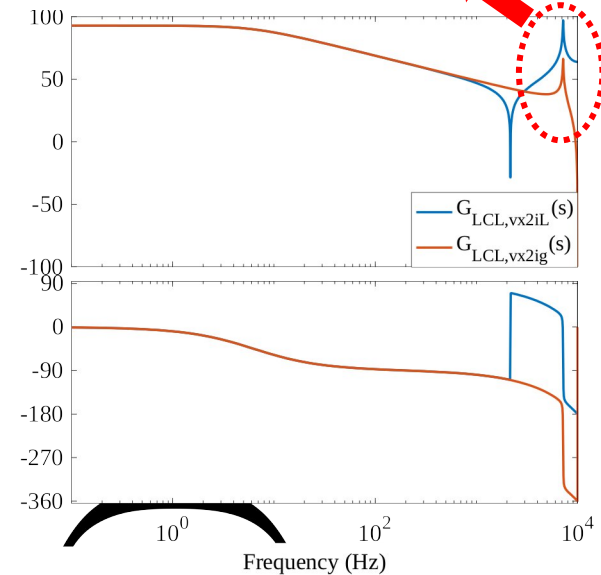


- **Motivations:** MPC for better dynamic performance; MPC for LCL filter active resonance damping.
- **Methods:** Modular MPC cascaded control structure including outer loop PI and inner loop per module MPC.
- **Merits:** Improved transient performance; Less resonance spikes; Higher control bandwidth.

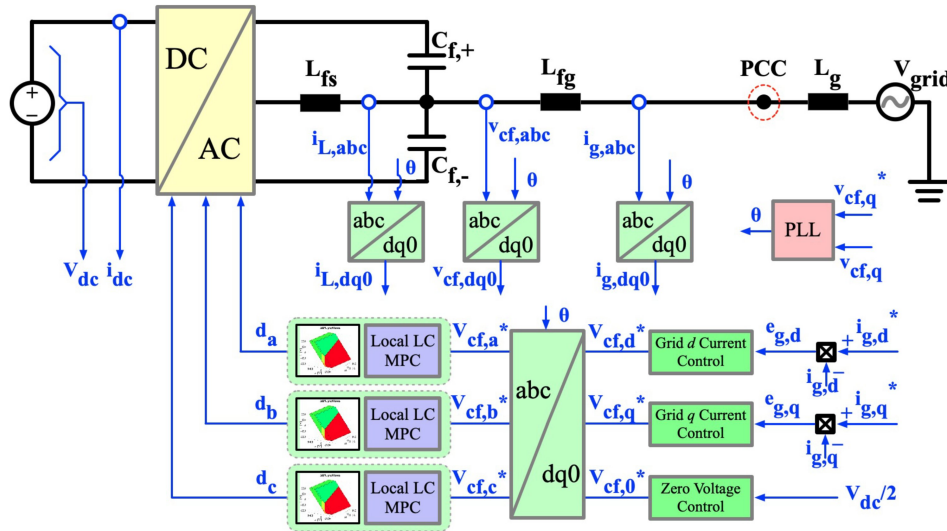
Resonance Issue in Typical LCL Filter Inverter System



LCL Filter Resonance Spikes

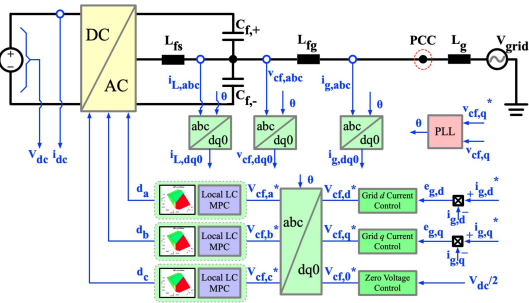


Modular Model Predictive Control for Active Damping

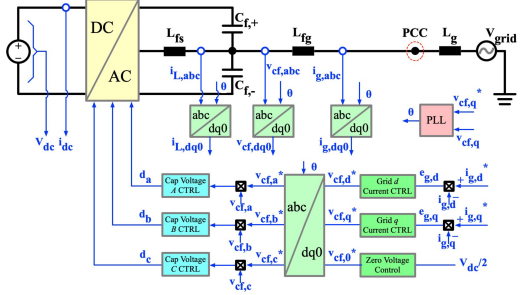


- **Outer Loop Grid Current Control:** Regulate grid current in $dq0$ reference frame with PI controller to derive the output capacitor references for inner loop MPC.
- **Inner Loop Per Module MPC Control:** Regulate output capacitor voltage in abc reference frame with MPC by receiving reference from outer loop PI.
- **Phase-Locked Loop:** Transformations between abc and $dq0$ reference frame for control purpose.

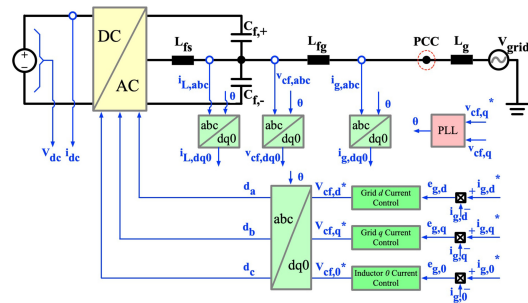
Modular Model Predictive Control for Active Damping



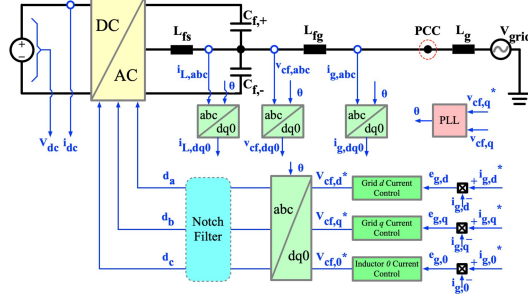
Proposed Modular MPC



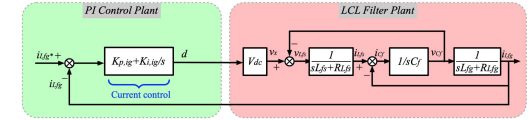
Cascaded PI control



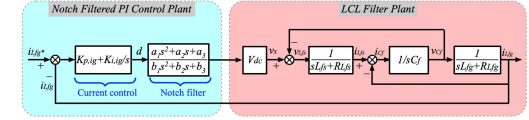
Conventional PI control



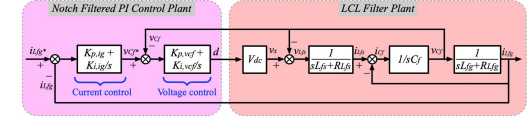
PI + Notch Filter control



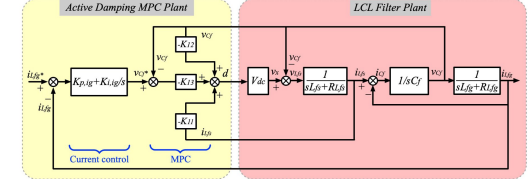
(a) PI control.



(b) Notch filtered PI control.



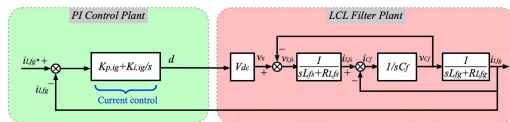
(c) Cascaded PI control.



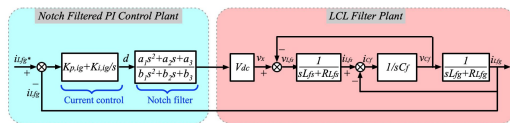
(d) Active damping MPC.



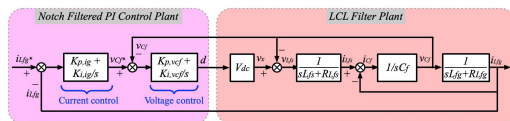
MPC Active Damping Mechanism



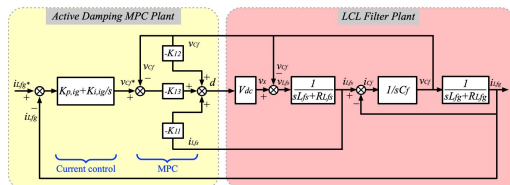
(a) PI control.



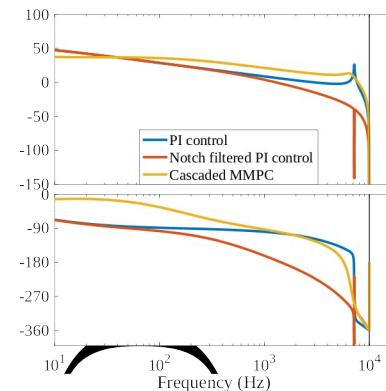
(b) Notch filtered PI control.



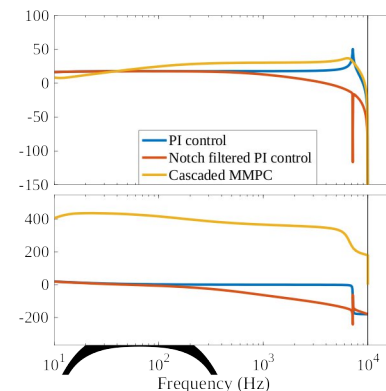
(c) Cascaded PI control.



(d) Active damping MPC.

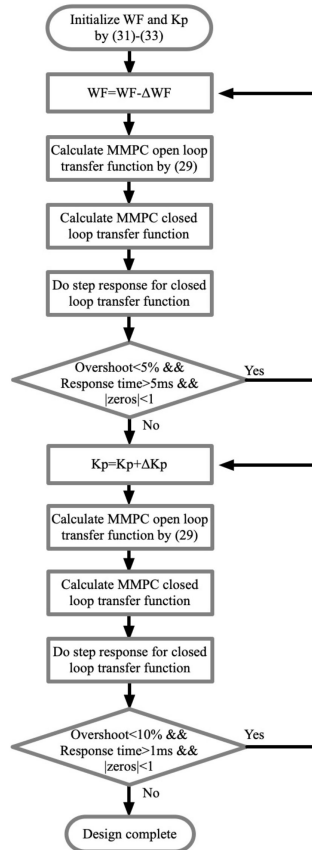


From Igrid error to Igrid

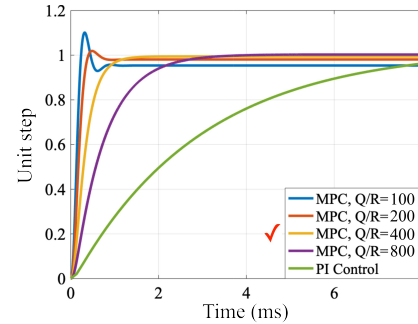


From Igrid error to Vcf

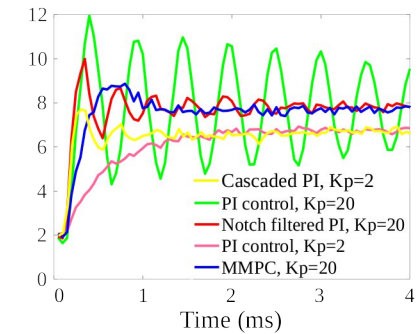
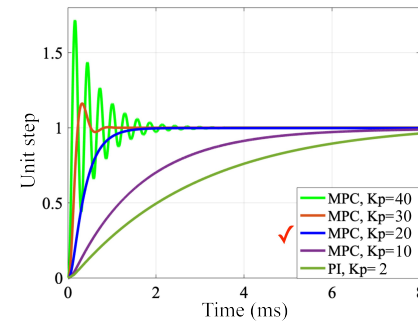
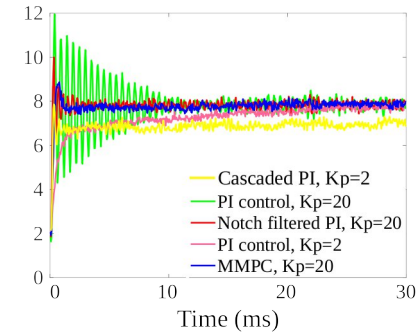
MPC Control Parameters Design Method

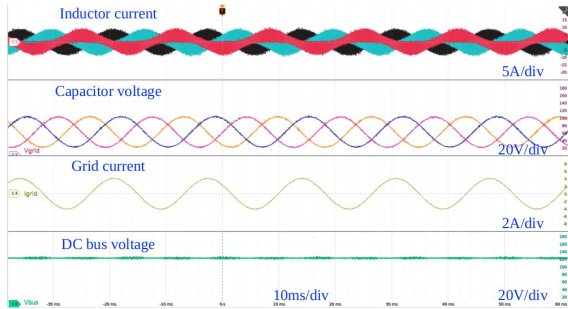


Control Parameters Simulation Tuning

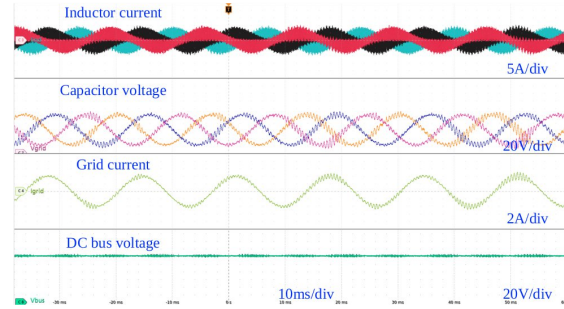


Control Parameters Experimental Validation

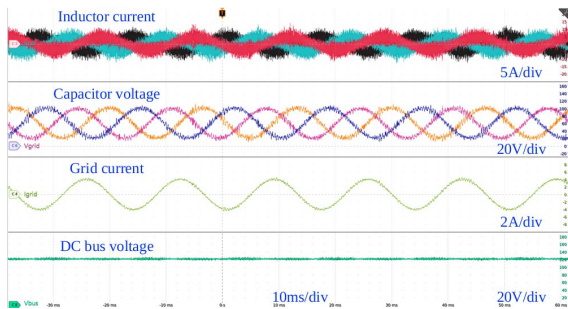




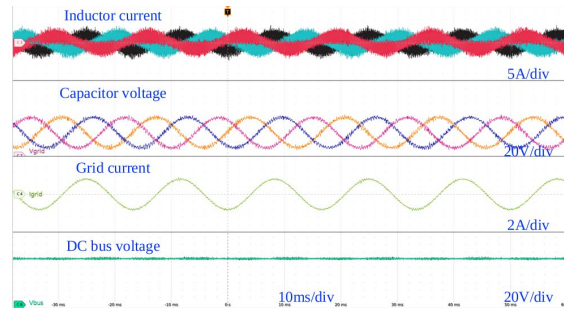
Proposed MPC with high gain



Conventional PI with high gain



Notch filtered PI with high gain

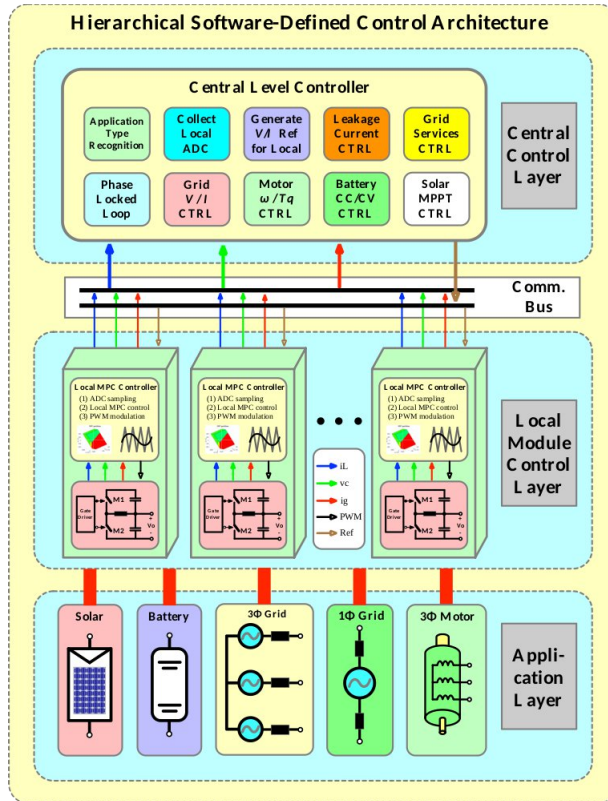


Cascaded PI with high gain

Validated Merits of designed MPC:

- Active damping for LCL filter.
- Better dynamic performance.
- High control bandwidth.
- Less oscillation in steady state.

Hierarchical Software-Defined Power Electronics Architecture

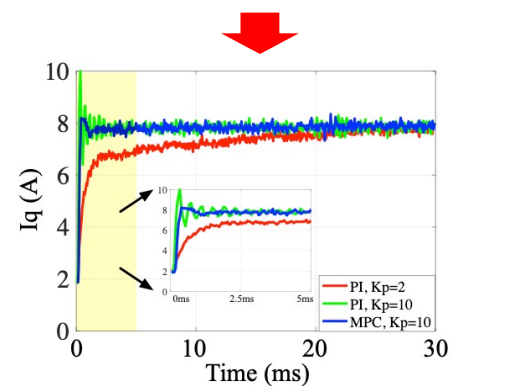
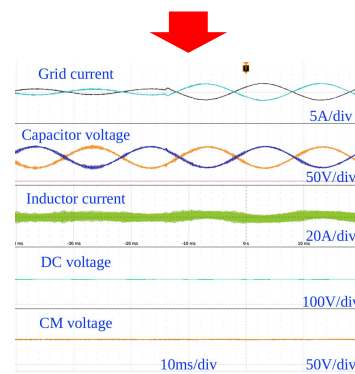
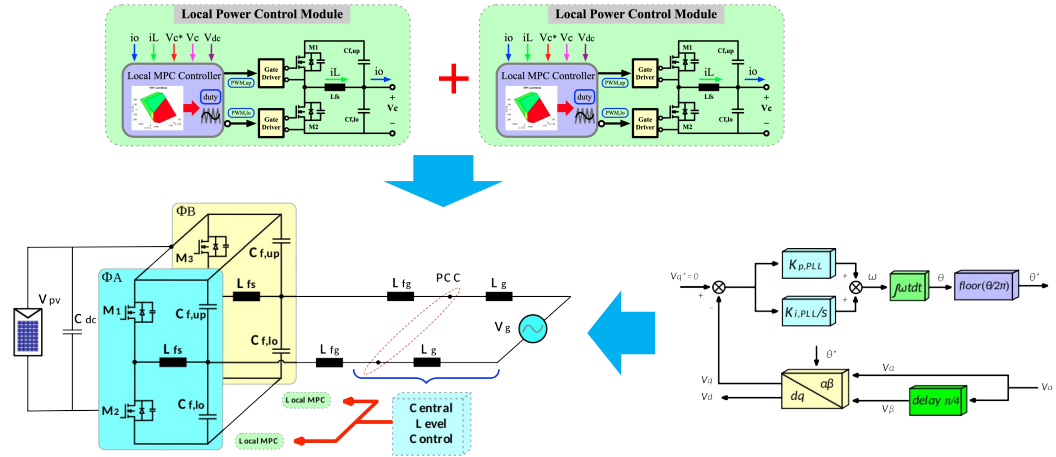
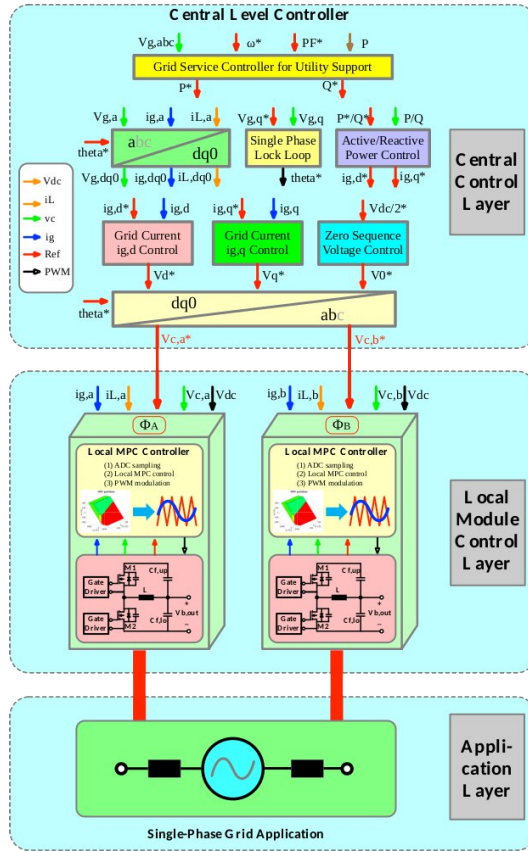


➤ **Central Control Layer:** Manage power converters from module to integrated circuitry topology; central voltage/current/power/torque/speed control functions; application type recognition.

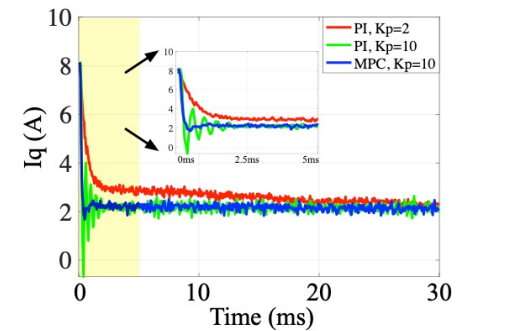
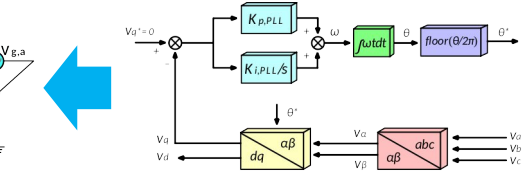
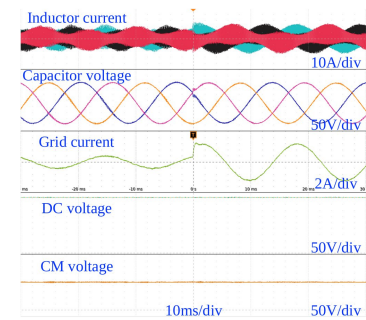
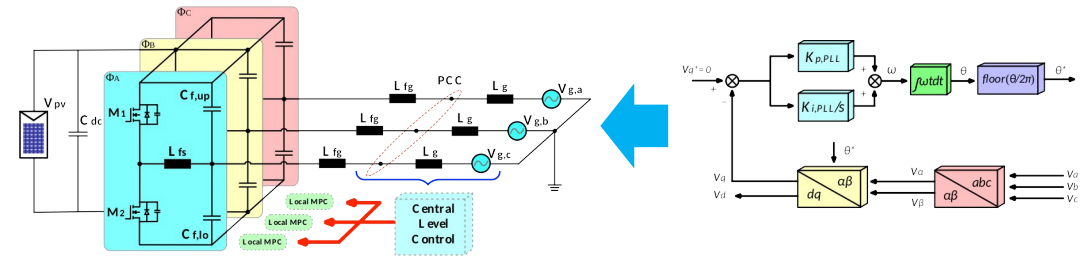
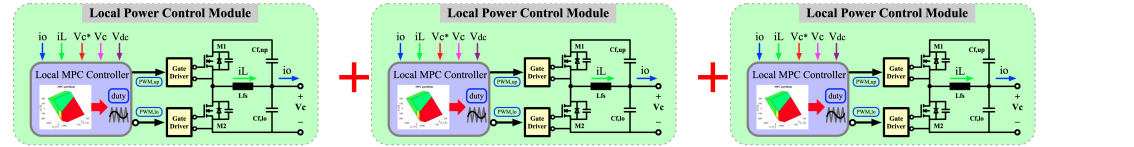
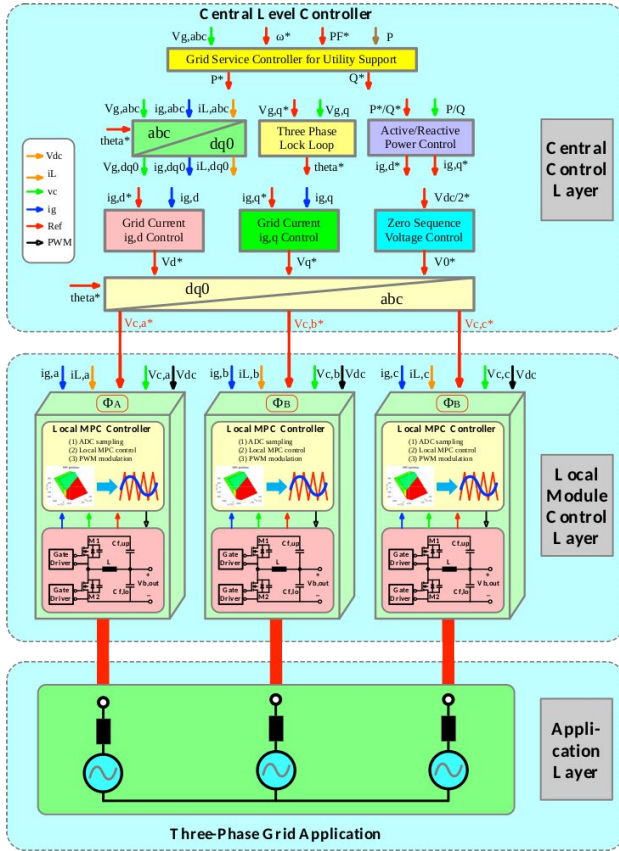
➤ **Local Power Module Layer:** Local voltage/current MPC control; variable-frequency critical-soft-switching control; state observer; PWM modulation.

➤ **Application Layer:** Interfaces with different electrified load/source applications, e.g., EV battery, single/three-phase grid, solar, motor.

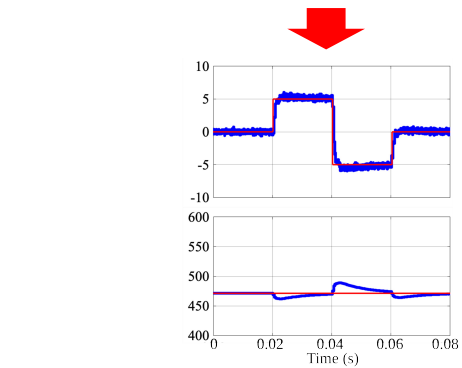
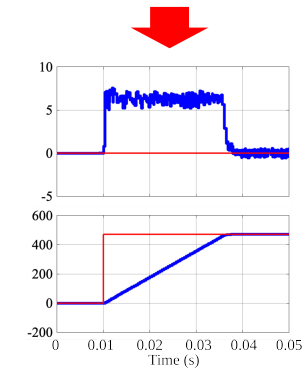
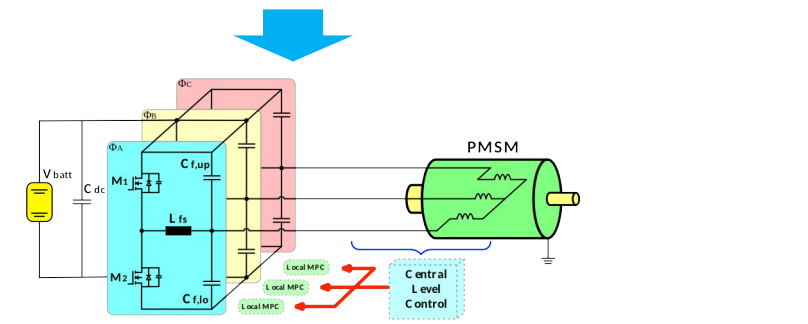
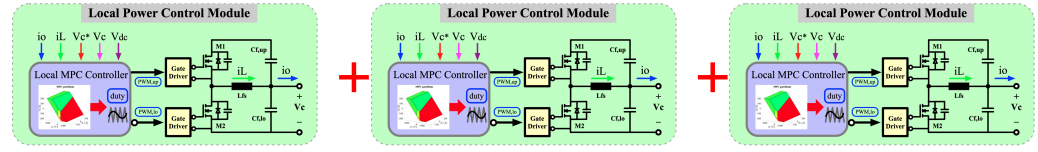
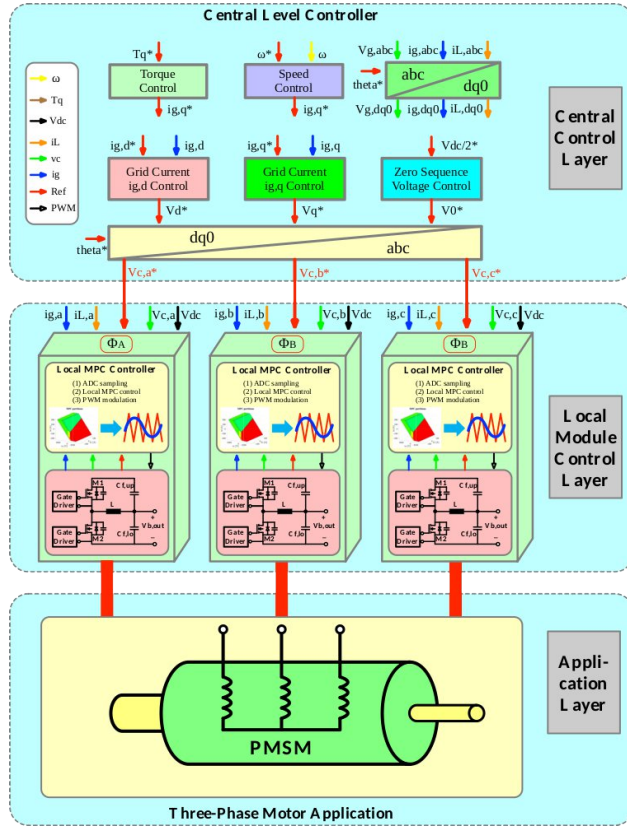
Single-Phase Grid-Connection Application



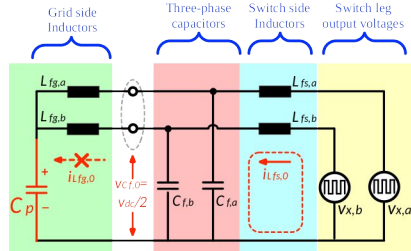
Three-Phase Grid-Connection Application



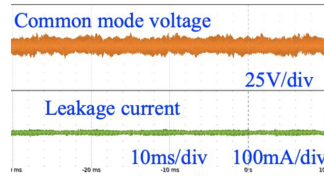
Three-Phase Motor Traction Application



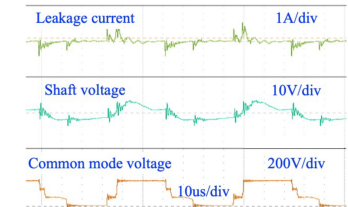
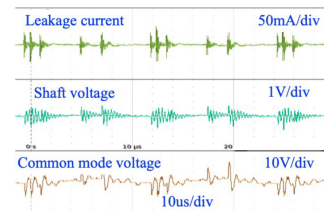
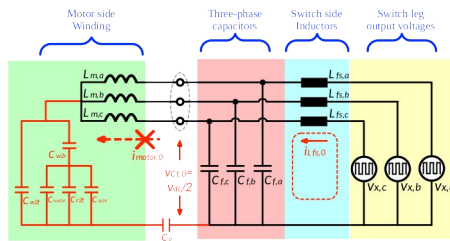
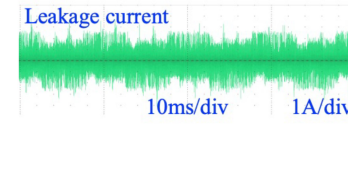
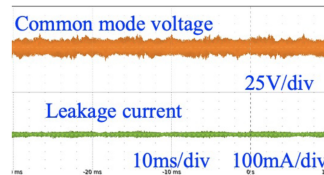
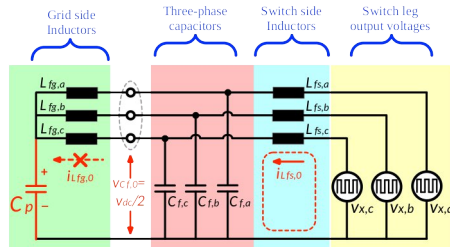
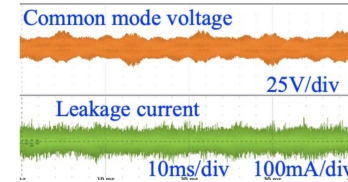
Merits of Zero-Sequence Stabilization for Low CM Noise



Proposed Control and Topology:



Conventional Control and Topology:



Software-Defined Hardware Design

Matthew Jahnes

Achieving High Efficiency and High Power Density Modules

4 Methods:

1) Upper Capacitor topology

- reduction in both EMI and capacitance RMS ripple for a given output capacitance
- allows for reduction in output capacitance

2) Variable Frequency Critical Soft Switching (VFCSS)

- enables an increase in switching by factor of 5, reduction in inductance by factor of 10, without sacrificing efficiency

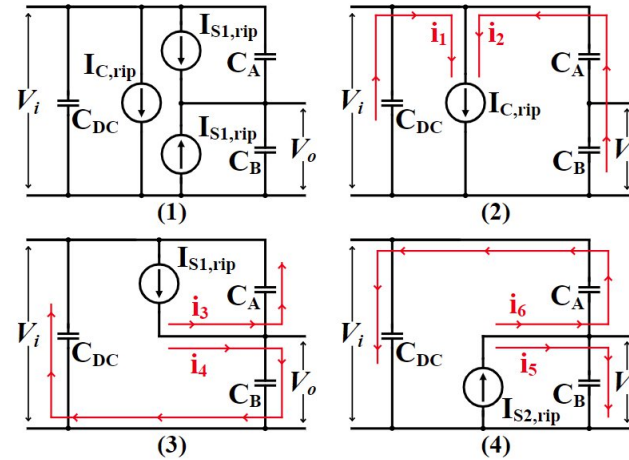
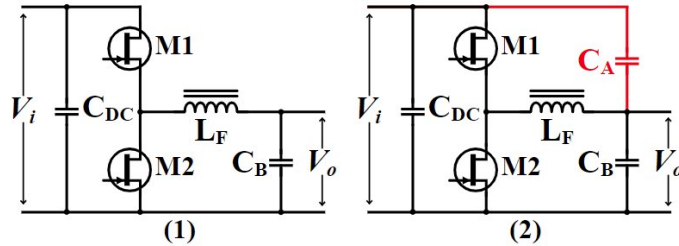
3) Additional C_{oss} Capacitance

- used in conjunction with critical soft switching scheme to reduce turn-off switching losses

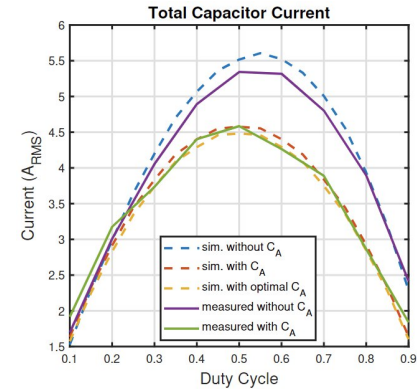
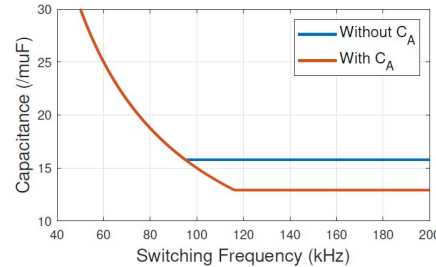
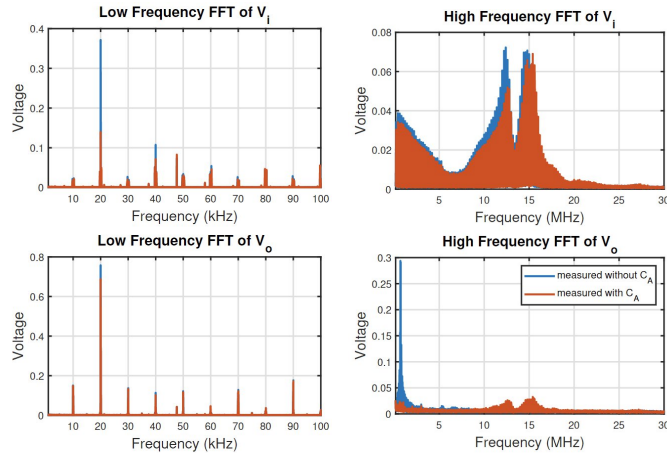
4) Optimization process for both size and efficiency

- procedure to optimize for both size and efficiency simultaneously

Upper Capacitor Topology



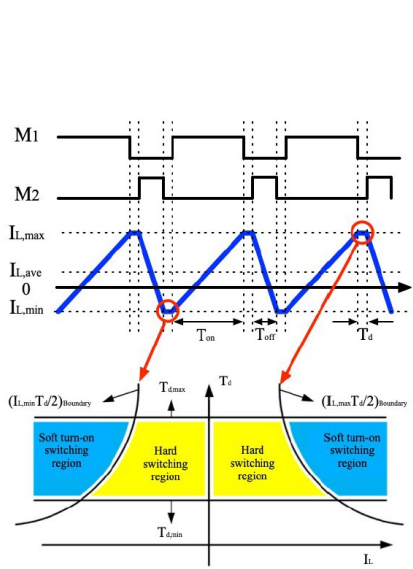
- Upper capacitor C_A is not included in typical buck converters
- It allows for differential mode ripple currents present at V_o and V_i to be cancelled
- Increasing f_{sw} is a common way to reduce required inductance and capacitance
- However, it becomes ineffective beyond a certain frequency as the limit of ripple current handling capability of the output capacitance is reached



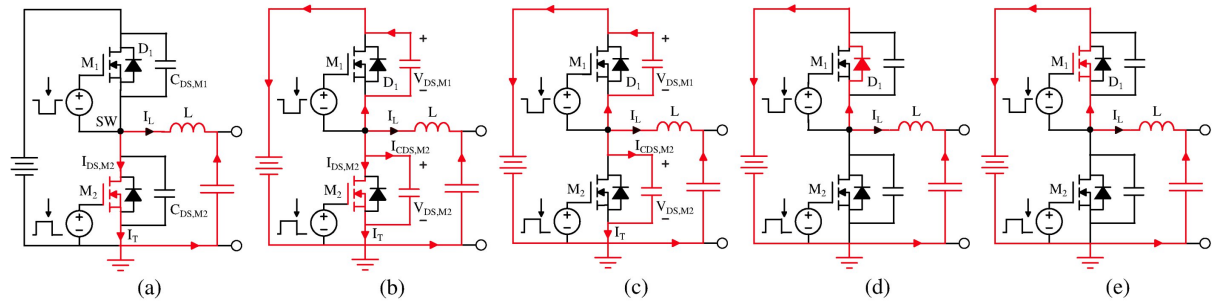
- By partially cancelling out ripple currents within the output capacitance, we can lessen the ripple current handling capacitance requirements
- For a given total capacitance, allocating a proportion to C_A brings:
 - over 50% reduction in the switching frequency harmonic
 - over 20% reduction in total capacitor ripple current

☑ **This allows for a reduction in output filter capacitance value and size**

Variable Frequency Critical Soft Switching (VFCSS)



VFCSS regions of operation

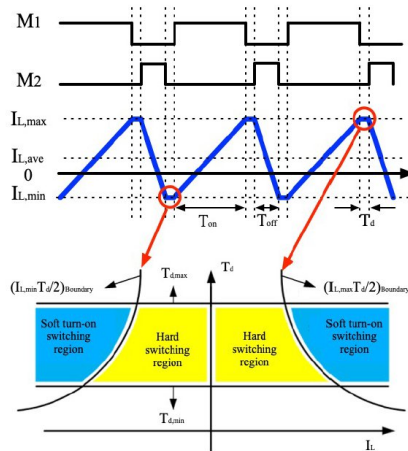


Critical Soft Switching allows for C_{ds} capacitors to be charged/discharged through the natural current commutation of the inductor current

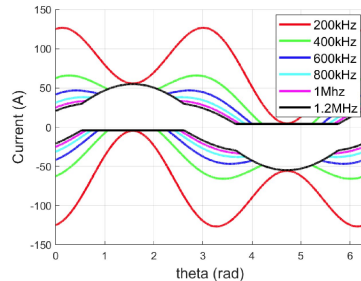
- and not by applying a step voltage during a forced V_{ds} transition
- instead, **FETs are switched “on” after the C_{ds} capacitances have transitioned in voltage** (charged/discharged)
- this transition occurs during the deadtime of the switching states
- the product of the deadtime and the inductor current needs to be sufficient to charge/discharge C_{ds} of both FETs

This allows for the exchange of turn-on losses for turn-off losses

B. Agrawal, L. Zhou, A. Emadi and M. Preindl, "Variable-Frequency Critical Soft-Switching of Wide-Bandgap Devices for Efficient High-Frequency Nonisolated DC-DC Converters," in *IEEE Transactions on Vehicular Technology*, vol. 69, no. 6, pp. 6094-6106, June 2020, doi: 10.1109/TVT.2020.2987028.
 L. Zhou and M. Preindl, "Optimal Frequency and Critical Soft Switching Control of DC/DC Converter," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 1536-1541, doi: 10.1109/ECCE.2019.8912991.
 L. Zhou and M. Preindl, "Variable-Switching Constant-Sampling Frequency Critical Soft Switching MPC for DC/DC Converters," in *IEEE Transactions on Energy Conversion*, vol. 36, no. 2, pp. 1548-1561, June 2021, doi: 10.1109/TEC.2021.3058306.



VFCSS regions of operation



Inductor current envelopes for different VFCSS upper f_{sw} bounds

Effective Critical Soft-Switching requires:

- sufficient product of deadtime and inductor current
- correct inductor current direction

☑ **need to control the peaks and valleys of the inductor current ripple**

$$I_{L,p-p} = \frac{D(1-D)V_{DC}}{f_{sw}L_{sw}}$$

The peak to peak inductor ripple current is a product of duty cycle, the DC voltage, switching frequency, and inductance

The DC term of the inductor ripple current is a product of the load

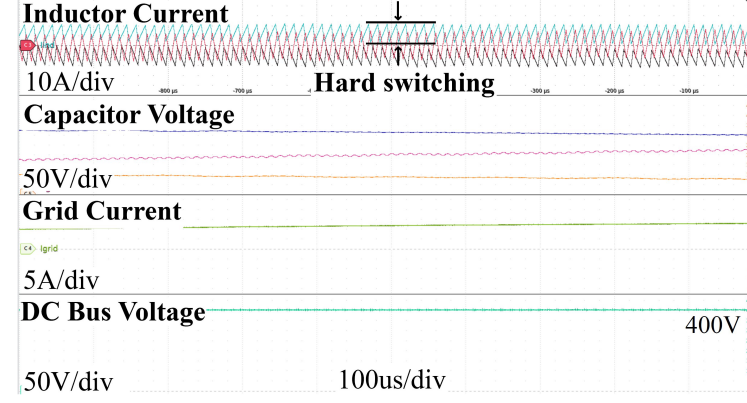
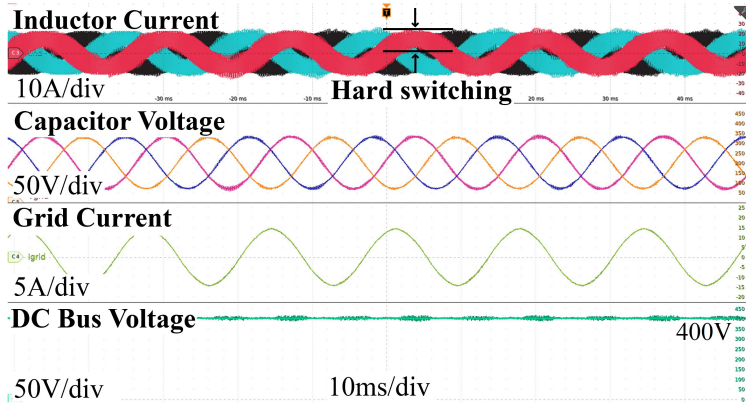
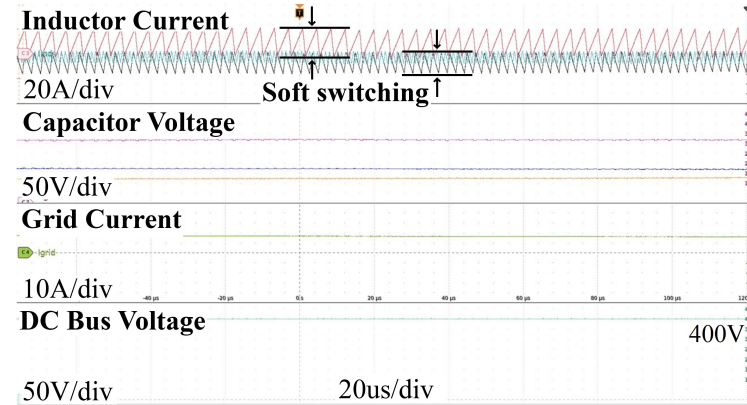
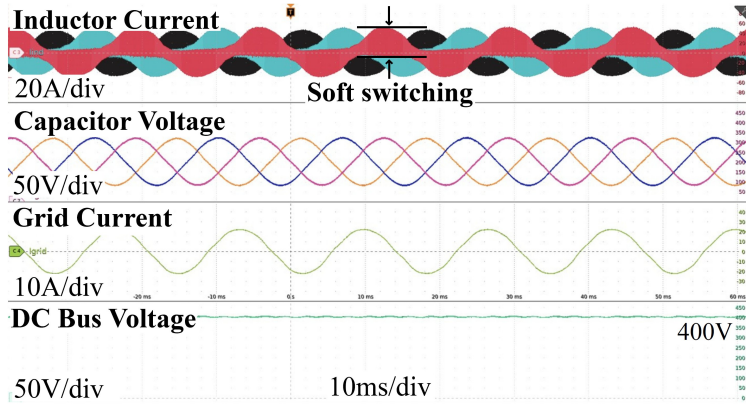
☑ **The switching frequency must be controlled to achieve a desired peak and valley points of the inductor ripple current**

☑ **Variable Frequency Critical Soft-Switching**

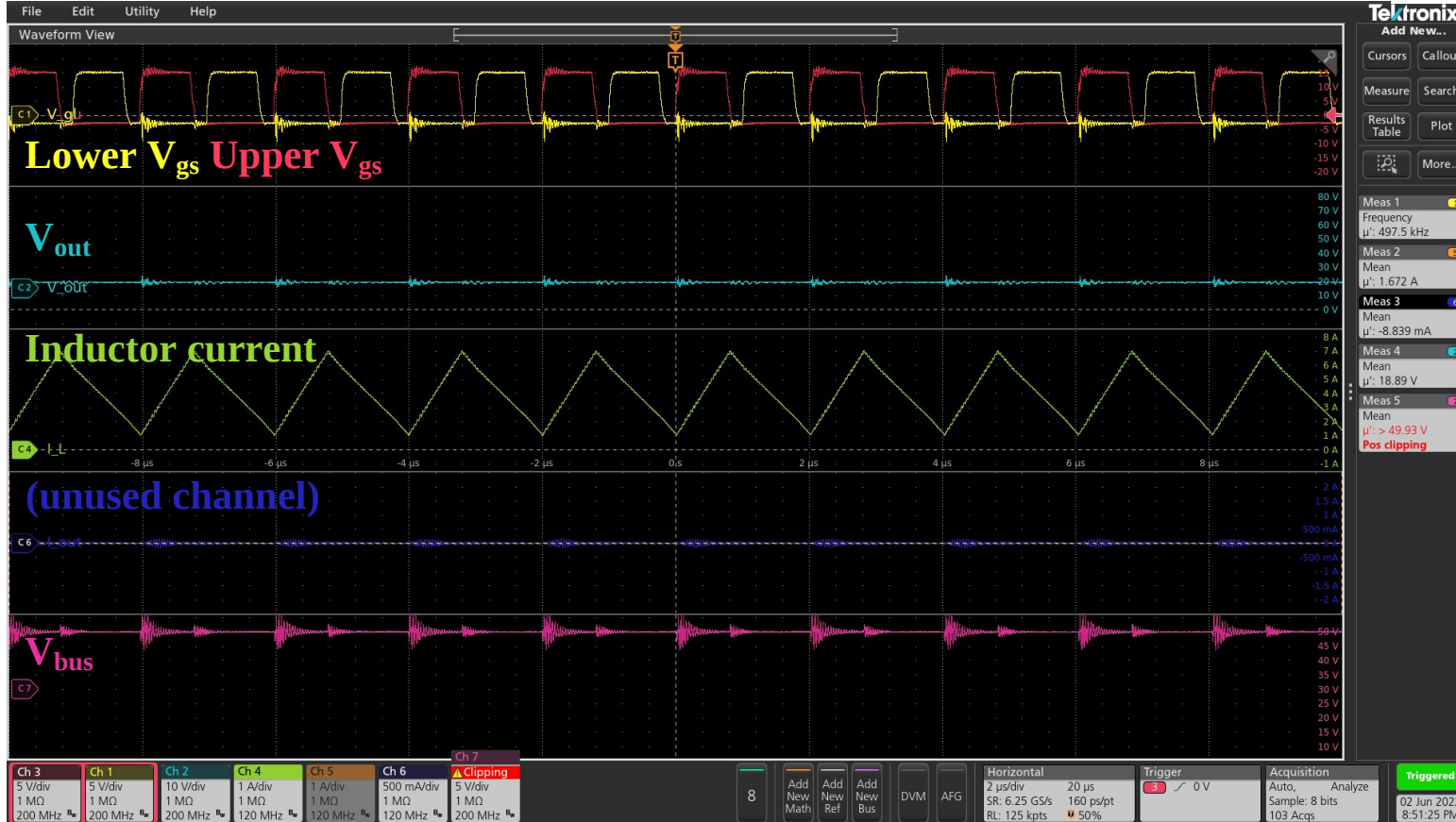
Effective VFCSS requires high inductor ripple current, necessitating a decrease in inductance

☑ allows for a simultaneous reduction in inductance (volume) and increase in efficiency

Variable Frequency Critical Soft-Switching (VFCSS)



EMI and Hard vs Soft-Switching

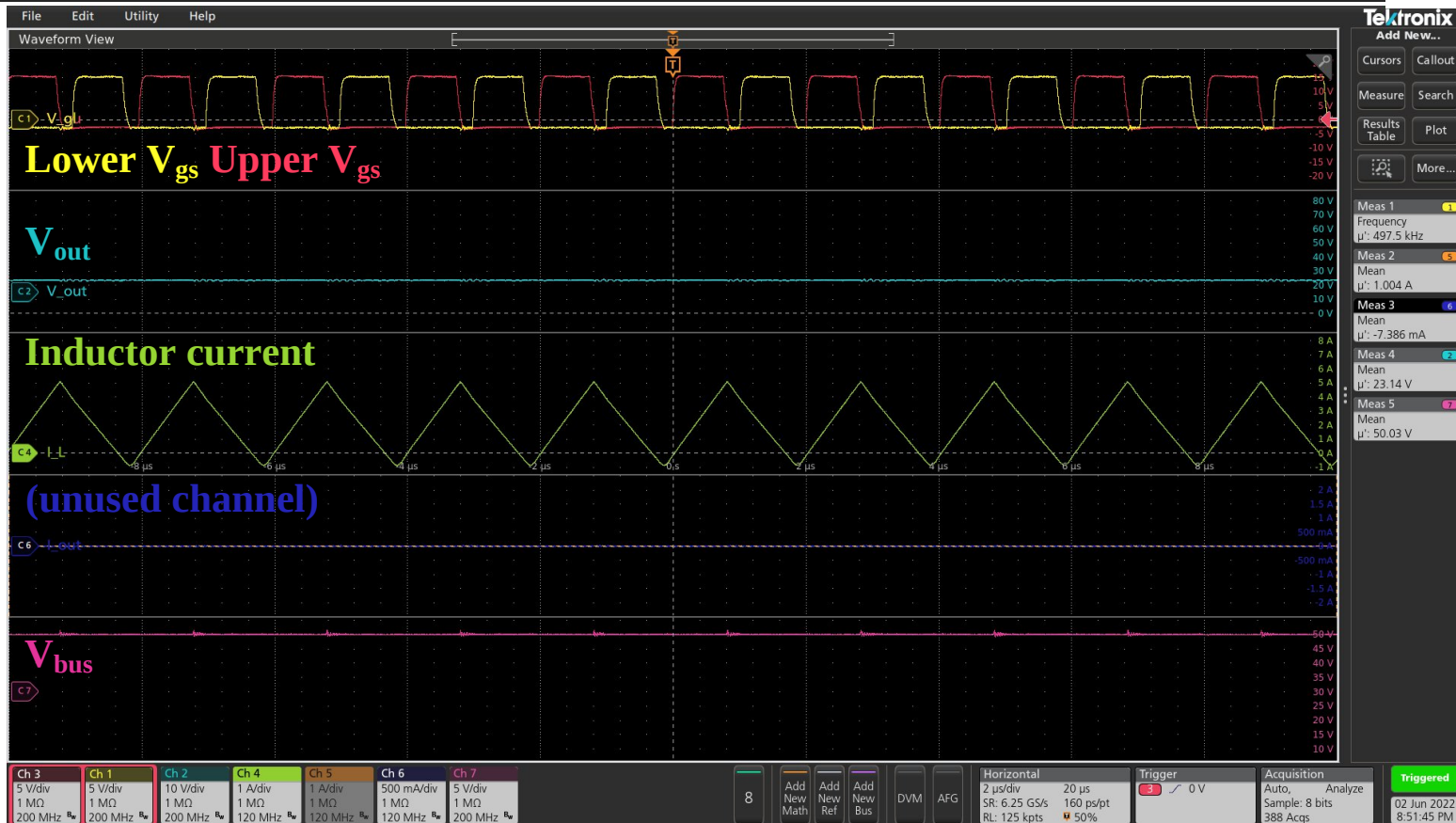


Hard-switching

- $f_{sw} = 500\text{kHz}$
- $D = 0.5$
- 4A load

(applying a step voltage to FET parasitic capacitances)

EMI and Hard vs Soft-Switching

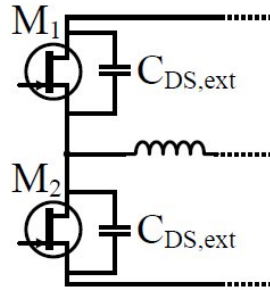


Soft-switching

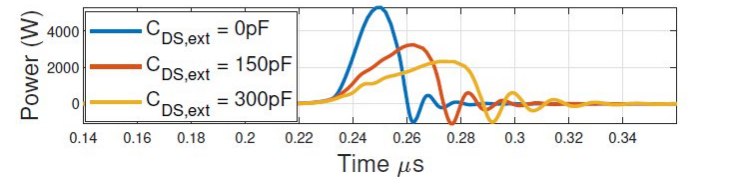
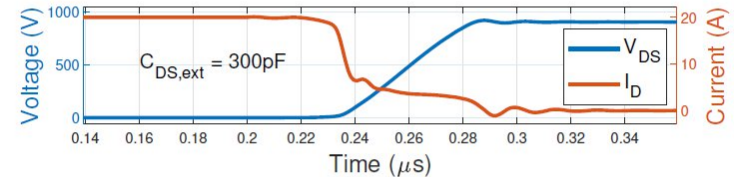
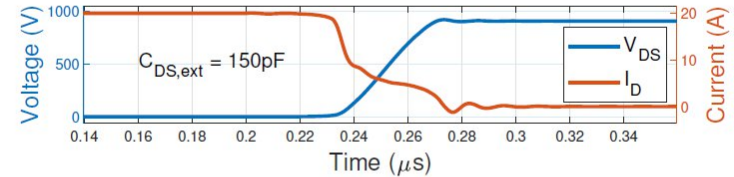
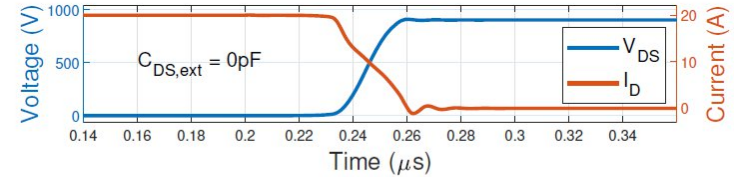
- $f_{sw} = 500\text{kHz}$
- $D = 0.5$
- 2A load

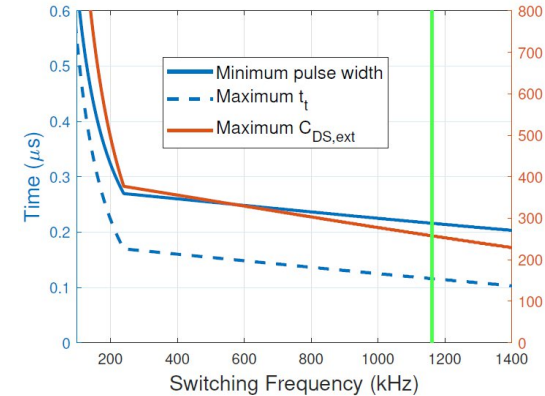
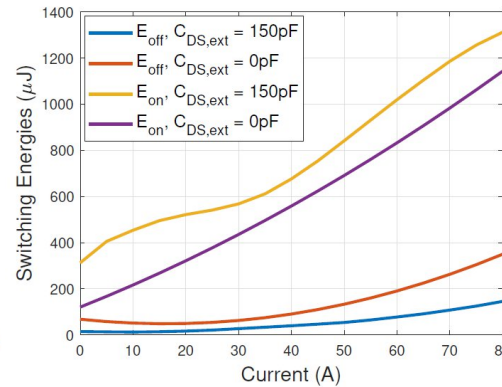
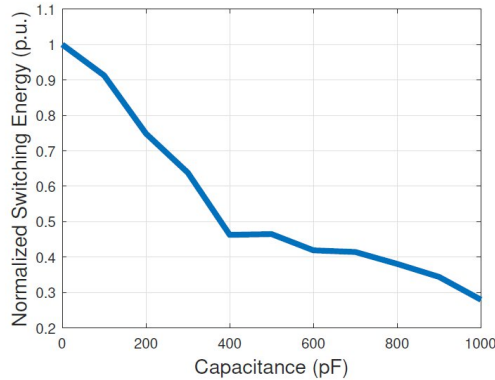
(not applying a step voltage to FET parasitic capacitances)

Additional C_{oss} Capacitance



- VFCSS incurs exclusively turn-off losses
- We can trade off turn-off switching energy with turn-on switching energy through additional Coss Capacitance
- This has the effect of slowing the switching transient time and reducing the V_{ds} I_d overlap



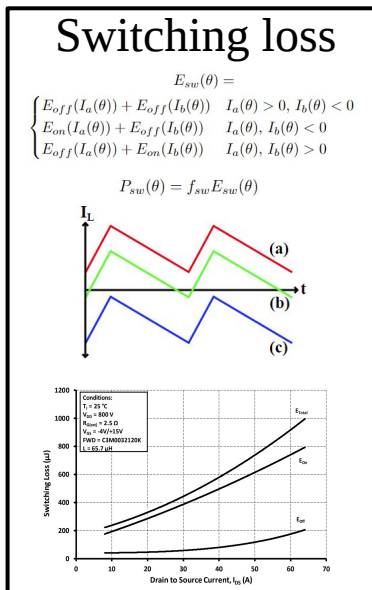


- The turn-off losses decrease with $C_{ds,ext}$
- The turn-on losses have a proportionally higher increase with $C_{ds,ext}$
 - turn-on losses can be disregarded as VFCSS incurs only turn-off losses
- Switching transient time increases with $C_{ds,ext}$, necessitating an optimization process to balance the two

Simultaneous Parameter Optimization for both Size and Efficiency

1) Develop a rigorous method for calculating loss as a function of circuit parameters

FET Loss



Conduction loss

$$P_{cond}(\theta) = R_{on} \left(I_{out}(\theta)^2 + \left(\frac{1}{2\sqrt{3}} I_{L,p-p}(\theta) \right)^2 \right)$$

Inductor Loss

Core loss

$$P_{core}(\theta) = k f_{sw}(\theta)^a B_{pk}(\theta)^b$$

$$= k f_{sw}(\theta)^a \left(\frac{4\pi N I_{pk}(\theta) 10^{-2}}{l_g + (l_m/\mu_r)} \right)^b$$

Winding loss

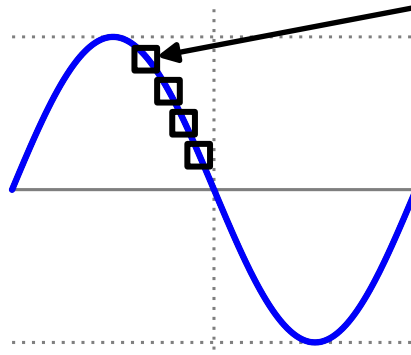
$$P_{Cu}(\theta) = R_{DC} I_{out}(\theta)^2 + R_{PWM}(\theta) \left(\frac{1}{2\sqrt{3}} I_{L,p-p}(\theta) \right)^2$$

Adjustable circuit parameters:

- switching frequency range, inductance, switching device, additional C_{oss} capacitance
- it is often the case where loss in one mechanism is traded off for loss in another mechanism
- therefore, it is necessary to vary all parameters simultaneously and pick the set of optimal parameters for the application

Parameter Optimization – Basic Efficiency Optimizatoin

- The operating point of an inverter changes with the phase of the output cycle
- ☑ the optimization must also take place over the entire cycle of the grid



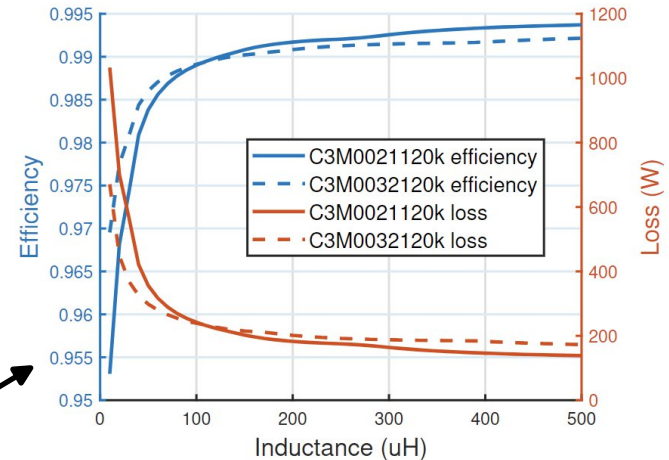
a) Loss at discrete points along the sine wave calculated for a given set of parameters



b) Set of parameters iterated, loss calculations repeated

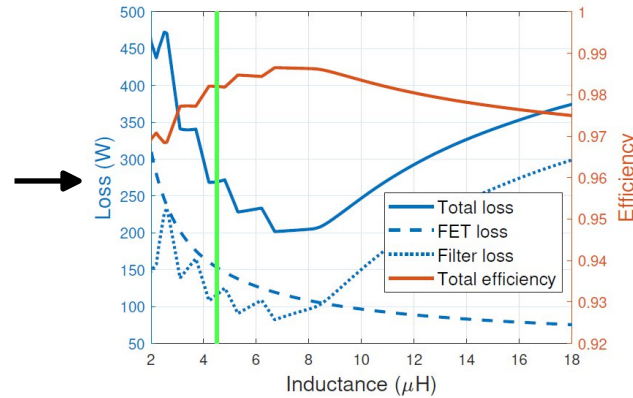
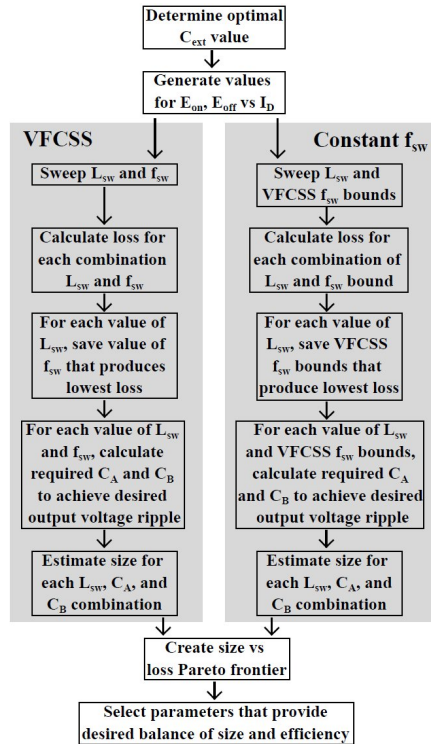


c) Parameters that produce the lowest loss are plotted against a controlled parameter

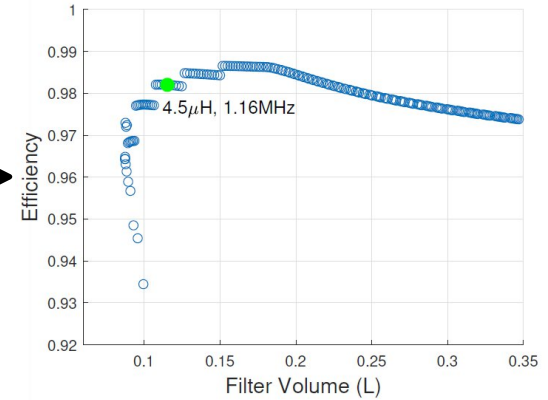


Theoretical maximum efficiency Pareto Frontier

Parameter Optimization – Advanced Efficiency and Size Optimization



Optimal loss values for a range of inductances



Pareto Frontier of volume and efficiency

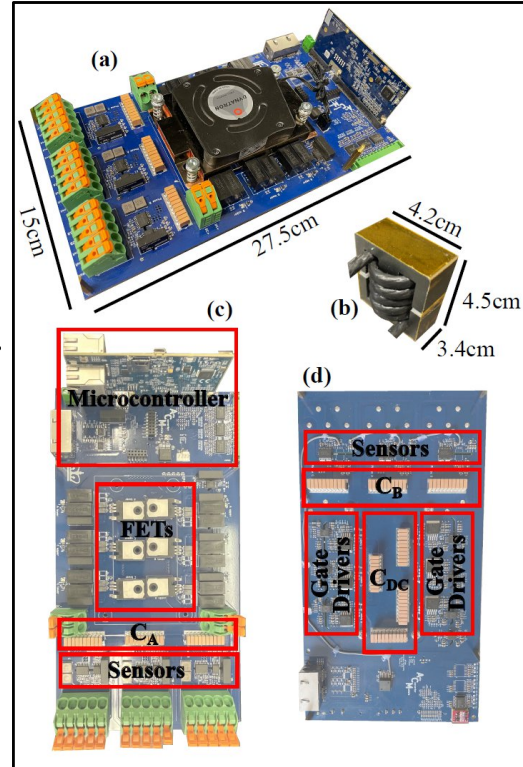
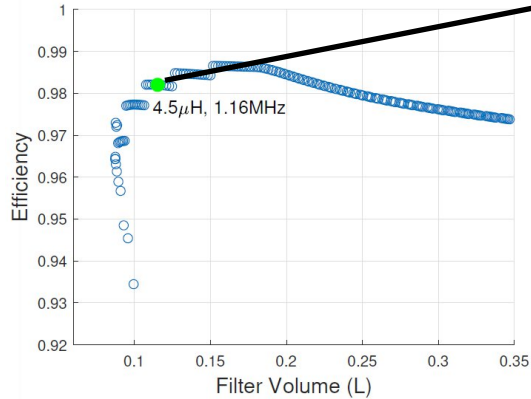
- At each set of parameters the filter volume is estimated
- plotting the filter volumes against the filter efficiencies results in a pareto front of volume vs efficiency

$$\frac{Y_L}{Y_L^*} = \left(\frac{E_L}{E_L^*} \right)^{\frac{3}{4}} = \left(\frac{0.5LI^2}{0.5L^*I^2} \right)^{\frac{3}{4}} = \left(\frac{L}{L^*} \right)^{\frac{3}{4}}$$

$$\frac{Y_C}{Y_C^*} = \left(\frac{E_C}{E_C^*} \right) = \left(\frac{0.5CV^2}{0.5C^*V^2} \right) = \left(\frac{C}{C^*} \right)$$

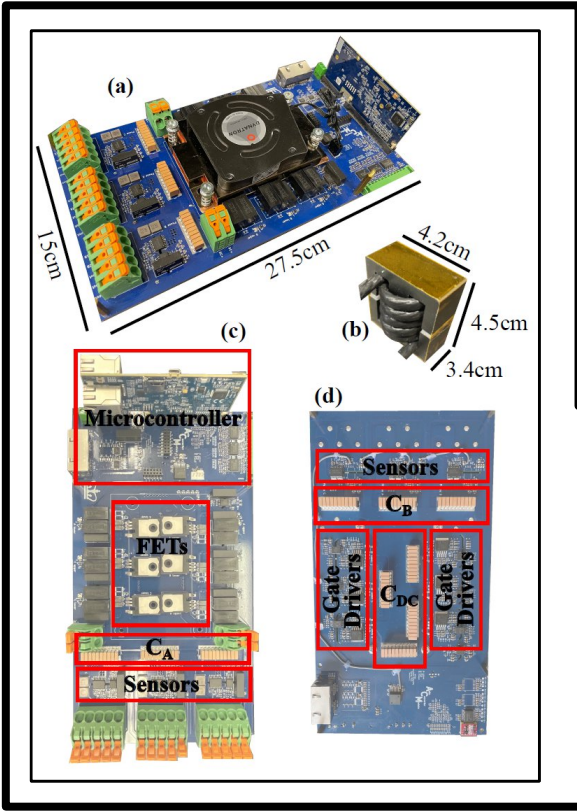
Prototypes

- A desired operating point is chosen and experimental apparatus constructed



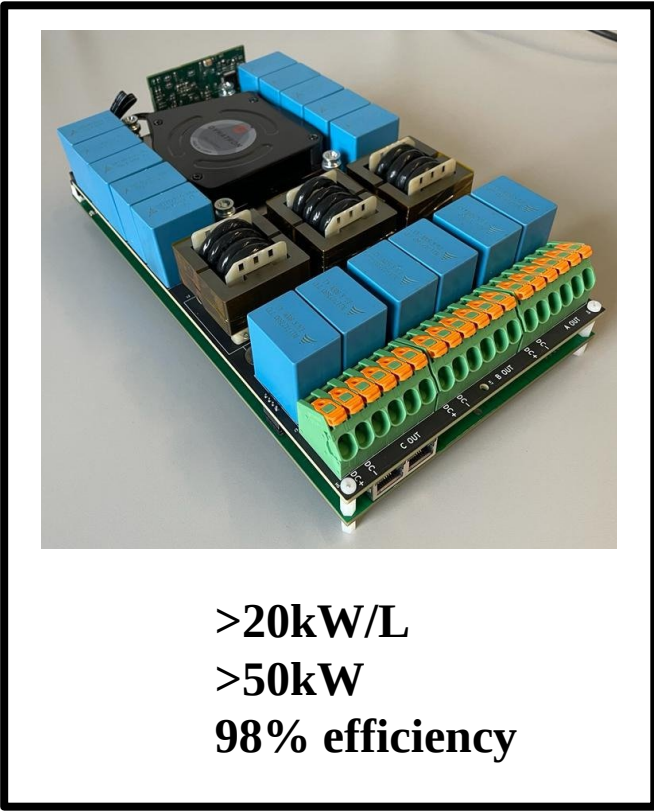
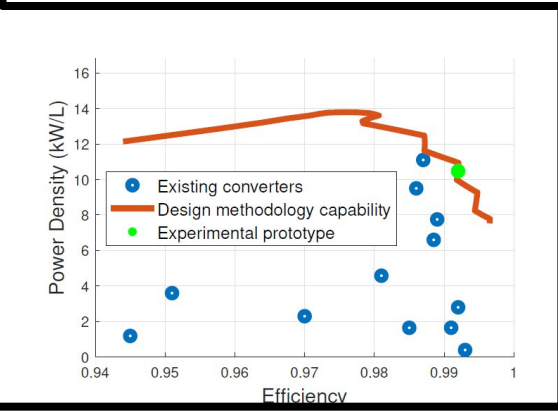
Optimized converter parameters:

- SiC CREE C3M0032120k
- $50\text{kHz} < f_{\text{sw}} < 1.16\text{MHz}$
- Inductance = $4.5\mu\text{H}$
- **99.2% efficient**
- **10.47kW/L**
- **15kW**



← **Current**

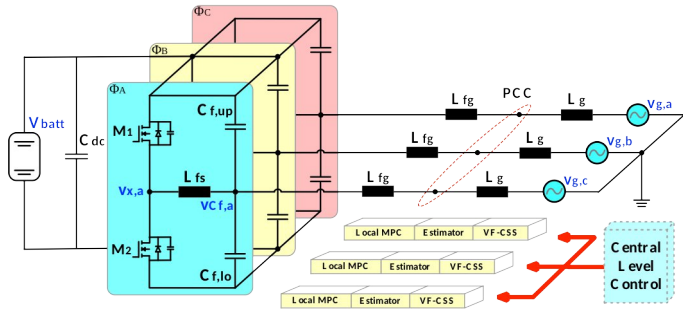
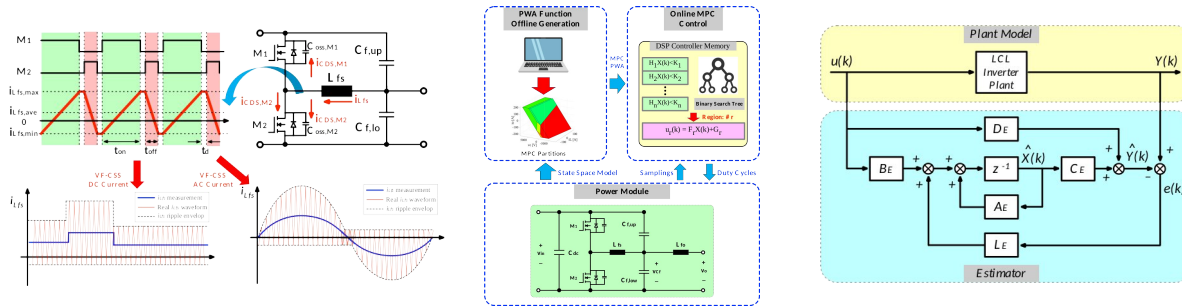
Future →



Design Case of Transformerless Converter

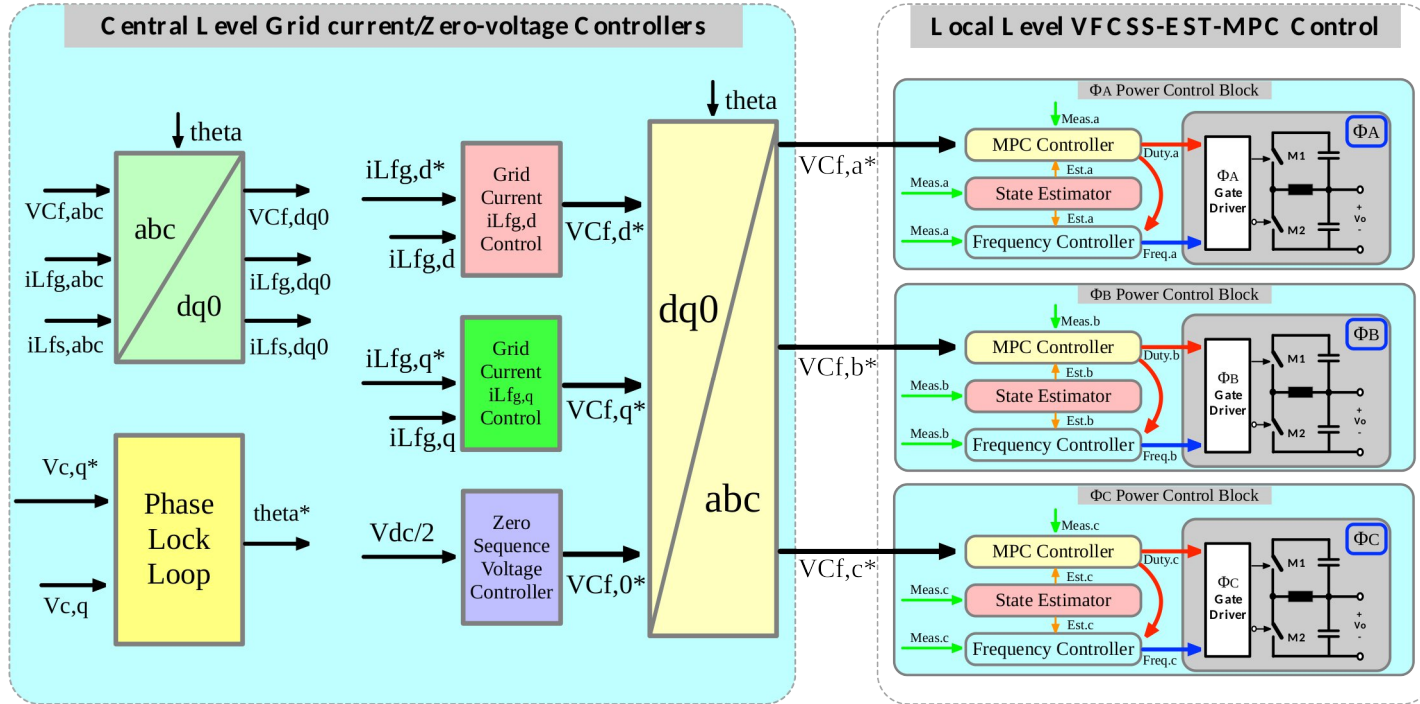
Liwei Zhou

Design Case of Three-Phase Grid-Tied Inverter Control

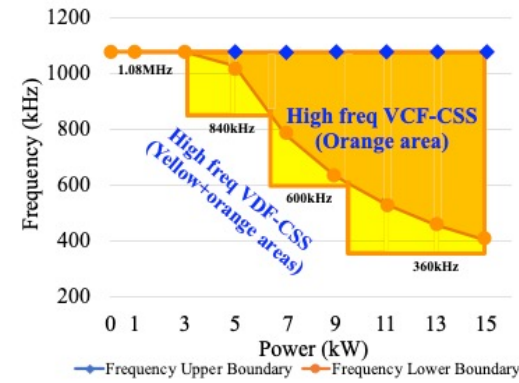
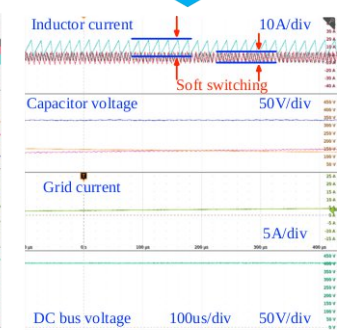
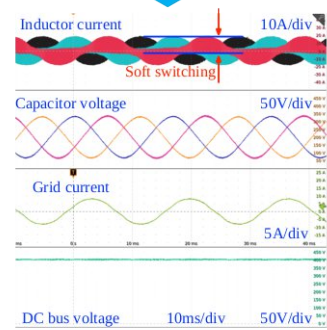
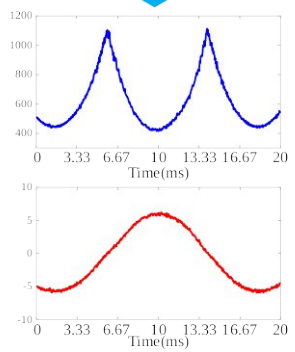
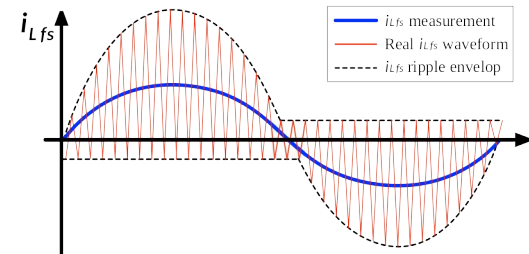
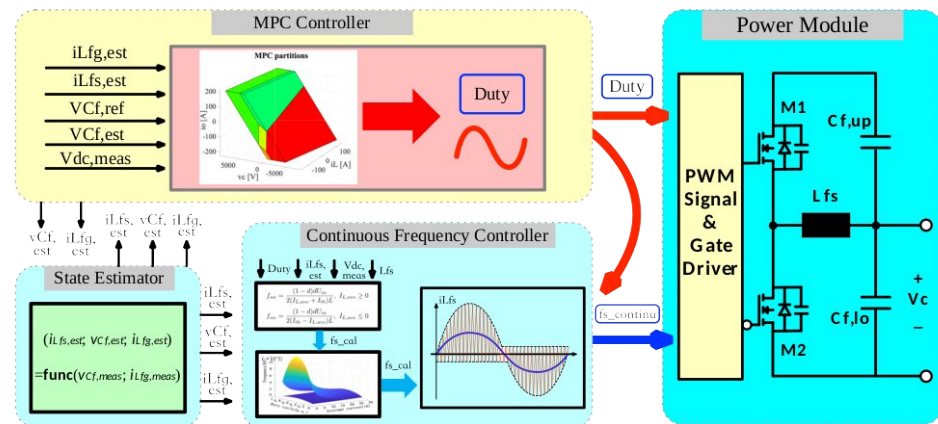


- **VF-CSS:** Variable-frequency critical-soft-switching to reduce the power losses and increase the power density.
- **Modular MPC:** Explicit MPC for per phase power module to improve the dynamic performance.
- **State Estimator:** Reduce the sensor cost and improve the anti-noise capability.

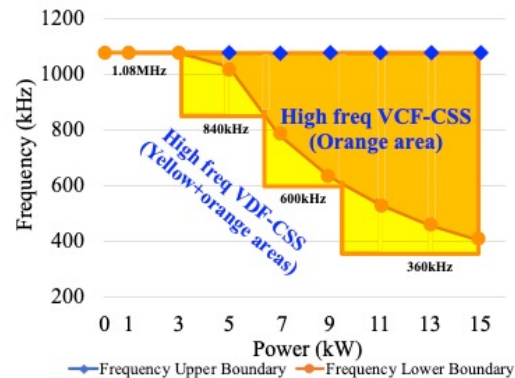
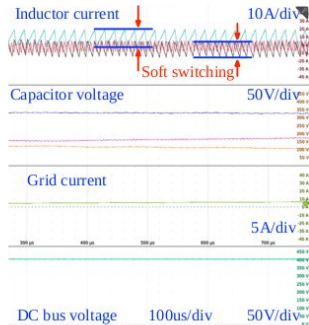
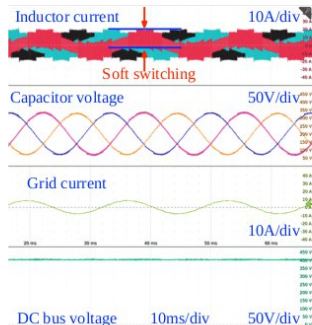
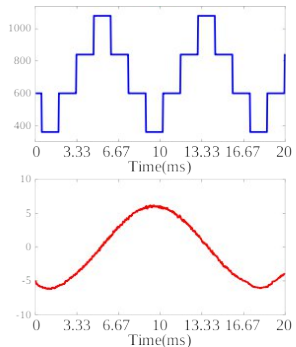
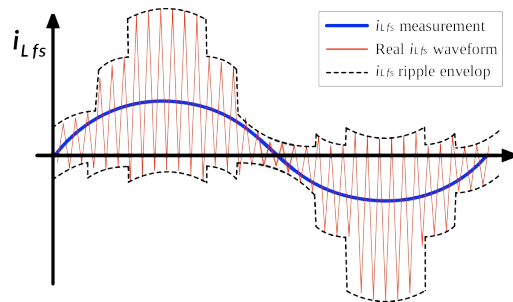
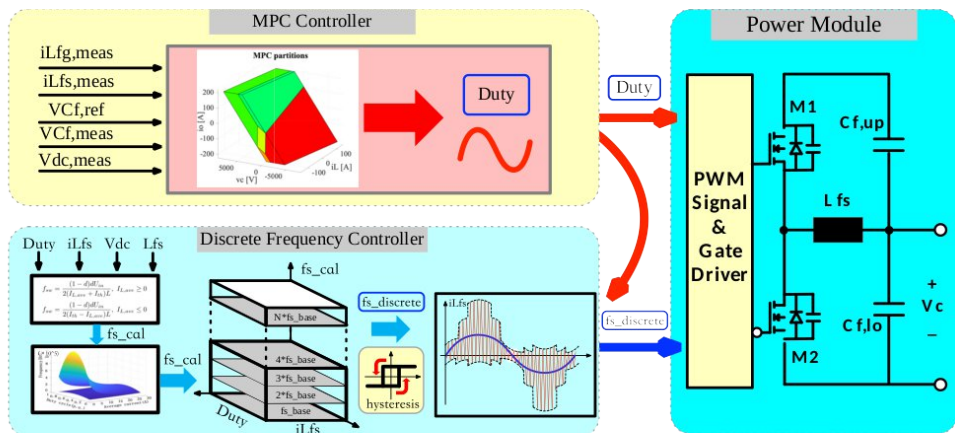
Holistic Control Diagram of Three-Phase Grid-Tied Inverter



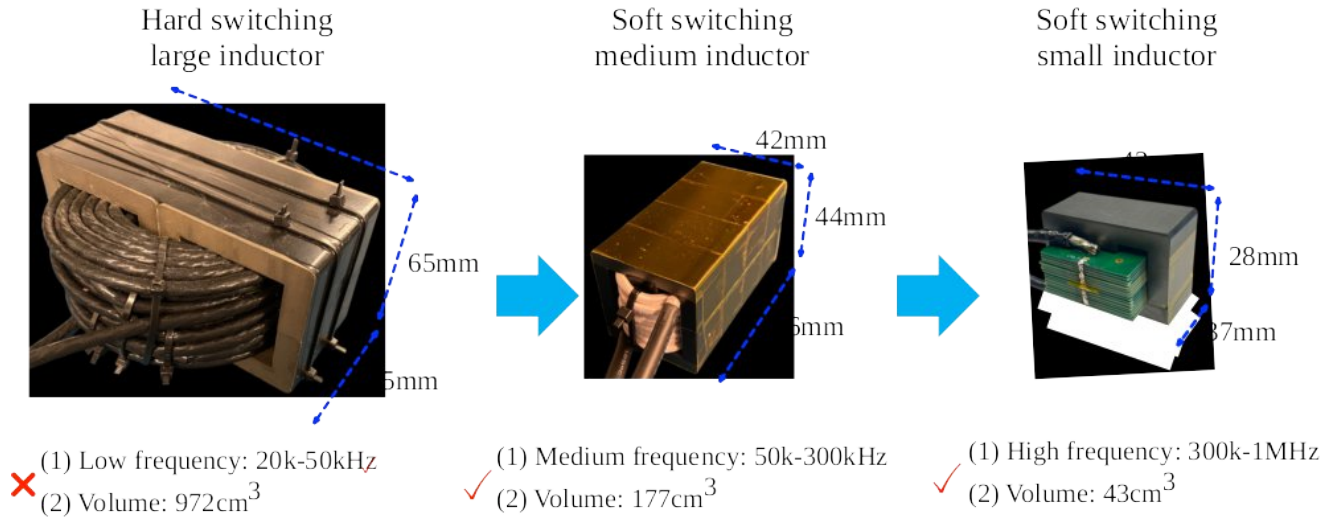
Variable-Continuous-Frequency Critical-Soft-Switching (VCF-CSS)



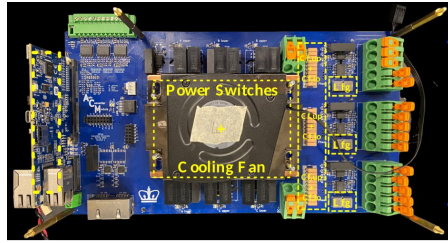
Variable-Discrete-Frequency Critical-Soft-Switching (VDF-CSS)



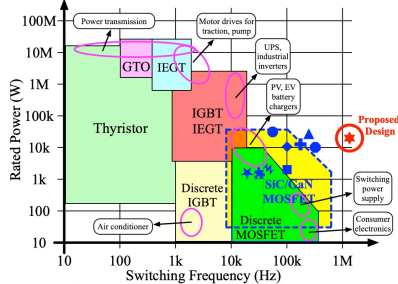
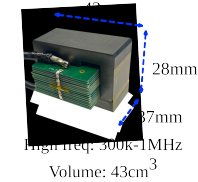
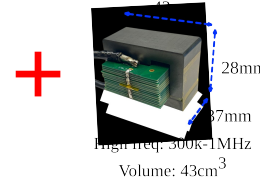
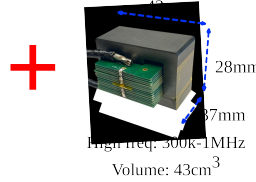
Volume Reduction and Frequency Increase of Inductor Due to VF-CSS



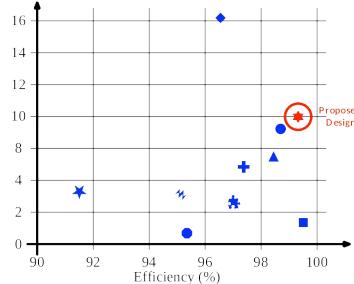
Merits of the Designed Three-Phase Grid-Tied Inverter



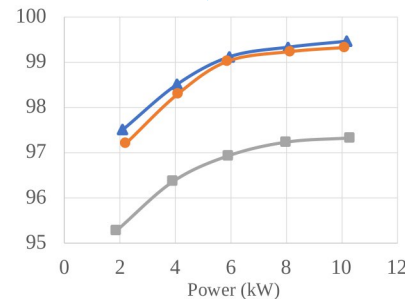
279mm
[1]



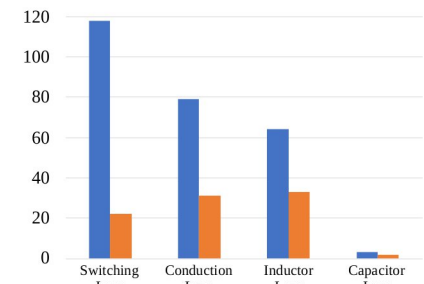
- ★ Proposed Design with SiC
- ◆ Ohio State University with GaN
- ETH with SiC
- ✦ Virginia Tech with SiC
- ✧ Concordia University
- ▲ Zhejiang University with SiC
- FAU with GaN
- DUT with SiC
- ✧ Kobe University
- ✧ York University



- ★ Proposed Design with SiC
- ◆ Ohio State University with GaN
- ETH with SiC
- ✦ Virginia Tech with SiC
- ✧ Concordia University
- ▲ Zhejiang University with SiC
- FSU with SiC
- DUT with SiC
- ✧ Kobe University
- ✧ York University



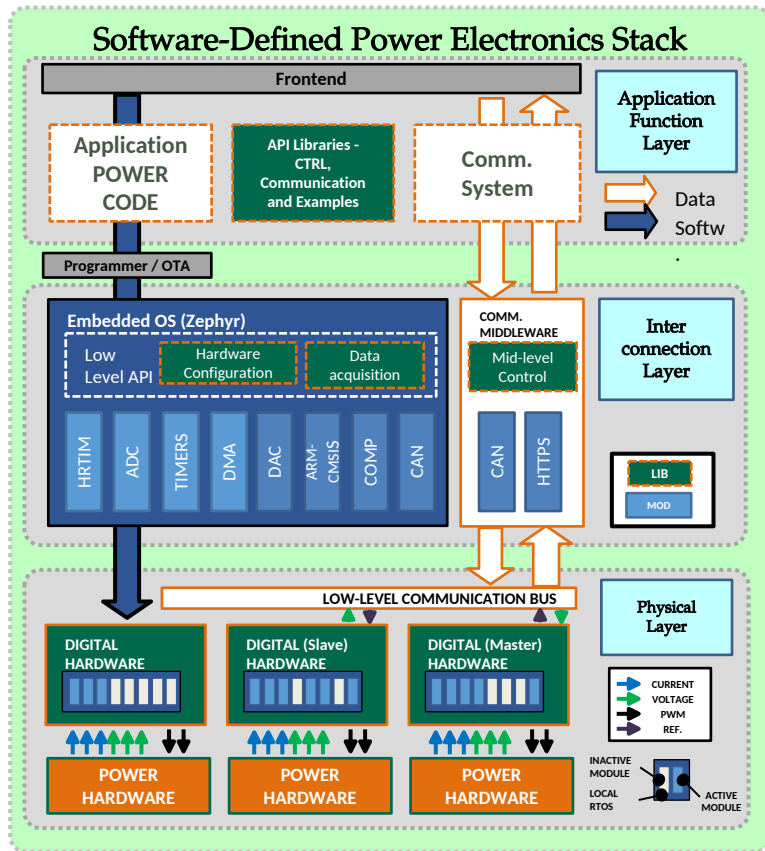
- ▲ VCF-CSS
- VDF-CSS
- Constant Freq



[1] Board designed by Matthew Jahnes

Zephyr-Based Implementation of Software Defined Power Electronics

Luiz Villa



- **Application Layer:**
 - A frontend for data visualization and firmware update
 - Libraries provide functions for power and data
- **Interconnection Layer:**
 - A programmer/over the air links the application to the Zephyr based system for code compiling and update
 - A communication middleware provides bi-directional data flow and mid-layer control
- **Physical Layer:**
 - Each module is composed of a digital and power hardware connected to a low-level communication bus
 - Multiple control schemes can be implemented: Decentralized, Mid-level or frontend based
- **Downlink and Uplink**
 - The downlink flashes onto the digital hardware
 - The uplink is done from a low-level bus to a communication system via a middleware

Software Defined Reprogrammable System Design

Objective

- Deduce the main constraints on the digital power hardware
- 3 main control schemes cover 90% of use cases

Voltage mode

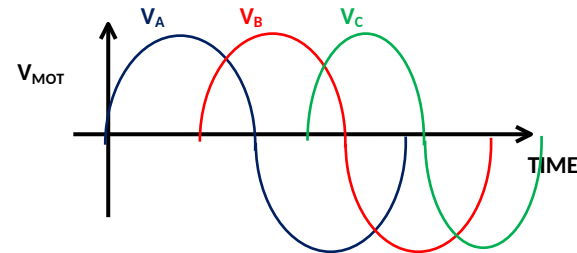
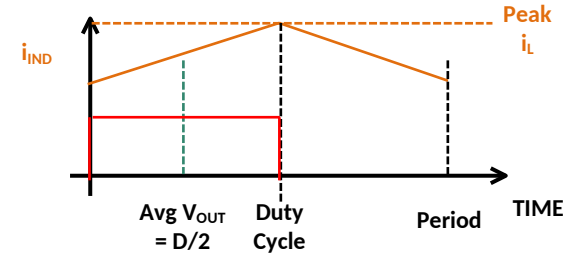
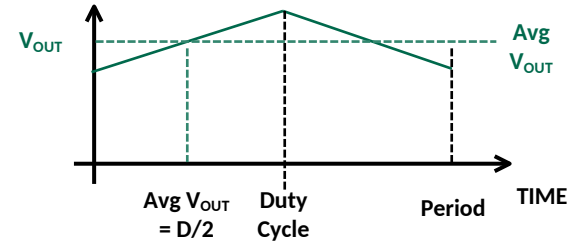
- Average measurements

Current Mode

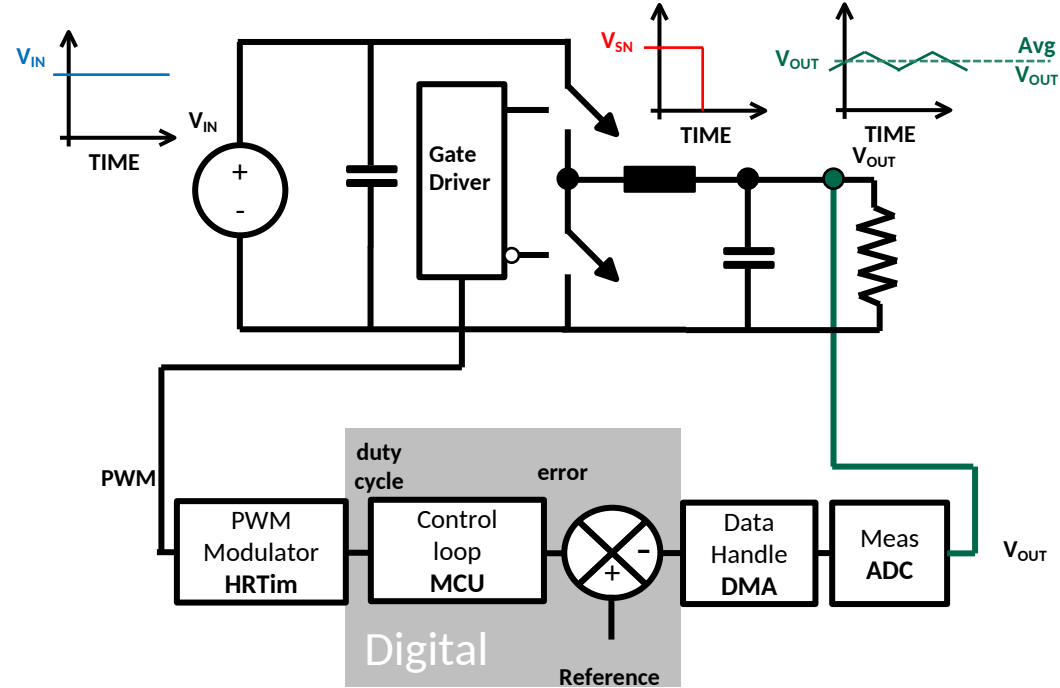
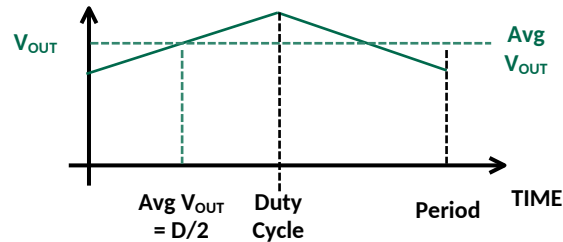
- Average and Peak Measurements

Voltage mode

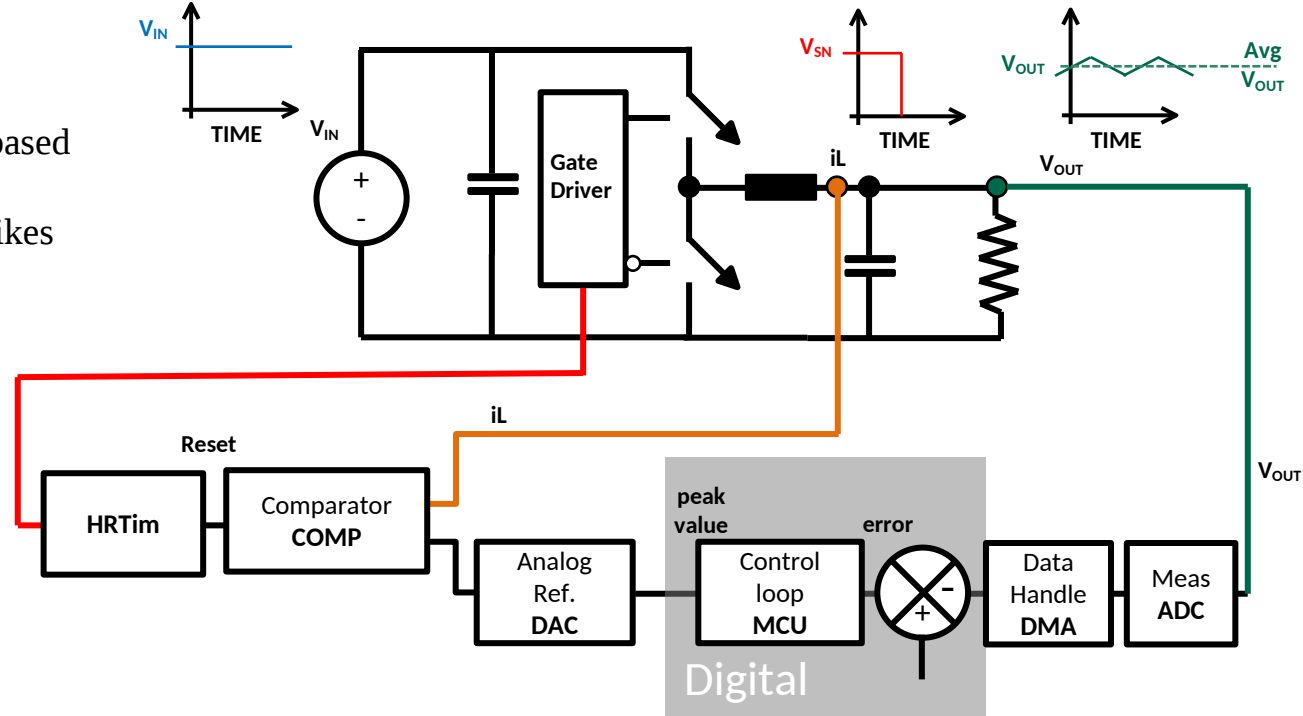
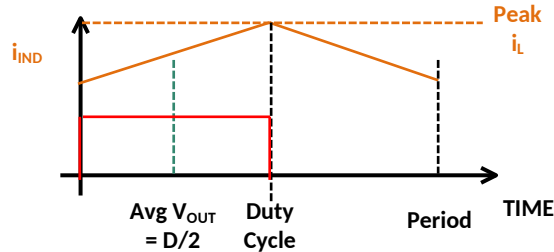
- Average and external measurements



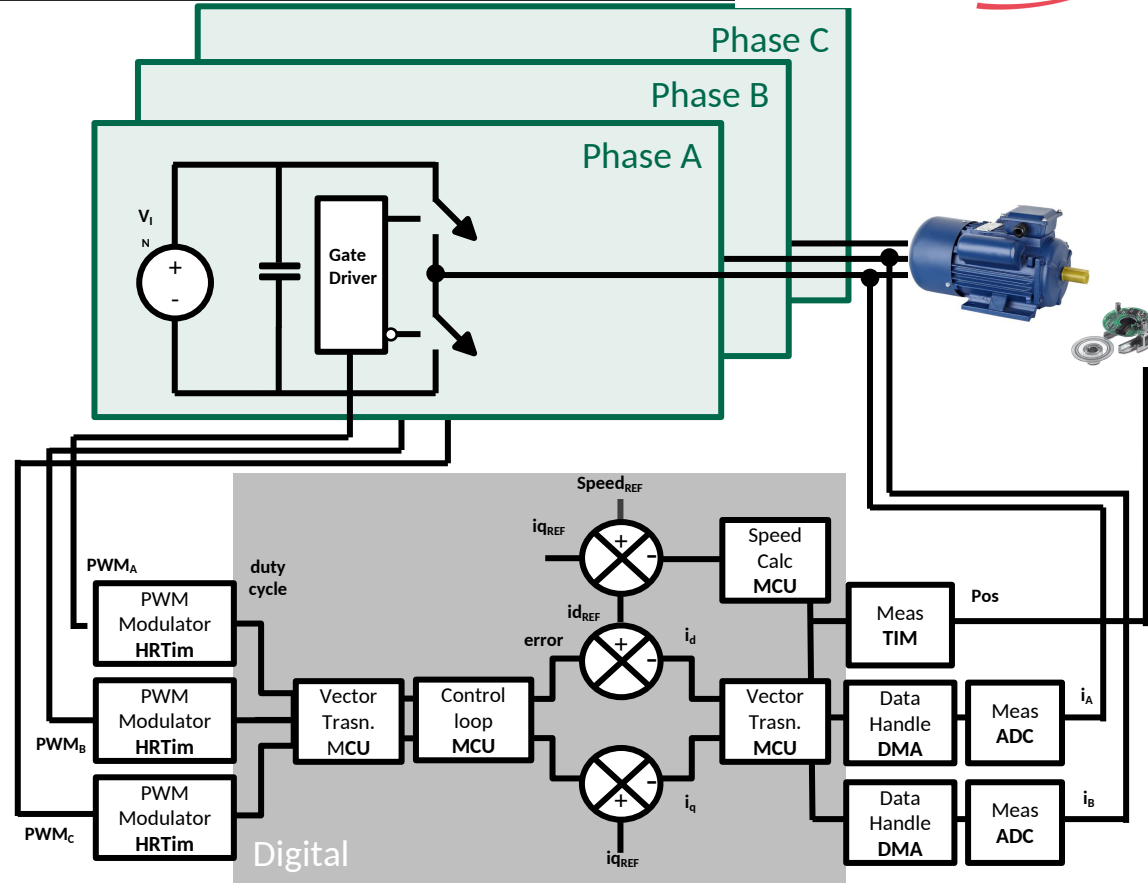
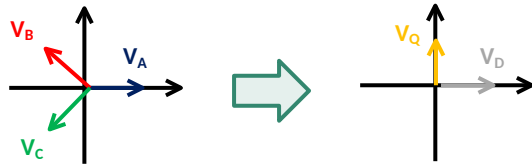
- Control of the duty cycle by the MCU
- Less Hardware intensive
- Average Measurement based control
- Can be done with non-specialized micro-controllers
- **Precision in the Measurement is necessary**



- Control of the duty cycle by a comparator
- Very hardware intensive
- Average and Peak Measurement based control
- Provides safety against current spikes and overloads
- **Requires a direct connection between the ADC, COMP and HRTIM**



- Control of the duty cycle by the MCU
- **Very calculation intensive**
- **Requires handling many measurements**
- Average control measurement based control
- Control bandwidth limited by the motor dynamics
- **It may require external measurements**



Critical real-time needs

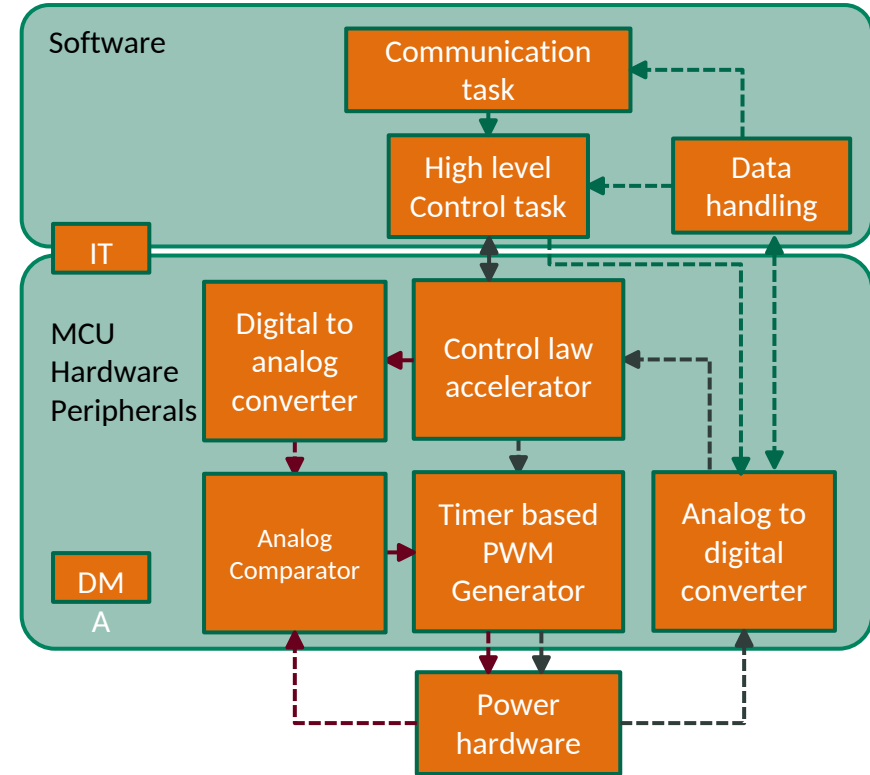
- Fast control tasks
- Fast acquisition
- Fast communication
- Very precise timers and PWMs

Peripheral needs

- Multiple triggers
- Multiple DMAs
- ADC and PWM synchronization
- **Dense and efficient Peripheral-to-Peripheral connection**

Communication Needs

- Fast low-layer communication for decentralized control/synchronization
- Slow high layer communication for hierarchical/centralized control



There are 2 constraints for controlling a power converter

- The maximum bandwidth of a converter is 1/10 of its switching frequency
- The minimum frequency of the control is x10 of the application bandwidth

Voltage Mode lies in between

- It is often associated with higher-order safety features for peak current

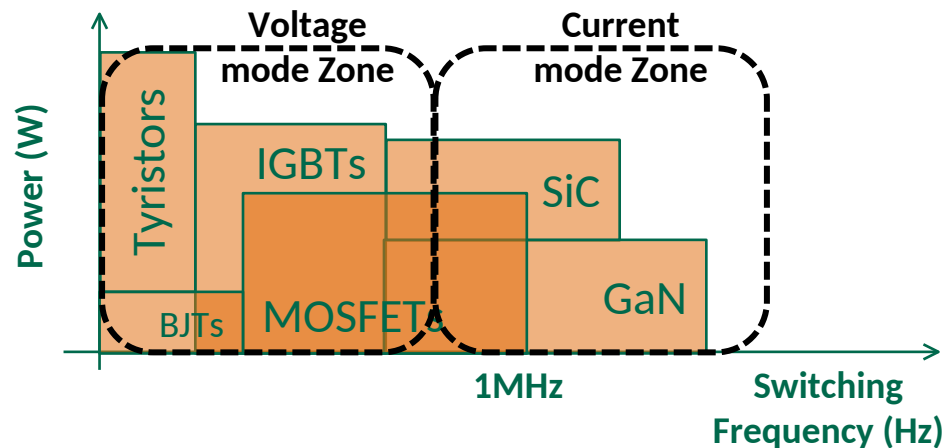
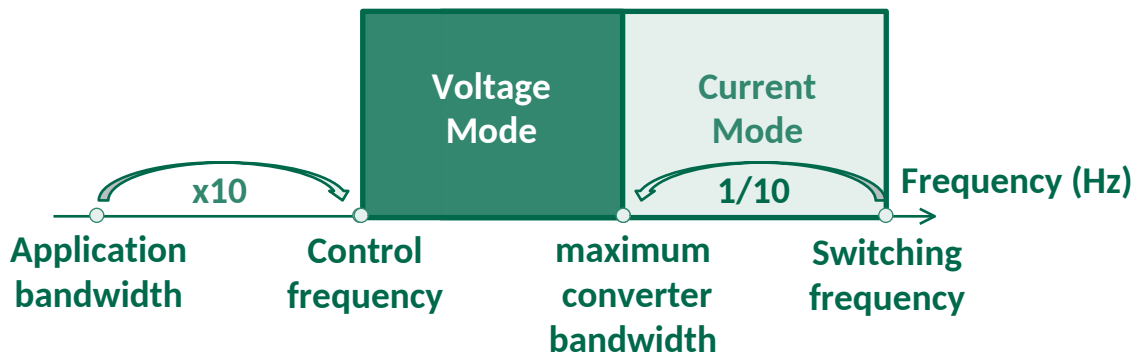
Current Mode requires hardware acceleration

Sensor Bandwidth

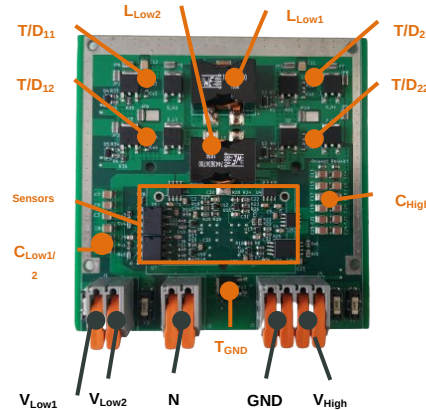
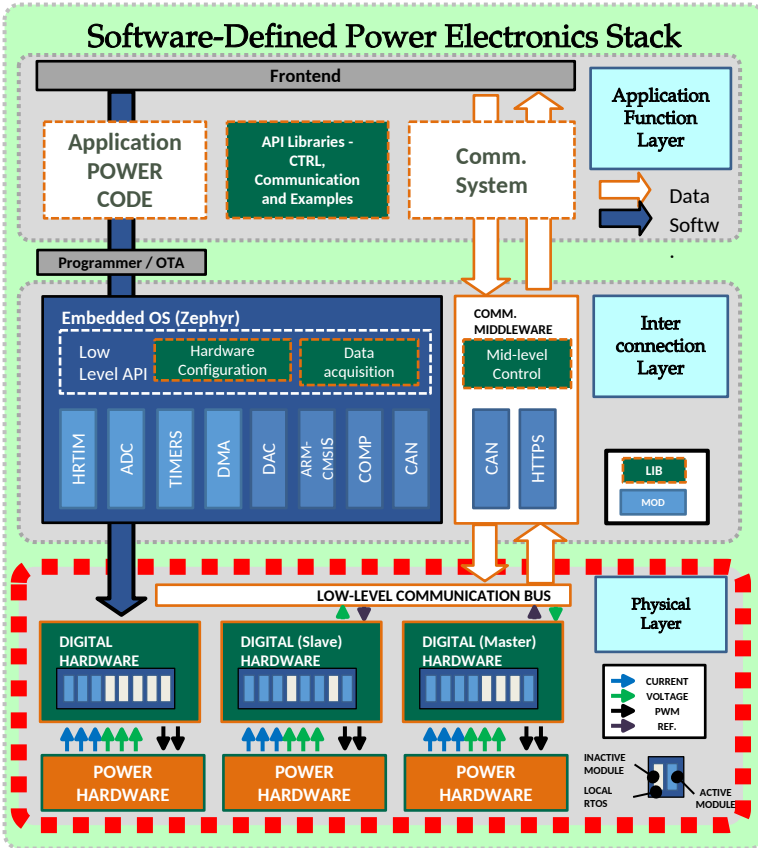
- Voltage sensor = 10 x Application bandwidth
- Current sensor = 10 x switching frequency

Number of Switching legs is a complexity factor

Switch Technology is linked with the choice of the Power SoC

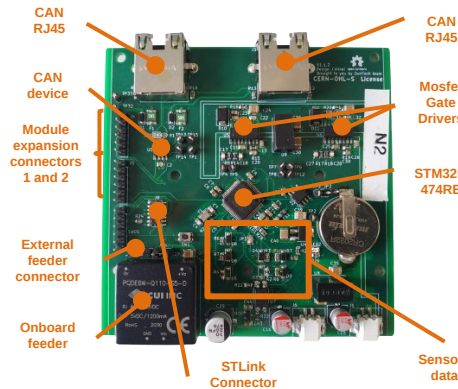


Software Defined Power Hardware Design



Power Hardware Design

- Hardware constraints and the iso-power curve theory
- The choice of the number of legs
- The developed solution

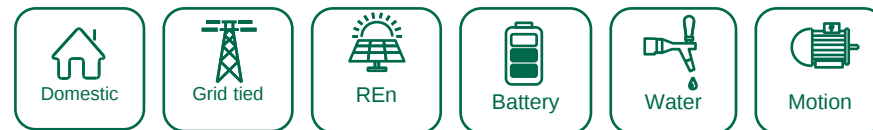


Digital Module Design

- The implications of different control techniques on the digital SoC
- Digital hardware constraints and the digital control bandwidth theory
- The developed solution

Reprogrammable functions

- From application to conversion level
- Current bi-directional
- DC and AC Capabilities



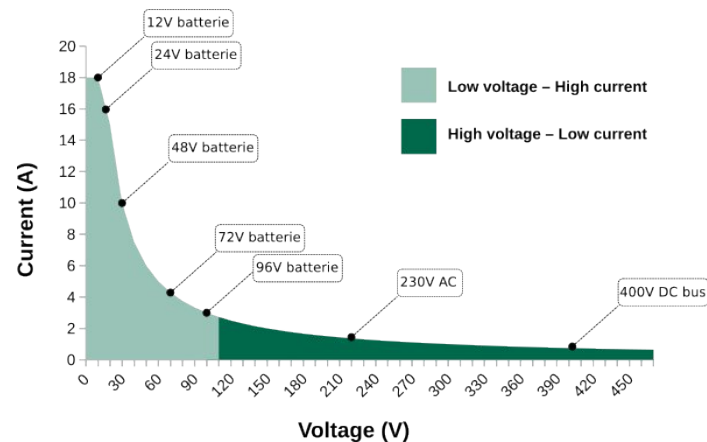
Standard and Stackable Hardware

- Isolated digital board
- High Frequency for smaller modules
- Ergonomics is a key issue

Iso-Power Curve Theory

- Low voltage and high current side
- High Voltage and low current side

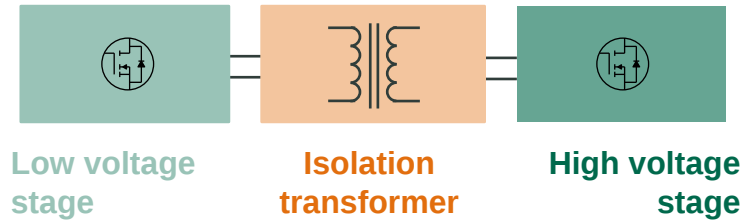
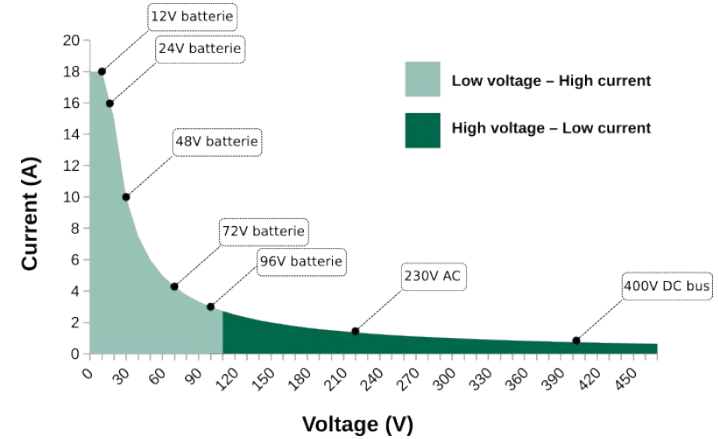
300W Iso power locus



Splitting the locus into two

- Requires creating an isolation barrier
- Requires taking into account DC buses on both sides
- Requires deciding how to size the LV and HV modules in terms of voltage, power, cost, conversion function, flexibility and complexity
- The sizing of the isolation transformer is also a key factor on the overall system

300W Iso power locus





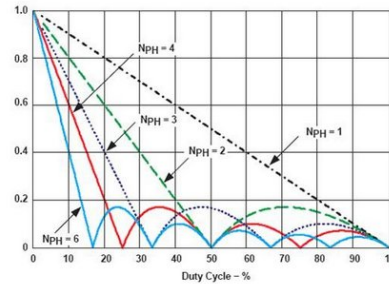
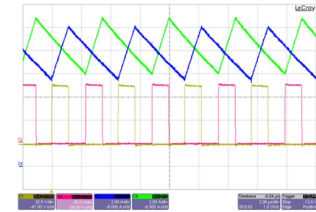
Handling uncertainty in the specifications

- Power modules are designed for a restricted number of operation points
- A broader range of operation points requires finding a technique to ease the stress on the input/output filters
- Interleaving is the technique used by us to reach this goal
- But what is the right number of legs?
- What are the trade-offs that interleaving introduces?

Low voltage stage

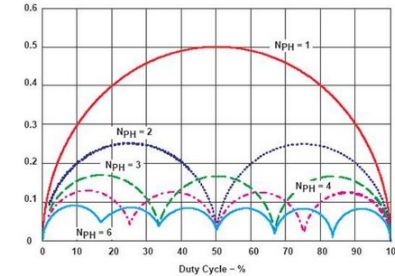
Isolation transformer

High voltage stage



Low side capacitor normalized current stress mode (2)

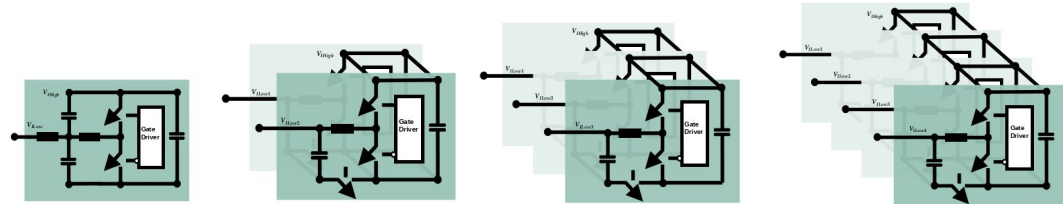
Two-leg synchronous buck interleaving (1)



High side capacitor normalized current stress buck mode (2)

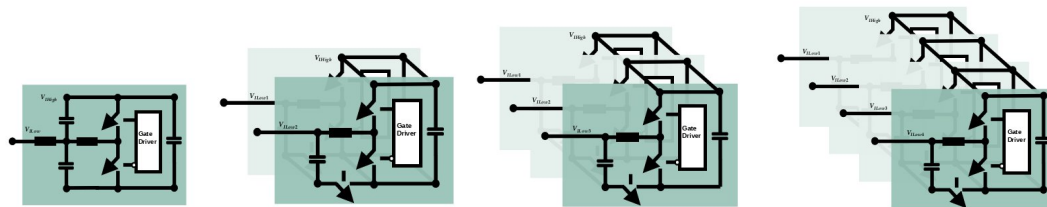
(1) [How to design a simple two-phase current sharing synchronous buck regulator](#)

(2) [Power Tips: When to choose multiphase](#)



Looking at the possibilities

- Cases : 1 to 4 legs
- Evaluation: module level



#L	Digital power feasibility			Control complexity		Topological merits			Hardware complexity		Topological flexibility			Module score
	Digital Power Soc	Hwd Ctrl V mode	Hwd Ctrl Curr mode	Mod. Sync	Neutral Ctrl	Isolat. Mod	Interleaving	Curr. balanc.	# sensors	# drivers	# mod 1AC	# mod 3AC	Leg Usage	
1	++	++	++	-	+	DAHB	--	++	4 (++)	1 (++)	2 (-)	3 (-)	++	8
2	+	+	+	+	+	DAB	+	-	6 (+)	2 (+)	1(++)	3(-)	++	9
3	+	+	-	++	-	n/a	++	-	8 (-)	3 (-)	1(++)	1(++)	-	3
4	-	-	-	++	++	DAB	++	-	10 (-)	4 (-)	1(++)	1(++)	+	3

Modulation is key to AC

- Different modulation techniques have different impacts on the bus sizing
- There is a trade off between system complexity and bus voltage level

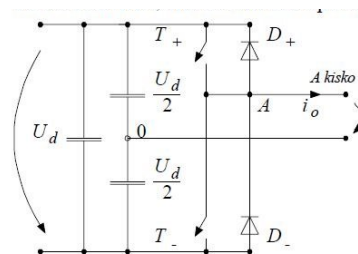


Figure 1. Half-bridge inverter.

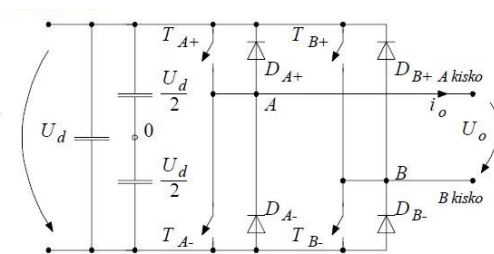


Figure 2. Full bridge inverter.

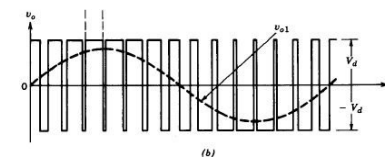
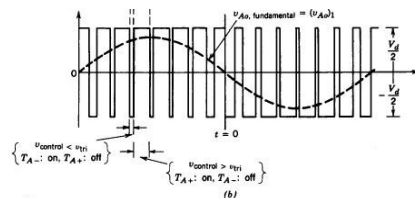
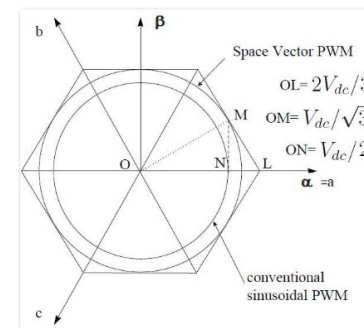
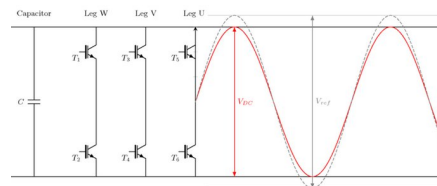
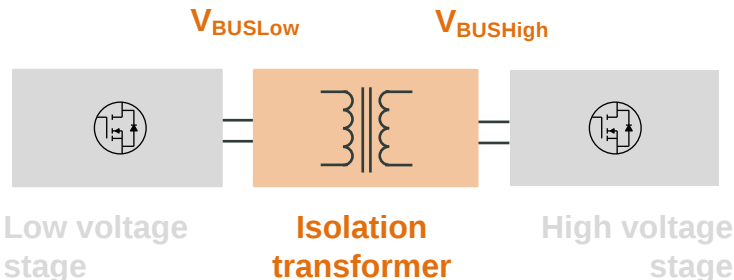
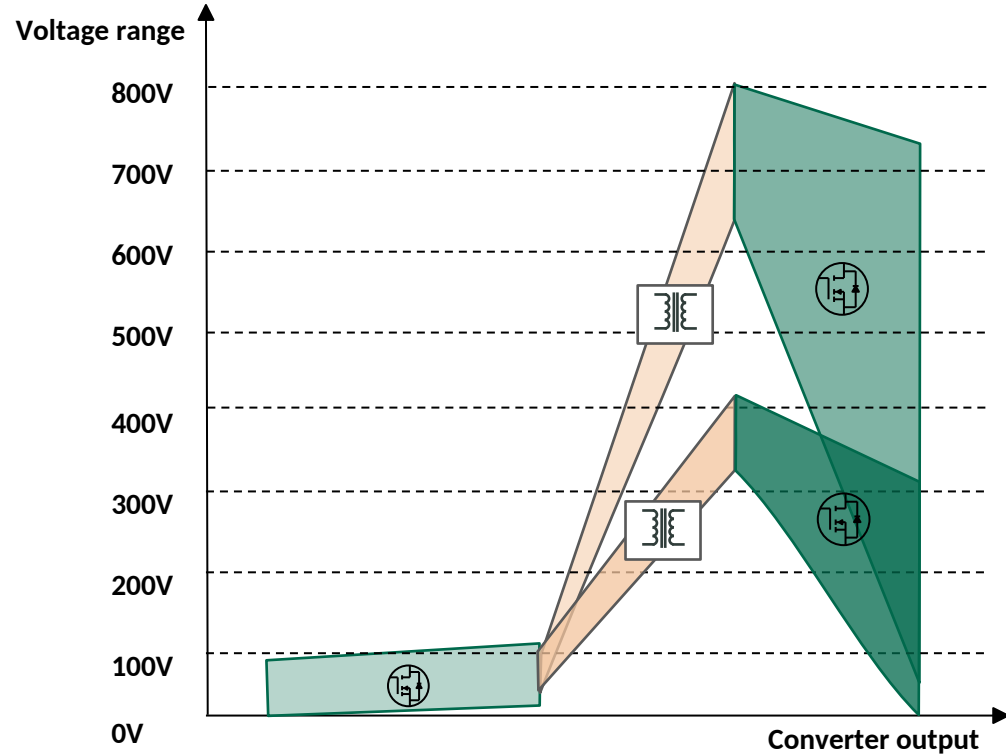
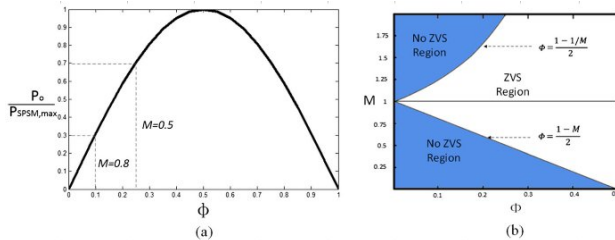


Figure 8-12 PWM with bipolar voltage switching.



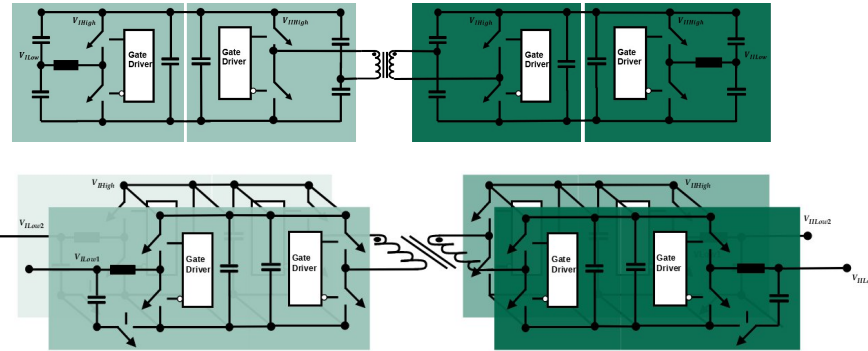
Going up and coming back down

- Three phase topology are theoretically covering all the possible functions
- A three phase three leg AC inverter requires a V_{PEAK} fo around 730V, meaning MOSFETs of 1200V lowering the efficiency of the high stage
- The isolation transformer is operated by a DAB or DAHB
- It must operate as closely as possible to its natural winding ratio.

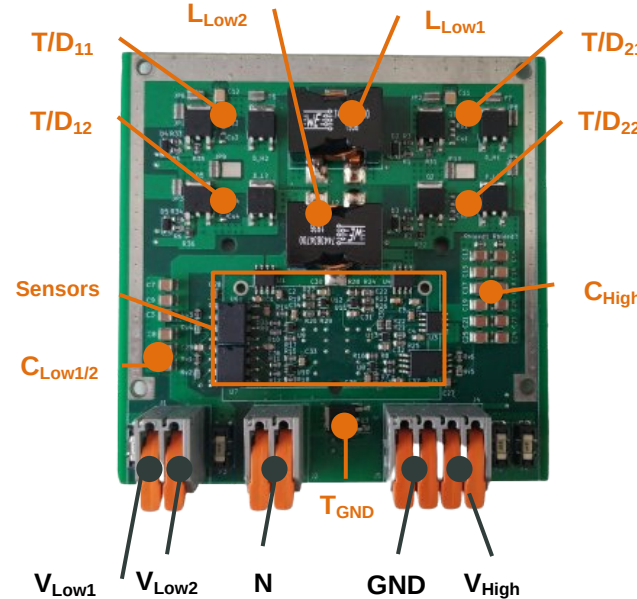
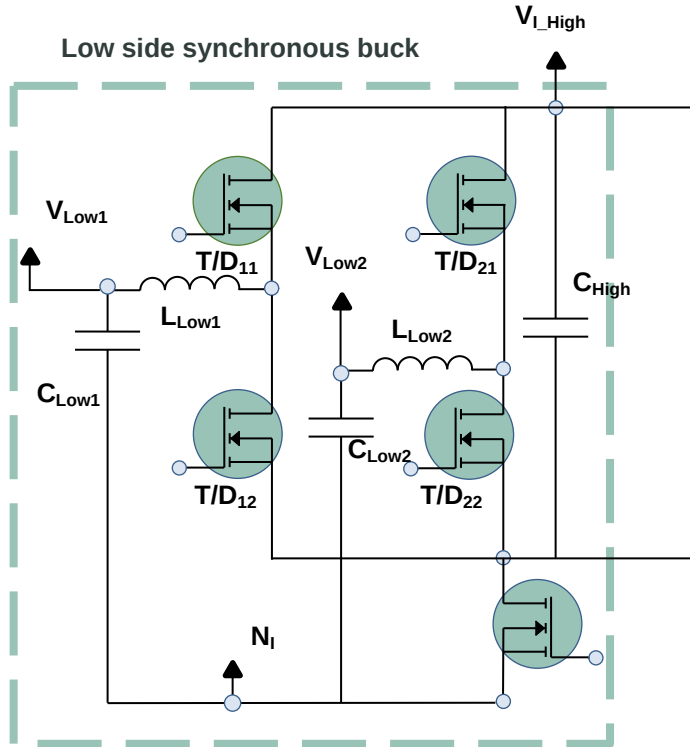


On the assembly level

- Cases : 1 to 4 legs
- Evaluation: assembly level



# Legs	Relaxing Hw constraints		Flexibility				Mix & match score
	High Side Voltage stress reduction	Transformer ratio	#modules for 1AC	#modules for 3AC	#modules for isopower / stress reduction	Unused leg in 1AC	
1+DAHB+1	+	+	4 (+)	5 (-)	18 (- -)	0 (++)	2
2+DAB+2	++	+	3 (++)	4 (+)	9 (-)	1 (- -)	3
3+DAB+3	--	-	3 (++)	3 (++)	3 (++)	1 (- -)	1
4+DAB+4	--	-	3 (++)	3 (++)	3 (++)	0 (++)	5



AT A GLANCE

Rated Power

300W per module

Number of channels

Dual low side

Single high side

Current ratings

8A per channel

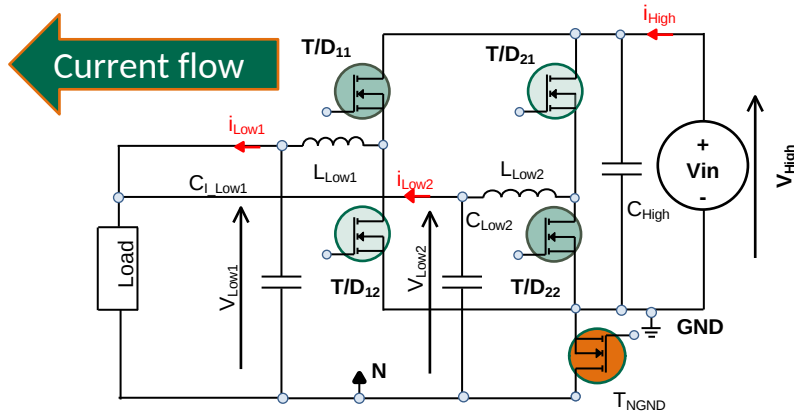
16A in parallel

Voltage ratings

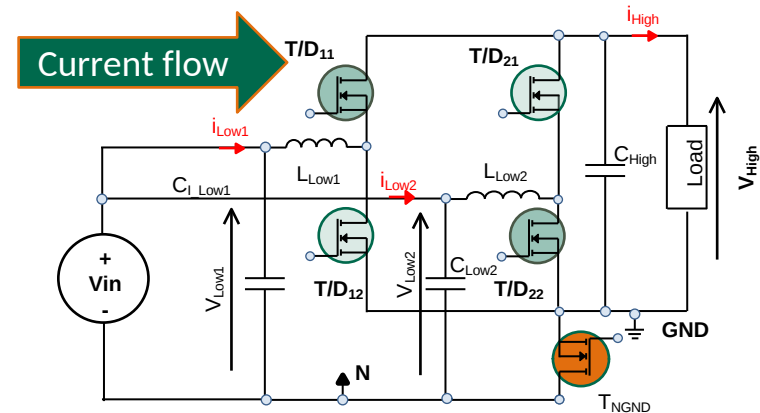
12V to 72V low side

40V to 100V high side

5 switches dual synchronous buck - DC-DC Interleaved Operation

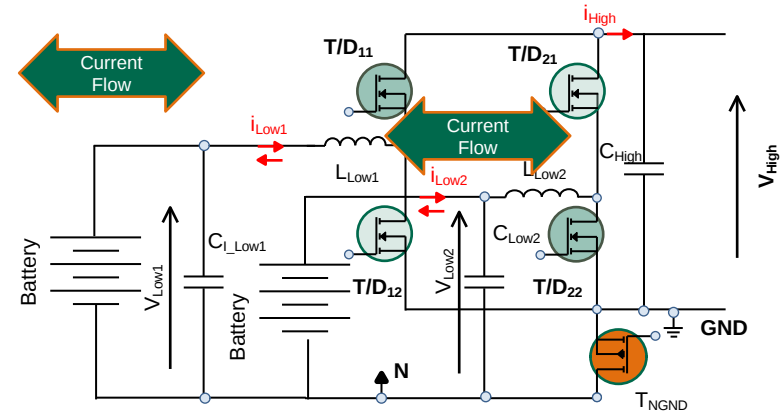
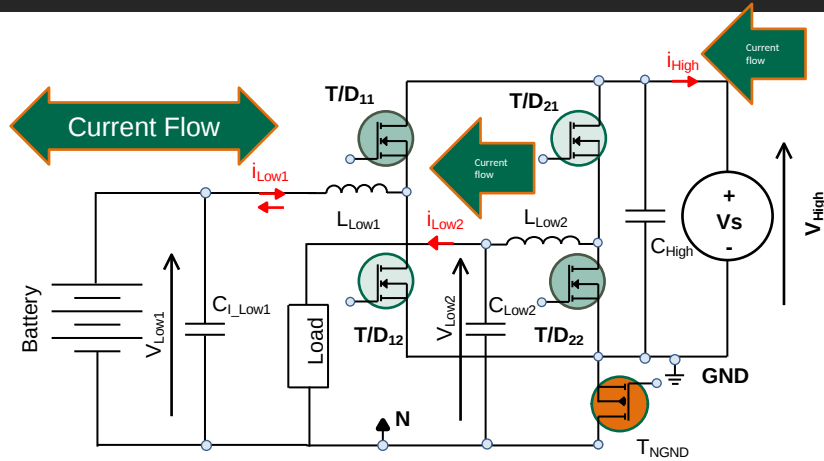


Variable	State
T_{NGND}	ON
Function	Buck
V_{IN}	$36V_{DC}$ to $48V_{DC}$
V_{OUT}	$10V_{DC}$ to $14V_{DC}$
Typical Application	Solar MPPT battery charger



Variable	State
T_{NGND}	ON
Function	Boost
V_{IN}	$24V_{DC}$
V_{OUT}	$48V_{DC}$ to $54V_{DC}$
Typical Application	Fuel cell Battery charger

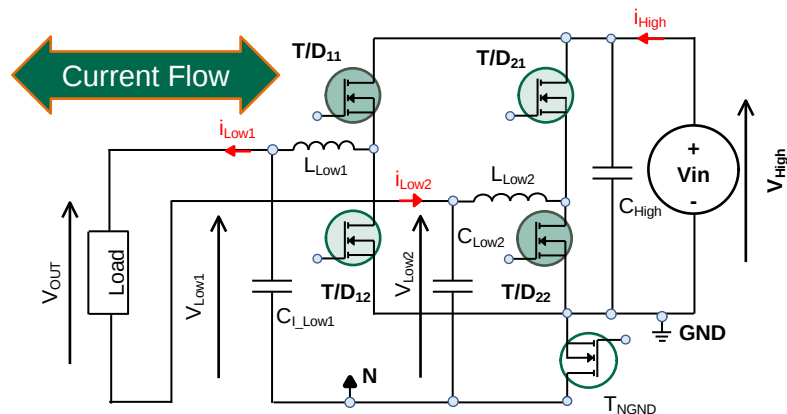
5 switches dual synchronous buck - DC-DC independent mode operation



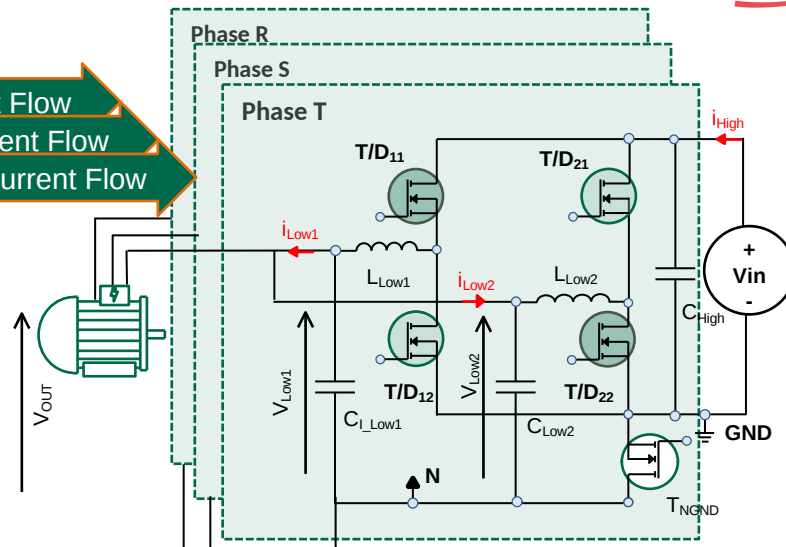
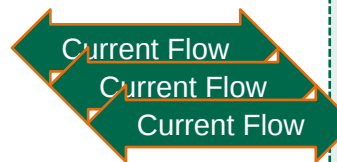
Variable	State
T_{NGND}	ON
Function	Leg 1 Battery Leg 2 Buck
V_{Source}	$48V_{DC}$
$V_{Battery}$	$24V_{DC}$
V_2	$12V_{DC}$
Typical Application	Solar Home system

Variable	State
T_{NGND}	ON
Function	Leg 1 Battery Leg 2 Battery
V_{High}	Floating V_{DC}
V_1	$24V_{DC}$
V_2	$12V_{DC}$
Typical Application	Peer-to-peer micro-grid transfer

5 switches dual synchronous buck - DC-AC mode operation



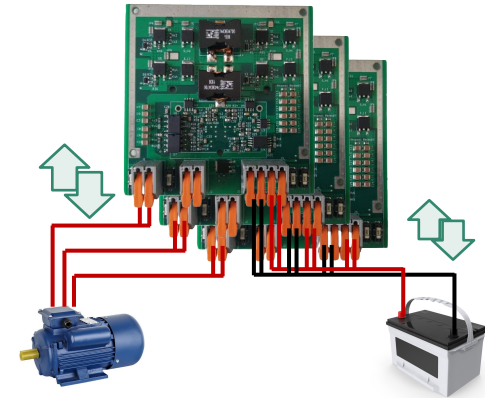
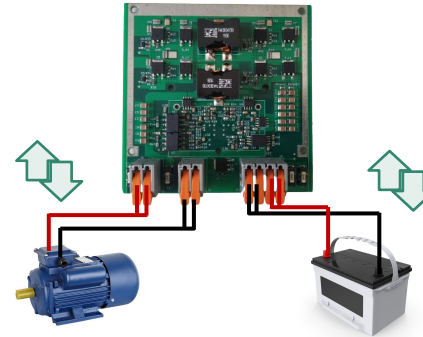
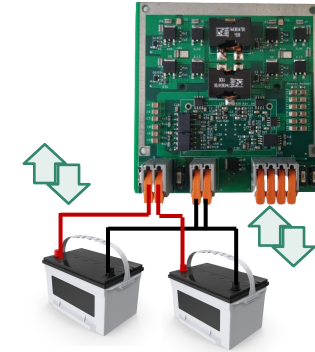
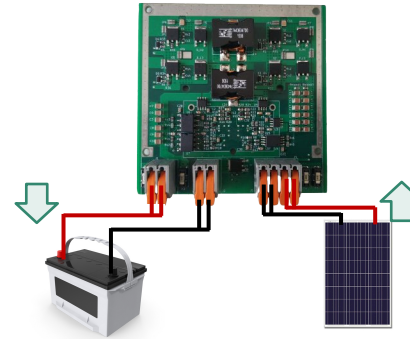
Variable	State
T_{NGND}	OFF
Function	Buck Inverter
V_{IN}	68V _{DC}
V_{OUT}	48.sin(ωt)
Typical Application	Single phase AC inverter



Variable	State
T_{NGND}	OFF
Function	3 phase Buck Inverter
V_{IN}	110V _{DC}
V_{OUT}	48.sin(ωt) 48.sin($\omega t + 2\pi/3$) 48.sin($\omega t - 2\pi/3$)
Typical Application	48V motor control

5 switches dual synchronous buck - Operation modes overview

Conversion	Function	V _{in}	V _{out}	P	V _{max}	Use Case
DC-DC	Buck interleaved	V _{HIGH}	V _{LOW1/2}	300	0.9 V _{HIGH}	Battery
	Boost interleaved	V _{LOW1/2}	V _{HIGH}	300	4*V _{LOW}	Battery
	Buck-Boost	V _{LOW1} OR V _{LOW2}	V _{LOW2} OR V _{LOW1}	150	0.9*4*V _{LOW}	Battery to Battery
DC-AC	1 phase	V _{HIGH}	V _{LOW1/2}	300	V _{HIGH}	Single phase motor control
	2 phase - 2 boards	V _{HIGH}	V _{LOW1/2}	600	V _{HIGH}	Stepper motor control
	3 phase - 3 boards	V _{HIGH}	V _{LOW1/2}	900	V _{HIGH} /2	Brushless motor control



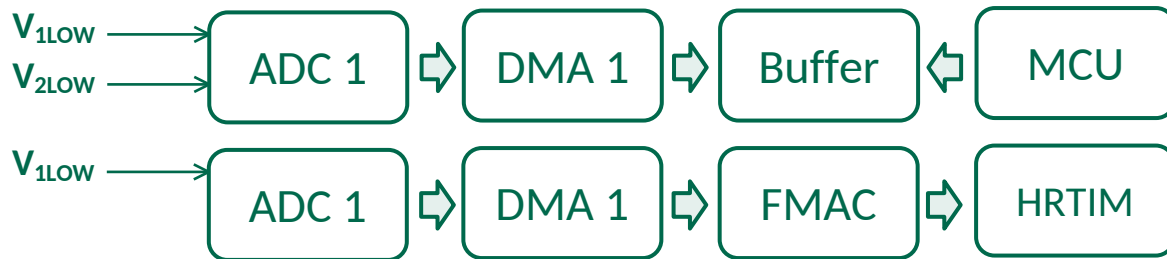
Software Defined Digital Hardware Design

➤ Reprogrammable ADC peripherals

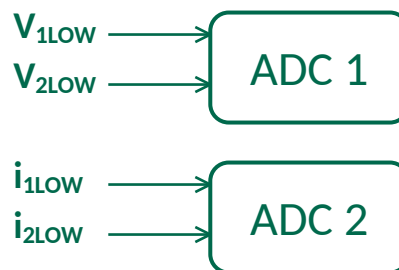
- ADC mode of operation depends on the control method
- Flexibility in terms of data and control
- Need to accelerate calculations

➤ Multi-mode data acquisition

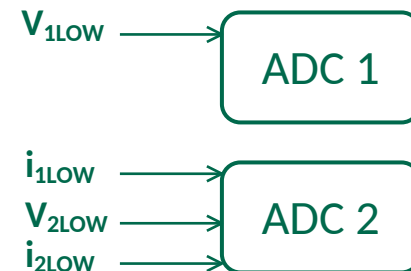
- Measurement scheme depends on control objectives of the application
- Application-level control may need intricate data measurements
- **Need for flexible channel allocation**



Synchronous measurements for accurate power measures

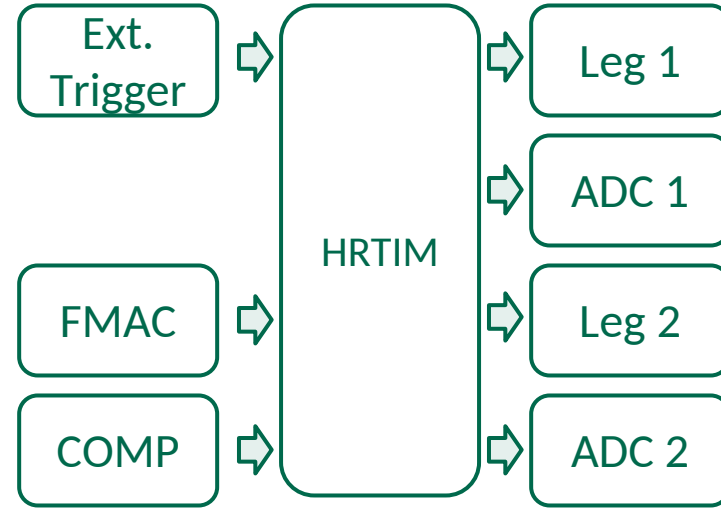


Fast measurement for accelerated control



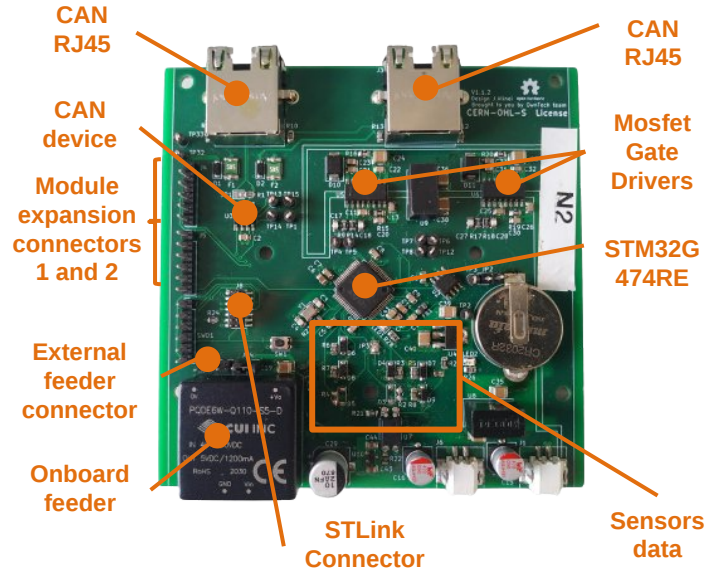
Slow measurements for Telemetry

- **Reprogrammable HRTimer**
 - PWM depends on the power conversion function
 - HRTimer must connect with other peripherals and provide triggers
 - HRTimer must be able to ensure either Voltage or Current mode controls
 - HRTimer must synchronize legs for interleaving and/or AC control
 - **The bandwidth of the HRTimer must be multiple orders of magnitude higher than the switching frequency**
- **Safety First**
 - HRTimers must be able to handle safety as well
 - **Current peak detection or other event driven shutdown** must be provided via analog means



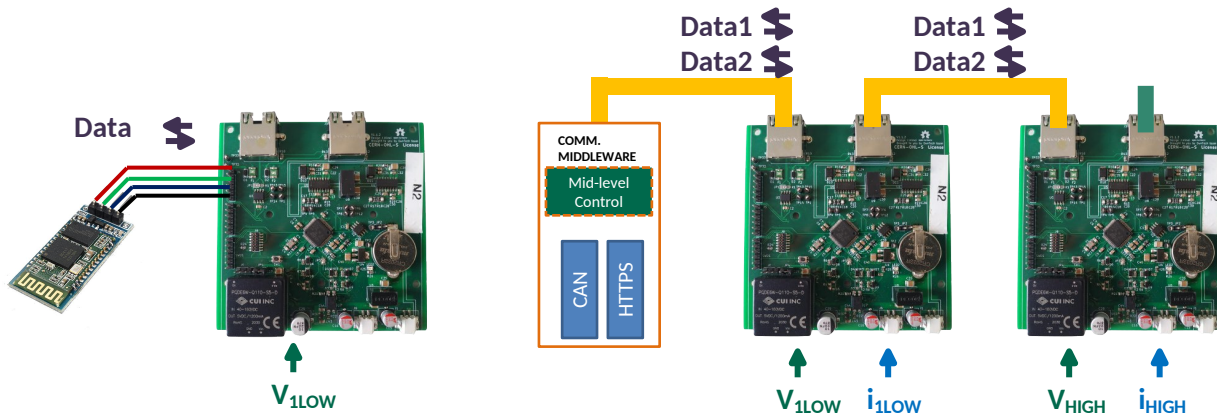
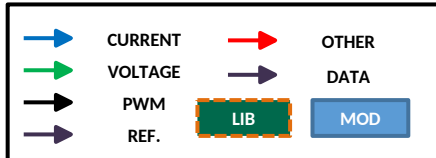
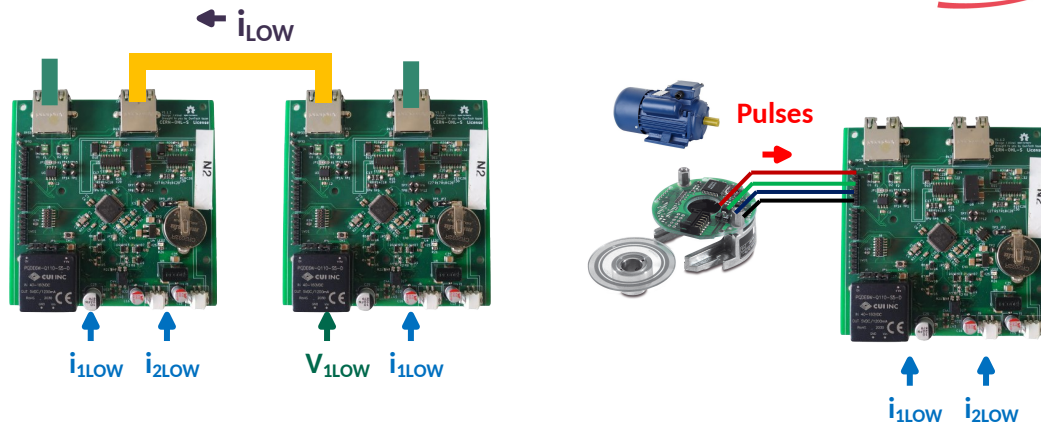


Peripheral	Details
HRTimer	13000 points at 200kHz
2 ADCs	Reassignable ADC channels for flexible control
2 DMAs	Flexible data handling
FMAC	Filter for accelerated control calculations
CORDIC	Accelerated trigonometric functions
FPU	Fast software math functions

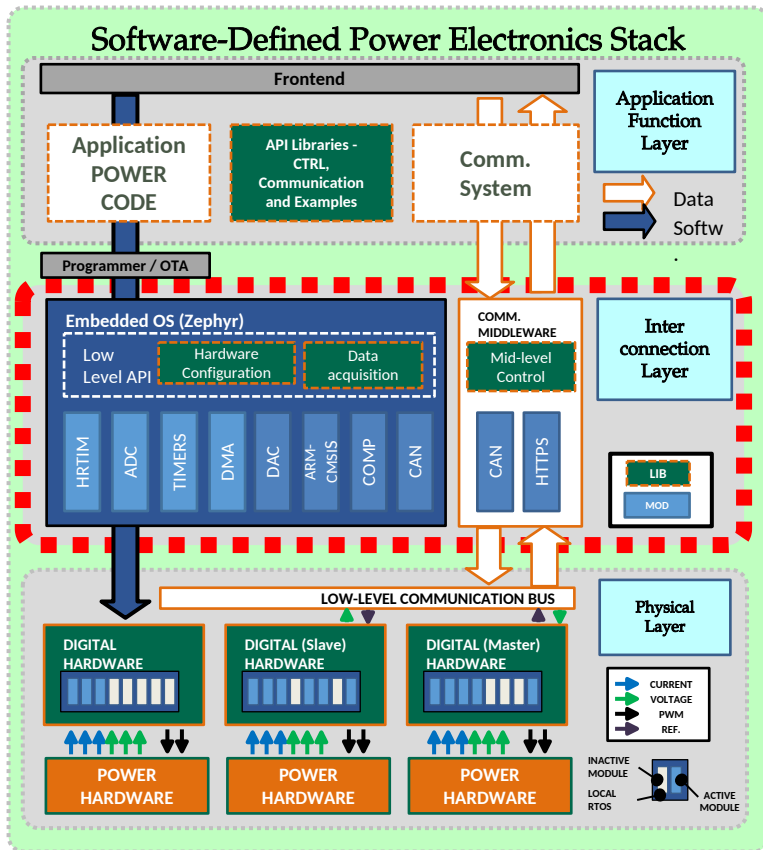


Peripheral	Details
Measurements	$V_{Low1/2}$, $i_{Low1/2}$, V_{High} , i_{High}
CAN-based communication	2 RJ45 connectors to create daisy-chain CAN
Isolated gate drivers	PWM to power stage driver
Expansion connector 1	USART, Rotary Encoder, GPIOs
Expansion connector 2	SD Card module, Rotary Encoder, GPIOs
STLink Connector	Programming and debugging

Function	Use case
CAN-Based communication	Master-slave control, System monitoring
Expansion connector 1	Bluetooth via USART, Rotary Encoder, GPIOs
Expansion connector 2	SD Card module, Rotary Encoder, GPIOs



The interconnection and Application layers



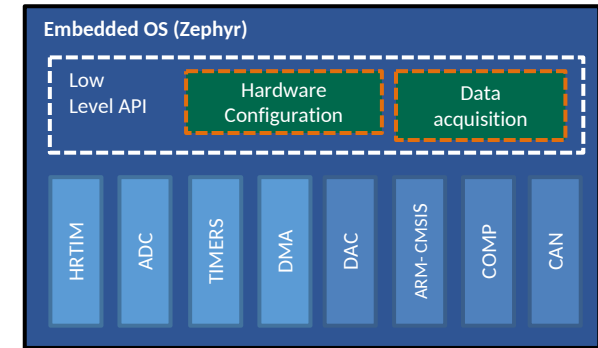
Leveraging an RTOS for P.E.

- Abstracting the hardware
- Creating drivers for the peripherals

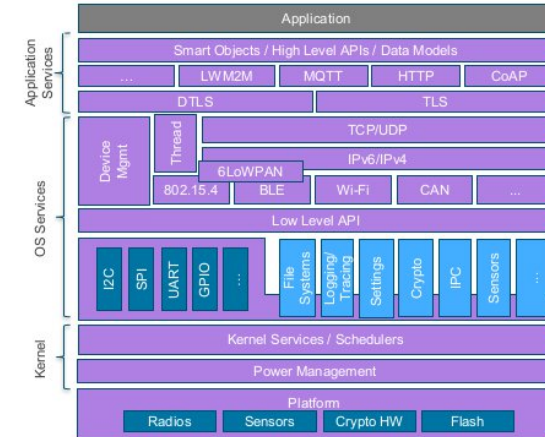
Communication Middleware

- Low-level communication Bus
- Standardizing communication protocols
- A dedicated hardware

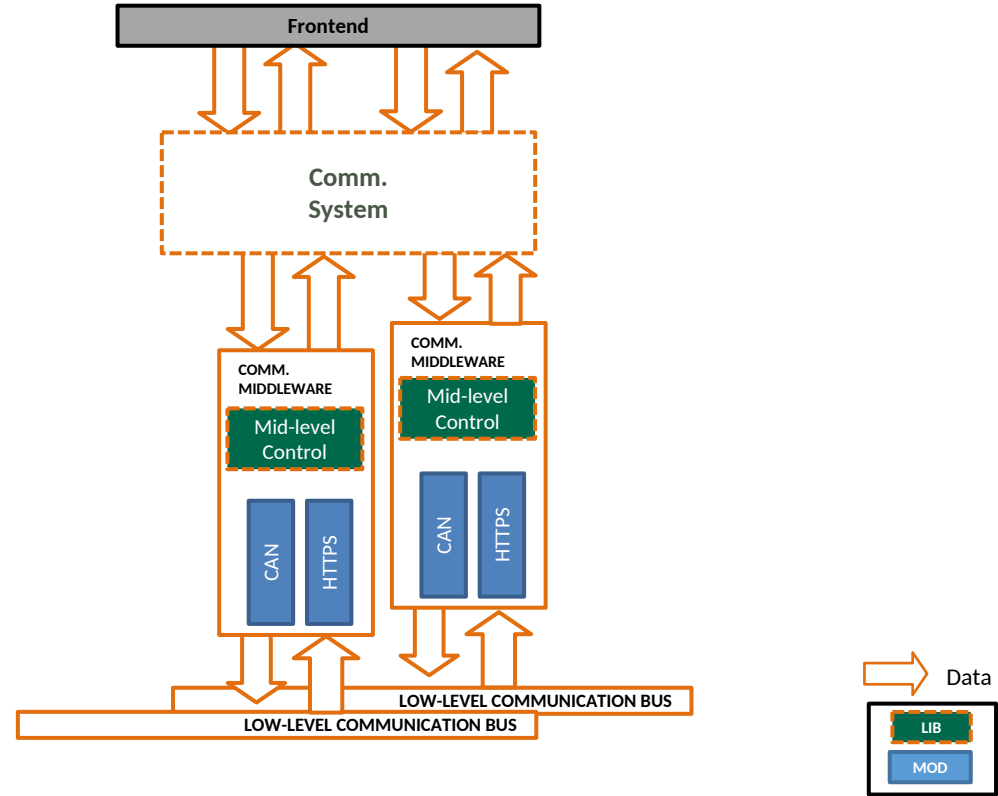
- RTOS have stacks and natively implement abstraction from hardware
- Out-of-the-box IoT compatible communication stack
- Driver-oriented programming and abstraction
- Low-level API abstraction possible
 - Using RTOS modules to create Power-Electronics oriented abstraction
 - Data Acquisition and handling also abstracted for easier control implementation



- Open source real-time OS
- Vibrant Community participation
- Safety and Security built-in
- Cross-architecture with broad SoC and development board support
- Vendor Neutral Governance
- Permissively licensed - Apache 2.0
- Complete, fully integrated, highly configurable, modular for flexibility



- Multi-purpose communication
 - Low level synchronization
 - High level data aggregation
- Data parsing and bi-directional flow
 - Uplink data harvesting
 - Downlink parameter update
- Data treatment
 - Data aggregation and system diagnosis
- Flexible control architectures
 - Decentralized
 - Hierarchical
 - Centralized



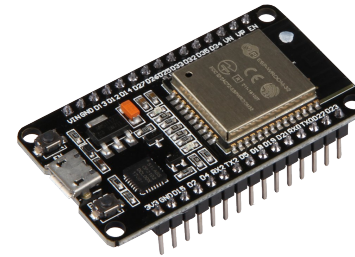
ThingSet

- Target agnostic data parsing system
- Possibility of creating data structures



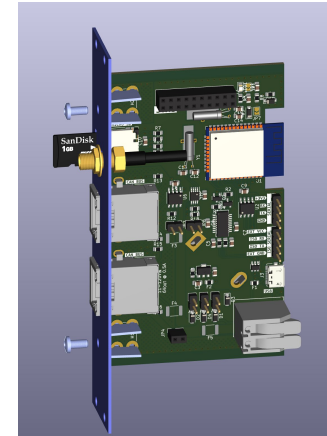
ESP32

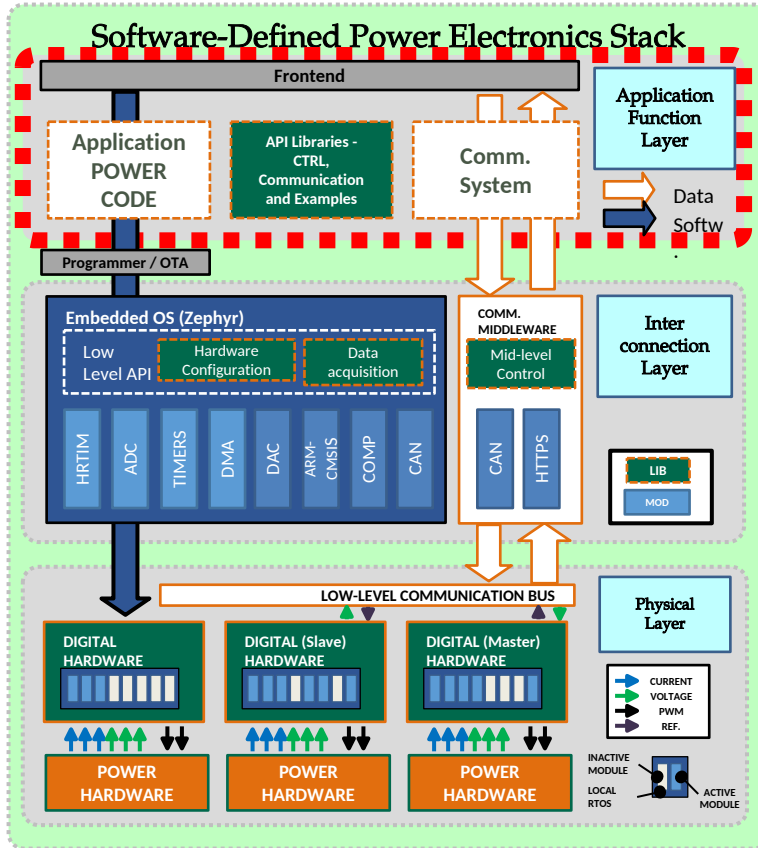
- Low-cost and ubiquitous IoT solution
- Separated cores allow for data pre-treatment



Dedicated board

- Open-Source ESP32 based solution compatible with CAN





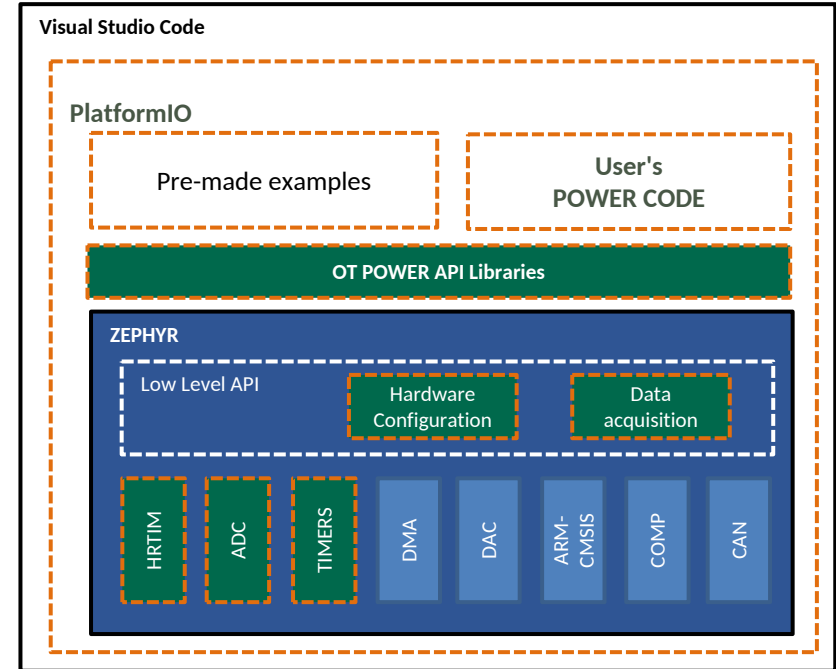
Leveraging an RTOS for P.E.

- Packaging software
- Leveraging abstraction

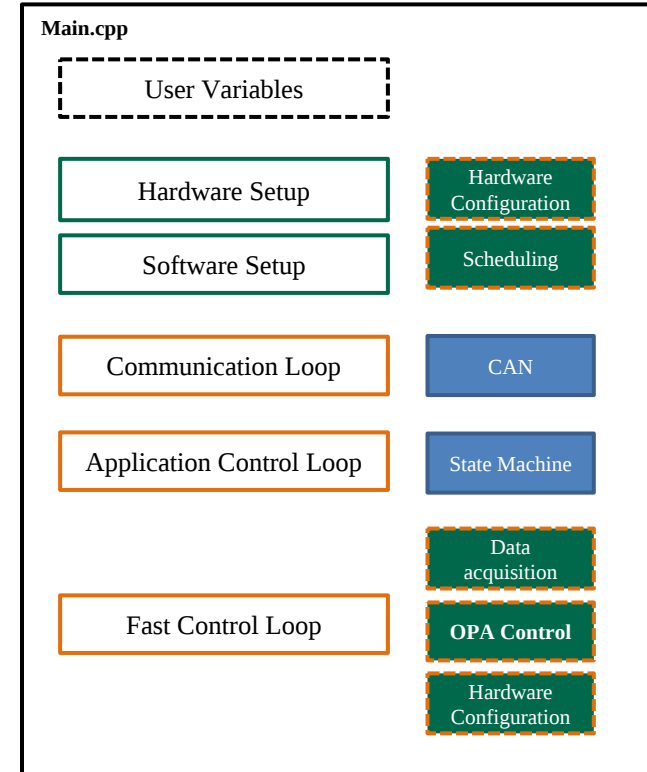
Communication System

- Flexible frontend

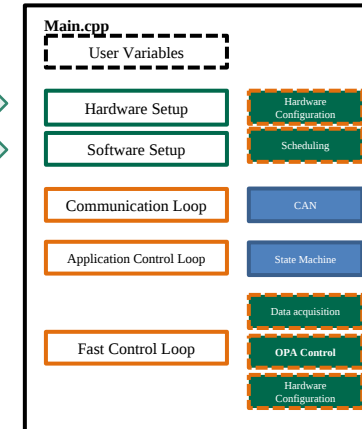
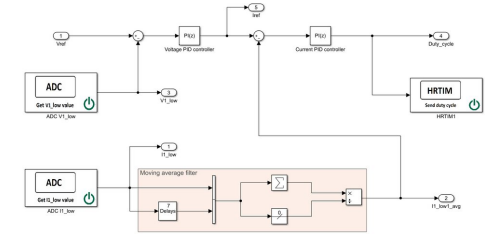
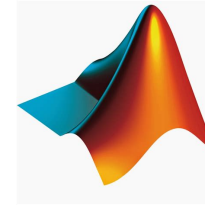
- VSCode outer envelope
- PlatformIO based usage
- Gitlab hosted Libraries
- Automatic handling of other 3rd party modules
- Low-Level API for abstracting the drivers
- In-House HRTIM driver
- Rewritten ADC driver for peripheral-to-peripheral connection
- In-house Timer module



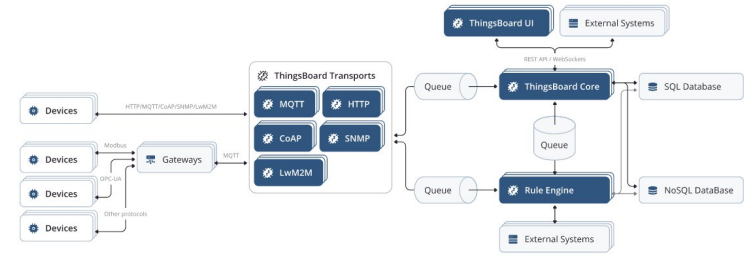
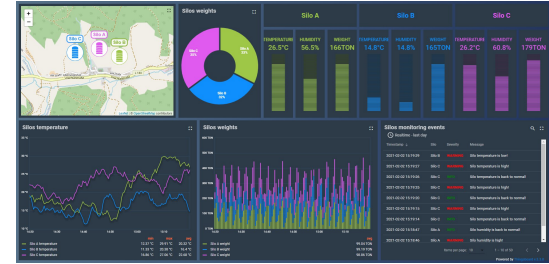
- Single main code for “Arduino-like” experience
- Setup and Loop ergonomics
- Hardware and Software Setup
- Communication, Application and Fast Control Loop




- Matlab blocks can be generated to call the abstraction layer modules
- Application code is automatically generated
- The code is automatically put in the folder tree
- The code is called from the application loop or the fast control loop



- Flexibility in the communication protocols
- Expansion with multiple devices
- Data aggregation
- Data treatment



- Legend:
-  ThingsBoard Components: horizontally scalable and fault tolerant
 -  Message Queue: Kafka, RabbitMQ, AWS SQS, Azure Service Bus, Google Pub/Sub
 -  Databases: PostgreSQL and Timescale/Cassandra (NoSQL)
 -  Gateways: support of Modbus, OPC-UA, BLE, CAN, MQTT, HTTP, and other protocols

Design Case of Multi-Level Converter

Matthias Preindl

Multilevel topologies have many benefits and applications:

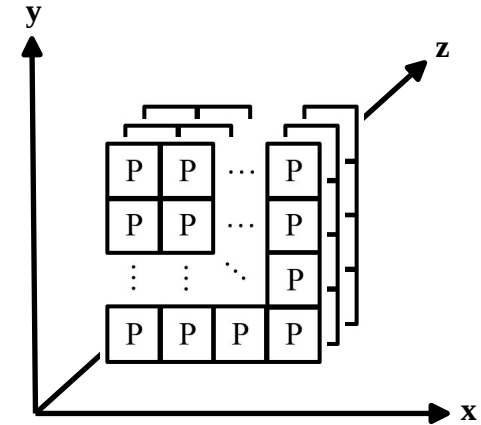
- HVDC, automotive
- Improved power quality, lower switching voltages, reduction in EMI

At the cost of:

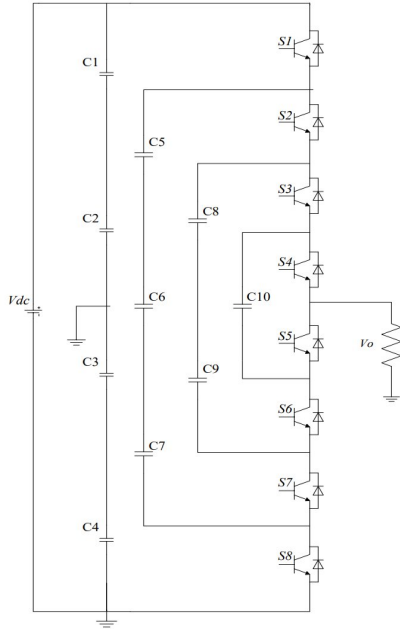
- complexity
- component quantities

Goal:

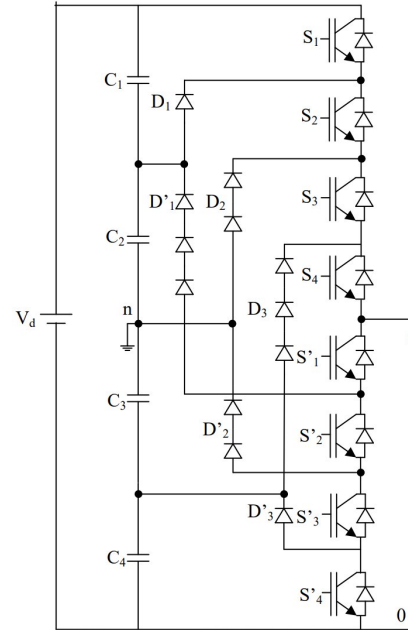
- Easily expandable and modular approach to power electronic conversion
- Linear component quantity and circuit complexity scaling with respect to number of levels
- ☑ a new power electronics environment



- Increase x ☑ increased current (parallel connection)
- Increase y ☑ increased voltage (series connection)
- Increase z ☑ increased number of outputs (multiphase connection)



Flying capacitor topology [1]



Diode clamped topology [2]

Typical multilevel topologies do not fit this goal

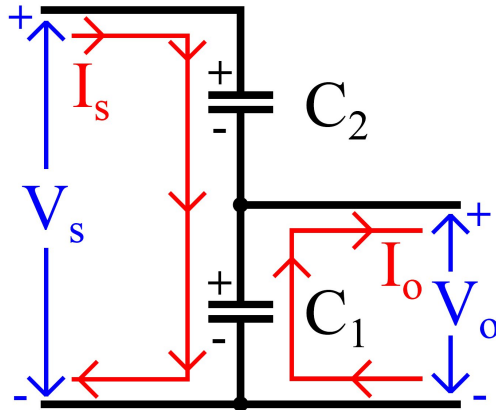
- circuit connections change as number of levels increases
- component quantities do not scale linearly
- switching state control must be applied to the entire converter

The MMC has linear component quantity and circuit complexity scaling

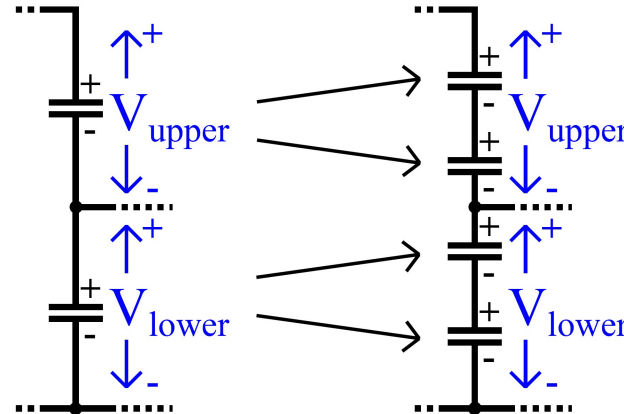
- switching state control must be applied to the entire converter
- Challenging to maintain capacitor voltage balance in steady state

✉ DC/DC implementation difficult

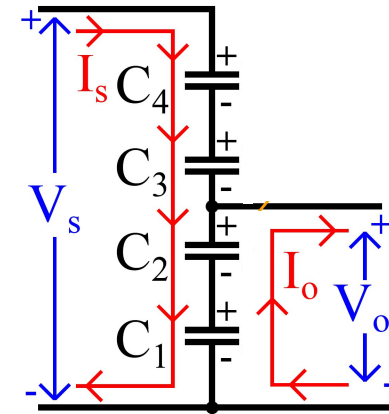
- We can build a multilevel topology around a center stack of capacitors
- Where each capacitor represents a voltage level
- And the input voltage is split along the series combination of these capacitors



2 capacitor/2 level



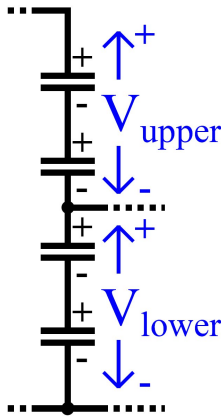
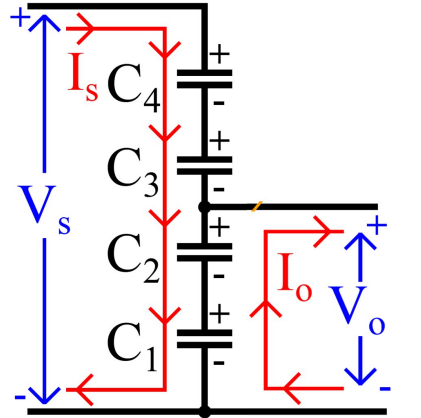
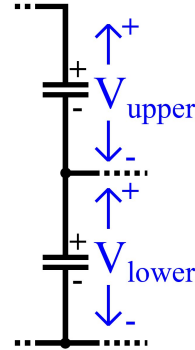
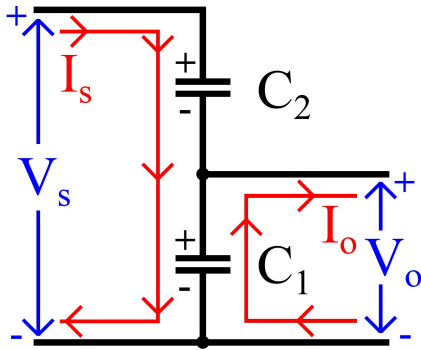
Multilevel expansion by splitting capacitors



4 capacitor/4 level

This topology, as it is shown above, does not maintain capacitor voltage in steady state

- For positive I_s and I_o , upper voltage will increase and lower voltage will decrease



For capacitor voltage balance in steady state, all capacitor currents must equal zero:

- upper capacitors: $I_{C,upper} = I_s$
- lower capacitors: $I_{C,lower} = I_s - I_o$

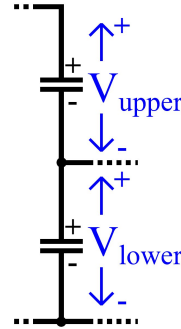
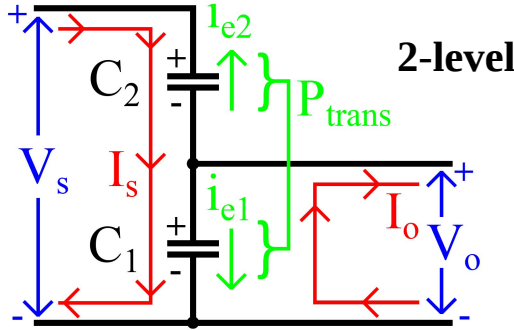
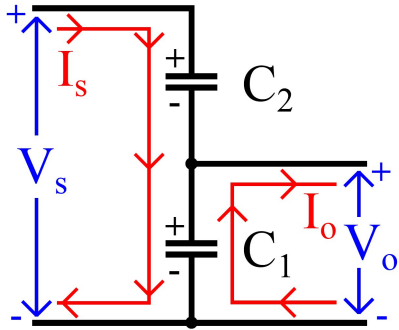
These capacitor currents can be interpreted as excess powers within each set capacitors:

- set of upper capacitors: $P_{e,upper} = (V_{in} - V_o)I_i$
- set of lower capacitors: $P_{e,lower} = V_o(I_i - I_o)$

Given $P_{in} = P_{out}$, it can be found that: $P_{e,upper} = -P_{e,lower}$

☑ Transferring excess powers between the upper set of capacitors and lower set of capacitors will result in a total cancellation of all excess powers

The excess powers do not depend on the number of levels

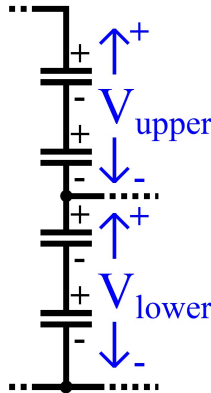
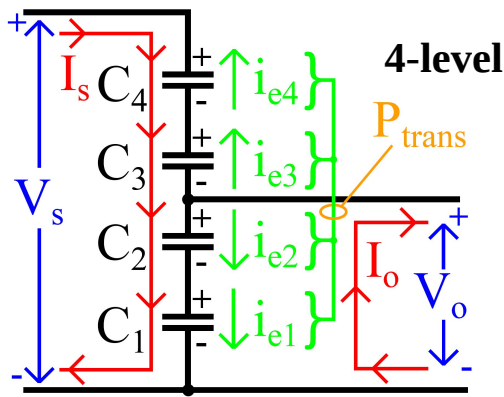
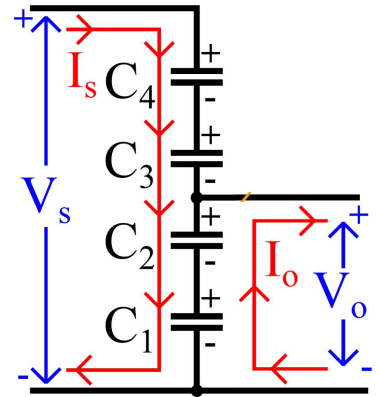


$$P_{e,C1} = V_{C1}(I_s - I_o)$$

$$P_{e,lower} = V_{lower}(I_s - I_o)$$

$$P_{e,C2} = V_{C2}I_s$$

$$P_{e,upper} = V_{upper}I_s$$

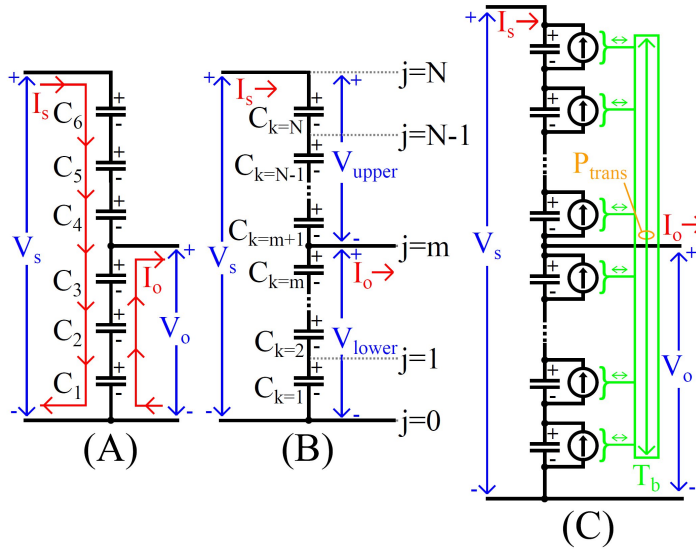


$$P_{e,C1} + P_{e,C2} = (V_{C1} + V_{C2})(I_s - I_o)$$

$$P_{e,lower} = V_{lower}(I_s - I_o)$$

$$P_{e,C3} + P_{e,C4} = (V_{C3} + V_{C4})I_s$$

$$P_{e,upper} = V_{upper}I_s$$



$$P_{e,lower} = \sum_{k=1}^m i_{ck} V_{ck} = I_s V_{upper}$$

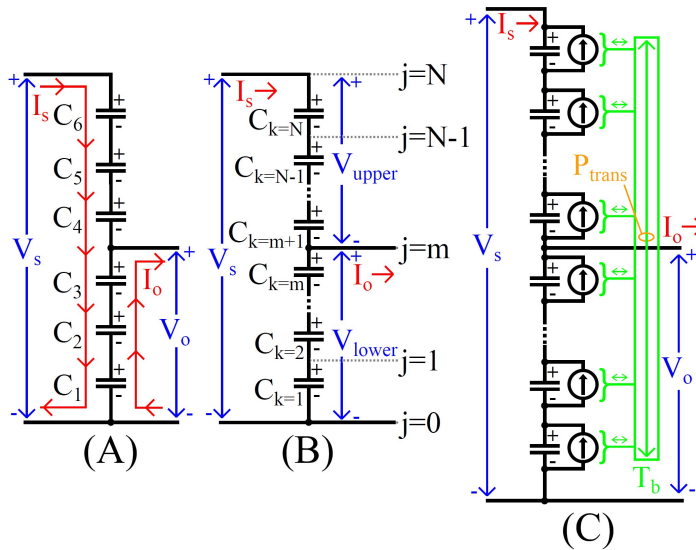
$$P_{e,upper} = \sum_{k=m+1}^{N-1} i_{ck} V_{ck} = (I_s - I_o) V_{lower}$$

$$P_o = I_s \sum_{k=1}^{N-1} V_{ck} = I_o \sum_{k=1}^m V_{ck}$$

$$P_{trans} = I_s \sum_{k=1+m}^{N-1} V_{ck} = (I_s - I_o) \sum_{k=1}^m V_{ck}$$

Because the excess powers do not depend on the number of levels:

- the amount of power P_{trans} that needs to be transferred between the upper and lower sets of capacitors does not change with the number of levels
- **linear component stress scaling with number of levels**



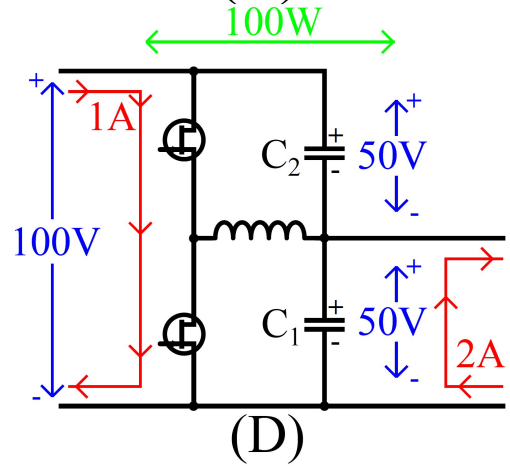
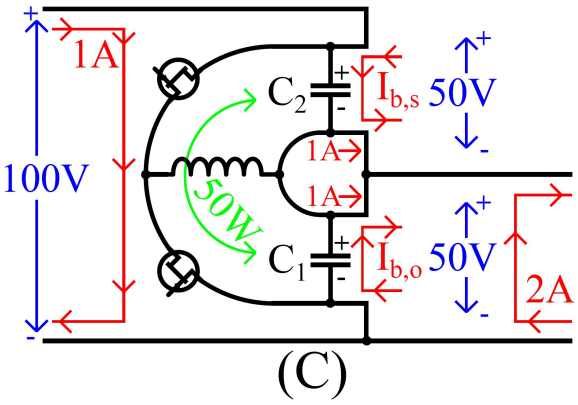
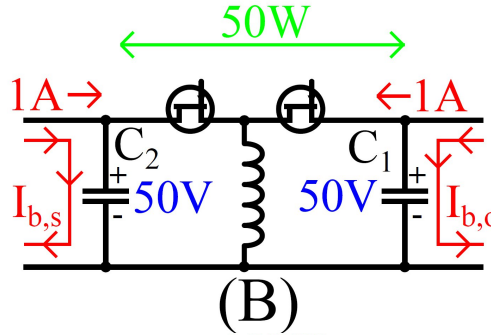
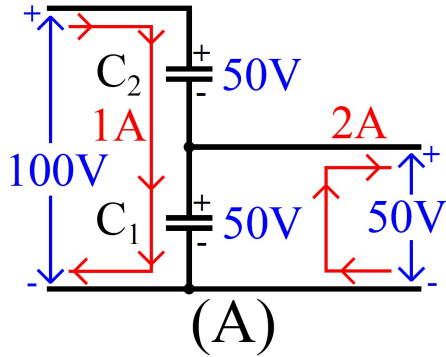
$$\left| \frac{P_{trans}}{P_o} \right| = \left| \frac{I_s \sum_{k=1+m}^{N-1} V_{ck}}{I_s \sum_{k=1}^{N-1} V_{ck}} \right| = \left| \frac{V_{upper}}{V_s} \right|$$

$$\left| \frac{P_{trans}}{P_o} \right| = \left| \frac{I_o \sum_{k=1}^m V_{ck}}{I_o \sum_{k=1}^m V_{ck}} \right| = \left| \frac{I_s - I_o}{I_o} \right|.$$

The excess powers are always less than the output power. This means that:

- the internal power transfer P_{trans} required to maintain voltage balance in steady state is less than P_o
- P_{trans} is a function of the conversion ratio
- **This converter topology internally converts less power than it outputs**
- a “differential” power converter

Topology implementation (Sanity check)



We can use this topological framework to develop a hypothetical 100W buck converter from a 50W buck/boost converter

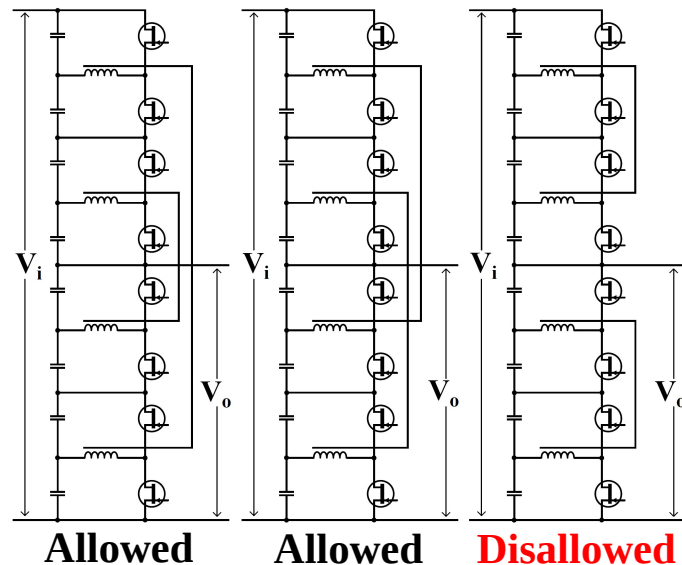
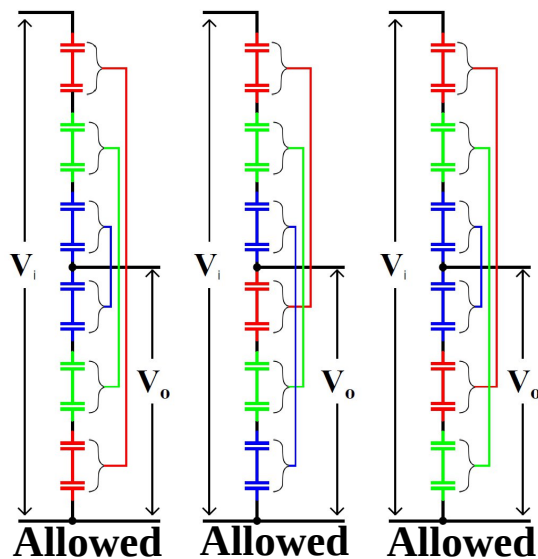
a) baseline 2-level converter made using the proposed topological framework

b) 50W buck/boost converter used to transfer power between upper and lower capacitors

c) connection of the 50W buck/boost converter

d) resulting 100W buck converter

There are allowable power transfer links – power must have a path to move from the upper set of capacitors to the lower set of capacitors



We can then develop a mathematical framework to accompany the topological framework

State space formulation :

$$V_c^+ = V_c + \frac{T_s}{C} \mathbf{T}_b i_b + \frac{T_s}{C} \mathbf{T}_e i_e$$

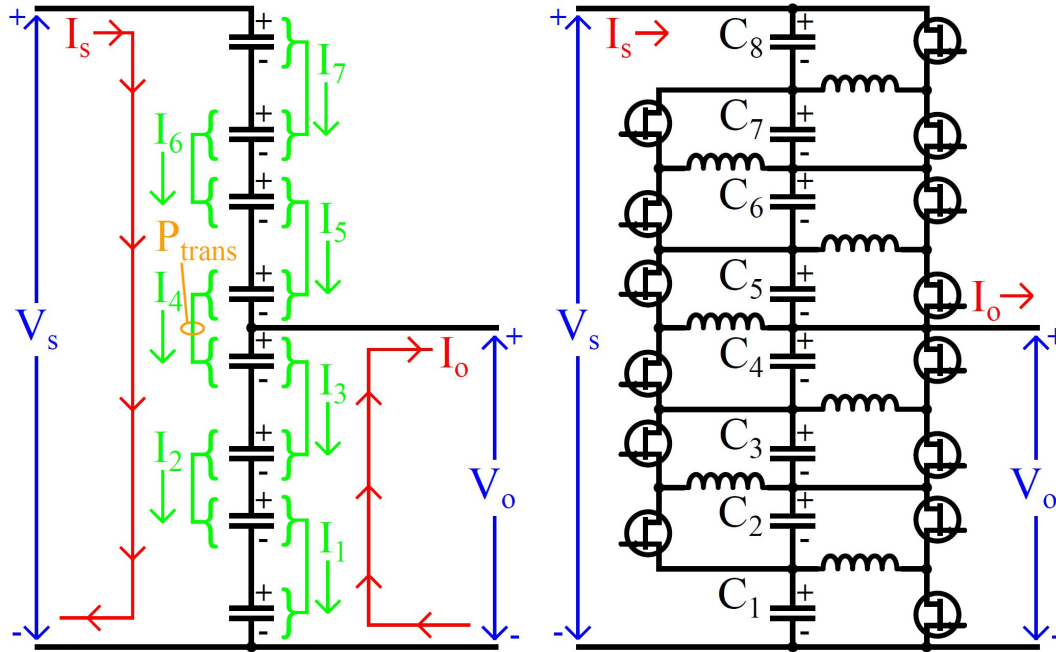
With constraint of:

$$V_c \mathbf{T}_b i_b = 0$$

- represents how the internal capacitive balancing currents cannot add power into the system

Where:

- V_c is vector of capacitor voltages $V_c = [V_{C,1}, V_{C,2}, \dots, V_{C,N}]'$
- C is capacitance
- T_s is controller sample interval
- i_e is a vector that contains the external currents I_i and I_o $i_e = [I_s, I_o]'$
- \mathbf{T}_e is a connectivity matrix that represents which capacitors are affected by the external currents i_e
- \mathbf{T}_b is a connectivity matrix that represents the capacitive power transfer links
- i_b is a vector that denotes the amount of power shared across each link



Circulating currents!

$$V_c^+ = V_c + \frac{T_s}{C} \mathbf{T}_b i_b + \frac{T_s}{C} \mathbf{T}_e i_e$$

$$V_c \mathbf{T}_b i_b = 0 \quad i_e = [I_s, I_o]'$$

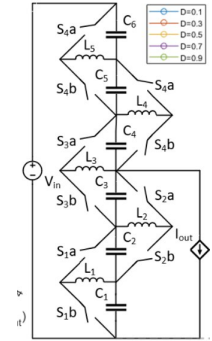
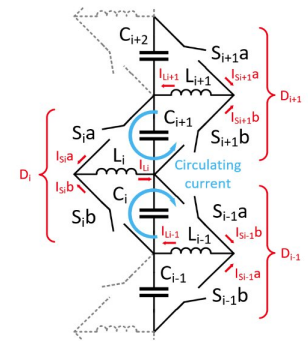
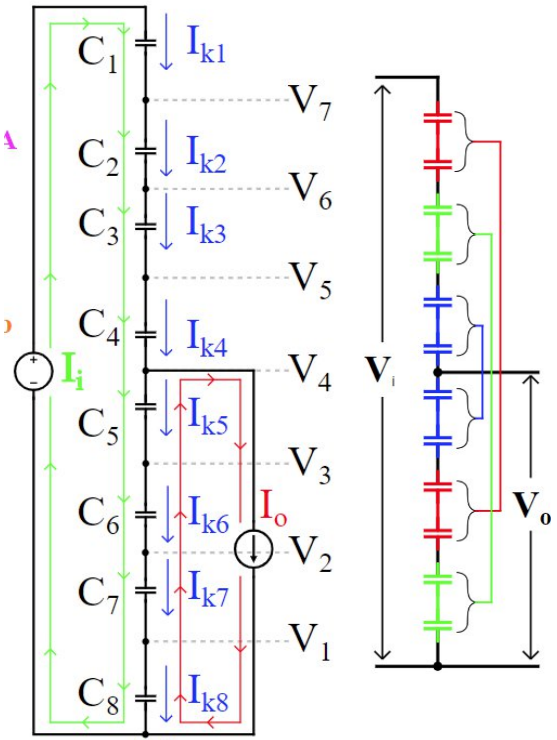
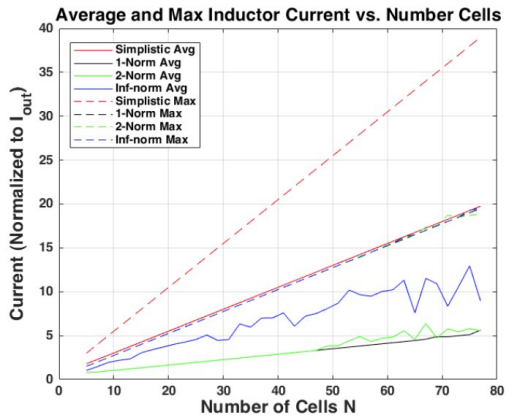
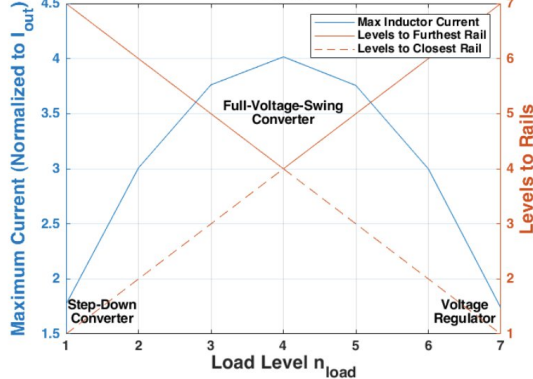
$$V_c = [V_{C,1}, V_{C,2}, \dots, V_{C,N}]'$$

$$\mathbf{T}_e = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \end{bmatrix}$$

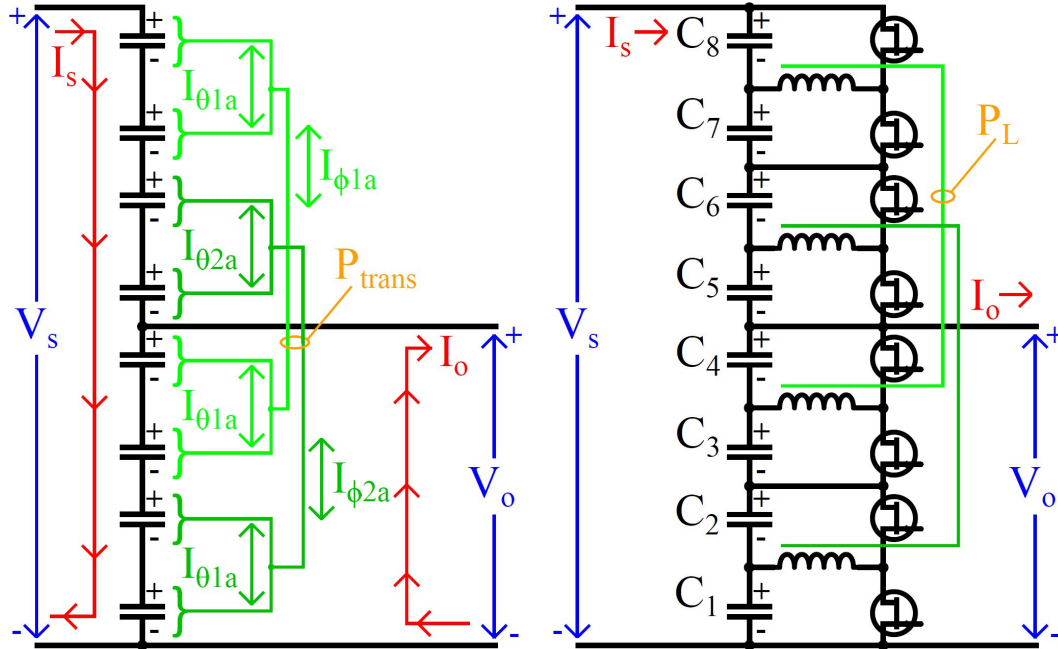
$$i_b = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \end{bmatrix} \quad \mathbf{T}_b = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

Topology Implementation – Half Bridges – Circulating

Inductor Current and Levels to Rails vs. Load Level
7 Cell



- This is because the capacitors below the output node need current to support their voltage
- This current comes from the upper capacitors, cascading through each module
- nonlinear component stresses with number of level



No circulating current!

$$V_c^+ = V_c + \frac{T_s}{C} \mathbf{T}_b i_b + \frac{T_s}{C} \mathbf{T}_e i_e$$

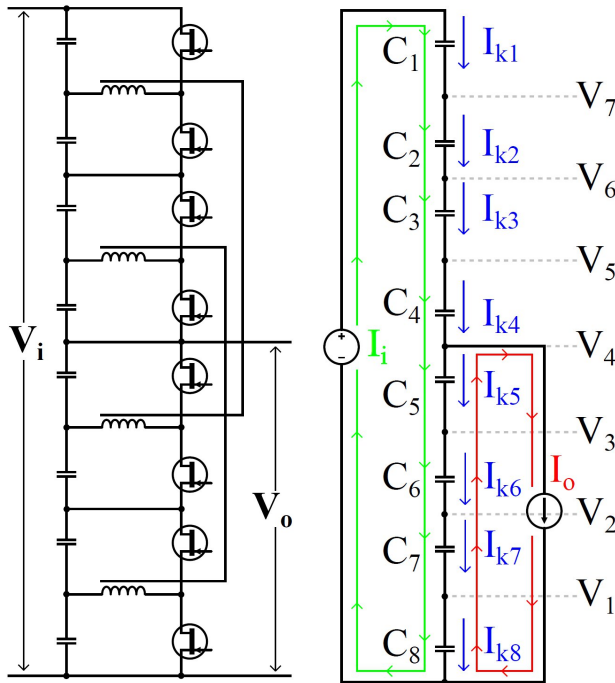
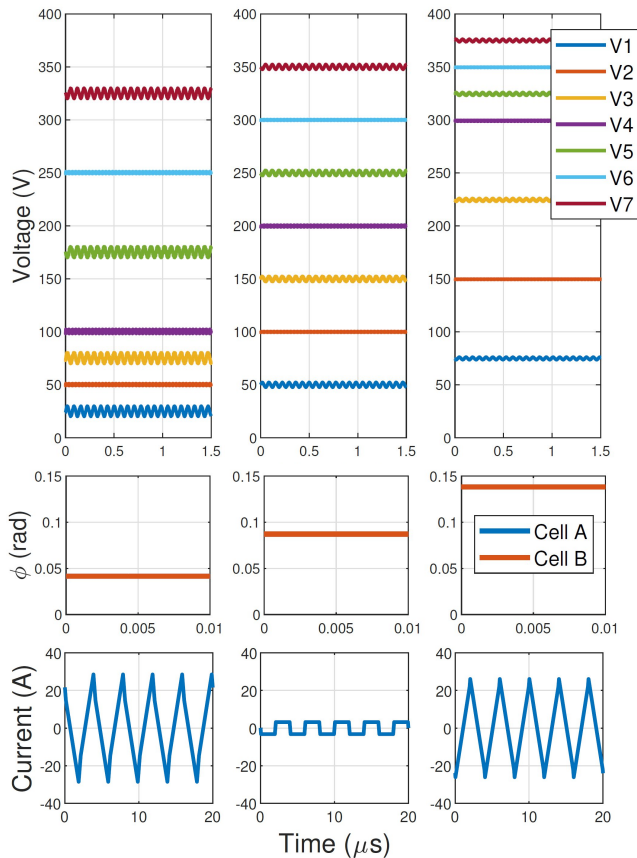
$$V_c \mathbf{T}_b i_b = 0 \quad i_e = [I_s, I_o]'$$

$$V_c = [V_{C,1}, V_{C,2}, \dots, V_{C,N}]'$$

$$\mathbf{T}_e = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \end{bmatrix}$$

$$i_b = \begin{bmatrix} I_{\phi 1} \\ I_{\theta 1a} \\ I_{\theta 1b} \\ I_{\phi 2} \\ I_{\theta 2a} \\ I_{\theta 2b} \end{bmatrix} \quad \mathbf{T}_b = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & -1 & 0 & -1 \end{bmatrix}$$

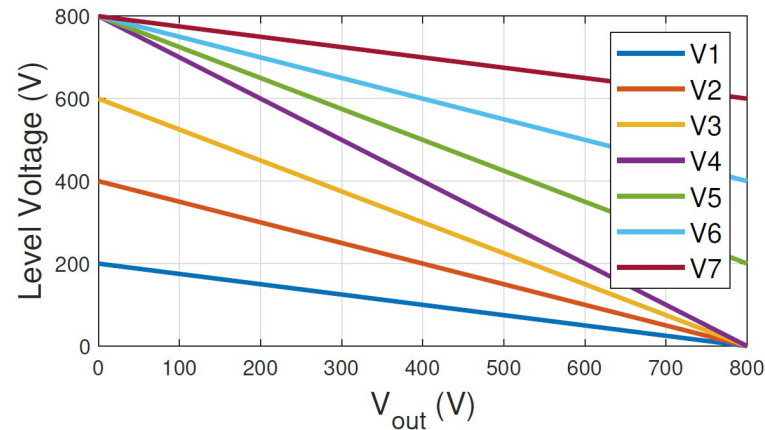
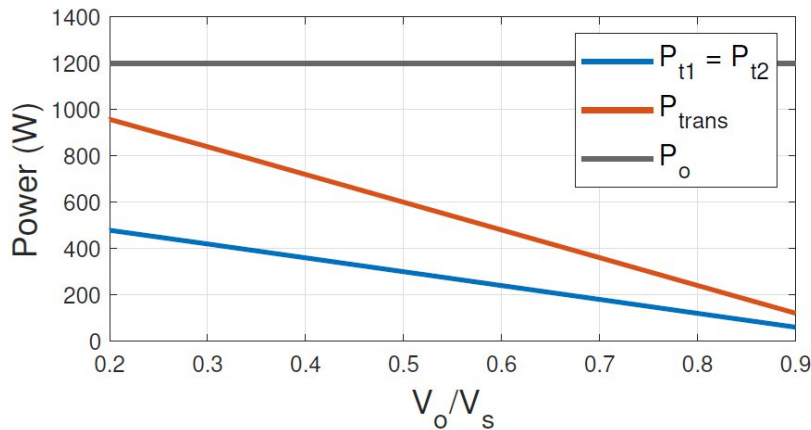
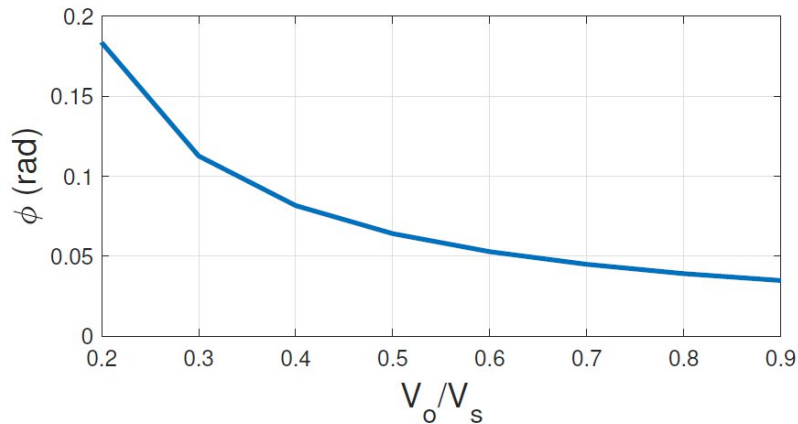
Topology Implementation – Dual Active Half Bridges – Results



High-Fidelity Simulation transient results

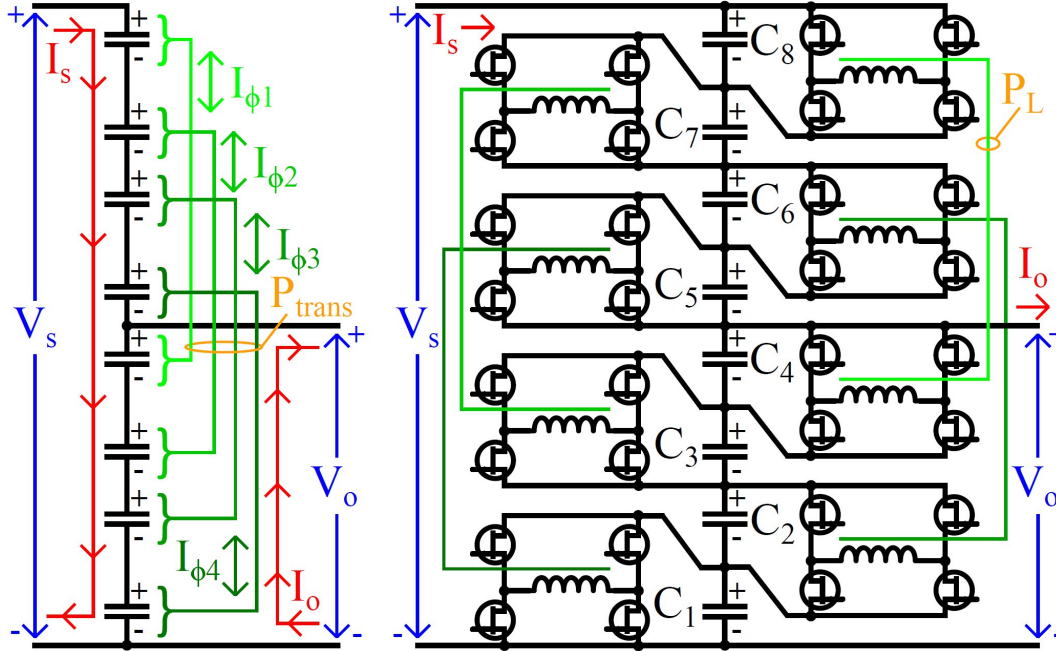
- $C = 24\mu\text{F}$
- $L = 2.5\mu\text{H}$
- $f_{\text{sw}} = 200\text{kHz}$
- $n = 1$
- load = 100R
- $V_{\text{in}} = 400\text{V}$
- all DAHBs operated with same parameters
- Duty cycle set to 0.5
- phase difference ϕ set to the same for both HBs
- PI control used to find required ϕ to achieve desired V_o

Topology Implementation – Dual Active Half Bridges – Results



High-fidelity simulation average results

- same parameters as previous sweep
- $V_{in} = 800V$
- Constant output power over V_{out} sweep
- ideal voltage splitting maintained over the sweep
- P_{trans} always less than P_o



No circulating current!

$$V_c^+ = V_c + \frac{T_s}{C} \mathbf{T}_b i_b + \frac{T_s}{C} \mathbf{T}_e i_e$$

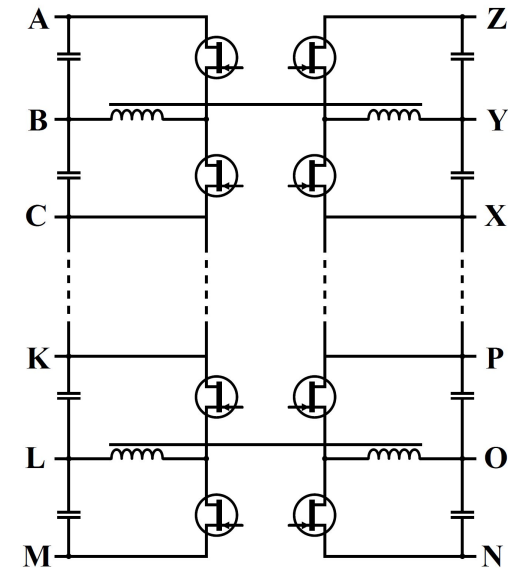
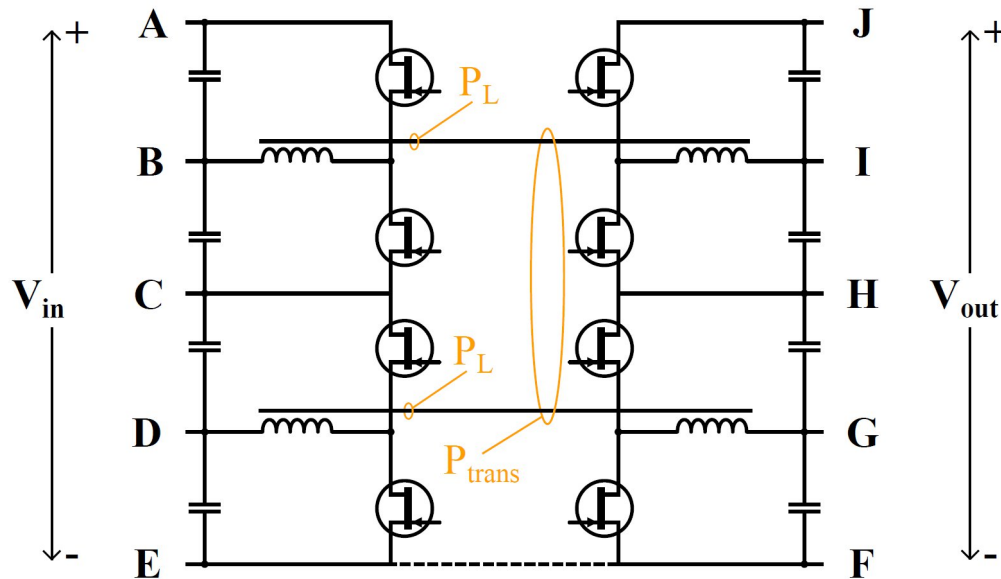
$$V_c \mathbf{T}_b i_b = 0 \quad i_e = [I_s, I_o]'$$

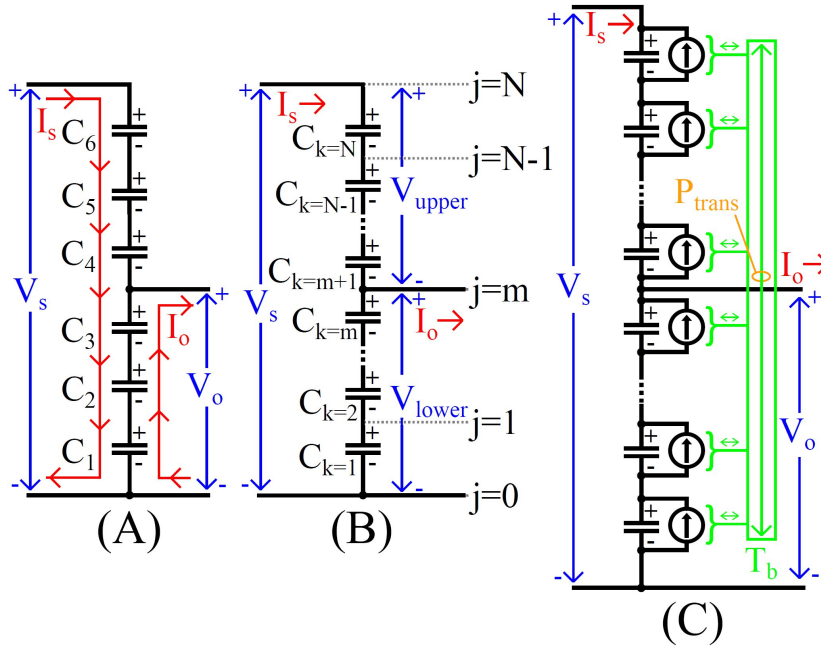
$$V_c = [V_{C,1}, V_{C,2}, \dots, V_{C,N}]'$$

$$\mathbf{T}_e = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \end{bmatrix}$$

$$i_b = \begin{bmatrix} I_\phi \\ I_{\theta 1} \\ I_{\theta 2} \\ I_{\theta 3} \\ I_{\theta 4} \end{bmatrix} \quad \mathbf{T}_b = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ -1 & 0 & 0 & -1 & 0 \\ -1 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & -1 \end{bmatrix}$$

- It is also allowable to mix and match capacitive power sharing techniques
- Any combination of methods can be used as long as all upper capacitor and all lower capacitors have a path to transfer power
- Isolated configurations can also be implemented



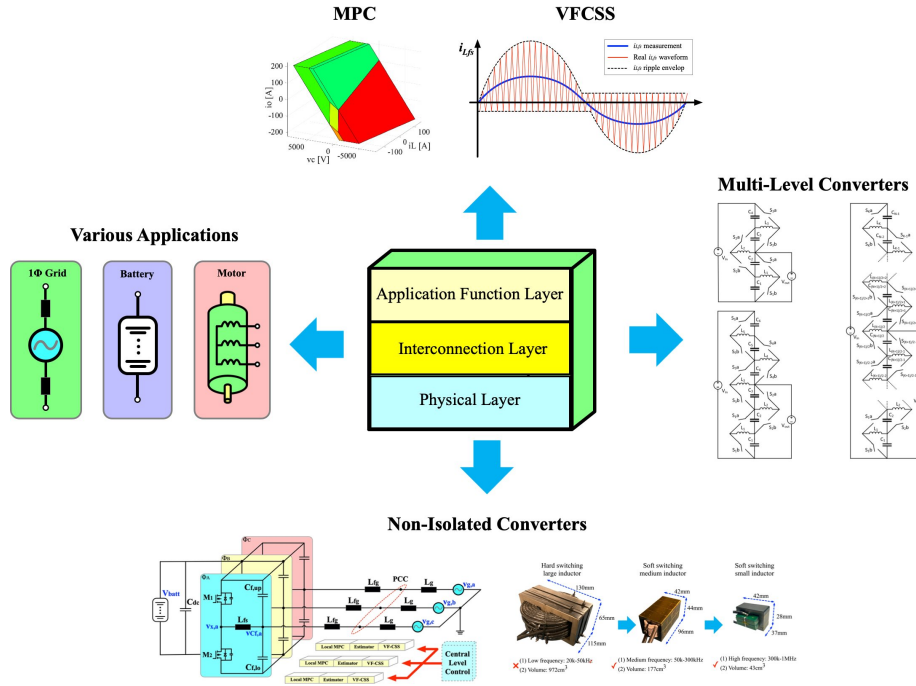


- This multilevel topological framework is:

- easily expandable (more capacitors = more levels)
- has linear component quantity scaling with levels
- can have linear component stresses scaling with levels (DAHB, DAFB)
- is fully balanced
- can operate bidirectionally
- has isolated and non-isolated variants
- can be used with advanced control methods
- can also be controlled with a single parameter (ϕ) to achieve the full output voltage range

Conclusion

Matthias Preindl, Luiz Villa

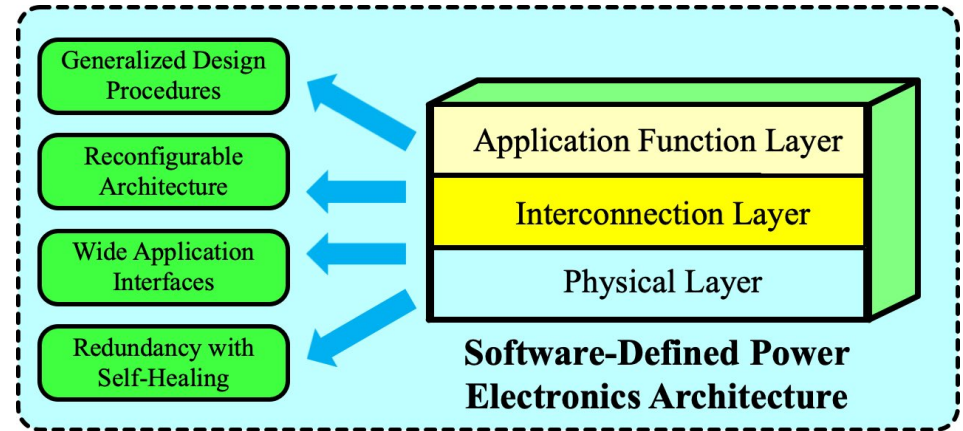


Software-Defined Power Electronics:

- Techniques: MPC, VFCSS.
- Applications: Grid, motor, battery, solar, etc.
- Hardware Optimization: High efficiency.
- Non-Isolated Topology: Low cost.
- Multi-Level Converters: High voltage, low ripple.

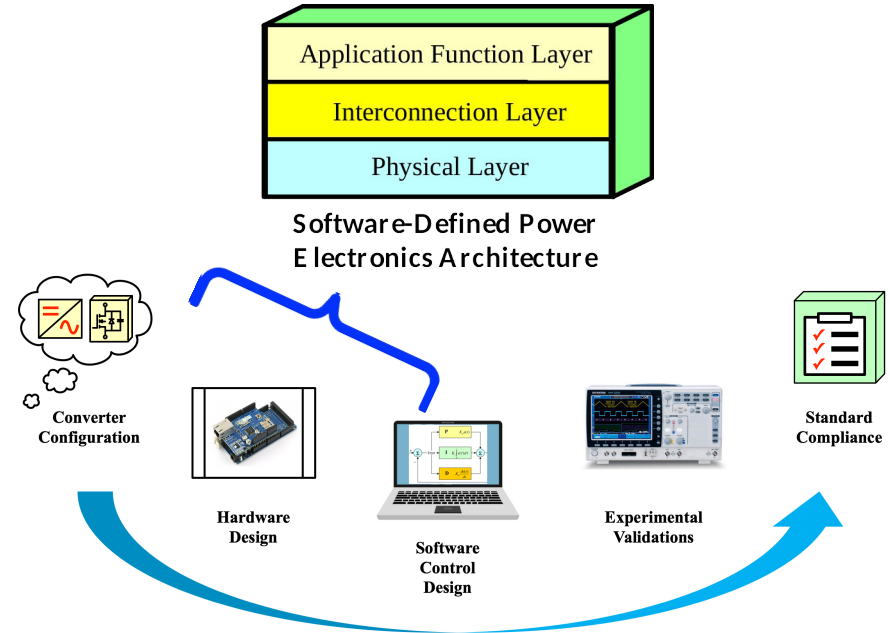
Software-Defined Power Electronics:

- Generalized design procedures.
- Reconfigurable architecture.
- Wide application interfaces.
- Redundancy with self-healing.



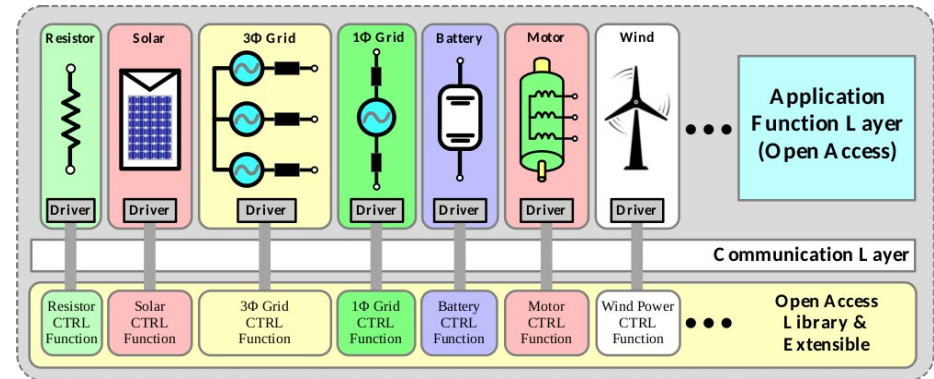
Generalized design procedures:

- Save repetitive design procedures.
- No hardware component redesign.
- No software algorithm redesign.



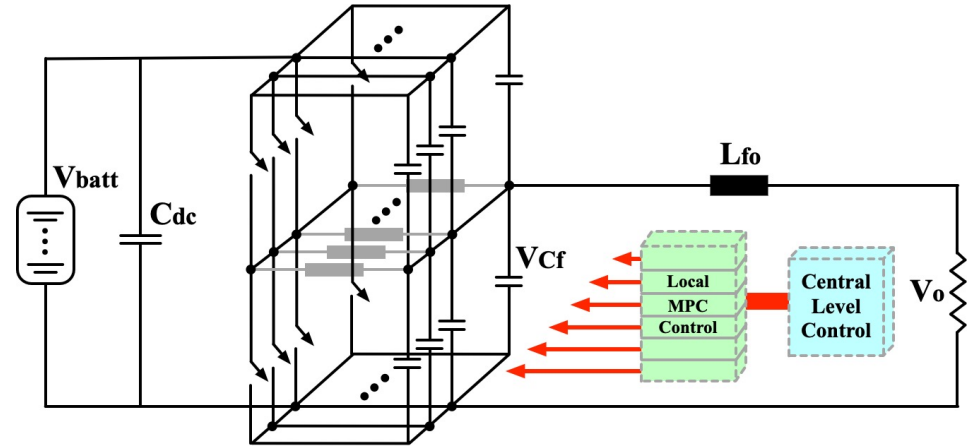
Reconfigurable Architecture :

- Feasible for various applications.
- Extensible control functions.
- Random number of power modules.



Redundancy with self-healing :

- Auxiliary modules for redundancy.
- Timely monitoring power failure.
- Substitute for failed modules.



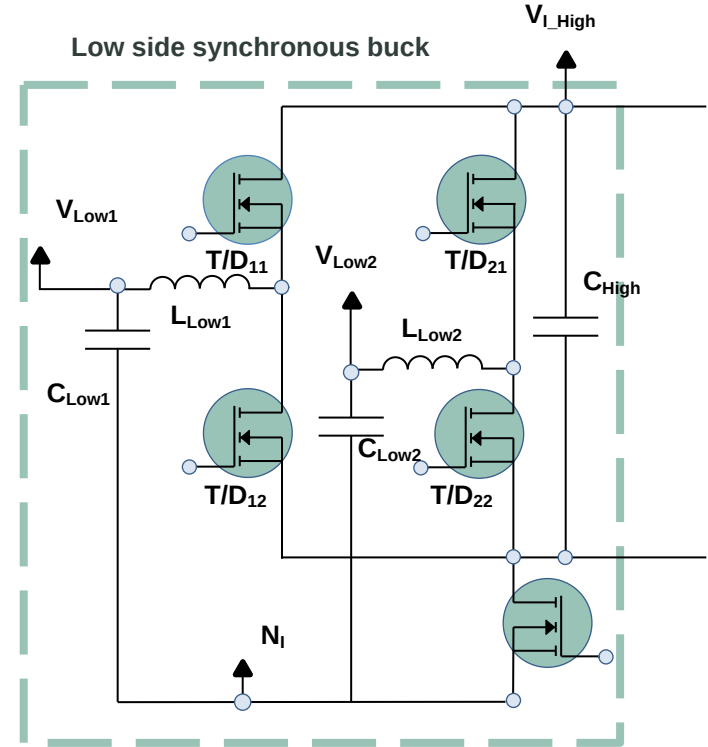
Choosing the starting point is really not easy

- Which Digital Power SoC ?
- Which Power Hardware ?

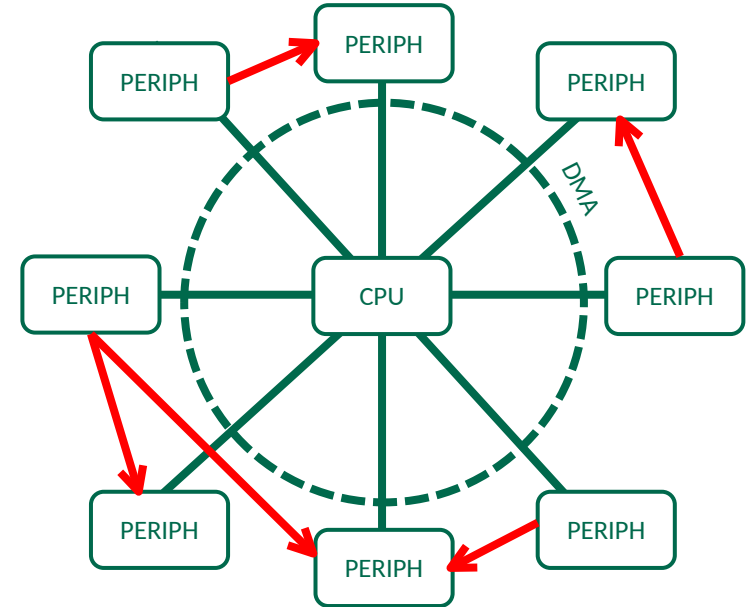
Interfaces are central

- Power SoC interfaces
- Software modules interfaces
- Communication protocols

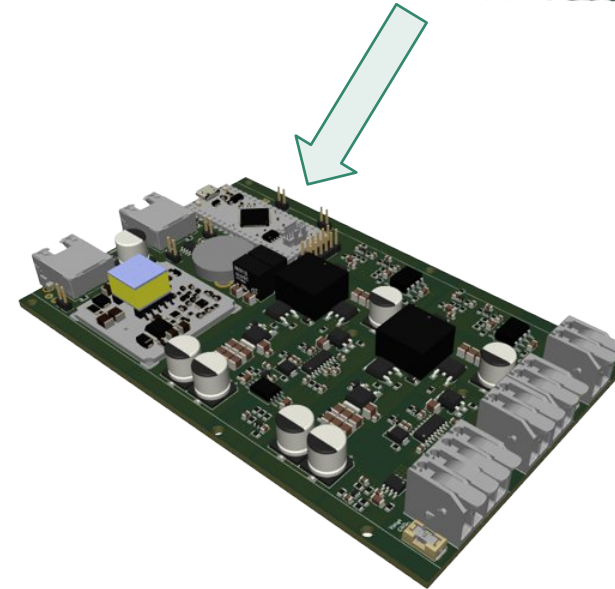
Everything is possible, but not always available



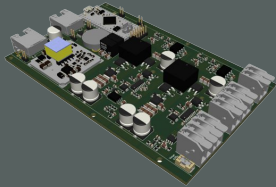
- Power electronics have a very niche need of combining CPU flexibility and hardware acceleration
- Manufactures have solutions, but they require bare-metal coding
- Interfaces needed by SDPE
 - **Peripheral-to-peripheral via DMA**
 - **Peripheral interconnection matrix**



- The problem is complex and the market fragmented
- It seems important to separate the brains from the muscles
- Dedicated board for the SoC
 - Feather footprint
 - Leverages highly specialized peripherals
- Dedicated board for power
 - 160mmx100mm footprint (Euroboard)



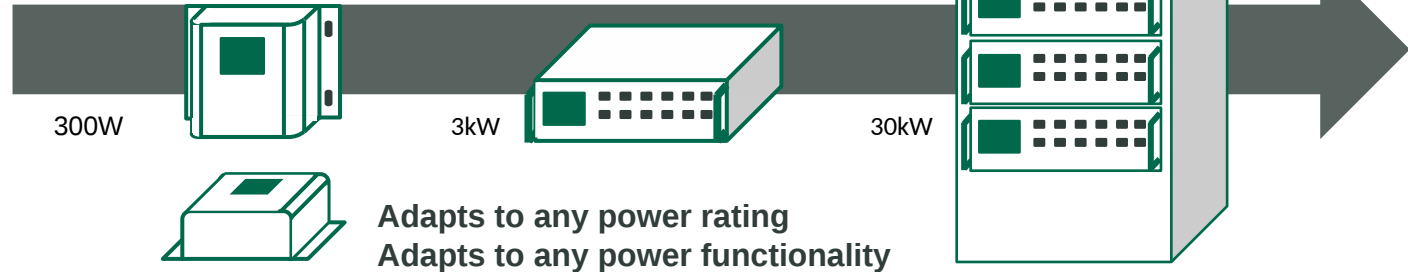
A standard module



- 300W per module
- Compact 100x100mm form factor
- Around 100€

As a stand alone module..

The same simple ergonomics.



Or in industrial 19" rack..

Conclusions - Great impact is possible !

