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# On-chip sample preparation and biosensing: Can porous silicon membranes do it all?

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**Abstract**—Porous silicon is a promising material for analytical biology, which has been used not only for biosensing but also for sample preparation in microfluidics. We therefore speculate that porous silicon membranes can be used to achieve all the functions involved in the analytical process on a single chip. However, integrating several membranes with the different characteristics required to implement these functions on-chip is challenging. In this work, we present a fabrication strategy for the monolithic integration of multiple membranes with tunable properties in planar microfluidics, thus paving the way towards the use of porous silicon to do it all, from sample preparation to biosensing.

## I. INTRODUCTION

Analysis of biological samples not only requires dedicated technologies to specifically identify and dose biomarkers of interest, but also steps to prepare the sample so that it is suitable for proper analysis. However integrating the sample preparation and biosensing functions into a single chip for point of care applications can be complicated and expensive because various technologies are usually used to perform these tasks [1]. An ingenious way to solve this issue and to simplify the chip design and fabrication is to use the same technology to perform all functions, as it has previously been proposed with silicon nanowires [2]. Porous silicon is a promising material for microfluidics [3] and biosensing applications [4], and membranes consisting of layers of different porosities have already been used to concomitantly filter and analyze biological samples [5], [6]. Porous silicon membranes are usually fabricated by anodization, which results in pores oriented perpendicular to the silicon wafer surface so that their on-chip implementation in a dead-end configuration leads to 3D fluidic systems [7]. To simplify the integration of porous silicon membranes into planar microfluidics, we have previously proposed a strategy for the fabrication of membranes with pores running parallel to the substrate, bridging microchannels lying in the same plane (Fig. 1). Preliminary results demonstrated that these lateral porous membranes can be used to performed various functions: size- and charge-based filtration, sample concentration and analytical detection by optical interferometry. One of the challenges for integrating all these functions on a single chip is to fabricate multiple membranes with tailored characteristics suited to perform each task. In this work, we present a fabrication process using a silicon-on-insulator (SOI) substrate, selective ion implantation, and metal electrode patterning to achieve this goal in a single electrochemical anodization step.

## II. FABRICATION OF LATERAL POROUS SILICON MEMBRANES

Porous silicon membranes, fabricated by anodization in a classical configuration (Fig. 2), exhibit vertical pores (*i.e.*, perpendicular to the substrate surface) since they form along the current flow. In order to enable the integration of such membranes within planar fluidics, we have proposed two fabrication processes, which produce lateral (*i.e.*, horizontal) porous silicon membranes, and that rely on (i) sandwiching a conductive silicon layer between two insulating layers and (ii) patterning an electrode on one side of a step created between two channels so that the injected current flows in a lateral direction during anodization (Fig. 2) [8].

### A. SOI process

The simplest way to have a silicon layer sandwiched between two insulators for lateral porous silicon membrane fabrication is to use a SOI wafer, where the conductivity of the device layer can be precisely tuned [9]. Following the process detailed in Fig. 3 (left), we have fabricated 10 $\mu$ m thick lateral mesoporous membranes with  $\approx$ 25nm diameter pores and  $\approx$ 50% porosity, bridging 20 $\mu$ m deep microchannels (Fig. 4).

### B. Ion implantation process

Another way to create conductive and insulating silicon layers is to modify the silicon doping by ion implantation [10]. Lateral porous silicon membranes were fabricated via the process illustrated in Fig. 3 (right), where the density of the anodization current was used to control the pore size ( $\approx$ 3–30 nm) and the membrane porosity ( $\approx$ 15–65%) (Fig. 4) [11].

## III. LATERAL POROUS SILICON MEMBRANES FOR SAMPLE PREPARATION

### A. Size-based filtration

The filtration capability of the lateral porous membrane was demonstrated using nanobeads and short molecules [9], [11], where experimental results showed the complete retention of 300nm beads, while the small molecules (single-stranded DNA and IgG) passed through the porous membrane (Fig. 5).

### B. Sample Concentration

Because of their small pore sizes and negatively charged surfaces, lateral porous membranes exhibit cation permselectivity [12]. As a results, they can be used in electrokinetic concentrators based on ion concentration polarization: for instance, we have achieved an estimated 100 fold preconcentration factor after 90s of accumulation of 100nM fluorescein in 0.1 $\times$  PBS (Fig. 6).

#### IV. LATERAL POROUS SILICON MEMBRANES FOR BIOCHEMICAL SENSING

Fourier transform infrared spectrometry was conducted on the implanted lateral porous silicon membranes used as interferometric sensors [13]. Fig. 7 shows the spectra obtained following the injection of different solvents. Fourier transform analysis was performed on these spectra to determine the refractive index of the filling liquids [14]. The sensitivity and detection limit of the interferometer was estimated to be  $\Delta\lambda/\Delta n \approx 156\text{nm}/\text{RIU}$  and  $2 \times 10^{-3}$  RIU, which are similar to those of conventional vertical porous membranes [15].

#### V. CAN LATERAL POROUS SILICON DO IT ALL?

##### A. Requirement for each function

The presented preliminary results indicate that porous silicon membranes are a good candidate to realize sample preparation and biosensing functions on the same chip (Fig. 8). To this aim, it is necessary to integrate various porous silicon elements of different morphologies to implement the different functions. Indeed, the use of membranes for biosensing requires the presence of large pores for their biofunctionalization, while to realize an efficient concentrator, smaller pores are desired.

##### B. Strategy for multiple membrane integration

Our strategy for the fabrication of membranes with different characteristics on a single chip relies on the combination of the two previously developed processes where the SOI substrate is used to provide the bottom insulation layer and ion implantation is used to locally manipulate the silicon resistivity to create porous elements with different morphologies in a single anodization step. Moreover, this approach enables the integration of both lateral porous silicon membranes and standard porous silicon layers on the same chip. The proposed process (Fig. 9) uses a SOI wafer with a highly doped p-type top layer ( $2\mu\text{m}$  thick,  $\approx 15\text{m}\Omega/\text{cm}$  resistivity). Photolithography is used to pattern a resist layer masking the silicon surface during subsequent implantation. Boron implantation is conducted to modify the silicon electrical conductivity. A silicon nitride layer that serves as the top insulating layer is then deposited. Plasma etching is used to create the microchannels and to form the silicon steps for the fabrication of lateral porous silicon membranes. Dry etching can also be used to open area into the box oxide layer to fabricate classical porous elements. A Cr/Au layer, to be used as the working electrode that injects the current parallel to the wafer surface during anodization, is sputtered and patterned. Finally, after anodization and electrode removal, sandblasting is used to form the inlet and outlet holes and the channels are encapsulated by anodic bonding a borofloat substrate. Fig. 10 shows SEM images of a fabricated chip integrating multiple membranes with various morphologies: pore diameters and porosities of  $\approx 25\text{nm}/50\text{nm}/35\text{nm}$  and  $\approx 80\%/90\%/65\%$  are obtained for the non-implanted lateral membrane, implanted lateral membrane and the classical vertical porous membrane, respectively.

#### VI. CONCLUDING REMARKS

A process based on the use of SOI substrates and selective ion implantation was developed for the fabrication, in a single

anodization step, of multiple porous silicon membranes with tunable morphologies on the same chip. This approach is foreseen to enable the integration of multiple membranes designed to perform the various functions dedicated to on-chip sample preparation and biosensing.

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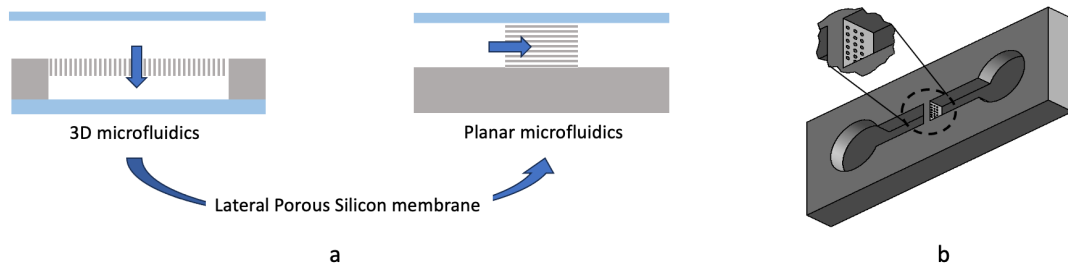


Fig. 1. Illustrations of the lateral porous silicon membrane integration into microfluidics. (a) Difference between a classical vertical porous silicon membrane in dead-end configuration integrated into a 3D microfluidic system and the proposed lateral porous silicon membrane integrated within planar microfluidics. (b) 3D schematics of the lateral porous silicon membrane in a microfluidic channel.

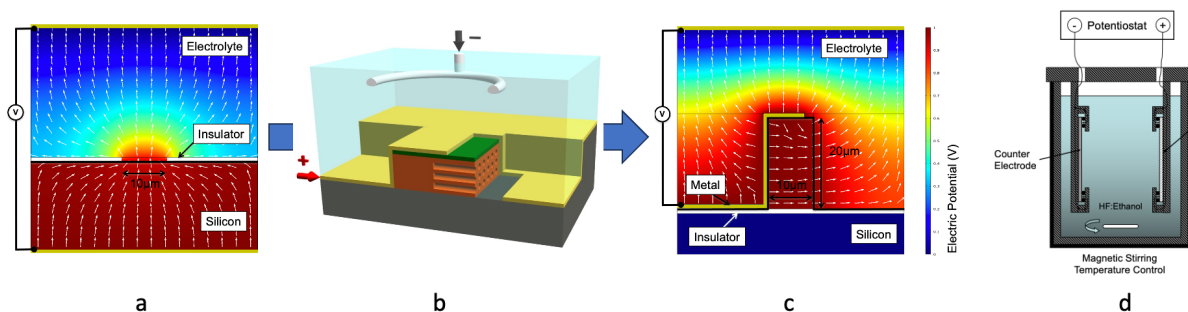


Fig. 2. Strategies for the fabrication of lateral porous silicon membranes. (a) COMSOL simulation showing the direction of the current flow during silicon anodization where the current is injected through the wafer backside, leading to the formation of vertical pores (classical configuration). (b) Schematics of the proposed strategy for the fabrication of lateral porous silicon membranes bridging two previously formed channels that requires sandwiching the membrane between two insulating layers and patterning an electrode to inject the current horizontally. (c) COMSOL simulation showing the horizontal direction of the current flowing through silicon to create lateral porous silicon membranes. (d) Schematics of a modified electrochemical cell to create lateral porous silicon membranes by injecting the current through the front side of a silicon wafer/chip.

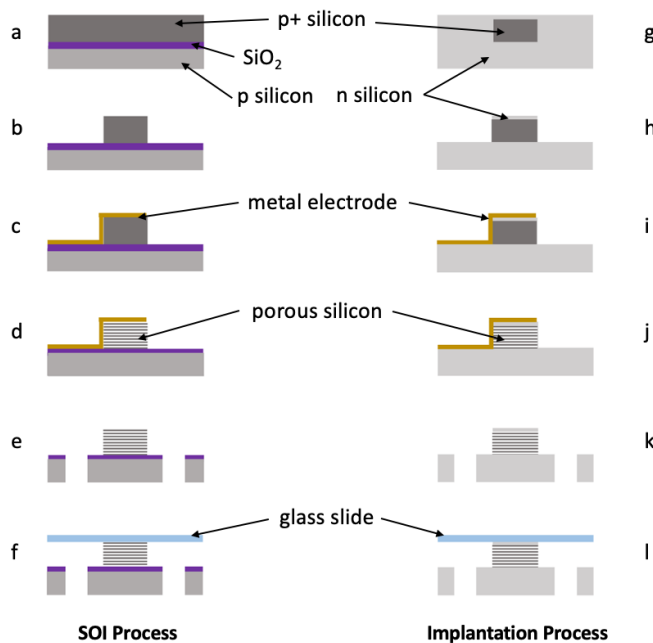


Fig. 3. The 2 processes developed for the fabrication of lateral porous silicon membranes, using an SOI substrate (left) or an implantation step (right). (a) SOI substrate, (g) boron and phosphorus implantation to create a p+ region at the membrane location, (b)/(h) dry etching microchannels, (c)/(i) electrode patterning, (d)/(j) silicon anodization in an HF electrolyte bath, (e)/(k) drilling inlet/outlet holes, (f)/(l) capping the membrane and fluidic channels with a borofloat substrate.

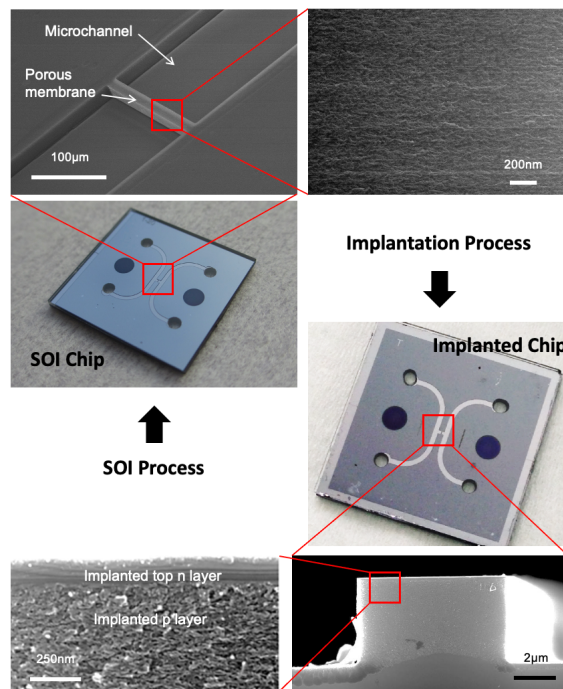


Fig. 4. Optical and SEM pictures of fabricated chips. Top: chip fabricated using the SOI process integrating a 10 $\mu$ m thick membrane. Bottom: chip fabricated using the implantation process integrating a 10 $\mu$ m thick membrane.

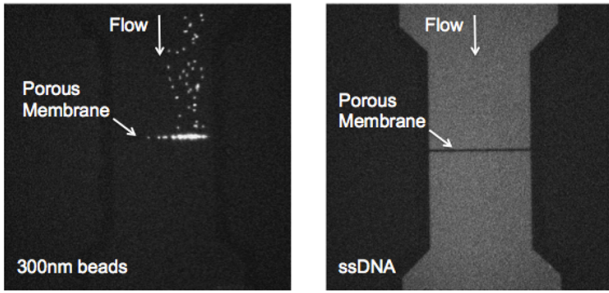


Fig. 5. Filtering capability of a lateral porous silicon membrane fabricated using the SOI process tested by flowing solutions of 300nm diameter nanobeads and short single-stranded DNA. The white arrows indicate the direction of the pressure-induced fluid flow. DNA molecules can flow back and forth through the membrane (right) unlike the nanobeads (left).

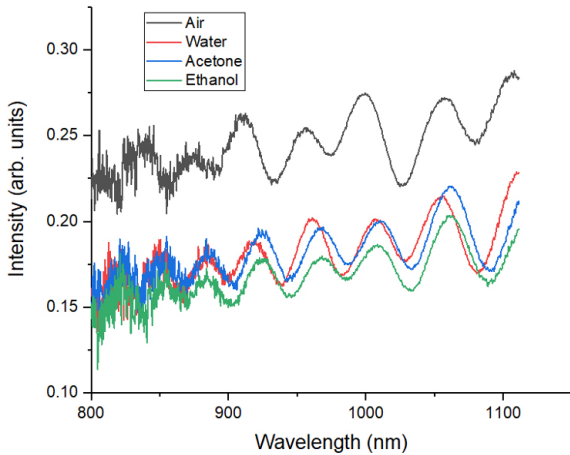


Fig. 7. Optical interferometry on a lateral porous silicon fabricated using the implantation process. Reflectance spectra recorded after filling the lateral porous silicon membrane with various solvents (water, acetone, ethanol). The spectrum marked as air means that no liquid fills the pores.

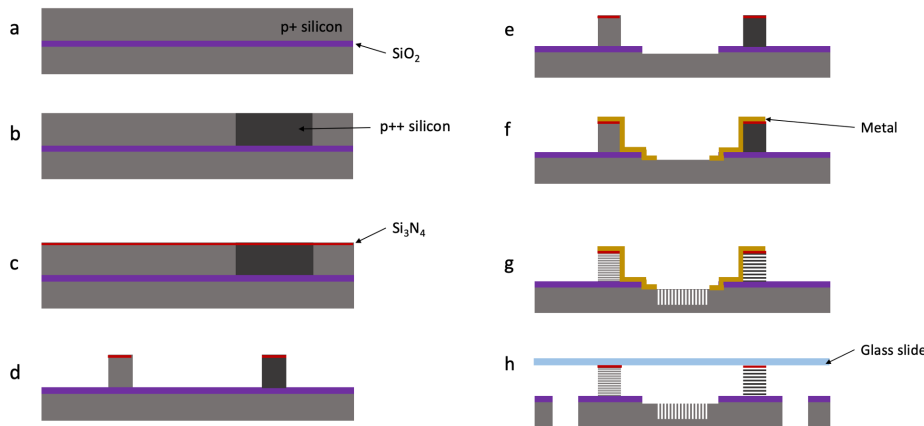


Fig. 9. Fabrication process developed for the integration of multiple membranes with various characteristics into a single chip. (a) Starting SOI substrate, (b) boron implantation to create the p++ highly doped silicon membranes, (c) deposition of a protective silicon nitride layer, (d) dry etching the microchannels, (e) etching the buried silicon dioxide layer where vertical porous silicon membrane is to be created, (f) patterning the metal electrode for current injection during anodization, (g) silicon anodization to fabricate porous silicon, (h) etching inlet/outlet holes and channel encapsulation with a borofloat substrate by anodic bonding.

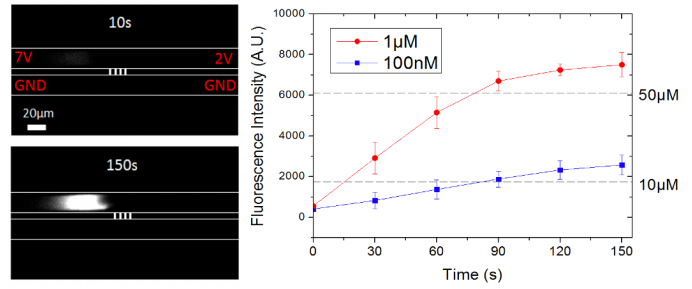


Fig. 6. Results of fluorescein concentration via ion concentration polarization using a lateral porous silicon membrane, fabricated with the SOI process and bridging two microchannels. Left: fluorescence images showing the increase of concentration of fluorescein as a function of time. The 100nM sample is introduced in the upper channel and is transported from left to right by electroosmotic flow. The porous silicon membrane is shown in the center of the image. Right: graph showing the increase of fluorescein concentration as a function of time for two sample concentrations (100nM and 1µM).

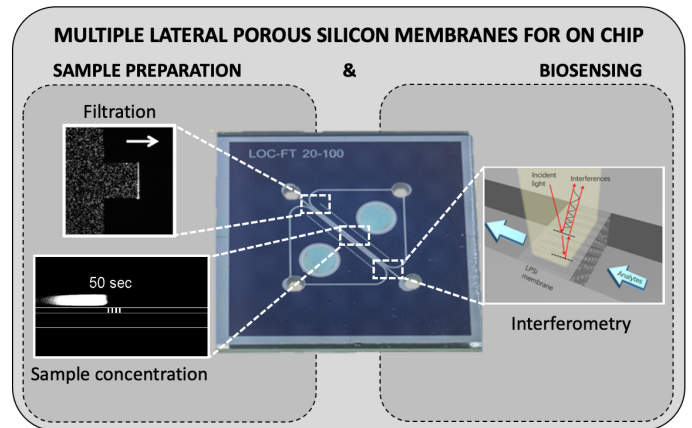


Fig. 8. Schematics illustrating the concept of the monolithic integration of sample preparation and biosensing on a microfluidic chip where porous silicon membranes can do it all.

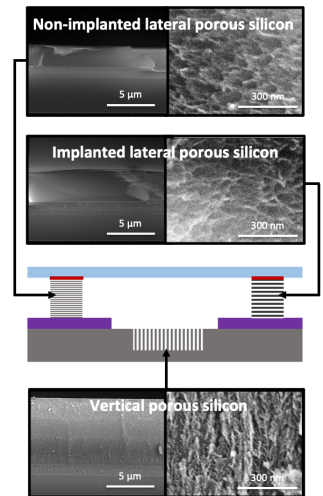


Fig. 10. Fabricated microfluidic chip integrating multiple porous silicon membranes displaying various characteristics (pore sizes and porosities).