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# An efficient Characterization Method to predict the Susceptibility of Integrated Circuits to Multitone Disturbance

A. Boyer, F. Caignet, M. Laidet

**Abstract**—With the growing concerns about safety of electronic equipment in complex electromagnetic environments, the characterization and prediction of integrated circuits (ICs) susceptibility to multitone disturbance become more and more urgent. This paper proposes an efficient method to characterize the response of an IC to multitone disturbance, based on a conventional continuous wave (CW) susceptibility test followed by a large-band injection test. The proposed test aims at verifying the application of the disturbance superposition principle of an IC terminal. If it applies, the risk of failure due to any combination of harmonic disturbances can be determined from the usual CW susceptibility test results. The only difference is that the RF synthesizer is replaced by an Arbitrary Waveform Generator in order to produce a comb signal composed of several equidistant harmonics with equal amplitude.

The paper presents the approach, the proposed indicators to test the disturbance superposition principle assessment and the validation results of the method applied to six different ICs, presenting different functions and technologies (op-amp, bandgap reference, DC-DC converter, digital gates, microcontroller I/O). In spite of the non-linear reaction of the tested IC to electromagnetic disturbance, the results show that the disturbance superposition principle applies as long as one failure mechanism is activated. The validation of this principle on an IC simplifies substantially the EMC risk assessment when the IC is exposed to a complex combination of harmonic disturbances, as demonstrated by the experimental results presented in this paper.

**Index Terms**—Integrated Circuit, Susceptibility, Multitone Disturbance, EMC Risk Assessment.

## I. INTRODUCTION

TESTING the susceptibility of electronic devices with multitone disturbance is not a recent idea and has mainly been proposed to accelerate radiated susceptibility tests [1] [2] [3]. With the growing complexity of electromagnetic (EM) environments and the increasing concerns about the functional safety of electronic equipment (e.g. for medical or automotive applications), questions about the EMI-risk assessment of electronic devices in a real environment arises recently [4] [5]. The susceptibility characterization of electronic circuits is usually based on the IEC62132 standard [6], which suggests the use of continuous wave (CW) signals. However, such excitation

signal is not sufficient to predict the risk of failure when they are exposed to more complex waveforms. Because of the non-linear behavior of ICs when their terminals are submitted to large voltage fluctuations, the prediction of the risk of failure from the susceptibility level to CW disturbance is not obvious. Besides, a practical problem is related to the cost and excessive duration of susceptibility tests to cover all the possible combinations of frequencies, amplitudes and phases of the tones forming the disturbance.

In spite of the major concerns for the final user safety, few research works have been devoted to this question and its theoretical foundation. [7] pointed out the risk to ignore the scenario of simultaneous exposure to several EM disturbance, but without the definition and evaluation of a generic test method. A first attempt was proposed in [8], which proposed an approach to test efficiently the impact of intermodulation products on electronic equipment susceptibility for dual-tone disturbance. The method was tested on the pin of a power high-side switch in [9]. Experiments presented in [10] showed that injecting two-tone interference is more appropriate for op-amp based-ICs than pure CW injection. [11] presented results of out-band two-tone injection test to desensitize RF receiver due to intermodulation product generation.

These different works focused only on the characterization of the effects of intermodulation in a two-tone disturbance scenario. Recently, [12] presents simulation results of the immunity of a voltage-controlled oscillator (VCO) submitted to two and three-tones disturbance, with constant amplitude, identical phase but randomly-selected frequencies. The results reveal that, depending on the failure criterion, the probability of failure is larger for single-tone than three-tones. In [13] and [14], the same authors propose a risk-based EMC analysis based on several probabilistic Bayesian network models applied to a VCO submitted to three-tone disturbance. The results highlight the causal dependence between the injected tones for this IC, which is extremely sensitive to intermodulation, complicating the EMI-risk assessment. However, the conclusion of these studies concerns only one type of IC and cannot be generalized to all types of ICs. Moreover, the proposed approach is still limited to a reduced number of tones because of the exponential increase of multitone combination

with the number of tones, without any consideration of a random selection of amplitude and phase. Furthermore, the prediction method does not provide general insight about how the different tones combine and how the IC reacts to this combination.

The objective of this paper is twofold. First, it aims at proposing an efficient characterization method of the susceptibility of an IC pin to multitone disturbance, without the risk of exponential increase of multitone combination. The main purpose is to characterize the nature of the response to simultaneous harmonic injection, and more specifically, to verify the disturbance superposition principle. The second purpose is to provide a method for EMC risk assessment to multitone disturbance, based only on CW susceptibility test results. Its application depends on the type of IC response to multitone disturbance and the verification of the disturbance superposition principle. The proposed approaches are tested on six different digital and analog ICs.

The paper is organized as follows: Section II introduces the disturbance superposition principle and defines the basis of an approach to test if this principle is verified. The large-band injection test bench, based on the injection of comb signal, is derived and proposed in Section III. The six case-studies are presented in Section IV. Their susceptibility levels to CW and large-band injection tests are presented in Sections V and VI. From the results of the large-band injection tests, a risk assessment to any combination of several tones with randomly-selected frequencies, amplitudes and phases is performed and compared with measurement results.

## II. PRINCIPLES OF A TEST TO QUALIFY IC MULTITONE SUSCEPTIBILITY

### A. Disturbance superposition principle

This study focuses on IC susceptibility when a multitone disturbance is coupled only on a single pin. This specific case is met for IC conducted susceptibility (CS) or near-field injection tests. The scenario of simultaneous coupling on several pins of the IC goes beyond the scope of this paper. Moreover, the same failure criterion is considered in CW and multitone susceptibility tests. The characteristics of the multitone disturbance (number of harmonics, frequencies, amplitudes and phases) are random but assumed stationary.

In a typical CW susceptibility test, the susceptibility threshold is determined for a list of frequencies  $f_k$ . For each frequency, a failure triggers if (1) is verified.  $E_k$  and  $S_k$  are the amplitude of the applied disturbance and the susceptibility threshold respectively. They are usually expressed in terms of average power in typical CS test such as Direct Power Injection (DPI) test [15], but they can also be expressed in terms of voltage. The unitless ratio  $I_k$  is called interference coefficient and determines if a sine-wave disturbance has a sufficient amplitude to trigger a failure.

$$I_k = \frac{E_k}{S_k} = 1 \quad (1)$$

Determining multitone susceptibility is an extremely important question to assess EMI risk when the device under test (DUT) will be exposed to complex EM disturbance. It

consists in finding the response of the device under test (DUT) to the superposition of several harmonic disturbances applied simultaneously, with frequencies, amplitudes and phases chosen randomly. The main issue is that the actual effect of the combination of each applied harmonic is not straightforward due to the non-linear response of the IC pin. Intermodulation can arise, leading to additional harmonics. Moreover, as explained in [13], the superposition of the different harmonics may lead to synergetic or inhibited interactions. The failure threshold to a multitone disturbance is not only the sum of the different contributions of the different harmonics and a complex process must be developed to extract the interactions between the harmonic contributions. However, these particular cases are not met for every IC and it can be useful to detect the simple case where the failure results from the linear superposition of the contribution of each harmonic. If this principle (called disturbance superposition principle in this paper) is met, the susceptibility level to multitone disturbance can be extrapolated from the CW susceptibility level. The scope of this paper is to determine a simple method and indicator to detect if an IC satisfies this principle and shows that the EMI risk assessment to complex EM disturbance can be done.

Let consider a multitone disturbance composed of  $N$  harmonics with frequencies  $f_k$  and amplitude  $E_k$ ,  $k \in [1; N]$ . The disturbance superposition principle is verified if (2) is met when the failure arises.  $S_k$  is the susceptibility threshold of the DUT to CW disturbance at a frequency  $f_k$ .  $I_{tot}$  is the total interference coefficient. The impact of each harmonic is weighted by the CW susceptibility threshold in order to account for the susceptibility of the IC at frequency  $f_k$ . In this case, the risk of failure can be determined from the CW susceptibility test results and the amplitude of the different harmonics forming the multitone disturbance.

$$I_{tot} = \sum_{k=1}^N I_k = \sum_{k=1}^N \frac{E_k}{S_k} = 1 \quad (2)$$

If a failure arises for  $I_{tot} > 1$ , inhibited interactions exist between the different harmonics, that tend to counterbalance their individual contributions. In contrary, if it happens for  $I_{tot} < 1$ , synergetic interactions exist and intensify the impact of each harmonic. In both cases, the disturbance superposition principle cannot be used to determine the multitone susceptibility only from CW susceptibility test results.

### B. Identification of the disturbance superposition principle

In order to assess the disturbance superposition principle application, a particularly interesting multitone signal is the comb signal. This signal is composed of  $N$  in-phase harmonics with identical amplitude, ranging from  $F_1 = N_1 \times F_0$  and  $F_2 = N_2 \times F_0$  with  $N_2 - N_1 + 1 = N$  and  $F_0$  the frequency gap between each harmonic given by (3). With this property, the sensitivity of the IC over a frequency range is tested equally and rapidly. Injecting a large number of equally-spaced harmonics ensures a fine frequency sampling of the tested range, avoiding the risk to miss sensitive frequencies. Finally, injecting in-phase harmonics optimizes the peak amplitude of the resulting disturbance.

The average and peak powers of the signal are given by (4)

and (5), where  $P_{\text{harmono}}$  is the average power per harmonic expressed in dB. The crest factor  $CF$  is defined by (6). Ideally, increasing  $N$  will improve the frequency resolution of the test or enlarge the tested frequency range. However,  $N$  is limited in practice by the RF power amplifier ratings because of the large crest factor of the comb signal. Increasing  $N$  leads to a saturation of the amplifier due to then excessive peak power, even if  $P_{\text{harmono}}$  remains too low to disturb the IC. Thus, the choice of  $N$  and the covered range must be done according to the power amplifier ratings and the maximum power to apply on the DUT.

$$F_0 = \frac{F_2 - F_1}{N - 1} \quad (3)$$

$$P_{\text{avg}}(\text{dB}) = 10\log\left(\sum_{k=1}^N P_k\right) = P_{\text{harmono}} + 10\log(N) \quad (4)$$

$$P_{\text{peak}}(\text{dB}) = P_{\text{harmono}} + 20\log(N) + 3 \quad (5)$$

$$CF(\text{dB}) = P_{\text{peak}} - P_{\text{avg}} = 10\log(N) + 3 \quad (6)$$

Let analyze the consequences of the verification of the disturbance superposition principle when a comb signal is injected. First, let consider that the terms  $E_k$  and  $S_k$  of (2) are given in average power and denoted  $P_{E_k}$  and  $P_{S_k}$ . As the average power per harmonic  $P_{E_k}$  is constant and equal to  $P_E$ , the failure arises when the average power per harmonic  $P_E$  is given by (7). The average power  $P_{E_{\text{avg}}}$  of the comb signal is given by (8). It is actually equal to the harmonic mean of the CW susceptibility level measured over the different harmonics forming the comb signal. If  $N$  becomes large enough,  $P_{E_{\text{avg}}}$  tends to the harmonic mean of the CW susceptibility over the tested range. In other words, the failure arises for a constant average power. This is the signature of a failure mode dependent on the average power of the multitone disturbance.

$$P_E = \left(\sum_{k=1}^N \frac{1}{P_{S_k}}\right)^{-1} \quad (7)$$

$$P_{E_{\text{avg}}} = N \cdot P_E = N \left(\sum_{k=1}^N \frac{1}{P_{S_k}}\right)^{-1} \quad (8)$$

Secondly, let consider that the terms  $E_k$  and  $S_k$  of (2) are expressed in voltage amplitude and denoted  $V_{E_k}$  and  $V_{S_k}$ . As the voltage per harmonic  $V_{E_k}$  is constant and equal to  $V_E$ , the failure arises when  $V_E$  is given by (9). The peak voltage  $V_{E_{\text{peak}}}$  of the comb signal is given by (10). It is actually equal to the harmonic mean of the CW susceptibility level, given in voltage, measured over the different harmonics forming the comb signal.

$$V_E = \left(\sum_{k=1}^N \frac{1}{V_{S_k}}\right)^{-1} \quad (9)$$

$$V_{E_{\text{peak}}} = N \cdot V_E = N \left(\sum_{k=1}^N \frac{1}{V_{S_k}}\right)^{-1} \quad (10)$$

If  $N$  becomes large enough,  $V_{E_{\text{peak}}}$  tends to the harmonic mean of the CW susceptibility level over the tested range. In other words, the failure arises for a constant peak voltage. As the amplitude is usually measured with a power meter in susceptibility test, the failure arises for a constant peak power. This is the signature of a failure mode dependent on the peak power of the multitone disturbance.

### C. Approach to verify the disturbance superposition principle

The previous properties can be reused to define a test to verify (i) if the tested IC fulfills the disturbance superposition principle over a given frequency range and (ii) if the failure arises for a constant average power or a constant peak power, which changes the definition of the interference coefficient.

The test consists in injecting a comb signal that covers a given frequency range with different values of frequency steps  $F_0$  or different values of  $N$ . The susceptibility level is recorded for each value of  $N$ . The average power of the disturbance is directly measured (e.g. by a power meter) and the peak power is computed according to (5) since the injected harmonics are in-phase. Three scenarios can appear:

- If failure arises for nearly the same average power whatever the value of  $N$ , the disturbance superposition principle applies for the tested frequency range and the failure depends on the average power of the incoming disturbance. When exposed to any combination of multitone disturbance covering this frequency range, the IC fails if the total interference coefficient defined by (11) is equal to 1, where the terms  $P_{E_k}$  are the average powers of the different harmonics composing the multitone disturbance and  $P_{S_k}$  the CW susceptibility level.

$$I_{\text{tot}} = \sum_{k=1}^N \frac{P_{E_k}}{P_{S_k}} = 1 \quad (11)$$

- If failure arises for nearly the same peak power whatever the value of  $N$ , the disturbance superposition principle applies for the tested frequency range and the failure depends on the peak power or voltage of the incoming disturbance. When exposed to any combination of multitone disturbance covering this frequency range, the IC fails if the total interference coefficient defined by (12) is equal to 1.

$$I_{\text{tot}} = \sum_{k=1}^N \sqrt{\frac{P_{E_k}}{P_{S_k}}} = 1 \quad (12)$$

- If the failure triggers for non-constant average and peak powers when  $N$  is changed, the disturbance superposition principle is not verified for the tested frequency range. The susceptibility level to a multitone disturbance cannot be determined from (11) or (12).

## III. IMPLEMENTATION OF THE DISTURBANCE SUPERPOSITION VERIFICATION TEST

### A. Large-band injection chain

In order to verify the disturbance superposition principle of an IC and the dependence to the average or peak power of the incoming disturbance, the large-band injection chain described in Fig. 1 is proposed. It reuses the same elements of typical CW susceptibility test bench, except the RF disturbance generator. A comb signal is synthesized by either a frequency multiplier [16] or an arbitrary waveform generator (AWG). This type of generator offers a more convenient technique to control the frequency range of the disturbance and the polarity of the synthesized pulse. The comb generator is followed by an RF power amplifier, whose input may be protected by an attenuator to prevent saturation due to an excessive peak power. The directional coupler is connected to the RF power meter in order to acquire and control the average and peak power of the comb signal. The reflected wave can also be monitored by a spectrum analyzer in order to measure the new harmonics produced by the distortion due to the non-linear behavior of the tested IC pin.

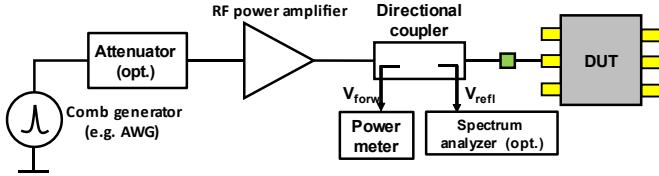


Fig. 1. Large-band injection chain to characterize the susceptibility of IC pin to multitone disturbance.

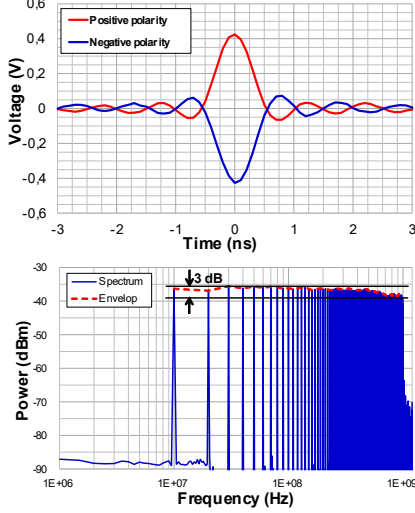


Fig. 2. Time-domain profile (top) and spectrum (bottom) of the large-band signal generated by the AWG.

In this study, the Anritsu AWG701B arbitrary waveform generator, with a 4.2 GS/s sampling frequency and a 3-dB bandwidth of 1.1 GHz, is used. Fig. 2 shows the transient profile and spectrum of the synthesized comb signal which covers the range 10 – 1000 MHz ( $F_0 = 10$  MHz,  $N = 100$ ). The time-domain profile of the signal is shown for both positive and negative polarities, exhibiting an excellent symmetry. The spectrum is relatively flat, with a variation which does not exceed 3 dB. This variation is due to the non-flat frequency response of the output amplifier of the AWG. Other sources of variation will affect the flatness of the spectrum of the comb signal that reaches the tested IC pin, e.g. the power amplifier gain, the coupling factor of the directional coupler and the cable attenuation. All of these parameters must be characterized in order to compensate their effect in the evaluation of  $I_{tot}$ .

### B. Characterization flow

The methodology to test the validity of the disturbance superposition principle on a test IC is summarized in Fig. 3. It is divided in four main steps. The first step consists in performing the susceptibility test with CW disturbance. The CW susceptibility level is not only measured, but the different failure modes are also detected. If several failure modes are mixed over all the test frequency range, the prediction of susceptibility to multitone disturbance from CW disturbance will be complicated, since several failure modes could be activated simultaneously, contrary to the CW test.

In the second step, the test frequency range is divided in several subranges. As mentioned in Section II.B, it is necessary to avoid the limitations due to an excessive crest factor of the comb signal. It is recommended to generate a comb signal that

covers only one frequency decade, with a maximum of several tens of harmonics in this frequency range. Moreover, the division of the test frequency range can be made according to the failure modes detected during the first step. Comb signals could be generated to cover frequency ranges where only one failure mode dominates, in order to assess the disturbance superposition principle for each failure mode.

For each test frequency range, the number of harmonics  $N$  (or frequency gap  $F_0$ ) has to be defined. The large-band susceptibility test must be repeated for different values of  $N$  (e.g. three values) to test the validity of the disturbance superposition principle. In order to limit the overall duration of the experiments, three different values of  $N$  are defined for each test frequency range. Once again,  $N$  should not exceed some tens to avoid saturation of the RF power amplifier.

Once the comb signal parameters have been defined, the large-band injection tests are performed, using the same failure criteria definition as for the CW susceptibility tests. The average and peak forward powers are measured when a failure is triggered. The tests are also done with positive and negative pulses. In the last step, the large-band test results are processed. For each test frequency range, the average and peak powers measured at the failure level are compared for the different values of  $N$ . If the failure arises for a nearly constant average power, the disturbance superposition principle is verified and  $I_{tot}$  is determined from (11). If the failure arises for a nearly constant peak power, the disturbance superposition principle is also verified and  $I_{tot}$  is evaluated from (12). In both cases, the EMI risk assessment in complex disturbance scenario is simplified: the risk of failure of the tested IC pin to any combination of multitone disturbance covering the tested frequency range can be determined according to (11) or (12), knowing the amplitude of the different harmonics forming the incoming disturbance.

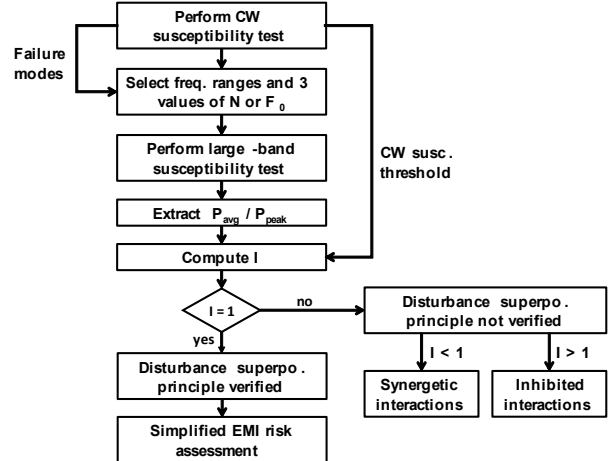


Fig. 3. Characterization flow to test the validity of the disturbance superposition principle.

## IV. PRESENTATION OF THE CASE STUDIES

Six commercial ICs have been selected as case studies in order to verify and test the limits of the disturbance superposition principle and the proposed method to assess it. They are listed in Table I with their main characteristics and the

failure criteria defined for the susceptibility tests. Although is not exhaustive, it offers a relatively large panel of typical and basic electronic functions built with different technologies. Moreover, the non-linear response of an IC to EM disturbance may compromise the prediction of the IC response to a combination of harmonic disturbance based only on a simple superposition of the individual effect of each harmonic. Selecting ICs with different failure modes ensures a robust test to verify the relevance of the disturbance superposition principle.

Three ICs are analog op-amp based circuits (LT1796, LMV651 and LM22677). The same failure criterion is defined: the EMI-induced DC offset which is a common failure mode in analog components [17]. This non-linear phenomenon offers a particularly interesting case to test the disturbance superposition principle. The three other case studies are digital circuits, with different failure modes. The disturbance is injected on unidirectional digital input pins. For AHCT04 and STM32, the failure criterion is a bit flip and the detection of an excessive jitter for 74FCT245. As the STM32 is a complex ICs, its overall operation is also checked during the susceptibility tests since the internal coupling of the incoming disturbance may affect the operation of other blocks of the MCU. Contrary to the three tested analog ICs, the tested digital ICs also constitute interesting case studies because of the presence of ESD protections which may trigger when the EM disturbances are applied and induce another type of non-linearity. For the three cases, an on-chip power and a ground clamps are connected to the tested digital inputs.

TABLE I  
DESCRIPTION OF THE CASE STUDIES

Reference	Description	Tested pin	Failure criteria
LT1798	Bandgap voltage reference	Power supply	Output voltage offset (20 mV)
LMV651	Op-amp	Non-inverting input	Output voltage offset (20 mV)
LM22677	Step-down DC-DC converter (12 V to 5 V)	Feedback input	Output voltage offset (10 mV)
AHCT04	CMOS inverter	Digital input	Bit flip
FCT245	8-bit CMOS transceivers	Digital input	Excessive jitter (25 ns)
STM32F030	32-bit microcontroller	Digital input	Bit flip and CPU operation

The same experimental set-up and failure criteria are applied for CW and large-band susceptibility tests. For all the case studies, except the LM22677, CS tests are performed according to the DPI standard. This method consists in applying the RF disturbance to an IC pin through a bias tee and ensures an excellent repeatability, which is estimated experimentally to less than 1 dB. The repeatability depends on the tested IC, the failure mode and the failure detection method. For the LM22677, near-field scan injection (NFSI) test [18] is performed as most of the I/O pins of the IC were not accessible for conducted injection on the test board. The NFSI test consists in placing a miniature near-field probe above the IC under test to create a local disturbance and detect the main sensitive pins.

For the LM22677, the NFSI test shows that the IC is sensitive to EM disturbance coupled on the feedback input pin. NFSI tests are performed with a home-made H-field probe designed on a semi-rigid coaxial cable and formed by a 5 mm loop.

These six ICs are mounted on different test boards. All the susceptibility tests were performed between 10 MHz and 1 GHz. The forward power is limited to 35 dBm during the DPI tests, and 45 dBm during NFSI tests. The susceptibility levels are given in terms of forward power measured by a power meter through a bidirectional coupler.

## V. CONTINUOUS-WAVE SUSCEPTIBILITY TEST RESULTS

Fig. 4 presents the measured susceptibility threshold of the six tested IC to CW disturbance (curve Threshold), i.e. the susceptibility limit to CW disturbance measured for each tested frequency. The disturbance amplitude is increased from a small level until the limit is found. This limit is reached either when predefined failures are triggered (points marked Failure) or when the DPI or NFSI test limit is reached (points marked No Failure). For some ICs, different failure modes appear and are marked on each graph (e.g. Failure 1, Failure 2). The susceptibility limit is given in term of forward power measured by a power meter connected to a directional coupler. The overall measurement time depends on the number of tested frequencies, dwell time and limit search algorithm. For 50 frequency points, it may range between 25 and 50 minutes.

The six measured CW susceptibility thresholds exhibit large differences, which are explained by the differences between the tested ICs in terms of functionalities, internal design, power supply, internal RF impedance, and the different PCBs. However, this huge variety of susceptibility curves constitutes an interesting test bench to evaluate the proposed methodology to test the disturbance superposition principle and its limits. The bandgap reference LT1798 (Fig. 4-a) is susceptible only in the range 100 – 1000 MHz, where a negative offset is induced systematically. The op-amp LMV651 (Fig. 4-b) fails between 10 and 1000 MHz, but exhibits clearly two different failure modes according to the frequency range. The failure mode 1 dominates up to 110 MHz and consists in a positive offset due to the slew rate asymmetry as explained in [19]. When the frequency increases, failure mode 1 disappears and a second failure mode dominates above 110 MHz. The failure mode 2 is associated to a negative offset due to the weak distortion provided by the differential pair. The step-down converter LM22667 (Fig. 4-c) is susceptible only above 200 MHz with a unique failure mode (a positive offset).

The CMOS inverter is susceptible up to 575 MHz (Fig. 4-d). Bit flip arises only when the disturbance superimposes to a digital signal input at logical low level. The transceiver FCT245 exhibits two distinct failure modes (Fig. 4-e). Up to 150 MHz (Failure 1), CW disturbance leads to jitter and glitch at the low to high level transition. Above this frequency, the second failure mode (Failure 2) progressively replaces the failure mode 1, with a completely different effect on signal integrity: the high-level voltage decreases while and the rise time increases with the disturbance amplitude, proving that not only the input buffer, but also the IC output buffer is affected by the EM disturbance.

The MCU STM32 shows a more complex behavior (Fig. 4-f). Up to 300 MHz, EM disturbance applied to the digital input pin lead to a bit flip. Above this frequency, the immunity level increases rapidly because of the low-pass filtering effect of the input buffer and a second failure mode appears between 300 and 450 MHz. This failure mode is not associated to the I/O

buffer since the EM disturbance leads to complete crash of the CPU, which needs a hardware reset to restart. Above 450 MHz, a third failure mode related to an instability of the CPU clock appears. It suggests that this failure is due to the noise coupled on power supplies which disturbs the clock generation module of the MCU.

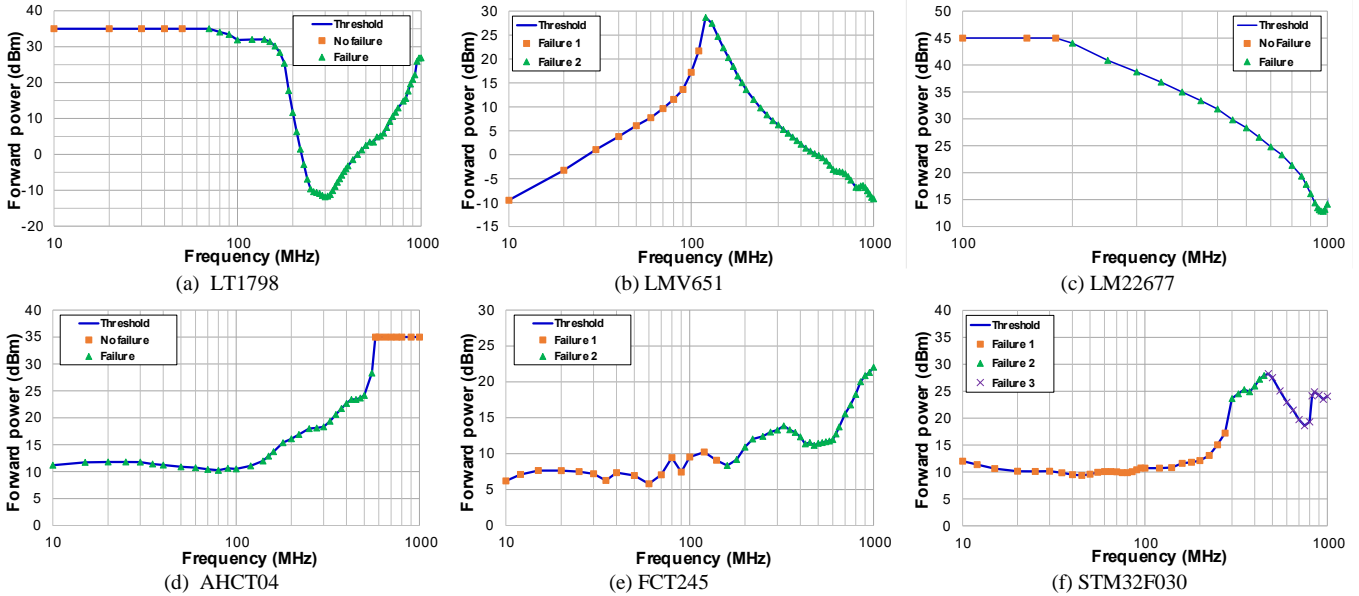


Fig. 4. CW susceptibility level of the circuits.

VI. LARGE-BAND SUSCEPTIBILITY TEST RESULTS

The procedure described in Section III.B is applied for the six tested ICs. The test frequency ranges for the comb signal were set according to the CW susceptibility test, in order to cover a half or a complete decade, or a frequency range where a particular failure mode dominates. For each frequency range, three values of  $N$  or frequency gap  $F_0$  have been selected to verify if the observed failure depends on the average or peak

power of the disturbance and if the disturbance superposition applies. The average power of the incoming comb signal disturbance is measured with the power meter connected to the directional coupler, as shown in Fig. 1, when the tested IC fails. The peak power is deduced according to (5). Then, the coefficient  $I_{tot}$  is computed from the measured CW susceptibility threshold (refer to Section V) according to (11) or (12), depending if the failure arises for a constant average or peak power.

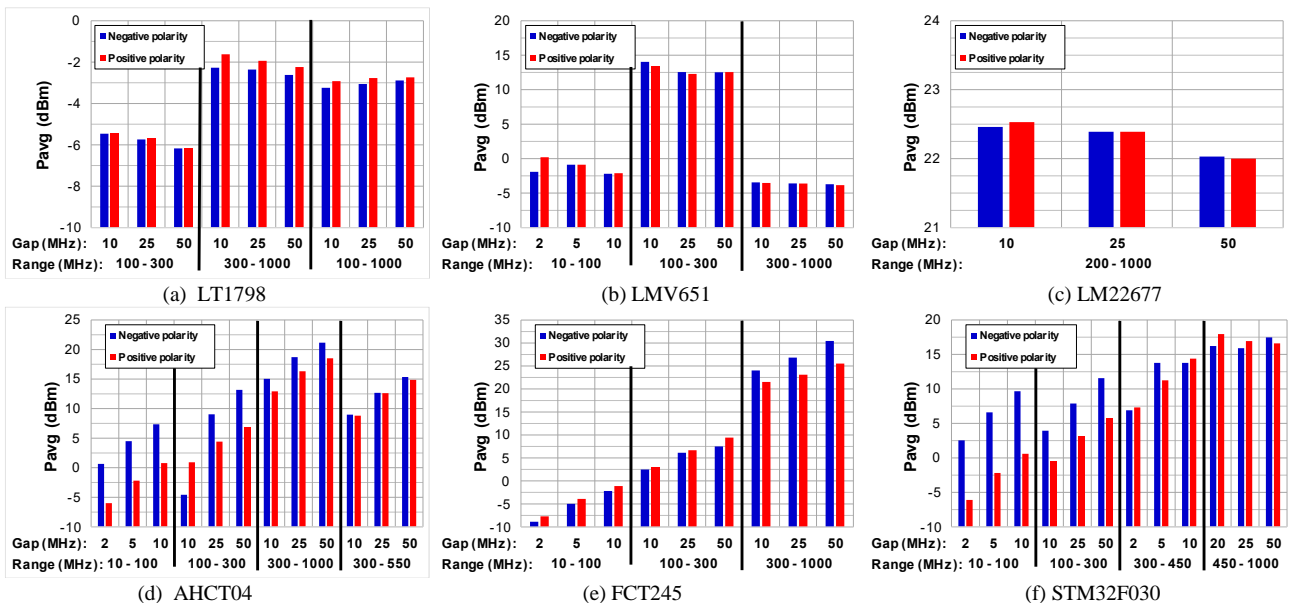


Fig. 5. Average power required to induce a failure during large-band susceptibility test, vs. frequency ranges and steps.

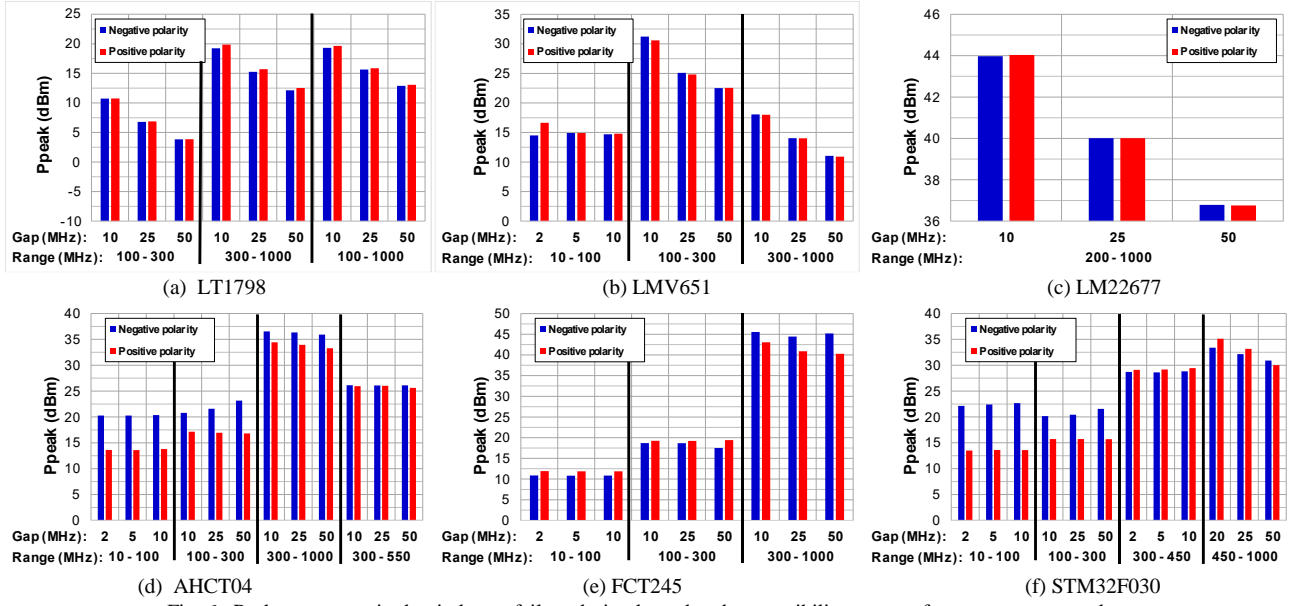


Fig. 6. Peak power required to induce a failure during large-band susceptibility test, vs. frequency ranges and steps.

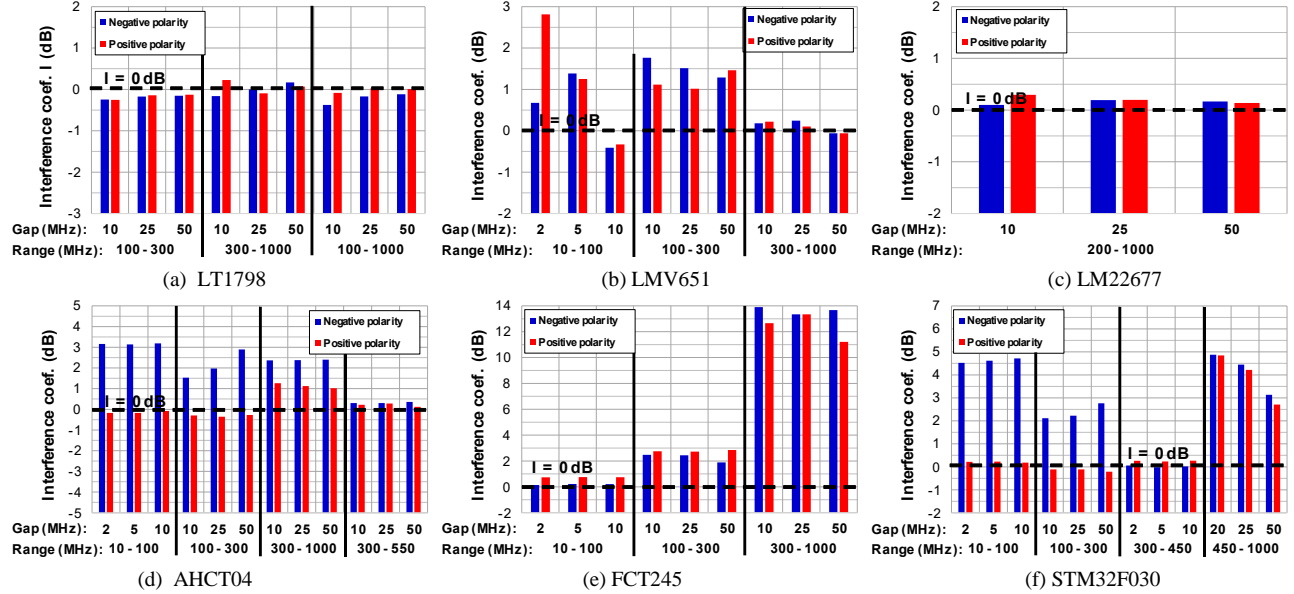


Fig. 7. Interference coefficient of the tested circuits to comb signal vs. frequency ranges and steps First row:  $I_{tot}$  based on (10). Second row:  $I_{tot}$  based on (11).

The results are summarized on Figs. 5, 6 and 7, which show the average and peak powers and  $I_{tot}$  when the failure arises for the different test frequency ranges and values of  $N$  or  $F_0$ . The test is done for positive and negative polarity of the comb signal. A common observation is that there is a clear link between the CW susceptibility threshold and the average or peak power measured at the failure level in the large-band test. Results are detailed in the following paragraphs, with a distinction between the analog and digital ICs.

### A. Results on Analog ICs

Large-band injections were applied on the LT1798 with a comb signal ranging between 10 and 100 MHz, but no failures were detected. This result is in accordance with CW test results. The large-band tests made above 100 MHz proves that the failure triggers for constant average power whatever the pulse polarity (Fig. 5-a). The disturbance superposition principle

applies for this IC as proved by  $I_{tot}$  which is close to 0 dB (Fig. 7-a). The gap with the theoretical value of 0 dB is less than the DPI test bench repeatability (1 dB). No distortion of the incoming disturbance has been detected by the spectrum analysis of the reflected wave. Similar results are obtained with the step-down converter LM22677. The tests have only been done between 200 and 1000 MHz because the power amplifier reached saturation before the failure was triggered below 200 MHz.

However, the results are less simple for the op-amp LMV651. On the range 300 – 1000 MHz, only the failure mode due to the weak distortion provided by the differential input is activated. As the failure triggers for a constant average power with  $I_{tot}$  close to 0 dB (Fig. 7-b), the disturbance superposition is verified for this range. This is not true for the ranges 10 – 100 MHz and 100 – 300 MHz. The incoming disturbance is not distorted, but both failure modes are activated simultaneously

and have opposite effects on the output offset. This partial compensation effect is also suggested by  $I_{tot}$  larger than 0 dB. This case illustrates a limitation of the initial assumption. It cannot be applied if several failure modes are activated simultaneously on a frequency range and if their interaction remains unknown. Moreover, the individual CW susceptibility threshold of each failure mechanism cannot be determined, so that  $I_{tot}$  is necessarily overestimated.

Despite that, the results obtained on these three analog ICs prove that, even if the failure results of a non-linear operation, the disturbance superposition principle can apply. The results also suggest that this principle is verified for failures due to the weak distortion provided by op-amp differential pairs. The generation of a DC offset is related to the average power of the disturbance, as suggested also in [10]. This principle could certainly be observed on other op-amp based ICs.

### B. Results on Digital ICs

Contrary to the previous ICs, the inverter AHCT04 fails for a constant peak power (Fig. 6-d). The disturbance superposition defined by (12) is verified for positive polarity over all the frequency ranges (Fig. 7-d), except for 300 – 1000 MHz since no failures were detected above 575 MHz during the CW susceptibility test.  $I_{tot}$  is obviously overestimated without the exact values of the CW susceptibility threshold. The results also suggest that the IC input is more sensitive to positive polarity pulses. CW test results show that failures are observed only when the disturbance is superimposed to a logical low level. This difference is explained by the asymmetrical switching level of the inverter. A last interesting observation is provided by the spectral analysis of the reflected wave during the CW test, which shows intermodulation products when failure occurs due to the IC internal ESD protection activation. These distortions appear in large-band test only for negative pulses, but not for positive pulses. For this polarity, the bit-flip failure is triggered without ESD protection clamps resulting in a nearly invariant impedance. Once again, although the IC input has not a purely linear electrical behavior, the disturbance superposition principle can apply.

The transceiver FCT245 exhibits a similar behavior than the AHCT04 on the range 10 – 100 MHz but with a similar sensitivity to positive and negative pulses (Fig. 6-e). However, although the failure arises for a nearly constant peak power, the disturbance superposition is not verified above 100 MHz because of the simultaneous activation of a second failure mechanism, which is not only related to the input buffer (Fig. 7-e). Both failure mechanisms tend to compensate each other, as suggested by  $I_{tot}$  larger than 0 dB when the failure criterion is reached.

The failure criteria applied to the STM32 and AHCT04 input buffers are identical and a similar behavior is observed up to 300 MHz. However, the failure above 300 MHz is not linked to the input buffer as suggested by the CW test results. Between 300 and 450 MHz, the injection of a comb signal leads also to a complete failure of the CPU. Experimental results prove that this failure also triggers for a constant peak power for both

polarities (Fig. 6-f) and complies with the disturbance superposition principle (Fig. 7-f). Above 450 MHz, the comb signal leads to an instability of the CPU clock. Contrary to the two other failure modes, the disturbance superposition principle does not apply for this failure (Fig. 7-f). Several failure mechanisms may be implied but, because of the complexity of the MCU, the identification of the internal blocks responsible of this failure remains difficult.

Similarly to the tested analog ICs, the results show that the disturbance superposition principle can apply even if the failure results of a non-linear operation. The proposed method succeeds in identifying IC, failure modes and frequency ranges where this principle can apply. The results also suggest that disturbance superposition principle is verified for digital input buffers and bit flip or jitter related failures, so that it may be certainly verified for other digital ICs.

## VII. RISK ASSESSMENT TO MULTITONE DISTURBANCE

The large-band injection tests show that the disturbance superposition applies on various frequency ranges for the six case studies. The susceptibility to multitone disturbance, consisting of any combinations of harmonic signals covering these ranges, can be evaluated. If the amplitudes of the harmonics forming the multitone disturbance are provided, the risk of failure can be assessed by evaluating  $I_{tot}$  from the CW susceptibility level according to (11) or (12). In order to validate this risk assessment, the large-band injection setup is reused to disturb the six tested ICs with multitone disturbance with 30 randomly selected frequency, amplitude and phase values. The frequencies are chosen on the ranges where the disturbance superposition applies. The amplitude and phase values are randomly sampled between 0 and 2 and between 0 and  $2\pi$  respectively, with default values equal to 2 and 0. For sake of simplicity, the number of tones  $N$  is limited to 3, but the tests were also done with 5 and 7 tones and led to the same conclusions. For each test, the amplitude of the disturbance is increased until the failure arises and  $I_{tot}$  is computed.

The experimental results are summarized in Figs. 8 to 10. Fig. 8 shows the distribution of the computed  $I_{tot}$  when only the tone frequencies are randomly selected. Figs. 9 and 10 also show the distribution of  $I_{tot}$  but for randomly selected phases and amplitudes. The tone frequencies remain constant during the tests, but their selection is also random. Except for the random selection of the phase for digital ICs, all the distributions are nearly centered around 0 dB, with a deviation which does not exceed 1 dB, i.e. the estimated repeatability of the susceptibility test bench. The distributions may change between the tested ICs because the variability depends mainly on the failure definition and the detection method. These results confirm that, if the disturbance superposition applies, the risk of failure due to multitone disturbance is correctly evaluated from the CW susceptibility threshold and the amplitudes of the injected tones.

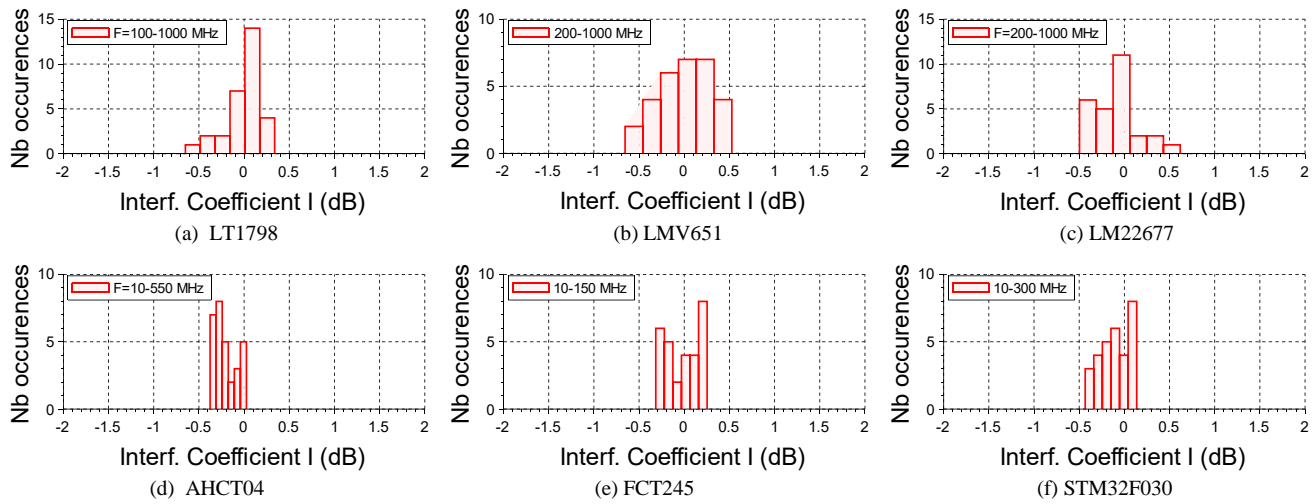


Fig. 8. Distribution of interference coefficient for random selection of three frequencies.

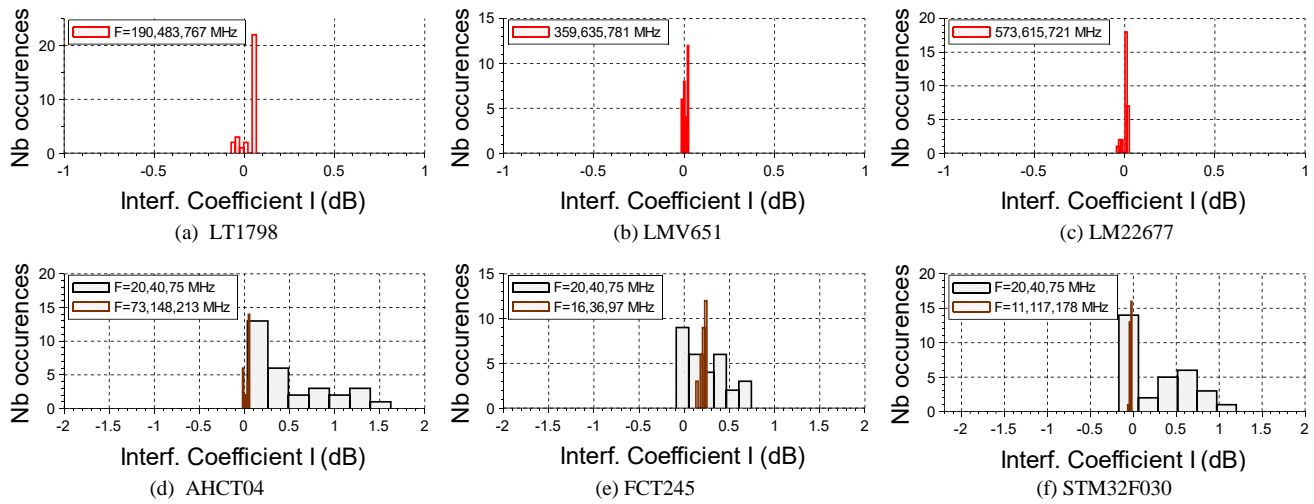


Fig. 9. Distribution of interference coefficient for random selection of phase.

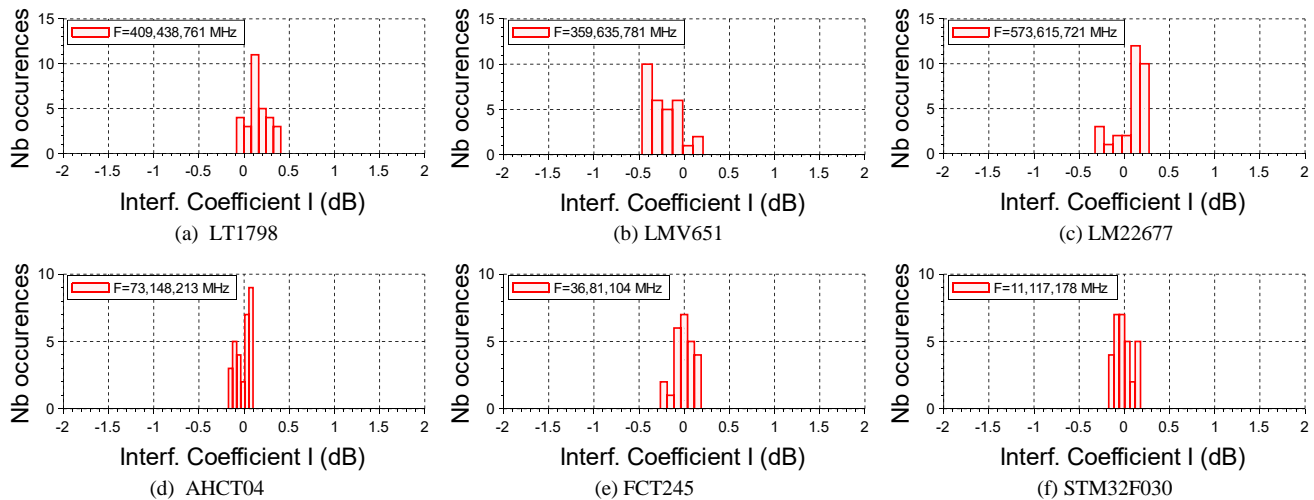


Fig. 10. Distribution of interference coefficient for random selection of amplitude.

For the three analog ICs, the phases of the tones have no significant influence on the risk assessment. This is consistent given the disturbance average power dependence of the failure mechanism. However, the phases of the tones have an impact on the risk assessment of the tested digital ICs, since the failure mechanisms depend on the peak power and the polarity of the

disturbance. Depending on the phases and frequencies of the different tones, the peak amplitude of the disturbance varies. If there is no particular relationship between tone frequencies, the phase has no influence because the disturbance always reaches the maximum amplitude. On the other hand, if the tone frequencies are multiple of a fundamental frequency (e.g. 20,

40 and 75 MHz), the disturbance may not reach the maximum amplitude and may exhibit a positive or negative pulse shape. It explains why the distribution of  $I_{tot}$  extends above 0 dB.

### VIII. CONCLUSION

With the growing concern about safety of electronic equipment in complex electromagnetic environments, the characterization and prediction of IC susceptibility to multitone disturbance become more and more urgent. This paper has proposed an experimental method and the associated indicators to characterize the nature of the response of an IC pin to multitone disturbance. The method relies on the injection of a comb signal composed of several equidistant harmonics with equal amplitude which test the susceptibility of an IC pin over a frequency range.

The main purpose of this injection is to verify the application of the disturbance superposition principle, which constitutes a simple case where the IC failure is due to the linear superposition of the contribution of each harmonic forming the disturbance. If this principle is verified by the test of the proposed indicator called total interference coefficient, the risk of failure of the IC to any combination of multitone disturbance to the tested pin can be easily evaluated from the CW susceptibility results. It avoids the exponential increase of multitone test configurations when a large number of simultaneous injected tones with different combinations of frequency, amplitude and phase is considered.

The proposed method is fast and convenient, as it may be easily inserted after a conventional CW IC susceptibility test. Moreover, it reuses the typical CW susceptibility test benches and results (CW susceptibility threshold curves). Only the harmonic disturbance generator is replaced by an AWG that produces a comb signal.

The method was tested on six different digital or analog ICs. Although the tested IC pins react non-linearly to electromagnetic interference (e.g. due to EMI-induced offset in analog circuits, jitter, bit flip and ESD protection triggering in digital circuits), the disturbance superposition applies as long as only one failure mechanism is activated. Once this principle has been verified, the tested case studies prove that the proposed EMI-risk assessment indicator (interference coefficient) succeeds in evaluating the risk of failure with an error less than 1 dB for multitone disturbance with randomly-chosen amplitude, frequency and phase. Although this study is not exhaustive and its conclusions cannot be extended to all existing ICs, it highlights the nature less exceptional than expected of the disturbance superposition principle. Further studies are necessary to identify which types of ICs and failure modes verify or not this principle.

In spite of these encouraging results, the proposed method still presents some limits to predict EM risks on electronic equipment placed in real electromagnetic environment. A first limit shown in this paper is that the method fails when several failure modes are activated simultaneously. Susceptibility tests cannot characterize independently each failure mode and the relationship between each failure mode is not extracted. Secondly, the method was limited to IC pin injection test in this

study, in order to neglect the influence of simultaneous injection on several pins. However, this situation is not realistic in practical situations. Future research works will be required to address these different issues in order to define a practical characterization method of electronic equipment response to multitone disturbance.

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