



HAL
open science

Top-down integration of suspended N⁺/P/N⁺ silicon-nanowire-based ion-sensitive field effect transistors for pH analysis at the submicronic scale

A. Lale, Auriane Grappin, Aurélie Lecestre, Laurent Mazenq, Jérôme Launay,
Pierre Temple-Boyer

► **To cite this version:**

A. Lale, Auriane Grappin, Aurélie Lecestre, Laurent Mazenq, Jérôme Launay, et al.. Top-down integration of suspended N⁺/P/N⁺ silicon-nanowire-based ion-sensitive field effect transistors for pH analysis at the submicronic scale. *Thin Solid Films*, 2023, 764, pp.139609. 10.1016/j.tsf.2022.139609 . hal-04744383

HAL Id: hal-04744383

<https://laas.hal.science/hal-04744383v1>

Submitted on 18 Oct 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

**Top-down integration of suspended N⁺/P/N⁺ silicon-nanowire-based
ion-sensitive field effect transistors for pH analysis at the submicronic scale**

A. Lale, A. Grappin, A. Lecestre, L. Mazonq, J. Launay, Pierre Temple-Boyer

LAAS-CNRS, Université de Toulouse, CNRS, UT3, INPT, 31031 Toulouse Cedex, France

LAAS-CNRS, 7 avenue du colonel Roche, 31031 Toulouse Cedex, France

Abstract: A technological process was proposed in order to integrate fully silicon-nanowire-based field-effect nanodevices on a silicon-on-insulator (SOI) substrate. Thanks to a double reactive ion etching process of the SOI silicon upper layer as well as to a "SiO₂ thermal oxidation growth / Al₂O₃ atomic layer deposition" gate process, silicon-nanowire-based field-effect transistors (SiNW-FET) and silicon-nanowire-based ion-sensitive field-effect transistors (SiNW-ISFET) were fabricated. Focuses were brought on (i) the integration of a suspended N⁺/P/N⁺ double-junction structure (gate length: ~ 0.75 μm and ~ 3.75 μm), (ii) the fabrication of a SiO₂/Al₂O₃ all-around surrounding gate structure, (iii) the achievement of low nanowire sections (width: ~ 150 nm, height: ~ 200 nm), and (iv) the final adaptation to the liquid phase analysis thanks to SU8-based wafer-level packaging. According to the proposed process, SiNW-FET and SiNW-ISFET devices showed excellent electrical characteristics in terms of leakage resistance R_{OFF}, subthreshold current slope and I_{ON}/I_{OFF} maximal ratio. SiNW-ISFET devices were finally studied for the pH analysis at the submicronic scale (analysed volumes: ~ 10 pL), evidencing standard potentiometric detection sensitivity (~ 56 mV/pH), as well as excellent amperometric detection sensitivity (~ 0.4 current decade per pH) in subthreshold regime.

Keywords: silicon nanowire, double-junction nanochannel, silicon nanowire field-effect transistor, silicon nanowire ion-sensitive field-effect transistor, measurement in liquid phase, micro-analysis

1. Introduction

In the frame of silicon-based technologies, field-effect transistors were thoroughly developed for electronic devices [1] as well as potentiometric sensors [2-4]. Focusing on the conventional metal-oxide-semiconductor field-effect transistors (MOSFET), this interest was associated to two main advantages conferred by silicon use. Firstly, its thermal oxidation enables the formation of Si/SiO₂ capacitive structures with excellent dielectric properties. Secondly, its semi-conductive properties enable the elaboration of P-type and N-type doped regions, and therefore P/N-based junctions or double-junctions. As a result, developing simultaneously the Gate and Source/Drain engineering, N-channel and P-channel MOSFET were microfabricated. Consequently, combined with the CMOS (complementary metal-oxide-semiconductor) technology achievement, MOSFET devices were microfabricated while reducing size, increasing density, improving performances and decreasing costs, leading to the very large-scale integration (VLSI) of electronic circuits [5,6]. Lastly, technological developments were extended to FET-based transducers such as chemical/biological field effect-transistors (ChemFET/BioFET) [3,4,7,8].

Considering the technological scaling down, bottlenecks were mainly associated to the previously quoted advantages of silicon. Concerning the Gate engineering, efforts were focused on the Si/SiO₂ capacitor, aiming to the gate oxide thickness decrease without increasing leakage currents. As a matter of fact, even if silicon gets hardly rid of its oxide SiO₂, plenty of dielectric metallic oxides were studied for conventional MOSFET-based devices [9,10] and further extended to ChemFET/BioFET sensors for liquid phase analysis [11]. In this context, aluminium oxide Al₂O₃ was emphasized due to high dielectric constant ($\epsilon_r \approx 10$), good interfacial properties, high chemical and thermal stabilities at high temperature (< 750°C) and excellent insulation/passivation properties in water-based solutions [12].

In the frame of Source/Drain engineering, several technological solutions were proposed to decrease the P/N junction size [13,14]. Nevertheless, with scaling down, the concept of junctionless transistors (JLT) was brought up to date [15,16]. Compared to the conventional MOSFET one, the JLT device does not need any PN junction to operate properly while using very thin (< 10 nm) and heavily doped ($> 10^{19}$ at/cm³) silicon channels. Consequently, thanks to ultra-thin silicon-on-insulator substrates, CMOS-compatible JLT technologies were proposed, emphasizing different channel geometries, such as thin films, nanofins and nanowires [17].

As part of ChemFET/BioFET microsensors, the JLT technology was further limited. Indeed, their performances are affected by gate leakage currents, usually specific of water analysis. Since the phenomenon is directly proportional to the gate sensitive surface, the use of nanowires took precedence over those of nanofins or thin films. As a result, silicon-nanowire field effect transistors (SiNW-FET) were mainly developed for the potentiometric analysis of ionic species and (bio)molecules in liquid phase [18,19].

All in all, the compromise between "Junction nanowire" or "Junctionless nanowire" technologies had to be solved while dealing with nanobiosensors. As a matter of fact, considering the "Bottom-up" approach associated to silicon nanowires (SiNW) grown by "Vapor – Solid – Liquid" technique [20], this compromise was of little importance: since the SiNW in-situ doping enables the formation of any type of junctions, both technologies were proposed [21-25]. Anyway, the "Top-down" approach was preferred in order to further improve fabrication yield and reproducibility. On the one hand, the "junctionless SiNW-FET" technology was developed since it is associated to simpler, easier and cheaper technological processes [26-30]. On the other hand, junction-based SiNW-FET were also studied, while tackling off different technological bottlenecks [31-36]. Thus, technological processes were studied, either based on the sidewall spacer technique applied to polysilicon thin films [31,32,34], or on optimized etching of polysilicon layers [33,35,36]. Nevertheless, in order to integrate fully monocrystalline, double-junction-based SiNW-

FET devices [37-49], the use of silicon-on-insulator (SOI) substrates allowed finally innovative, CMOS-compatible, top-down technological processes such as: supper lattice nanowire pattern transfer [37], plasma dry etching [38,43,45,47,49], (100) and (111) wet anisotropic etching [39-42,44,46], and sidewall mask technology [48].

This paper proposes to investigate the fabrication of silicon-nanowire-based ion-sensitive field effect transistors (SiNW-ISFET) while integrating a suspended $N^+/P/N^+$ double-junction structure through the development of a double reactive ion etching (RIE) process, and to study their electrical performances in the frame of pH analysis at the submicronic scale.

2. Experimental details

All the technological developments were performed in the LAAS-CNRS cleanroom facility by relying on previously-studied silicon-based processes and related equipment. In this case, scanning electron microscopy (SEM) observations were performed with a FEI Helios 600i system using a high-resolution electron column based on a Schottky field emission gun. Photoresist patterns were imaged at an accelerating voltage of 1 kV and a current of 86 pA, the others samples were analysed at 30 kV and 86 pA.

2.1. Microfabrication of silicon nanofins by reactive ion etching

To fabricate silicon nanofins, a photolithographic process was developed in order to carry out masking nanopatterns thanks to a CANON FPA3000i4 "Lithography by projection" stepper. The AZ ECI 3012 photoresist (provided by Microchemicals) was chosen for its development resolution (400 nm) and an AZ BARLI II bottom anti-reflexive coating (BARC, also provided by

Microchemicals) was moreover used (thickness: 200 nm). By preventing UV reflections on the silicon substrate, this coating allows to improve the masking resolution under 300 nanometres.

Using specifically oxidized (field oxide thickness: 65 nm) P-type (boron doping: 10^{15} at/cm³) silicon substrate, the photolithographic process was optimized in order to achieve photoresist nanopatterns adapted to the BARC/SiO₂/Si reactive ion etching (RIE) step, leading to the fabrication of silicon nanowires. Considering a photoresist thickness around 1.2 μm, a compromise had to be found between the UV exposure dose, whose increase is responsible for the nanopattern width decrease towards zero, and the focus depth, whose increase is responsible for photoresist wall steepness lower than 90° (clearly non-adapted to the RIE process). According to simulation results achieved with the GENISYS software (not shown), the following ranges were finally defined in order to obtain a 90° steepness:

- UV exposure dose: [600 J/m² – 800 J/m²],
- focus depth: [- 0.1 μm – - 0.5 μm].

Thus, considering the final fabrication of single silicon nanowires as well as parallel networks of silicon nanowires, photolithographic parameters were optimized in order to fabricate 1.2 μm-thick photoresist nanopatterns, with vertical side walls and widths ranging from 190 to 290 nanometres (figure 1).

Consequently, technological developments were dedicated to the photoresist nanopattern transfer into a silicon substrate by inductively-coupled plasma reactive ion etching (ICP-RIE), using a TRIKON OMEGA 21 equipment. This technological process implied three different RIE steps to etch the 200 nm-thick BARC coating, the 65 nm-thick field oxide SiO₂ and the silicon substrate (P-type, boron doping: 10^{15} at/cm³):

- BARC: O₂/CF₄/CHF₃/Ar plasma (P_{ICP} = 300 W, P_{bias} = 40 W, p = 0.666 Pa),
- SiO₂: CHF₃ plasma (P_{ICP} = 500 W, P_{bias} = 60 W, p = 0.666 Pa),
- Si(P): SF₆/C₄F₈/O₂ plasma (P_{ICP} = 450 W, P_{bias} = 30 W, p = 0.8 Pa).

The first BARC RIE step was characterized by an etch rate around 350 nm/min. As non-selective towards the photoresist layer, the etching duration should be controlled precisely, any time overrun being responsible for the nanopattern deterioration. The second etching step is associated to a standard RIE process of silicon dioxide SiO₂, whose etch rate was previously studied (~ 20 nm/min). Finally, concerning the Si(P) RIE step, the SF₆/C₄F₈/O₂-based plasma was preferred to the Cl₂ one. Indeed, the etch rate around 190 nm/min led to good results for etching homogeneity and verticality. This last property is related to the sidewall passivation during the deep silicon etching, decreasing significantly lateral phenomena. As a result, the final silicon nanofins so manufactured had a similar width than the photoresist nanopatterns, thus ranging from 190 to 290 nanometres (table 1 and figure 2).

2.2. Transfer of the silicon nanowire microfabrication on SOI substrates

In order to achieve junction-based SiNW-ISFET devices, a silicon-on-insulator (SOI) substrate was specifically required in order to fabricate silicon nanowires and to define precisely their geometry. The technological process was therefore designed while considering a 6-inch (100) SOI substrate (provided by SOITEC) with the following characteristics:

- upper silicon layer: P-type (boron doping: 10¹⁵ at/cm³), thickness: 280 nm,
- buried SiO₂ layer: thickness: 1 μm,
- silicon substrate: P-type (boron doping: 10¹⁵ at/cm³), thickness: ~ 675 μm.

To be compatible with the final SiNW-ISFET technological process, the previous microfabrication process (see §2.1) had to be used while considering the SOI substrate upper field oxide (thickness: 65 nm). At first glance, this substrate modification should not change the photolithographic and RIE processes to pattern photoresist and etch the BARC/SiO₂/Si structure. Nevertheless, an unexpected problem occurred due to the wall passivation properties of the SF₆/C₄F₈/O₂-based plasma. Since etched patterns were characterized by different geometries (single nanowire versus parallel networks of nanowires) as well as different surface densities, it was expected to over etch locally the buried SiO₂ layer in order to obtain a good etching homogeneity all around the wafer. Unfortunately, according to passivation phenomena due to the SF₆/C₄F₈/O₂-based plasma, this over etching was responsible for by-product deposition on the silicon nanowire sidewalls, preventing the successful integration of SiNW-based FET.

In order to tackle off this technological bottleneck, a double RIE process (requiring two photolithographic masks) was developed for the final fabrication of silicon nanowires on an SOI substrate. The first mask was designed in order to etch partially the upper silicon layer, outlining the silicon nanowire patterns. Thus, using a constant opening/etching width all around the wafer, the silicon etch rate was thoroughly controlled, preventing any over etching of the buried SiO₂ layer. Then, the second mask was designed in order to etch the remaining silicon layer while protecting the previously-made silicon nanofins. Thus, the RIE process was carried out on the whole wafer, preventing any sidewall parasitic deposition associated to the buried SiO₂ layer (figure 3).

2.3. Integration of N⁺/P/N⁺ silicon nanowire ion-sensitive field effect transistors

The SiNW-ISFET process was developed to product an N⁺/P/N⁺ silicon nanowire between the source and drain contacts and to adapt the final device to liquid phase analysis thanks to

microfluidic structures fabricated by wafer level packaging (figure 4). The different nanodevices geometries and characteristics were defined as following:

- number of parallel silicon nanowires: 1, 20 and 100,
- silicon nanowire initial width: 300 nanometres,
- silicon nanowire length: 2, 5, 10 and 20 micrometres,
- gate length: 2 and 5 micrometres.

First of all, specific simulations were performed using the SILVACO ATHENA™ software in order to optimize the implantation/diffusion processes associated to the creation of the N⁺ source and drain regions into the chosen P-type SOI substrate. To that end, using a pre-implantation oxide (thickness: 11 nm), an arsenic-based implantation (energy: 15 keV, dose: 5×10^{15} at/cm³) was chosen in order to control lateral diffusion of the N⁺ regions into the P-type upper silicon layer around 1.25 μm. After removing this arsenic-rich oxide using hydrofluoric acid (HF), a diffusion/activation anneal at 1070°C was performed under an O₂ ambient, causing the growth of a 65 nm-thick field oxide on P-type regions. Then, the double RIE process (see below) was performed in order to fabricate N⁺/P/N⁺ silicon nanowires with the following widths:

- silicon nanowire width: ~ 190, ~ 240 and ~ 290 nanometres,
- silicon nanowire height: ~ 240 nanometres.

At this stage, a first gate oxide (thickness: 20 nm) was grown by thermal oxidation at 1000°C and further removed into HF cleaning. According to the thermal oxidation of silicon [5,50], these technological steps lead to the silicon sidewall smoothing while decreasing the silicon nanowire width and height (figure 5):

- silicon nanowire width: ~ 170 , ~ 220 and ~ 270 nanometres,
- silicon nanowire height: ~ 220 nanometres.

Then, a specific photolithographic mask was used in order to etch completely the buried oxide layer on either side of the $N^+/P/N^+$ double junction structure thanks to an HF cleaning. This gate opening step was responsible for the silicon nanowire suspension (figure 6), allowing the final fabrication of an all-around surrounding gate and preparing them for water-based analysis into microfluidic structures.

Afterwards, the gate insulator was fabricated. After an RCA cleaning, a silicon oxide SiO_2 layer (thickness: 20 nm) was grown by thermal oxidation at $1000^\circ C$ and an amorphous alumina Al_2O_3 layer (thickness: 25 nm) was deposited on top by atomic layer deposition with tri-methyl-aluminium $Al(CH_3)_3$ and dioxygen O_2 as precursors [51]. Due to deposition process conformity, an SiO_2/Al_2O_3 all-around surrounding gate structure, whose advantages were previously demonstrated [52], was achieved. Simultaneously, the Al_2O_3 layer ensured insulation/passivation properties in water-based solutions [53], aiming to the SiNW-ISFET improvement. As previously, after this new thermal oxidation step, the silicon nanowire width and height were further decreased and the channel length reached its final value (as simulated using the SILVACO ATHENA™ software):

- silicon nanowire width: ~ 150 , ~ 200 and ~ 250 nanometres,
- silicon nanowire height: ~ 200 nanometres,
- final gate length: ~ 0.75 and ~ 3.75 micrometres.

At this stage, the suspended $N^+/P/N^+$ SiNW-ISFET structures were structured. Hence, contact openings were made towards the source and drain N^+ regions by etching the upper alumina Al_2O_3

layer along with the field oxide layer, and a titanium/platinum/silver Ti/Pt/Ag (20 nm / 150 nm / 1000 nm) metallization was finally deposited by lift-off to form the contact pads. This metallic structure was previously studied for the integration of platinum-based electrochemical microcells ElecCell for water-based solution analysis, focusing on Ti/Pt counter and working microelectrode as well as on Ag/AgCl reference microelectrodes [54]. Its use is therefore required for the characterization of the SiNW-ISFET devices in liquid phase. According to their electrical properties, the Ti/Pt/Ag contact resistance was estimated to 10 Ω , whereas the resistance of the N⁺-type silicon nanowire region was 300 ohms per micron (i.e. 3000 Ω for a 10 μm long nanowire).

It should finally be noted that, by integrating Ti/Pt/Ag metallic gates on specific silicon chips and Ti/Pt/Ag(AgCl) reference microelectrodes (using a specific electrochemical oxidation process of the silver upper metallic layer into a 0.01 M KCl solution [54]), the "Metallization" photolithographic mask allowed the simultaneous fabrication of both SiNW-FET and SiNW-ISFET devices (number per chip: 16) on 7 \times 8 mm² silicon chips (figure 7).

2.4. Adaptation to the liquid phase analysis: from wafer-level to chip-level packaging

In order to adapt the SiNW-ISFET to the liquid phase, apart from the wafer-level alumina passivation layer (see §2.3), a previously-studied wafer-level packaging was used [55,56]. Starting from a SU8-based passivation layer (thickness: \approx 7 μm) deposited by spin coating, UV photolithography was performed in order to fabricate hydrophilic, SU8-based, microfluidic structures (figure 8) such as microtanks (diameter: 1 mm) and closed microchannels (height: \sim 5 μm , width: \sim 5 μm). The full integration of the N⁺/P/N⁺ SiNW-ISFET and its Ti/Pt/Ag(AgCl) reference microelectrode into microfluidic channels (figure 9) allowed the final devices to be finally adapted to the analysis of microvolumes around a dozen of picolitres (typically: 5 \times 5 \times 500 μm^3).

Lastly, after dicing, the SiNW-ISFET silicon chips were placed on and connected electrically to a specific printed circuit board (PCB) using a SET FC150 flip-chip packaging system, ensuring the chip/PCB mechanical strength and the electrical bonding sealing thanks to an Epotek H70E glue and a Polytech EP601 underfill respectively. A Pyrex ring was finally glued on the PCB to create an upper tank on the SiNW-ISFET chip, facilitating liquid handling during electrical characterization.

2.5. Electrical characterization of the SiNW-FET and SiNW-ISFET devices

SiNW-FET devices were characterized on the wafer by probe testing in order to check the technological process before the SU8-based wafer-level packaging procedure (see §2.4). To that end, a wafer probe Cascade Summit 1200 and its Faraday cage were coupled to a Keithley 4200 analyser (current detection limit: 3×10^{-15} A).

For the SiNW-ISFET measurement in liquid phase, a metallic shielded room was used with the aim of preventing any electromagnetic or optical interferences. A Keithley 707 commutation system was employed to test simultaneously sixteen different microdevices, whereas current-voltage (I-V) characterization was performed using an Agilent 4142B analyser (current detection limit: 5×10^{-11} A). In addition, using standard pH = 4.0, pH = 7.0, pH = 10.0 buffers (provided by Sigma) were used combined with a Metrohm Ag/AgCl/KCl reference microelectrode to apply the gate voltage to the analysed samples. The experimental studies were finally focused on pH, pK and pNa measurements.

All the electrical characterizations were performed at ambient temperature (22 ± 1 °C).

3. Results and discussion

3.1. Electrical properties of the N⁺/P/N⁺ SiNW-FET devices

The SiNW-FET electrical characterization was performed for "150 nm-wide – 200 nm-high" silicon nanowires. For the two studied gate lengths (0.75 μm and 3.75 μm), classical NMOS $I_{\text{DS}}(V_{\text{DS}})$ analytical curves were found for increasing gate-source voltage V_{GS} , evidencing both linear and saturation modes, even for a "0.75 μm gate length" single nanowire (figure 10a). On the basis on 42 different devices, the threshold voltage V_{T} was estimated to 0.62 ± 0.26 V, whatever the gate length value and the nanowire number (1, 20 or 100).

Figure 10b shows the SiNW-FET $I_{\text{DS}}(V_{\text{GS}})$ semi-logarithmic curves obtained for different nanowire configurations ($V_{\text{DS}} = 0.1$ V). Hence, no variation of the off-state current I_{OFF} was evidenced for the two different gate lengths. Due to the 3 fA limitation, the I_{OFF} value obtained for a single nanowire SiNW-FET could not be measured experimentally. Nevertheless, since the 20-nanowire and 100-nanowire configurations were characterized by values around 15 fA and 70 fA respectively, the "single nanowire" I_{OFF} value was finally estimated to 0.7 fA. In fact, this value increased linearly with the drain-source voltage V_{DS} (result not shown). Thus, the corresponding conductance was estimated to 350 fS for a 100-nanowire device and, consequently, to 3.5 fS for a single nanowire (equivalent to a leakage resistance R_{OFF} around 3×10^{14} Ω). In the same way, the gate current I_{G} obtained for a single nanowire SiNW-FET was estimated to 0.03 fA for a 3 V gate-source voltage, corresponding to a gate resistance R_{G} around 10^{17} Ω .

The subthreshold slope was finally evaluated around 0.167 V per current decade, i.e. 6 current decades per volt, independently of the different "150 nm-wide – 200 nm-high" SiNW-FET configurations (figure 10b). Such low values were already shown for nano field-effect transistors (nanoFET) devices [52,57,58]. The $I_{\text{ON}}/I_{\text{OFF}}$ ratio was finally analysed as a function of the drain-source voltage V_{DS} (result not shown). In all cases, the maximal $I_{\text{ON}}/I_{\text{OFF}}$ ratio was obtained for around 0.8 V, estimated around 4×10^9 and 8×10^8 for the 0.75 μm and 3.75 μm gate lengths respectively.

According to the $I_{DS}(V_{GS})$ linear curves, the SiNW-FET transconductance G_m was also studied (figure 10c). This parameter was shown to increase linearly with the nanowire number. Based on this assumption, the R_{ON} resistance of single nanowire transistor was estimated to 1200 k Ω and 125 k Ω at a V_{DS} voltage value of 0.1 and 1 V respectively.

Lastly, the 100-nanowire configuration was used to study G_m variations (figure 10d). For both gate lengths (0.75 μm and 3.75 μm), the G_m value followed linear variations with the drain-source voltage V_{DS} , reaching saturation at approximately 1.3 V. Slope values were estimated to 770 and 175 $\mu\text{S/V}$ for 0.75 and 3.75 μm gate lengths respectively, evidencing a slope ratio around 4.4. According to the MOSFET theory, this slope ratio is correlated to the gate length ratio inverse, known to be equal to 5. As a consequence, based on this experimental value, the N^+ lateral diffusion into the P-type layer was estimated to 1.1 μm (rather than 1.25 μm as predicted by SILVACO ATHENA™ simulations), for effective gate lengths around 0.9 and 3.9 μm for both nanodevices respectively.

All in all, the electrical characteristics of the single-nanowire $N^+/P/N^+$ SiNW-FET devices (width: \sim 150 nm, height: \sim 200 nm, gate length: \sim 0.75 μm , nanowire length: \sim 10 μm) were summarized in table 2.

3.2. Electrical properties of the $N^+/P/N^+$ SiNW-ISFET devices in the frame of a liquid phase analysis

The SiNW-ISFET electrical characterization was mainly performed for "150 nm-wide – 200 nm-high" silicon nanowires, using a pH = 4.0 buffer. Consequently, on the basis on 53 different devices, the threshold voltage V_T was estimated to 0.85 ± 0.23 V, whatever the technological parameters. This value agrees globally with the SiNW-FET one (see §3.1), demonstrating the reproducibility of the whole process and its compatibility with liquid phase analysis.

Figure 11a shows the $I_{DS}(V_{GS})$ semi-logarithmic curves obtained for different SiNW-ISFET configurations ($V_{DS} = 1$ V). The gate current I_G and the off-state current I_{OFF} were lower than the 50 pA detection limit whatever the tested configuration. Taking in consideration the 100-nanowire devices, the I_{OFF} value of a single nanowire should be lower than 0.5 pA. Consequently, the leakage resistance R_{OFF} of a single nanowire should be higher than $2 \times 10^{12} \Omega$.

Again, the subthreshold slope did not depend on the different SiNW-ISFET configurations and was evaluated to 0.11 V per current decade for a "150 nm-wide – 200 nm-high" silicon nanowire. Compared to the corresponding SiNW-FET result (0.167 V, see §3.1), this lower value is due to technological considerations. Indeed, according to the Ti/Pt/Ag metallization process, the SiNW-FET devices should be characterized by a partially surrounding metal/insulator/semiconductor gate structure. On the contrary, since silicon oxidation and atomic layer deposition processes are known to be conformal, the $\text{SiO}_2/\text{Al}_2\text{O}_3$ deposition is performed all around the silicon nanowire. As a matter of fact, the lower subthreshold slope obtained for the SiNW-ISFET devices shows that an all-around surrounding Electrolyte/Insulator/Semiconductor (EIS) gate was effectively achieved. In order to check this assumption, SiNW-ISFET with different silicon nanowire widths were characterized [52]. As shown by Ritzenthaler et al., the subthreshold slope was found to vary greatly with the silicon nanowire width (0.11, 0.125 and 0.18 volt per current decade, i.e. 9, 8 and 5.5 current decades per volt, for values of 150 nm, 200 nm and 250 nm respectively, result not shown), confirming the improvement brought thanks to the all-around EIS gate configuration.

Lastly, since it was not possible to determine precisely the off-state current, the I_{ON}/I_{OFF} ratio was not studied properly. Nevertheless, according to our characterization data and considering only the 150 nm-wide silicon nanowire SiNW-ISFET, it should be higher than 6×10^7 and 1.5×10^7 for the 0.75 μm and 3.75 μm gate lengths respectively.

As observed previously for the SiNW-FET device (see §3.1), the SiNW-ISFET transconductance G_m was shown to increase linearly with the nanowire number (figure 11b). The R_{ON} resistance was evaluated again for a single nanowire transistor, evidencing a 600 k Ω and 62.5 k Ω for a V_{DS} voltage of 0.1 V and 1 V respectively. The G_m linear variations with the drain-source voltage V_{DS} was also studied (result not shown). In agreement with SiNW-FET results, the slope ratio between the two gate lengths (0.75 and 3.75 μm) was estimated around 4.3.

All in all, the electrical characteristics of the single-nanowire $N^+/P/N^+$ SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 μm , nanowire length: ~ 10 μm) were summarized in table 2. Even if the SiNW-ISFET data were impacted by the current detection limit in liquid phase, the comparison with the SiNW-FET one is interesting. Firstly, in all cases, the series resistance (estimated around 0.3 k $\Omega/\mu\text{m}$ for a single nanowire) was effectively negligible compared to the SiNW-FET/ISFET R_{ON} resistance. Secondly, compared to the SiNW-FET partially-surrounding MIS gate structure, the SiNW-ISFET all-around surrounding EIS gate structure was responsible for an improvement of the conduction properties: around three current decades per volt (from 6 to 9) were gained and the G_m conductance was doubled. Thirdly, since their electrical characterization was hindered by the current detection limit, the SiNW-ISFET real performances should be better than the experimentally-obtained ones.

3.3. pH detection properties of the $N^+/P/N^+$ SiNW-ISFET devices

Furthermore, working always with the "150 nm-wide – 200 nm-high" nanowire geometry, the pH detection properties of the SiNW-ISFET sensor were studied in consideration of water-based solutions analysis at the submicronic scale (analysed volume: ~ 10 pL). Figure 12a shows the typical $I_{DS}(V_{GS})$ linear/semi-logarithmic curves obtained with a "single nanowire" SiNW-ISFET (length gate: 0.75 μm , $V_{DS} = 1$ V) for three different buffer solutions (4.0, 7.0 and 10.0). In the light

of the different SiNW-ISFET configurations (single nanowire, 20 nanowires and 100 nanowires), the detection sensitivity was estimated to 56 ± 4 mV/pH, whatever the technological parameters (53 different devices were tested). It should finally be noted that the subthreshold drain-source current I_{DS} was found to decrease greatly with the pH increase (result not shown). In the studied case, for a 1.25 V gate-source voltage V_{GS} , this value is multiplied by approximately 250 between pH = 4 and pH = 10, for an amperometric detection sensitivity around 0.4 current decade per pH.

Standard potentiometric analyses were finally performed to check the pH measurement hysteresis between pH = 3 and pH = 9 (figure 12b), as well as the selectivity to K^+ and Na^+ ions in the [1-3] pX concentration range (result not shown). In this frame, a "100 nanowire" configuration was preferred in order to increase the measured current (length gate: 0.75 μm , $V_{DS} = 1$ V). Thus, no hysteresis phenomena and no pK or pNa interference were evidenced for the $\text{SiO}_2/\text{Al}_2\text{O}_3$ SiNW-ISFET devices, demonstrating the performances of amorphous alumina as a pH-sensitive layer.

4. Conclusion

Silicon-nanowire-based field effect transistors (SiNW-FET) as well as silicon-nanowire-based ion-sensitive field effect transistors (SiNW-ISFET) were fabricated on SOI substrate while focusing on the integration of a suspended $N^+/P/N^+$ double-junction structure (gate length: ~ 0.75 μm and ~ 3.75 μm). First, a double reactive ion etching process was optimized in order to fabricate single silicon nanowire (length: ~ 10 μm) and parallel networks of such nanowires. Second, a conformal process based on a silicon thermal oxidation followed by an alumina atomic layer deposition was developed in order to achieve an $\text{SiO}_2/\text{Al}_2\text{O}_3$ all-around surrounding gate structure and to reach low silicon nanowire sections (width: ~ 150 nm, height: ~ 200 nm). Lastly, a SU8-based wafer-level packaging process was developed in order to adapt the SiNW-ISFET to the analysis of

microvolumes around a dozen of picolitres. Hence, even if current detection limit inherent to nanowire-based devices had to be considered, excellent electrical characteristics were obtained:

- SiNW-FET: $R_{\text{OFF}} \approx 3 \times 10^{14} \Omega$, subthreshold slope ≈ 0.167 V/decade, $(I_{\text{ON}}/I_{\text{OFF}})_{\text{max}} \approx 4 \times 10^9$,

- SiNW-ISFET: $R_{\text{OFF}} > 2 \times 10^{12} \Omega$, subthreshold slope ≈ 0.11 V/decade, $(I_{\text{ON}}/I_{\text{OFF}})_{\text{max}} > 6 \times 10^7$.

Finally, the pH analysis at the submicronic scale (analysed volumes: ~ 10 pL) was demonstrated. In the standard potentiometric measurement configuration, SiNW-ISFET devices were characterized by quasi-Nernstian pH detection properties (56 ± 4 mV/pH), whatever the technological parameters. Furthermore, considering the subthreshold operation mode, the amperometric detection sensitivity was estimated to 0.4 current decade per pH, enabling accurate pH measurement in liquid phase.

Works will be continued while applying the proposed SiNW-ISFET technology to chemical, biochemical and biological analysis in liquid phase, focusing on the recording of neuronal bio-electro-chemical activities. Moreover, taking into consideration technological developments, the double reactive ion etching process will be further investigated. According to first preliminary technological realizations, it should enable the fabrication of triangular silicon nanowires on standard silicon substrate and the corresponding technological process should be further designed, microfabricated and optimized.

Acknowledgements

Technological realizations were partly supported by the French RENATECH network.

References

- [1] S.M. Sze, "Physics of semiconductors devices", 2nd edition, John Wiley & Sons Inc., Canada (1981)
- [2] S. Hong, M. Wu, Y. Hong, Y. Jeong, G. Jung, W. Shin, J. Park, D. Kim, D. Jang and J.-H. Lee, "FET-type gas sensors: a review", *Sensors and Actuators*, B330 (2021) 129240
- [3] P. Bergveld, "Thirty years of ISFETOLOGY: What happened in the past 30 years and what may happen in the next 30 years", *Sensors and Actuators*, vol. B88 (2003) 1-20
- [4] N. Chaniotakis and M. Fouskaki, "Bio-chem-FETs: field effect transistors for biological sensing, *Biological identification*, Woodhead publishing (2014) 194-2019
- [5] S.M. Sze, "VLSI technology", 2nd edition, Mac Graw Hill Book, New-York (1983)
- [6] H. Iwai, "Roadmap for 22 nm and beyond", *Microelectronic Engineering*, 86 (2009) 1520-1528
- [7] M. Omar Noor and U.J. Krull, "Silicon nanowires as field effect transducers for biosensors development: a review", *Analytica Chimica Acta*, 825 (2014) 1-25
- [8] D. Sadighbayan, M. Hasanzadeh and E. Ghafar-Zadeh, "Biosensing based on field-effect transistors (FET): recent progress and challenges", *Trends in Analytical Chemistry*, 133 (2020) 116067-1-116067-16
- [9] R.M. Wallace and G.D. Wilk, "High-k dielectric materials for microelectronics", *Critical Reviews in Solid State and Materials Sciences*, 28 (2003) 231-285
- [10] J.A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X.P. Wang, C. Adelman, M.A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschant, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V.V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J.W. Maes, D. Manger, W. Vandervorst, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M.

- Jurczak, J. Van Houdt and D.J. Wouters, "High-k dielectrics for future generation memory devices", *Microelectronic Engineering*, 86 (2009) 1789-1795
- [11] L. Manjakal, D. Szwagierczak and R. Dayiya, "Metal oxides based electrochemical pH sensors: current progress and future perspectives", *Progress in Materials Science*, 109 (2020) 100635 1-31
- [12] K.B. Jinesh, J.L. van Hemmen, M.C.M. van de Sanden, F. Roozeboom, J.H. Klootwijk, W.F.A., Besling and W.M.M. Kessels, "Dielectric properties of thermal and plasma-assisted atomic layer deposition Al₂O₃ thin films", *Journal of the Electrochemical Society*, 158 (2011), G21-G26
- [13] M. Vinet, "MOSFET transitions towards fully depleted architectures", *Proceedings of Technical Program of 2012 VLSI-TSA "Technology, System and Application"* (2012), <https://doi.org/10.1109/VLSI-TSA.2012.6210109>
- [14] F. Cristiano, M. Shatesteh, R. Duffy, K. Huet, F. Mazzamutto, Y. Qiu, M. Quillec, H.H. Henrichsen, P.F. Nielsen, D.H. Petersen, A. La Magna, G. Caruso and S. Boninelli, "Defect evolution and doping activation in laser annealed Si and Ge", *Materials Science in Semiconductor Processing*, 42 (2016), 188-195
- [15] J.P. Colinge, C.W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. Mc Carthy and R. Murphy, "Nanowire transistors without junctions", *Nature Nanotechnology*, 5 (2010), 225-229
- [16] J.P. Colinge, C.W. Lee, N.D. Akhavan, R. Yan, I. Ferain, A. Kranti and R. Yu, "Junctionless transistors: Physics and properties", "Semiconductor-On-Insulator materials for nanoelectronics applications, Springer Berlin Heidelberg (2011)
- [17] A. Nowbahari, A. Roy and L. Marchetti, "Junctionless transistors: state of the art", *Electronics*, 9 (2020), 1174-1195

- [18] L. Mu, Y. Chang, S.D. Sawtelle, M. Wipf, X. Duan and M.A. Reed, "Silicon nanowire field-effect transistors: a versatile class of potentiometric nanobiosensors", *IEEE Access*, 3 (2015), 287-302
- [19] Y.-C. Syu, W.-E. Hsu and C.-T. Lin, "Review – field effect transistors biosensing: devices and clinical applications", *ECS Journal of Solid-State Science and Technology*, 7 (2018), Q3196-Q3207, DOI: 10.1149/2.0291807jss
- [20] P.C. McIntyre and A. Fontcuberta i Morral, "Semiconductor nanowires: to grow or not to grow", *Materials Today Nano*, 9 (2020), 100058
- [21] Y. Cui, Q. Wei, H. Park and C.M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species", *Science*, 293 (2001), 1289-1292
- [22] G. Zheng, F. Patolsky, Y. Cui, W.U. Fang and C.M. Lieber, "Multiplexed electrical detection of cancer markers with nanowire sensor arrays", *Nature biotechnology*, 23 (2005), 1294-1301
- [23] H. Zhu, Q. Li, H. Yuan, H. Baumgart, D.E. Ioannou and C.A. Richter, "Self-aligned multi-channel silicon nanowire field-effect transistors", *Solid-State Electronics*, 78 (2012), 92-96
- [24] B.-R. Li, C.-W. Chen, W.-L. Yang, T.-Y. Lin, C.-Y. Pan and Y.T. Chen, "Biomolecular recognition with a sensitivity-enhanced nanowire transistor biosensor", *Biosensors and Bioelectronics*, 45 (2013), 252-259
- [25] J. Li, G. He, H. Ueno, C. Jia, H. Noji, C. Qi and X. Guo, "Direct real-time detection of single proteins using silicon nanowire-based electrical circuits", *Nanoscale*, 8 (2016), 16172-16176
- [26] E. Stern, J.F. Klemic, D.A. Routenberg, P.N. WyremBak, D.B. Turner-Evans, A.D. Hamilton, D.A. La Van, T.M. Fahmy and M.A. Reed, "Label-free immunodetection with CMOS-compatible semiconducting nanowires", *Nature*, 445 (2007), 519-522
- [27] N. Elfström, A. Eriksson Karlström and J. Linnros, "Silicon nanoribbons for electrical detection of biomolecules", *Nanoletters*, 8 (2008), 945-949

- [28] O. Knopfmacher, A. Tarasov, W. Fu, M. Wipf, B. Niesen, M. Calame and C. Schönenberger, "Nernst limit in dual-gated Si-nanowire FET sensors", *Nanoletters*, 10 (2010) 2268-2274
- [29] S. Chen, J.G. Bomer, E.T. Carlen and A. van den Berg, "Al₂O₃/silicon nanoISFET with near ideal Nernstian response", *Nanoletters*, 11 (2011) 2334-2341
- [30] S. Rollo, D. Rani, W. Olthuis and C. Pascual Garcia, "High performance fin-FET electrochemical sensor with high-k dielectric materials", *Sensors and Actuators*, B303 (2020), 127215-1 – 127215-7
- [31] C.-Y. Hsiao, C.-H. Lin, C.-H. Hung, C.-J. Su, Y.-R. Lo, C.-C. Lee, H.-C. Lin, F.-H. Ko, T.-Y. Huang and Y.-S. Yang, "Novel poly-silicon nanowire field effect transistor for biosensing application", *Biosensors and Bioelectronics*, 24 (2009), 1223-1229
- [32] M.M.A. Hakim, M. Lombardini, K. sun, F. Giustiniano, P.L. Roach, D.E. Davies, P.H. Howarth, M.R.R. de Planque, H. Morgan and P. Ashburn, "Thin film polycrystalline silicon nanowire biosensors", *Nanoletters*, 12 (2012), 1868-1872
- [33] M.-C. Chen, H.-Y. Chen, C.-Y. Lin, C.-H. Chien, T.-F. Hsieh, J.-T. Horng, J.-T. Qiu, C.-C. Huang, C.-H. Ho and F.-L. Yang, "A CMOS-compatible poly-Si nanowire device with hybrid sensors/memory characteristics for system-on-chip applications", *Sensors*, 12 (2012), 3952-3963
- [34] C. Wenga, E. Jacques, A.-C. Salaün, R. Rogel, L. Pichon and F. Geneste, "Step-gate polysilicon nanowires field-effect transistor compatible with CMOS-technology for label-free DNA biosensor", *Biosensors and Bioelectronics*, 40 (2013), 141-146
- [35] C.-W. Huang, Y.-J. Huang, P.-W. Yen, H.-H. Tsai, H.-H. liao, Y.-Z. Juang, S.-S. Lu and C.-T. Lin, "A CMOS wireless biomolecular sensing system-on-chip based on polysilicon nanowire technology", *Lab on a Chip*, 13 (2013), 4451-4459

- [36] J.-Y. Kim, J.-H. Ahn, D.-I. Moon, T.J. Park, S.Y. Lee and Y.-K. Choi, "Multiplex electrical detection of avian influenza and human immunodeficiency virus with an underlap-embedded silicon nanowire field-effect transistor", *Biosensors and Bioelectronics*, 55 (2014), 162-167
- [37] Y.L. Bunimovich, Y.S. Shin, W.-S. Yeo, M. Amori, G. Kwong and J.R. Yeath, "Quantitative real-time measurements of DNA hybridization with alkylated non-oxidized silicon nanowires in electrolyte solution", *Journal of the American Chemical Society*, 128 (2006), 16323-16331
- [38] Z. Gao, A. Agarwal, A.D. Trigg, N. Singh, C. Fang, C.-H. Tung, Y. Fan, K.D. Buddharaju and J. Kong, "Silicon nanowire arrays for label-free detection of DNA", *Analytical Chemistry*, 79 (2007), 3291-3297
- [39] S. Chen, J.G. Bomer, W.G. van der Wiel, E.T. Carlen and A. van der Berg, "Top-Down fabrication of sub-30 nm monocrystalline silicon nanowires using conventional microfabrication", *American Chemical Society Nano*, 3 (2009), 3485-3492
- [40] B. Reddy, B.R. Dorvel, J. Go, P.R. Nair, O.H. Elibol, G.M. Credo, J.S. Daniels, E.K.C. Chow, X. Su, M. Varma, M.A. Alam, and R. Bashir, "High-k dielectrics Al₂O₃ nanowire and nanohotplate field effect sensors for improved pH sensing", *Biomedical Microdevices*, 13 (2011) 335-344
- [41] K. Bedner, V.A. Guzenko, A. Tarasov, M. Wipf, R.L. Stoop, D. Just, S. Rigante, W. Fu, R.A. Minasawa, C. David, M. Calame, J. Gobrecht and C. Schönenberger, "pH response of silicon nanowires sensors: impact of nanowire width and gate oxide", *Sensors and Materials*, 25 (2013) 567-576
- [42] N. Lu, A. Gao, P. Dai, T. Li, Y. Wang, X. Gao, S. Song, C. Fan and Y. Wang, "Ultra-sensitive nucleic acids detection with electrical nanosensors based on CMOS-compatible silicon nanowire field-effect transistors", *Methods*, 63 (2013) 212-218
- [43] E. Buitrago, M. Fernandez-Bolanos, S. Rigante, C.F. Zilch, N.S. Schröter, A.M. Nightingale and A.M. Ionescu, "The top-down fabrication of a 3D-integrated, fully CMOS-compatible

- FET biosensor based on vertically stacked SiNWs and FinFETs", *Sensors and Actuators*, B193 (2014) 400-412
- [44] D. Rani, V. Pachauri, A. Mueller, X.T. Vu, T.C. Nguyen and S. Ingebrandt, "On the use of scalable NanoISFET arrays of silicon with highly reproducible sensor performance for biosensor applications", *American Chemical Society Omega*, 1 (2016) 84-92
- [45] A. Casanova, M.-C. Blatché, F. Mathieu, L. Bettamin, H. Martin, D. Gonzalez-Dunia, L. Nicu and G. Larrieu, "Integration of FinFETs and 3D nanoprobe devices on a common bio-platform for monitoring electrical activity of single neurons", 2017 IEEE International Electron Devices Meeting, IEDM, 26.4.1-4, <https://doi.org/10.1109/IEDM.2017.8268464>
- [46] X. Yang, A. Gao, Y. Wang and T. Li, "Wafer-level and highly controllable fabricated silicon nanowire transistor arrays on (111) silicon-on-insulator (SOI) wafers for highly sensitive detection in liquid and gaseous environments", *Nano Research*, 11 (2018), 1520-1529
- [47] C.-C. Wu, Y.B. Manga, M.-H. Yang, Z.-S. Chien and K.-S. Lee, "Label-free detection of BRAF^{V599E} gene mutation using side-gated nanowire field effect transistors", *Journal of the electrochemical society*, 165 (2018), B576-B581
- [48] K. Zhou, Z. Zhao, L. Pan and Z. Wang, "Silicon nanowire pH sensors fabricated with CMOS compatible sidewall mask technology", *Sensors and actuators*, B279 (2019), 111-121
- [49] S.-K. Cho and W.-J. Chu, "Ultra-high sensitivity pH-sensors using silicon nanowire channel dual-gate field-effect transistors fabricated by electrospun polyvinylpyrrolidone nanofibers pattern template transfer", *Sensors and actuators*, B326 (2021), 128835-1 – 128835-8
- [50] T.S. Pui, A. Agarwal, F. Ye, Z.Q. Tou, Y. Huang and P. Cheng, "Ultra sensitivity detection of adipocytokines with CMOS compatible silicon nanowire arrays", *Nanoscale*, 1 (2009), 159-163
- [51] A. Lale, E. Scheid, F. Cristiano, L. Datas, B. Reig, J. Launay and P. Temple-Boyer, "Study of aluminium oxide thin films deposited by plasma-enhanced atomic layer deposition from tri-

- methyl-aluminium and dioxygen precursors: investigation of interfacial and structural properties", *Thin Solid Films*, 666 (2018), 20-27
- [52] R. Ritzenthaler, F. Lime, O. Faynot, S. Cristoloveanu and B. Iñiguez, "3D analytical modelling of subthreshold characteristics in vertical multiple-gate FinFET characteristics", *Solid-State Electronics*, 65-66 (2011) 94-102
- [53] A. Lale, M. Joly, S. Mekkaoui, X. Joly, E. Scheid, J. Launay and P. Temple-Boyer, "Effect of thermal annealing on the dielectric, passivation and pH detection properties of aluminium oxide thin films deposited by plasma-enhanced atomic layer deposition", *Thin Solid Films*, 732 (2021) 138761.1-138761.10
- [54] C. Christophe, F. Sékli Belaïdi, J. Launay, P. Gros, E. Questel and P. Temple-Boyer, "Elaboration of integrated microelectrodes for the detection of antioxidant species", *Sensors and Actuators*, B177 (2013) 350-356
- [55] M.L. Pourciel Gouzy, S. Assié Souleille, L. Mazonq, J. Launay, P. Temple-Boyer, "pH-ChemFET-based analysis devices for the bacterial activity monitoring", *Sensors and Actuators*, B134 (2008) 339-344
- [56] F. Larramendy, L. Mazonq, P. Temple-Boyer and L. Nicu, "Three-dimensional close microfluidic channels fabrication by stepper projection single step lithography: the *diabolo* effect", *Lab on chip*, 12 (2012) 387-390
- [57] X.P.A. Gao, G. Zheng, and C.M. Lieber, "Subthreshold regime has the optima sensitivity for nanowire FET biosensors", *Nano Letters*, 10 (2010) 547-552
- [58] N.K. Rajan, X. Duan and M.A. Reed, "Performance limitations for nanowire/nanoribbon biosensors", *Wiley Interdisciplinary Reviews: Nanomedicine and Nanobiotechnology*, 5 (2013) 629-45

Tables and figures captions

Table 1: typical width of studied nanostructures according to photolithographic parameters (focus depth is chosen to obtain 90° vertical walls for the photoresist nanopatterns)

Table 2: electrical characteristics of single-nanowire SiNW-FET and SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 μm, nanowire length: ~ 10 μm)

Figure 1: fabrication of AZ ECI 3012 photoresist nanopatterns (thickness: 1.2 μm)
a) variations with the UV exposure dose of the focus depth to obtain vertical side walls and associated final photoresist nanopattern width
b) SEM picture (tilt: 52°) of 1.2 μm-thick, 270 nm-wide photoresist patterns

Figure 2: SEM pictures (tilt: 52°) of 240 nm-wide silicon nanofins after the SF₆/C₄F₈/O₂ RIE process

Figure 3: SEM pictures (tilt: 52°) of test devices for the definition of 200 nm-wide silicon nanofins
a) after the first partial etching of the thin silicon upper layer outlining the silicon nanofins
b) after the second and final etching of the thin silicon upper layer

Figure 4: Schematics of the suspended N⁺/P/N⁺ double-junction SiNW-ISFET adapted to liquid phase analysis by wafer-level packaging
a) before the SU-8 film integration, b) with the integrated SU-8-based microfluidic channel

Figure 5: SEM sectional picture of a silicon nanowire (width: 170 nm, height: 220 nm) obtained by reactive ion etching (RIE) and thermal oxidation of a SOI substrate silicon upper layer

Figure 6: SEM picture (tilt: 52°) of suspended N⁺/P/N⁺ silicon nanowires (gate length: ~ 0.75 μm) integrated on a SOI substrate

Figure 7: microfabrication of SiNW-FET and SiNW-ISFET devices on a 6-inch silicon wafer (chip size: 7 × 8 mm², device number per chip: 16)

Figure 8: integration of SU8-based microfluidic structures on SiNW-ISFET chips using photolithographic-based wafer-level packaging

Figure 9: SEM picture (tilt: 52°) of suspended N⁺/P/N⁺ SiNW-ISFET integrated into SU8 microfluidic channels for the liquid phase analysis at the submicronic scale (analysis volume around 5 × 5 × 500 μm³)

Figure 10: Electrical characterization of "150 nm-wide – 200 nm-high" SiNW-FET devices

- a) I_D(V_{DS}) curves obtained for a single nanowire (gate length: 0.75 μm)
- b) I_D(V_{GS}) semi-logarithmic curves obtained for different nanowire configurations (V_{DS} = 0.1 V)
- c) I_D(V_{GS}) curves obtained for different nanowire configurations (V_{DS} = 0.1 V)
- d) transconductance variations with the V_{DS} voltage for 100-nanowire configurations (gate lengths: 0.75 μm and 3.75 μm)

Figure 11: Electrical characterization of "150 nm-wide – 200 nm high" SiNW-ISFET devices

- a) I_D(V_{GS}) semi-logarithmic curves obtained for different nanowire configurations (V_{DS} = 1 V, pH = 4)
- b) I_D(V_{GS}) linear curves obtained for different nanowire numbers (L_G ≈ 0.75 μm, V_{DS} = 1 V, pH = 4)

Figure 12: pH detection properties of 150 nm-wide – 200 nm-high" SiNW-ISFET devices

- a) I_D(V_{GS}) curves obtained for a single nanowire (gate length: L_G ≈ 0.75 μm) for different buffer solutions (V_{DS} = 1 V, pH = 4, 7 and 10)
- b) I_D(V_{GS}) curves obtained for a 100-nanowire configuration (gate length: L_G ≈ 0.75 μm) for buffer solutions going down and back from pH = 9 and pH = 3 (V_{DS} = 1 V)

photolithographic parameters		typical widths		
UV exposure dose	focus depth	mask nanopattern	photoresist nanopattern	silicon nanofin
615 J/m ²	- 0.45 mm	300 nm	290 nm	290 nm
670 J/m ²	- 0.27 mm	300 nm	240 nm	240 nm
720 J/m ²	- 0.11 mm	300 nm	190 nm	190 nm

Table 1: typical width of studied nanostructures according to photolithographic parameters (focus depth is chosen to obtain 90° vertical walls for the photoresist nanopatterns)

	single nanowire SiNW-FET	single nanowire SiNW-ISFET
threshold voltage V_T	0.6 ± 0.2 V	0.85 ± 0.23 V at pH = 4
serie resistance R_S	3 k Ω	3 k Ω
gate resistance R_G	10^{17} Ω	$> 7 \times 10^{12}$ Ω
leakage resistance R_{OFF}	3×10^{14} Ω	$> 2 \times 10^{12}$ Ω
subthreshold slope	0.167 V per current decade	0.11 V per current decade
resistance R_{ON} at $V_{DS} = 1$ V	125 k Ω	62.5 k Ω
$(I_{ON}/I_{OFF})_{max}$	4×10^9	$> 6 \times 10^7$

Table 2: electrical characteristics of single-nanowire SiNW-FET and SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 μm , nanowire length: ~ 10 μm)

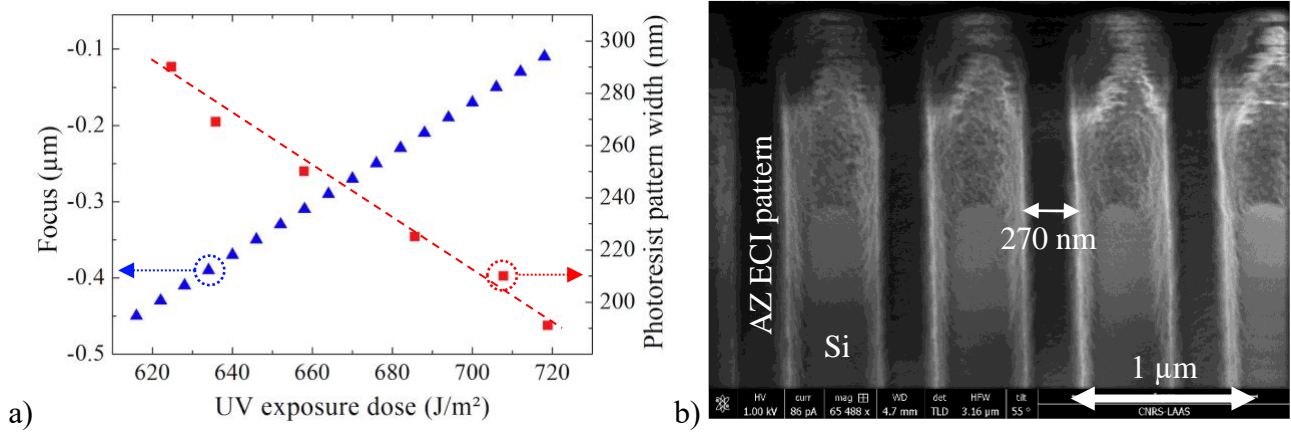


Figure 1: fabrication of AZ ECI 3012 photoresist nanopatterns (thickness: 1.2 μm)
 a) variations with the UV exposure dose of the focus depth to obtain vertical side walls and associated final photoresist nanopattern width
 b) SEM picture (tilt: 52°) of 1.2 μm -thick, 270 nm-wide photoresist patterns

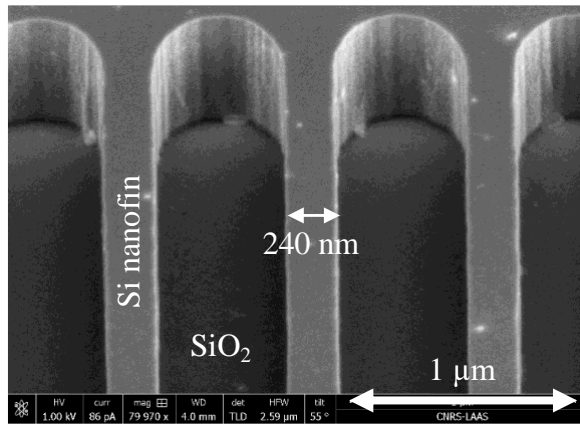


Figure 2: SEM picture (tilt: 52°) of 240 nm-wide silicon nanofins after the SF₆/C₄F₈/O₂ RIE process

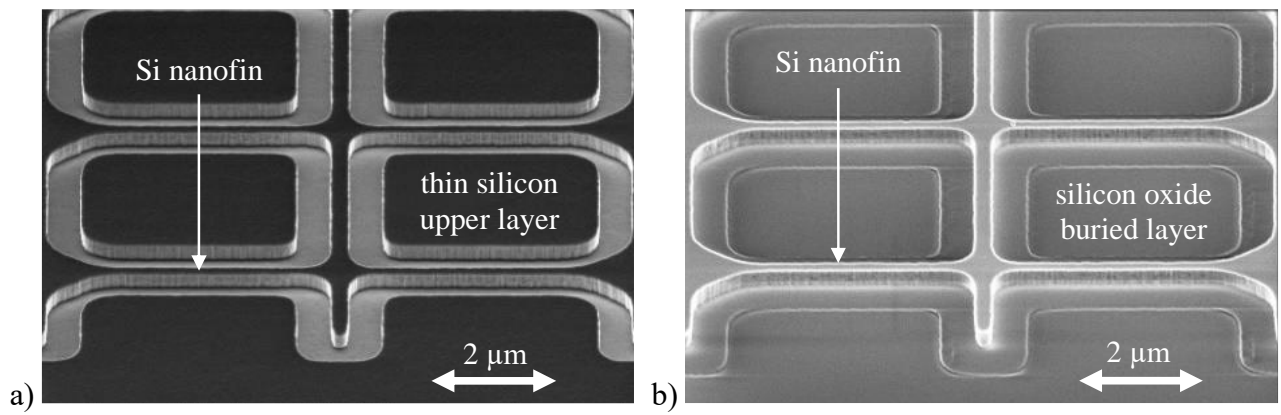


Figure 3: SEM pictures (tilt: 52°) of test devices for the definition of 200 nm-wide silicon nanofins
a) after the first partial etching of the thin silicon upper layer outlining the silicon nanofins
b) after the second and final etching of the thin silicon upper layer

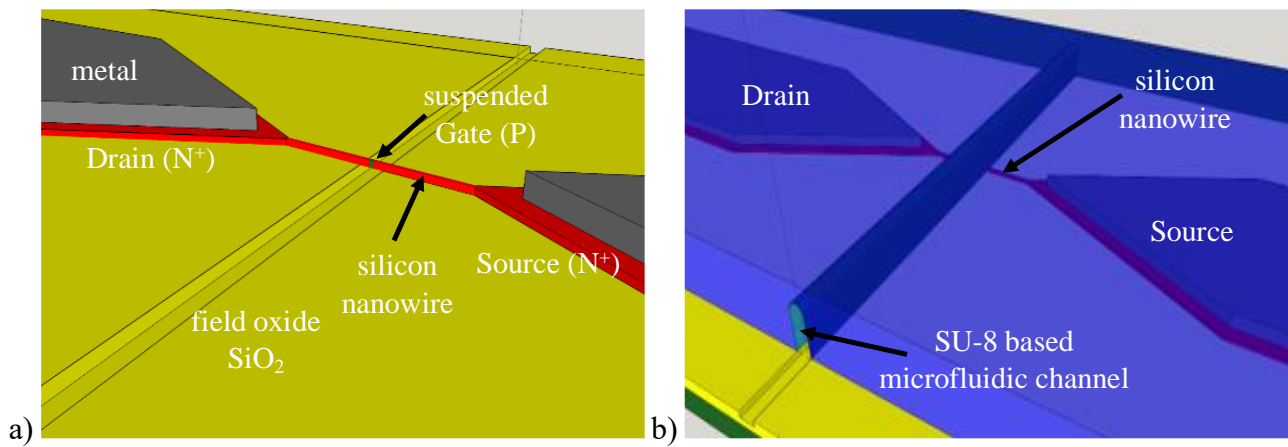


Figure 4: Schematics of the suspended $N^+/P/N^+$ double-junction SiNW-ISFET adapted to liquid phase analysis by wafer-level packaging
 a) before the SU-8 film integration, b) with the integrated SU-8-based microfluidic channel

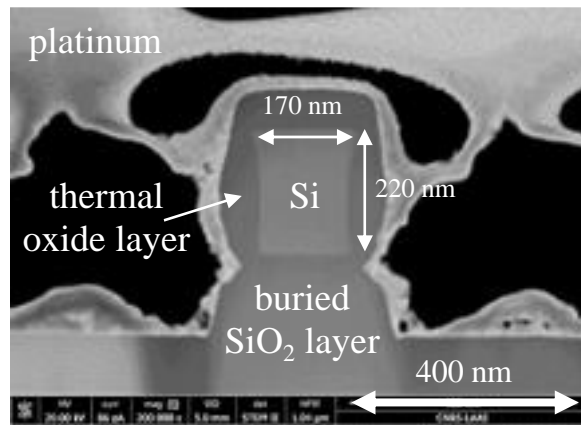


Figure 5: SEM sectional picture of a silicon nanowire (width: 170 nm, height: 220 nm) obtained by reactive ion etching (RIE) and thermal oxidation of a SOI substrate silicon upper layer

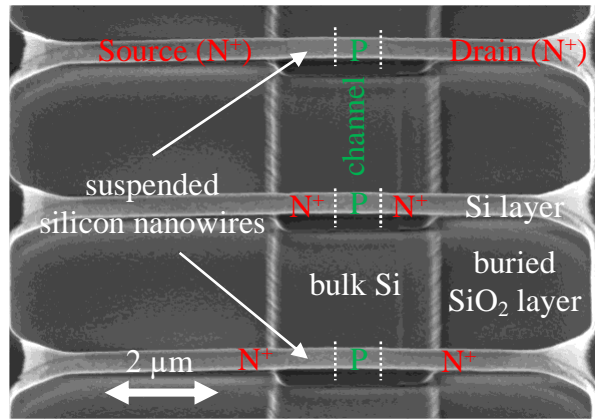


Figure 6: SEM picture (tilt: 52°) of suspended N⁺/P/N⁺ silicon nanowires (gate length: ~ 0.75 μm) integrated on a SOI substrate

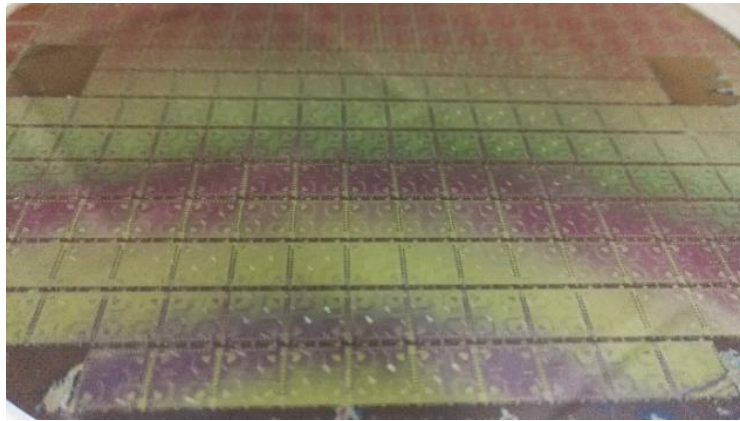


Figure 7: microfabrication of SiNW-FET and SiNW-ISFET devices on a 6-inch silicon wafer (chip size: $7 \times 8 \text{ mm}^2$, device number per chip: 16)

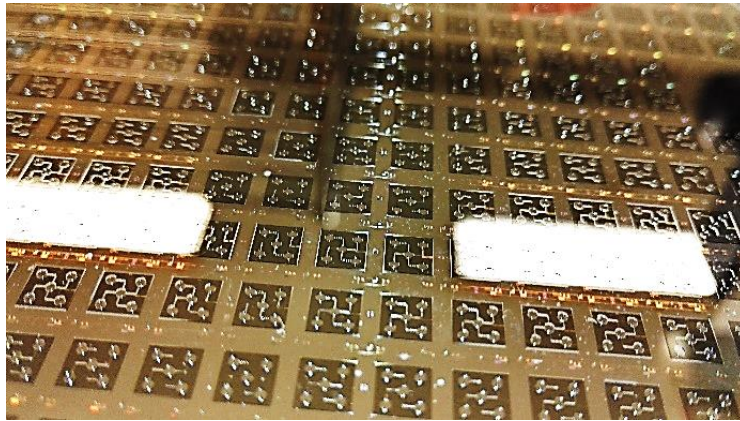


Figure 8: integration of SU8-based microfluidic structures on SiNW-ISFET chips using photolithographic-based wafer-level packaging

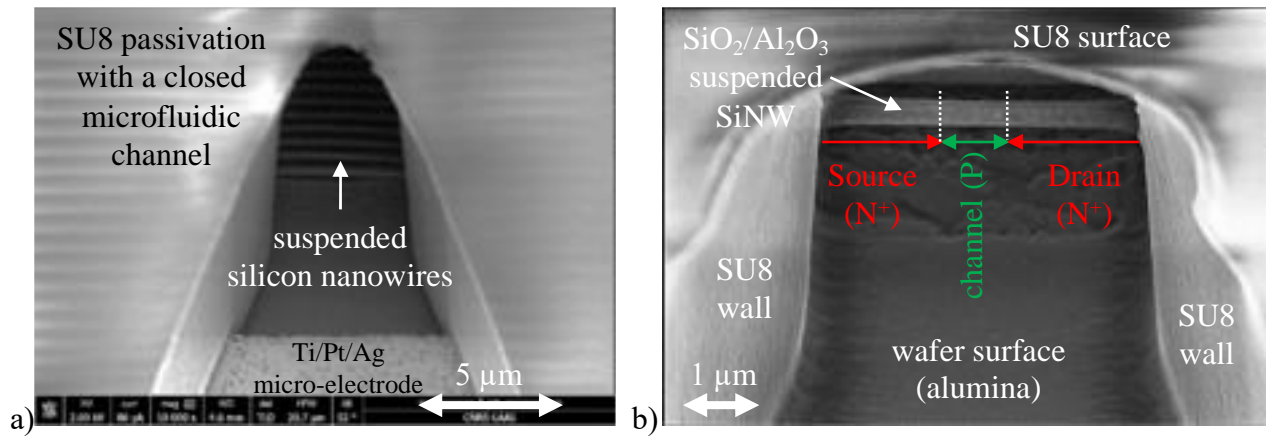


Figure 9: SEM picture (tilt: 52°) of suspended N⁺/P/N⁺ SiNW-ISFET integrated into SU8 microfluidic channels for the liquid phase analysis at the submicronic scale (analysis volume around 5 × 5 × 500 μm³)

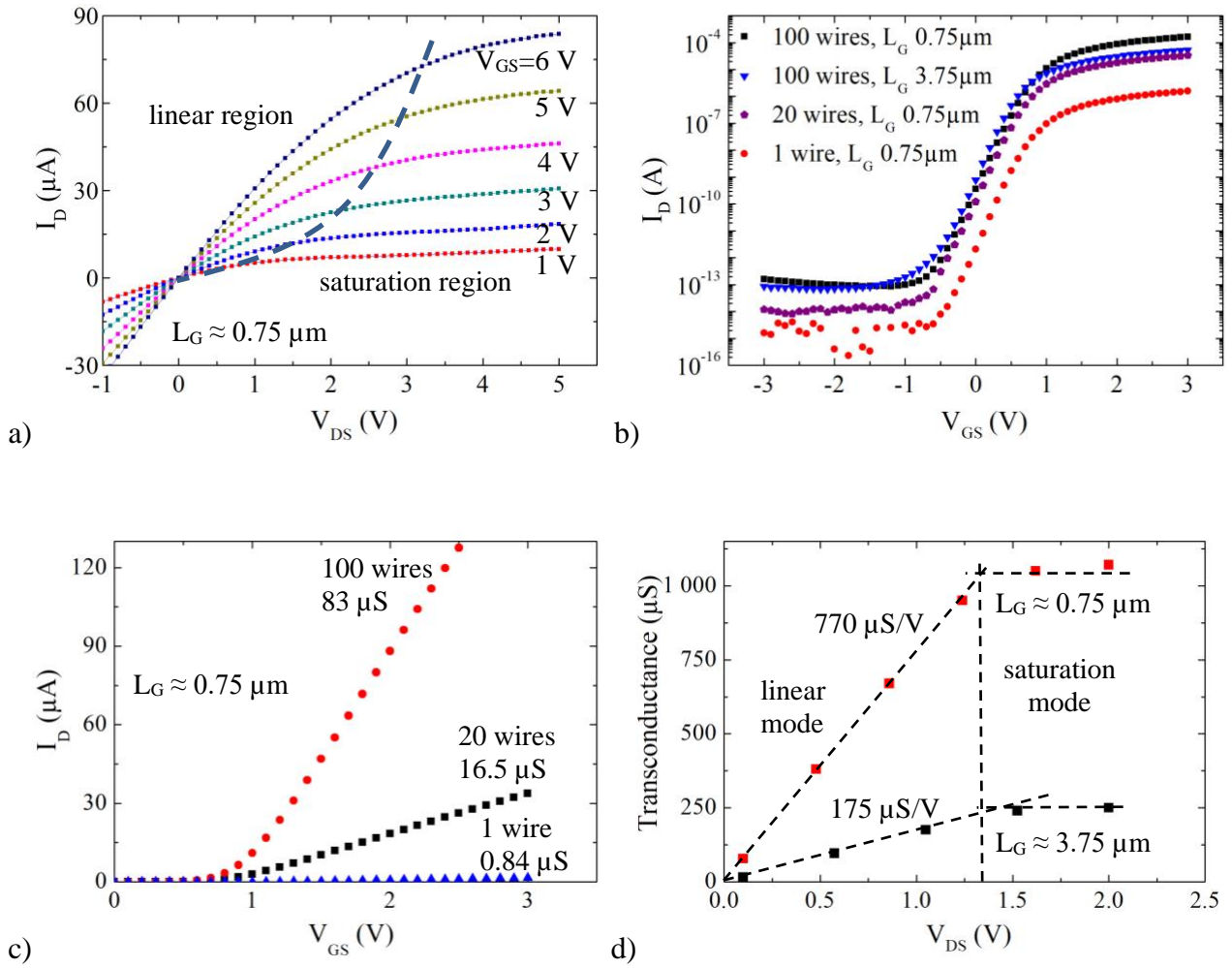


Figure 10: Electrical characterization of "150 nm-wide – 200 nm-high" SiNW-FET devices
 a) $I_D(V_{DS})$ curves obtained for a single nanowire (gate length: 0.75 μm)
 b) $I_D(V_{GS})$ semi-logarithmic curves obtained for different nanowire configurations ($V_{DS} = 0.1$ V)
 c) $I_D(V_{GS})$ curves obtained for different nanowire configurations ($V_{DS} = 0.1$ V)
 d) transconductance variations with the V_{DS} voltage for 100-nanowire configurations (gate length: 0.75 μm and 3.75 μm)

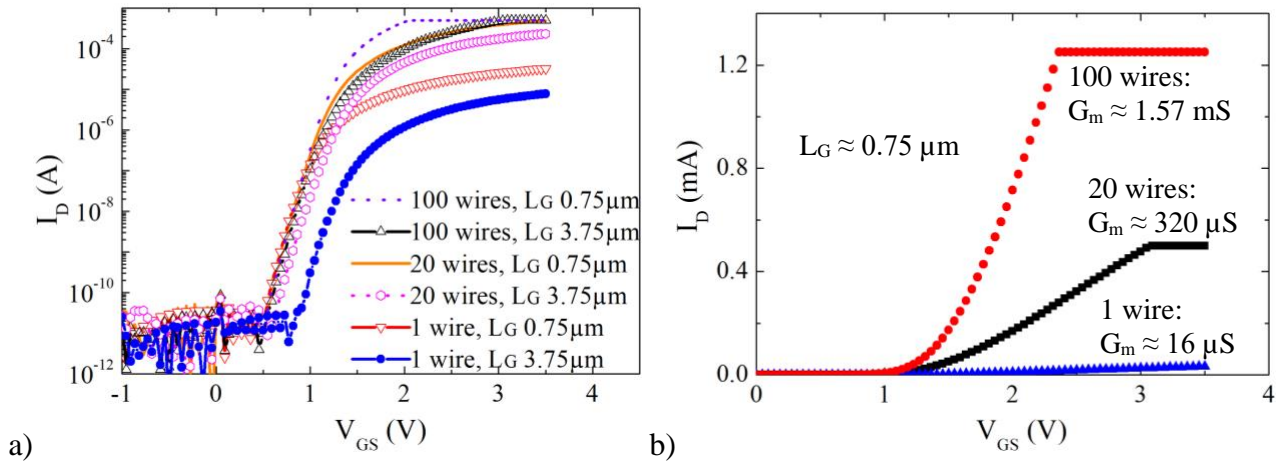


Figure 11: Electrical characterization of "150 nm-wide – 200 nm high" SiNW-ISFET devices
a) $I_D(V_{GS})$ semi-logarithmic curves obtained for different nanowire configurations ($V_{DS} = 1 \text{ V}$, $\text{pH} = 4$)
b) $I_D(V_{GS})$ linear curves obtained for different nanowire numbers ($L_G \approx 0.75 \mu\text{m}$, $V_{DS} = 1 \text{ V}$, $\text{pH} = 4$)

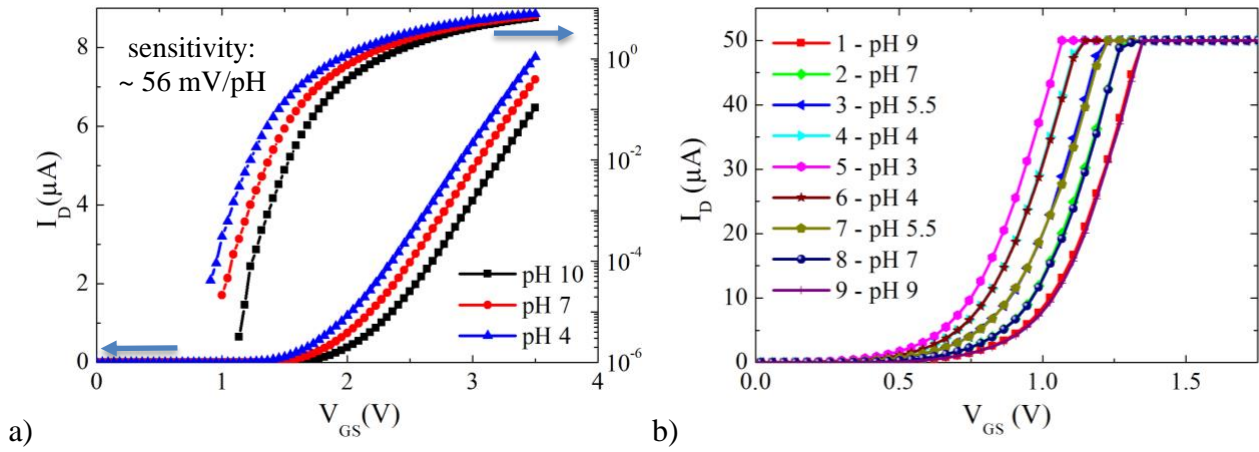


Figure 12: pH detection properties of 150 nm-wide – 200 nm-high" SiNW-ISFET devices
 a) $I_D(V_{GS})$ curves obtained for a single nanowire (gate length: $L_G \approx 0.75 \mu\text{m}$)
 for different buffer solutions ($V_{DS} = 1 \text{ V}$, pH = 4, 7 and 10)
 b) $I_D(V_{GS})$ curves obtained for a 100-nanowire configuration (gate length: $L_G \approx 0.75 \mu\text{m}$)
 for buffer solutions going down and back from pH = 9 and pH = 3 ($V_{DS} = 1 \text{ V}$)