Top-down integration of suspended N+/P/N+ silicon-nanowire-based ion-sensitive field effect transistors for pH analysis at the submicronic scale

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Abstract: A technological process was proposed in order to integrate fully silicon-nanowire-based field-effect nanodevices on a silicon-on-insulator (SOI) substrate. Thanks to a double reactive ion etching process of the SOI silicon upper layer as well as to a "SiO_2 thermal oxidation growth / Al_2O_3 atomic layer deposition" gate process, silicon-nanowire-based field-effect transistors (SiNW-FET) and silicon-nanowire-based ion-sensitive field-effect transistors (SiNW-ISFET) were fabricated. Focuses were brought on (i) the integration of a suspended $N^+/P/N^+$ double-junction structure (gate length: ~ 0.75 µm and ~ 3.75 µm), (ii) the fabrication of a SiO_2/Al_2O_3 all-around surrounding gate structure, (iii) the achievement of low nanowire sections (width: ~ 150 nm, height: ~ 200 nm), and (iv) the final adaptation to the liquid phase analysis thanks to SU8-based wafer-level packaging. According to the proposed process, SiNW-FET and SiNW-ISFET devices showed excellent electrical characteristics in terms of leakage resistance R_{OFF}, subthreshold current slope and I_{ON}/I_{OFF} maximal ratio. SiNW-ISFET devices were finally studied for the pH analysis at the submicronic scale (analysed volumes: ~ 10 pL), evidencing standard potentiometric detection sensitivity (~ 56 mV/pH), as well as excellent amperometric detection sensitivity (~ 0.4 current decade per pH) in subthreshold regime.

Keywords: silicon nanowire, double-junction nanochannel, silicon nanowire field-effect transistor, silicon nanowire ion-sensitive field-effect transistor, measurement in liquid phase, micro-analysis

1. Introduction

In the frame of silicon-based technologies, field-effect transistors were thoroughly developed for electronic devices [1] as well as potentiometric sensors [2-4]. Focusing on the conventional metal-oxide-semiconductor field-effect transistors (MOSFET), this interest was associated to two main advantages conferred by silicon use. Firstly, its thermal oxidation enables the formation of Si/SiO_2 capacitive structures with excellent dielectric properties. Secondly, its semi-conductive properties enable the elaboration of P-type and N-type doped regions, and therefore P/N-based junctions or double-junctions. As a result, developing simultaneously the Gate and Source/Drain engineering, N-channel and P-channel MOSFET were microfabricated. Consequently, combined with the CMOS (complementary metal-oxide-semiconductor) technology achievement, MOSFET devices were microfabricated while reducing size, increasing density, improving performances and decreasing costs, leading to the very large-scale integration (VLSI) of electronic circuits [5,6]. Lastly, technological developments were extended to FET-based transducers such as chemical/biological field effect-transistors (ChemFET/BioFET) [3,4,7,8].

Considering the technological scaling down, bottlenecks were mainly associated to the previously quoted advantages of silicon. Concerning the Gate engineering, efforts were focused on the Si/SiO_2 capacitor, aiming to the gate oxide thickness decrease without increasing leakage currents. As a matter of fact, even if silicon gets hardly rid of its oxide SiO_2, plenty of dielectric metallic oxides were studied for conventional MOSFET-based devices [9,10] and further extended to ChemFET/BioFET sensors for liquid phase analysis [11]. In this context, aluminium oxide Al_2O_3 was emphasized due to high dielectric constant ($\varepsilon_r \approx 10$), good interfacial properties, high chemical and thermal stabilities at high temperature (< 750°C) and excellent insulation/passivation properties in water-based solutions [12].

In the frame of Source/Drain engineering, several technological solutions were proposed to decrease the P/N junction size [13,14]. Nevertheless, with scaling down, the concept of junctionless transistors (JLT) was brought up to date [15,16]. Compared to the conventional MOSFET one, the JLT device does not need any PN junction to operate properly while using very thin (< 10 nm) and heavily doped (> 10^{19} at/cm^3) silicon channels. Consequently, thanks to ultra-thin silicon-on-insulator substrates, CMOS-compatible JLT technologies were proposed, emphasizing different channel geometries, such as thin films, nanofins and nanowires [17].

As part of ChemFET/BioFET microsensors, the JLT technology was further limited. Indeed, their performances are affected by gate leakage currents, usually specific of water analysis. Since the phenomenon is directly proportional to the gate sensitive surface, the use of nanowires took precedence over those of nanofins or thin films. As a result, silicon-nanowire field effect transistors (SiNW-FET) were mainly developed for the potentiometric analysis of ionic species and (bio)molecules in liquid phase [18,19].

All in all, the compromise between "Junction nanowire" or "Junctionless nanowire" technologies had to be solved while dealing with nanobiosensors. As a matter of fact, considering the "Bottom-up" approach associated to silicon nanowires (SiNW) grown by "Vapor – Solid – Liquid" technique [20], this compromise was of little importance: since the SiNW in-situ doping enables the formation of any type of junctions, both technologies were proposed [21-25]. Anyway, the "Top-down" approach was preferred in order to further improve fabrication yield and reproducibility. On the one hand, the "junctionless SiNW-FET" technology was developed since it is associated to simpler, easier and cheaper technological processes [26-30]. On the other hand, junction-based SiNW-FET were also studied, while tackling off different technological bottlenecks [31-36]. Thus, technological processes were studied, either based on the sidewall spacer technique applied to polysilicon thin films [31,32,34], or on optimized etching of polysilicon layers [33,35,36]. Nevertheless, in order to integrate fully monocrystalline, double-junction-based SiNW-

FET devices [37-49], the use of silicon-on-insulator (SOI) substrates allowed finally innovative, CMOS-compatible, top-down technological processes such as: supper lattice nanowire pattern transfer [37], plasma dry etching [38,43,45,47,49], (100) and (111) wet anisotropic etching [39-42,44,46], and sidewall mask technology [48].

This paper proposes to investigate the fabrication of silicon-nanowire-based ion-sensitive field effect transistors (SiNW-ISFET) while integrating a suspended $N^+/P/N^+$ double-junction structure through the development of a double reactive ion etching (RIE) process, and to study their electrical performances in the frame of pH analysis at the submicronic scale.

2. Experimental details

All the technological developments were performed in the LAAS-CNRS cleanroom facility by relying on previously-studied silicon-based processes and related equipment. In this case, scanning electron microscopy (SEM) observations were performed with a FEI Helios 600i system using a high-resolution electron column based on a Schottky field emission gun. Photoresist patterns were imaged at an accelerating voltage of 1 kV and a current of 86 pA, the others samples were analysed at 30 kV and 86 pA.

2.1. Microfabrication of silicon nanofins by reactive ion etching

To fabricate silicon nanofins, a photolithographic process was developed in order to carry out masking nanopatterns thanks to a CANON FPA3000i4 "Lithography by projection" stepper. The AZ ECI 3012 photoresist (provided by Microchemicals) was chosen for its development resolution (400 nm) and an AZ BARLI II bottom anti-reflexive coating (BARC, also provided by

Microchemicals) was moreover used (thickness: 200 nm). By preventing UV reflections on the silicon substrate, this coating allows to improve the masking resolution under 300 nanometres.

Using specifically oxidized (field oxide thickness: 65 nm) P-type (boron doping: 10^{15} at/cm^3) silicon substrate, the photolithographic process was optimized in order to achieve photoresist nanopatterns adapted to the BARC/SiO_2/Si reactive ion etching (RIE) step, leading to the fabrication of silicon nanowires. Considering a photoresist thickness around 1.2 µm, a compromise had to be found between the UV exposure dose, whose increase is responsible for the nanopattern width decrease towards zero, and the focus depth, whose increase is responsible for photoresist wall steepness lower than 90° (clearly non-adapted to the RIE process). According to simulation results achieved with the GENISYS software (not shown), the following ranges were finally defined in order to obtain a 90° steepness:

- UV exposure dose: [600 J/m^2 – 800 J/m^2],
- focus depth: [- 0.1 µm – - 0.5 µm].

Thus, considering the final fabrication of single silicon nanowires as well as parallel networks of silicon nanowires, photolithographic parameters were optimized in order to fabricate 1.2 µm-thick photoresist nanopatterns, with vertical side walls and widths ranging from 190 to 290 nanometres (figure 1).

Consequently, technological developments were dedicated to the photoresist nanopattern transfer into a silicon substrate by inductively-coupled plasma reactive ion etching (ICP-RIE), using a TRIKON OMEGA 21 equipment. This technological process implied three different RIE steps to etch the 200 nm-thick BARC coating, the 65 nm-thick field oxide SiO_2 and the silicon substrate (P-type, boron doping: 10^{15} at/cm^3):

- BARC: $O_2/CF_4/CHF_3$/Ar plasma (P_{ICP} = 300 W, P_{bias} = 40 W, p = 0.666 Pa),

- SiO_2: CHF_3 plasma (P_{ICP} = 500 W, P_{bias} = 60 W, p = 0.666 Pa),

- Si(P): $SF_6/C_4F_8/O_2$ plasma (P_{ICP} = 450 W, P_{bias} = 30 W, p = 0.8 Pa).

The first BARC RIE step was characterized by an etch rate around 350 nm/min. As non-selective towards the photoresist layer, the etching duration should be controlled precisely, any time overrun being responsible for the nanopattern deterioration. The second etching step is associated to a standard RIE process of silicon dioxide SiO_2, whose etch rate was previously studied (~ 20 nm/min). Finally, concerning the Si(P) RIE step, the $SF_6/C_4F_8/O_2$-based plasma was preferred to the Cl_2 one. Indeed, the etch rate around 190 nm/min led to good results for etching homogeneity and verticality. This last property is related to the sidewall passivation during the deep silicon etching, decreasing significantly lateral phenomena. As a result, the final silicon nanofins so manufactured had a similar width than the photoresist nanopatterns, thus ranging from 190 to 290 nanometres (table 1 and figure 2).

2.2. Transfer of the silicon nanowire microfabrication on SOI substrates

In order to achieve junction-based SiNW-ISFET devices, a silicon-on-insulator (SOI) substrate was specifically required in order to fabricate silicon nanowires and to define precisely their geometry. The technological process was therefore designed while considering a 6-inch (100) SOI substrate (provided by SOITEC) with the following characteristics:

- upper silicon layer: P-type (boron doping: 10^{15} at/cm^3), thickness: 280 nm,

- buried SiO_2 layer: thickness: 1 µm,

- silicon substrate: P-type (boron doping: 10^{15} at/cm^3), thickness: ~ 675 µm.

To be compatible with the final SiNW-ISFET technological process, the previous microfabrication process (see §2.1) had to be used while considering the SOI substrate upper field oxide (thickness: 65 nm). At first glance, this substrate modification should not change the photolithographic and RIE processes to pattern photoresist and etch the BARC/SiO_2/Si structure. Nevertheless, an unexpected problem occurred due to the wall passivation properties of the $SF_6/C_4F_8/O_2$-based plasma. Since etched patterns were characterized by different geometries (single nanowire versus parallel networks of nanowires) as well as different surface densities, it was expected to over etch locally the buried SiO_2 layer in order to obtain a good etching homogeneity all around the wafer. Unfortunately, according to passivation phenomena due to the $SF_6/C_4F_8/O_2$-based plasma, this over etching was responsible for by-product deposition on the silicon nanowire sidewalls, preventing the successful integration of SiNW-based FET.

In order to tackle off this technological bottleneck, a double RIE process (requiring two photolithographic masks) was developed for the final fabrication of silicon nanowires on an SOI substrate. The first mask was designed in order to etch partially the upper silicon layer, outlining the silicon nanowire patterns. Thus, using a constant opening/etching width all around the wafer, the silicon etch rate was thoroughly controlled, preventing any over etching of the buried SiO_2 layer. Then, the second mask was designed in order to etch the remaining silicon layer while protecting the previously-made silicon nanofins. Thus, the RIE process was carried out on the whole wafer, preventing any sidewall parasitic deposition associated to the buried SiO_2 layer (figure 3).

2.3. Integration of $N^+/P/N^+$ silicon nanowire ion-sensitive field effect transistors

The SiNW-ISFET process was developed to product an $N^+/P/N^+$ silicon nanowire between the source and drain contacts and to adapt the final device to liquid phase analysis thanks to

microfluidic structures fabricated by wafer level packaging (figure 4). The different nanodevices geometries and characteristics were defined as following:

- number of parallel silicon nanowires: 1, 20 and 100,
- silicon nanowire initial width: 300 nanometres,
- silicon nanowire length: 2, 5, 10 and 20 micrometres,
- gate length: 2 and 5 micrometres.

First of all, specific simulations were performed using the SILVACO ATHENA™ software in order to optimize the implantation/diffusion processes associated to the creation of the N^+ source and drain regions into the chosen P-type SOI substrate. To that end, using a pre-implantation oxide (thickness: 11 nm), an arsenic-based implantation (energy: 15 keV, dose: 5×10^{15} at/cm^3) was chosen in order to control lateral diffusion of the N^+ regions into the P-type upper silicon layer around 1.25 µm. After removing this arsenic-rich oxide using hydrofluoric acid (HF), a diffusion/activation anneal at 1070°C was performed under an O_2 ambient, causing the growth of a 65 nm-thick field oxide on P-type regions. Then, the double RIE process (see below) was performed in order to fabricate $N^+/P/N^+$ silicon nanowires with the following widths:

- silicon nanowire width: ~ 190, ~ 240 and ~ 290 nanometres,
- silicon nanowire height: ~ 240 nanometres.

At this stage, a first gate oxide (thickness: 20 nm) was grown by thermal oxidation at 1000°C and further removed into HF cleaning. According to the thermal oxidation of silicon [5,50], these technological steps lead to the silicon sidewall smoothing while decreasing the silicon nanowire width and height (figure 5):

- silicon nanowire width: ~ 170, ~ 220 and ~ 270 nanometres,

- silicon nanowire height: ~ 220 nanometres.

Then, a specific photolithographic mask was used in order to etch completely the buried oxide layer on either side of the $N^+/P/N^+$ double junction structure thanks to an HF cleaning. This gate opening step was responsible for the silicon nanowire suspension (figure 6), allowing the final fabrication of an all-around surrounding gate and preparing them for water-based analysis into microfluidic structures.

Afterwards, the gate insulator was fabricated. After an RCA cleaning, a silicon oxide SiO_2 layer (thickness: 20 nm) was grown by thermal oxidation at 1000°C and an amorphous alumina Al_2O_3 layer (thickness: 25 nm) was deposited on top by atomic layer deposition with tri-methyl-aluminium $Al(CH_3)_3$ and dioxygen O_2 as precursors [51]. Due to deposition process conformity, an SiO_2/Al_2O_3 all-around surrounding gate structure, whose advantages were previously demonstrated [52], was achieved. Simultaneously, the Al_2O_3 layer ensured insulation/passivation properties in water-based solutions [53], aiming to the SiNW-ISFET improvement. As previously, after this new thermal oxidation step, the silicon nanowire width and height were further decreased and the channel length reached its final value (as simulated using the SILVACO ATHENA™ software):

- silicon nanowire width: ~ 150, ~ 200 and ~ 250 nanometres,

- silicon nanowire height: ~ 200 nanometres,

- final gate length: ~ 0.75 and ~ 3.75 micrometres.

At this stage, the suspended $N^+/P/N^+$ SiNW-ISFET structures were structured. Hence, contact openings were made towards the source and drain N^+ regions by etching the upper alumina Al_2O_3

layer along with the field oxide layer, and a titanium/platinum/silver Ti/Pt/Ag (20 nm / 150 nm / 1000 nm) metallization was finally deposited by lift-off to form the contact pads. This metallic structure was previously studied for the integration of platinum-based electrochemical microcells ElecCell for water-based solution analysis, focusing on Ti/Pt counter and working microelectrode as well as on Ag/AgCl reference microelectrodes [54]. Its use is therefore required for the characterization of the SiNW-ISFET devices in liquid phase. According to their electrical properties, the Ti/Pt/Ag contact resistance was estimated to 10 Ω, whereas the resistance of the N^+-type silicon nanowire region was 300 ohms per micron (i.e. 3000 Ω for a 10 µm long nanowire).

It should finally be noted that, by integrating Ti/Pt/Ag metallic gates on specific silicon chips and Ti/Pt/Ag(AgCl) reference microelectrodes (using a specific electrochemical oxidation process of the silver upper metallic layer into a 0.01 M KCl solution [54]), the "Metallization" photolithographic mask allowed the simultaneous fabrication of both SiNW-FET and SiNW-ISFET devices (number per chip: 16) on 7 × 8 mm^2 silicon chips (figure 7).

2.4. Adaptation to the liquid phase analysis: from wafer-level to chip-level packaging

In order to adapt the SiNW-ISFET to the liquid phase, apart from the wafer-level alumina passivation layer (see §2.3), a previously-studied wafer-level packaging was used [55,56]. Starting from a SU8-based passivation layer (thickness: ≈ 7 µm) deposited by spin coating, UV photolithography was performed in order to fabricate hydrophilic, SU8-based, microfluidic structures (figure 8) such as microtanks (diameter: 1 mm) and closed microchannels (height: ~ 5 µm, width: ~ 5 µm). The full integration of the $N^+/P/N^+$ SiNW-ISFET and its Ti/Pt/Ag(AgCl) reference microelectrode into microfluidic channels (figure 9) allowed the final devices to be finally adapted to the analysis of microvolumes around a dozen of picolitres (typically: 5 × 5 × 500 $µm^3$).

Lastly, after dicing, the SiNW-ISFET silicon chips were placed on and connected electrically to a specific printed circuit board (PCB) using a SET FC150 flip-chip packaging system, ensuring the chip/PCB mechanical strength and the electrical bonding sealing thanks to an Epotek H70E glue and a Polytech EP601 underfill respectively. A Pyrex ring was finally glued on the PCB to create an upper tank on the SiNW-ISFET chip, facilitating liquid handling during electrical characterization.

2.5. Electrical characterization of the SiNW-FET and SiNW-ISFET devices

SiNW-FET devices were characterized on the wafer by probe testing in order to check the technological process before the SU8-based wafer-level packaging procedure (see §2.4). To that end, a wafer probe Cascade Summit 1200 and its Faraday cage were coupled to a Keithley 4200 analyser (current detection limit: 3×10^{-15} A).

For the SiNW-ISFET measurement in liquid phase, a metallic shielded room was used with the aim of preventing any electromagnetic or optical interferences. A Keithley 707 commutation system was employed to test simultaneously sixteen different microdevices, whereas current-voltage (I-V) characterization was performed using an Agilent 4142B analyser (current detection limit: 5×10^{-11} A). In addition, using standard pH = 4.0, pH = 7.0, pH = 10.0 buffers (provided by Sigma) were used combined with a Metrohm Ag/AgCl/KCl reference microelectrode to apply the gate voltage to the analysed samples. The experimental studies were finally focused on pH, pK and pNa measurements.

All the electrical characterizations were performed at ambient temperature (22 ± 1 °C).

3. Results and discussion

3.1. Electrical properties of the $N^+/P/N^+$ SiNW-FET devices

The SiNW-FET electrical characterization was performed for "150 nm-wide – 200 nm-high" silicon nanowires. For the two studied gate lengths (0.75 μm and 3.75 μm), classical NMOS $I_{DS}(V_{DS})$ analytical curves were found for increasing gate-source voltage V_{GS}, evidencing both linear and saturation modes, even for a "0.75 μm gate length" single nanowire (figure 10a). On the basis on 42 different devices, the threshold voltage V_T was estimated to 0.62 ± 0.26 V, whatever the gate length value and the nanowire number (1, 20 or 100).

Figure 10b shows the SiNW-FET $I_{DS}(V_{GS})$ semi-logarithmic curves obtained for different nanowire configurations (V_{DS} = 0.1 V). Hence, no variation of the off-state current I_{OFF} was evidenced for the two different gate lengths. Due to the 3 fA limitation, the I_{OFF} value obtained for a single nanowire SiNW-FET could not be measured experimentally. Nevertheless, since the 20-nanowire and 100-nanowire configurations were characterized by values around 15 fA and 70 fA respectively, the "single nanowire" I_{OFF} value was finally estimated to 0.7 fA. In fact, this value increased linearly with the drain-source voltage V_{DS} (result not shown). Thus, the corresponding conductance was estimated to 350 fS for a 100-nanowire device and, consequently, to 3.5 fS for a single nanowire (equivalent to a leakage resistance R_{OFF} around 3×10^{14} Ω). In the same way, the gate current I_G obtained for a single nanowire SiNW-FET was estimated to 0.03 fA for a 3 V gate-source voltage, corresponding to a gate resistance R_G around 10^{17} Ω.

The subthreshold slope was finally evaluated around 0.167 V per current decade, i.e. 6 current decades per volt, independently of the different "150 nm-wide – 200 nm-high" SiNW-FET configurations (figure 10b). Such low values were already shown for nano field-effect transistors (nanoFET) devices [52,57,58]. The I_{ON}/I_{OFF} ratio was finally analysed as a function of the drain-source voltage V_{DS} (result not shown). In all cases, the maximal I_{ON}/I_{OFF} ratio was obtained for around 0.8 V, estimated around 4×10^9 and 8×10^8 for the 0.75 μm and 3.75 μm gate lengths respectively.

According to the $I_{DS}(V_{GS})$ linear curves, the SiNW-FET transconductance G_m was also studied (figure 10c). This parameter was shown to increase linearly with the nanowire number. Based on this assumption, the R_{ON} resistance of single nanowire transistor was estimated to 1200 kΩ and 125 kΩ at a V_{DS} voltage value of 0.1 and 1 V respectively.

Lastly, the 100-nanowire configuration was used to study G_m variations (figure 10d). For both gate lengths (0.75 µm and 3.75 µm), the G_m value followed linear variations with the drain-source voltage V_{DS}, reaching saturation at approximatively 1.3 V. Slope values were estimated to 770 and 175 µS/V for 0.75 and 3.75 µm gate lengths respectively, evidencing a slope ratio around 4.4. According to the MOSFET theory, this slope ratio is correlated to the gate length ratio inverse, known to be equal to 5. As a consequence, based on this experimental value, the N^+ lateral diffusion into the P-type layer was estimated to 1.1 µm (rather than 1.25 µm as predicted by SILVACO ATHENA™ simulations), for effective gate lengths around 0.9 and 3.9 µm for both nanodevices respectively.

All in all, the electrical characteristics of the single-nanowire $N^+/P/N^+$ SiNW-FET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 µm, nanowire length: ~ 10 µm) were summarized in table 2.

3.2. Electrical properties of the $N^+/P/N^+$ SiNW-ISFET devices in the frame of a liquid phase analysis

The SiNW-ISFET electrical characterization was mainly performed for "150 nm-wide – 200 nm-high" silicon nanowires, using a pH = 4.0 buffer. Consequently, on the basis on 53 different devices, the threshold voltage V_T was estimated to 0.85 ± 0.23 V, whatever the technological parameters. This value agrees globally with the SiNW-FET one (see §3.1), demonstrating the reproducibility of the whole process and its compatibility with liquid phase analysis.

Figure 11a shows the $I_{DS}(V_{GS})$ semi-logarithmic curves obtained for different SiNW-ISFET configurations (V_{DS} = 1 V). The gate current I_G and the off-state current I_{OFF} were lower than the 50 pA detection limit whatever the tested configuration. Taking in consideration the 100-nanowire devices, the I_{OFF} value of a single nanowire should be lower than 0.5 pA. Consequently, the leakage resistance R_{OFF} of a single nanowire should be higher than 2×10^{12} Ω.

Again, the subthreshold slope did not depend on the different SiNW-ISFET configurations and was evaluated to 0.11 V per current decade for a "150 nm-wide – 200 nm-high" silicon nanowire. Compared to the corresponding SiNW-FET result (0.167 V, see §3.1), this lower value is due to technological considerations. Indeed, according to the Ti/Pt/Ag metallization process, the SiNW-FET devices should be characterized by a partially surrounding metal/insulator/semiconductor gate structure. On the contrary, since silicon oxidation and atomic layer deposition processes are known to be conformal, the SiO_2/Al_2O_3 deposition is performed all around the silicon nanowire. As a matter of fact, the lower subthreshold slope obtained for the SiNW-ISFET devices shows that an all-around surrounding Electrolyte/Insulator/Semiconductor (EIS) gate was effectively achieved. In order to check this assumption, SiNW-ISFET with different silicon nanowire widths were characterized [52]. As shown by Ritzenthaler et al., the subthreshold slope was found to vary greatly with the silicon nanowire width (0.11, 0.125 and 0.18 volt per current decade, i.e. 9, 8 and 5.5 current decades per volt, for values of 150 nm, 200 nm and 250 nm respectively, result not shown), confirming the improvement brought thanks to the all-around EIS gate configuration.

Lastly, since it was not possible to determine precisely the off-state current, the I_{ON}/I_{OFF} ratio was not studied properly. Nevertheless, according to our characterization data and considering only the 150 nm-wide silicon nanowire SiNW-ISFET, it should be higher than 6×10^7 and 1.5×10^7 for the 0.75 μm and 3.75 μm gate lengths respectively.

As observed previously for the SiNW-FET device (see §3.1), the SiNW-ISFET transconductance G_m was shown to increase linearly with the nanowire number (figure 11b). The R_{ON} resistance was evaluated again for a single nanowire transistor, evidencing a 600 kΩ and 62.5 kΩ for a V_{DS} voltage of 0.1 V and 1 V respectively. The G_m linear variations with the drain-source voltage V_{DS} was also studied (result not shown). In agreement with SiNW-FET results, the slope ratio between the two gate lengths (0.75 and 3.75 µm) was estimated around 4.3.

All in all, the electrical characteristics of the single-nanowire $N^+/P/N^+$ SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 µm, nanowire length: ~ 10 µm) were summarized in table 2. Even if the SiNW-ISFET data were impacted by the current detection limit in liquid phase, the comparison with the SiNW-FET one is interesting. Firstly, in all cases, the series resistance (estimated around 0.3 kΩ/µm for a single nanowire) was effectively negligible compared to the SiNW-FET/ISFET R_{ON} resistance. Secondly, compared to the SiNW-FET partially-surrounding MIS gate structure, the SiNW-ISFET all-around surrounding EIS gate structure was responsible for an improvement of the conduction properties: around three current decades per volt (from 6 to 9) were gained and the G_m conductance was doubled. Thirdly, since their electrical characterization was hindered by the current detection limit, the SiNW-ISFET real performances should be better than the experimentally-obtained ones.

3.3. pH detection properties of the $N^+/P/N^+$ SiNW-ISFET devices

Furthermore, working always with the "150 nm-wide – 200 nm-high" nanowire geometry, the pH detection properties of the SiNW-ISFET sensor were studied in consideration of water-based solutions analysis at the submicronic scale (analysed volume: ~ 10 pL). Figure 12a shows the typical $I_{DS}(V_{GS})$ linear/semi-logarithmic curves obtained with a "single nanowire" SiNW-ISFET (length gate: 0.75 µm, V_{DS} = 1 V) for three different buffer solutions (4.0, 7.0 and 10.0). In the light

of the different SiNW-ISFET configurations (single nanowire, 20 nanowires and 100 nanowires), the detection sensitivity was estimated to 56 ± 4 mV/pH, whatever the technological parameters (53 different devices were tested). It should finally be noted that the subthreshold drain-source current I_{DS} was found to decrease greatly with the pH increase (result not shown). In the studied case, for a 1.25 V gate-source voltage V_{GS}, this value is multiplied by approximately 250 between pH = 4 and pH = 10, for an amperometric detection sensitivity around 0.4 current decade per pH.

Standard potentiometric analyses were finally performed to check the pH measurement hysteresis between pH = 3 and pH = 9 (figure 12b), as well as the selectivity to K^+ and Na^+ ions in the [1-3] pX concentration range (result not shown). In this frame, a "100 nanowire" configuration was preferred in order to increase the measured current (length gate: 0.75 µm, V_{DS} = 1 V). Thus, no hysteresis phenomena and no pK or pNa interference were evidenced for the SiO_2/Al_2O_3 SiNW-ISFET devices, demonstrating the performances of amorphous alumina as a pH-sensitive layer.

4. Conclusion

Silicon-nanowire-based field effect transistors (SiNW-FET) as well as silicon-nanowire-based ion-sensitive field effect transistors (SiNW-ISFET) were fabricated on SOI substrate while focusing on the integration of a suspended $N^+/P/N^+$ double-junction structure (gate length: ~ 0.75 µm and ~ 3.75 µm). First, a double reactive ion etching process was optimized in order to fabricate single silicon nanowire (length: ~ 10 µm) and parallel networks of such nanowires. Second, a conformal process based on a silicon thermal oxidation followed by an alumina atomic layer deposition was developed in order to achieve an SiO_2/Al_2O_3 all-around surrounding gate structure and to reach low silicon nanowire sections (width: ~ 150 nm, height: ~ 200 nm). Lastly, a SU8-based wafer-level packaging process was developed in order to adapt the SiNW-ISFET to the analysis of

microvolumes around a dozen of picolitres. Hence, even if current detection limit inherent to nanowire-based devices had to be considered, excellent electrical characteristics were obtained:

- SiNW-FET: $R_{OFF} \approx 3 \times 10^{14}\ \Omega$, subthreshold slope $\approx$ 0.167 V/decade, $(I_{ON}/I_{OFF})_{max} \approx 4 \times 10^{9}$,

- SiNW-ISFET: $R_{OFF} > 2 \times 10^{12}\ \Omega$, subthreshold slope $\approx$ 0.11 V/decade, $(I_{ON}/I_{OFF})_{max} > 6 \times 10^{7}$.

Finally, the pH analysis at the submicronic scale (analysed volumes: ~ 10 pL) was demonstrated. In the standard potentiometric measurement configuration, SiNW-ISFET devices were characterized by quasi-Nernstian pH detection properties (56 ± 4 mV/pH), whatever the technological parameters. Furthermore, considering the subthreshold operation mode, the amperometric detection sensitivity was estimated to 0.4 current decade per pH, enabling accurate pH measurement in liquid phase.

Works will be continued while applying the proposed SiNW-ISFET technology to chemical, biochemical and biological analysis in liquid phase, focusing on the recording of neuronal bio-electro-chemical activities. Moreover, taking into consideration technological developments, the double reactive ion etching process will be further investigated. According to first preliminary technological realizations, it should enable the fabrication of triangular silicon nanowires on standard silicon substrate and the corresponding technological process should be further designed, microfabricated and optimized.

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Tables and figures captions

Table 1: typical width of studied nanostructures according to photolithographic parameters (focus depth is chosen to obtain 90° vertical walls for the photoresist nanopatterns)

Table 2: electrical characteristics of single-nanowire SiNW-FET and SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 μm, nanowire length: ~ 10 μm)

Figure 1: fabrication of AZ ECI 3012 photoresist nanopatterns (thickness: 1.2 μm)
a) variations with the UV exposure dose of the focus depth to obtain vertical side walls and associated final photoresist nanopattern width
b) SEM picture (tilt: 52°) of 1.2 μm-thick, 270 nm-wide photoresist patterns

Figure 2: SEM pictures (tilt: 52°) of 240 nm-wide silicon nanofins after the $SF_6/C_4F_8/O_2$ RIE process

Figure 3: SEM pictures (tilt: 52°) of test devices for the definition of 200 nm-wide silicon nanofins
a) after the first partial etching of the thin silicon upper layer outlining the silicon nanofins
b) after the second and final etching of the thin silicon upper layer

Figure 4: Schematics of the suspended $N^+/P/N^+$ double-junction SiNW-ISFET adapted to liquid phase analysis by wafer-level packaging
a) before the SU-8 film integration, b) with the integrated SU-8-based microfluidic channel

Figure 5: SEM sectional picture of a silicon nanowire (width: 170 nm, height: 220 nm) obtained by reactive ion etching (RIE) and thermal oxidation of a SOI substrate silicon upper layer

Figure 6: SEM picture (tilt: 52°) of suspended $N^+/P/N^+$ silicon nanowires (gate length: ~ 0.75 μm) integrated on a SOI substrate

Figure 7: microfabrication of SiNW-FET and SiNW-ISFET devices on a 6-inch silicon wafer (chip size: 7 × 8 mm^2, device number per chip: 16)

Figure 8: integration of SU8-based microfluidic structures on SiNW-ISFET chips using photolithographic-based wafer-level packaging

Figure 9: SEM picture (tilt: 52°) of suspended $N^+/P/N^+$ SiNW-ISFET
integrated into SU8 microfluidic channels for the liquid phase analysis at the submicronic scale
(analysis volume around $5 \times 5 \times 500\ \mu m^3$)

Figure 10: Electrical characterization of "150 nm-wide – 200 nm-high" SiNW-FET devices
a) $I_D(V_{DS})$ curves obtained for a single nanowire (gate length: 0.75 µm)
b) $I_D(V_{GS})$ semi-logarithmic curves obtained for different nanowire configurations (V_{DS} = 0.1 V)
c) $I_D(V_{GS})$ curves obtained for different nanowire configurations (V_{DS} = 0.1 V)
d) transconductance variations with the V_{DS} voltage for 100-nanowire configurations
(gate lengths: 0.75 µm and 3.75 µm)

Figure 11: Electrical characterization of "150 nm-wide – 200 nm high" SiNW-ISFET devices
a) $I_D(V_{GS})$ semi-logarithmic curves obtained for different nanowire configurations (V_{DS} = 1 V, pH = 4)
b) $I_D(V_{GS})$ linear curves obtained for different nanowire numbers ($L_G \approx 0.75$ µm, V_{DS} = 1 V, pH = 4)

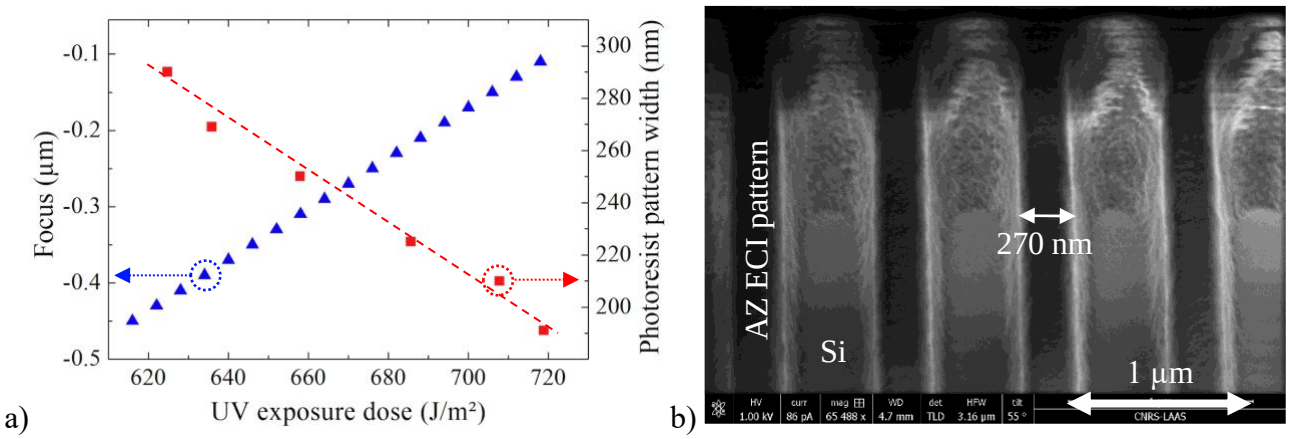
Figure 12: pH detection properties of 150 nm-wide – 200 nm-high" SiNW-ISFET devices
a) $I_D(V_{GS})$ curves obtained for a single nanowire (gate length: $L_G \approx 0.75$ µm)
for different buffer solutions (V_{DS} = 1 V, pH = 4, 7 and 10)
b) $I_D(V_{GS})$ curves obtained for a 100-nanowire configuration (gate length: $L_G \approx 0.75$ µm)
for buffer solutions going down and back from pH = 9 and pH = 3 (V_{DS} = 1 V)

photolithographic parameters		typical widths		
UV exposure dose	focus depth	mask nanopattern	photoresist nanopattern	silicon nanofin
615 J/m^2	- 0.45 mm	300 nm	290 nm	290 nm
670 J/m^2	- 0.27 mm	300 nm	240 nm	240 nm
720 J/m^2	- 0.11 mm	300 nm	190 nm	190 nm

Table 1: typical width of studied nanostructures according to photolithographic parameters (focus depth is chosen to obtain 90° vertical walls for the photoresist nanopatterns)

	single nanowire SiNW-FET	single nanowire SiNW-ISFET
threshold voltage V_T	0.6 ± 0.2 V	0.85 ± 0.23 V at pH = 4
serie resistance R_S	3 kΩ	3 kΩ
gate resistance R_G	10^{17} Ω	> 7×10^{12} Ω
leakage resistance R_{OFF}	3×10^{14} Ω	> 2×10^{12} Ω
subthreshold slope	0.167 V per current decade	0.11 V per current decade
resistance R_{ON} at V_{DS} = 1 V	125 kΩ	62.5 kΩ
$(I_{ON}/I_{OFF})_{max}$	4×10^9	> 6×10^7

Table 2: electrical characteristics of single-nanowire SiNW-FET and SiNW-ISFET devices (width: ~ 150 nm, height: ~ 200 nm, gate length: ~ 0.75 μm, nanowire length: ~ 10 μm)



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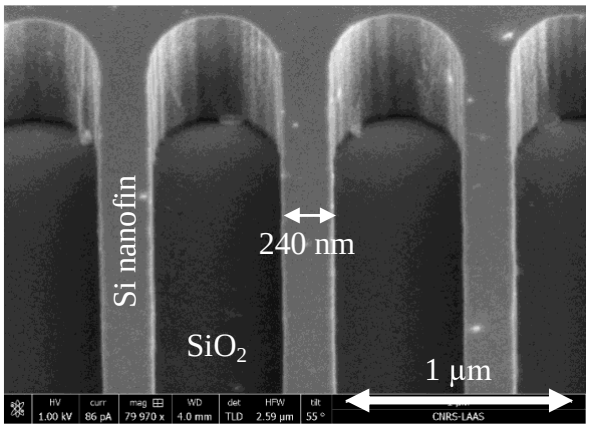

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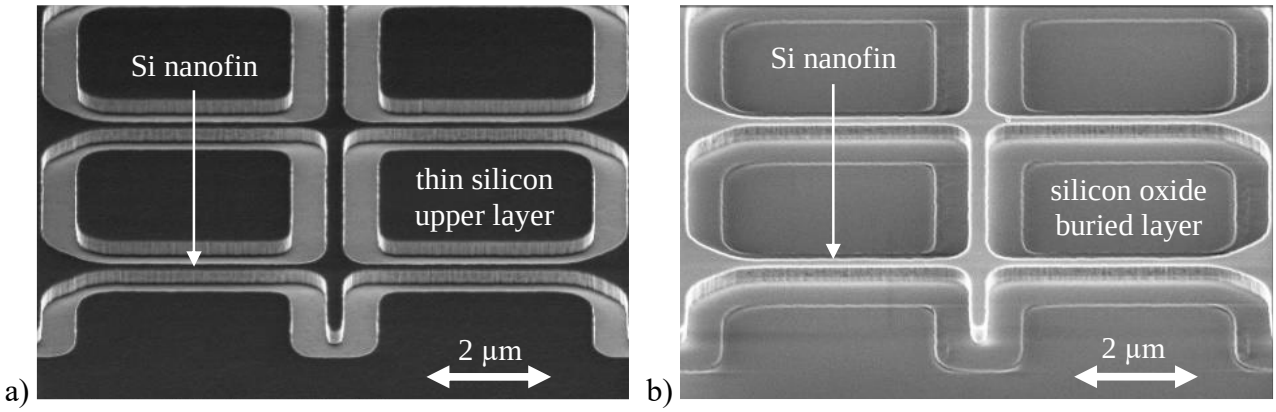

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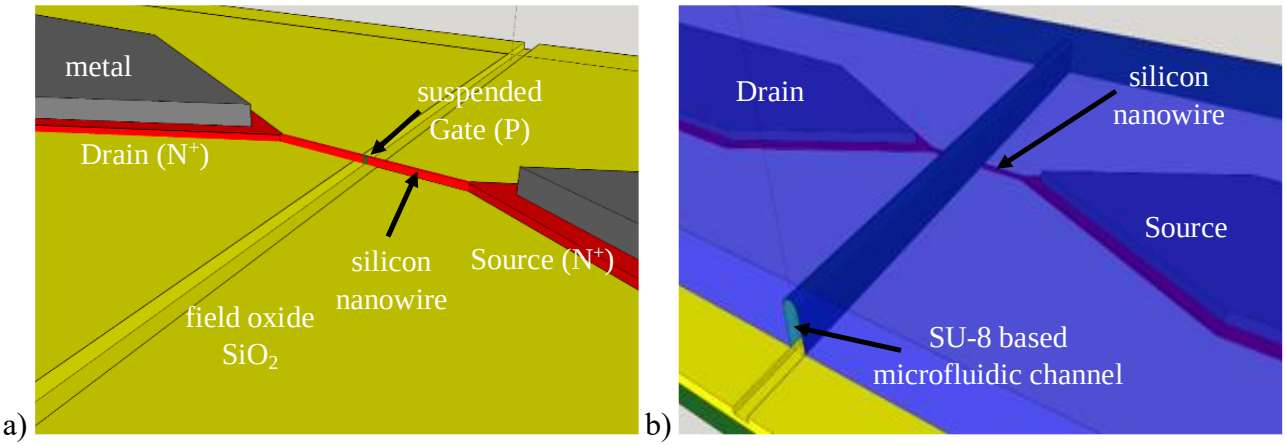

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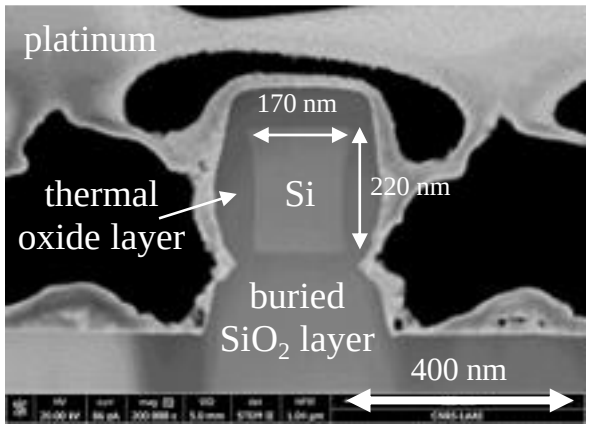

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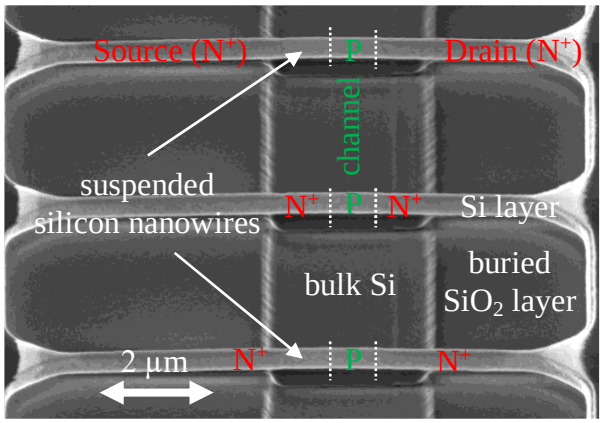
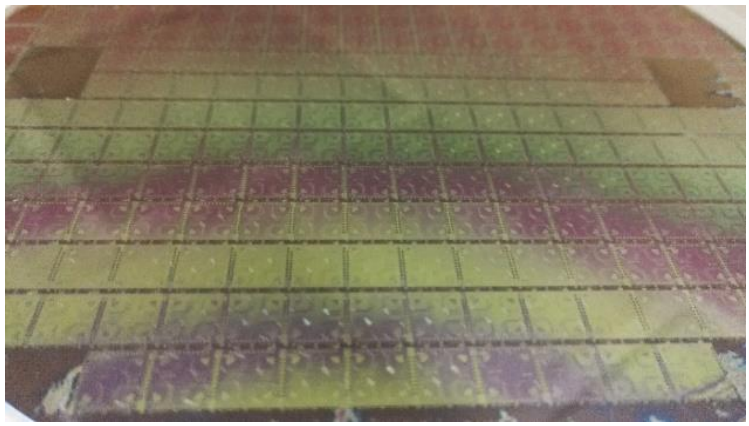


Figure 6: SEM picture (tilt: 52°) of suspended $N^+/P/N^+$ silicon nanowires (gate length: ~ 0.75 µm) integrated on a SOI substrate



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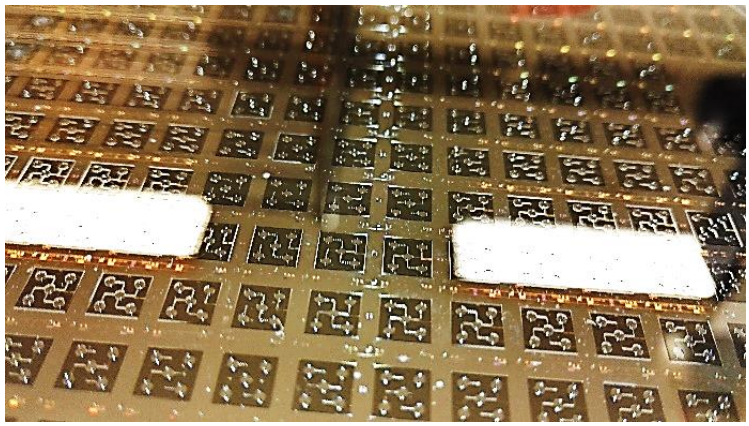
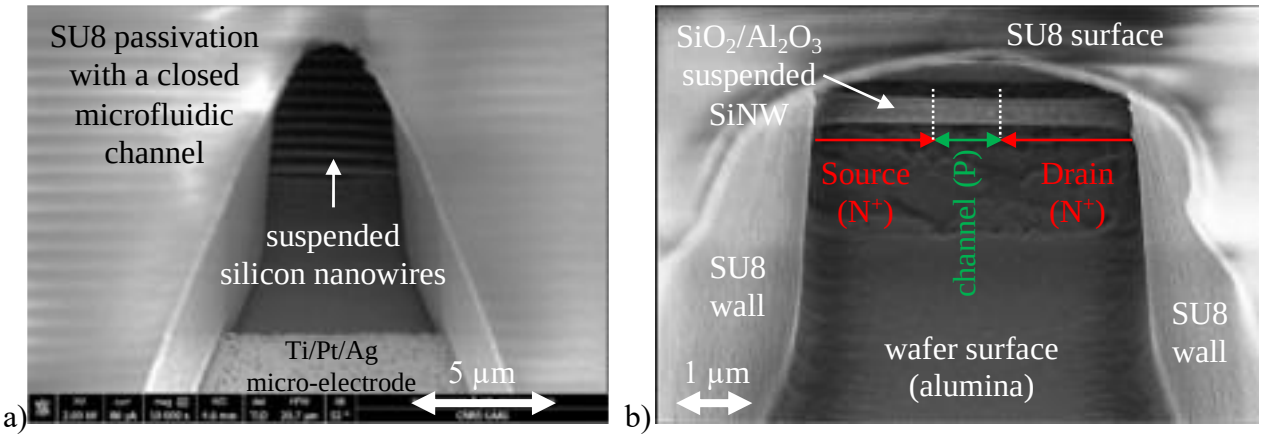


Figure 8: integration of SU8-based microfluidic structures on SiNW-ISFET chips using photolithographic-based wafer-level packaging



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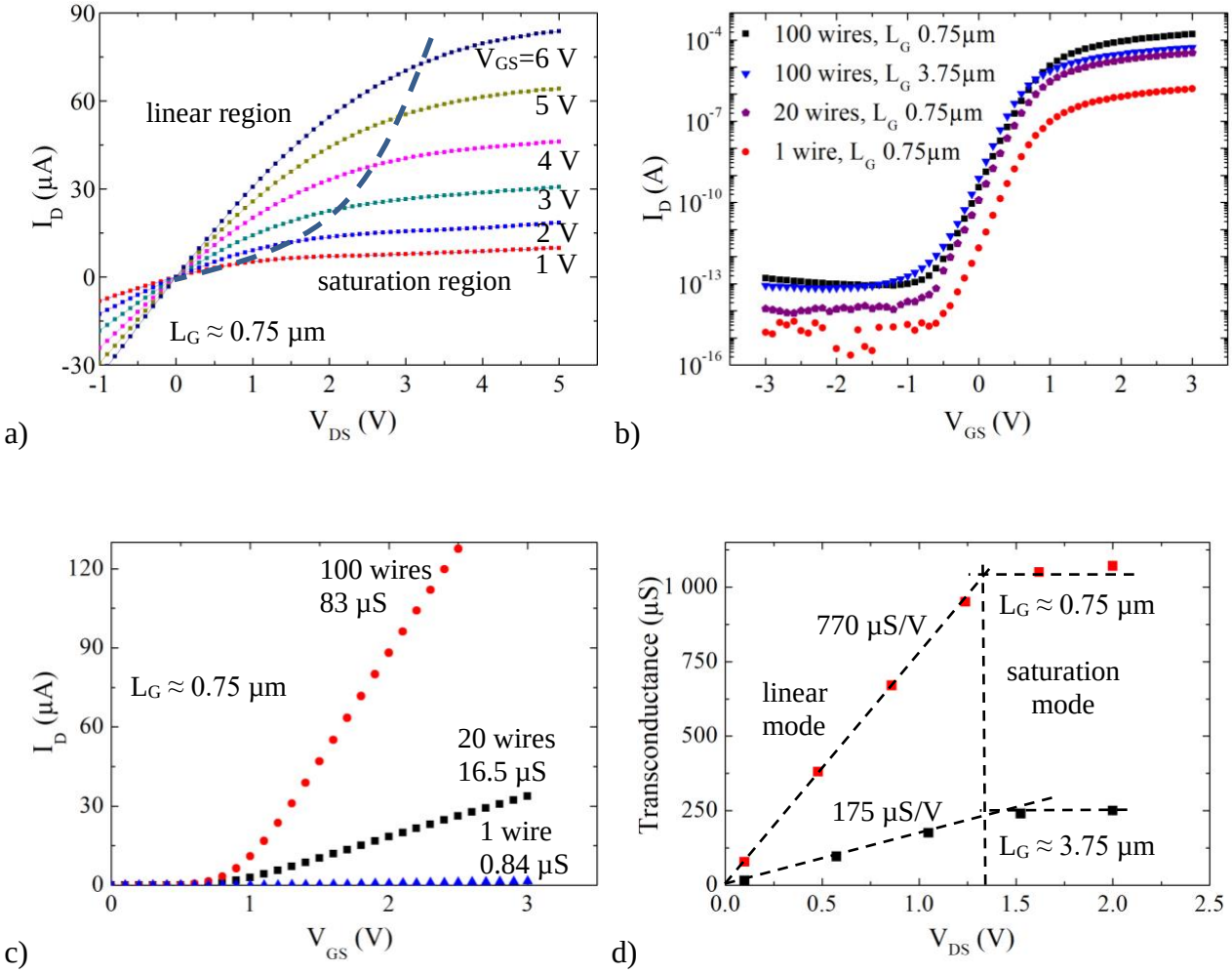

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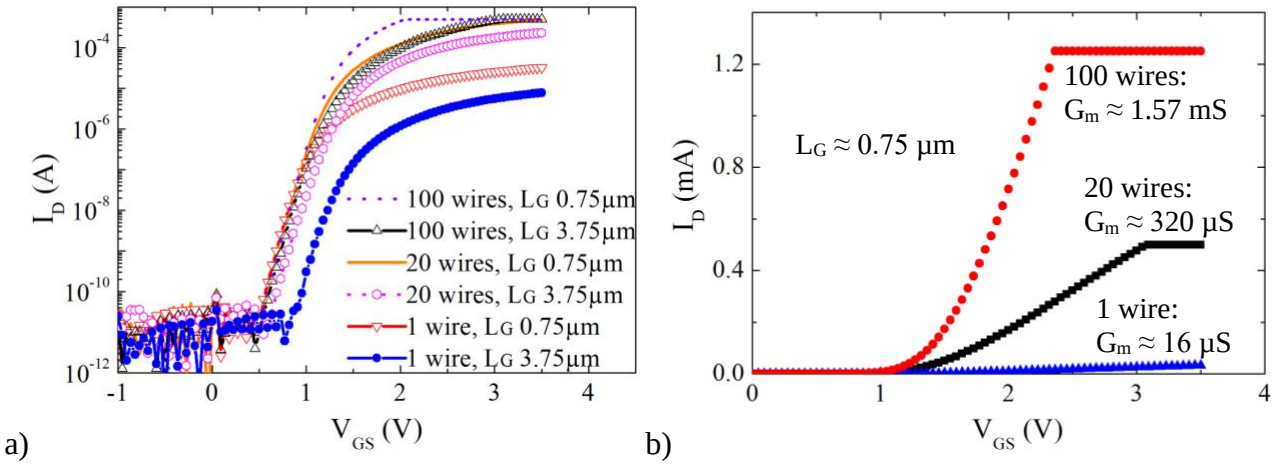

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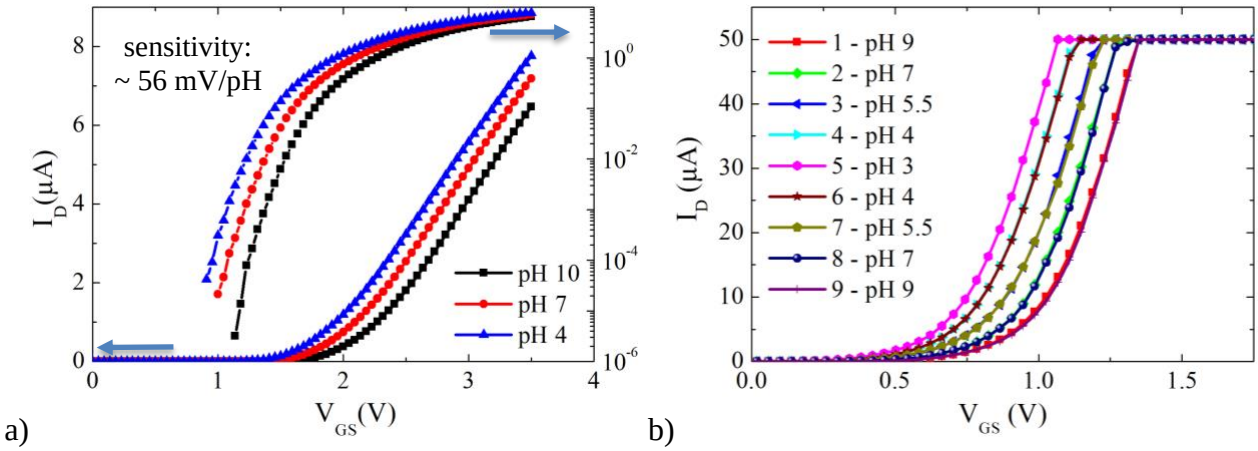

a) b)

Figure 12: pH detection properties of 150 nm-wide – 200 nm-high" SiNW-ISFET devices
a) $I_D(V_{GS})$ curves obtained for a single nanowire (gate length: $L_G \approx 0.75$ µm) for different buffer solutions (V_{DS} = 1 V, pH = 4, 7 and 10)
b) $I_D(V_{GS})$ curves obtained for a 100-nanowire configuration (gate length: $L_G \approx 0.75$ µm) for buffer solutions going down and back from pH = 9 and pH = 3 (V_{DS} = 1 V)