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Abstract

We present a fabrication process based on selective ion implantation to monolithically integrate several porous silicon membranes with different morphologies in the same planar fluidic chip through a single anodization step. By manipulating the dopant concentration of specific zones of a silicon on insulator wafer, the porous silicon elements formed through electrochemical anodization present different characteristics in terms of pore size and porosity. Using this technique, we are able to fabricate both lateral porous silicon membranes and standard porous silicon membranes with vertical pores that can be used in flow-through and flow-over configurations. Achieved mean pore sizes and porosities for the various membranes integrated in the same chip range from 25 nm to 50 nm, and 65% to 90%, respectively. Because porous silicon membranes have been used for biosensing and for sample preparation in microfluidics devices, this method is foreseen to enable the use of porous silicon membranes to achieve all the functions involved in the analytical process on a single chip.

Keywords: Porous silicon; Membrane; Lab-on-a-chip; Sensor; Sample preparation

1. Introduction

Advances in microfluidics have enabled the development of low-cost lab-on-a-chip (LOC) devices designed for point-of-care (POC) diagnostics [1]. The need for POC technology has recently been highlighted by the COVID-19 pandemic, as on site testing has been essential to monitor and control the spread of the virus [2]. Biological analysis, which are mainly conducted in central laboratories, consist in detecting a biomarker in a sample to provide information of the patient's medical state. Due to the complexity of biological samples and the restrictions imposed by the analytical technique used, biological samples undergo sample preparation, that most often rely on centrifugation, prior to analysis. Numerous strategies have been explored to miniaturize and implement sample preparation functions on chip [3]. However, the co-integration of miniaturized solutions for sample preparation

and biosensing in a single device can be challenging and is most likely to be carried out in a hybrid approach, increasing the LOC complexity and possibly its final cost. A change of paradigm consists in using a generic and single technology to perform sample preparation and biosensing in a monolithically integrated LOC, as demonstrated by the platform developed by Patolsky's team that uses silicon nanowires to do it all: a dense forest of silicon nanowires at the chip input for filtration, molecular separation and pre-concentration, and nanowire transistors downstream for the detection of protein biomarkers directly in a blood sample [4].

Porous silicon is a nanostructured material formed by a crystalline silicon skeleton and a network of voids that can conveniently be fabricated through silicon anodization, a technique suitable for large scale production and monolithic integration. Porous silicon displays unique properties such as photoluminescence, high thermal and electrical insulation, and biocompatibility that are of interest for various applications, ranging from energy conversion to drug delivery [5]. Porous silicon has extensively been used for biosensing using optical transduction, often relying on reflectance-based interferometry [6]. This transduction method has been applied to the detection of enzyme activity [7], proteins [8], immunoglobulins [9], DNA [10], bacteria [11], and bacteria lysate [12]. Porous silicon membranes have also shown great potential for performing various tasks in microfluidic devices, some of which are of interest for sample preparation [13]. Size- and charge-based sample filtration and on-chip separation have been extensively presented in the literature [14], [15], [16], [17], [18]. Additionally, the ion-selectivity property of porous silicon [19] could be used to perform sample concentration via ion concentration polarization, an electrokinetic phenomenon that relies on the selective charge transport through an ion selective fluidic junction (e.g. nafion or porous silicate membranes [20], [21], and nanochannel arrays [22]). Hence, porous silicon membranes can be used to perform various functions involved in sample preparation and biosensing. However, implementing the entire analytical process using porous silicon in a single LOC requires the integration of multiple porous membranes with tailored characteristics suited to perform each function. Indeed, membranes with relatively large pores and surface area are needed to minimize the fluidic resistance of flow-through separation membranes in order to process enough sample volume in a given time. Also, porous membranes used for biosensing have to accommodate a biochemical functionalization layer and allow target molecules to easily permeate. On the other hand, smaller pores that favor surface over bulk conductivity, are required for preconcentration efficiency. Additionally, flow-through and flow-over membrane configurations provide their own advantages when performing a dedicated function. For instance, while flow-through membranes has been demonstrated to reduce the response time of porous silicon biosensors [23], flow-over membranes are associated with larger flow rates. Finally, the monolithic integration of porous silicon alleviates the challenges raised by the hybrid integration of analytical functions.

We have recently proposed a strategy for integrating flow-through porous silicon membranes within planar microfluidics in a monolithic fashion. Porous silicon membranes are most commonly fabricated via electrochemical anodization by injecting the anodization current through the backside of a silicon wafer, which results in pores perpendicular to the surface of the wafer [24]. In this configuration, flow-through membranes are created by backside etching the silicon wafer and are integrated into LOC by sandwiching them between encapsulating layers that bear microfluidic channels. This leads to three-dimensional (3D) microfluidics that can be prone to leaks and can turn into complex networks when integrating multiple membranes. Conversely, our strategy relies on the fabrication of porous silicon membranes with pores running parallel to the surface of the wafer for their integration in 2D fluidics. Since pores propagate along current flow during anodization, lateral pores are fabricated by injecting the current through a front side electrode patterned on a step bridging planar microchannels and electrically insulating the silicon step so that the current injected on the side of the step flows parallel

to the surface of the wafer [25]. We have implemented this strategy via two fabrication processes, one relying on the use of silicon on insulator (SOI) substrates that uses the box oxide as the bottom insulating layer [26], the other one relying on local implantation to modify the conductivity of the step to anodize [27]. The on-chip size- and charge-based filtering capability of these lateral porous silicon membranes was demonstrated [28], [29], along with flow-through sensing by interferometric transduction [30], [31]. In this paper, we address the issue of integrating multiple porous silicon membranes in flow-through and flow-over configurations with tunable characteristics (pore size and porosity) on the same chip by developing a dedicated monolithic fabrication process. This process, which is based on local ion implantation to create regions of different doping levels on a SOI wafer, leads to the integration of two types of flow-through lateral porous silicon membranes exhibiting a two-fold difference in average pore size (25 nm and 50 nm) along with a flow-over porous silicon membrane, all fabricated in a single anodization step.

2. Results and Discussion

The characteristics of porous silicon fabricated by electrochemical anodization are dictated by the intrinsic properties of the substrate and the anodization conditions. The dopant type and concentration and the crystallographic orientation govern the electrochemical etch rate of silicon and in turns, the properties of porous silicon in terms of pore size and porosity [32], [33], [34] : for instance, an increase in pore size is expected with higher doping levels for p-type silicon [35]. The same goes with the current density during anodization (rate of holes available for reaction) and the composition of the electrolyte (HF concentration and solvent/surfactant used), that all dictate the dissolution rate of silicon [36], [37], [38]. Thus, one can use these parameters to tune the characteristics of porous membranes and two strategies can be explored to integrate of multiple membranes with different morphologies on a single chip. Because the electrochemical dissolution of silicon is a collective process, where the silicon wafer is immersed in a given electrolyte and all exposed silicon on the wafer undergoes anodization, fabrication of porous membranes exhibiting different mean pore sizes and porosities through a change in electrolyte and current density can only be achieved by sequentially fabricating the various membranes. On the other hand, the intrinsic substrate properties can be locally modified so that exposed silicon with different dopant types and concentrations will give rise to porous silicon exhibiting different morphologies upon anodization. These two strategies for fabricating multiple membranes with different properties are summarized in Figure 1.

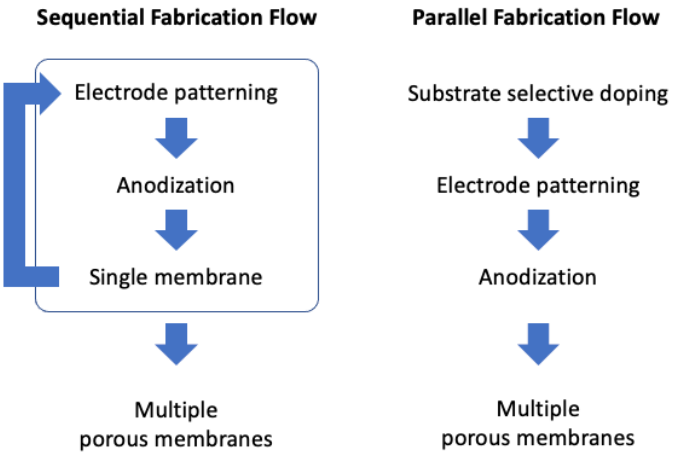

Figure 1. Schematic presentation of the two strategies for monolithically integrating multiple porous silicon membranes with different characteristics on a same fluidic chip.

Stemming from our previous work on the fabrication of lateral porous silicon membranes on a SOI substrate, the implementation of the sequential strategy consists in fabricating a first set of membranes in a first anodization run with a dedicated set of parameters (current density, electrolyte composition) leading to the desired porous silicon characteristics, then fabricating another set of membranes in a second anodization step, a process that can be repeated (Fig. S1). This strategy requires adequate protection of previously fabricated porous silicon. A straightforward answer to this technological constraint is to take advantage of the metal layer used as the working electrode. We have previously used a sputtered layer of Cr/Au that withstands HF to protect previously fabricated porous membranes during subsequent anodization. However, chromium thin films are known to exhibit high intrinsic stress, and because porous silicon membranes are mechanically fragile, this strategy led to delamination and destruction of the porous membranes upon encapsulation (see Fig. S2). Further developments or alternative solutions relying on, e.g., the use of process-compatible polymer layers, such as fluoropolymer [39], [40], are needed to demonstrate the feasibility of this approach.

Alternatively, we have developed a process that relies on the local modification of silicon conductivity to fabricate multiple membranes with different morphologies on a single chip using a single anodization step. This parallel fabrication strategy, which is a combination of the two previously developed processes for lateral porous silicon membrane fabrication [26], [27], offers advantages over the sequential process in terms of process time, cost and complexity. This process, which is detailed in Figure 2, was implemented on a 16x16 mm^2 chip integrating two types of flow-through lateral porous silicon membranes bridging planar microchannels and a flow-over membrane situated at the bottom of the fluidic microchannel (see chip design in Figure S3).

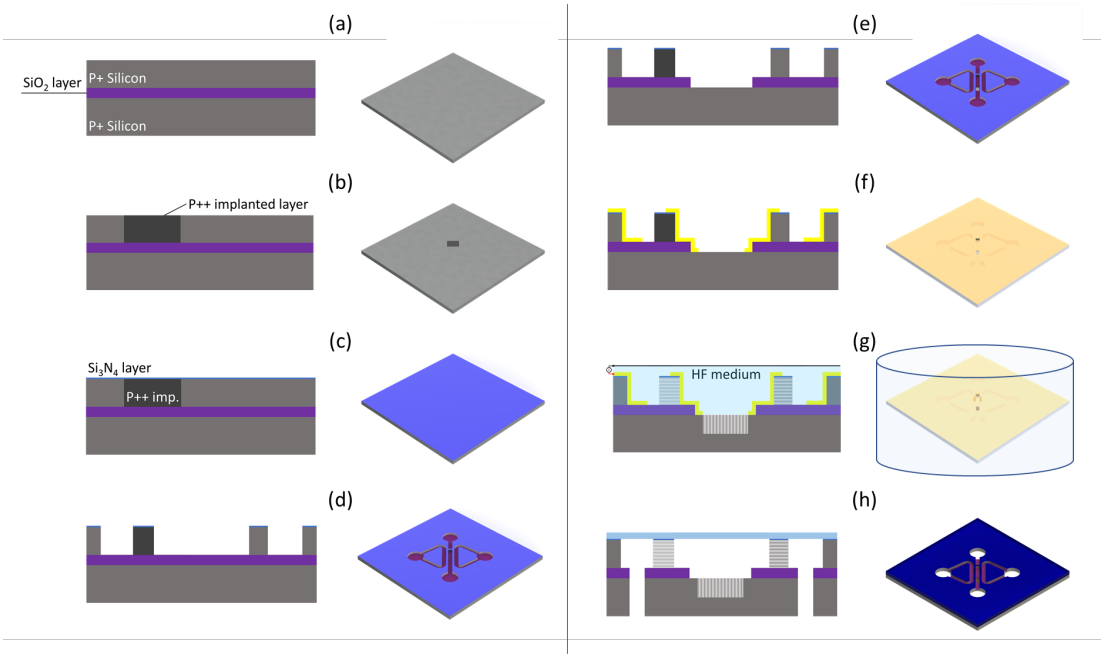

Figure 2. Process flow for the fabrication of multiple porous membranes with distinct characteristics and their integration into planar microfluidics in a single anodization step. (a) Highly doped P-type SOI wafer as the starting substrate; (b) Selective boron implantation to locally increase the dopant concentration; (c) LPCVD deposition of a silicon nitride layer; (d) Microchannel fabrication by reactive ion etching; (e) Box oxide opening by reactive ion etching; (f) Patterning of the metal layer used as the working electrode during silicon anodization – the metal layer is opened where porous silicon is to be formed; (g) Electrochemical anodization in an HF electrolytic bath; (h) Fluidic inlet/outlet holes fabricated by sandblasting and fluidic channel capped with a glass chip through anodic bonding.

The fabrication process relies on the use of a <100> P-type SOI wafer (d= 100 mm, t= 2/1/450 µm, ρ= 15 mΩ.cm - device and handle layers). The process starts with the thermal growth of a 40 nm oxide layer used to prevent surface damage and channeling effects during subsequent ion implantation (Fig. 2a). Local implantation is carried out by protecting selective areas of the wafer using a 1.2 µm thick ECI photoresist layer, patterned by photolithography. Boron implantation (ion energy 150 keV, dose $1x10^{16}$ cm^{-2}) and, after photoresist removal, thermal annealing (8 h at 1150 °C) are performed with the aim of increasing the dopant concentration of selected regions of the wafer from the initial concentration of $6x10^{18}$ cm^{-3} to more than $1x10^{19}$ cm^{-3} (Fig. 2b), a value known to cause a relevant impact in the pores morphology [35]. The dopant profile along the device layer thickness obtained using secondary ion mass spectroscopy (SIMS) shows a uniform dopant concentration ranging from $5.8x10^{19}$ cm^{-3} at the surface of the wafer surface to $4.9x10^{19}$ cm^{-3} in the vicinity of the active layer/dioxide interface (Figure S4, where the peak of dopant concentration observed at the Si/SiO_2 interface is due to the tendency of boron to preferentially migrate to the interface [41]). After removing the oxide layer in buffered HF, an 80 nm thick silicon nitride layer is deposited by LPCVD (Fig. 2c). This top nitride layer is used to insulate the surface of the wafer from the electrolyte during anodization. Along with the box oxide layer, these two insulating layers force the current to flow parallel to the surface of the wafer during the fabrication of the lateral porous silicon membranes by anodization. The microchannels are fabricated by reactive ion etching (RIE) the silicon nitride and silicon device layers using a 2.6 µm thick ECI photoresist layer (Fig. 2d). Opening the buried oxide layer where flow-over porous silicon

membranes are to be fabricated, is then achieved by RIE using another 2.6 µm thick ECI photoresist mask (Fig. 2e). A 100 nm/500 nm thick Cr/Au layer, used as the working electrode during anodization, is deposited by sputtering to ensure the conformal coating of the sides of the microchannels. A photoresist layer (AZ4562 5 µm) is patterned where lateral porous silicon and vertical porous silicon membranes are to be formed (on the microchannel walls and at the bottom of the microchannels, respectively). The metal layer is removed by wet etching and the Au layer is thickened by gold plating to 1 µm (Fig. 2f). The wafer is then diced into chips to carry out the anodization process at the chip level. Anodization is conducted by loading the chip in a home-made anodization cell and current is provided by a Keithley 2450 sourcemeter (Fig. 2g). It is important to note that during the etching of the nitride layer, the device layer and the box oxide, 2 mm diameter circular areas are also etched to expose the silicon handle layer (see Fig. S3). These large areas are used to increase the overall surface area of silicon exposed to the electrolyte during anodization (~0.06 cm^2 vs. ~10^{-6} cm^2 for a single porous membrane) for a better control of the current density where relatively large currents (in the order of 10 mA) result desired current densities (100-400 mA/cm^2). After anodization, the metal electrode is removed by wet etching. Finally, chip packaging is done by opening inlet/outlet holes for fluidic connections through sandblasting (using a 40 µm thick protective dry film laminated using a SA 3024 OC from Dynachem at 64°C, 2 MPa) and by capping the microchannels with a 500 µm thick borofloat 33 (Schott) glass chip through anodic bonding (370°C, 5x10^{-5} mbar, 600 V for 10 min) (Fig. 2h).

Figure 3 shows SEM images of various porous membranes fabricated on a single of chip using an anodization current density of 225 mA/cm^2 for 60 s and a 1:1 HF:ethanol electrolyte. The mean pore size (d_{mean}) and the porosity (P) of the porous silicon layers were respectively estimated using the SEM cross-section images analyzed with ImageJ and using the spectroscopic liquid infiltration method (SLIM) [33], which is based on the analysis of the Fabry-Perot interference fringes obtained with a VERTEX 70 FTIR. The mean pore size of the 2 µm deep and 10 µm thick non-implanted and implanted lateral porous silicon membranes that bridge adjacent microchannels are ~25 nm and ~50 nm, respectively, resulting in a two-fold increase due to the local ion implantation process. The porosities are respectively ~80% and ~90%. Additionally, the 8.1 µm thick vertical porous silicon layer located at the bottom of the main microchannel and used in flow-over configuration exhibits a ~35 nm average pore size and a ~65% porosity. Changing the solvent for anodization to 1:1 HF:1-butanol (and current density of 200 mA/cm^2 applied for 60 s) analogously led to the fabrication of porous membranes with different characteristics (Fig. S5). Even if the increase in mean pore size was in this case only 75%, this result proves the feasibility of our approach of combining local implantation with a single anodization step to fabricate porous silicon membranes of various configurations and properties on a single chip.

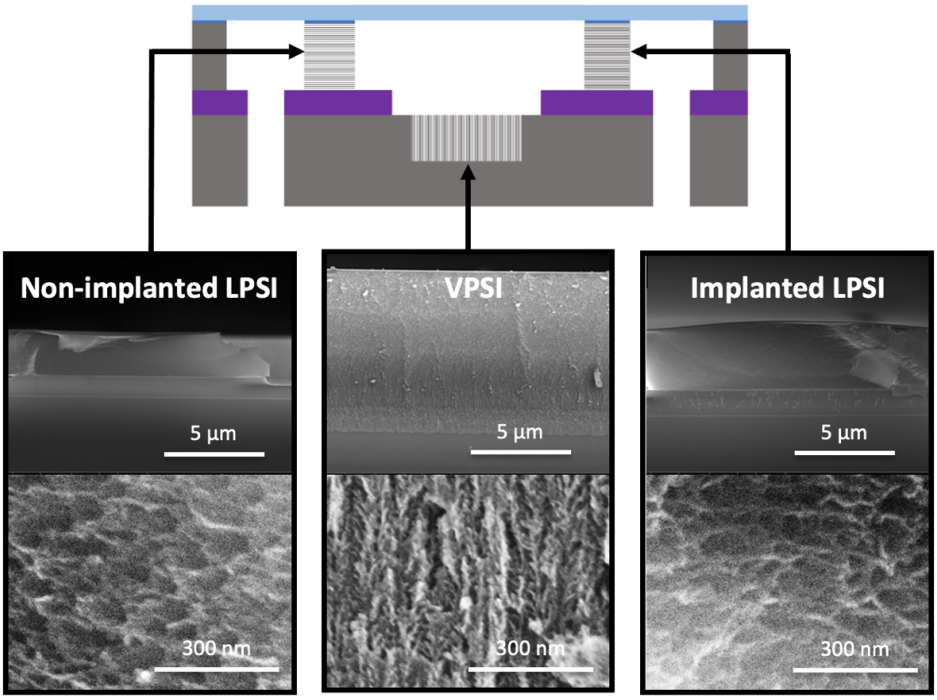

Figure 3. SEM images of the cross-section of different porous silicon elements fabricated with a single anodization step (1:1 HF:ethanol, 225 mA/cm^2, 60 s) on a 2 µm SOI chip. Left: non-implanted lateral porous silicon membrane with d_{mean} ~25 nm and P ~80%; Center: 8.1 µm deep vertical porous silicon layer with d_{mean} ~35 nm and P ~65%; Right: implanted lateral porous silicon membrane with d_{mean} ~50 nm and P ~90%.

Optical pictures of fabricated fluidic chips with integrated porous silicon membranes of different characteristics are shown in Figure 4. The chips include three parallel microchannels and lateral porous silicon membranes bridge the central microchannel to the side microchannels. The central microchannel integrates either a lateral or a vertical porous silicon membrane. The microchannels were filled with a solution of 10 µM of fluorescein (hydrodynamic radius of ~1 nm, Sigma Aldrich) in PBS 1X buffer (~150 mM, pH 7.4, Sigma Aldrich), after exposing the chip to oxygen plasma to increase the fluidic channels' wettability. Fluidic flow was induced in the microchannels by applying ~0.2 bar at the chips' fluidic inlet using a MFCS-8C pressure controller (Fluigent). The chip was observed using a IX70 Olympus inverted epifluorescence microscope equipped with an EMCCD camera (Andor), a light source (Lumencore), and dedicated optical filters. We observed the complete filling of the porous membranes with the fluorescent solution (Fig. 4d, where the micrometer size air bubbles seen in the microchannels should disappear upon proper degassing of the solution before injection). Last, the fabricated porous membranes were characterized by optical interferometry using a VERTEX 70 FTIR (Bruker Optics), equipped with a tungsten light source, a quartz beam splitter and a Si-diode detector (SiD 510), able to cover the spectral range between 500 nm and 1100 nm. The spectrometer was connected to a HYPERION microscope equipped with a 36x objective (with incident angle ~8°) and an adjustable rectangular observation window (maximum size of 277x277 µm^2). The spectroscopy software OPUS (Bruker Optics) was used to control the equipment and acquire the data. Figure 4e

presents the interferometric spectra of a non-implanted lateral porous silicon and vertical porous silicon layer fabricated using 200 mA/cm^2, 60 s of anodization time and a 1:1 HF:1-butanol electrolyte. Because the top view area of the lateral porous silicon membranes is 100x10 µm^2, spectra were recorded using a 90x10 µm^2 window size. The interference patterns exhibit clear reflectance peaks that can thus be used for interferometric-based sensing.

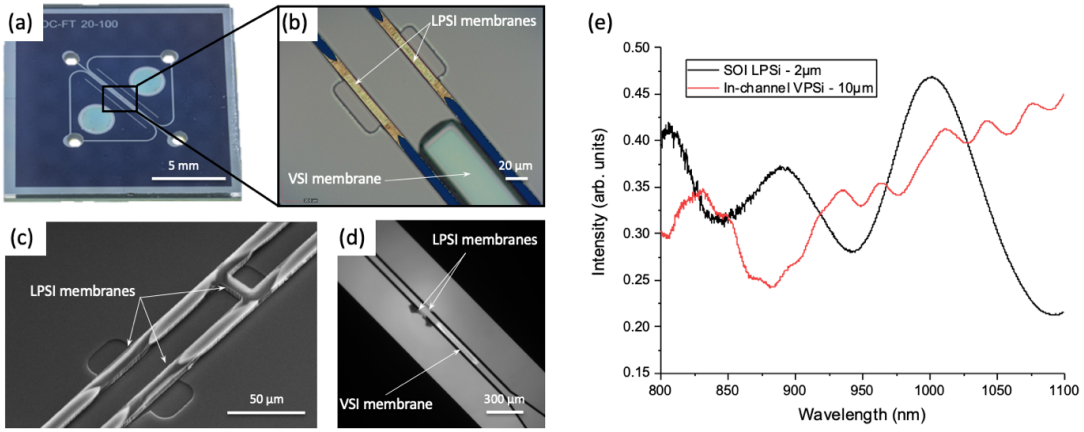

Figure 4. (a) Optical photograph of a fabricated microfluidic chip integrating various porous silicon membranes fabricated using a single anodization step; (b) Optical picture showing a close-up view of the microfabricated chip with lateral porous silicon membranes bridging two side microchannels and a vertical porous silicon element integrated at the bottom of a central microchannel. (c) SEM image of fabricated microchannels and multiple lateral porous silicon membranes. (d) Fluorescence microscope images of the microchannels after loading a solution of 10 µM fluorescein in PBS 1X buffer into the microfluidic chip. (e) Reflectance spectra of the lateral and vertical porous silicon membranes.

3. Conclusions

A strategy to monolithically integrate multiple porous silicon membranes displaying various and controllable morphologies on a single chip is presented here. This strategy relies on ion implantation to locally modify the dopant concentration of a SOI device layer and a single anodization step to fabricate membranes of different configurations and properties. As a proof-of-concept, this process was used to fabricate microfluidic chips integrating 10 µm thick lateral porous silicon membranes bridging 2 µm deep microchannels and vertical porous silicon membranes situated at the bottom of the fluidic channels. Notably, a twofold increase in mean pore size, from ~25 nm to ~50 nm, was achieved between non-implanted and implanted lateral porous silicon membranes onto a single chip. We believe that this work opens the door to the integration of porous silicon membranes useful for performing various tasks involved in biological analysis on a single chip, from sample preparation through filtration and sample concentration to on-chip biosensing via optical interferometry, that require membranes with tailored and distinct characteristics.

Acknowledgments

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