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Bipolar ac (Bipac) switch with buried layer for specific ac mains applications

Hiba Rizk, Abdelhakim Bourennane, Marie Breil, Jean-Pierre Laur

A new vertical bipolar bidirectional switch (Bipac) with a buried layer is proposed for specific ac mains applications (230 V – 50 Hz). It is mainly dedicated for the low load current ones (0.5 A_{rms}) and must support a voltage of 750 V in the blocking state. Moreover, the Si-chip area must not exceed 10 mm^2. The study of the new proposed Bipac structure is carried out using 2-D Sentaurus physical simulation. The operating principles are first validated, and then the physical and geometrical parameters of the buried layer are determined to meet the specifications. As compared to the classical Bipac, the Bipac with buried layer exhibits a much higher current gain that makes it more attractive to replace the triac in the targeted applications.

Index **AC-switch, bipolar transistor, triac, monolithic bidirectional silicon switch, power semiconductor switch**

I. Introduction

The triac [1] is a power semiconductor switch widely used in the AC mains applications (230 V – 50 Hz) due to its reliability and low fabrication cost. However, the triac is not controllable to turn-OFF and presents relatively high power dissipation due to an ON-state voltage greater than 1 V. So far, the function of a bidirectional switch is provided either by the association of unidirectional discrete devices [2-3] or by a monolithic voltage controlled device [4-5] or by a monolithic current controlled device [6-7]. Moreover, having a holding current (I_h) limits the use of the triac in low power applications (< 100 W), and therefore low load current applications (CFL, LED) [8]. In order to overcome this issue, the Bipac [9-10] was proposed. It exhibits an ON-state voltage drop lower than 1 V, allows an ON/OFF control with respect to a single reference electrode and its technological process of realization is similar to that of a classical triac. However, it has a low current gain in the conducting state [9]. In order to improve the current gain of the device without degrading its breakdown voltage, a buried layer is added within the drift region. Both of them, buried layer and drift region, are of the same type (N or P) but of different doping concentrations.

II. Comparison between the Bipac and the triac power losses

The triac and Bipac devices are both bidirectional devices that are controlled by a single gate electrode. The triac is controlled only to turn-ON while the Bipac is controlled both to turn-ON and turn-OFF. The power losses for these two devices are carried out using analytical expressions. In the conducting state, the Bipac I(V) characteristics (Fig. 1) are approximated using exponential expressions. This study considers only the worst case quadrant of an NPN-Bipac (first quadrant). The electrical circuits used for evaluating the conduction power losses within each of the two devices are shown in Fig. 2. R_g and R_L set the gate current and the maximum load current, respectively. The conduction power losses were calculated by assuming full-wave conduction in the two devices (Fig. 3). These losses involve power losses in the gate resistances as well as in the main switch.

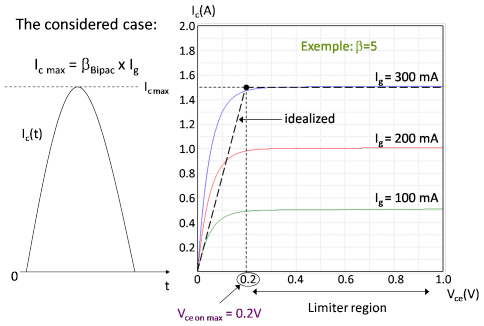

Fig. 1. I_C-V_{CE} characteristics of a Bipac in the first quadrant.

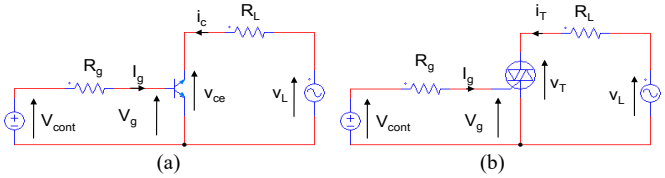

Fig. 2. Electrical circuits used for evaluating power losses in: (a) Bipac, (b) triac.

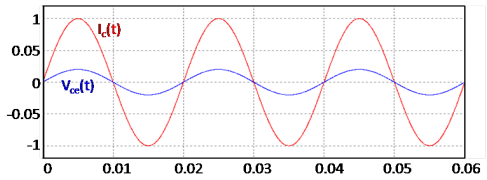

Fig. 3. Assumption of full-wave conduction for Bipac power losses evaluation.

In order to evaluate the Bipac power losses, the idealized $I_c(V_{ce})$ characteristics given in Fig. 1 is used. It is represented by a straight line giving the worst case Bipac ON-state resistance, noted R_{eq} and determined by the equation $R_{eq} = V_{ceON\,max}/I_{Cmax}$.

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The parameters used for power losses evaluations are given in table I. The different formulas used for power losses calculation in triac and Bipac devices are summarized in tables II and III, respectively. In the case of the Bipac, the gate current Ig is set by the formula I_{Cmax}/β where I_{Cmax} is the peak load current and β is the Bipac current gain.

TABLE I
PARAMETERS USED FOR POWER LOSSES EVALUATIONS

	Gate-emitter voltage	Gate current	ON-state voltage drop	Dynamic resistance
Triac (Fig.2)	Vge = 0.7 V	Ig = 20 mA	V_{Ton} = 1 V	r_d = 0.4 Ω
Bipac (Fig.2)	Vge = 0.7 V	Variable (I_{Cmax}/β)	$V_{ceON\ max}$ = 0.2 V	Non linear (see Fig. 1)

TABLE II
TRIAC CONDUCTION LOSSES EVALUATION

Gate-cathode losses	Anode1-anode2 losses	Losses in R_g
$P_g = V_g.I_g$ (Fig. 2)	$P_{A1-A2} = V_{T.ON}.I_{Aver}$ $\frac{2V_{Ton}.I_{Tmax}}{\pi} + r_d.I_{Teff}^2$ $I_{Tmax} = I_{Cmax}$ (Fig. 1)	$P_{Rg} = (V_{cont} - V_g).I_g$ with V_{cont} = 3.3 V (Fig. 2)
Total losses = $P_g + P_{CE} + P_{Rg}$		

TABLE III
BIPAC CONDUCTION LOSSES EVALUATION

Gate-emitter losses	Collector-emitter losses	Losses in R_g
$P_g = V_g.I_g$ (Fig. 2)	$P_{CE} = R_{eq}.I_{C-rms}^2$ $= \frac{V_{ceonmax}.I_{Cmax}}{2}$ $R_{eq} = \frac{V_{ceonmax}}{I_{Cmax}}$ (Fig. 1)	$P_{Rg} = (V_{cont} - V_g).I_g$ with V_{cont} = 3.3 V (Fig. 2)
Total losses = $P_g + P_{CE} + P_{Rg}$		

The evaluation of conduction losses as function of rms load current, for different Bipac current gains, is given in Fig. 4. These characteristics show that if the Bipac current gain β is higher than 5, the power losses in the Bipac are lower than those in the triac.

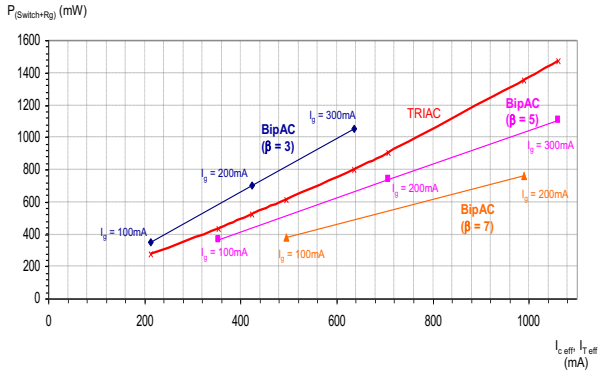


Fig. 4. Comparison between conduction power losses in the Bipac for different current gains and those in the triac.

III. CURRENT-GAIN LIMITATION OF THE CLASSICAL BIPAC

Based on previously published simulation results on the determination of Bipac cell geometrical parameters [9], the following values were used for this study: XLn = 10 µm, Xg = 2 µm and D = 5 µm (Fig. 5). Thus, the width of an elementary active cell is 17 µm. In the case of the specific targeted application, it is required that the Bipac supports a voltage of 750 V in the blocking state, and carries-out a peak collector current Ic of 0.8 A at a collector-emitter voltage Vce = 0.2 V in the conducting state. The Si-chip area must not exceed 10 mm^2.

It was determined by 2D Sentaurus simulations that 130 µm thick N-substrate is necessary while 230 µm thick P-substrate are required to meet the 750 V breakdown voltage requirement.

The current carrying capability in the conducting state was evaluated as function of the chip area (where surface area = cell width * area factor) and the gate current. In order to reach 0.8 A peak load current in the conducting state, the gate electrode must be controlled by 350 mA for 12.5 mm^2 chip area or by 300 mA for 16 mm^2 in the case of NPN-Bipac structure. Whereas, it must be controlled by 350 mA gate current for 16 mm^2 chip area in the case of PNP-Bipac structure. In conclusion, in all these cases, the chip area is still higher than the maximum acceptable 10 mm^2 chip area.

In order to meet the different specifications, a new device architecture that derives from the classical Bipac structure is proposed.

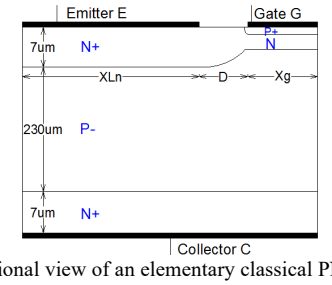


Fig. 5. Cross-sectional view of an elementary classical PNP-Bipac structure [9].

IV. THE NEW BIPAC ARCHITECTURE AND OPERATING PRINCIPLES

To improve the current gain of the classical Bipac structure, one layer of the same type as that of the drift region was inserted in this latter as shown in Fig. 6 for the case on NPN-Bipac. Thus, the NPN-Bipac structure with P-buried layer is simulated in both blocking and conducting states. The values of the physical and geometrical parameters used are indicated in Fig. 6.

Even though this section considers only the case of P-wafer, the results and the operating principles are valid for both cases: P-wafer and N-wafer.

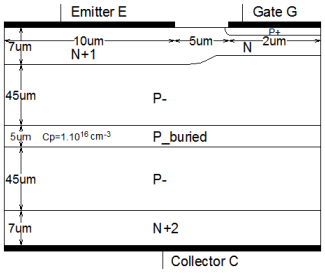


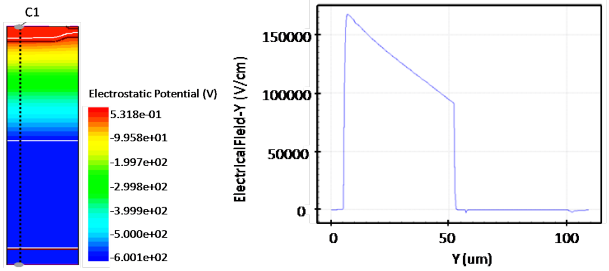
Fig. 6. Physical and geometrical parameters of the simulated NPN-Bipac with P-buried layer.

A. Blocking state

The NPN-Bipac with P-buried layer is first simulated in the blocking state. The equipotential lines at Vce = -600 V and Vce

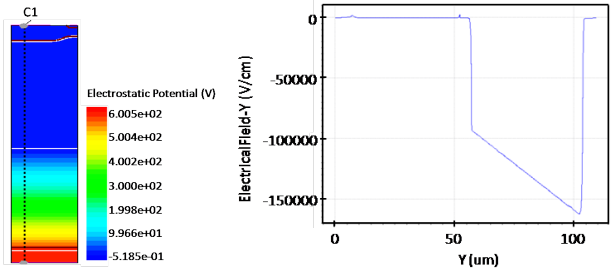
= 600 V are shown in Fig. 7(a) and Fig. 8(a), respectively. A vertical cut-line (C1) is realized in each case, and the electric field distributions are given in Fig. 7(b) and Fig. 8(b).

The P-buried layer in the drift region modifies the shape of the electrical field results in a trapezoidal electric field distribution instead of triangular distribution as in the case of the classical Bipac structure.



(a) (b)

Fig. 7. (a) Equipotential lines, and (b) electric field in the NPN structure with P-buried layer at Vce = -600 V.

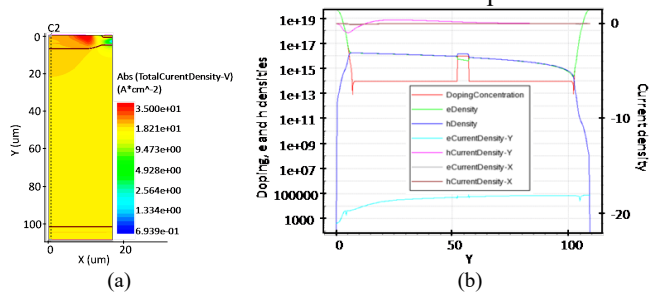


(a) (b)

Fig. 8 (a) Equipotential lines, and (b) electric field in the NPN structure with P-buried layer at Vce = 600 V.

B. *Conducting state*

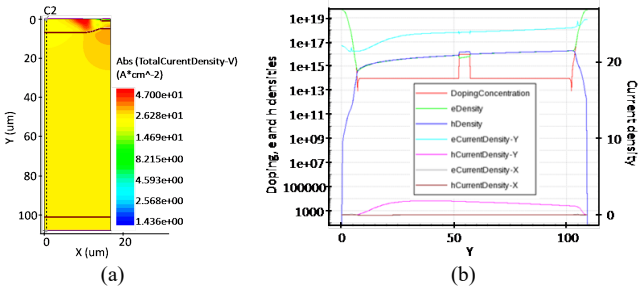
For the conducting state simulations, the NPN-Bipac structure with P-buried layer is controlled by 100 mA gate current. The chip area is set to 5 mm^2. The structure is saved in the 1st and 3rd quadrants. In each of the two quadrants, a vertical cut-line is realized in the emitter zone. Fig. 9 and Fig. 10 show the positions of the cross-sections (C2) as well as the corresponding carrier and current densities. In both illustrated cases, a strong injection of electrons in the P$^-$ drift region as well as in the P-buried layer is noticed. So, the voltage drop in the conducting state is similar to that of the classical NPN-Bipac.



(a) (b)

Fig. 9. (a) Cut-line at the emitter level on the 2D structure, (b) carrier distribution as function of Y in the 1st quadrant.

The insertion of the buried layer makes it possible to improve the current gain without degrading the breakdown voltage. Indeed, the presence of this buried layer transforms the triangular distribution of the electric field into a trapezoidal distribution and thus allowing to support the same breakdown voltage while using a lower drift region thickness. Moreover, the buried layer does not prevent the strong injection of electrons and the modulation of the conductivity of the drift region in ON-state.



(a) (b)

Fig. 10. (a) Cut-line at the emitter level on the 2D structure, (b) carrier distribution as function of Y in the 3rd quadrant.

V. Comparison between NPN and PNP Bipac structures with one buried layer

The aim is to explore the potentialities and to optimize the Bipac structure with a buried layer of the same type as that of the wafer in the case of N and P wafers. 2D simulations were carried out by mainly varying the concentration of the buried layer and the drift region thickness situated on both sides of this latter.

A. *Case of P-buried layer in the P-substrate of NPN-Bipac*

1) *Simulation conditions*

The NPN-Bipac structure simulated in the case of P-buried layer has a width of 17 µm [9]. The thicknesses Yn_1 and Yn_2 of the N$^+$ emitter region and the N$^+$ collector region respectively are equal and set at 7 µm. The thickness Yp of the P-buried layer is set at 10 µm (Fig. 11). The carriers' lifetime is 10 µs. The 2D simulations carried out have shown that a chip area of 5 mm^2 is not enough to meet the specifications, whereas a surface of 10 mm^2 can in some conditions allow to meet the electrical specifications. Consequently, to compare the two Bipacs, an area factor such that the simulated chip area is 10 mm^2 was used.

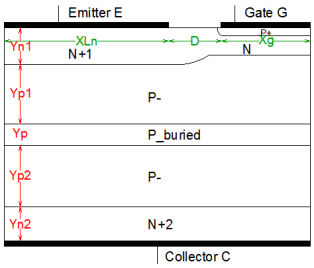


Fig. 11. Geometrical parameters of the NPN-Bipac with P-buried layer.

First, simulations were done on a wide range of P$^-$ substrate thicknesses (Yp_1 and Yp_2) and P-buried layer concentration (Cp). Note that Yp_1 always equals Yp_2. The results allowed selecting and refining the study for both 50 µm and 55 µm Yp_1 values and this for Cp concentrations ranging from 5x10^{15} cm^{-3} to 5x10^{16} cm^{-3}. In the ranges of variations of the previously defined parameters Yp_1 and Cp, the evolution of the breakdown

voltage Vbr, as well as of the collector current Ic (and thus of the current gain) for two values of control gate current Ig (100 mA and 200 mA) were studied. Thus, the pairs of parameters (Yp_1, Cp) that meet the targeted breakdown voltage condition of 750 V and the minimum Ic peak current of 0.8 A are determined. It should be noted that the results presented here are for the worst case quadrant for each of the two wafer types.

2) Gate controlled by Ig = 200 mA

The simulation results for Ig = 200 mA as well as the gain deduced are summarized in Fig. 12 and Fig. 13 respectively. The pairs (Yp_1, Cp) meeting the conditions imposed by the specifications are marked in solid (filled) patterns on the curves giving the current gain (Fig. 13).

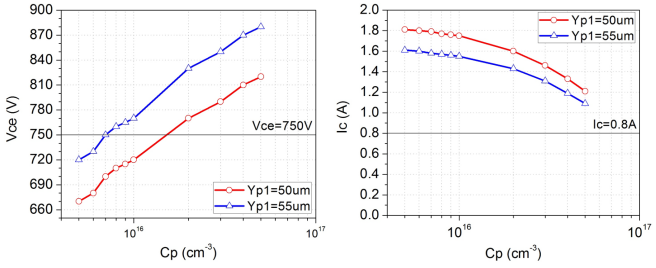


Fig. 12. (a) Breakdown voltage, and (b) collector current at Vce = 0.2 V for NPN-Bipac with P-buried layer controlled by a gate current Ig = 200 mA.

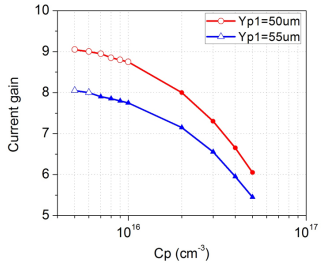


Fig. 13. Current gain of NPN-Bipac with P-buried layer controlled by a gate current Ig = 200 mA.

In summary, for a thickness $Yp_1 = Yp_2 = 50$ µm, the concentration of the P-buried layer must be between 2.10^{16} cm^{-3} and 5.10^{16} cm^{-3}. For a thickness $Yp_1 = Yp_2 = 55$ µm, this concentration must be between 7.10^{15} cm^{-3} and 5.10^{16} cm^{-3}.

3) Gate controlled by Ig = 100 mA

The simulations results for Ig = 100 mA as well as the calculated current gains are presented in Fig. 14 and Fig. 15.

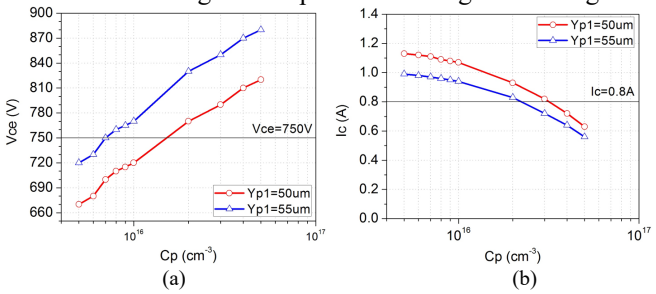


Fig. 14. (a) Breakdown voltage, and (b) collector current at Vce = 0.2 V for NPN-Bipac with P-buried layer controlled by a gate current Ig = 100 mA.

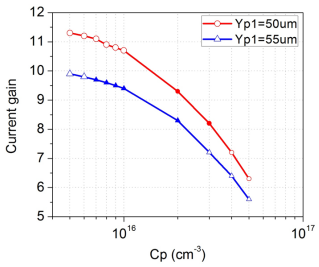


Fig. 15. Current gain of NPN-Bipac with P-buried layer controlled by a gate current Ig = 100 mA

In summary, for a thickness $Yp_1 = Yp_2 = 50$ µm, the concentration of the P-buried layer must be between 2.10^{16} cm^{-3} and 3.10^{16} cm^{-3}. For a thickness $Yp_1 = Yp_2 = 55$ µm, this concentration must be between 7.10^{15} cm^{-3} and 2.10^{16} cm^{-3}.

B. Case of a N-buried layer in the N-substrate of PNP-Bipac

The simulated structure, PNP-Bipac with N-buried layer in the N^- substrate, has a width of 17 µm. The thicknesses Yp_1 and Yp_2 of the P^+ emitter region and the P^+ collector region respectively, are set to 5 µm. The thickness of the N-buried layer is fixed at 10 µm. The carriers' lifetime is 10 µs. The area factor is chosen such that the simulated chip area is 10 mm^2.

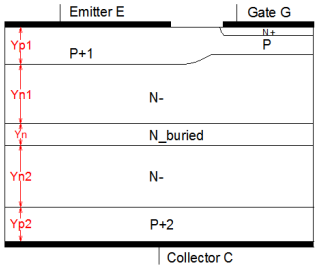


Fig. 16. Geometrical parameters of the PNP-Bipac with N-buried layer.

The simulations are carried out for N^- substrate thicknesses $Yn_1 = Yp_2$ between 40 µm and 50 µm, and for N-buried layer concentrations Cn ranging from 1.10^{14} cm^{-3} to 5.10^{16} cm^{-3}.

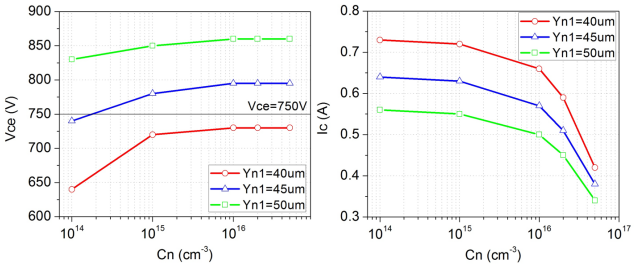


Fig. 17. (a) Breakdown voltage, and (b) collector current at Vce = 0.2 V for PNP-Bipac with N-buried layer controlled by a gate current Ig = 200 mA.

The simulation results are given in Fig. 17 and Fig. 18. It can be noticed that none of the simulated pairs (Yn_1, Cn), of the Bipac structure on N-substrate, meets the specifications. This study was carried out with a gate current of 200 mA. It is obvious that a lower gate current would not allow meeting the required specifications (Vbr = 750 V, I_{cmax} = 0.8 A, $V_{ce\ on} \leq 0.2$ V).

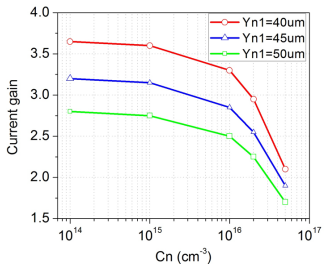


Fig. 18. Current gain of PNP-Bipac with N-buried layer controlled by a gate current Ig = 200 mA.

In the following, the paper focuses on the optimization of the NPN-Bipac structure, with P-buried layer, that offers the best performance as compared to the classical Bipac structure.

VI. Bipac ON-state losses

The physical and geometrical parameters of the Bipac structure with buried layer where selected such that to meet all the requirements, including the capability to carry a peak collector current Ic of 0.8 A while the ON-state voltage drop does not exceed 0.2 V. To highlight the impact of a peak collector current Ic (V_{ch}/Rc) higher than 0.8 A, the circuit given in the Fig. 19 is used.

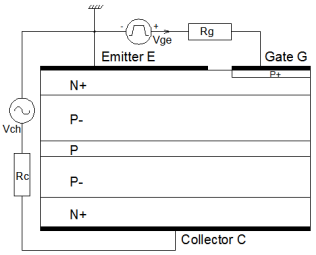


Fig. 19. Control circuit of NPN-Bipac with P-buried layer used to verify the drop voltage in conducting state.

By choosing Rc = 400 Ω and sinusoidal voltage source having an amplitude Vch = 325 V, the collector current Ic illustrated in Fig. 20 is obtained. The current Ic_{max} thus obtained is slightly greater than 0.8 A. Fig. 21 shows the voltage drop Vce waveform with zoom on the first quadrant (worst case quadrant for the NPN-Bipac). V_{max} and V_{min} indicate respectively the maximum and minimum obtained values for Vce.

For the two considered thicknesses Yp_1, only the highest concentration (Cp = 5.10^{16} cm^{-3}) is simulated. The simulation results given in Table IV reveal that the drop voltage in the conducting state remains lower than 0.2 V.

However, in the case of the NPN-Bipac with P-buried layer controlled by a gate current Ig = 100 mA, the collector current Ic flowing through the structure at Vce = 0.2 V is slightly higher than 0.8 A [Fig. 14(b)] for some selected pairs (Yp_1, Cp) such as (50 µm, 3.10^{16} cm^{-3}) and (55 µm, 9.10^{15} cm^{-3}). In these cases, when the chosen Vch and Rc are applied, and the resulting Ic current exceeds 0.8 A, the Bipac acts as a current limiter. Therefore, the Ic current flowing through the device is limited to a value of about 0.8 A (but less than Ic_{max}), while the maximum voltage V_{max} reaches values well greater than 0.2 V, as shown in the results of Table V giving the maximum and minimum voltage drop values for the selected (Yp_1, Cp) pairs. Thus, if the Bipac is controlled by 100 mA gate current, a slight variation in the P-buried layer doping concentration during the technological process will lead to a considerable degradation of the Bipac current carrying capability. Thereby, the current is limited before it reaches 0.8 A and the ON-state losses increases.

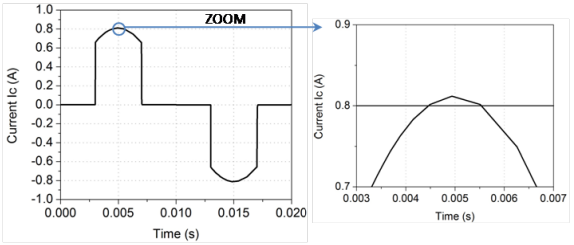


Fig. 20. Ic current waveform.

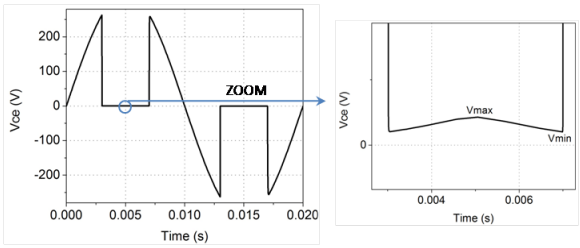


Fig. 21. Vce voltage waveform.

TABLE IV
VOLTAGE DROP IN NPN-BIPAC WITH P-BURIED LAYER FOR IG = 200 MA AND CP = 5.10^{16} CM^{-3}

	$Yp_1 = Yp_2 = 50$ µm	$Yp_1 = Yp_2 = 55$ µm
V min (V)	0.07	0.08
V max (V)	0.1	0.14

TABLE V
VOLTAGE DROP IN NPN-BIPAC WITH P-BURIED LAYER FOR IG = 100 MA

	$Yp_1 = Yp_2 = 50$ µm		$Yp_1 = Yp_2 = 55$ µm		
Cp (cm^{-3})	2.10^{16}	3.10^{16}	7.10^{15}	8.10^{15}	9.10^{15}
V min (V)	0.11	0.27	0.102	0.105	0.108
V max (V)	2.18	26	0.2	0.25	0.41

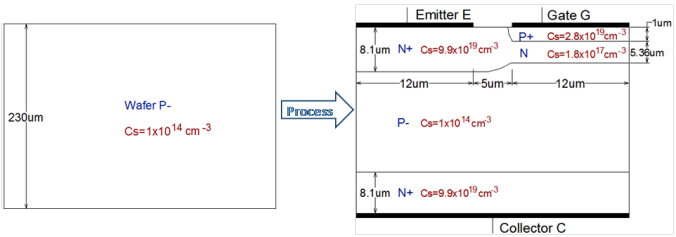
VII. Technology Process simulations

In order to validate the technological compatibility of the technological process of the NPN-Bipac with P-buried layer with that of the classical NPN-Bipac, Silvaco™ process-type 2D simulations as well as Sentaurus™ electrical 2D-simulations were used to compare the two versions of NPN-Bipac.

First, the technological process is simulated in the actual conditions of its realization by taking the dimensions defined on mask according to the drawing constraints required in the clean room at LAAS. Then, the electrical simulations were carried out with the physical and geometrical parameters thus obtained.

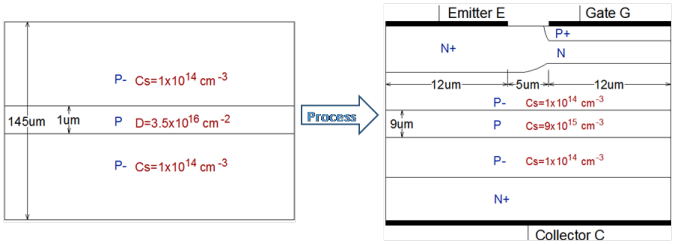
For the classical NPN-Bipac structure, the P^- wafer has a doping of $1.10^{14}cm^{-3}$, a thickness of 230 µm allowing a breakdown voltage of about 750 V (Fig. 22).

For the NPN-Bipac with P-buried layer, a multi-epitaxial wafer is considered as shown in Fig. 23. The doping profile of a buried half-layer after the process is given in Fig. 24. The peak boron doping concentration is $9x10^{15}cm^{-3}$ and junction depth is about 4.5 µm.



(a) (b)

Fig. 22. 2D simulation of the technology process realization of classical NPN-Bipac: (a) starting P^- wafer, (b) obtained structure at the end of process simulation.



(a) (b)

Fig. 23. 2D Simulation of the technology process realization of NPN-Bipac with buried P-layer: (a) Starting wafer, (b) obtained structure at the end of process simulation.

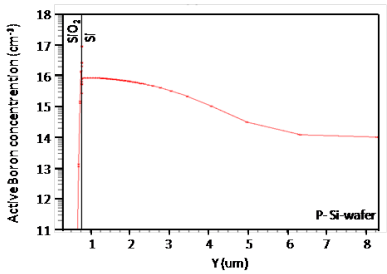
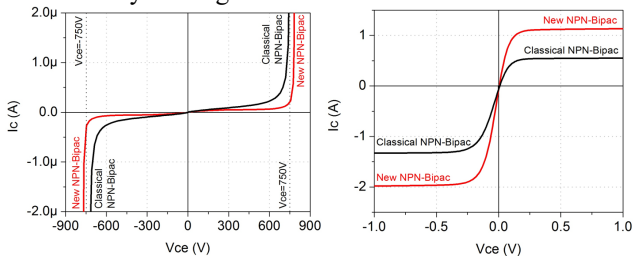


Fig. 24. Doping profile of the P-buried half-layer (in P^- wafer) obtained by technology process simulations.

The wafer thicknesses and concentrations used in the two structures allow a breakdown voltage of about 750 V as shown in the results of the electrical simulations given in Fig. 25. Similarly, the ON-state characteristics are evaluated by electrical simulation for a 10 mm^2 chip area and by applying a gate current Ig of 200 mA. It can be noticed that for a breakdown voltage of 750 V, the current gain of the NPN-Bipac with buried layer is higher.



(a) (b)

Fig. 25. Comparison of (a) the blocking capability and (b) the Ic (Vce) characteristics of the two Bipac structures (classical NPN-Bipac and NPN-Bipac with P-buried layer).

VIII. Conclusion

In this paper, the power losses in the Bipac structure were evaluated and compared to those in the classical triac. A Bipac current gain (β=Ic/Ig) higher than five is necessary in order for the Bipac to be more interesting than the triac. To that end, a new version of the Bipac, named Bipac with buried layer, is proposed in order to improve the current gain of the classical Bipac without degrading its blocking capability. The impact of using a buried layer, of doping type identical to that of the drift region, were studied in the blocking and conducting states. 2D simulation study of the Bipac with buried layer has allowed to provide ranges of values of geometrical and physical parameters that allow to meet the different specifications: breakdown voltage, peak collector current Ic, ON-state voltage drop and chip area. 2D technology process simulations coupled to 2D electrical simulations confirmed the possibility of realizing the Bipac with buried layer using the same technological process used of the classical Bipac structure. However, the starting wafer of the Bipac with buried layer is a multi-epitaxial wafer. The comparison of the electrical characteristics of the two Bipac versions (with buried layer and classical) confirmed the improvement in the current gain. Indeed, the current gain with the Bipac with a buried layer is more than five which makes it attractive to replace the triac in the targeted applications

IX. Acknowledgement

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