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Fast detection of EMC level drifts induced by aging using biased thermal step stress : Application to an AC input EMC filter

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Abstract—This paper presents the use of step stress accelerated aging tests associated with VNA measurements to efficiently detect the risk of potential EMC level drifts. The method is applied to an AC input EMC filter and a deviation in common mode attenuation is observed. Key points ensuring the validity of the results are discussed. Perspectives and limits are presented.

Index Terms—EMC filter, aging, step stress, EMC drift, conducted emission, EMC deviation, accelerated aging test

I. INTRODUCTION

The standard-based traditional techniques used to perform EMC characterization are sometimes considered inadequate, as they do not consider the actual conditions met by electronic systems. In response, a risk-based approach of EMC is emerging [1] [2] [3].

The aging of electrical materials and its effect on EMC levels at long term is one of the aspects that must be taken into account to ensure functional safety many years after a product is released. Studies have been conducted at discrete component [4] [5], integrated circuit [6] [7] and system levels [3] [8] but no general conclusion can be drawn. Since predicting the drifts is complex and time consuming, a first quick evaluation of the risk of potential EMC level drifts could be very valuable.

Performing aging studies involves selecting stress conditions of accelerated aging tests such as temperature. Selecting a high stress temperature induce a high acceleration factor, which is especially interesting for a fast detection method, but may lead to overstress conditions from which no conclusions can be pulled. On the other hand, selecting a lower temperature slows down the acceleration process, resulting in longer test times.

In response to this problem, protocols such as step stress allow to start with a low temperature and gradually increase it. Therefore it combines high temperature to efficiently accelerate the aging of electronic components, while low temperatures provide a comparison to look for overstress conditions

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that may appear at higher temperatures. A drawback of this method is that no aging model can be extracted since multiple temperatures are used.

The aim of this paper is to present how step stress can help to quickly detect EMC level drifts. First, the EMC filter used as a case study and the experimental setup are presented. Then, the reliability of the results is discussed. After, aging results are presented. Finally, a simple electrical model of the filter is presented, associated with some perspectives and an overview of the work.

II. CASE STUDY AND EXPERIMENTAL PROTOCOL

This paper focuses on a replica of the main input EMC filter of the 60 W flyback converter UCC28750EVM-071 evaluation board. A common mode choke and two class-Y capacitors are used for common mode rejection and a class-X capacitor is used for differential mode rejection as presented in Fig. 1a.

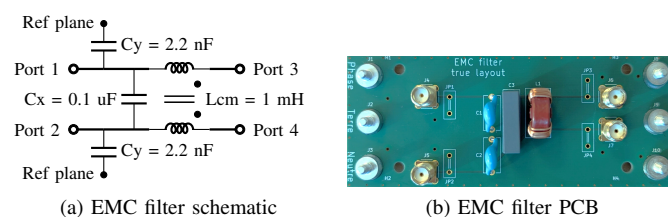


Fig. 1. Case study : AC input EMC filter

The study consists of successive characterizations of the differential and common mode attenuation of the filter. Between each characterization, the device is stored at high temperature while being biased. At each step, the stress temperature is increased according to the values listed in Table I. Each temperature is held constant for 66 hours. Devices are characterized at ambient temperature.

TABLE I
STEP STRESS TEMPERATURES

Step	Stress temperature
Step 1	120 °C
Step 2	135 °C
Step 3	150 °C
Step 4	165 °C

Fig. 1b presents the EMC filter board used in the study. SMA connectors are connected to the filter terminals via 2 cm matched lines to perform 4 port measurements with a VNA. Differential and common mode attenuation are then extracted from S-parameters measurements as described in CISPR 17 [9]. Vias placed on each line can be connected with jumpers to the main power supply for biasing during accelerated aging tests. This dual configuration keeps the measurement lines independent of the bias network during VNA measurements.

This type of power supply has a typical switching frequency around 100 kHz and a rise time of about 10 ns. This results in a conducted emission where the most of the power is between 100 kHz and 100 MHz. Therefore, this frequency range is the main range of interest for this study. However, in anticipation of future studies, measurements were made over the full range of the VNA, between 9 kHz and 4 GHz.

III. RELIABILITY OF THE RESULTS

When studying the evolution of the filter characteristics, a very good accuracy of the measurement process is required to ensure that the measured changes are a consequence of component degradation. Therefore, at each step of Table I, reference boards left at ambient temperature are characterized with the same protocol as the stressed ones. If any deviation appears on these boards, it is due to the measurement protocol itself. Figs. 2 presents multiple measurements of the common mode attenuation of a reference filter board. The worst case of both common mode and differential mode attenuation presents a standard deviation of less than 1 dB over the entire frequency range.

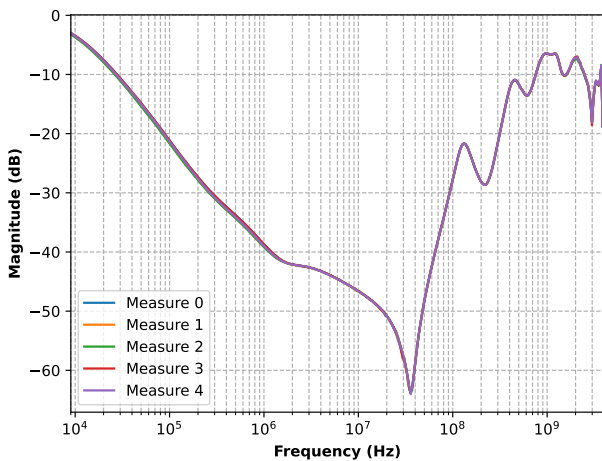


Fig. 2. Successive measurements of reference board common mode attenuation

As the entire board is stressed, another challenge is to account for the aging of the traces and the SMA connectors. Therefore, a board with 2 cm lines connected in short, open, load and through configurations is stressed. The deviations of the S-parameters are monitored. Hence, with a de-embedding process, the effect of the traces can be removed for each step. Fig. 3 presents the evolution of the different configurations.

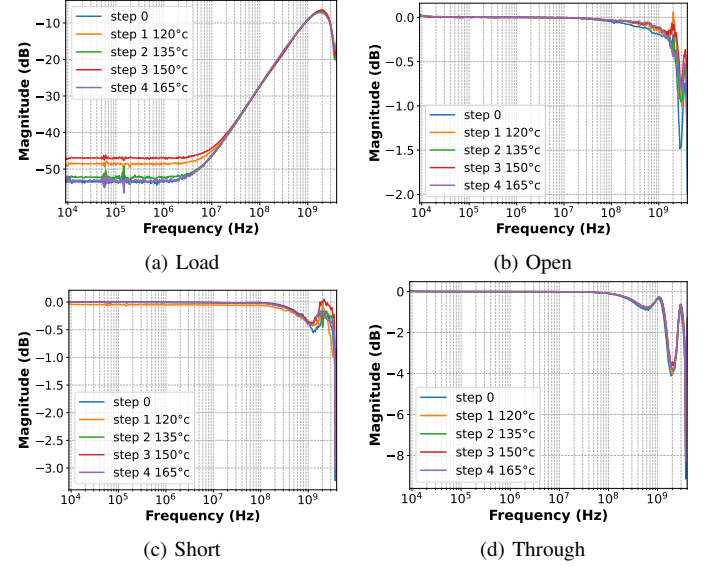


Fig. 3. Evolution of calibration kit during step stress

While the short, open and through configurations require only SMA connectors and traces, the load configuration requires a 50 ohm resistor mounted at the end of the line. As this load is a reference, it cannot be stressed with the rest of the board. Thus, in this protocol, the load is mounted for the measurement phase and is disassembled before starting the stress phase. This assembly cycle was studied on an unstressed board to verify it does not affect the validity of the results. Fig. 4 presents S11 measurements for successive assembly cycles of the same resistor on the same board.

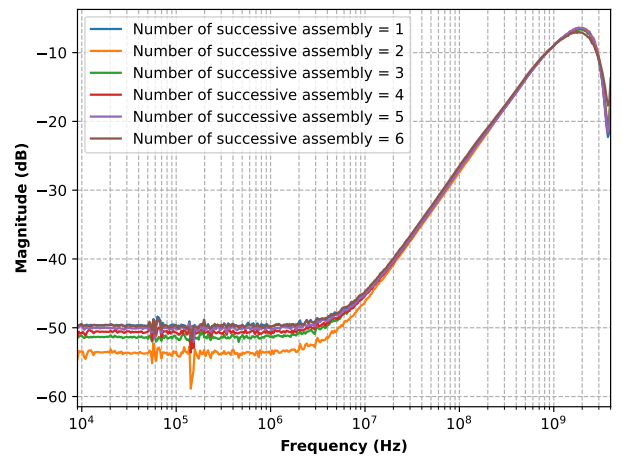


Fig. 4. Load S11 after multiple resistor's assembly cycles

Some deviations in low frequency appear but the S11 coefficient remains close to or below -50 dB as expected for a matched load. Therefore the effect of the resistor assembly cycles is considered negligible in this study. In addition, the resistor will certainly fail before a significant deviation appears, as it failed in open circuit after 7 consecutive assembly cycles.

IV. STEP STRESS RESULTS

Figs. 5 and 6 present the measurements of differential and common mode attenuation over the different steps. Between step 0 and step 3 the differential mode attenuation seems unaffected by the stress. Between step 0 and step 4 the common mode attenuation displays a clear deviation of about 6 dB in the low frequency range between 10 kHz and 10 MHz. As this frequency range is mostly affected by the common mode choke, this reduction in attenuation efficiency is likely to be linked to a decrease in the nominal inductance of the common mode choke.

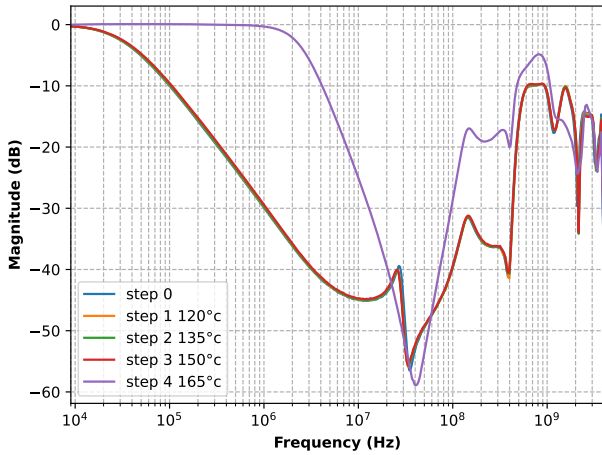


Fig. 5. Evolution of differential mode attenuation

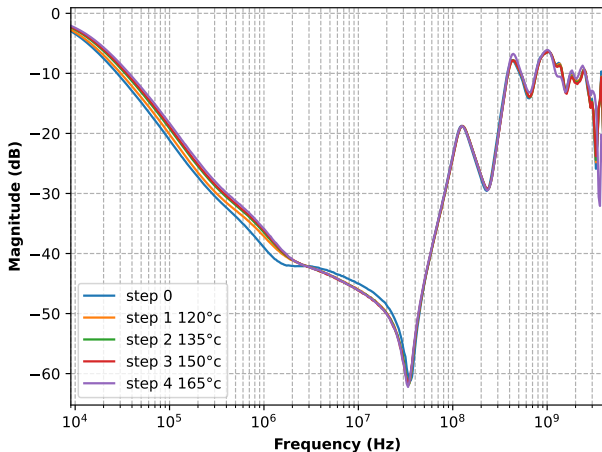


Fig. 6. Evolution of common mode attenuation

At step 4 the differential mode attenuation shows a brutal change, dropping to 0 dB between 10 kHz and 1 MHz. This

is not a consequence of aging but more likely the result of an over temperature leading to a sudden breakdown of the class-X capacitor in open circuit. Fig. 7 displays another failure mechanism where the traces connecting one of the SMA connectors and the filter burst in open circuit. Hence, the filter is no longer measured and results cannot be analyzed. These results confirm the importance of stress temperature selection. For further studies, a stress temperature between 130 and 150 °C seems adequate as it provides a high acceleration factor without overstressing the devices.

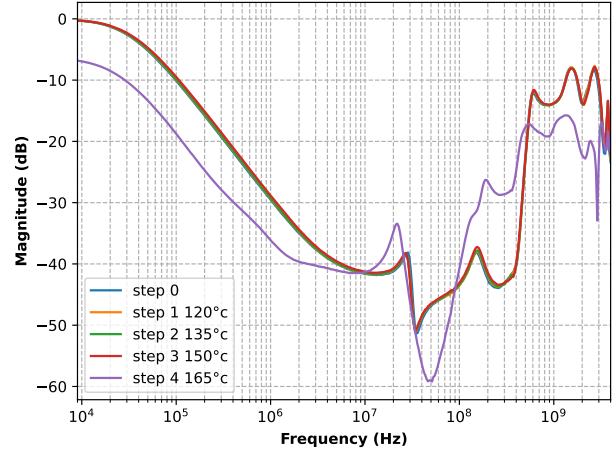


Fig. 7. Evolution of second board differential mode attenuation

Fig. 8a presents the aspect of the class-X capacitor which probably failed in open circuit. Figs. 8b presents the burnt trace near an SMA connector. The temperature induced stress on the board might have created a conductive path between the main line (connected to the trace) and the earth (connected to the body of the SMA) during the accelerated aging test. This highlights the difficulty to produce HF measurement boards with small isolation tolerances compatible with aging studies.

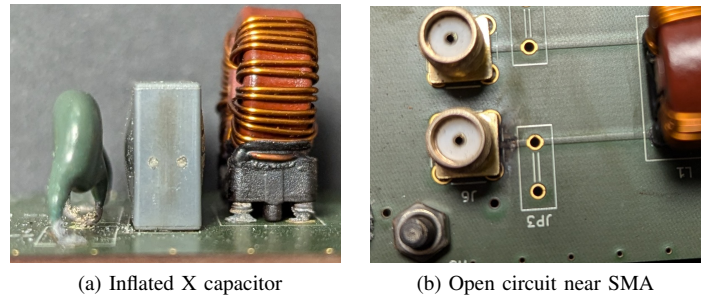


Fig. 8. Failure mechanisms at step 4

V. MODELING AND PERSPECTIVES

As mentioned in the previous part, the deviation of common mode attenuation at low frequency can be intuitively linked to a reduction of the nominal common mode inductance. To verify this hypothesis, a simple first-order HF electrical model, shown in Fig. 9 is created from the manufacturer's data of

the discrete components. The interconnection traces are not modeled as their influence can be ignored below 100 MHz.

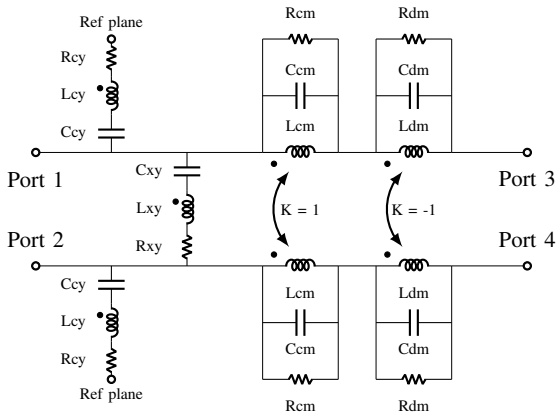


Fig. 9. Electrical model of the EMC filter

After some tuning of the parameters, a good fit between simulation and measurement of the fresh board at initial state can be obtained up to 100 MHz as shown in Fig. 10. The model could be enhanced by considering inductive coupling between components or by improving the model of the common mode choke at higher frequencies. However, since the main objective of such filter is to reduce noise propagation for frequencies below 100 MHz, the model is considered sufficient for the study.

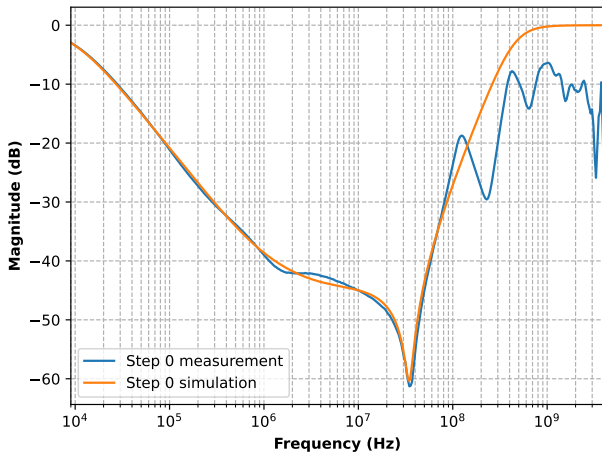


Fig. 10. Common mode attenuation : simulation vs measurements at initial state

By using the same model and simply reducing the nominal common mode inductance of the common mode choke, a good fit can be obtained with the state 3 measurements as shown in Fig. 11. This verifies the hypothesis and can help to quantify the reduction of the nominal common mode inductance, which is about 20%. For further studies, to predict the evolution of the filter characteristics, a fixed temperature test focused on the common mode choke should be considered to precisely characterize its evolution according to the stress time.

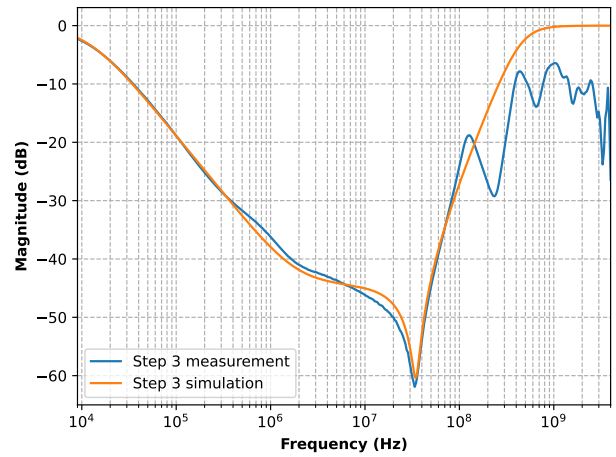


Fig. 11. Common mode attenuation : simulation vs measurements at state 3

VI. CONCLUSION

This paper has presented how step stress can be used to quickly detect EMC level drifts on an EMC filter. This technique allows a range of temperatures to be used during the accelerated aging test to efficiently speed-up the aging process while looking for overstress conditions at high temperature. In addition, the results can be analyzed to focus future tests on some components of interest and to help select an appropriate stress temperature. For this study, a deviation in common mode attenuation was observed and related to the aging of the common mode choke. Stress temperature up to 150°C could be used on this component to extract its aging law.

REFERENCES

- [1] L. Devaraj, A. Ruddle, A. Duffy, "Electromagnetic Risk Analysis for EMI Impact on Functional Safety With Pro-babilistic Graphical Models and Fuzzy Logic", IEEE Lett. on EMC Practice and Applications, Dec. 2020, Vol. 2, No. 4, pp. 96-100.
- [2] D. Pissoor, K. Armstrong, "Why is the IEEE developing a standard on managing risks due to EM disturbances?", in proc. of 2016 IEEE Int. Symp. on EMC, July 2016, pp. 78-83.
- [3] A. Boyer, H. Huang, S. Ben Dhia, "Predicting the risk of non-compliance to EMC requirements during the life-cycle", in Proc. of 2016 Asia-Pacific Int. Symp. on EMC, Shenzhen, China, May. 2016, pp. 452-455.
- [4] A. Lekdim, L. Morel, M.A. Raullet, "Magnetic properties evolution of a high permeability nanocrystalline FeCuNbSiB during thermal ageing", The European Physical Journal Applied Physics, Aug. 2017, 10.1051/epjap/2017160449.
- [5] A. Gupta, O.P. Yadav, and D. DeVoto, J. Major, "A Review of Degradation Behavior and Modeling of Capacitors", in Proc. of ASME 2018 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, San Francisco, USA, Aug. 2018, ind. V001T04A004.
- [6] S. Ben Dhia, A. Boyer, "Long-term Electro-Magnetic Robustness of Integrated Circuits: EMRIC research project", Microelectronics Reliability, 2013, Vol. 53, pp. 1266-1272.
- [7] J. Al Rashid, M. Koohestani, L. Saintis, M. Barreau, "A State-of-the-Art Review on IC EMC Reliability", in proc. of the 31st European Safety and Reliability Conference, Sept. 2021, pp. 1850-1857.
- [8] H. Huang, "Development of predictive models for the electromagnetic robustness of electronic components", PHD thesis, INSA Toulouse, France, 2015.
- [9] CISPR 17: 2011 - Edition 2.0 - Methods of measurement of the suppression characteristics of passive EMC filtering devices, International special committee on radio interference, 2011.