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Inductance and capacitance parasitic prediction thanks to data analysis applied to SiC MOSFET wide frequency band characterization

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Abstract

The paper presents a wide frequency band characterization for modeling discrete SiC MOSFET - TO247 package. The data analysis is conducted for several components and for three configurations driving to several impedances to characterize. An accurate *RLC* model of the transmission behavior between two ports is given over 1 MHz to 1 GHz. Moreover, the performance of the differential impedance, which is a generic indicator that eases the identification process, is discussed. Some conclusions are provided on the best way to run the characterization.

1. Introduction

Due to the energetic transition, it is important to increase the power density ratio related to power electronics devices. The use of wide band gap semiconductors such as SiC and GaN, allows to develop new power electronic devices with higher efficiency [1][2]. Nevertheless, the higher switching speeds, combined with parasitic elements due to the packaging and the system itself, produces switching oscillations. A mitigation solution is to embed integrated capacitances [3], where their values as their integration is related to the parasitic inductance to face. Thus, the SiC behavior, and more precisely the parasitic inductance prediction, is of major importance. On the one hand, wide frequency characterization methods appear to be one way to get the inductance value [4]. On the other hand, during aging, it was demonstrated that a degradation process changed the wide frequency impedance behavior [5]. To conclude, getting an accurate inductance value prediction, and being able to monitor the impedance change induced by the degradation are still challenging.

Based on [4][6][7], methods for extracting parasitic capacitance and inductance are used. The models' validity are obtained over a wide frequency range: $10\ kHz - 200\ MHz$. In this work, the validity of the models is extended up to 1 GHz, beyond the frequency ranges previously considered. This extension enables a more accurate identification of inductive elements, which are significant in the impedance measurements within the frequency range of 30 MHz to 1 GHz.

It is notable that, to support both converter design and the detection of packaging-related degradation, a robust and well-characterized modeling framework is essential. Failures can be monitored through the various *RLC* electrical parameters. In particular, for degradation detection, automated analysis using a complete impedance measurement dataset and an interpretable physically-based model allowing to distinguish between various degradation mechanisms is a key objective. This is the purpose of the off-state wide frequency characterization, that reveals both capacitances at low frequency, and inductances at higher frequency. Moreover, the equivalent model prediction targets to predict any parameter change following the damage state.

Thus, in addition to modeling, this paper presents a study examining the impact of inherent choices in the measurement setup that can significantly influence the accuracy of the results. A statistical approach, along with a systematic comparison of different setups, is therefore necessary to reinforce the measurement methodology and enable the acquisition of refined models.

The paper is organized as follows. The second section describes the test bench used for TO247 packages wide frequency characterization. The protocol established is synthetized. In the third section, the characterization method is applied to healthy SiC MOSFET TO247 devices over 1 MHz to 3 GHz. It is emphasized how a slightly different methodology strengthens the accuracy of the inductance extraction. In addition, the validity of the

model is increased up to 1 GHz. In the fourth section, a statistical analysis confirms the preliminary results by indicating that the differential impedance is easier to extract and more accurate for modeling.

2. Wide frequency characterization test bench applied to discrete component

2.1. Test bench description

The Fig. 1 presents the test bench used for the wide frequency characterization. As presented in Fig. 1, to perform the high frequency characterization, a PCB interface, made of an FR4-epoxy, 1.6 mm thick, and copper tracks, 35 µm thick, is designed. Its connection to a Vector Network Analyzer (VNA) is achieved thanks to 3 Sub-Miniature of Type A connectors (SMA). The two measurement ports are thus connected to the gate, the drain or the source of the SiC MOSFET whereas the third port can be shorted or connected to a 50 Ω load.

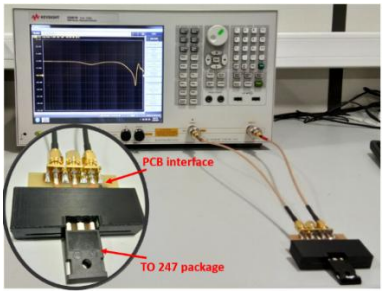

Fig. 1 Wide frequency test-bench

2.2. Wide frequency characterization process

As established earlier [5][6] a scattering parameter characterization followed by the impedance behavior reconstruction is performed. The VNA (Keysight E5061B) achieves a small signal measurement. VNA allows the characterization of scattering–parameters (S-parameters) in two-port networks, port 1 and port 2 respectively. The S-parameters establish relationships between their input/output ports in terms of wave power reflection and transmission [8]. The impedance parameters (Z-parameters) are obtained through an off-line post-processing process based on VNA measurements [4]. Every measurement presented is obtained thanks to a computation based on an initial S- parameters' set. Measurements are done in zero bias conditions. Therefore, devices behave as passive networks. For the whole frequency band, 1601 points are stored. Every point is the average made on 16 successive measurements. The VNA raw data are directly used.

3. Wide frequency characterization of SiC MOSFET

3.1. Full bandwidth analysis overview

Table 1 The 3 measurement configurations

Configuration name	VNA Port 1	VNA Port 2	Free Port (50 Ω or shorted)
Configuration 1	Source	Drain	Gate
Configuration 2	Source	Gate	Drain
Configuration 3	Drain	Gate	Source

The Z-parameters are computed for 10 components from the same reference (C2M0160120D). Let us emphasize that components were never used before. Measurements are conducted in three configurations as detailed in Table 1. In each configuration, the Z-parameters obtained are denoted as follows: Z_{11} for input impedance at port 1, Z_{12} for coupling impedance from port 1 to 2, Z_{21} for coupling impedance from port 2 to 1 and Z_{22} for input impedance at port 2. The third port, denoted the free port, can be connected either to 50 Ω or a short load. The impact of this choice is a key point of the paper and will be discussed later.

3.2. Initial limits of low frequency electrical equivalent circuit

To discuss the performance of the proposed method, a single prototype is analyzed as done in [4][6]. The 4 S-parameters are obtained. Then, the equivalent impedances are extracted. The impedance model is simplified as Z_{12} equals Z_{21}. Then, the following equivalent electrical circuit, is used to extract the parasitic elements.

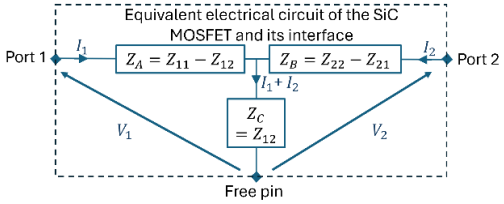

Fig. 2 Three impedances equivalent electrical circuit

Z_A, Z_B and Z_C are related to the input and coupling impedances depicted in § 3.1. In the following, as it is assumed that the inductive behavior is mainly due to the source wire bonds, the impedance of the source pin, denoted Z_{Source} is depicted. Following the configuration, Z_{Source} corresponds to Z_A or Z_C.

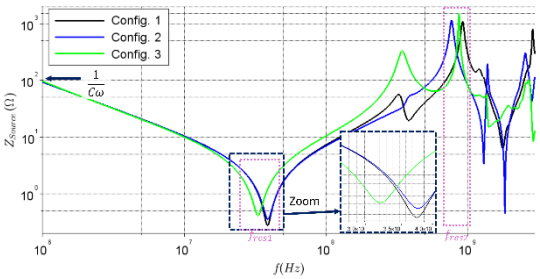

Fig. 3 Equivalent Z_{Source} for the three configurations when the free port is shorted

Fig. 3 illustrates Z_A, - configurations 1 and 2 - and Z_C, - configuration 3 - when the free port is shorted. Each impedance behavior can be segmented into three distinct frequency bands based on the first and second resonant frequency f_{res1} and f_{res2}. The first two frequency bands are analyzed according to methodology detailed in [6]. As expected, a *RLC* behavior is recovered at low frequency, around the peak resonant frequency f_{res1}. In any configuration, the capacitive behavior due to the off state of the SiC MOSFET is identifiable under f_{res1}. It is obvious that C value remains almost similar following the configurations. Its value is identified at $f = 1\,MHz$ and provided in Table 2. Between f_{res1} and f_{res2}, the inductive behavior is associated with the loop inductances of the component. Usually, three resistances, three inductances and three capacitors, - one per port - are identified. The identification process should be done in every configuration. Nevertheless, Table 2 emphasizes the differences that can be obtained. In the following, the L identification is targeted. There are two identification methods: the first is to study the slope of the inductive behavior, for $f \geq 10 * f_{res1}$. The second, used in [6], is based on the resonant frequency. At such a frequency, $\omega = \frac{1}{\sqrt{LC}}$. Thus, in our study, Fig. 3 demonstrates that following the configuration, the resonant frequency is not fixed for a given impedance but highly depends on the configuration. It is demonstrated that two values are obtained for the inductance. The first is $9.9 \pm 0.2\,nH$ and the second $13.8\,nH$.

Table 2 Extracted *RLC* parameters in each configuration, with a shorted strategy for the free port

	C_s	L_s	R_s
Config. 1	1.70 nF	9.92 nH	0.28 Ω
Config. 2	1.71 nF	9.89 nH	0.35 Ω
Config. 3	1.67 nF	13.8 nH	0.41 Ω

This result is recovered for the 10 samples.

3.3. Extension of the modeling frequency range

To ease inductances prediction, it is worthy to analyze the impedance behavior between f_{res1} and f_{res2}. A non-perfect inductive behavior is revealed, as the associated slopes are not straight lines. It is first analyzed in the present paper. In our demonstration, focusing on L_s value, configurations 1 and 2 should reveal the transmission impedance where L_s impacts more. Then, a pure inductive behavior, represented by a straight line is simulated, such as $Z_s = j2\pi f L_s$, and $L_s = 9.8\,nH$. As illustrated in Fig. 4, it does not match at all. Surprisingly, $L_s = 13.8\,nH$ provides better fitting. It is more obvious looking at the measurement obtained in configuration 2, with a free port connected to a 50 Ω load. In such a case, the impact of the current to ground return path is minimized, revealing the perfect inductive behavior of SiC MOSFET. Finally, a *RLC* circuit, parallelized with a C_p capacitance representing the SMA parasitic, is superimposed. It demonstrates nicely how the modeling fits quite perfectly at low and medium frequencies, e.g. $f \leq f_{res2}$. Let us remark that accuracy at f_{res2} can be improved using a *RC* model for the SMA connectors. This latter improvement is not the focus point of the paper and is not considered in the following. The result highlighted the interest of using a 50 Ω connection for the free port for the correct model identification process. As far as the *L* and *C* values are concerned, there is still a challenge to face, when dealing more precisely with SiC MOSFET. Indeed, at low frequency the constant capacitor model points out the nonlinearity of real input capacitors of SiC MOSFET. This known behavior is revealed in the proposed wide frequency band characterization. Effectively, when $f \leq f_{res1}$ the behavior does not match the constant C_s model. Nevertheless, the configuration dependance remains.

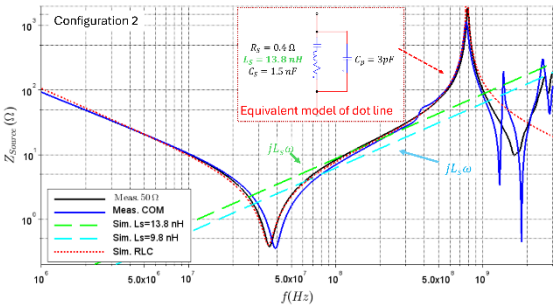

Fig. 4 Comparison of measurements in configuration 2 and perfect models for several values of L_s

3.4. SiC MOSFET behavior at a glance

The wide frequency behavior of the SiC MOSFET is explained in the following, thanks to an equivalent electrical scheme provided in Fig. 5.

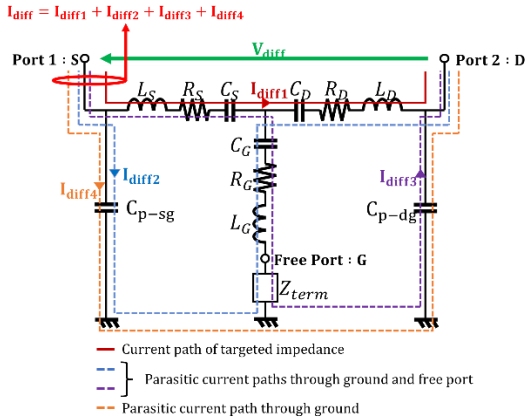

Fig. 5 Current paths' during a measurement

During the two port measurement, several current paths are characterized. Based on Fig. 5, four current paths and their couplings are revealed. Whereas the most interesting one is $Z_{diff} = \frac{V_{diff}}{I_{diff1}}$, which is related to f_{res1}, three others interact. The I_{diff4} current path is linked to f_{res2}. The two last, namely I_{diff2} and I_{diff3} allow understanding the disturbing resonances experienced between f_{res1} and f_{res2}. Effectively, in such an example, L_G is coupled to both C_{p-SG} and C_{p-DG}, leading to disturbing resonances. The disturbing resonances prevent an accurate identification of the inductive behavior and consequently, to extract the correct L value and extend the *RLC* model validity beyond 200 MHz. Using a 50 Ω load connected to the free port (i.e. the Gate port) acts as a damping resistor, minimizing ringing effects. Consequently, with this approach, the model's validity extends up to 1 GHz, enabling L identification.

4. Data analysis applied to the wide frequency band characterization

Depending on the configuration, the parasitic elements values are slightly different. Using the mean values computed on 10 prototypes, it is recovered a mean value of $L_s = 13.5\,nH$ in configuration 1, whereas $L_s = 14.6\,nH$ in configuration 2. Then, for a further simulation purpose, the averaging of the three configurations is one solution. In such a way, there is a loss of accuracy.

In the following, Z_{Source} is still analyzed and equals Z_A in configuration 1 and 2 or Z_C in configuration 3. The Relative Standard Deviation RSD is plotted for each configuration. The RSD is when the standard deviation is divided by the mean value at each frequency. In Fig. 6, a 5% RSD error line is plotted to highlight the performance. As stated previously, there is a loss of accuracy close to f_{res1}. Dealing with Z_C is different, as when $f \leq f_{res2}$, the identification process will produce an error, lower or really close to 5%. Meaning that for Z_C, the error made during the identification process is lower than for Z_A and Z_B impedances.

To summarize, a wide frequency identification is possible up to $f = 1\,GHz (\leq f_{res2})$, using a 50 Ω load for the free port. However, the accuracy of inductance extraction based on Z_A and Z_B measurements is not guaranteed. Effectively, a small deviation in the measurement of the value retained for the resonance frequency will have a challenging impact. Moreover, the resonance frequency depends on the configuration, which leads to uncertainties for the equivalent model consideration. In the following, Z_{diff} is used to address the above challenges.

4.1. Averaged differential impedance model Z_{diff}

Finally, the differential impedance, a generic indicator, is computed such as

$$Z_{diff} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \quad (1)$$

An average is done on the 10 characterized samples. The Fig. 7 illustrates Z_{diff} in configuration 1, where a 50 Ω load is connected to the gate.

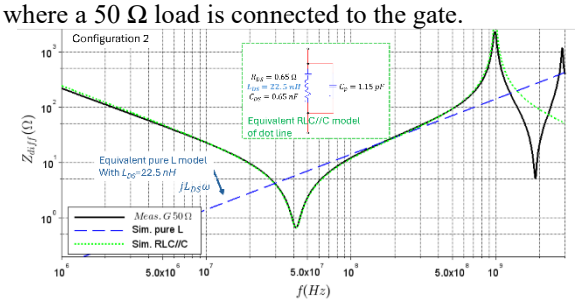

Fig. 7 Z_{diff} for config. 1 and 50 Ω connected to the gate

At low frequency the expected behavior remains. Considering, Z_{diff} eliminates undesired common mode resonances. More precisely, contrary to Fig. 2, there is no resonance peak between f_{res1} and f_{res2}. Thus, Z_{diff}

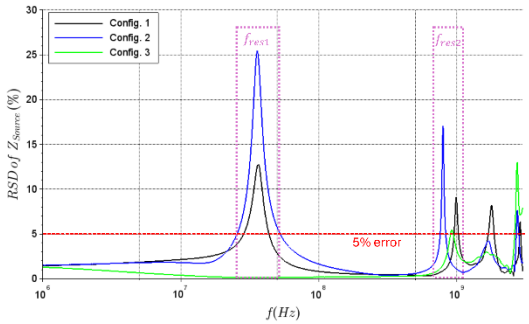

Fig. 6 Relative standard deviation in configuration 1 and 50 Ω strategy for Z_A, Z_B and Z_C

reflects the transmission packaging behavior. As illustrated in Fig. 7, an equivalent electrical circuit is simulated and superposed to the experimental curve. The parasitic values of the model are given in Table 3.

Table 3 Parasitic values of the equivalent model of Z_{diff}

C_{DS}	L_{DS}	R_{DS}
0.65 nF	22.5 nH	0.65 Ω

The RSD analysis is better, being below 5% for the whole bandwidth and when $f < 1\ GHz$. For such a conclusion, Z_{diff} should be compared to Z_A and Z_B sum. Using $Z_{diff,}$, and a 50 Ω connection for the free port, an accurate and single transmission equivalent model between two ports, namely the Drain and the Source, is obtained. The inductance is easier to extract. As illustrated in Fig. 8, comparing the three configurations enables the difference in inductances to be monitored. In configuration 1, the inductive behavior, L_{DS} is the sum of L_D and L_S contributions. In configuration 2, the inductive behavior L_{GS} is the sum of L_G and L_S. In configuration 3, the inductive behavior L_{GD}, is the sum of L_D and L_G. As expected, the greatest inductance is recovered for configuration 2 where the most inductive parts, namely the source and gate path contribute. This impact is due to the gate wire bond being added to several source bond wires. The overall current path length is also contributing, leading to a clear shift between this configuration and the other two. Effectively, measurement configurations 1 and 3 have similar lengths. This can be recovered from Fig. 5 analyze. Consequently, their inductive behavior is almost similar. In both configurations, the drain path does not contribute, as there are no wire bonds. The difference between both are related to the difference between L_G and L_S. For C2M0160120D device, there are several source wire bonds, whereas a single gate wire bond is present. As a matter of facts, the L_S inductance is lower than L_G.

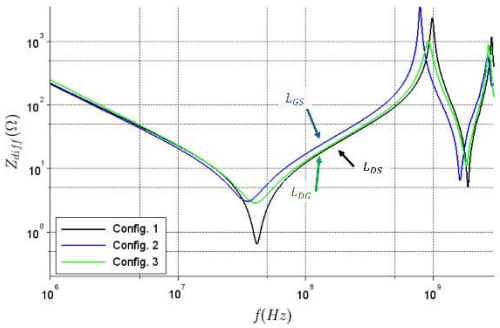

Fig. 8 Z_{diff} in all configurations and 50 Ω connection

This difference can be used to monitor wire bond failure, between healthy and faulty devices. Furthermore, this method reveals the location of the failure, as the source and gate bond wires affect differently the three differential impedances. This interesting use of Z_{diff} was demonstrated in [5].

5. Conclusions

This paper discusses the wide frequency equivalent model of the off state SiC MOSFET. The model is obtained using a S-parameter measurement. Several parasitic values, representing the MOSFET and its package, are extracted, following the impedance considered. The paper demonstrates that a 50 Ω load connected to the free port provides better accuracy. This latter can be improved using the differential impedance, which is a unique impedance that models the wide frequency transmission between two ports.

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