HAL
open science

Optimization of the elaboration of insulating layers for the gate structures and the passivation of MIS-HEMT transistors on GaN

Richard Meunier

To cite this version:

Richard Meunier. Optimization of the elaboration of insulating layers for the gate structures and the passivation of MIS-HEMT transistors on GaN. Electronics. Université Paul Sabatier - Toulouse III, 2016. English. NNT : 2016TOU30150 . tel-01376016

HAL Id: tel-01376016

https://laas.hal.science/tel-01376016v1

Submitted on 4 Oct 2016

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Université Fédérale
Toulouse Midi-Pyrénées

THÈSE

en vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par :

Université Toulouse 3 Paul Sabatier (UT3 Paul Sabatier)

Présentée par

Richard MEUNIER

Soutenue le mercredi 22 juin 2016

Optimization of the elaboration of insulating layers for the gate structures and the passivation of MIS-HEMT transistors on GaN

(Optimisation de l'élaboration de couches isolantes pour les structures de grille et la passivation de transistor MIS-HEMTs sur matériau GaN)

Directeurs de thèse **:**

M. Frédéric MORANCHO – Professeur des Universités, Université Toulouse 3

M. Alphonse TORRES – Ingénieur CEA-LETI

Membres du Jury

M. Yvon CORDIER	Directeur de Recherche CNRS, CNRS-CRHEA	Rapporteur
Mme Marie-Paule BESLAND	Directrice de Recherche CNRS, IMN Jean Rouxel	Rapporteur
M. Farid MEDJDOUB	Chargé de Recherche CNRS, IEMN	Examinateur
M. Gaëtan TOULON	Ingénieur, EXAGAN	Examinateur
M. Alain CAZARRÉ	Professeur des Universités, Université Toulouse 3	Examinateur

Table of contents

Acknowledgments **i**

General Introduction **iii**

1 GaN for power electronics : state of the art and context **1**

1.1 Power electronics and devices 1

1.1.1 Needs and demands of the market, specifications, theory VS reality 1

1.1.2 Limits of silicon 3

1.1.3 Wide band gap materials 5

1.1.4 Figures of merit of semiconductors for power application . . 9

1.2 Place of GaN in power electronics 11

1.2.1 Generalities on GaN and crystal structure 12

1.2.2 GaN properties 13

1.2.2.1 Electric properties 13

1.2.2.2 Physico-chemical properties 18

1.2.3 The AlGaN/GaN heterostructure 19

1.2.3.1 Spontaneous and piezoelectric polarization 21

1.2.3.2 Bidimensional electron channel 23

1.2.4 Models and formation mechanisms 26

1.3 Context of Ph.D. 31

1.4 Conclusion 33

2 The Metal Insulator Semiconductor structure on GaN **35**

2.1 Presentation of the structure 35

2.1.1 Principle of operation 35
2.1.2 The metal-semiconductor junction 37
2.1.2.1 Full depletion approximation 37
2.1.2.2 Full depletion analysis 38
2.1.3 HEMT and MIS-HEMT threshold voltage 41
2.2 Dielectrics on GaN and AlGaN 45
2.2.1 MIS on GaN and AlGaN 46
2.2.2 Surface contamination and interface states density 48
2.3 Gate recess etching 50
2.3.1 Principle 50
2.3.2 Threshold voltage increase 51
2.4 Conclusion 52

3 Device realization 55
3.1 Origin and characteristics of the material 55
3.2 Surface conditioning 57
3.2.1 Chemical treatments 57
3.2.2 Plasma treatments 58
3.3 MIS-HEMT and capacitance fabrication 59
3.3.1 Process flow 60
3.3.2 Encountered difficulties and adopted solutions 61
3.3.3 MESA etching insulation 63
3.3.4 Metallization and ohmic contact 63
3.3.5 High-κ dielectric deposition and in-situ N_2 plasma treatment 64
3.3.6 Gate metal deposition 65
3.4 Optional process : recess etching below gate 66
3.5 Conclusion 67

4 Results and discussions 69
4.1 Surface treatments and their characterization 69
4.1.1 X-Ray Photo-electron Spectroscopy 70
4.1.1.1 Principle 70
4.1.1.2 Application to the AlGaN surface 73
4.1.2 Chemical treatments 74

4.1.2.1 HCl and SC2 treatments 74
4.1.2.2 NH_4OH and SC1 77
4.1.3 Plasma treatments 81
4.1.3.1 Oxygen plasma 81
4.1.3.2 Nitrogen containing plasma 81
4.1.4 Surface treatments conclusion 84
4.2 Schottky gate devices 85
4.2.1 C(V) results 85
4.3 MIS structures 88
4.3.1 Thermal ALD structures 88
4.3.1.1 C(V) results 88
4.3.1.2 $I_d(V_g)$ results on circular transistor with L_g=100μm 91
4.3.2 PEALD structures 93
4.3.2.1 C(V) results 93
4.3.2.2 $I_d(V_g)$ results on circular transistor with L_g=100μm 99
4.4 Influence of the dielectric thickness 101
4.4.1 C(V) results 102
4.4.2 $I_d(V_g)$ results on circular transistor with L_g=100μm 103
4.4.3 Threshold voltage evolution 105
4.5 Influence of post-deposition thermal treatment 106
4.5.1 C(V) results 107
4.5.2 $I_d(V_g)$ results on circular transistor with L_g=100μm 109
4.6 Superiority of PEALD over thermal ALD 111
4.7 Normally-Off architecture : MIS structure with partial or full AlGaN recess etching 119
4.7.1 Gate Recess Etching 119
4.7.1.1 C(V) Results 119
4.7.1.2 $I_d(V_g)$ results on circular transistor with L_g=100μm 122
4.7.1.3 Threshold voltage evolution 124
4.7.2 AlGaN Full-recess etching below gate 125
4.8 Conclusion 127

General conclusion **129**

Perspectives 133

Bibliography 134

Acknowledgments

First and foremost I would like to thank the CEA-Leti and the LAAS-CNRS for allowing me to do my PhD under their care and supervision. I would like especially to thank the LC2E laboratory and all its members in CEA-Leti, where I had the chance to do the entirety of my thesis under the supervision of Mr. Alphonse TORRES. Regarding LAAS-CNRS, I would like to thank the professor and supervisor of my work, Pr. Frédéric MORANCHO who supported me continuously during all my research. It was a great pleasure and privilege to work with all these competent and kind scientists and researchers.

Still in CEA-Leti, I would like to acknowledge the PTA (Plateforme de Technologie Amont) and the CIME (Centre Interuniversitaire de MicroElectrnoique), which offered me the possibility and necessary formations to work on their equipment. A special thanks goes to all the members of those two clean rooms which assisted me during my PhD and provided with invaluable knowledge, help and advice.

I would also like to thank the III-V Lab which provided me with some very good quality material and services, which greatly contributed to the success of my work and my obtaining great results.

This section could not be complete without thanking Dr. Yvon CORDIER and Dr. Marie-Paule BESLAND which agreed to be my reviewers, and were very kind and comprehensive all throughout the correction process. Acknowledgments go as

well to the other members of my jury, Mr. Farid MEDJOUB and Mr. Gaëtan TOULON, and its president Pr. Alain CAZARRÉ.

Last but not least, a special thanks goes to my family, friends and CEA co-PhD students who supported, encouraged and assisted me all along my PhD research. They have been a tremendous support during those years, and I consider myself very lucky to have them in my life. The last word goes to my companion, Julie RANDRIANARISOA, without whom I could never have come as far as I am now. Her love and infallible support is greatly responsible for me completing this PhD, and I will always be grateful for her being at my side.

So again, to all these great peoples and institutions : thank you very much !

General Introduction

Throughout the 20th century, humanity has thrived like it never had before, mostly through the use of fossil fuels and their derivatives. Whether it be for transportation, energy production or synthetic products, most of the world and its industry as we know it now would not have been, and still could not be possible without the use of oil and gas. However, as we now entered the 21st century, we also realize the dire impacts this had on our environment. Greenhouse gas levels have never been as high as they are now, and CO_2 emission has become one if not the major concern in ecology throughout the world. But despite the growing global awareness of the problem, energetic needs are constantly rising due to economic growth of emerging countries and world population growth, with International Energy Agency estimations predicting that electricity consumption throughout the world could rise by 75% in less than 25 years (according to Areva). And with the rapid decay of fossil fuels reserves, we could soon be confronted with one of the major challenges humanity has ever faced. As a consequence, innovation in the energy domain has become one of the main research focus this last years. The advent of solar and wind technology paved the way for new possibilities in terms of clean energy production, and hybrid or fully electrical technologies have recently made leaps in terms of performance and sustainability.

Parallel and directly linked to the development of those various "green" technologies, energy conversion has now become one of the cornerstones for the impro-

vement of electrical performances and consumption. As electronic devices become more and more complicated, energy conversion systems have multiplied and are often the guarantors of an optimal functioning. Generally referred to as power electronics, they are most of the time constituted of semiconductors like power transistors, which can in turn be directly linked to losses in circuits. With more than 10% of the produced energy being lost in the conversion process [1], improving those systems has become mandatory for a better, cleverer and more economical way of managing energy.

Largely dominated by silicon based components, the semiconductor industry is now gradually faced with a growing need for evolution, particularly in the power industry. While they have greatly contributed towards circuits performance optimization, Si based technologies are now arriving at maturity and their further growth has become limited by the intrinsic properties of the material. As such, it becomes necessary for a new generation of components to appear in order to push back the limits defined by actual technology. As such, large band gap material appear as one of the go-to solutions, their physical properties largely surpassing the ones of silicon or this particular application. Recent years studies have notably been marked by the arrival of incredible like gallium nitride GaN and silicon carbide SiC. Furthermore, recent developments in heteroepitaxy of GaN on Si allowed to combine the efficiency of improved performance with low cost production on large scale wafers (200 mm). It thus marked a real rupture with silicon components and became a very serious candidate for future generations of power converters.

However, despite its appealing properties and general scientific consensus on its potential, GaN on Si technology is still being confronted with many challenges that hinder its developments and slows its market introduction. This is particularly true for high bias (>1000 V) and high current (> 100 A) applications where quality of the material and robustness of technology are primordial. It is precisely in this context that this Ph.D. is inscribed, through the study and development of one of the key technological steps that comes into play for the fabrication of a MIS-

HEMT (Metal Insulator Semiconductor - High Electron Mobility Transistor). The present work will be mostly focused on the insulating step of the process, with the main objective of improving the electrical behavior of the transistor through gate leakage reduction while reducing interface states density. This manuscript is the culmination of three years of studies and experimentation and is divided in four chapters.

Chapter 1 : This chapter will first focus on describing the properties of a power converter should have in order for them to respond to the needs and demands of the current market, and highlight why there is a need for wide band gap materials in today's industry. It will then assess the place of GaN in power electronics through the study of its properties, and expose the reasons why it is becoming a key player.

Chapter 2 : Focused on the Metal Insulating Semiconductor on GaN, this second chapter will review the different equations responsible for the unique and peculiar behavior of transistors made on an AlGaN/GaN heterostructures. As it is the main subject of the present study, the major focus will then be on the introduction of the insulating layer and the impact it will have on the MIS-HEMT's electrical properties. Also, and though it was at first not intended to be realized during this Ph.D., the influence of the gate recess etching on the threshold voltage increase will also be described in the last part of the chapter.

Chapter 3 : This chapter will describe all the different technological steps I put in place and performed during my Ph.D. First, I will describe the surface conditioning processes that were studied. In a second time, I will expose all the process flow that was used in order to achieve the completion of functional MIS-HEMT structures, through the creation of diodes and circular transistors in particular. Lastly, I will detail the optional process of recess etching below the gate that I could implement inside the devices' elaboration

Chapter 4 : This final chapter will be the heart of the present study, where the results of my work will be presented and commented upon. In a first part, surface treatments and their characterization will be the main topic, with an emphasis on the results obtained through X-ray Photo-electron Spectroscopy. The rest of the chapter will then review all the electrical results that were obtained through the study of Schottky gate devices and fully functional MIS-HEMT structures. Capacitance C(V) and gate current $I_d(V_g)$ measurements will be at the center of those results. They will assess the impact of the insulating layer deposition method, how results evolve depending on its thickness, and how post deposition thermal treatment might have an influence. Last but not least, I will present how a partial or full gate recess etching impacted electrical properties and helped to achieve a normally-off architecture.

1

GaN for power electronics : state of the art and context

1.1 Power electronics and devices

1.1.1 Needs and demands of the market, specifications, theory VS reality

The ever growing demand of energy is one of tomorrow's greatest challenge if we want to keep the standards as they are today. Despite our efforts, the demand for electricity keeps to increase, and is expected to do so more than any other resources in future years. With a growth of 2.5% each year, levels of demand and

production of electricity should be twice as large in 2013 as they were in 2006.

The technology using power electronics is the key to regulating energy flux between the power source and the devices. In every system needing electricity to operate, it is responsible for reliability, stability and efficiency of the way in which the energy is spent. And whether it be for personal computers and domestic appliances, or for transportation and heavy industry, global semiconductor market in this particular domain is accountable for more than 50 billions of dollars in 2010 alone. Optimization of power management requires components able to sustain high voltage and current levels, at high frequencies and high temperature, with low losses in conduction as well as commutation.

Power electronics is the technology that concerns energy conversion. With less than 50 years of existence, it still is a young technology but has known a great and rapid development in recent years, due to the fact that more than 15% of produced electrical energy needs some kind of conversion. It is a technology that is based on commutation electronics, and takes advantage of the properties of a perfect switch : it does not dissipate any energy, whether it is perfectly closed (null resistance, no bias between source and drain) or perfectly opened (infinite resistance, no current going through). When associated with different filtering elements, it is thus theoretically possible to modify voltage and/or current, without any losses. Unfortunately, reality does not match theory yet and losses are still unavoidable because of the physical components which are part of power switches. However, the increasing efficiency in the devices and the overall size, weight and cost reduction allowed the generalization of power electronics components in domains where losses must be kept to a minimum, in order to reduce heating and achieve high yield performances. The automotive market is a perfect example where such technology will play a key role in future developments. In the coming 20 years, it is expected that cars will evolve from fully thermal to fully electric while going through intermediate hybrid states. The energy management in these new kind of engines is becoming more and more challenging and will require sophisticated elec-

tronic modules such as power converters in order to sustain optimum functioning regimes.

1.1.2 Limits of silicon

Today, silicon is the core material used in most semiconductor technologies. It is at the foundation of modern electronics as we know them and can be found in a large majority of components. But with the rapidly increasing demand in power electronics, the microelectronics industry is now confronted with the intrinsic limits of silicon.

As stated earlier, power components play the role of switches with two different states :

- an on-state, where specific resistance R_{ON} must be as low as possible. We sometimes use $R_{ON} \cdot S$, S being the active surface of the power component, in order to introduce a notion of volume and cost.

- an off-state, where the voltage withstand must be as high as possible until breakdown voltage V_{BD} is reached.

Both characteristics are closely related to the lowly doped layer (epitaxial layer in most cases), which plays a double role : it ensures the voltage withstand in the off-state, and has an important resistive effect in the on-state. We thus have the following relation :

$$R_{ON} \cdot S(\Omega \cdot cm^2) = \alpha \cdot V_{BD}^{\beta} \tag{1.1}$$

where α and β are two positive and real constants. This equation defines the limits of silicon : the value of the specific on-state resistance cannot be inferior to a value related to the bias we want the power component to sustain.

If we look at figure 1.1, we can see the silicon limits and how they fare comparatively to large band gap materials and different architectures.

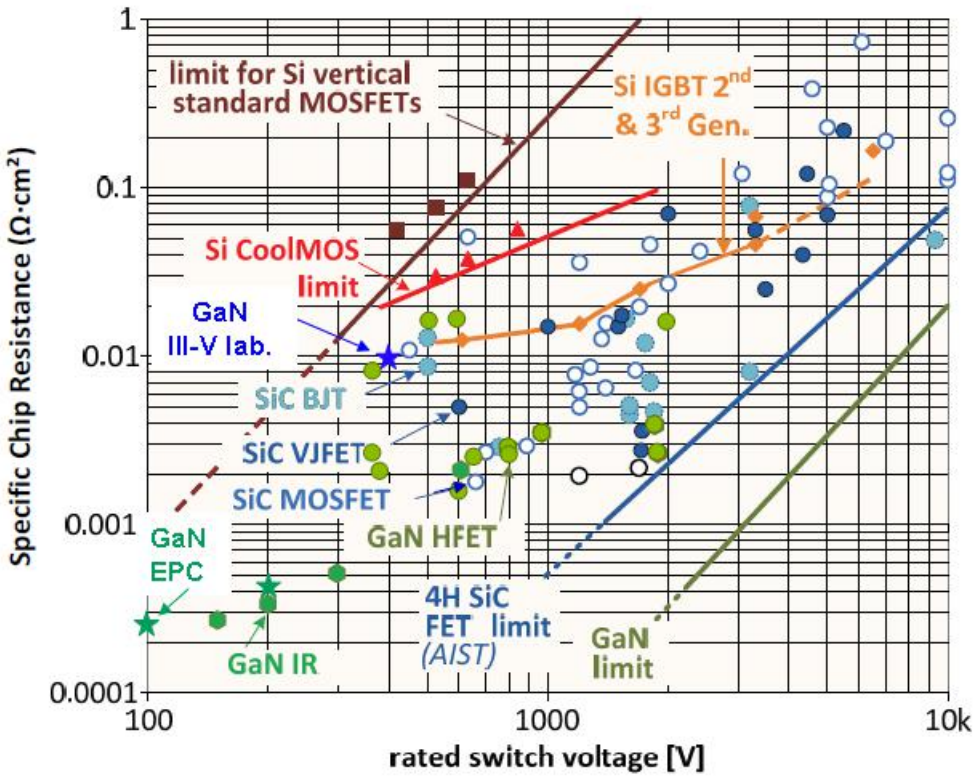

FIGURE 1.1 – Specific chip resistance R_{on} in function of rated switch voltage for different materials.

We can see that there is a large zone where silicon components cannot grant the needed characteristics, even with complex architectures such as IGBTs for instance. And if we want to comply with the power increase, it has become necessary in silicon technology to increase the size of the components. However, this does not represent a viable solution since the size increase will lead to higher energy losses, especially in commutation, and that does not agree with the current market tendency where size reduction and high energy efficiency are of the utmost importance. It is thus capital to develop a new and innovative technology based on compatible materials for us to overcome those limitations.

1.1.3 Wide band gap materials

In this context where silicon is no longer an option, the emergence of wide band gap materials is regarded as the most promising solution in the power electronics industry. With operating constraints such as high temperatures (300-700 K) and high voltage ($\geqslant$ 600 V), silicon carbide (SiC), gallium nitride (GaN) and diamond are the most promising candidates to date. Compared to silicon, they present the advantage of working on a large scale of temperatures, a high breakdown electric field and a high electron saturation velocity.

Having a large band gap (around 3 eV) will reduce the thermoionic carrier formation, which, if to high, can change the nature of the semiconductor. Those carriers are formed following an Arrhenius law, $n = n_0 e^{-E_a/kT}$, where E_a is the activation energy, k the Boltzmann constant and T the temperature. In the case of semiconductors, the activation energy is the gap energy E_g. This explains why large band gap materials are preferable for high temperature uses, since the higher E_g will be, the lower the influence of temperature becomes.

And furthermore, critical breakdown field in semi-conductor materials is directly related to their band gap energy [2, 3]. So the higher the band gap, the higher the breakdown field is, which allows these materials to have exceptional voltage withstands.

Table 1.1 shows the main electrical characteristics of conventional and wide band gap semiconductors.

	Conventional semiconductors		Large band gap semiconductors			
	Silicon	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Gap energy E_g (eV)	1.12	1.43	3.03	3.26	3.39	5.45
Electron mobility μ_n ($\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$)	1450	6500	850	980	1250	2000
Hole mobility μ_p ($\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$)	450	400	101	115	35	2000
Critical breakdown field E_c ($\mathrm{MV} \cdot \mathrm{cm}^{-1}$)	0.3	0.4	2.5	3	3.3	10
Intrinsic carrier density n_i (cm^{-3})	$1.\times10^{10}$	$2.\times10^{6}$	$2.\times10^{-6}$	$8.\times10^{-9}$	$1.\times10^{-10}$	$1.\times10^{-27}$
Thermal conductivity λ ($\mathrm{W} \cdot \mathrm{cm}^{-1} \cdot \mathrm{K}^{-1}$)	1.412	0.455	4.9	4.9	1.3	20
Relative permitivity ϵ_r	11.8	13.1	9.66	10.1	9.5	5.7
Electron saturation velocity ν_{sat} ($\times10^7$ $\mathrm{cm} \cdot \mathrm{s}^{-1}$)	1	1	2	2	2.2	2.7

TABLE 1.1 – Electrical properties of conventional and wide band gap semiconductors.

Of all the different materials, diamond exhibits the best overall properties for power applications, followed by gallium nitride which is also a good candidate for optoelectronics and power due to its direct gap and its breakdown electric field 10 times that of silicon. However, it has the smallest thermal conductivity, compared

to the other materials.

With three different crystalline structures available, silicon carbide is also a good candidate for power electronics. With an hexagonal atomic structure, 4H-SiC and 6H-SiC are only differing by their mobility which is isotropic in the first and super to the anysotropic one in the last. 3C-SiC has the highest electron mobility and saturation velocity because of reduced phonon scattering resulting from the higher symmetry of its cubic atomic structure.

All those materials have a higher breakdown field compared to silicon and are able to sustain a voltage roughly 10 times superior. Consequently, for the same voltage withstand, a component made from wide band gap material can be made with a thickness 10 times inferior, or with a doping a 100 times higher in the drift section (lowly doped layer) than that of a typical PN^- junction. For this typical kind of junction, the breakdown voltage is directly related to the critical breakdown electric field following this relation :

$$V_{BD}(V) = \frac{\epsilon_0 \cdot \epsilon_r \cdot E_c^2}{2 \cdot q \cdot N_d} \tag{1.2}$$

where ϵ_0 and ϵ_r are respectively the void and the semiconductor permittivity, q is the electron elementary charge, N_d the doping level in the N^- region and E_c the critical breakdown field.

Specific on resistance can be given by this equation [4] :

$$R_{ON} \cdot S(\Omega \cdot cm^2) = \frac{27 \cdot V_{BD}^2}{8 \cdot \epsilon_0 \cdot \epsilon_r \cdot \mu_n \cdot E_c^2} \tag{1.3}$$

where μ_n is the electron mobility.

Figure 1.2 shows the superiority of wide band gap materials overs silicon.

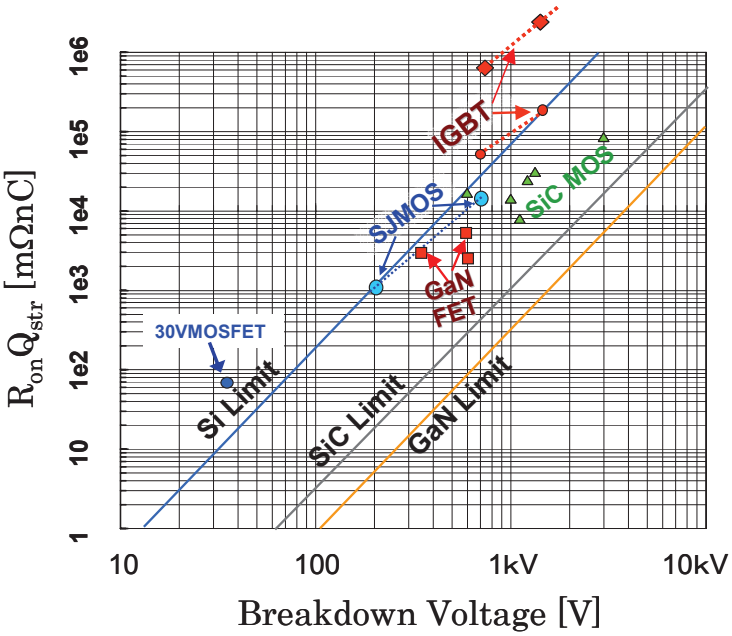

FIGURE 1.2 – R_{on} versus breakdown voltage for Si, SiC and GaN, with their respective limit[5].

For a unipolar component presenting specific on-resistance below 1 $\Omega \cdot cm^2$, limits of silicon is around 1 kV whereas wide band gap semiconductors allow the fabrication of components able to sustain more than 10 kV. For advanced power applications, only those materials are able to cope with the needed specifications as can be seen in figure 1.1).

Again, diamond is the material presenting the best electrical and thermal properties. With its low intrinsic carrier concentration, it is thus able to sustain high temperatures. However, its fabrication process is still at an early stage and conditions to achieve the production of diamond are still hard to meet. Furthermore, if we limit ourselves to the previous equations, we do not take into account technological aspects which can have an important role, such as changing the mobility through the use of doping, which is a very difficult process to implement in diamond.

Compared to diamond and GaN, SiC is the material presenting the most advanced technology, with actual power devices being commercialized. The JFET on

SiC transistor is right now the most advanced power switch, being able to perform at temperatures up to 300 °C. However, the high price of large SiC diameter substrates and associated epitaxies (around a 100 times higher than silicon) makes it a debatable solution in terms of economical concerns.

1.1.4 Figures of merit of semiconductors for power application

In order to compare the possible power electonics performance of different materials, some commonly known figure of merit are liste in Table 1.2. The numbers in this table have been normalized in repect to Si, and le larger the number, the better the material's performance in the corresponding category. We can notice that SiC polytypes and GaN have similar figures of merit, which implies similar performances. Diamond's figure of merit are at least 40 to 50 times more than any other semiconductor in the table.

Material	Si	GaAs	6H-SIC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81,000
BFM	1.0	14.8	125.3	223.1	186.7	25,106
FSFM	1.0	11.4	30.5	61.2	65.0	3,595
BSFM	1.0	1.6	13.1	12.9	52.5	2,402
FPFM	1.0	3.6	48.3	56.0	30.4	1,476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5,304,459
BPFM	1.0	0.9	57.3	35.4	10.7	594
BTFM	1.0	1.4	748.9	458.1	560.5	1,246,711

TABLE 1.2 – Main figure of merit for wide bandgap semiconductors compared with Si [6]

JFM Johnson's figure of merit is a measure of the ultimate high frequency capability of the material. More specifically, it is the product of the charge carrier saturation velocity in the material and the electric breakdown field under same conditions, first proposed by A. Johnson of RCA in 1965.

$$JFM = \frac{v_{sat} E_{BD}}{2\Pi} \tag{1.4}$$

where v_{sat} is the saturation velocity and E_{BD} is the electric field at which impact ionization initiates breakdown. Unfortunately, this figure of merit is difficult to determine experimentally as both v_{sat} and E_{BD} are intrinsic properties of a device, although easily found from simulation.

BFM Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET [7]. The BFM is useful in order to compare different semiconductor materials in high power voltage applications. It takes into account the barriers mobility and the dielectric permittivity of the material, as well as its critical electric field. It is expressed as :

$$BFM = \varepsilon_r \mu_n E_c^3 \tag{1.5}$$

It is mainly used for low frequency applications where conduction losses are predominant. It gives an appreciation in terms of voltage sustaining capability.

FSFM This is the FET switching speed figure of merit.

BSFM This is the bipolar switching speed figure of merit.

FPFM This is the FET power handling capacity figure of merit.

FTFM This is the FET power switching product figure of merit.

BPFM This is the bipolar power handling capacity figure of merit.

BTFM This is the bipolar switching product figure of merit.

1.2 Place of GaN in power electronics

Gallium was discovered in 1875 in France by Lecoq de Boisbaudran through the spectroscopy analysis of the zincblende from Pierrefitte in the French Pyrénées. Discovered around 1920, gallium nitride GaN crystal was first studied in the seventies but was then abandoned due to synthesis difficulties. In the nineties, under the influence of Japanese research groups, great progress was achieved in synthesizing the crystal. In 1997 and 2000, the development of a new prototype of MBE (molecular beam epitaxy) for Research and Development (R&D) allowed to grow nitride materials such as GaN. Because of its direct gap, it was first used for optoelectronic devices. Later on, its mobility and its high electron saturation velocity was used for designing HEMT (high electron mobility transistors) structures for high frequency (HF) application, and high temperature and high voltage applications were possible thanks to its high breakdown field. Until then, difficulties with high levels of P doping, resulting in device resistance being too important, represented a great challenge for HF bipolar technologies. However, work is still under progress in order to solve the inherent problems associated with technological process :

- GaN does not exist in liquid phase, which makes it difficult to obtain bulk GaN substrates. To date, epitaxy is realized on sapphire, silicon carbide or silicon substrates through metal organic chemical vapor deposition (MOCVD) in order to reduce fabrication costs. The choice of the substrate is based on a compromise between price, performances and device reliability ;

- thermal oxidation, which is largely used in the silicon MOS and CMOS industry, is not possible on GaN due to the poor quality of the native oxide ;

- P type doping is still a problem ;

- despite the fact that it is now possible to produce high quality material on 200 mm silicon substrates, defect density remains very high ;

Nowadays, silicon IGBTs and thyristors are the only available options for high voltage applications (1 - 10 kV), but it is expected that GaN unipolar components (HEMTs and MOSFETs) could replace those devices. This could lead to higher frequencies, higher voltages and higher temperatures of operation. However, GaN thermal conductivity is relatively low which poses problems to evacuate heat during conception of the devices. Nonetheless, it remains much cheaper than diamond and far more adapted to doping.

1.2.1 Generalities on GaN and crystal structure

Gallium nitride (GaN) is part of the nitride III-N family which is composed of boron-nitride (BN), aluminum-nitride (AlN) and indium-nitride (InN). They can crystallize under a cubic or hexagonal form, but the hexagonal phase is the most stable we can achieve through standard growing conditions. Those two structures are zinc blende (cubic) and wurtzite (hexagonal) which can be seen in figure 1.3.

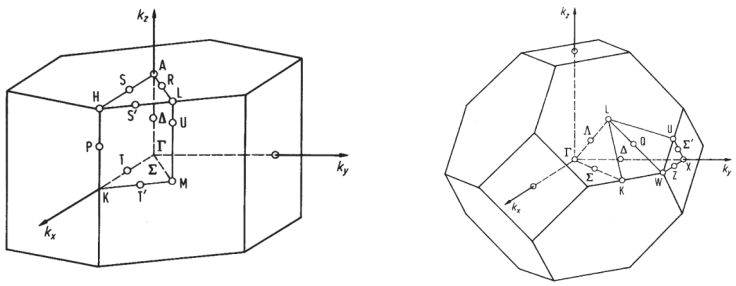

FIGURE 1.3 – GaN cubic Zinc Blende (left) and hexagonal Wurtzite (right) structure.

The latter is the one being used in laboratory for GaN layers epitaxy due to its metastable nature, which presents numerous crystalline properties suitable to the elaboration of heterojunctions. Table 1.3 shows the crystal parameters of both structures.

	Cubic c-GaN	Hexagonal h-GaN
Lattice parameter	$a_{300K} = 4.511$Å	$a_{300K} = 3.188$Å $a_{300K} = 5.185$Å

TABLE 1.3 – Lattice parameters for GaN crystalline structures.

The c/a ratio of the GaN lattice is very close to the $\sqrt{8/3}$ theoretical value for a perfect hexagonal structure. We can thus assume that gallium atoms are in lowly distorted tetrahedral sites.

1.2.2 GaN properties

1.2.2.1 Electric properties

GaN is a semiconductor presenting a direct band gap, which means that the conduction band minimum (E_c) and the valence band maximum (E_v) are at an almost identical value on the diagram representing the energy E relatively to the wave vector k. For GaN, this point is located at the Γ point, center of the Brillouin zone (k = 0). The first Brillouin zones and the band structures in the major direction are represented in figure 1.4.

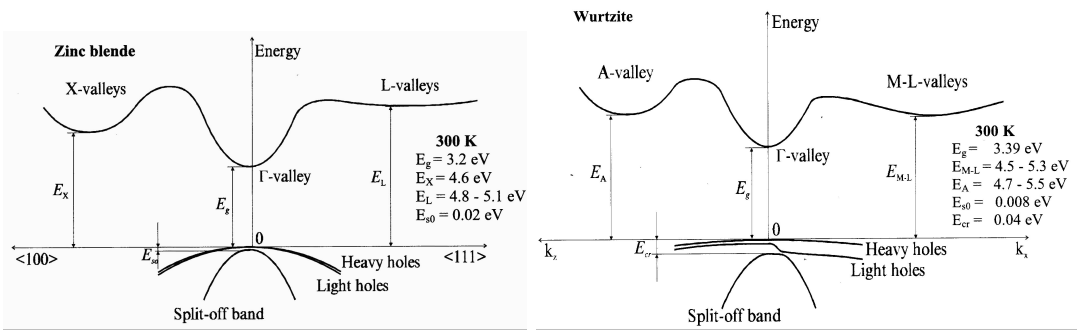

FIGURE 1.4 – GaN cubic Zinc Blende (left) and hexagonal Wurtzite (right) structure and their Brillouin zones.

Hexagonal and cubic structures have a band gap of 3.43 eV and 3.20 eV respectively at 300 K. Those values rise with temperatures, as described in the following equation :

$$E_g = E_0 - \frac{a \cdot T^2}{T + b} \tag{1.6}$$

where E_0 = 3.47 eV, a = 0.599 meV.K^{-1} and b = 880 K. This formula gives us a gap of 3.424 eV for hexagonal GaN at a 300 K temperature. This energy is to be compared to the 4H-SiC value of 3.240 eV and the Si value of 1.103 eV at 300 K obtained through the same calculation. This band gap energy is directly related to the breakdown field, which we will take into account later on. A wide band gap is generally associated to a low intrinsic carrier concentration, but non intentionally doped GaN is always n-type doped and electronic density can vary from 10^{16} to 10^{19} at.cm^{-3} depending on the growing conditions. However those values are not very accurate since defects in the GaN structure will contribute to obtain higher values, while compensation phenomenons, located at deep energy levels, can contribute to the general lowering of these values. Hall measurements allow more precise and reliable way to obtain accurate values for the density and donor activation energy depending on temperature. The activation energy is related to the carrier concentration and given by the following equation :

$$E_a(N_d) = E_a(N_d = 0) - \delta \cdot N_d^{1/3} \tag{1.7}$$

where δ is the shield constant in GaN (2.4x10^{-8} eV.cm^{-1}). For a doping level of 3x10^{17} at.cm^{-3}, we have an activation energy of 17 meV. Beyond 3x10^{18} at.cm^{-3}, activation energy becomes null and electronic density does not decrease with temperature, which corresponds to a metallic behavior (semiconductor beyond the Mott transition).

As stated earlier, another very important characteristic in power electronics is the breakdown electric field since this parameter will directly influence the maxi-

mum bias sustainable by the component. The higher its value, the easier it will be to elaborate devices with high doping levels and reduced size, with the beneficial properties such as a lower on-resistance. The theoretical breakdown field in GaN is compared to the one of other semiconductors in figure 1.5

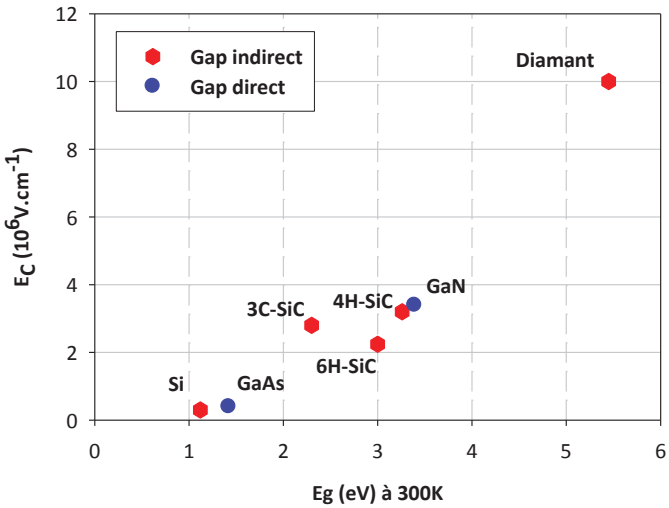

FIGURE 1.5 – Critical breakdown fields for different semiconducting materials with a doping concentration of 10^{16} cm^{-3} depending on their gap (at 300 K)[8]

We can see that large band gap materials have superior breakdown field compared to materials such as silicon or gallium-arsenide. Diamond's critical breakdown field (around 10 MV.cm^{-1} at 300 K) is theoretically a hundred times higher than silicon's, while at 3.4 MV.cm^{-1}, gallium-nitride's is eleven times higher.

As stated previously, breakdown electric field and bang gap energy are tightly related by the following formula :

$$E_C \propto E_g^{3/2} \tag{1.8}$$

According to this relation, we can see that the higher the gap, the higher the theoretical breakdown field will be, as shown on figure 1.5. This also means that the critical field will decrease as temperature rises.

Last but not least of the electric parameters is the electron mobility. Under the influence of an electric field, charge carriers (electrons and holes) will migrate in the material, and the mean free path without interaction will set the movements of those carriers in the crystal. Generally wrote as μ, the mobility will be under the direct influence of any modifications in the lattice, such as those induced by temperature rising or doping. Those dependency can be calculated by the following formula :

$$\mu = \mu_{min}(\frac{T}{300})^{\beta} + \frac{\mu_{max}(\frac{T}{300})^{\alpha} - \mu_{min}(\frac{T}{300})^{\beta}}{1 + (\frac{N_{tot}}{N_{ref}})^{\gamma}} \tag{1.9}$$

where T is the temperature, N the carrier concentration, α, β and γ parameters directly related to the semiconductor considered. Table 1.4 shows those values for GaN.

Carriers	μ_{min} ($cm^2.V^{-1}.s^{-1}$)	μ_{max} ($cm^2.V^{-1}.s^{-1}$)	N_{ref} (cm^{-3})	α	β	γ
Electrons	55	1000	$2x10^{17}$	-2	-3.8	1
Holes	30	170	$3x10^{17}$	-5	-3.7	2

TABLE 1.4 – Minimum and maximum carrier mobility in GaN and associated calculation parameters [8].

If we now look at figure 1.6, we can trace the evolution of the electron and hole mobility for temperature ranging from 150 K to 475 K for different carrier concentration.

The first thing we can notice here is that mobility will decrease inversely proportional to the doping of the semiconductor. For a low concentration, we can also see that temperature has a large impact on mobility. For a carrier density around 10^{16} cm^{-3}, GaN mobility is around 900 $cm^2.V^{-1}.s^{-1}$ at 300 K, which is very similar to the one of 3C-SiC. However, hole mobility is around 170 $cm^2.V^{-1}.s^{-1}$, which is 4 times more important than in 3C-SiC, but also 4 times lower than silicon's.

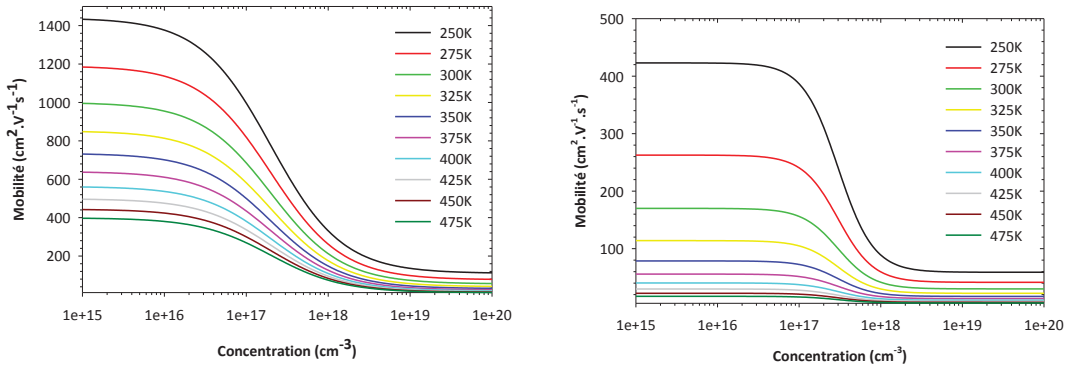

FIGURE 1.6 – Electron (left) and hole (right) mobility depending on carrier concentration as calculated using equation 1.8.

Those values are reported in Table 1.5

Semiconductor	Electron mobility ($cm^2.V^{-1}.s^{-1}$) at 300K	Hole mobility ($cm^2.V^{-1}.s^{-1}$) at 300K
GaN	900	170
3C-SiC	900	40
4H-siC	750	115
Si	1360	600
GaAs	8500	400

TABLE 1.5 – Carrier mobility in semiconductors at 300K.

The main difference between the mobility in GaAs and GaN is related to the difference in the effective mass of the carriers, which is higher in GaN, but this apparent superiority of GaAs over GaN is not valid anymore under a high electric field. In fact, III-V semiconductors band structure is peculiar and under those conditions, the variation of mobility is non-linear and not continuously increasing as is the case in other semiconductors. At 200 kV/cm for GaN, there is an overspeed peak which induces a higher electron velocity. As a consequence, saturation velocity is reached a lot later, which is why GaN can be used at high voltages.

1.2.2.2 Physico-chemical properties

One particular property of the GaN crystal, when growing along the 0001 direction (which is the most common) perpendicular to the c plane, is that it is polarized. And since the structure does not present any inversion center, (0001) and $(000\bar{1})$ directions are not identical. In consequence, those two directions define different types of surface, which are the Ga(0001) face and the N$(000\bar{1})$ face.

Associated to this macroscopic polarization comes a piezoelectric polarization. Though the origin and orientation of both polarizations are identical, the direction of the piezoelectric one changes depending on the strains in the epitaxial layer.

The electric field generated by the global polarity could be problematic for optoelectronic devices since the recombination of carriers in quantum wells will diminish, thus lowering the LEDs efficiency. However for FETs (Field Effect Transistors) and HEMTs (High Electron Mobility Transistors) architectures, the high electric field will be highly beneficial, especially for the formation of a 2D electron gas on which we will come back later on. Regarding fabrication processes, the different nature in the faces will influence the behavior of GaN regarding thermal treatments, cleanings or metal adherence during deposition.

Regarding thermal properties, GaN thermal conductivity is 1.3 $W.K^{-1}.cm^{-1}$ but depends on crystal quality. In a power electronics domain where large heat dissipation is necessary, it represents the capacity of the material to transfer a certain quantity of heat per time constant (1 W = 1 $J.s^{-1}$) and per surface unity under a temperature gradient. Thermal conductivity of GaN is relatively close to the one of silicon (1.5 $W.K^{-1}.cm^{-1}$). It is however 3 times higher than GaAs and sapphire conductivity, but 3 to 4 times lower than SiC depending on the polytype. Ideally, this value has to be as high as possible for power electronics since non dissipated heat will generate a rise in the component temperature, which translates into a lowering of the mobility and thus of the global electric performances of the components.

Another key parameter is the thermal dilatation coefficient which gives an infor-

mation on how the material will dilate or contract depending on the temperature. This is a parameter to keep in mind when choosing the base substrate material for growth during hetero-epitaxy. Table 1.6 gives the thermal values for different semiconductor materials.

	Thermal conductivity ($W.K^{-1}.cm^{-1}$)	Thermal dilatation coefficient ($x10^{-6}$ K^{-1})	
		$\Delta a/a_{300K}$	$\Delta a/a_{900K}$
h-GaN	1.3	5.59	5.11
Si	1.5	2.6	4.2
3C-SiC	4.9	3.8	4.8
GaAs	0.5	5.73	6

TABLE 1.6 – Theoretical values for thermal conductivity and thermal dilatation coefficient in semiconductors [9, 10, 11].

1.2.3 The AlGaN/GaN heterostructure

As stated earlier, one of the major applications in power devices for which GaN is considered among the best materials, is the creation of HEMT structures. Compared to traditional MESFET (Modulation Electron Surface Field Effect Transistor), the HEMT is able to bypass the problem of electron transportation in highly doped environment, which presents many restrictive phenomenons regarding electronic performances, especially for mobility. The main principle behind the high mobility transistor is to create a bidimensional electron gas (2DEG) using an AlGaN/GaN heterojunction, which band diagram is represented in figure 1.7.

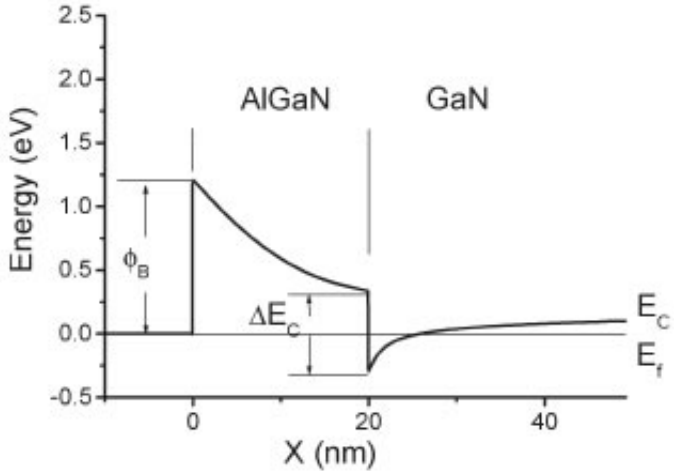

FIGURE 1.7 – Band diagram for the AlGaN/GaN heterostructure, with E_f the Fermi level energy, E_C the conduction band energy and Φ_B the Schottky barrier height. Δ_{EC} is the energy difference between the AlGaN and GaN respective conduction bands [12].

By choosing the right material, we can create a localized potential drop of the conduction band below the Fermi level and confine the carriers in a quantum well. The resulting potential and associated band diagram are thus directly related to the band gap of each semiconductor and their respective doping levels. The electron exchange between the two materials allow Fermi levels alignment and, as in a PN junction, a space charge appears.

The resulting well in GaN is a high electron density region with an excellent mobility, since it is free of any impurity. Electrons can move freely between source and drain along the heterojunction in a bidimensional space. Despite the restrictive aspect of the 2DEG, electron concentration in such structures can achieve very high levels, up to $2x10^{13}$ cm^{-2}. It is important to notice that this value is referenced as a unit of surface and not volume.

The HEMT structure represented in figure 2.2 presents a typical heterojunction between the GaN buffer layer and the AlGaN barrier. In this transistor, gate modulation is achieved by applying negative voltages which allows to deplete more or less the bidimensional channel between the gate and the drain. This kind of operation is referred to as depletion transistor or normally-on.

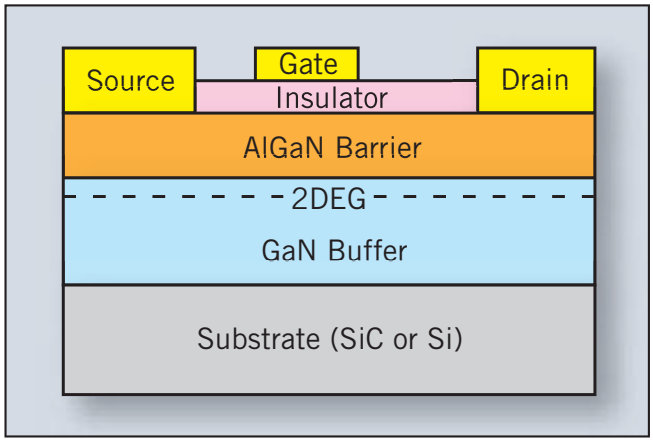

FIGURE 1.8 – Schematics of a typical AlGaN/GaN HEMT with and insulation layer.

1.2.3.1 Spontaneous and piezoelectric polarization

One of the specifications of the HEMT structure based on GaN is that there is no need to dope the barrier layer, in our case AlGaN, in order to obtain a high electron density in the potential well (as opposed to GaAs for example). Electric fields are indeed already present in the AlGaN/GaN heterojunction and they will allow the formation of a high density bidimensional electron gas. Those electric fields are the consequence of 2 types of polarization : spontaneous and piezoelectric polarization.

Spontaneous polarization Without being under the influence of any mechanical constraint, the crystalline structure of GaN presents a spontaneous polariza-

tion. It is the result of the non-superposition of the barycenters of the negative and positive charges in the crystal (electrons and holes respectively). It is also present in AlGaN and generates an electric field around 3 MV/cm.

Piezoelectric polarization The piezoelectric polarization is, as its name indicates, explained by the piezoelectric effect : because of the lattice mismatch between the AlGaN and GaN layers, the resulting mechanical constraint induces and electric field of around 2 MV/cm. This value is influenced by the Al percentage and thus the induced deformation in the crystalline structure. The vectorial sum between both types of polarization in the AlGaN/GaN heterostructure results in the apparition of positive fixed charges at the interface on the AlGaN side, as shown in figure 1.9 :

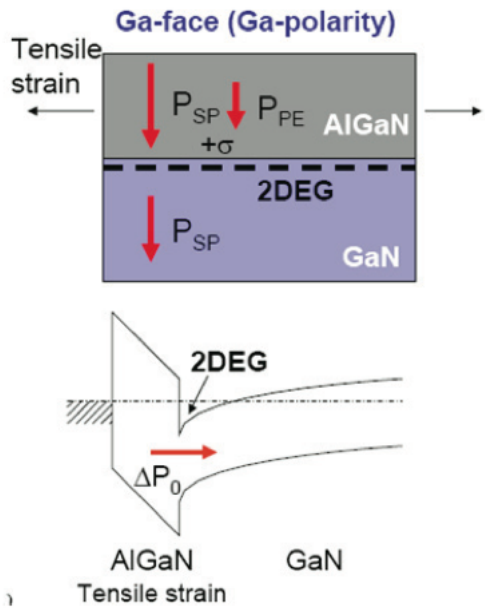

FIGURE 1.9 – AlGaN/GaN structure piezoelectric polarization process

Supposing GaN is not constrained, it is possible to precisely calculate the surfacic charge density that is generated depending of the x in Al_xGa_{1-x} [13] :

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \tag{1.10}$$

$$|\sigma(x)| = |2\frac{a(0) - a(x)}{a(x)}(e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}) + P_{SP}(x) - P_{SP}(0)| \tag{1.11}$$

with : - the lattice constant a(x) = (-0.077x + 3.189)10^{-10} m - elastic constants C_{13}(x) = (5x + 103) GPa and C_{33}(x) = (-32x + 405) GPa - piezoelectric constants e_{13}(x) = (-0.11x - 4.49) C.m^{-2} and e_{33}(x) = (0.73x - 0.73) C.m^{-2} - spontaneous polarization P_{SP}(x) = (-0.052x - 0.029)C.m^{-2}

The electric field resulting from these positive charges will induce the accumulation of compensatory mobile negative charges, the electrons, at the interface on the GaN side. As a consequence, we can deduce that the maximum theoretical electron density in the channel will be limited by the polarization charge density $\sigma(x)$ (assuming all the charges are compensated).

Using non-doped semiconductors combined with the quantum confinement phenomenon will reduce electronic interactions in order to maintain maximum electron mobility in the channel (2000 cm^{-2}/V.s) highly superior to the mobility in doped bulk GaN. There resides all the HEMT interest for microwave applications.

1.2.3.2 Bidimensional electron channel

The 2D electron gas is located in the GaN region of the AlGaN/GaN interface. As stated earlier, it is achieved through the heterojunction between AlGaN and GaN, giving birth to a high surface density of electrons. The density of carriers in the 2DEG is subject to changes depending on the growth conditions, namely the Al content. The best way to increase it is to put more aluminum in the AlGaN

barrier layer. However, beyond 30% of Al, the channel resistance increases significantly due to a diffusion of the alloy or interface roughness. Furthermore, the gate leakage current may increase as well with the Al concentration, which could lead to premature gate breakdown. The introduction of an AlN layer between AlGaN and GaN can counterbalance those effects , but will also generate instabilities at the gate contact level[14]. It has indeed been reported that gate transistor with an AlN layer is unstable through direct polarization after a current stress of 5 mA/mm, whereas AlN free transistors were able to sustain 100 mA/mm without instability [15]. Those perturbations are attributed to a high barrier height sensibility regarding the AlN thickness. A little variation of the AlN thickness may generate high currents locally when a small direct polarization is applied to the gate. The control of the AlN layer is thus capital if we want to achieve reliable structures for power devices.

The creation of an electron channel in the GaN layer is due to the formation of a potential well at the AlGaN/GaN interface. In order to understand his phenomenon, it is necessary to study the band structure at the AlGaN/GaN heterojunction. At the junction of 2 semiconductors, an electron diffusion will take place and, because of the difference in electronic affinity between the 2 materials, the electrons in AlGaN have a larger potential energy than those in GaN. The free electrons in AlGaN will thus spread towards GaN and accumulate at the interface. This diffusion will stop once thermodynamical equilibrium is achieved, that is to say when the Fermi levels of both materials are aligned.

$$E_{FAlGaN} = E_{FGaN} \tag{1.12}$$

As shown in figure 1.10, a discontinuity of the conduction band and the AlGaN/GaN interface appears and provokes the formation of a triangular potential well in GaN because of the band curving, with or without achieving the equilibrium state. Carriers will then accumulate in this well and will be responsible for the conduction phenomenon in the transistor. Since they are confined on a very

small thickness, the electrons will form the so-called 2D electron gas which is the transistor's channel. Under the influence of an electric field, electrons will transit through this channel from the source to the drain of the transistor.

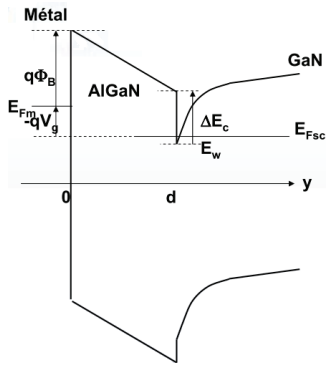

FIGURE 1.10 – AlGaN/GaN heterojunction.

Once the device is realized, the transistor effect will be assured by the Schottky gate contact : by applying a negative voltage on the gate, the space charge region at the metal/semiconductor junction will rise, and beyond a certain value, a diminution of the electrons concentration in the channel will occur. The transistor presents a "Normally-ON" behavior, which means it conducts current when no gate voltage is applied.

The discontinuity in the conduction band represents around 70% of the forbidden gap energy difference between the 2 materials and is directly related to the aluminum content of the AlGaN layer [13].

$$\Delta E_C = 0.7[E_g(x) - E_g(0) \tag{1.13}$$

where :

$$E_g(x) = x \cdot E_g(AlN) + (1-x) \cdot E_g(GaN) - x \cdot (1-x) 1.0 eVs \tag{1.14}$$

$$E_g(x) = x \cdot 6.13 eV + (1-x) \cdot 3.42 eV - x \cdot (1-x) 1.0 eVs \tag{1.15}$$

1.2.4 Models and formation mechanisms

While it is admitted that this electrical compensation phenomenon is at the origin of the 2D electron gas formation, its creation mechanisms are still poorly known, especially when it comes to the origin of the electrons. The most commonly admitted hypothesis is of a high charge density at the AlGaN barrier surface which neutralizes polarization charges and is the source of the electron gas. Multiple studies have been conducted in order to determine the natures of those surface states and different models have been investigated.

First model : single donor level In this particular model, we only consider one state of surface energy E_D below the conduction band [16]. This state is considered as a donor state : electrically neutral when occupied, and positively charged when it has lost its electron. If the level is deep enough, it will be positioned initially under the Fermi level and the 2D gas will be empty : $n_{SURF} = n_S = 0$ (n_S being the surface charge density in the 2DEG). While increasing the barrier thickness, the surface potential will rise due to the constant polarization electric field. Upon reaching a critical thickness t_{CR}, the donor level will reach the Fermi level and electrons will start to migrate from the occupied states of the surface to the empty states in the well in order to create the 2DEG. Upon doing so, the positive surface states will compensate the negative polarization charges at the surface and the electrons in the 2DEG will neutralize the positive charges at the interface. As long as all the surface states are not empty, the surface barrier height remains constant ($E_F = E_D$). This is what is called "Fermi level pinning" and is illustrated in figure 1.11. More electrons will migrate when the AlGaN increases and as such, the global electric field will tend to decrease.

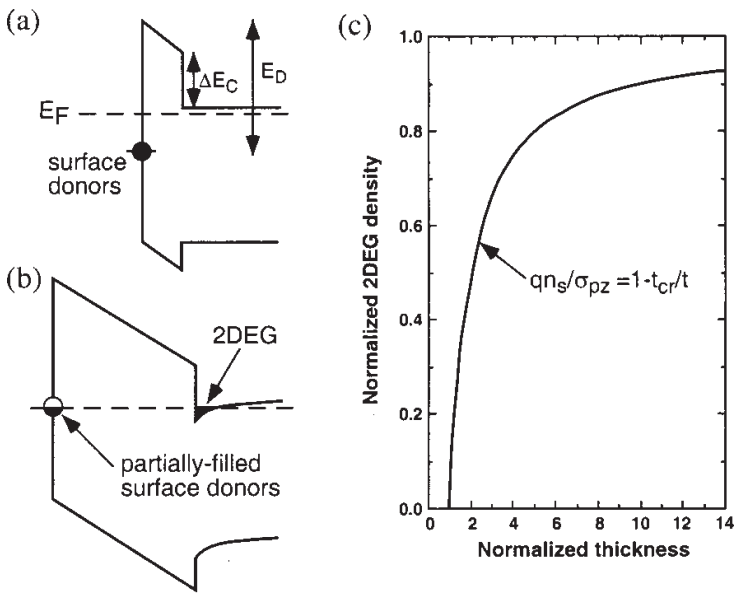

FIGURE 1.11 – Energy diagram of the AlGaN/GaN illustrating the one donor surface level model where the AlGaN thickness is (a) inferior and (b) superior to the critical thickness. (c) is the 2D electron density calculation depending on the AlGaN barrier thickness, for a one donor level model [16].

The Poisson equation allows to calculate the critical thickness t_{CR} :

$$t_{CR} = \frac{(E_D - \Delta E_C) \cdot \epsilon}{q \cdot \sigma} \tag{1.16}$$

where q is the elementary charge and σ the polarization charges.

Supposing every electron coming form the AlGaN surface compensates a polarization charge at the AlGaN/GaN interface, we can deduce the following relation :

$$Q = \sigma - n_S \tag{1.17}$$

with Q the polarization charges which are not compensated by the electrons contributing to the electric field.

But since the electric field is directly related to the sum of the electric charges at the interface, we can precisely calculate the electron density of the 2DEG de-

pending on the AlGaN electric field and the layer's thickness :

$$n_S = \frac{\sigma}{q} - \frac{\epsilon}{dq^2}(E_D + E_F - \Delta E_C) \tag{1.18}$$

where d is the AlGaN barrier thickness and E_F the Fermi energy given by [13] :

$$E_F = E_0 + \frac{\pi h^2}{m^*} n_S \tag{1.19}$$

where E_0 is the energy of the first level formed in the quantum well between the 2 semiconductors :

$$E_0 = (\frac{9\pi h q^2}{8\epsilon_0\sqrt{8m^*}}\frac{n_s}{\epsilon})^{2/3} \tag{1.20}$$

If we neglect the rise of the Fermi level in the channel, the 2DEG becomes :

$$qn_S = \sigma(1 - \frac{t_{CR}}{t}) \tag{1.21}$$

As we can see in figure 1.12, the density measurements done by Hall effect (black dots) tend to confirm the theory for low thicknesses. We can see the apparition of the 2DEG at 35 Å which allows us to estimate the surface donor energy at E_D = 1.65 eV. The fall of the n_S after 150Å can presuppose a relaxation of the constraints in AlGaN for superior thicknesses.

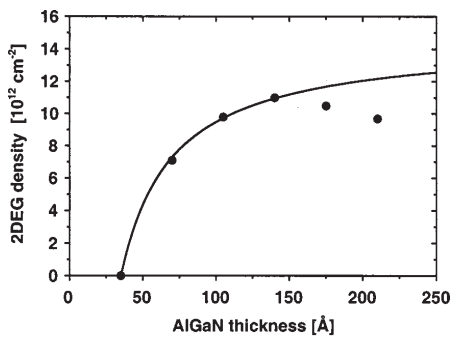

FIGURE 1.12 – Room temperature 2DEG density measured by Hall effect as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness [16].

Theoretically, there is a saturation of the 2D electron gas density for important AlGaN thicknesses. The electric field at the interface will tend to decrease as long as the thickness increases, and will become null when all the polarization charges are neutralized. This explains the asymptotic behavior.

Second model : donor state distribution at the surface Even if the previous model works well, it has been contradicted by multiple studies [17, 18], particularly regarding the surface barrier height at the AlGaN barrier. The published results that we can see in figure 1.13 indeed showed that the surface barrier height decreases when the AlGaN thickness rises, which is incompatible with the one donor state model.

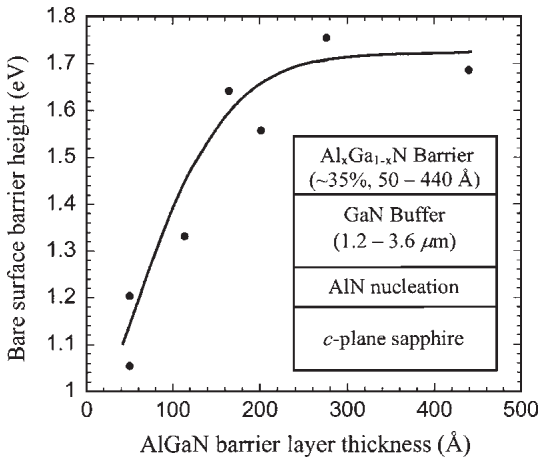

FIGURE 1.13 – Variation of the AlGaN surface barrier height depending on the AlGaN layer thickness [18]

.

Starting from this observation, we can assume that the surface states are distributed in the material gap. We thus consider a critical barrier height Φ_C (potential between the conduction band and the highest occupied surface state) and a constant surface states density n_0. Upon increasing the barrier thickness and if n_0 is low enough, the barrier height at the surface will necessarily increase in order to allow the transition of more electrons to the 2DEG. All the surface states which

height is inferior to the barrier's Φ_S will as such contribute to the formation of the 2DEG by losing their electron, as shown in figure 1.14 and the following equation :

$$n_{SURF} = n_S = n_0(\Phi_S - \Phi_C) \tag{1.22}$$

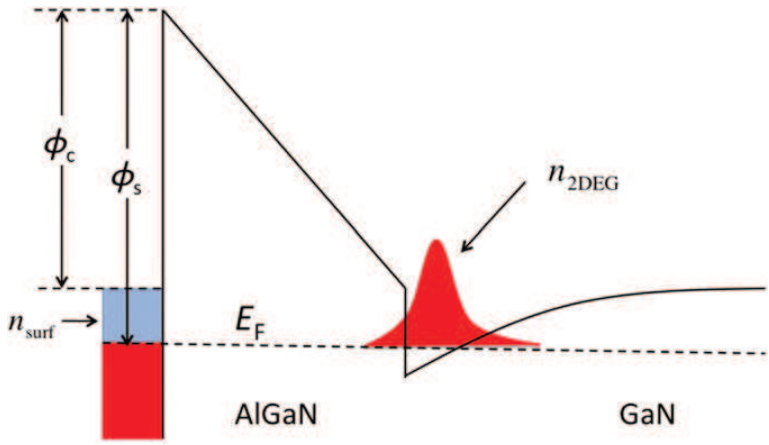

FIGURE 1.14 – Energy for the AlGaN/GaN heterostructure illustrating the electron transfer between the surface states and the 2DEG at the AlGaN/GaN interface [19].

This model is very close to the previous one, except that the barrier height Φ_S is modified with the AlGaN thickness. The formula for the electron density in the 2DEG is similar, but the donor state energy E_D is replaced by the surface potential Φ_S, giving the following equation :

$$n_S = \frac{\sigma}{q} - \frac{\epsilon}{da^2}(\Phi_S + E_F - \Delta E_C) \tag{1.23}$$

The variations of Φ_S in function of the thickness d are directly related to the states density n_0 : the lower n_0 is, the more important the variations of Φ_S will be. If the states density of surface donors is high enough, the electrons transfer from the surface to the 2DEG will only have a slight influence on the Fermi level. As

such, we are in the same configuration as in the first model with only one donor state, assuming the hypothesis that $E_D = q\Phi_C$ and that the surface states density is infinite.

However, multiple studies have shown noticeable differences regarding n_0, Φ_C and $\Delta\Phi$ (barrier height elevation) of the measured donor states at the surface, as can be seen in table 1.7. Those variations can be attributed to the different experience conditions, particularly if we take AlGaN oxides into account. Different studies [20, 21] have shown that oxidation has an influence on the surface properties. Depending on the type of reconstruction with the oxygen atoms, the state density as well as the energy levels of the highest occupied state are modified, and this will have a direct influence on the formation of the 2D electron gas.

Source	n_0 ($cm^{-2}.eV^{-1}$)	Φ_C (eV)	$\Delta\Phi$ (eV)
Ibbeston et al.[16]	∞	1.65	0
Koley et al.[18]	1.6 x10^{13}	1.0	0.8
Higashiwaki et al.[20]	4 - 6 x 10^{12}	1.0	1.5
Gordon et al.[19]	$<10^{13}$	1.0	1.3

TABLE 1.7 – Parameters differences between different studies

1.3 Context of Ph.D.

As stated at the beginning of this work, the demand regarding power devices is in a large expansion and is expected to expand even further in the years to come. Compared to the silicon industry, gallium-nitride technology is still at its beginning and what we know so far about it is probably just the tip of the iceberg. However, in an energy driven economical context, the HEMT structure represents a very promising solution for achieving high power and frequency switching devices. But even though theory predicts high performances for AlGaN/GaN heterostructures, we are still very dependent on material quality and process steps. As stated earlier, GaN epitaxy is complicated, and there are still a lot of problems preventing us for

achieving performances as high as we would like. Whether it be defects, doping or device architecture challenges, every step in the elaboration process brings its fair share of difficulties, and each one of them must be addressed separately.

This works takes place in the context of the creation of GaN on silicon industry oriented device processing chain in the LC2E laboratory. Using the already present CMOS industry equipment of the CEA-Leti, the objective here is to achieve high performance devices for power applications with cost reduction through the use of large diameter 200 mm silicon substrates.

In terms of device technology and considering its maturity on silicon, the Schottky gate structure has been studied intensively and already yielded some good results. However, for it to be reliable, a very good control of the different creation processes is necessary. Even though it has proven to be a very robust structure, it still presents some defects, particularly in terms of gate leakage current, and its performances are very sensitive to material quality. The natural way to reduce this hindrance would be, as in the silicon industry, to turn to the use of an intermediate insulating layer between the gate and the material to achieve MOS-like devices.

This is precisely where this work will be integrated. From the choice of the insulator to its electrical testing, going through deposition, characterization, pre- or post-processing and material conditioning, it was my work as a Ph.D student in CEA-Leti to address the different challenges in order to create a reliable MIS-HEMT device (MIS standing for Metal Insulator Semiconductor). Most of the research was carried on wafers produced at CEA-Leti, but also on some samples coming from the III-V Lab in Paris.

The main objective in the elaboration of a MIS-HEMT during my work was to address one of the major problematic in power device elaboration, which is to suppress or at least greatly reduce the gate-leakage current. As the continuous down-scaling of the device size has lead to very thin gate oxides, the leakage current that can flow from the channel to the gate comes into the order of the subthreshold

leakage current and the gate cannot be considered as an ideally insulated electrode anymore. This affects the circuit functionality and increases the standby power consumption due to the static gate current. Another key aspect directly following, is to elaborate a sufficiently robust and optimal process in order to better achieve a normally-off device. Ultimately, and mainly for safety reasons, it is preferable to apply a positive gate bias in order to open the device channel, instead of applying a negative bias in order to close it.

While introducing a gate dielectric is a very good solution towards solving the above mentioned problems, it also comes with its limitations and constraints typically found in CMOS structures in general. As we will see in the next chapter, we also have to take into account the potential barrier height of the dielectric and the critical electric field.

1.4 Conclusion

In this first chapter, we first analyzed what are the present and future demands regarding the market for power devices and their applications. That led to the conclusion that silicon has now reached its limits in order for it to stay competitive in those domains of applications and the necessity to switch to large band gap materials.

As such, we have seen that gallium nitride has a place of choice among such materials and enunciated the different properties, showings its particular place in the microelectronics industry. Among the two different forms, we have seen that the hexagonal structure presents many advantages over the cubic one. The different advantages of the use of GaN over conventional semiconductors for power and high frequency switching applications were then exposed, and the AlGaN/GaN heterostructure was introduced. This showed the particularly interesting 2DEG generation for the elaboration of HEMT devices.

We introduced after that the different existing possibilities for the creation

of GaN. Even if great progress has been made in recent years, it still appears that it is too complex and expensive to produce bulk GaN, but hetero-epitaxy through MOCVD on silicon is making great progress, allowing the creation of large diameter GaN production chain at high quality levels, despite the still large quantity of defects generated.

Lastly, a brief introduction of this Ph.D. subject was enunciated in order to emphasize the importance of GaN and its properties in the elaboration of MIS-HEMT structures.

2

The Metal Insulator Semiconductor structure on GaN

2.1 Presentation of the structure

2.1.1 Principle of operation

The first structures using two dimension electron gas appeared in 1980 and were created by Thomson-CSF [22] and Fujitsu [23] under the form of MESFETs (MEtal Semiconductor Field Effect Transistor) which used doped gallium arsenide GaAs. These simple structures were later on replaced by HEMT in the mid 90s [24], using AlGaAs/GaAs and AlGaAs/InGaAs heterostructures. Due to the presence

of the two dimensional electron gas at the AlGaN/GaN interface, these structure have also been labelled as TEGFETs (Two dimensional Electron Gas Field Effect Transistors).

As presented in the first chapter, the AlGaN/GaN heterostructure is the solution envisioned in order to realize reliable power devices on GaN. In order to take maximum advantage of the high mobility of the electrons and the high electric field, one of the first studied architecture for HEMT devices is the Schottky gate transistor.

Having a long history of development on silicon architectures, it has been well adapted to fit high power demands over the years. Figure 2.1 shows a typical Schottky gate structure for an AlGaN/GaN HEMT.

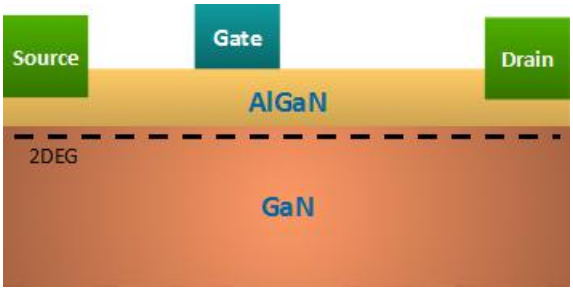

FIGURE 2.1 – Schematics of a Schottky gate transistor on an AlGaN/GaN heterostructure

As seen in chapter 1, the AlGaN layer's gap is more important than the one of GaN (the difference is even more important with higher Al concentration)[25]. The gate is metallic and is the element making a Schottky contact with the semiconductor. Once a high polarization is applied, the gate will deplete the electron channel locally, making the AlGaN layer an insulator. The electrons coming from the donors are then transferred to the non intentionally doped GaN, which will increase their density at the AlGaN/GaN interface (heterojunction) : this is what is called the channel and is only a few nanometers thick. In this region, electron mobility is very high, because of the lack of donor ions in non intentionally doped GaN. The behavior of these carriers inside potential wells can be described through

the use of quantum mechanics (Schrödinger-Poisson equations) which we will not detail here. The source and drain are metallic contacts and constitute what are called the ohmic contacts.

One important characteristic to point out is that those transistors function in a normally-on state. This means that the device is naturally in a conducting "on" state where the carriers can flow freely. In order to deplete the channel, it is thus necessary to apply a negative bias on the gate.

One of the major challenge to date is the finality of achieving normally-off devices. It is obvious that for security reasons, we need the power component to be in the off state when no bias is applied to the gate. Taking this into consideration, the MIS (Metal Insulator Semiconductor) structure represents a viable possibility because it allows positive gate bias without gate current injection, and reduces the gate leakage currents to a minimum whether it be in the open or closed state. The principle of the structure is to add an insulator layer between the metallic gate and the AlGaN barrier, as shown in figure 2.2.

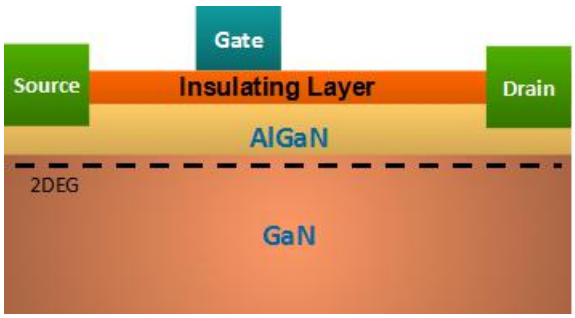

FIGURE 2.2 – Schematics of a HEMT with insulated gate transistor on an AlGaN/GaN heterostructure

2.1.2 The metal-semiconductor junction

2.1.2.1 Full depletion approximation

The simple analytic model of the metal-semiconductor junction is based on the full depletion approximation. This approximation is obtained by assuming that

the semiconductor is fully depleted over a distance x_d, called the depletion region. While this assumption does not provide an accurate charge distribution, it does provide very reasonable approximate expressions for the electric field and potential throughout the semiconductor.

2.1.2.2 Full depletion analysis

We now apply the full depletion approximation to an M-S (metal-semiconductor) junction containing an n-type semiconductor. We define the depletion region to be between the metal-semiconductor interface (x = 0) and the edge of the depletion region (x = x_d). The depletion layer width, x_d, is unknown at this point but will later be expressed as a function of the applied voltage.

To find the depletion layer width, we start with the charge density in the semiconductor and calculate the electric field and the potential across the semiconductor as a function of the depletion layer width. We then solve for the depletion layer width by requiring the potential across the semiconductor to equal the difference between the built-in potential and the applied voltage, Φ_i - V_a. The different steps of the analysis are illustrated by figure 2.3 :

As the semiconductor is depleted of mobile carriers within the depletion region, the charge density in that region is due to the ionized donors. Outside the depletion region, the semiconductor is assumed neutral. This yields the following expressions for the charge density,ρ :

$$\begin{aligned} \rho(x) &= qN_d \qquad 0 < x < x_d \\ \rho(x) &= 0 \qquad\quad x \leq x_d \end{aligned} \tag{2.1}$$

where we assumed full ionization so that the ionized donor density equals the donor density per volume unit, N_d. This charge density is shown in figure 2.3 (a). The charge in the semiconductor is exactly balanced by the charge in the metal, Q_M, so that no electric field exists except around the metal-semiconductor interface.

Using Gauss's law we obtain the electric field as a function of position :

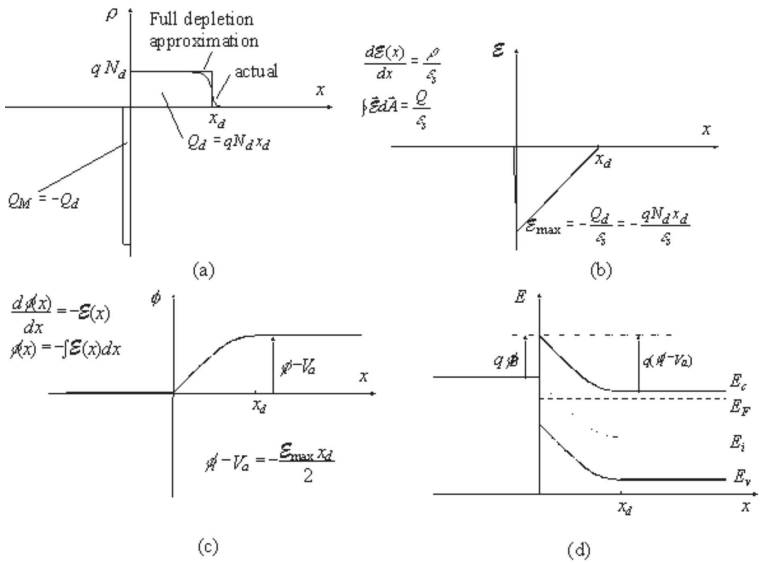

FIGURE 2.3 – (a) Charge density, (b) electric field, (c) potential and (d) energy as obtained with the full depletion analysis.

$$\begin{aligned} E(x) &= -\tfrac{qN_d}{\varepsilon_s}(x_d - x) \qquad && 0 < x < x_d \\ E(c) &= 0 && x \leq x_d \end{aligned} \tag{2.2}$$

where ε_s is the dielectric constant of the semiconductor. We also assumed that the electric field is zero outside the depletion region, since a non-zero field would cause the mobile carriers to redistribute until there is no field. The depletion region does not contain mobile carriers so that there can be an electric field. The largest (absolute) value of the electric field is obtained at the interface and is given by :

$$E(x) = -\frac{qN_d x_d}{\varepsilon_s} = -\frac{Q_d}{\varepsilon_s} \tag{2.3}$$

where the electric field was also related to the total charge (per unit area), Q_d, in the depletion layer. Since the electric field is minus the gradient of the potential, one

obtains the potential by integrating the expression for the electric field, yielding :

$$\begin{aligned} \phi(x) &= 0 & x \leq 0 \\ \phi(x) &= \frac{qN_d}{2\varepsilon_s}[x_d^2 - (x_d - x)^2] & 0 < x < x_d \\ \phi(x) &= \frac{qN_d x_d^2}{2\varepsilon_s} & x_d \leq x \end{aligned} \tag{2.4}$$

We now assume that the potential across the metal can be neglected. Since the density of free carriers is very high in a metal, the thickness of the charge layer in the metal is very thin. Therefore, the potential across the metal is several orders of magnitude smaller than that across the semiconductor, even though the total amount of charge is the same in both regions.

The total potential difference across the semiconductor equals the built-in potential, Φ_i, in thermal equilibrium and is further reduced/increased by the applied voltage when a positive/negative voltage is applied to the metal as described by equation :

$$\phi(x = \infty) - \phi(x = 0) = \phi_i - V_a \tag{2.5}$$

This boundary condition provides the following relation between the semiconductor potential at the surface, the applied voltage and the depletion layer width :

$$\phi_i - V_a = -\phi(x = 0) = \frac{qN_d x_d^2}{2\varepsilon_s} \tag{2.6}$$

Solving this expression for the depletion layer width, x_d, yields :

$$x_d = \sqrt{\frac{2\varepsilon_s(\phi_i - V_a)}{qN_d}} \tag{2.7}$$

In addition, we can obtain the capacitance as a function of the applied voltage

by taking the derivative of the charge with respect to the applied voltage yielding :

$$C_j = \mid \frac{dQ_d}{dV_a} \mid = \sqrt{\frac{q\varepsilon_s N_d}{2(\phi_i - V_a)}} = \frac{\varepsilon_s}{x_d} \tag{2.8}$$

The last term in the equation indicates that the expression of a parallel plate capacitor still applies. This can be explained by the fact that the charge added/removed from the depletion layer as one decreases/increases the applied voltage is added/removed only at the edge of the depletion region. While the parallel plate capacitor expression seems to imply that the capacitance is constant, the metal-semiconductor junction capacitance is not constant since the depletion layer width, x_d, varies with the applied voltage.

In order to obtain the expression from the threshold voltage V_{th} in a metal-semiconductor junction, we just need to transform equation 2.6 in :

$$\phi_i - V_{th} = \frac{qN_d d^2}{2\varepsilon_s} \tag{2.9}$$

with $x_d = d$, which is the full depletion depth. From this we then extract the following expression for V_{th} :

$$V_{th} = \phi_i - \frac{qN_d d^2}{2\varepsilon_s} \tag{2.10}$$

2.1.3 HEMT and MIS-HEMT threshold voltage

HEMT : In order to evaluate the threshold voltage of an HEMT structure, we add a lower gap semiconductor to the previous model, resulting in the formation of the 2D electron gas. We will henceforward call the higher gap semiconductor the barrier. This is illustrated in figure 2.4.

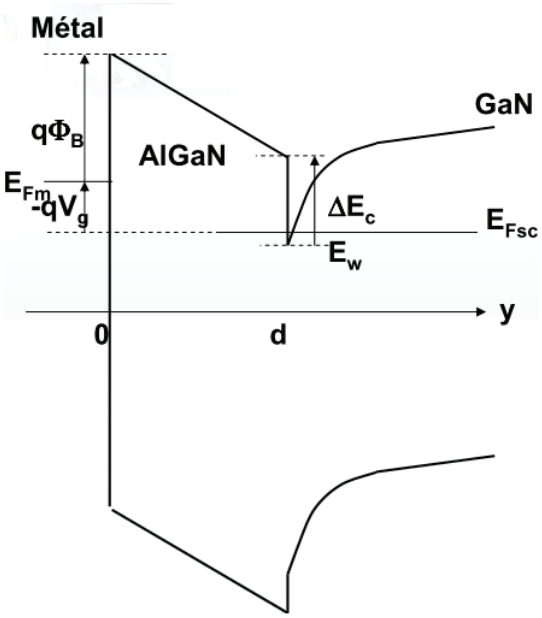

FIGURE 2.4 – Band Diagram of the AlGaN/GaN heterojunction.

In order to adapt equation 2.6 to the HEMT band structure, we must adjust the different contributions coming from adding another semiconductor and the formation of the 2DEG. As such we will obtain :

$$\Phi_B - V_{th} = \frac{qN_d d^2}{2\varepsilon_s} + \frac{\Delta E_c}{q} + 2DEG\,contribution \tag{2.11}$$

where ΔE_C is the conduction band offset between the two semiconductors and Φ_B the Schottky barrier height.

Regarding the 2DEG contribution, it can be evaluated fairly simply. Assuming the electron gas can be assimilated to a plane capacitance, we have the basic relation :

$$Q = C \cdot U \Rightarrow U = \frac{Q}{C} \tag{2.12}$$

where Q is the charge, C the capacitance and U the voltage. Assuming that the formation of the 2DEG is directly at the two semiconductors interface, the charge and the capacitance can be expressed as :

$$\begin{aligned} Q &= qn_sS \\ C &= \frac{\varepsilon_s S}{t_b} \end{aligned} \tag{2.13}$$

where n_s is the surface charge density in the 2DEG, S the surface of the capacitance and t_b the barrier thickness. As such we can now express 2.12 as :

$$U = \frac{qn_st_b}{\varepsilon_s} \tag{2.14}$$

By replacing the 2DEG contribution into equation 2.11 by U, we obtain :

$$V_{th} = \Phi_B - \frac{\Delta E_c}{q} - \frac{qN_dd^2}{2\varepsilon_s} - \frac{qn_st_b}{\varepsilon_s} \tag{2.15}$$

MIS-HEMT : Now that we have the threshold voltage expression for the HEMT, we only need to include the insulation layer in our band diagram and again look at the different contributions. For the practicality of the notation, we will consider the case of an oxide as insulating layer. Figure 2.5 illustrates our typical MIS-HEMT band diagram.

Taking that in to account, we have to modify the 2DEG contribution, due to the introduction of the oxide. Again taking the place capacitance model at the interfaces, we now have :

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox/b}} + \frac{1}{C_{b/s}} \tag{2.16}$$

where $C_{ox/b}$ and $C_{b/s}$ are the oxide/barrier capacitance and the barrier/semiconductor capacitance respectively. As such, we have :

$$\frac{1}{C_{tot}} = \frac{t_{ox}}{\varepsilon_{ox}S} + \frac{t_b}{\varepsilon_bS} \tag{2.17}$$

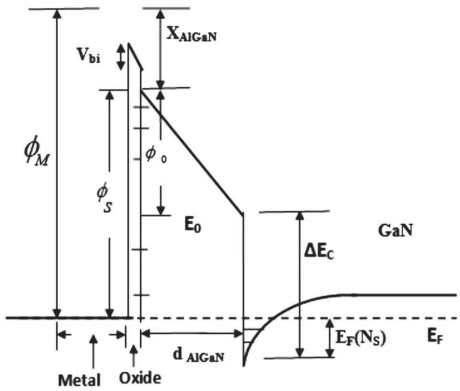

FIGURE 2.5 – Conduction band profile for a metal/oxide/AlGaN/GaN interface [26].

where t_{ox} and ε_{ox} are the oxide thickness and dielectric constant, while t_b and ε_b are the barrier thickness and dielectric constant respectively. The 2DEG contribution U finally becomes :

$$U = \frac{Q}{C_{tot}} = (\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_b})qn_s t_b \tag{2.18}$$

By replacing those terms in the threshold voltage equation, we obtain :

$$V_{th} = \Phi_B - \frac{\Delta E_c}{q} - \frac{q\overline{n_{ox}}t_{ox}^2}{2\varepsilon_{ox}} - (\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_b})qn_s t_b \tag{2.19}$$

with $\overline{n_{ox}}$ the average oxide bulk charge per volume unit.

If we want to take into account the induced charges at the oxide/semiconductor interface, we must add another term which has the same expression as the 2DEG contribution. The threshold voltage then becomes :

$$V_{th} = \Phi_B - \frac{\Delta E_c}{q} - \frac{q\overline{n_{ox}}t_{ox}^2}{2\varepsilon_{ox}} - (\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_b})qn_s t_b - \frac{qn_{ox}t_{ox}}{\varepsilon_{ox}} \tag{2.20}$$

where n_{ox} is the surface charge density at the oxide/semiconductor interface. This influence can be attributed to the different interface states that will be created upon introducing the insulating layer in the structure, whether they are traps generated at the interface or charges due to the nature of deposited dielectric.

In this equation, we can clearly see the role that the insulating layer will play in the threshold voltage of the component based on its deposited thickness, its dielectric constant and its average oxide bulk charge per volume unit. Considering these parameters, we can predict the V_{th} shift that will be induced depending on what high-κ dielectric was deposited and its thickness.

2.2 Dielectrics on GaN and AlGaN

For the last fifty years, the miniaturization of MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) was successfully accomplished (Moore's law) through the use of very thin oxides of only a few nanometers. Following this need to miniaturize and the coming of new materials with higher mobility, there was a necessity in the last decade to move to the use of high permittivity dielectrics like HfO_2 and Al_2O_3. While SiO_2 remained the leader in MOS and MEMS technologies, the necessity to build structures with high permittivity dielectrics became primordial for miniaturization in the VLSI (Very Large Scale Industry). Complementary Metal Oxide Semiconductor (CMOS) field effect transistors on silicon still heavily rely on its oxide, thermal SiO_2, which is a very good gate dielectric but becomes leaky under a certain deposited thickness. As such, high-κ dielectrics use became a new standard, as they offered the same electrostatic control with constant capacitance and suppressed the gate leakage current that occurs for thin SiO_2 layers.

In III-V materials, the use of native oxides is very limited due to their poor quality which tends to inhibit the inherent properties of the material itself. However, with great progress made in deposition techniques, Atomic Layer Deposition (ALD) in particular, these problems are being resolved. Those techniques can now address the requirements for passivation on GaN and AlGaN, which necessitates the suppression of the dangling bonds at the material surface in order to reduce the interface states between the insulator and GaN or AlGaN layer.

2.2.1 MIS on GaN and AlGaN

Regarding the use of high-κ dielectrics on GaN and AlGaN, they must match very strict characteristics such as chemical and thermal stability, low mobile and trapped charge density, low defect density in order to enhance the breakdown, a higher permittivity than the one of the semiconductor in order to lower the electric field in the dielectric and a large difference in band gap energy in order to reduce leakage currents. Furthermore, the choice of a gate dielectric for a MIS-FET or MIS-HEMT requires that the oxide does not react with the semiconductor, and that the band offsets of the insulator on the semiconductor do exceed 1 eV, so that it may act as a sufficient insulator [27]. And last but not least, the interface between the dielectric and the semiconductor must show a low state density. Table 2.1 presents GaN, AlN and $Al_{0.25}Ga_{0.75}N$ properties in comparison to different dielectrics.

Regarding the values for $Al_{0.25}Ga_{0.75}N$, they were calculated taking into account that its conduction band is at 25% of the difference between the AlN and GaN one, which corresponds to 0.65 eV. This value was then subtracted from the conduction band offset of the different materials relatively to GaN.

If we look back to equation 2.20 and take into account the values in table 2.1, we can see that the choice of the dielectric is crucial in order to control the threshold voltage of the device. For every material correspond a specific conduction band offset, dielectric constant and charges in the dielectric itself, as well as interface states that will be associated. Depending on the surface properties prior to the high-κ dielectric deposition, traps or charges can be generated at the insulator semi-conductor interface, which can greatly influence the electrical behavior of the structure. Most of those interface states are generally associated to surface contamination, and can be suppressed through the use of the appropriate treatment for surface conditionning before insulator deposition.

Material	GaN	AlN	SiO_2	Si_3N_4	HfO_2	Al_2O_3
Band gap (eV)	3.2	6.2	9	5.3	6.0	8.8
Electronic affinity (eV)	3.3	0.6	0.9	2.1	2.4	1
Dielectric constant ε_r	9.7	9.1	3.9	7	25	9
Optical dielectric constant ε_∞	6.0	4.8	2.25	3.8	4	3.12
Conduction band offset relatively to GaN	-	2.58	2.6	1.3	1.09	2.16
Conduction band offset relatively to AlN	-2.58	-	-0.1	-1.3	-1.5	-0.5
Conduction band offset relatively to $Al_{0.25}Ga_{0.75}N$	0.65	-1.93	1.95	0.65	0.44	2.47

TABLE 2.1 – Electrical properties of GaN and different insulating dielectrics [27].

Regarding aluminum oxide Al_2O_3, it is probably one of the most suited material for the realization of MIS-HEMT devices. As one of AlGaN natural two oxides, the use of Al_2O_3 as gate insulator will produce a very clean and controlled Al_2O_3/AlGaN interface, which will result in an efficient neutralization of the dangling bonds at the AlGaN surface, assuming that contamination prior to deposition is very low. Furthermore, alumina's dielectric constant being relatively high, it will also allow a higher deposition thickness, without influencing the threshold voltage too much, as demonstrated in equation 2.20. It is also a very well-known material in the semiconductor industry, and deposition techniques have improved a lot, whether it is through the use of thermal oxidation of aluminum, Plasma Enhanced Chemical Vapor Deposition (PECVD) or atomic layer deposition (ALD). However, as stated earlier, due to the necessity to passivate the dangling bonds, ALD

is preferable to PECVD as it is a softer deposition method. The latter being quite aggressive, it could provoke surface damage, which would increase the interfaces states instead of reducing them.

One of the major drawbacks of alumina is its relative weakness to high temperature, which will make it crystallize and loose its insulating properties, making it very leaky. As such, it can often only be used in gate-last fabrication processes, since the ohmic contact rapid thermal annealing is generally around 900 °C. Another problem is that it remains weak to high electric fields. As a consequence, it will deteriorate in a destructive way once the breakdown voltage of the device is reached, making it useless for further utilization. To amend for this, ohmic contacts and gate structures have been improved by using field plates, in order to redistribute electric field lines in the device and prevent the destruction of the oxide.

2.2.2 Surface contamination and interface states density

In order to realize MIS devices, there are a few prerequisites regarding surface conditioning and preparation before the deposition of the insulating layer. Due to various conditions, the AlGaN surface can be contaminated after epitaxy. The two major contaminants at the surface are carbon and oxygen. This contamination can come either from the reactor chamber during the growth process, or during processing due to air exposure.

As stated earlier, the native oxides of AlGaN are of very poor quality. Consequently, they cannot be used in order to realize a MIS structure like it would be done with thermal SiO_2 on silicon. The two major oxides formed are gallium oxide Ga_2O_3 and Al_2O_3. Thermodynamically speaking, the formation of alumina is more favorable than gallium oxide (référence), so we found it in greater quantities proportionally speaking.

Regarding carbon, it comes either from the ethyl or methyl containing precursor gases, or from organic contamination as on other semiconductor materials. Howe-

ver, during my Ph.D., due to the fact that lift-off technique was used for metallic deposition, organic resist was used for all the different lithographic steps, as well as a protection when cutting 200mm wafers into smaller samples. The resists which were used are composed of mostly carbon polymers, and even stripping processes and solvent cleaning left large amounts of carbon all over the AlGaN surface. This can be seen in figure 2.6 images where we can see a typical AlGaN surface after a lithography step.

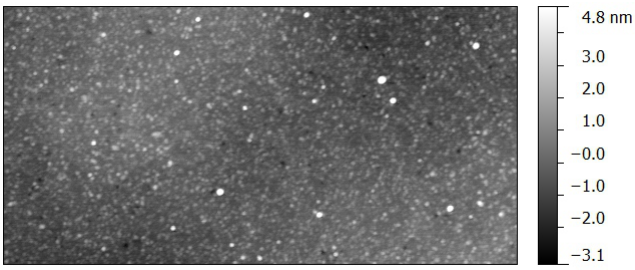

FIGURE 2.6 – Typical AlGaN surface after resin stripping.

In order to get rid of those contaminants, there exist different possibilities. The first one would be to grow an SiN layer in the epitaxy reactor chamber in order to prevent oxidation and organic contamination of the AlGaN surface. It would however require etching steps afterwards in order to realize the ohmic contact or the high-κ deposition.

Another method to remove native oxides is through chemical treatments. It has been proven that HCl- or NH_4OH-containing solutions can be effective in order to remove surface oxidation. Standard Chemical 1 and 2, referred to as SC1 and SC2, are standard microelectronics treatments composed of water and peroxide to which is added ammonia and chloride for SC1 and SC2 respectively. However, AlGaN native oxide bonds are relatively strong, so those chemical treatments must often be carried at high temperature (between 50 and 70°C) in order for them to be efficient.

Regarding carbon contamination, most chemical treatments have proven in-

effective, but a low energy oxygen or nitrogen plasma can be a viable solutions. However, regarding O_2 plasma, it can further increase the oxygen contamination of the surface, as well as induce nitrogen vacancies, thus creating non-desirable effects. The latter could for example lead to the formation of surface traps, which would hinder the electrical properties of the device.

2.3 Gate recess etching

As said earlier, in order to implement the integration of GaN power components in complete circuits, it is necessary to achieve a normally-off functioning state (enhancement mode) instead of normally-on (depletion mode). The big challenge today is to achieve that without deteriorating the properties and performances obtained on normally-on transistors.

The easiest solution to achieve that is to use the formation properties of the 2D electron gas in function of the AlGaN barrier thickness. Under a certain thickness of AlGaN, the electron density becomes too low for the channel to conduct current anymore, and a positive bias has to be applied in order for the transistor to be closed. This is due to the fact that surface potential diminishes with AlGaN thickness, so that a portion of the donnors states located under the Fermi level will not provide electrons to the 2DEG anymore.

Taking that into account, different transistors were made using a barrier of only a few nanometers [28], but the on resistance R_{ON} of such structures becomes too large, greatly hindering the properties of the transistors. In order to compensate for such phenomenon, the depletion zone is restrained to the part under the gate by doing a gate recess etching.

2.3.1 Principle

The principle is to reduce by etching the AlGaN layer thickness only under the gate, which allows to keep a high density of carriers everywhere else in the transistor.

Figure 2.7 a typical ICP-RIE chamber.

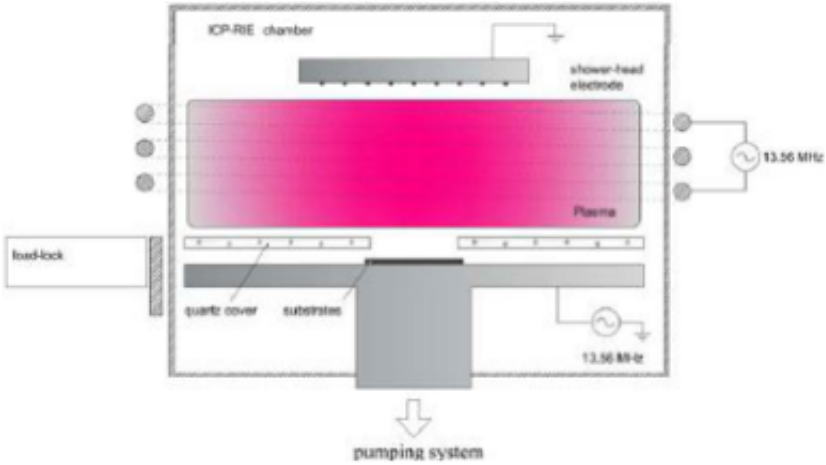

FIGURE 2.7 – Schematics of a typical ICP-RIE process chamber

This will allow to achieve a normally-off state while maintaining a relatively low R_{ON} since only the resistance of the etched zone will increase.

However, if the principle appears pretty simple, the recess must be carried with absolute control over the etching rate because of the extreme sensitivity of the electron density relatively to the barrier thickness. Since it is a physical process, perturbations, such as roughness increase and surface damaging, must be taken into account since they can potentially deteriorate the mobility in the channel.

2.3.2 Threshold voltage increase

Since the threshold voltage of normally-on devices is negative, there is a need in such an architecture for the threshold voltage to be as high as possible. One of the way to increase it is to use gate recess etching as well. By reducing the AlGaN barrier thickness, the 2DEG density is reduced and can be estimated by using the following relation :

$$N_{2DR} = N_{2D}(1 - \frac{t_{CR}}{t_{RA}}) \tag{2.21}$$

where t_{RA} is the remaining AlGaN thickness under the gate and t_{CR} the critical thickness under which the 2DEG vanishes. If we express that in terms of band diagram, we can see from figure 2.8 that the threshold voltage has a linear behavior regarding the AlGaN remaining thickness, if N_D is neglected. According that the Schottky barrier height Φ_B is constant, we thus have the following relation :

$$qV_{th} = \Phi_B - \Delta E_C - \frac{qN_{2D}t_{RA}}{\varepsilon} \tag{2.22}$$

where ε is the AlGaN dielectric constant [29].

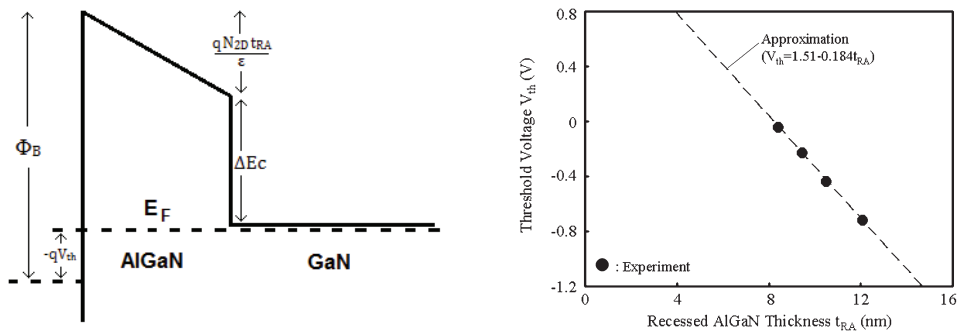

FIGURE 2.8 – Band diagram of a normally-off AlGaN/GaN heterostructure at the threshold voltage (left) and V_{th} evolution depending on the AlGaN thickness (right) [29].

However, we can see that the variation of the threshold voltage V_{th} with the gate recess is limited. Furthermore, such an etching and the reduction of the AlGaN barrier exposes the transistor to important current losses, which will reduce the I_{on} over I_{off} ratio.

2.4 Conclusion

Throughout this chapter, we have seen that a large array of parameters can be held responsible for how a MIS-HEMT on an AlGaN/GaN heterostructures will behave. Furthermore, if we were to compare it to its counterpart on silicon, the

intrinsic properties of such an heterostructure have to be taken into account. As such, the presence of spontaneous charges, under the form of the 2DEG, will play a major role in the transistor properties. This tends to complicate a lot the device realization as every step in the creation process can have a drastic influence on the 2DEG and its behavior. Furthermore, it is greatly dependent on the quality of the base material, since as seen in chapter I, lots of dislocations tend to appear during the epitaxy process, and variability from one wafer to another can be quite high depending on the growth conditions.

In the context of my Ph.D., it has been chosen to only focus on one aspect of the device realization, namely the insulating step of the transistor using a gate dielectric. As such, this study will only focus on the influences this technological step will have on the realized devices.

First and foremost will be to evaluate the dielectric layer's influence on the gate leakage current. As the main objective of the MIS structure is precisely to reduce leakage to a minimum, drain current measurements depending on the gate voltage are the choice analysis as they will allow us to measure both drain and gate currents simultaneously. The aim will be to extract the I_{on} over I_{off} ratio, as well as the subthreshold slope which indicates the quality of the transition from the off to the on state.

The second aspect of the study will be the threshold voltage V_{th} and its evolution. As seen throughout this entire chapter, it is one of the parameter on which all the choices made regarding the insulating layer will have a direct effect. Indeed, its shift is directly correlated to the choice of the selected material, as well as the deposited thickness. In order to assess that, capacitance measurements appear to be the go-to solution to measure the thickness influence, as both are directly related through equation 2.17. Drain current measurement will also play a major role in the extraction of V_{th} as will be seen in chapter IV.

Finally, equation 2.20 indicates that the introduction of a dielectric layer in the structure shifts the threshold voltage towards the negative bias, further in-

creasing the normally-on state of the transistor. However, as was explained earlier, a normally-off state is much more preferable, mainly for security reason. Due to the availability of the appropriate equipment, and although it was not originally a part of the study, the influence of gate recess etching was studied in this Ph.D. Both capacitance and current measurement will be helping in verifying equation 2.22 and eventually lead to a normally-off transistor through the implementation of a full recess etching of the AlGaN barrier.

3

Device realization

3.1 Origin and characteristics of the material

There were three large diameters wafers from which I elaborated my samples. The first one was provided by the III-V Lab and was named TS088. I then worked on wafers produced by CEA-Leti named 081 and AA865P. All those wafers were grown following a similar epitaxy structure, from a Silicon substrate. The buffer layers are composed of $Al_xGa_{1-x}N$, x varying from 1 to 0 in multiple states, so that it starts with an AlN layer and ends with a thick GaN layer. Figure 3.1, represents a TEM (transmission electron microscope) image of a typical stacking for wafers that were used during this Ph.D.

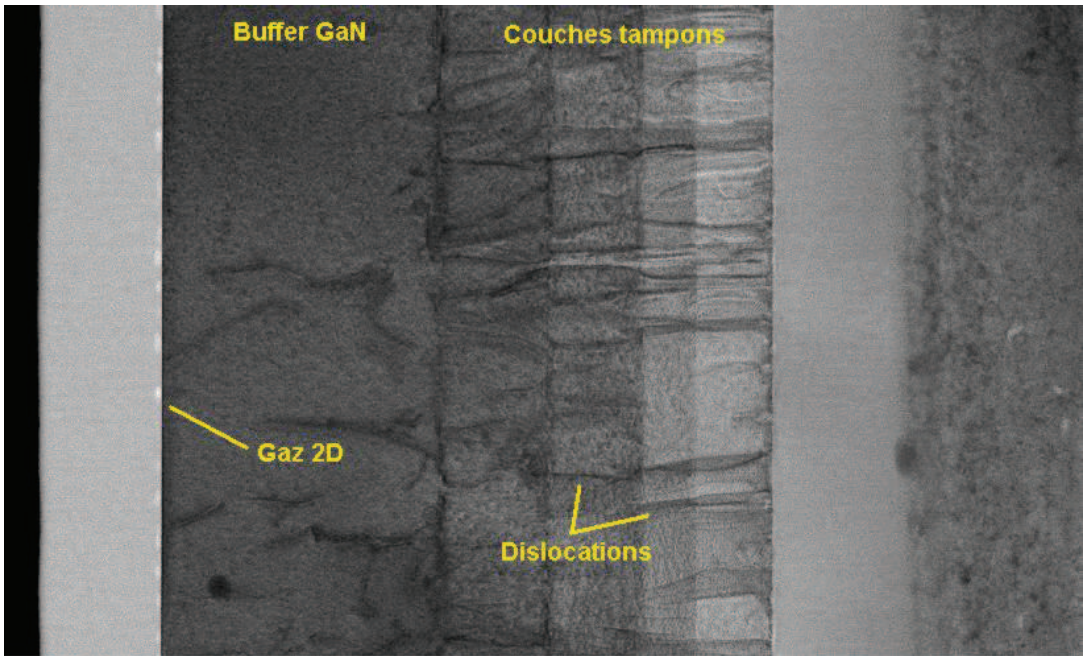

FIGURE 3.1 – TEM image for a typical AlGaN/GaN heterostructure epitaxied at CEA-Leti

As we can see, there are some apparent dislocations inside the GaN layers. As stated in the first chapter, those defects are always present on hetero-epitaxy layers such as the ones that were grown at CEA-Leti or III-V Lab. They will have an influence on the GaN layer resistivity, as well as the vertical and lateral breakdown voltage.

All those wafers were first coated with resist and then sliced in square samples of 3 cm by 3 cm. This was necessary in order to acquire multiple samples and for the practical reason that there is no equipment that can accept 200 mm diameter wafers in the Plateforme de Technologies Amont (PTA), which is a small clean room in CEA-Leti. It is important to keep in mind that different wafers with different epitaxy were used throughout this Ph.D. As such, since the exact properties of the samples were not known, the ensuing results obtained were difficult

to interpret due to the induced variability.

3.2 Surface conditioning

In order to achieve the best performances, it is crucial to understand the different mechanisms occurring at the interface between the high-κ dielectric and the AlGaN. While all those different interactions are not yet fully understood, previous papers already stated that the oxidation as well as the carbon contamination on the surface may induce the presence of surface traps, which in turn have a drastic influence on RF dispersion as well as breakdown voltage, decreasing the overall efficiency of the devices [30]. In this context, surface treatments are interesting to reduce to its minimum the surface contamination before the device processing, thus eliminating the poor native oxide and reducing the electron traps that might hinder electronic properties. Nitrogen deficiency and stoichiometry disorder at the AlGaN surface can also be induced through device processing, inducing localized deep donor levels which a have strong negative impact on overall performances [31].

3.2.1 Chemical treatments

Some reports have already shown that chemical treatments represent a good solution in order to suppress the poor native oxide at the AlGaN surface [32, 33]. In order to be as exhaustive as possible, we decided to evaluate chemical treatments which are already used in the microelectronics industry [34]. The treatments we evaluated were HCl, NH_4OH, SC1 (NH_4OH + H_2O_2) and SC2 (HCl + H_2O_2) at different temperatures and concentrations. All these different treatments were realized at the Plateforme de Technologies Amont.

For the HCl, a 1 :1 HCl :H_2O solution was used and a 2 minutes dip was carried on 3 samples at 20°C, 40°C and 60°C, with a reference sample rinsed only with acetone and IPA.

For the SC1 and SC2, a 1 :1 :5 NH_4OH :H_2O_2 :H_2O and a 1 :1 :5 HCl :H_2O_2 :H_2O solutions were used respectively, with again a 2 minutes dip at 20°C, 40°C and 60°C with a prior low power O_2 plasma exposure of 2 minutes. In this case, the reference sample was only rinsed with acetone and IPA with the same 2 minutes O_2 plasma exposure.

For the NH_4OH treatments, 3 solutions were prepared at 15, 10 and 8.5% concentration, and 10 minutes dip were carried out for each one of them at 20°C, 45°C and 75°C with a 10 minutes O_2 plasma treatment before the cleansing. The reference sample was again rinsed only with acetone and IPA and exposed to the same 10 minutes low power O_2 plasma for 10 minutes.

3.2.2 Plasma treatments

Apart from chemical treatments, it has been stated that a nitride-based plasma pre-treatment prior to surface passivation or high-κ deposition could improve the device performances [35, 36, 37, 38].

Regarding the N-containing plasma treatments, a first batch of 4 samples was treated with decoupled forming gas plasma (N_2 with 3 % of H_2) during 2 minutes on a Fusion Gemini 200MCU/ES. The four different conditions for the samples were the following : 150°C at 500 W, 150°C at 1500 W, 300°C at 500 W and finally 300°C at 1500 W. The major drawback of this technique is its ex-situ characteristic, meaning the sample has to undergo a transfer between the plasma treatment and dielectric deposition, thus subjecting it to potential air contamination.

As for the N_2 and NH_2 in-situ 50W plasma treatments, 2 samples were treated during 30 seconds and another 2 for 2 minutes for each kind of plasma. They were performed as an in-situ procedureon on an ASM Polygon ALD platform, which presents the advantage of being able to perform a plasma treatment just before an eventual high-κ dielectric deposition.

All these different treatments were carried out on the silicon platform with the help of the process ingeneers.

After each kind of treatment, we analyzed the samples in an XPS (X-Ray Photo- electron Spectroscopy) chamber, making sure to transfer the samples as fast as possible in order to limit the re-contamination of the surface. The HCl-, NH_4OH-, SC1- and SC2- treated samples were analyzed in a Thermo Electron Theta 300 spectrometer. The other samples were analyzed in an S-Probe Spectrometer (SSI) with a monochromated AlKα radiation and a 0.8 eV energy resolution.

3.3 MIS-HEMT and capacitance fabrication

In this section, I will focus on explaining the different steps that were performed in order to process the devices that were then used to characterize the quality of the MIS structures. Out of the different available ones on the mask, mostly two structures were taken into consideration : a 400 μm diameter diode and a 1 mm width circular transistor with a 100 μm gate length. Figure 3.2 shows the layout of the mask that was used throughout the Ph.D. work. It was opted to use a ohmic contact and gate last procedure for different technical reasons that will be explained later on.

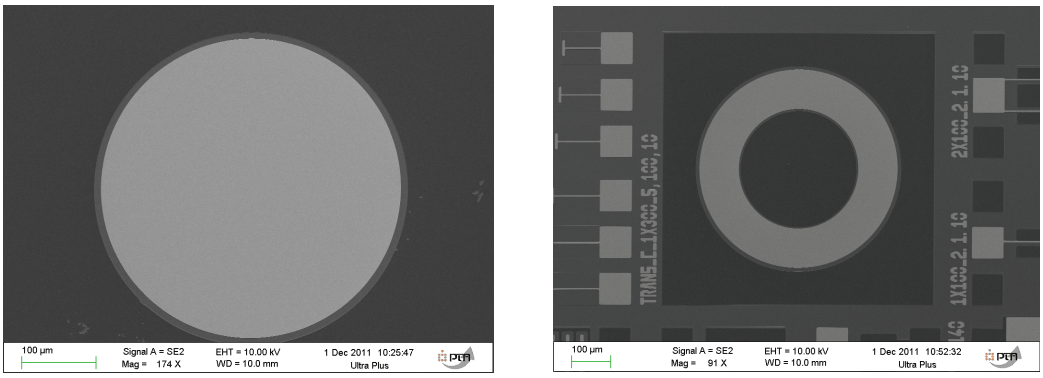

FIGURE 3.2 – SEM image of the diode (left) and circular transistor (right) layout as they were used to perform electrical measurements.

3.3.1 Process flow

Before detailing each process step that were put in place for this Ph.D., it is important to have a global view and approach regarding the device realization. As such, a process flow was put into place as described in figure 3.3. Those four different steps were at the heart of my Ph.D. as they were the cornerstones which, if done in the cleanest possible way, would ensure the best possible performances of my devices.

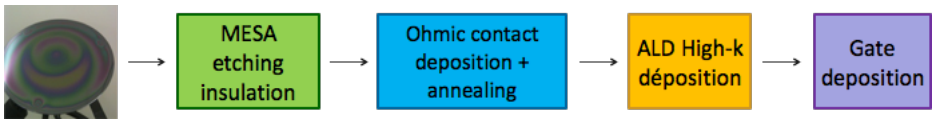

FIGURE 3.3 – Simplified process flow from the wafer to the finished device

Between each step of the process flow, a photolithography step was performed in order to "draw" each of the patterns out. The first step is to clean the sample with acetone in ultrasounds for five minutes, which is then rinsed with isopropanol, dried with N_2 and then heated for ten minutes at 180°C. Resist is then spin-coated on top of the sample and heated in order to remove the residual solvent. After that comes insulation with ultra-violet (UV) light through a glass mask on which chrome patterns are drawn. As in traditional photography, the insulated sample is then placed in a developer which, depending on the polarity of the resist, will take away the exposed pattern or the non-exposed pattern for positive and negative resist respectively. For each type of resist corresponds a particular spin-coating velocity, heating, exposure time, UV type (normal or deep UV), developer and developing time.

Apart from the MESA, alignment of the lithography is crucial in every step of the process flow in order to prevent the different patterns from overlapping. As the entire process is composed of four major steps, four masks were used, the last three needing a precise alignment. On each mask, the same cell composed of different devices is repeated multiple times, so that one 3x3cm sample contains roughly 20

cells.

3.3.2 Encountered difficulties and adopted solutions

All those steps were carried at the PTA or at the CIME (Centre Interuniversitaire de MicroElectronique et Nanotechnologies) in CEA-Leti, and different difficulties were encountered.

The first one came from the fact that I was working on small samples and not on full wafers. This greatly limited my access to the industry compatible process in clean room 41 equipment, since it necessitated the use of a holder. This was generally a source of problems considering the fact that most samples had followed at on time or another a process step in PTA, which made it risky in terms of contamination. PTA being a small clean room used for developing proof of concepts predominantly, the contamination restrictions are almost nonexistent and cross contamination can occur very easily, especially from noble materials. Before the arrival of a dedicated ALD at CIME, it was thus problematic for me to get access to dielectric deposition.

The second problem came form the ohmic contact annealing. Since the oven at CIME is not very well sealed, a lot of oxygen would seep into the chamber, thus degrading drastically the contact resistance. The majority of annealing resulted in a Schottky contact behavior. For the same reasons of contamination, it was also impossible to get access to industry compatible ovens. The samples had thus to be shipped by mail to the III-V Lab.

Fairly rapidly, it was also noted that the resist we first used, the AZ1512, was not appropriate for the lift-off technique since it would expand the patterns dimensions after developing. This could eventually lead to the gate patterns overlapping the ohmic contact ones, ruining the whole device. As a solution, it was decided to use a bi-stack resist consisting of LOR10A and AZ5214, which is schematized in figure 3.4. This would ensure the nice development on even the smaller patterns, but would require the use of NEP (N-Ethylpyrrolidone) solvent heated at 60°C for

half an hour and a thorough rinsing afterwards.

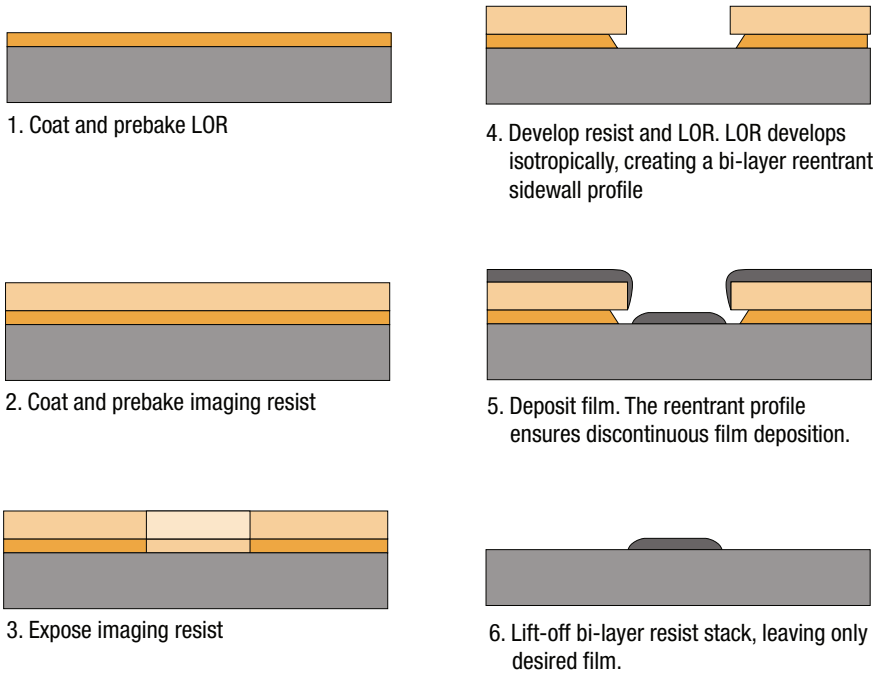

FIGURE 3.4 – Schematics of the steps involved in the LOR 10A lithography process

The major problem however was regarding gate lithography. The developer used for this step is very basic, and would remove the Al_2O_3. As a consequence it was decided to first cover the alumina with a 30 nm layer of chrome, and then go on with the lithography. Doing so prevented the developer from removing the dielectric. After the 200 nm Au depositions, the lift-off would reveal the pattern, and gold played the role of a hard mask in order to remover the excessive chrome with a chromium-etch solution. This solution is particularly convenient due to the fact that the etching rate of chromium-etch is very precise and well known, at 100 nm per minute. Considering this, a 18 seconds etch was enough to exactly remove the 30 nm of chromium, without risking over etching under the gold patterns.

3.3.3 MESA etching insulation

In order to realize the different devices that were used in this Ph.D., the very first step in the creation of an insulating pattern which will separate the different cells of the mask from each other. This will prevent any interference that might occur from one pattern to an other and is called the MESA.

After this first level of photolithoghraphy, the sample was deeply etched in order to totally cut through the AlGaN barrier and into the GaN buffer, thus suppressing the 2DEG where the resist is not present. The resist is then removed and the sample cleaned, and coated in resist again in order to proceed to the ohmic contact level. This etching was carried through a chloride etch by engineers at the silicon platform.

3.3.4 Metallization and ohmic contact

The second step in the process was to perform ohmic contact. In the microelectronics industry, gold has been forbidden for different reasons, principally due to the fact that it is highly contaminating. Indeed, traces of gold can be found in an equipment after a gold-containing wafer was processed in the aforementioned equipment, thus generating potentially devastating cross-contamination if multiple steps are carried through multiple machines. As such, gold has been banned in many processes, even though it has great electrical and conducting properties.

In the GaN industry, the alternative to gold that was chosen is the titanium-aluminum Ti/Al contact. Both metals have the advantage of not inducing any known cross-contamination, and their deposition is fairly easy and well established on semiconductor materials. Once both metals are deposited, they are then annealed, generally at temperature around 900°C, thus forming in the optimal case a $TiAl_3$ alloy as well as TiN at the Ti/AlGaN interface.

The typical ohmic contact stack deposited during my Ph.D was a 95/200 nm Ti/Al ohmic contact deposited by evaporation at the PTA in CEA-Leti on a

Plassys evaporator, with a one minute argon etching prior to deposition. The evaporator itself is composed of a deposition chamber, an argon beam for light plasma etching and eight rotating crucibles in order to deposit up to eight different materials. The evaporation is made under high vacuum through the heating and sublimation of the desired material with an ion beam.

Once this is done, the sample is then put into a solvent for the lift-off step, where all the remaining resist is dissolved, taking off the excess metal and revealing the metallic pattern.

Regarding the annealing process, all my samples were sent and annealed at III-V Lab at 900°C with a 600°C pre-annealing step, always under the same conditions. This was to ensure the ohmic nature of the contact and ensure reproductibility on the différent samples.

3.3.5 High-κ dielectric deposition and in-situ N_2 plasma treatment

As stated earlier, the high-κ dielectric deposition was made through Atomic Layer Deposition (ALD). Since Al_2O_3 was the selected material to be deposited in order to realize MIS structures, two deposition techniques were used. The first one, referred to as thermal ALD, uses Tri Methyl Aluminum (TMA) as a precursor, and water pulses as oxidizer. The second one is Plasma Enhanced ALD (PEALD), which uses 30 seconds oxygen plasma cycles instead of water pulses for the oxidation step. The alumina was deposited full sheet, just after ohmic contact annealing. It thus performed the role of gate dielectric as well as passivation layer. Figure 3.5 represents a typical Al_2O_3 growth cycle for thermal ALD. The CIME equipment presented the possibility to grow alumina through both ALD techniques.

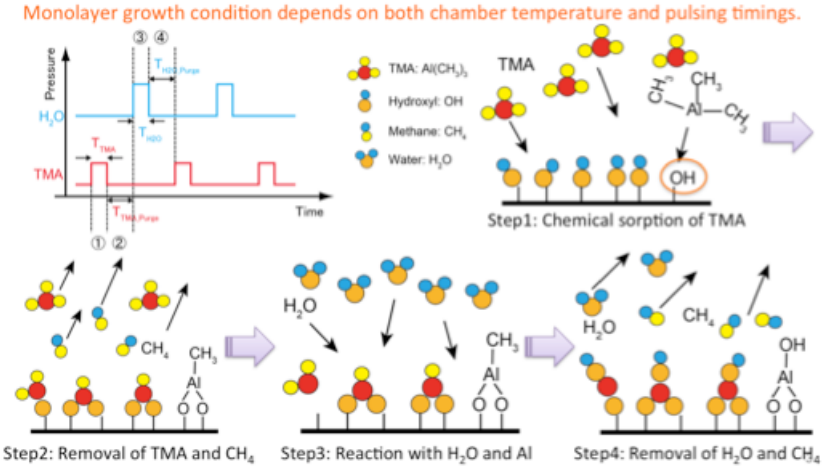

FIGURE 3.5 – Al_2O_3 growth through ALD using TMA precursor and water pulses for oxidation

For some of the samples, it was also in the ALD chamber that in-situ nitrogen plasma was carried, just before high-κ dielectric deposition. The only accessible parameter I had access to in order to change the influence of the plasma was the power. Bias information was unfortunately not available. Since it is a deported plasma in a relatively large reactor, it remains difficult to estimate the exact energy of the plasma that was hitting the surface.

All the different processes were carried at 250°C inside the reactor chamber. It was chosen to deposit the gate dielectric after the ohmic contact because of the annealing for the later. Being at 900°C, alumina would crystallize very rapidly, thus losing its insulating properties and making it very leaky (référence faible qualité AL2O3 crystalisé).

3.3.6 Gate metal deposition

Similarly to the ohmic contact, the gate metals were deposited in the same Plassys evaporator with the lithography/lift-off technique. For the MIS structures, the chosen materials were chrome and gold in as 30/200 nm Cr/Au stack. Since the adopted creation process was a gate last process, where gate metal deposition is the

last step, gold was chosen here because of commodity. In an industry environment, it could be easily replaced by another non contaminating material.

Regarding the fabrication of Schottky gate structure, Ni/Pt/Au was used since, as we will see in the results in chapter 4, Cr/Au gates led to very leaky behavior and non coherent results in C(V) measurements. This is probably due to chrome diffusion in AlGaN (essayer de trouver une référence).

3.4 Optional process : recess etching below gate

Recess etching was carried in the ICP-RIE Oxford available at the PTA using BCl_3 as plasma for the ICP. Before any etching, there was a thorough preconditioning of the chamber in order to ensure that the AlGaN surface was etched as uniformly as possible. Since BCl_3 is the gas that was used, the pre-conditioning consisted in a cleaning of the chamber with an O_2 plasma directly followed by a BCl_3 etching, with only a silicon wafer in the reactor chamber. Another BCl_3 etching was then carried through with a resist coated silicon wafer with the final etch process conditions. After all this, the samples were then placed inside the chamber with the same resist coated wafer as carrier, the resist playing the role of protection agent. The etching speed was measured by Nicolas Herbecq during his internship in LC2E, and was estimated to be 7 nm per second. Table3.1 reports the different processes that were tested by Nicolas during his internship.

Plasma	Flux (sccm)	ICP Power (W)	Depth (nm)	Speed (nm/min)
BCl_3	50	700	28	14
BCl_3	10	700	24	12
BCl_3	50	200	13	6.5
BCl_3	10	200	11	5.5
Cl_2	10	700	70	35
Cl_2	10	200	65	32.5

TABLE 3.1 – Influence of gas, flux, ICP power on etching depth and speed on AlGaN

This etching was done at two different times during the device processing. First before ohmic contact deposition, in order to bring the latter closer to the 2DEG and thus lower the contact resistance. Second time was before the high-κ dielectric deposition with the gate pattern defined with resist through photolithography. The resist was removed afterwards, followed by a complete solvent cleansing before the gate-dielectric deposition.

3.5 Conclusion

As we have seen in this chapter, the entire process is rather simple in appearance. It also presented the huge advantage that all of the different steps were achievable inside the PTA or CIME, without having to use the silicon platform. However, behind its apparent simplicity, the entirety had to be made in the most minute way since a simple mistake often meant losing the sample and having to do redo the entire process from scratch. Furthermore, Al_2O_3 being sensitive to the developer that was used for the lithography step, it took quite some effort and ingenuity to come up with the solution of using a chrome protective layer. It complicated the entire process a bit, adding the necessity to remove the chromium partially with a chromium-etch solution.

Another major difficulty was the mask alignment during lithography. Since all had to be done by hand, it necessitated a good knowledge of the different levels of alignment and oftentimes quite some skill. Indeed, binoculars were sometimes slightly tilted due to other users manipulations, thus compromising the alignment even when things appeared to be aligned. Also, resist was sometimes non uniformly coated on a square sample, tilting slightly the sample when sticking it to the mask. Many a wrong alignment occurred thus forcing me to redo the entire lithography step, which proved very time consuming.

Last but not least, since CEA is comprised of many Ph.D. students and researchers, availability of the different machines was often scarce. This was especially true for the electric measurements equipment, which were often fully booked weeks in advance.

However, despite all these inconveniences, very good samples were made. The entire process also proved quite robust, despite the apparent simplicity and the rather limited control I had. PTA being a small clean room, where the thoroughness of the different users was very variable, it was still possible to perform brilliantly as will be shown in the next chapter. Availability of the PTA and CIME personnel proved also invaluable and greatly contributed to achieving very good results.

4

Results and discussions

4.1 Surface treatments and their characterization

The first results we will discuss are the ones regarding pre-treatments and the characterization of their effect using X-ray photoelectron spectroscopy (XPS). As stated in the previous chapter, chemical and plasma treatments were performed on samples in order to evaluate their influence on surface contamination.

4.1.1 X-Ray Photo-electron Spectroscopy

4.1.1.1 Principle

The method that was used to characterize the AlGaN surface during my Ph.D. was X-Ray Photoelectron Spectrometry (XPS). It is a surface-sensitive quantitative spectroscopic technique that measures the elemental composition at the parts per thousand range, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the top 0 to 10nm of the material being analyzed. XPS requires high vacuum (P $\sim 10^{-8}$ millibar) or ultra-high vacuum (UHV ; P $< 10^{-9}$ millibar) conditions, although a current area of development is ambient-pressure XPS, in which samples are analyzed at pressures of a few tens of millibar.

X-Ray Photo-electron Spectroscopy is a surface chemical analysis technique that can be used to analyze the surface chemistry of a material in its as-received state, or after some treatment, for example : fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some or all of the surface contamination (with mild ion etching) or to intentionally expose deeper layers of the sample (with more extensive ion etching) in depth-profiling XPS, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light. XPS is routinely used to analyze inorganic compounds, metal alloys, semiconductors, polymers, elements, catalysts, glasses, ceramics, paints, papers, inks, woods, plant parts, make-up, teeth, bones, medical implants, bio-materials, viscous oils, glues, ion-modified materials and many others. As such, it is particularly well suited to analyze surface contamination.

XPS can be performed using a commercially built XPS system, a privately built XPS system, or a synchrotron-based light source combined with a custom-designed electron energy analyzer. Commercial XPS instruments in the year 2005 used ei-

ther a focused 20- to 500-micrometer-diameter beam of monochromatic aluminum Kα X-rays, or a broad 10- to 30-mm-diameter beam of non-monochromatic (polychromatic) aluminum Kα X-rays or magnesium Kα X-rays. Because the energy of an X-ray depending of its particular wavelength is known (for aluminum Kα X-rays, $E_{\text{photon}} = 1486.7$ eV), and because the emitted electrons' kinetic energies are measured, the electron binding energy of each of the emitted electrons can be determined by using an equation that is based on the work of Ernest Rutherford (1914) :

$$E_{\text{binding}} = E_{\text{photon}} - (E_{\text{kinetic}} + \phi) \tag{4.1}$$

where E_{binding} is the binding energy (BE) of the electron, E_{photon} is the energy of the X-ray photons being used, E_{kinetic} is the kinetic energy of the electron as measured by the instrument and ϕ is the work function of the spectrometer (not the material). This equation is essentially a conservation of energy equation. The work function term ϕ is an adjustable instrumental correction factor that accounts for the few eV of kinetic energy given up by the photoelectron as it becomes absorbed by the instrument's detector. It is a constant that rarely needs to be adjusted in practice. Figure 4.1 illustrates a typical setup for an XPS analysis.

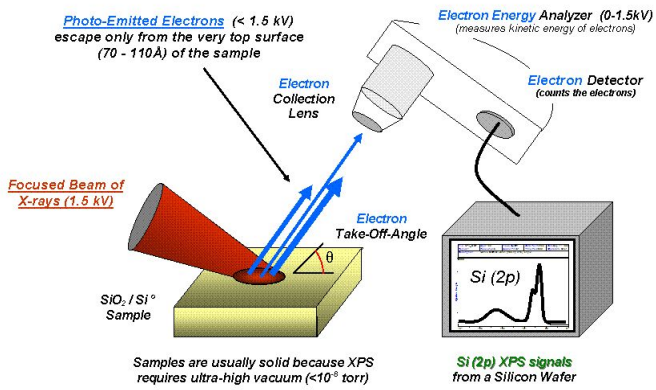

FIGURE 4.1 – X-Ray Photoelectron Spectroscopy Principle

A typical XPS spectrum is a plot of the number of electrons detected (some-

times per unit time) (Y-axis, ordinate) versus the binding energy of the electrons detected (X-axis, abscissa) as shown in figure 4.2. Each element produces a characteristic set of XPS peaks at characteristic binding energy values that directly identify each element that exists in or on the surface of the material being analyzed. These characteristic spectral peaks correspond to the electron configuration of the electrons within the atoms, e.g., 1s, 2s, 2p, 3s, etc. The number of detected electrons in each of the characteristic peaks is directly related to the amount of element within the XPS sampling volume. To generate atomic percentage values, each raw XPS signal must be corrected by dividing its signal intensity (number of electrons detected) by a "relative sensitivity factor" (RSF), and normalized over all of the elements detected. Since hydrogen is not detected, these atomic percentages exclude hydrogen.

To count the number of electrons during the acquisition of a spectrum with a minimum of error, XPS detectors must be operated under ultra-high vacuum (UHV) conditions because electron counting detectors in XPS instruments are typically one meter away from the material irradiated with X-rays. This long path length for detection requires such low pressures. XPS detects only the electrons that have actually escaped from the sample into the vacuum of the instrument, and reach the detector. In order to escape from the sample into vacuum, a photoelectron must travel through the sample and across the upper layer of contamination. Photo-emitted electrons can undergo inelastic collisions, recombination, excitation of the sample, recapture or trapping in various excited states within the material, all of which can reduce the number of escaping photoelectrons. These effects appear as an exponential attenuation function as the depth increases. Figure 4.2 represents a survey analysis spectrum for the AlGaN surface where all the elements are scanned and then identified by their peaks.

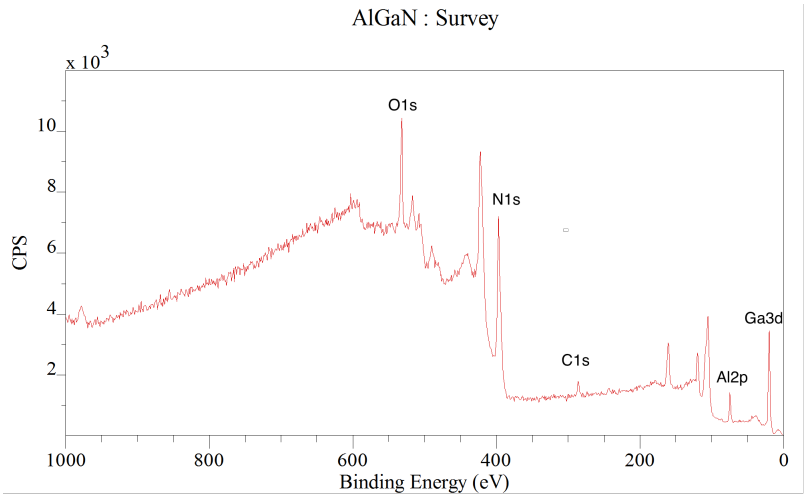

FIGURE 4.2 – AlGaN survey XPS scan

4.1.1.2 Application to the AlGaN surface

Regarding AlGaN analysis, the large difference between the characteristic energy of the AlGaN atoms allows to scan for gallium, aluminum and nitrogen. So typically, we will analyze peaks 3d for gallium, 2p for aluminum and 1s for nitrogen. Since we are interested in analyzing the surface contamination, we also analyse the carbon 1s and oxygen 1s peaks. Since it is easy to detect and almost always present at the same energy (around 285eV), Carbon 1s also serves as a reference in order to calibrate the beam and max out the count number for the analysis. Figure 4.3 represent the typical spectra of the different elements obtained for an untreated AlGaN surface.

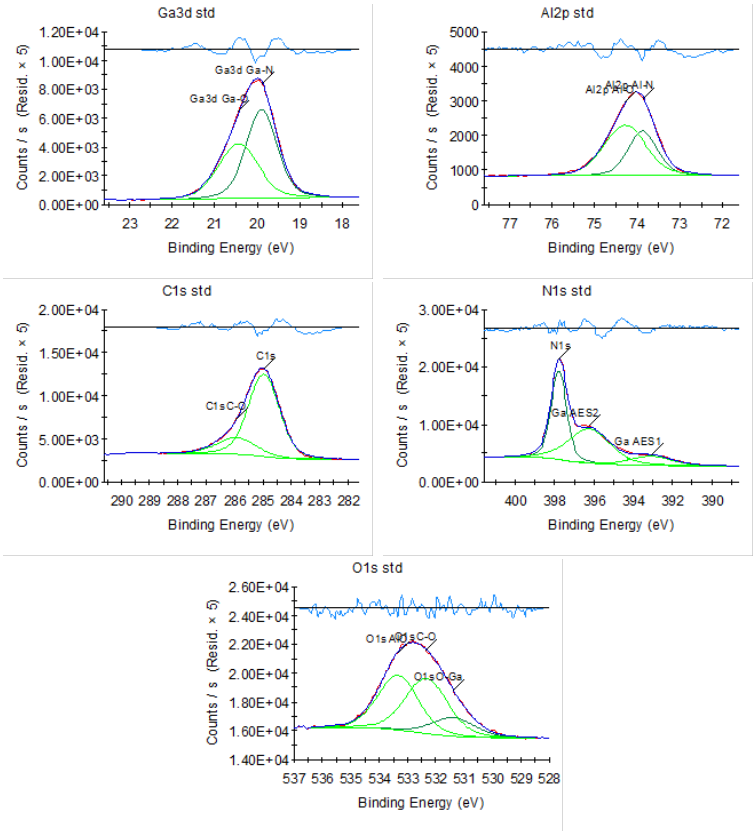

FIGURE 4.3 – AlGaN elements core levels analyzed through XPS

Once the spectrum of an element is normalized, we are then able to extract the different components of each peak corresponding to the orbitals of the analyzed element, which will give us information relatively to the bonding that is taking place for this particular element. We are thus able to separate the pure from the oxidized part of an element and determine its relative proportion using the surface under the curves.

4.1.2 Chemical treatments

4.1.2.1 HCl and SC2 treatments

A 1 :1 HCl :H_2O solution was used since it is the most common dilution used regarding hydrochloric acid. As we can see in figure 4.4 and table 4.1, this treatment

was effective in removing the native oxides and if we compare the three treated samples with the reference sample, the oxides were reduced at best of 21% and 11% regarding the aluminum and gallium respectively. Whether at high or low temperature, these results were very similar for the three samples so we can assume that the temperature at which they were treated was not a key parameter in the oxide removal power of the solution. Furthermore, the carbon concentration levels stayed the same so we can assume that this treatment is not a good solution regarding carbon contamination. One of the major drawbacks regarding HCl is that, while removing part of the oxides, it added chloride contamination which could not be removed by only rinsing the samples. One solution to increase the oxide removal of this solution might be to dip the samples for a longer time than 2 minutes, but it might on the other hand increase the chloride contamination.

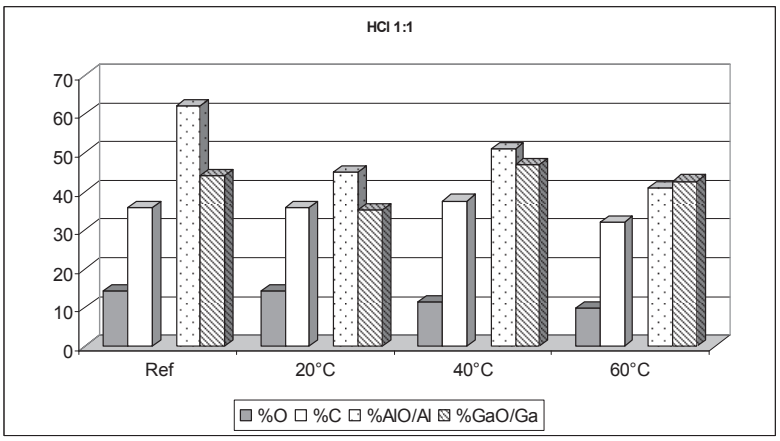

FIGURE 4.4 – Oxygen and carbon contamination after HCl treatment.

Treatments	III-N stoichiometry	$Al_xGa_{1-x}N$ (%)
Acetone/IPA rinse	0.8 : 1	29%
HCl at 20°C	1 : 1	33%
HCl at 40°C	0.9 : 1	34%
HCl at 60°C	1.2 : 1	36%

TABLE 4.1 – III-N stoichiometry and surface composition after HCl treatments

Regarding SC2 and due to its composition, we could suppose that results would be similar to the HCl solution. Instead, we can see in figure 4.5 and table 4.2 that the oxide removal is already very good at 20°C and is even better at higher temperature. For a similar time, we can see that its efficiency is more than twice as good at 40°C for the aluminum oxide, and the same can be said regarding the gallium oxide at 60°C. Unfortunately if we compare with the reference sample, the effect on carbon contamination is irrelevant (2% better at best) and we find again traces of chloride contaminants. Further more, we can see that the nitride level is slightly decreased, which is probably due to the presence of peroxide in the solution. The action of SC2 on metal oxides can be described in the following equations :

$$M + H_2O_2 \rightarrow MO + H_2O \tag{4.2}$$

$$H_2O + HCl \rightarrow H_3O^+ + Cl- \tag{4.3}$$

$$MO + 2H_3O^+ \rightarrow M^+ + 3H_2O \tag{4.4}$$

As we can see, peroxide has to make an oxygen bonding with a metal particle in order for it to be effective. But while this bonding is efficient to then remove oxides with H_3O^+, it might as well make bonds with nitrogen which might be removed along with the oxides, explaining the decrease in the nitride level.

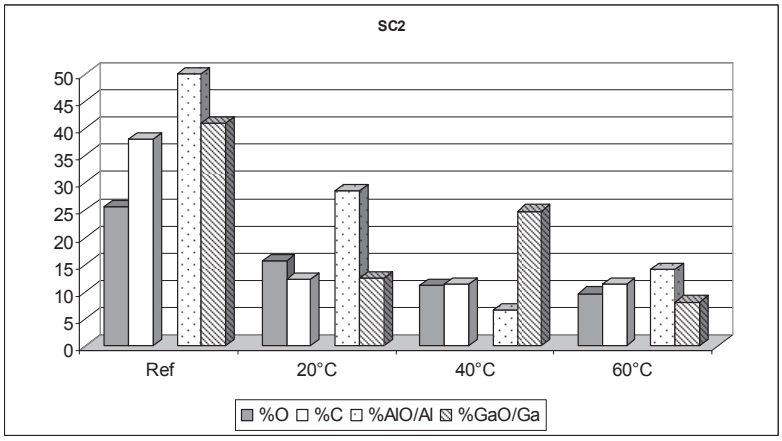

FIGURE 4.5 – Oxygen and carbon contamination after SC2 solution treatment.

Treatments	III-N stoichiometry	$Al_xGa_{1-x}N$ (%)
Acetone/IPA rinse + 2 min O_2 plasma	1.2 : 1	35%
SC2 at 20°C	1.5 : 1	27%
SC2 at 45°C	1.0 : 1	30%
SC2 at 60°C	1.2 : 1	27%

TABLE 4.2 – III-N stoichiometry and surface composition after SC2 treatments

4.1.2.2 NH_4OH and SC1

It has already been proven that ammonia is a very efficient oxide remover for GaN [39] and AlGaN [31], and a lot of papers state that they use it at 50° C as surface treatment [31, 34, 38]. Knowing this, we decided to see the impact of concentration and temperature. If we look at figure 4.6 and table 4.3, what we first see is that again the efficiency is greatly dependent of the temperature. Without considering the concentration, we clearly see that oxide removal is more than 3 times better at 75°C than at 20°C, whether it be for aluminum or gallium. What is also worth mentioning is that even at 20°C, the gallium oxide is well removed but not the aluminum one. This probably comes from the fact that Al is thermodynamically more prone to oxidize, and as such, a higher temperature is needed for the de-

oxidization process to activate. Concentration also has an important effect, and it seems better to use lower concentrations in order to get the best results. While at high temperature with a 15% solution we achieved to reduce to 9% and 3% the aluminum and gallium oxides respectively, the 10% and 8.5% solutions gave us astonishing results, with gallium oxide as low as 3% and aluminum oxide under the threshold of the XPS detection. On the downside, we cannot say that the different solutions had an effect whatsoever on the carbon contamination in comparison to our reference sample. The surface stoichiometry seems also to be preserved.

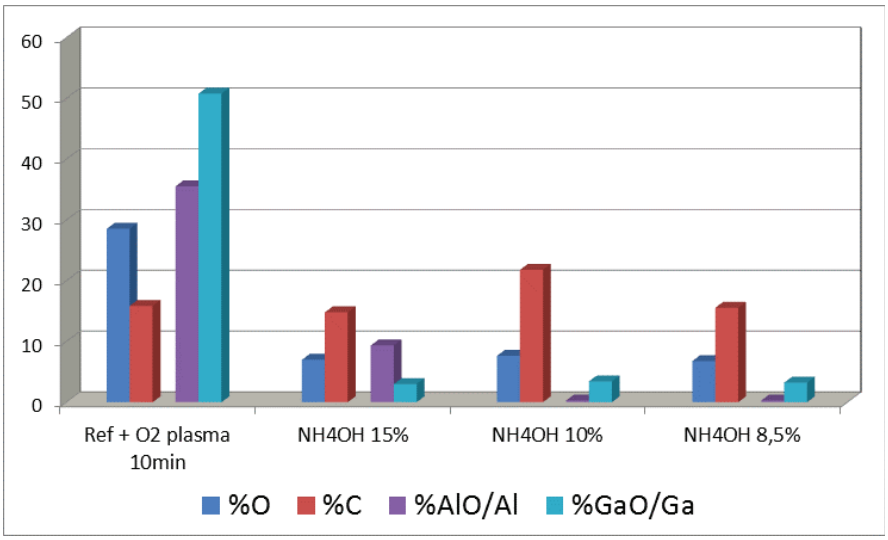

FIGURE 4.6 – Oxygen and carbon contamination after NH_4OH solutions treatments at different concentrations at 75° C.

Treatments	III-N stoichiometry	$Al_xGa_{1-x}N$ (%)
Acetone/IPA rinse + 10 min O_2 plasma	1.4 : 1	42%
NH_4OH 15% at 20°C	1.2 : 1	24%
NH_4OH 15% at 45°C	0.9 : 1	30%
NH_4OH 15% at 75°C	1.4 : 1	24%
NH_4OH 10% at 20°C	1.3 : 1	25%
NH_4OH 10% at 45°C	1.2 : 1	23%
NH_4OH 10% at 75°C	1.4 : 1	26%
NH_4OH 8.5% at 20°C	1.2 : 1	21%
NH_4OH 8.5% at 45°C	1.4 : 1	22%
NH_4OH 8.5% at 75°C	1.4 : 1	26%

TABLE 4.3 – III-N stoichiometry and surface composition after NH_4OH treatments

Regarding SC1, since it is an NH_4OH-containing solution, we could hope that the results would be very good too, but we could not achieve results as good as with the diluted ammonia. But if we look at figure 4.7 and table 4.4, it seems that the addition of peroxides only hinders the efficiency of the treatment. As with SC2,

this can be explained by the fact that peroxide has to bond with metal elements for the solution to be effective (cf equations 4.1, 4.2 and 4.3), but in this case, the OH^- molecules, brought by the presence of NH_4OH are not efficient enough in removing the created oxides, even at high temperature. Still with aluminum oxide at 7% and gallium oxide at 8% for the 40°C and 60°C treatments respectively, we achieved very good results in comparison to HCl-containing treatments. The effect on carbon is still negligible however and as with SC2, nitrogen was removed at the surface probably due to the peroxide once again.

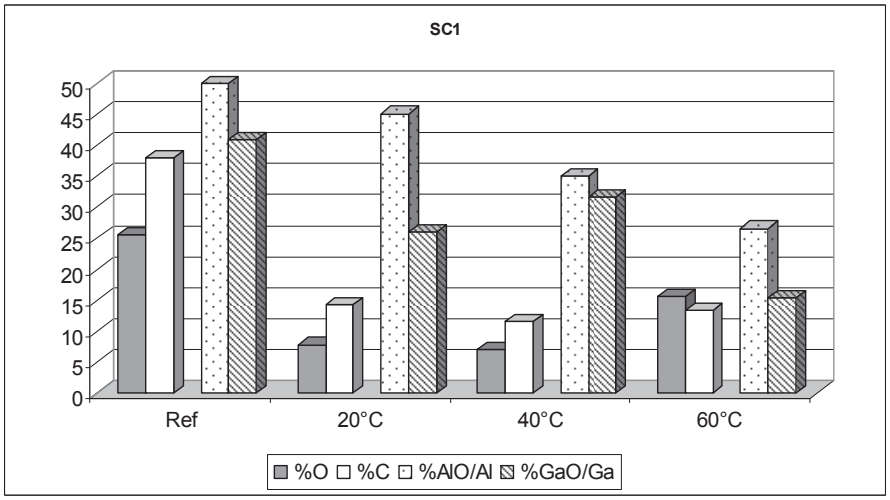

FIGURE 4.7 – Oxygen and carbon contamination after SC1 solutions treatments at different temperatures.

Treatments	III-N stoichiometry	$Al_xGa_{1-x}N$ (%)
Acetone/IPA rinse + 2 min O_2 plasma	1.2 : 1	35%
SC1 at 20°C	1.3 : 1	31%
SC1 at 45°C	1.3 : 1	40%
SC1 at 60°C	1.2 : 1	33%

TABLE 4.4 – III-N stoichiometry and surface composition after SC1 treatments

4.1.3 Plasma treatments

4.1.3.1 Oxygen plasma

The first plasma we tried was a high pressure W oxygen plasma performed on a RIE TEGAL 915. It is a pretty light plasma, mostly used to strip resist and perform light surface cleaning and descum. 2 minutes and 10 minutes exposures were conducted on samples previously rinsed with acetone and IPA. On the first sample, we can clearly see in table 4.5 that it had a positive effect regarding carbon contamination and we achieved a low carbon presence of 14%. Even while increasing the exposure length, we were not able to reduce this level and we concluded that the remaining carbon presence was due to the epitaxial conditions of the AlGaN and the precursor used. On the downside, the oxygen plasma had the negative effect of seriously reducing the presence of nitrogen at the surface, while increasing or leaving as they were the levels of oxides.

Treatments	III-N stoichiometry	$Al_xGa_{1-x}N$ (%)	Carbon concentrati
Acetone/IPA rinse	0.8 : 1	29%	36
Acetone/IPA rinse + 2 min O_2 plasma	1.2 : 1	35%	14
Acetone/IPA rinse + 10 min O_2 plasma	1.4 : 1	42%	15

TABLE 4.5 – III-N stoichiometry and carbon contamination before and after O_2 plasma treatment

4.1.3.2 Nitrogen containing plasma

After most of the treatments previously enumerated, what we noticed was that depending on the treatment, the III-Nitride stoichiometry of the surface was changed, mostly due to a reduction of the nitrogen level. In order to remediate to this problem, we decided to investigate whether it was possible or not to re-inject nitrogen on the surface through N-containing plasma treatments. It has been reported that a low power N-based plasma exposure is effective to improve global electric properties while higher energy only deteriorates overall efficiency (ECS2012 12).

However, the intervening processes were not identified and to our knowledge, we are the first to report of an XPS analysis that studies the effects of such plasma treatments on the AlGaN/GaN heterostructure surface. All the samples we used in the following study were treated with a light O_2 plasma for 2 minutes to ensure the nitrogen deficiency and the optimum 10 minutes 10% NH_4OH dip at 75°C. Unfortunately, our samples were subjected to re-oxidation between the preparation and the plasma treatments so we will only focus on the nitrogen levels.

Decoupled plasma : Since the AlGaN layer we have is very thin (around 20 nm), we first tested a decoupled forming gas plasma (N_2 with 3% of H_2), which has the advantage of being light due to its decoupled nature. If we look at figure 4.8, what we clearly see is a drastic increase in the nitrogen level on the 100 W at 150°C sample, with its N percentage more than 3 times higher than on the reference sample. However, if we increase the power, the effect is reduced and nitrogen is still re-injected but in a less efficient way. Our interpretation is that at a higher energy, the forming gas is more dissociated, which results in a larger presence of H-radicals. Those radicals tend to form NH_3 gas molecules, thus hindering the effectiveness of the nitridation. This phenomenon is even more visible at 300°C, where nothing was gained comparing to our reference sample, even at low power.

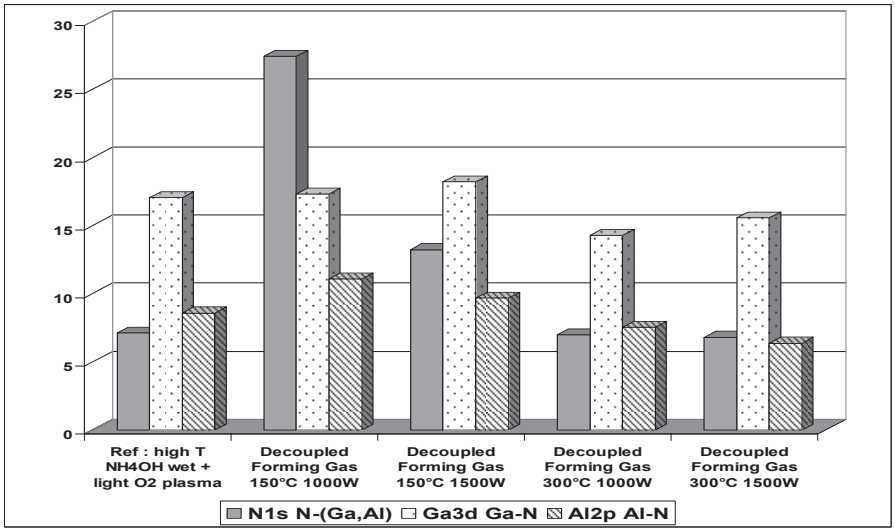

FIGURE 4.8 – N, Ga and Al percentages after forming gas plasma treatments.

In-situ plasma : The first plasma we tried was a 50 W N_2 at 300°C which ensured us to be free of the hindering hydrogen presence, with exposure times of 30 seconds and 2 minutes. Again, if we look at Figure 4.9, we can clearly see a dramatic improvement of the nitrogen level on sample treated for 30 seconds, with the N percentage again more than 3 times higher than on the reference sample. However, that increase was less significant if the exposure time is 2 minutes, with a resulting N-percentage still increased by 2. In our opinion, this comes from the fact that treatments were done at too high temperature, thus limiting the nitridation process if the exposure is too long. In the same conditions, an NH_3-based plasma proved to be much less efficient. Again the resulting percentage was 2 times higher than the reference sample, but at such a high temperature, it is possible for the NH_3 molecules to be partially dissociated but not fully, which might explain why the overall increase is not as effective.

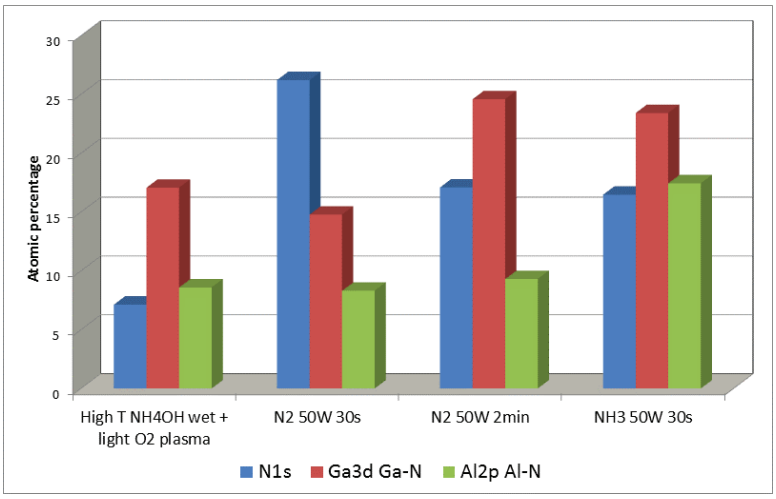

FIGURE 4.9 – N, Ga and Al percentages after N_2 and NH_3 in-situ plasma treatments

4.1.4 Surface treatments conclusion

Through the use of different chemical solutions, is has been proven that a low concentration NH_4OH dip at a temperature of 75°C for 10 minutes is the most effective to remove the AlGaN surface's native oxide. Although, as stated in the previous chapter, the influence of such a treatment on the electrical properties of transistors could not be tested, it is however a promising way for industry application where metalization steps could follow directly the surface treatment, without any prior resist coating. As such, the interface between AlGaN and metal could be relatively free of native oxide which would limit hindering effects such as the ones caused by interface traps due to poor quality oxide.

As for nitrogen containing plasma treatments, it has been proven that it is possible to reestablish proper surface stoichiometry, even from a surface which has been deeply depleted of nitrogen. Since the plasma was in-situ, it was possible to test it prior to the high-κ dielectric deposition, and its influence on the electrical properties of a MIS-HEMT will be exposed later on in this chapter. Coupled with

a low energy oxygen plasma, it could prove an efficient way to remove carbon contamination from the surface. While the latter removes carbon in an efficient way but depletes the surface of its nitrogen, the nitrogen containing plasma treatment could partially to fully repair the damage, though it might have an influence on the surface quality in fine.

4.2 Schottky gate devices

In order to apprehend the fabrication of a full MIS-HEMT, I first started by creating a normal HEMT with Shottky gate contact. As explained in chapter 3, ohmic contact was realized with Ti/Al while the gate was made using Ni/Pt/Au as stack. C(V) and $I_d(V_g)$ measurements were carried through diodes and circular transistors.

4.2.1 C(V) results

The C(V) measurements were made using a semi-automatic equipment called SIAM. The samples size being 3 cm by 3 cm, it was possible to create roughly 20 different cells on one sample, each cell containing the aforementioned diode and circular transistor seen in figure 3.2. The measurement were always the same : first the equipment would measure briefly C(V=0) in order to assess the maximum capacitance and define the scale for the built-in software, then two sweeps were made, always from depletion to accumulation, and then back from accumulation to depletion. Figure 4.10 represents a typical C(V) curve that was obtained for the Schottky gate devices.

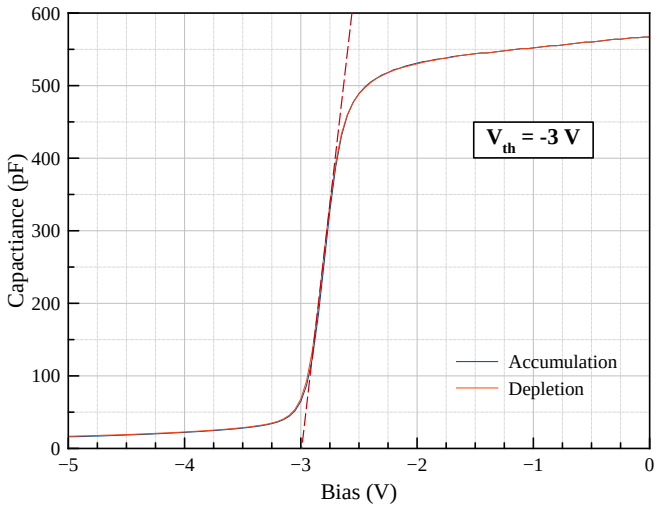

FIGURE 4.10 – C(V) response for a Schottky 400 μm diameter diode during accumulation and depletion at 100 kHz on III-V Lab wafer

This response was obtained on a wafer coming from III-V Lab. Depending on the epitaxy, the response can vary greatly as can be seen in figure 4.11 where the sample was made from a CEA wafer.

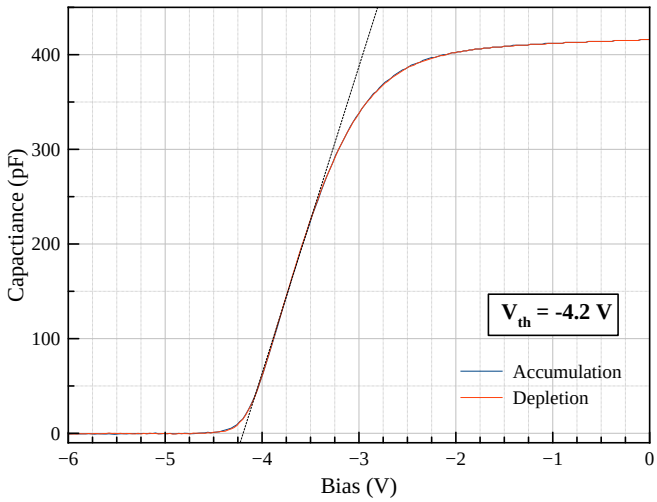

FIGURE 4.11 – C(V) response for a Schottky 400 μm diameter diode during accumulation and depletion at 100 kHz on CEA wafer

As we can see in the second C(V) response, the threshold voltage is lower and the capacitance below -4 V is slightly negative. Since a negative capacitance does not have any physical consistency, this can be associated to a leaky behavior of the diode. Also, the threshold slope in figure 4.10 is much sharper than in figure 4.11. This can come from the presence of surface traps at the metal semiconductor interface which causes the transition to be slower. Those defects may not only come from the epitaxy, but also from the engineering process depending on the surface quality before the gate metal deposition. However, having used the exact same process for the two different samples, this could probably be attributed to the buffer layers below the GaN being less insulating in the sample made on the CEA wafer.

Using these curves, it is possible to calculate the sheet carrier density n_s of the material by using the following equation :

$$n_s = \int_{V_{th}}^{0} \frac{C(V)}{q \cdot S} dV \tag{4.5}$$

where q is the elementary charge and S the surface of the diode. It is generally expressed in cm^2. The average sheet carrier density is generally around 10^{13} cm^{-2} for an AlGaN/GaN epitaxy such as the ones we used. Table 4.6 lists the results obtained for the two Schottky samples tested above.

Samples	C_{tot} (pF)	V_{th}	n_S (cm^{-2})
III-V Lab : TS088	567	-3 V	$1.41e^{13}$
CEA : 081	416	-4.2 V	$7.12e^{12}$

TABLE 4.6 – Summary of the different C(V) results obtained through Schottky structures for a III-V Lab and a CEA wafer

Generally speaking, the quality from the III-V Lab was greater than the CEA one since the latter came from early batches made on an equipment the CEA just received. As such, the MOCVD process used to create it was less accomplished since it was in its earlier development stage. This can explain the differences of

quality, notably the weaker n_s and the leaky behavior.

4.3 MIS structures

As stated in chapter 3, Metal Insulator Semiconductor devices were made using Al_2O_3 as gate insulator deposited by atomic layer deposition. The equipment that was used gave us the possibility to deposit alumina via two types of deposition. The first one is thermal ALD, where the cycles are made using pulses of TMA (Trymethylaluminum) as a precursor and water as the oxidant. The second one is PEALD, where TMA is the precursor again, but this time oxygen plasma is used for oxidation.

4.3.1 Thermal ALD structures

Diodes and circular transistors were realized once again in order to assess the performances of the insulated gate structures. In the same way as for Schottky devices, C(V) measurements were performed on the diodes. Furthermore, $I_d(V_g)$ response was evaluated on the circular transistor. All the results for thermal ALD come from samples made from the III-V Lab wafer.

4.3.1.1 C(V) results

The results for the C(V) response at 100 kHz can be seen in figure 4.12.

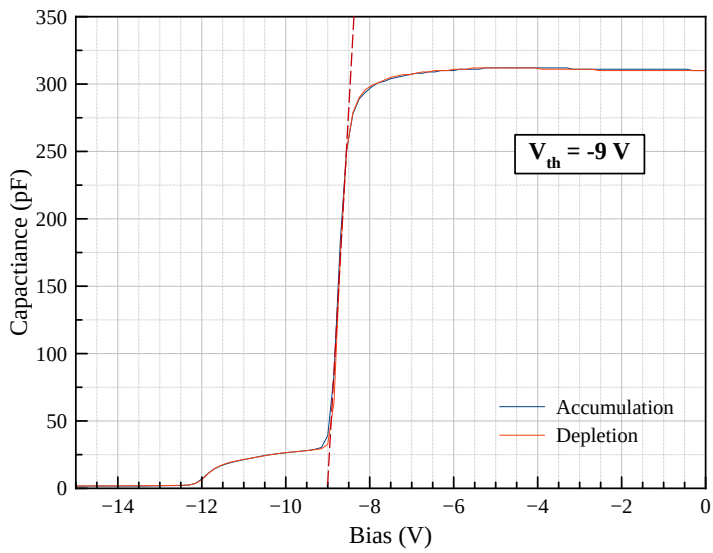

FIGURE 4.12 – C(V) response for a Thermal ALD MIS 400μm diameter diode during accumulation and depletion at 100 kHz

As we can see, the response is very peculiar with a stepped behavior appearing at the threshold voltage, as if there were two different threshold voltages. Electrically, this could assimilated as a parasitic capacitance plugged in parallel.

Another point worth mentioning, is that below a certain measuring frequency, the capacitance before the threshold was negative, and behavior was most of the time very erratic. Again, this does not have any physical sense, but indicates a very leaky the structure. This is probably due to a bad interface between the AlGaN barrier and the Al_2O_3 layer, as we can see in figure 4.13.

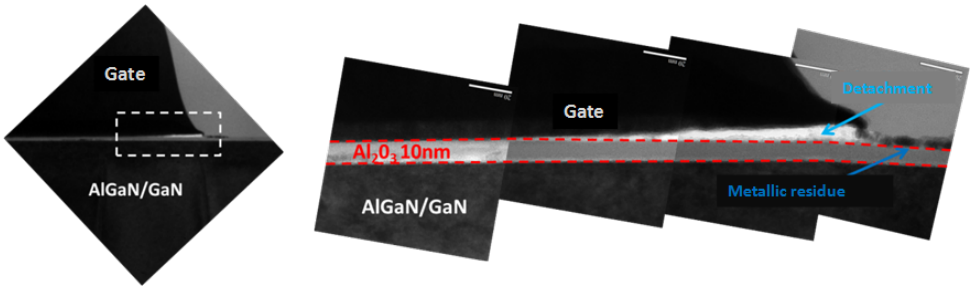

FIGURE 4.13 – TEM images at the interface between AlGaN and Al_2O_3 showing a detachment between the barrier and the insulating layer. The picture on the right corresponds to a close-up of the highlighted part of the left image.

As we can see, a detachment appeared at the edges of the transistor, leaving a gap between the insulating layer and the surface.

One of the other problems might be the surface native contamination. As explained earlier, surface treatments could not be integrated in the manufacturing process, thus potentially leaving the surface highly oxidized and carbon contaminated. This contamination is probably at the origin of various surface traps which hinders the device performances.

Regarding the threshold voltage, its shift towards negative bias is corresponding to what was expected according to equation 2.20. However, with the stepped behavior, a proper V_{th} is difficult to estimate since the peculiar form of the curve does not allow to precisely tell at which point the diode "truly" switches on. We can see however that it is roughly around -9 V, which is a considerable shift from the -3 V of the Schottky device. However, a threshold voltage shift is generally due to fixed charges, with oxide or interface traps staying populated at a given measurement frequency. Regarding the absence of hysteresis, it could be that 100 kHz is still to high a measuring frequency, not giving a chance for eventual oxide or interface traps to be populated or depopulated.

4.3.1.2 $I_d(V_g)$ results on circular transistor with L_g=100μm

The drain current response depending on the gate voltage was carried on the circular transistor as seen in figure 3.2. This $I_d(V_g)$ measurement and all the other that will be encountered later on were made with the exact same protocol : a three-point measure (one point on the source, one on the drain and the last one on the gate) was carried out by setting a fixed drain-source voltage V_{ds}, then the drain current I_s and gate current I_g were measured during a gate voltage sweep, always from depletion towards accumulation. The gate current that is reported in the later graphics is always it absolute value.

For the thermal ALD MIS structure, one of the typical response we had can be seen in Figure 4.14.

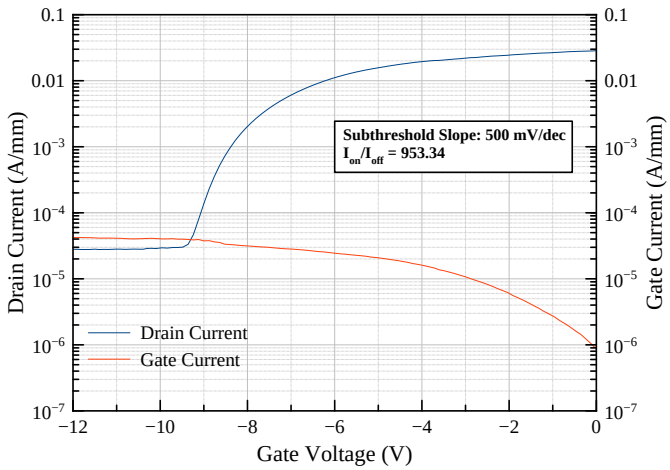

FIGURE 4.14 – $I_d(V_g)$ logarithmic response for a Thermal ALD on a circular transistor at V_{ds} = 5 V

What we can see on figure 4.14 with the logarithmic scale, is that even when fully blocked, the drain current level is quite high, roughly at 3 e^{-5} A.mm^{-1}. As a consequence, the I_{on} over I_{off} ratio is pretty low, being around 1000 only. Another point worth noticing is that the transition is quite slow, with a very high subthreshold slope value at 500 mV/dec. As for the gate leakage current, we see

that it is higher than the drain current in the off state, and decreases slowly once the threshold voltage is passed.

Using the linear scale curve, we can precisely measure the threshold like in figure 4.15. The principle here is to extract the threshold voltage by assuming that once the saturation regime is attained, the current increase is linear. So by carefully selecting the linear part of the curve, we can fit a line which will cross the x-axis at V_{th}.

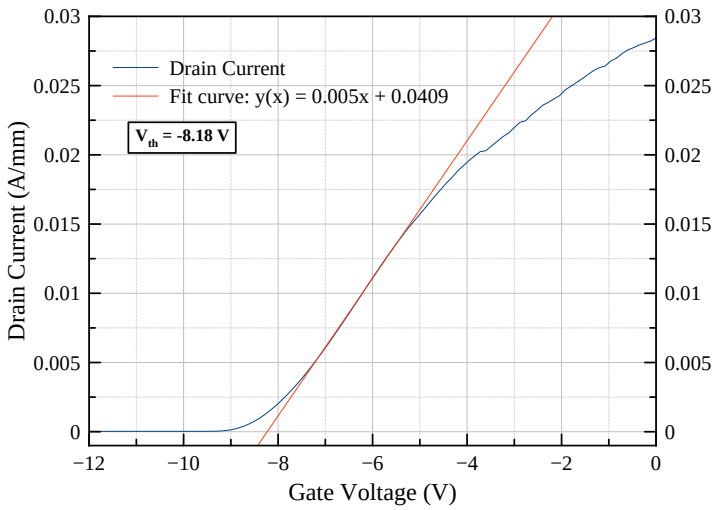

FIGURE 4.15 – $I_d(V_g)$ linear response for a Thermal ALD on a circular transistor at $V_{ds} = 5$ V with threshold voltage extraction

Those poor results are distinctive of a high gate leakage level. The ALD layer does not properly insulate the device and instead leaks like a sieve, as confirmed by the poor I_{on}/I_{off} ratio : the transistor cannot be fully blocked even at a bias well below the threshold voltage, so drain current remains high. Gate current above the drain current might also indicate that the leakage takes place in the buffer. The detachment we observed for the C(V) results might be at play here again. The very high subthreshold slope might be due to charge trapping at the interface, or maybe a high oxide state density.

4.3.2 PEALD structures

Regarding the PEALD MIS structures that were made, they were exactly the same as the thermal ALD ones. Once again, C(V) measurements were carried out at on circular diodes, as well as $I_d(V_g)$ measures on the circular transistor.

4.3.2.1 C(V) results

The first measurements that were made on the diode were C(V) sweeps at 100 kHz. Figure 4.16 represents such a measurement.

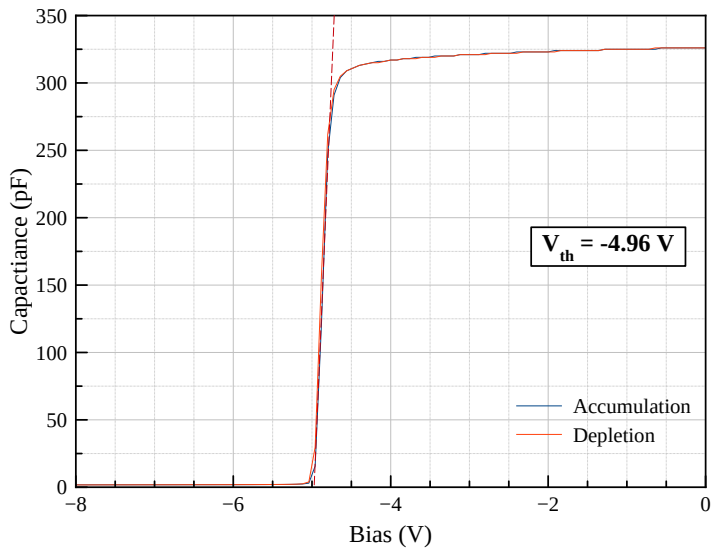

FIGURE 4.16 – C(V) response for a PEALD MIS 400 μm diameter diode during accumulation and depletion at 100kHz on a III-V Lab wafer

As we can see, the transition between the on and off state is sharper than for the thermal ALD : it is almost instantaneous, with a much sharper transition even compared to the Schottky devices.

One of the major point that can be seen, is that the threshold voltage is around -5 V, which is close to the -3 V obtained for the Schottky device. This could be due to the fact that the interface between the oxide and the AlGaN barrier is very

good, with a seamless transition between the two.

Secondly, as can be seen in figure 4.17, changing the sampling frequency did not alter whatsoever the quality of the transition. The threshold voltage was only slightly altered, and there were no negative C(V) appearing or hysteresis of any kind, even for a frequency as low as 1 kHz. This tends to indicate that the structure is very well insulated, with very few traps, explaining the extremely good behavior of the device. The absence of hysteresis at 1kHz indicates clearly that oxide or interface state density is very low. One hypothesis at this point is that the oxygen plasma of the PEALD is cleaning the surface of the AlGaN through the first cycles of the Al_2O_3 deposition, thus ensuring a smooth interface between the AlGaN barrier and the oxide.

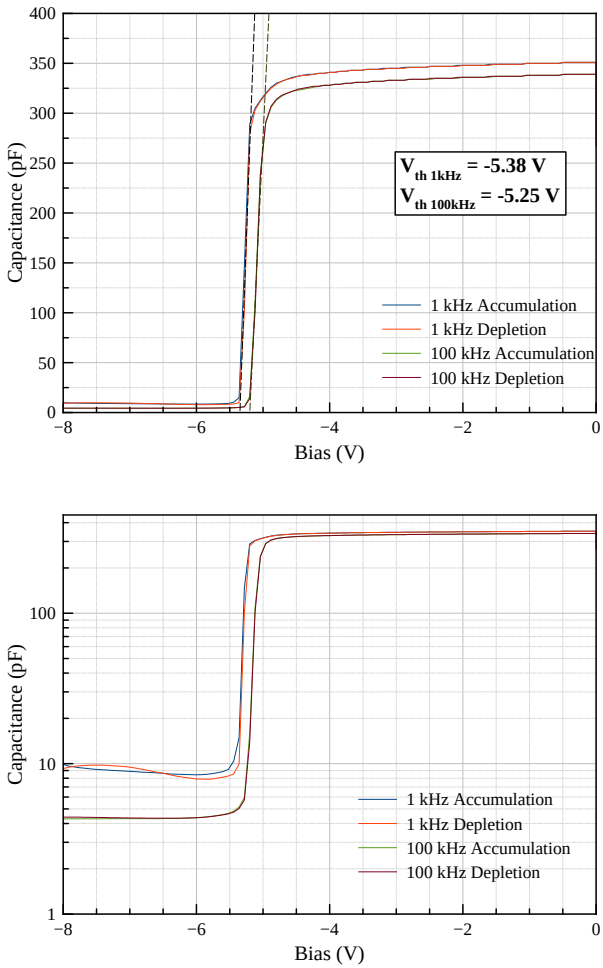

FIGURE 4.17 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400 μm diameter diode during accumulation at different frequency. The Al_2O_3 thickness is 10 nm and was deposited with a N_2 plasma pre-treatment.

However, one point that is worth noticing at this stage is that there always is a residual capacitance of only a few pF in the off state of the device, even for very low voltages. This could mean that, although the channel is fully pinched, there are still some small leaks or parasitic "fringe" capacitance. One of the possibilities could be that the buffer layers are not sufficiently insulated, inducing leakages through the buffer, mostly due to dislocations that appeared during the epitaxy. Also, since this sample was subjected to a N_2PP, this might have degraded the surface a bit

prior to deposition, explaining the slight increase in minimum capacitance at 1 kHz. This will be discussed later on in this chapter.

In order to assess the buffer influence stated above, samples were made on commercial DOWA wafer which were made with a different buffer structure, as can be seen in figure 4.18. Both sample were made with the exact same device processing.

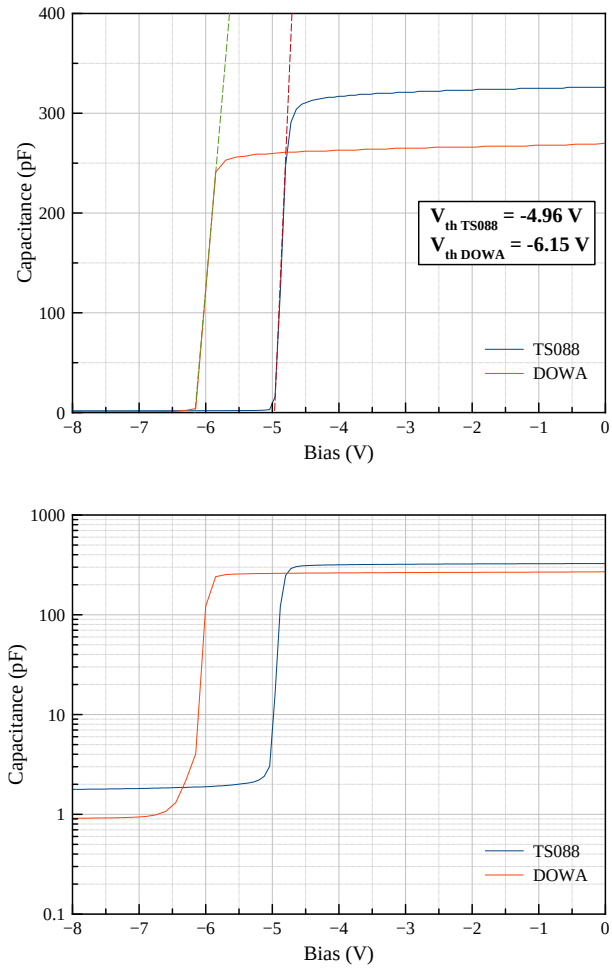

FIGURE 4.18 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400μm diameter diode during accumulation for samples from a DOWA and III-V Lab wafers. The Al_2O_3 thickness is 10 nm and the sampling frequency is 100 kHz for both samples.

We can clearly see here that the difference in the epitaxy layers clearly has an impact on the device properties as both samples were processed in the exact same way. Unfortunately, both materials characteristics remain unknown. However, through calculation, we can approximate the total equivalent thickness t_{ea} as :

$$t_{eq} = \frac{\epsilon_{AlGaN/Al_2O_3} \cdot \epsilon_0 \cdot S}{C_{tot}} \tag{4.6}$$

where ϵ_{AlGaN/Al_2O_3} and ϵ_0 are the AlGaN/Al_2O_3 and the vacuum permittivity and S the surface of the diode. Making the assumption that AlGaN and Al_2O_3 have the same permittivity at 9.3 as explained in chapter 2, we obtain and equivalent thickness of 38 nm. Since 10 nm of alumina was deposited, we can approximate the barrier thickness for the DOWA sample as being 28nm thick. The TS088 sample equivalent thickness is 21 nm.

Having calculated that, we can now understand why C_{tot} for the DOWA is lower than for TS088 since equation 2.17 states that C_{tot} is inversely proportional to the barrier thickness. A thicker barrier thus leads to a lower C_{tot}. Now if we look at equation 2.20, we can see that if the barrier thickness increases, the threshold voltage diminishes. This explains the slight C_{th} difference between the two sample, the DOWA's one being logically lower. Finally, both sample have a similar n_s as can easily be seen on the figure, both sample having approximately the same area under their respective curve. Table 4.7

Samples	C_{tot} (pF)	V_{th}	n_S (cm^{-2})
III-V Lab : TS088	270	-4.93 V	$7.82e^{12}$
DOWA	326	-6.15 V	$7.87e^{12}$

TABLE 4.7 – Summary of the different C(V) results obtained for different samples with a different epitaxy

Interestingly, changing the frequency to 1 kHz on the DOWA sample has a similar effect as the one observed in figure 4.17. Looking at figure 4.19 we clearly see that, at a lower frequency, the switching behavior stays the same while V_{th}

is slightly shifted towards the negative. However the minimum capacitance C_{min} stays exactly the same here, though it wobbles a bit once the transistor is blocked. This might indicate that 1 kHz is the limit frequency at which transistor can operate. Unfortunately, DOWA wafers being scarce during my Ph.D., I could not realize a sample subjected to N_2PP so it is difficult to compare the influence of measurement frequency between the two wafers. However, figure 4.19 shows that the residual capacitance once the channel is pinched is inferior to 1 pF, which corresponds to detection limit of the measuring apparatus. Since in this figure, both sample were made in the exact same way, we can surmise that the DOWA buffer insulates in a better way.

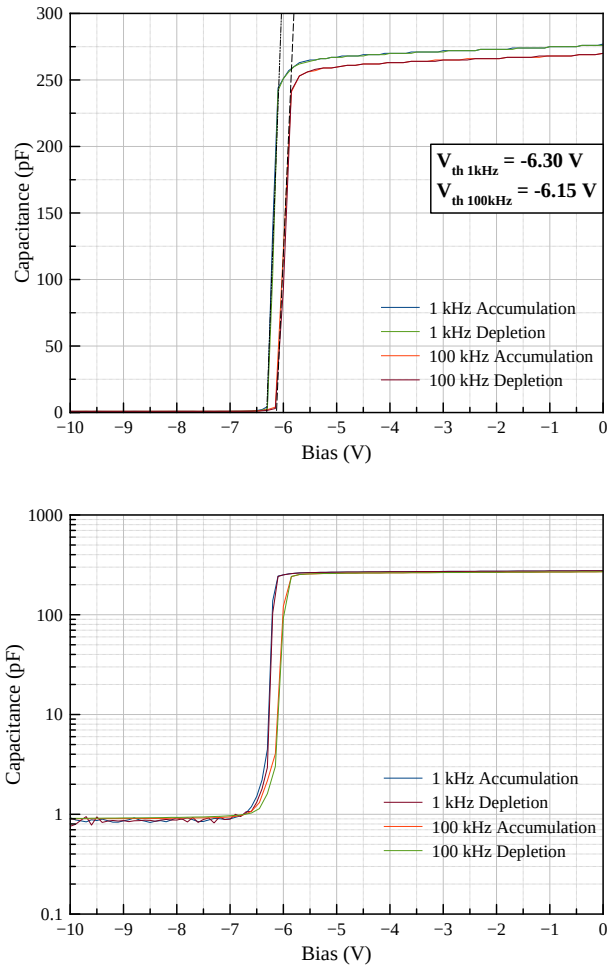

FIGURE 4.19 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400μm diameter diode during accumulation for samples from a DOWA wafers at different frequencies. The Al_2O_3 thickness is 10 nm.

4.3.2.2 $I_d(V_g)$ results on circular transistor with L_g=100μm

As for the C(V), $I_d(V_g)$ yielded very good results using Al_2O_3 deposited by PEALD as a gate insulator. One of the typical response that was obtained for a circular transistor made with a 10 nm alumina layer can be seen in Figure 4.20.

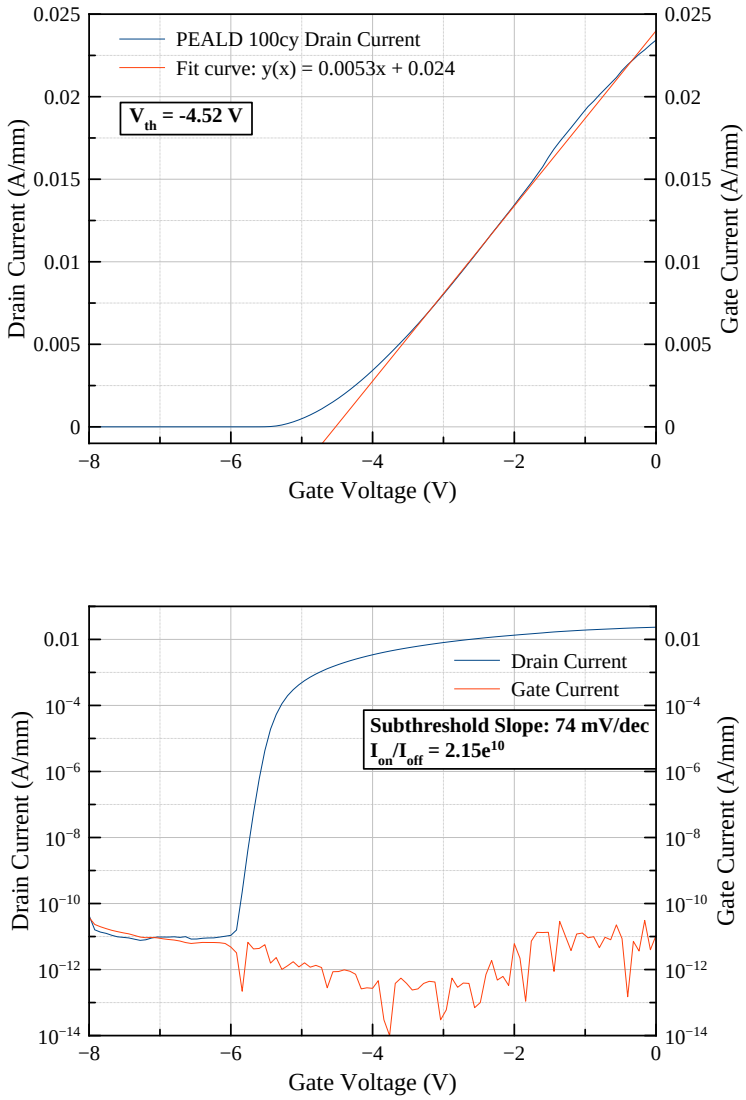

FIGURE 4.20 – Linear (up) and logarithmic (down) $I_d(V_g)$ response for a PEALD on a circular transistor at V_{DS}=5 V

We can directly observe that the current level at the off-state is much lower than for the thermal ALD. In fact, we can see that the gate leakage current is reduced by six orders of magnitude and that the drain and gate current are the same, which means that the leakage current is exclusively a gate leakage current.

The second major difference between the two ALD deposition techniques is during the pinch-off transition. In the thermal ALD case, the transition is soft, slow and indistinct, the current difference between the on and off state being weak. However, in case of PEALD, the transition is really sharp and fast, with a record subthreshold slope of only 74 mV per decades being achieved [40, 41]. No erratic behavior was observed whatsoever.

Finally, a very good I_{on}/I_{off} ratio of 10^{10} was achieved, with leakage currents as low as 10^{-11} A.mm^{-1}. Regarding the current at 0 V being around 10 mA.mm^{-1}, it is not as high as one could hope, but this can be explained by the geometry of the circular transistor, the gate being really large and long. A smaller gate could probably yield higher levels of current output but could unfortunately not be evaluated during this Ph.D.

Those results are very interesting because it clearly appears that the alumina insulating layer is performing its job pretty well. It is also surprising since the difference with thermal ALD results is quite huge, even if both samples were created with the exact same procedure. The only difference between the two is the oxidation process that was used during ALD. Again, the hypothesis that the surface is cleaned during the first cycle could explain a better AlGaN/Al_2O_3 interface.

4.4 Influence of the dielectric thickness

We have seen through theory in chapter 2 that the dielectric thickness has a direct influence on the the threshold voltage : with increasing deposited thickness, V_{th} is predicted to shift further towards negative voltage with a second degree order dependency. In order to confirm equation 2.20, samples were made for different thicknesses of Al_2O_3. Again, C(V) and $I_d(V_g)$ measurements were performed using the same diode and circular transistor as previously.

4.4.1 C(V) results

In order to assess the influence of the dielectric thickness, C(V) measurements were made with three different insulating layers. Figure 4.21 shows the obtained results for samples on which alumina was deposited for 25, 50 and 100 PEALD cycles, which corresponds to 3, 6 and 10 nm depositions respectively.

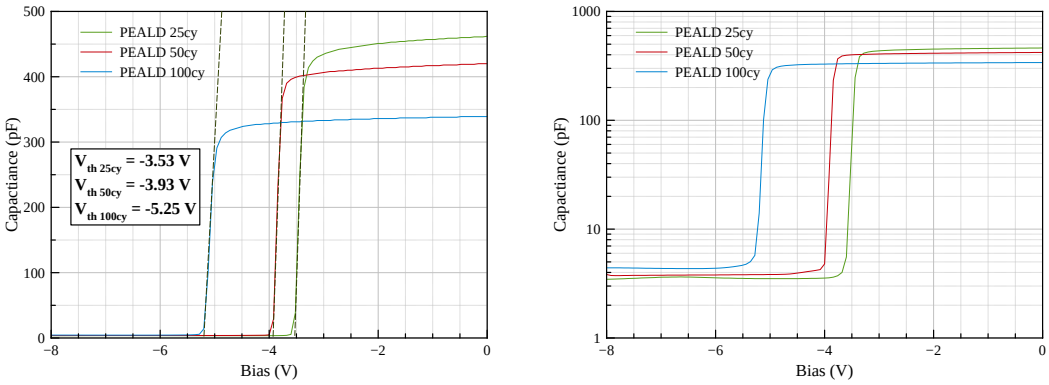

FIGURE 4.21 – Linear (left) and logarithmic (right) C(V) response for a PEALD MIS 400 μm diameter diode during accumulation for different dielectric thicknesses. Sampling frequency is 100 kHz.

As we clearly see, theory was confirmed and V_{th} was shifted towards negative biases. It is also important to notice that the maximum capacitance decreases when the insulating thickness increases, as confirmed by equation 2.17. As for the surface state density n_S, which corresponds to the area under the curves, it stays almost constant independently of the alumina thickness. All the results regarding the influence of the dielectric thickness are summarized in table 4.8.

Samples	Thickness (nm)	C_{tot} (pF)	V_{th}	n_S (cm^{-2})
Schottky	-	567	-3 V	1.41e^{13}
PEALD 25cy	3	462	-3.53 V	7.85e^{12}
PEALD 50cy	6	395	-3.93 V	8.00e^{12}
PEALD 100cy	10	339	-5.25 V	8.46e^{12}

TABLE 4.8 – Summary of the different C(V) results obtained for different Al_2O_3 thicknesses

Having measured the total capacitance, it is now possible to verify equation 2.17 stating that $1/C_{tot}$ should vary linearly with the oxide layer thickness t_{ox}. This can be confirmed in figure 4.22.

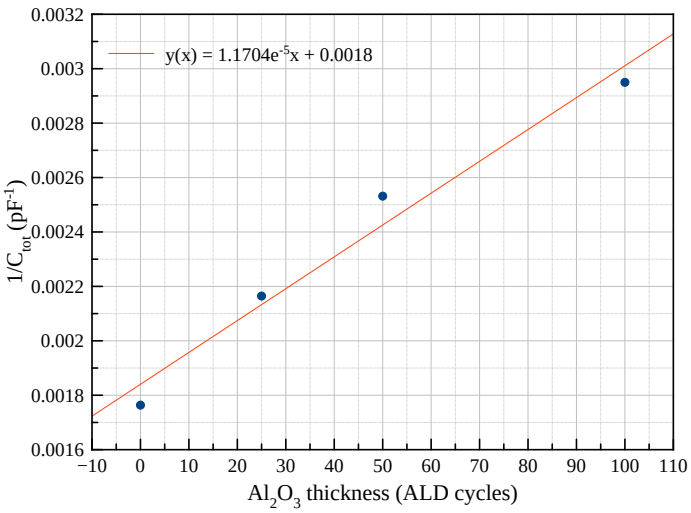

FIGURE 4.22 – $1/C_{tot}$ evolution depending on oxide layer thickness

4.4.2 $I_d(V_g)$ results on circular transistor with L_g=100μm

In the same way, $I_d(V_g)$ measurements were carried on the circular transistor, for the same thicknesses as previously. Results can be seen in figure 4.23.

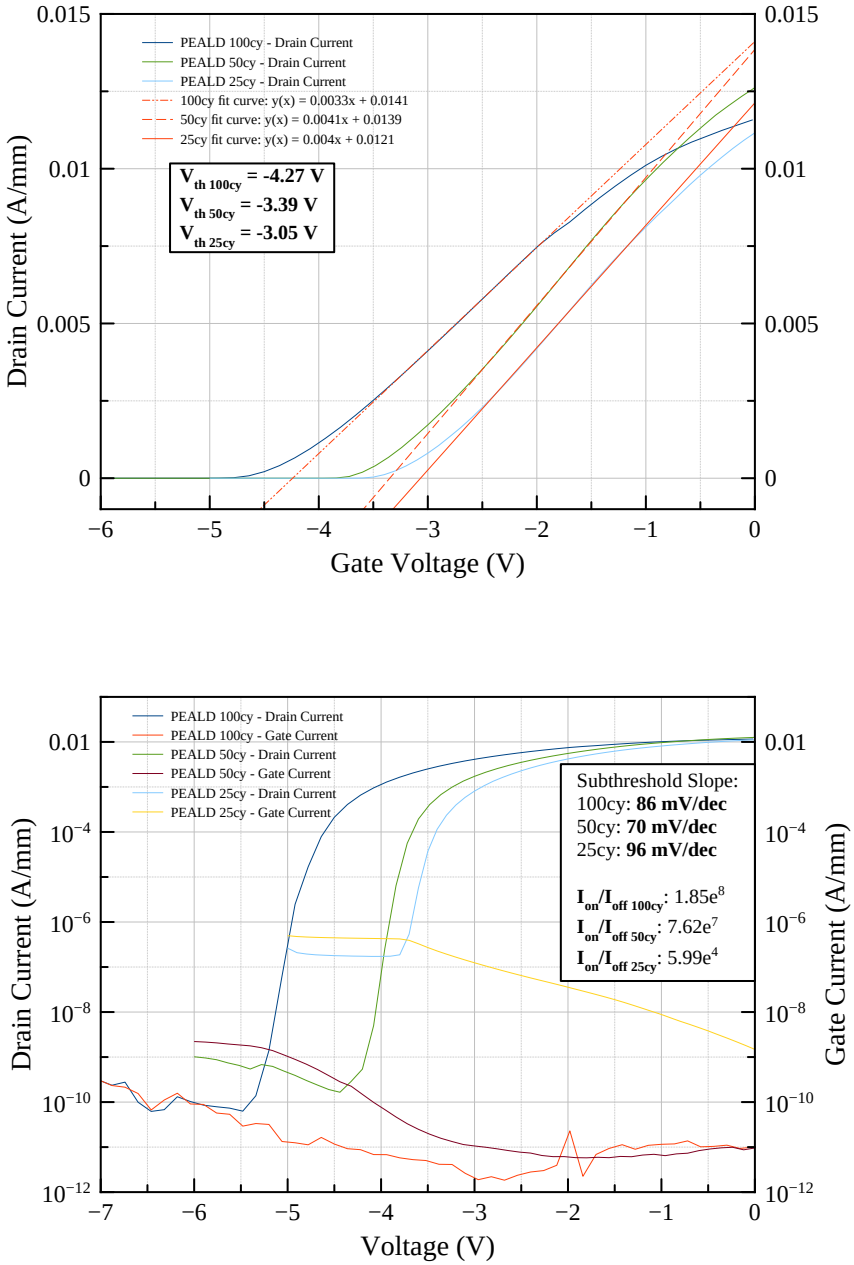

FIGURE 4.23 – Linear (up) and logartithmic (down) $I_d(V_g)$ response for a PEALD circular transistor for different dielectric thicknesses. V_{DS}=5 V.

Again, we can confirm the threshold voltage's shift towards the negative values predicted by theory. What is important to notice here is that with increasing deposited thickness comes a decrease in the off-state drain current and gate current. Intuitively, this is not surprising since an increased insulating layer is supposed to further reduce gate leakage currents. Regarding the small bump in the deep blue curve, this can probably be attributed to some residual surface contamination between the AlGaN barrier and Al_2O_3 layer which slightly hinders the transistor between the on and off state of the device. Table 4.9 summarizes the obtained results for the current measurements.

Samples	Thickness (nm)	V_{th}	I_{on}/I_{off}	Subthreshold slope
PEALD 100cy	10	-4.27 V	$2.15e^{10}$	86 mV/dec
PEALD 50cy	6	-3.93 V	$7.62e^{7}$	70 mV/dec
PEALD 25cy	3	-3.05 V	$5.99e^{4}$	90 mV/dec

TABLE 4.9 – Summary of the different $I_d(V_g)$ results obtained for different Al_2O_3 thicknesses

4.4.3 Threshold voltage evolution

Using both C(V) and $I_d(V_g)$ measurements, it was possible to extract the evolution in the threshold voltage V_{th} depending of the Al_2O_3 thickness. Of course, results were different for the two measurements since they were not made on the same device, not even in the same cell. This evolution was reported in figure 4.24

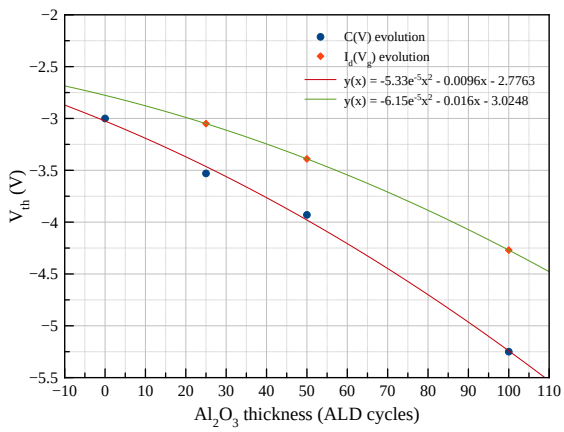

FIGURE 4.24 – V_{th} evolution depending on the insulating layer thickness

Equation 2.20 tells us that the V_{th} dependency towards the dielectric thickness is of the second order and it can be easily verified here as shown by the fit curves. The fit values obtained could even be directly linked to the elements of equation 2.20. Arguably however, with only three or four points per curve, it is easy to extract a parabola that fits relatively well, but a linear approximation is also quite a good approximation. As such, it could be interesting to complete this curve by adding multiple points to it, especially for high dielectric thicknesses. Unfortunately, this could not be achieved during this Ph.D.

4.5 Influence of post-deposition thermal treatment

In order to see if it was possible to further improve the electrical properties of our PEALD MIS structures, rapid thermal annealing after ALD deposition was experimented. The objective here is to anneal the high-k at different temperature in order to reduce positive charge trapping inside the Al_2O_3 and thus make the V_{th} less negative. This was done prior to the gate deposition process.

4.5.1 C(V) results

As we can see in figure 4.25, the RTA did not have the expected effect. Compared to a MIS structure without any RTA, it made V_{th} more negative and slightly increased the minimum capacitance C_{min}. And the higher the RTA temperature, the further V_{th} was shifted towards negative values and the C_{min} increased.

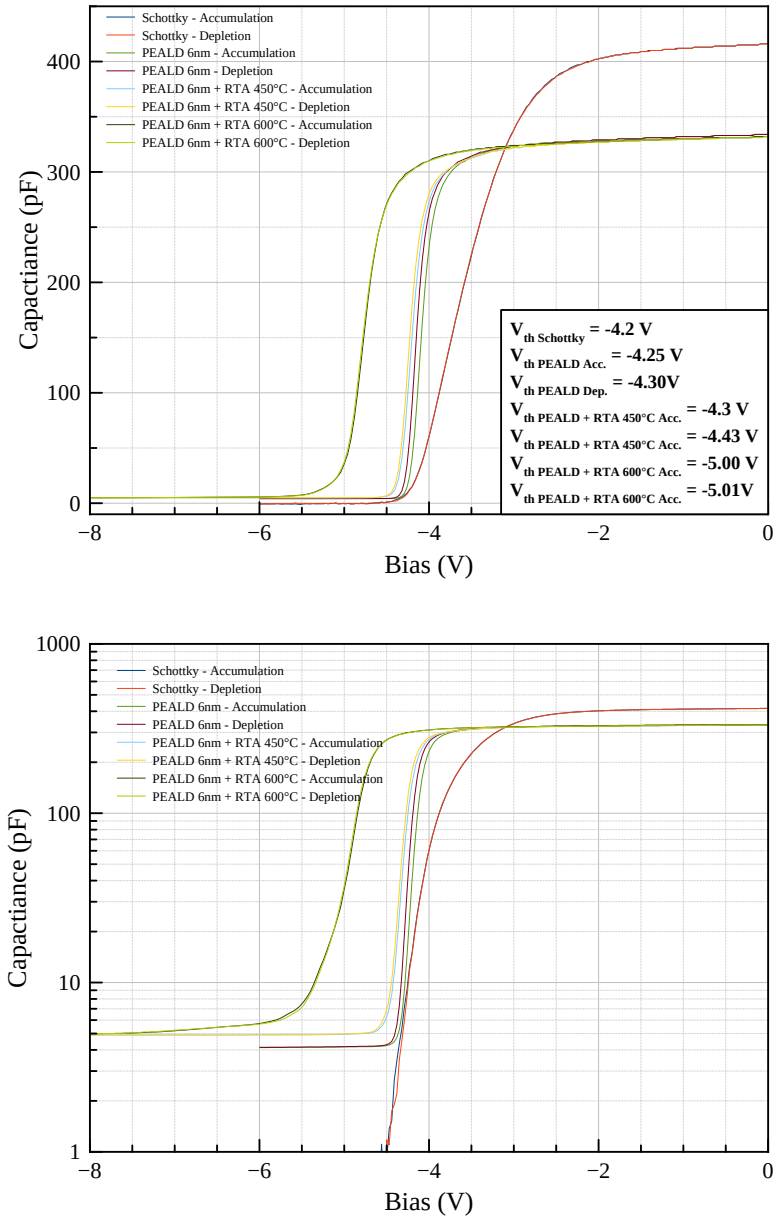

FIGURE 4.25 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400 μm diameter diode after different RTA. The Al_2O_3 thickness is 10 nm and the sampling frequency is 100 kHz.

The logarithmic curve here is quite interesting as we can clearly see that for the 600°C, the transition happens very slowly compared to the other curves while the

V_{th} difference between accumulation is in counterpart almost null. Full depletion is also achieved at a largely inferior bias, well past -6 V. This could be explained by the fact that interface and oxide traps become occupied as soon as the accumulation begins and remain occupied. Table 4.10 summarizes the different results obtained for C(V) measurements.

Samples	C_{tot} (pF)	V_{th}(accumulation/depletion)	n_S (cm^{-2})
Schottky	416	-4.20 V	$7.12e^{12}$
MIS 6 nm	334	-4.25 V/-4.30 V	$6.65e^{12}$
MIS 6 nm + RTA 450°C	332	-4.30 V/-4.43 V	$6.76e^{12}$
MIS 6 nm + RTA 600°C	332	-5.00 V/-5.01 V	$7.55e^{12}$

TABLE 4.10 – Summary of the different C(V) results obtained through Schottky and MIS structures, with and without RTA.

4.5.2 $I_d(V_g)$ results on circular transistor with L_g=100μm

Regarding for $I_d(V_g)$ results measurements, we see in figure 4.26 that RTA led to more negative V_{th} and higher gate leakage current in both cases, with again higher degradation, the higher the RTA temperature was.

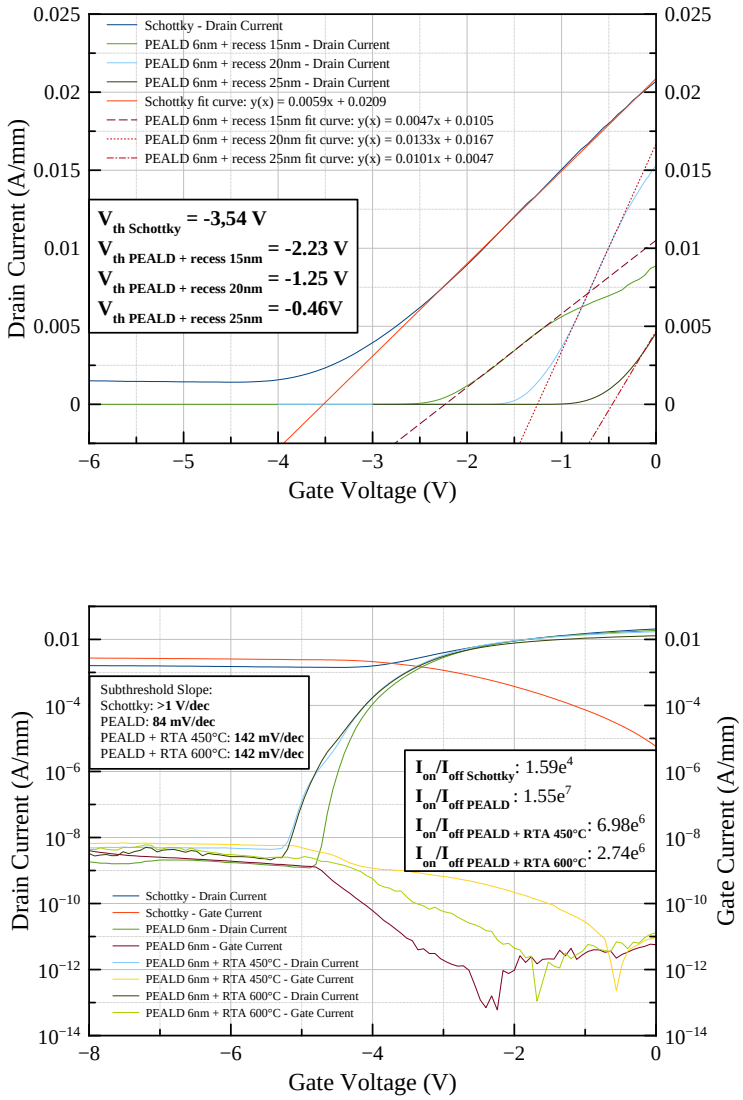

FIGURE 4.26 – Linear (Up) and logarithmic (Down) $I_d(V_g)$ response for a PEALD MIS transistor after different RTA. The Al_2O_3 thickness is 10 nm and $V_{ds} = 5$ V.

After RTA, one possible explanation regarding the overall decrease in electrical performances could be due to the fact that there is a formation of a bad quality Ga_2O_3 at the interface. This is confirmed by the fact that the C(V) transitions are less abrupt and with a higher C_{min}, and that the gate leakage current levels

are higher. As with the thermal ALD, this behavior is characteristic of bad quality interface between the oxide and the AlGaN surface. Table 4.11 summarizes the different $I_d(V_g)$ results obtained through the use of post-PEALD RTA.

Samples	V_{th}	I_{on}/I_{off}	Subthreshold slope
Schottky	-3.54 V	1.59e^4	>1 V/dec
MIS 6 nm	-3.39 V	1.55e^7	84 mV/dec
MIS 6 nm + RTA 450°	-3.53 V	6.98e^6	142 mV/dec
MIS 6 nm + RTA 600°	-3.63 V	2.74e^6	142 mV/dec

TABLE 4.11 – Summary of the different $I_d(V_g)$ results obtained through Schottky and MIS structures, with and without RTA.

All in all, this experiment towards increasing the threshold voltage was a failure. However, it is important to add that the annealing was performed in an un-optimized way since the oven in which it was made might have be badly insulated. As a matter of fact, even though the annealing was performed under a small vacuum, where multiple purges were made beforehand with inert gas, it is most probable that high oxygen contamination occurred. This could confirm the hypothesis of the poor quality Ga_2O_3 formation at the interface.

Another point worth mentioning is that even though Al_2O_3 crystallization only occurs at 900 °C, it might have begun slightly at 600°C. I have ensured during this entire Ph.D. that alumina was staying in its amorphous form, but it could not be verified here, for example using Transmission Electron Microscopy. Crystallized Al_2O_3 has proved to lead to poor MIS-HEMT behavior in other studies (trouver référence).

4.6 Superiority of PEALD over thermal ALD

In view of above showed results, it is obvious that, for the exact same processing and measuring conditions, PEALD is vastly superior to thermal ALD. While it is most probably related to interface quality, the two methods still deposit the same oxide, and it is thus confusing that such a difference should arise.

One of the hypothesis that was made is that PEALD tend to "clean" the surface prior to deposition. In the very first deposition cycles, deposition of Al_2O_3 by ALD is known to have cleaning properties on other III-V materials such as GaAs or InGaAs (reference à mettre), but so far, this has not been proven valid for GaN nor AlGaN. XPS analysis were performed in order to assess the influence of thermal- and PE-ALD on the AlGaN surface during the first deposition cycles but proved inconclusive. Carbon contamination was also checked, but the difference between the two deposition techniques was very tiny, and arguably not enough to prove that PEALD cleans the surface of carbon due to its oxygen plasma.

However, this latter hypothesis could still be valid through the use of AFM analysis. In order to sustain this argument, three different samples have to be compared : a raw AlGaN sample, without any treatment, an O_2 plasma treated sample and a sample on which alumina was deposited with only a few cycles of PEALD. These three images can be seen in figure 4.27, 4.28 and 4.29 respectively.

If we look at the raw sample, we can see that it has a grainy aspect, far from the traditional terrace like appearance of AlGaN. After a 10 min oxygen plasma treatment, we can see that we recovered the terrace-like aspect, and XPS analyses have proven that carbon levels were drastically reduced. Now if we look at the samples which underwent PEALD deposition, we can clearly see that the terraces are there as well.

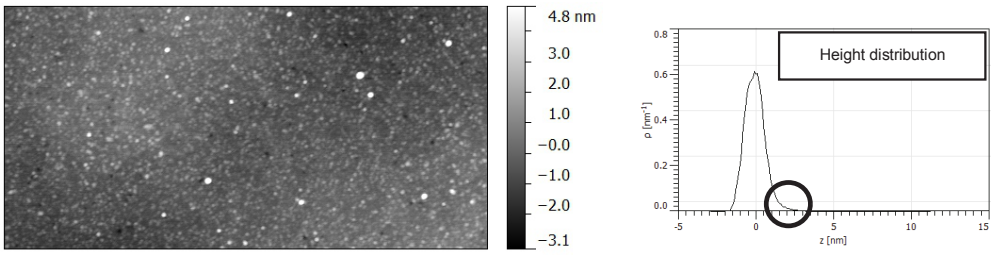

FIGURE 4.27 – AFM picture and height distribution of reference sample. Grainy aspect and small asymmetry in height distribution. Rms=0.72nm.

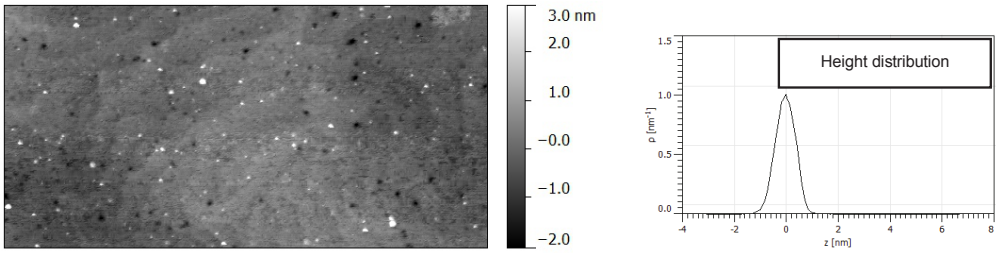

FIGURE 4.28 – AFM picture and height distribution of a reference sample treated with a 10 min oxygen plasma. Recovery of the terrace like aspect and reduction of roughness. Rms=0.43nm.

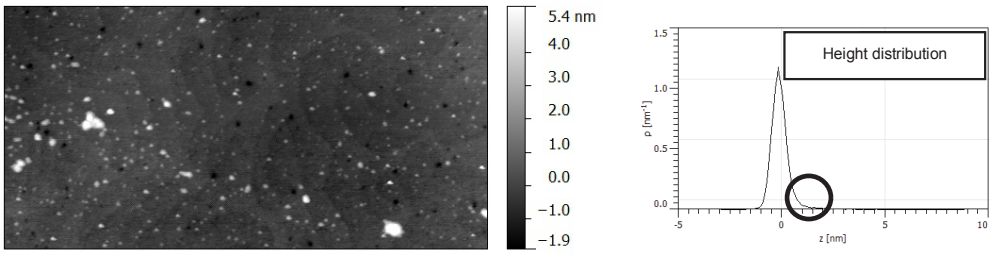

FIGURE 4.29 – AFM picture and height distribution of a reference sample after 3 cycles of ALD using O_2-plasma steps. Terrace like aspect is visible with a reduced roughness. Rms=0.63nm. Small asymmetry in height distribution is related to N_2 plasma pre-treatment.

In terms of electrical response, it is also evident that the deposition method has a dramatic effect, as was observed previously. This can be seen both in C(V) and $I_d(V_g)$ through figure 4.30 and 4.31 repectively, where thermal and PEALD results are directly confronted.

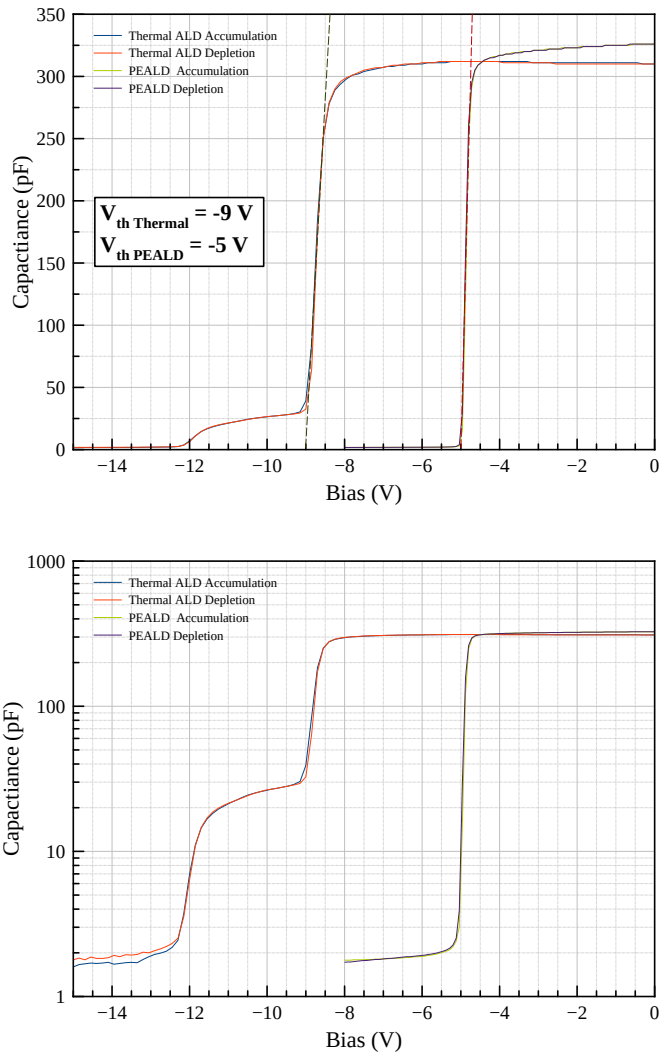

FIGURE 4.30 – Linear (up) and logarithmic (down) C(V) response for a 400 μm diameter diode after both thermal ALD and PEALD deposition. The Al_2O_3 thickness is 10 nm and the sampling frequency is 100 kHz.

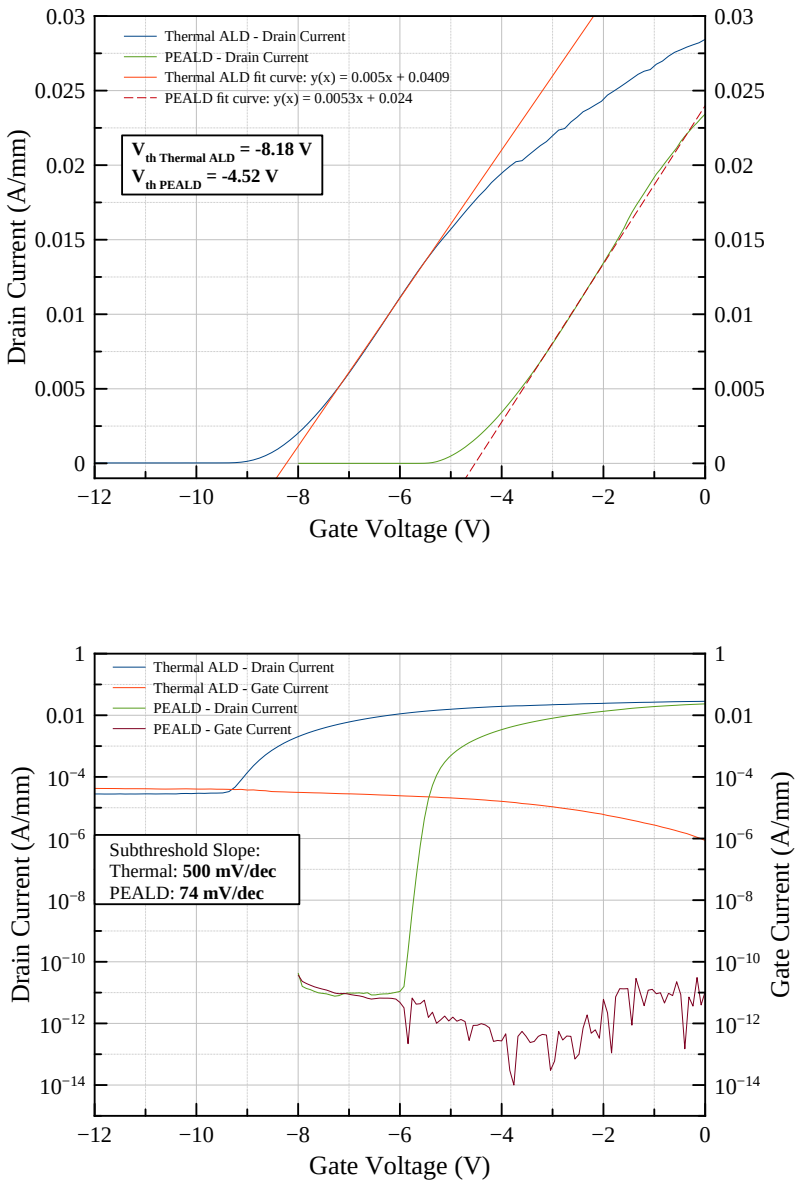

FIGURE 4.31 – Linear (up) and logarithmic (down) $I_d(V_g)$ response for a circular transistor after both thermal ALD and PEALD deposition. The Al_2O_3 thickness is 10 nm and $V_{ds} = 5$ V.

Influence of N_2 plasma pre-treatment Since it also underwent a nitrogen plasma treatment prior to deposition, one could arguably say that it is the latter that is responsible for the surface recovery seen in figure 4.29. However, this has to be compared in turn with figure 4.32 where the samples were treated with N_2 plasma only. Roughness was increased as can be seen through the numerous white dots on the image, but we can see no terrace recovery whatsoever. This would tend to confirm that the oxygen plasma is responsible for the surface recovery and, similarly to the O_2 plasma only treatment, that the carbon contamination was indeed reduced during the first cycles of PEALD.

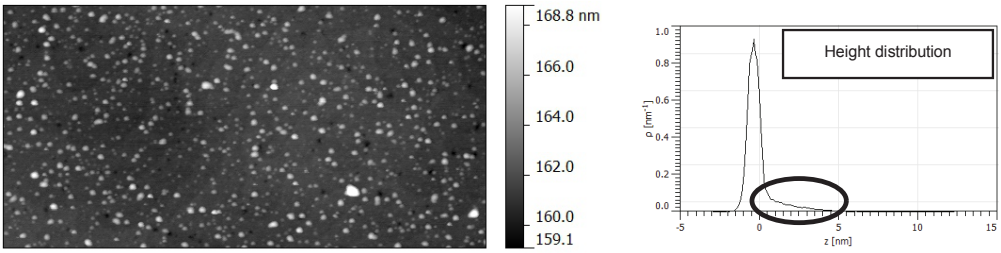

FIGURE 4.32 – AFM picture and height distribution of a reference sample treated only with N_2 plasma pre-treatment. Roughness increase and strong height distribution asymmetry. Rms = 1.02 nm.

In terms of electrical response, it is also evident that the influence of the N_2PP is rather important, as can be seen both in C(V) and $I_d(V_g)$ through Figure 4.33 and 4.34 repectively.

Looking at the C(V) results, whether it be with thermal or PEALD, we can see that influence of N_2PP is rather nefarious : negative V_{th} shift, C_{min} increase, and a high degradation of the transition quality in the case of thermal ALD. As stated earlier, this corresponds to an increase in the leaking behavior of the structure and potentially the appearance of charged surface states.

For the $I_d(V_g)$ comparison, the increase in leakage behavior is also directly observed in both cases with an increase of both drain and gate current in the off state and a lowering off the I_{on}/I_{off} ratio. The augmentation off the subthreshold

slope and V_{th} shift is generally characteristic of the presence of oxide or surface traps.

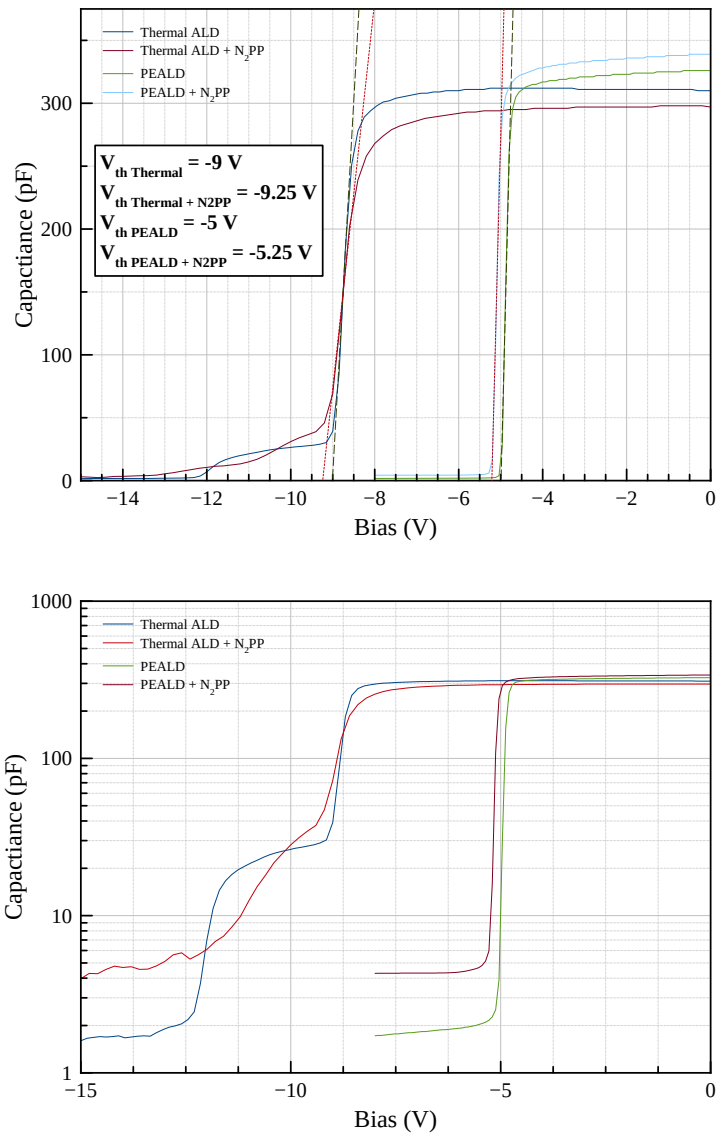

FIGURE 4.33 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400 μm diameter diode after both thermal ALD and PEALD deposition, with and without N_2PP. The Al_2O_3 thickness is 10 nm and the sampling frequency is 100 kHz.

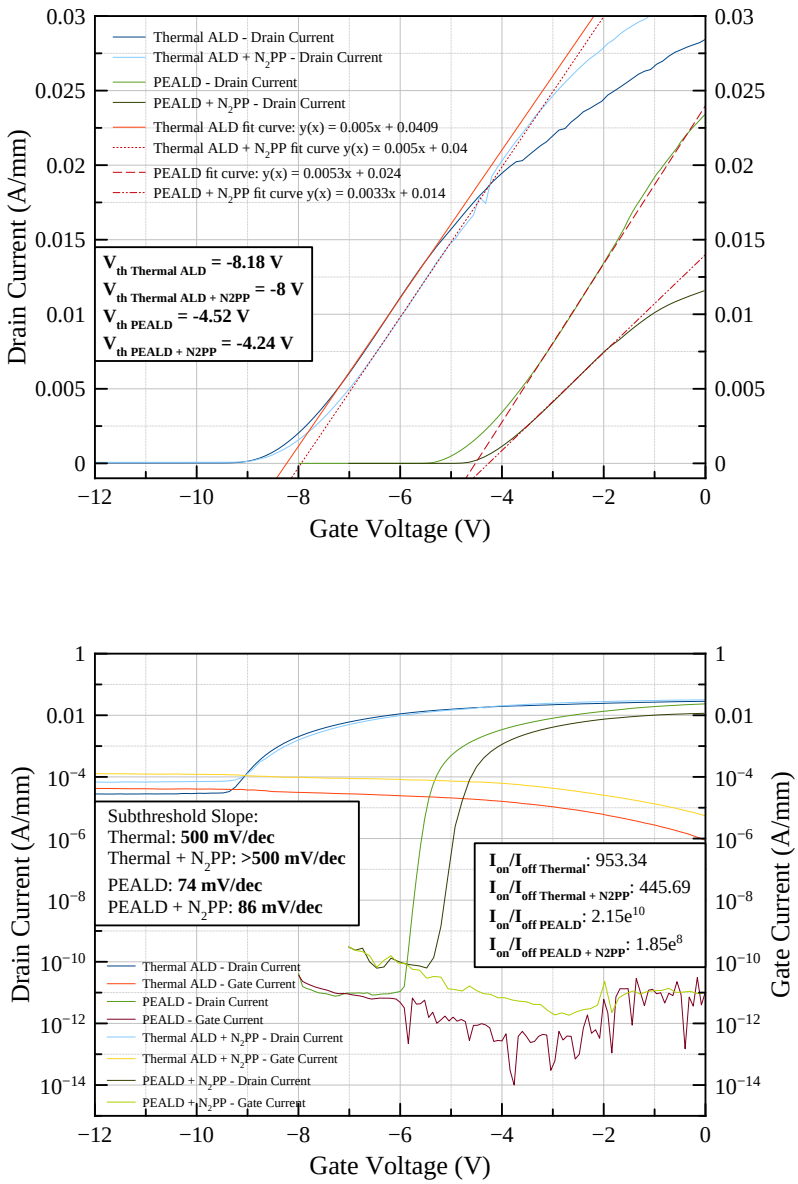

FIGURE 4.34 – Linear (up) and logarithmic (down) $I_d(V_g)$ response for a circular transistor after both thermal ALD and PEALD deposition, with and without N_2PP. The Al_2O_3 thickness is 10 nm and $V_{ds} = 5$ V.

4.7 Normally-Off architecture : MIS structure with partial or full AlGaN recess etching

Up until now, all the results that have been showed were for normally-on structures. This comes from the intrinsic electrical properties of the AlGaN/GaN heterostructure. As was stated in the previous chapters, one objective is to achieve the fabrication of components functioning in a normally-off regime. The first step towards achieving a normally-off behavior is to increase the threshold voltage towards 0 V. In order to do so, partial and full gate recess etching were implemented in the transistor creation process.

4.7.1 Gate Recess Etching

As stated in chapter 3, one objective of the MIS-HEMT structure is to obtain a device with a threshold voltage as close as possible to 0 V, the ideal case being when a positive threshold is attained. However, this has to be made without deteriorating the qualities of the MIS-HEMT. With this consideration in mind, the solution that was retained is to perform a gate recess etching. This was performed through the use of a ICP-RIE etching, which is particularly well suited for the AlGaN barrier etching, thanks to its slow etching rate which ensures that as little damage as possible is made to the surface.

4.7.1.1 C(V) Results

In order to assess the influence of the gate recess etching on the threshold voltage, different components were made for different etching depths. Figure 4.35 displays the obtained results for a 10, 15 and 20 nm recess. The results for a non-recessed MIS diode and a Schottky diode were included for comparison.

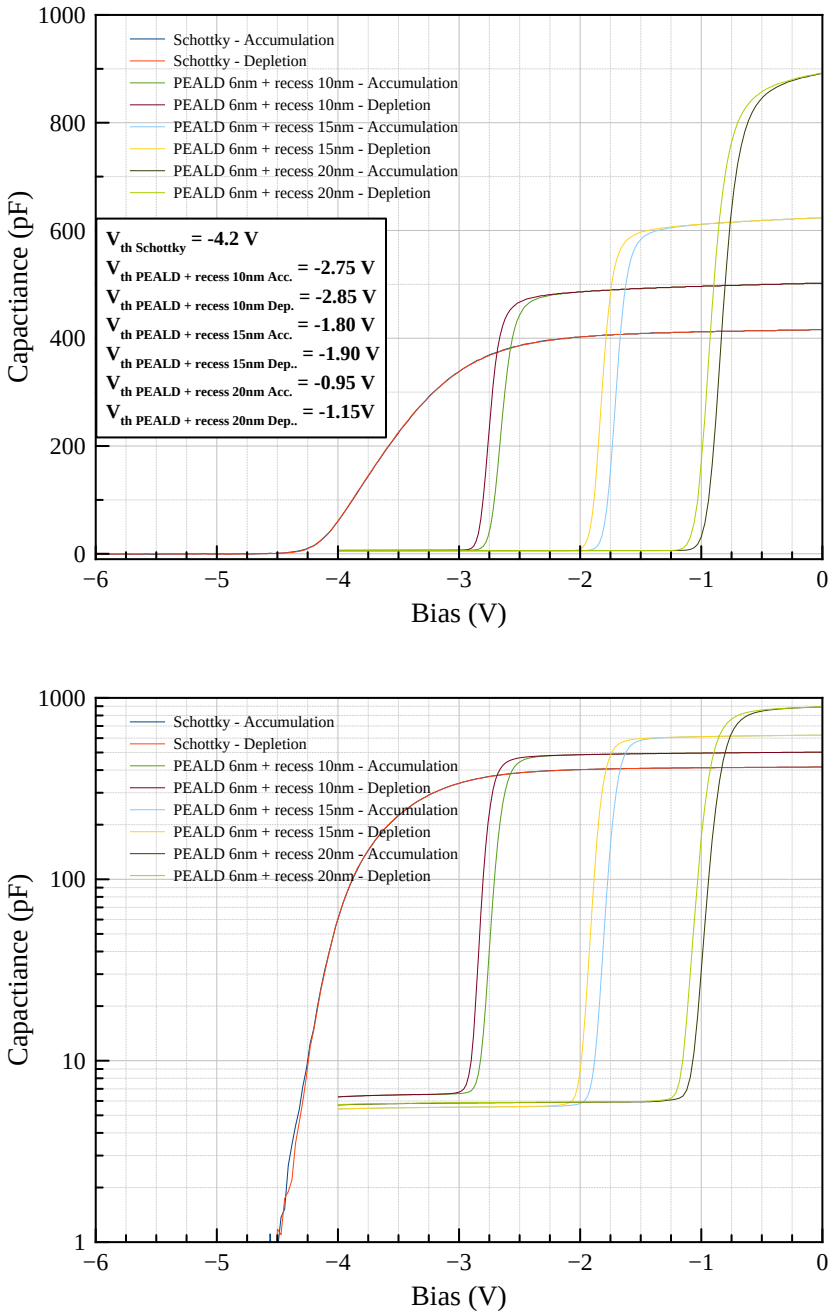

FIGURE 4.35 – Linear (up) and logarithmic (down) C(V) response for a PEALD MIS 400μm diameter diode after different recess etchings. The Al_2O_3 thickness is 6 nm and sampling frequency is 100 kHz.

As we can clearly see, the shift in the threshold voltage increases towards the positive voltage when the recess depth increases. With a recess of 20nm, the AlGaN thickness being of 25 nm, it was possible to increase V_{th} by 4 V, without sacrificing the abrupt transition between the on and off state. Furthermore, measurements were stable again for frequencies as low as 0.1 kHz, which indicates a good preservation of the low leakage properties introduced via the PEALD MIS structure. However, depletion was slightly degraded with a higher C_{min}, and a small hysteresis was introduced between the depletion and accumulation regime. This is probably due to the roughness increase at the bottom of the recess. It might have generated traps or vacancies, which could in term induce the slight performance degradation we observed. Results are summarized in table 4.12

Samples	C_{tot} (pF)	V_{th}(accumulation/depletion)	n_S (cm^{-2})
Schottky	416	-4.20 V	$7.12e^{12}$
MIS 6 nm	332	-4.25 V/-4.30 V	$6.65e^{12}$
MIS 6 nm + recess 10 nm	502	-2.75 V/-2.85 V	$4.79e^{12}$
MIS 6 nm + recess 15 nm	624	-1.80 V/-1.90 V	$5.06e^{12}$
MIS 6 nm + recess 20 nm	891	-0.95 V/-1.15 V	$3.67e^{12}$

TABLE 4.12 – Summary of the different C(V) results obtained through Schottky and MIS structures, with and without gate recess etching.

In the same manner as with increasing the oxide layer thickness, $1/C_{tot}$ should vary linearly with the barrier thickness t_b as again predicted in equation 2.17. That can be confirmed in figure 4.36.

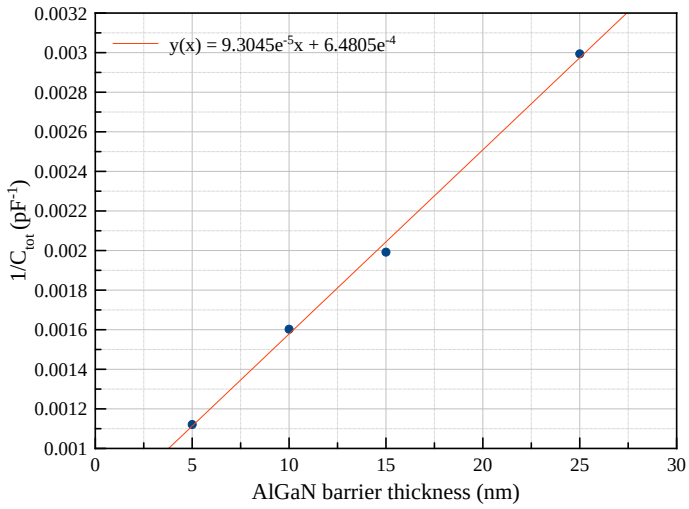

FIGURE 4.36 – $1/C_{tot}$ evolution depending on barrier thickness

4.7.1.2 $I_d(V_g)$ results on circular transistor with L_g=100μm

Regarding the $I_d(V_g)$ measurements, similar results were achieved through the use of gate recess etching, again without degradation of performance. This can be seen in figure 4.37.

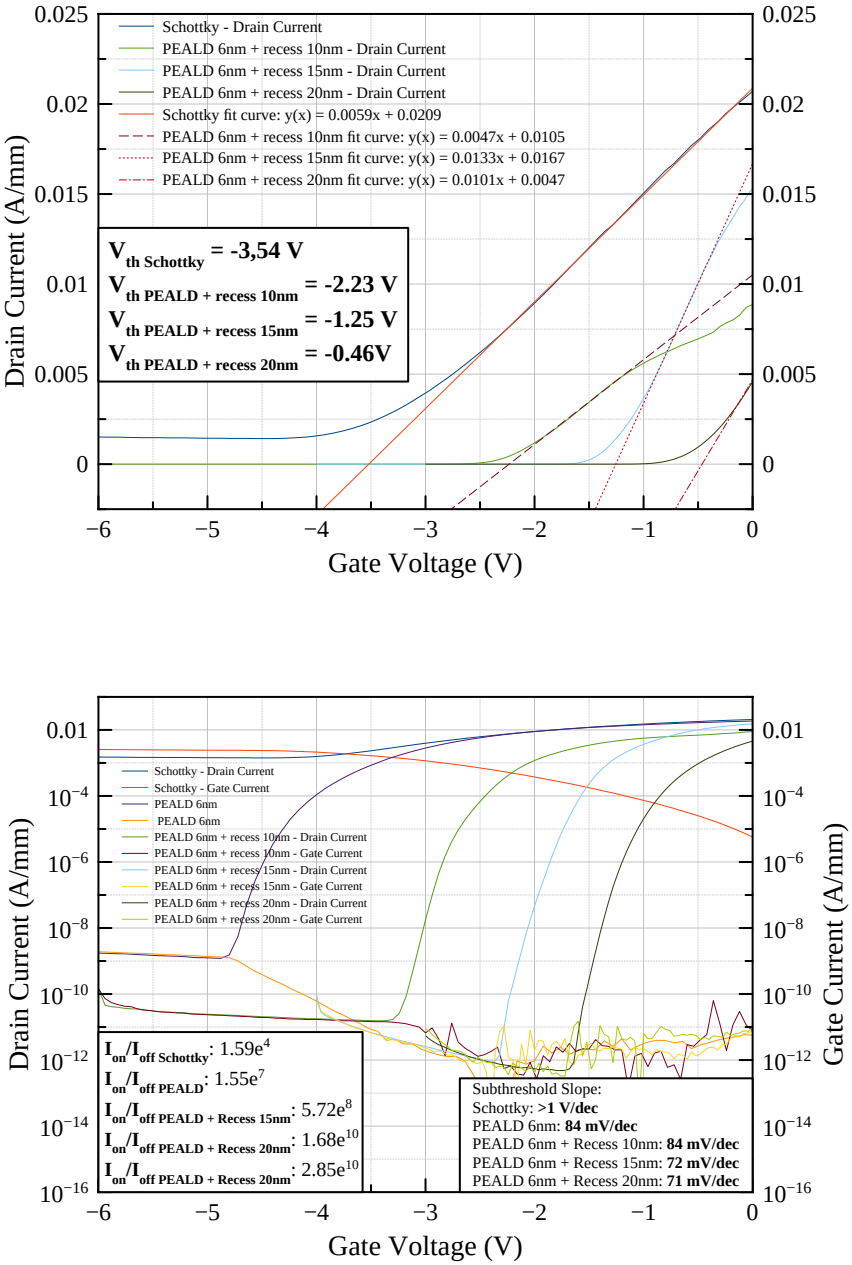

FIGURE 4.37 – Linear (up) and logarithmic (down) $I_d(V_g)$ response for a PEALD MIS on a circular transistor after different recess etchings. The Al_2O_3 thickness is 6 nm and $V_{DS} = 5$ V.

While the increase in V_{th} is not fully linear when going from the reference MIS structure to the one with a 10 nm recess, the increase can be considered linear when looking at the three recessed structures with a 0.7 V increase every 5 nm recessed. Again, we find that the further the recess, the higher the threshold voltage increase, and the lower the gate leakage current. We were thus able to achieve gate leakage currents as low as 10^{-12} A.mm^{-1} in the case of the 20 nm recess, for a record I_{on}/I_{off} ratio of 10^{10}. We can see that the reference Schottky sample is again very leaky, thus confirming what we already obtained on the C(V) characteristic. Table 4.13 summarizes the different results obtained through the use of the gate recess etching.

Samples	V_{th}	n_S (cm^{-2})	I_{on}/I_{off}	Subthreshold slope
Schottky	-3,54 V	7.12e^{12}	1.59e^{1}	>1 V/dec
MIS 6 nm	-4.24 V	6.65e^{12}	1.55e^{7}	84 mV/dec
MIS 6 nm + recess 10 nm	-2.23 V	4.79e^{12}	5.72e^{8}	84mV/dec
MIS 6 nm + recess 15 nm	-1.25 V	5.06e^{12}	1.68e^{10}	72mV/dec
MIS 6 nm + recess 20 nm	-0.46 V	3.67e^{12}	2.85e^{10}	71mV/dec

TABLE 4.13 – Summary of the different $I_d(V_g)$ results obtained through Schottky and MIS structures, with and without gate recess etching.

4.7.1.3 Threshold voltage evolution

In the case of recess etching, theory predicted that the threshold voltage should vary linearly with the AlGaN barrier thickness. This was confirmed and is illustrated in figure 4.38. We were thus able to verify equation 2.22, with again the possibility to extract the different elements of the equation from the fit curve obtained. Again, with only a few points, the fit is quite good but it would be nice to verify for more recess values. However, the AlGaN barrier thickness is here a limiting factor since it is only 25 nm thick. Again, this thickness was measured through calculating the equivalent thickness seen in equation 4.6, to which the 6 nm of the Al_2O_3 insulating layer was subtracted.

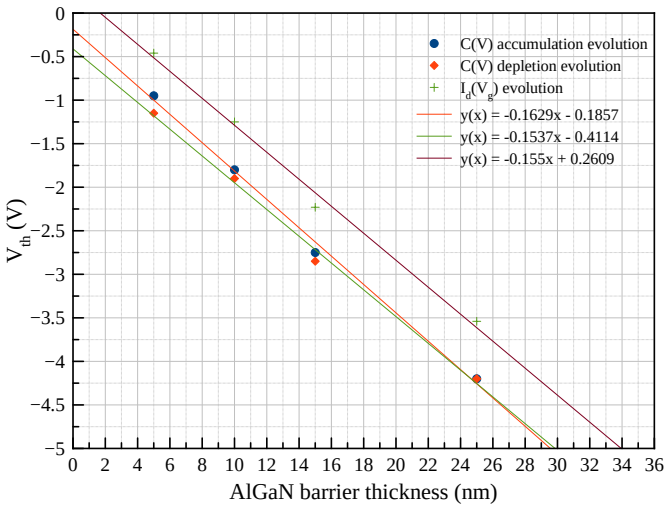

FIGURE 4.38 – V_{th} evolution depending on barrier thickness

4.7.2 AlGaN Full-recess etching below gate

In view of the very good results obtained through the use of gate recess etching combined with PEALD, a full recess was performed in order to see whether it is possible or not to achieve a normally-off behavior. As such, the full barrier was etched, followed by a 20 nm Al_2O_3 PEALD deposition. Figure 4.39 illustrates the obtained results for $I_d(V_g)$ measurements.

As we can see, it was possible to obtain a positive threshold voltage of 2.2 V with a relatively simple device processing method. Furthermore, the good insulating properties that were previously achieved were maintained, with very low gate leakage current and a good I_{on}/I_{off} ratio of 10^7. As for the subthreshold slope, it diminished a little but is still at a very good 80 mV/dec.

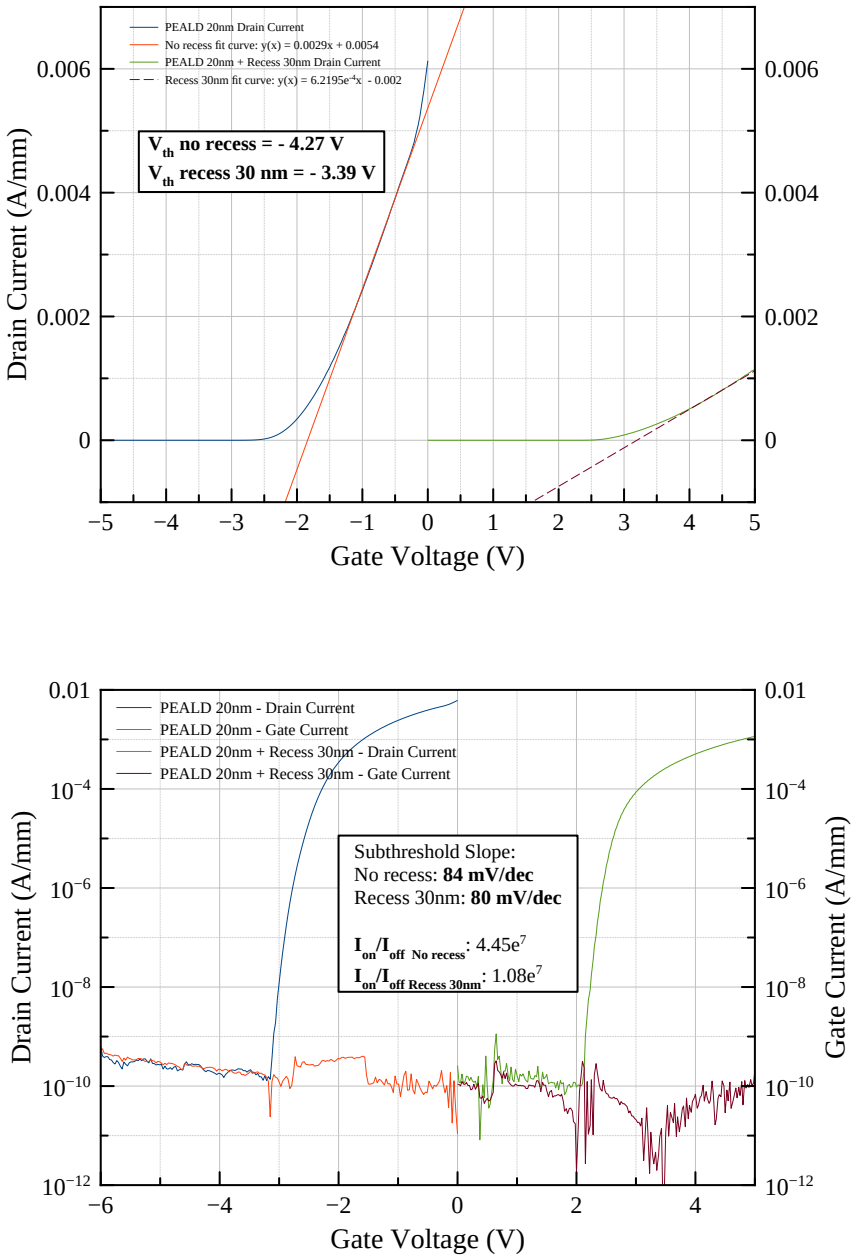

FIGURE 4.39 – Linear (up) and logarithmic (down) $I_d(V_g)$ response for a PEALD MIS on a circular transistor after a full recess etch below the gate. The Al_2O_3 thickness is 20 nm and $V_{DS} = 5$ V.

It is important to notice that gate leakage current levels were unaffected through the process, staying at 10^{-10} A.mm^{-1}. Only the current at the on state was reduced by one order of magnitude at 1 mA.mm^{-1}. While the subthreshold slope underwent a an amelioration, we can affirm that a full recess etching has indeed an impact on the devices, but still allows to achieve viable normally-off devices.

The best explanation towards understanding the light degradation in the performances is the roughness increase that was generated while performing the recess. Even if ICP-RIE is a very gentle way of etching, it is likely that it has nonetheless an impact on the surface, and in case of a full recess, on GaN. One possible solution could be to use a TMAH at high temperature chemical treatment, which has be proved successful in restoring surface smoothness after an etching process (mettre référence). While it was tried, this process proved to complicated to achieve within PTA once ohmic contacts were made, the TMAH strongly attacking the latter and damaging the sample in an unrecoverable way.

4.8 Conclusion

Through all of this Ph.D, multiple results have been obtained and be outlined and discussed here.

The first striking element is the apparent superiority of the PEALD MIS structure over Schottky devices. While very good results have been achieved on Schottky devices (mettre références), it is important to take into account the context in which the devices were created. Even with the excellent equipment and the evolution of processing techniques, it remains very difficult to achieve good results on Schottky devices. The need of using passivation techniques arises, and the control over the surface must be much higher than for MIS devices. In this Ph.D, all the samples were made in a small clean room, where variability in processing cannot be controlled. It was almost impossible in PTA to ensure that the sample would not get contaminated between to steps, while passivation and its associated constraints

revealed a challenge far to difficult to achieve in a not fully-controlled environment.

Another fact to keep in mind is that though Schottky devices, if not processed with utmost care, tend to have higher gate leakage current levels, but they still remain more robust compared to MIS-structures, especially in stressful condition. At higher voltage, the oxide in a MIS insulated device will break once its limit is reached, rendering the device virtually useless. In the Schottky device however, once the breakdown voltage is reached, it will still be possible to use the device, albeit some degradation in its properties. So while MIS devices are easier to process, they are more fragile and one must be very careful when manipulating them, if one does not want to permanently damage them.

Lastly, in this Ph.D, while good results were achieved, it is still important to take a few steps back in order to realize that not everything is as good as it seems. For example, samples degraded over time if not conserved under strict conditioning (vacuum ideally), which led to the impossibility to measure the same results on the samples again after some time. Another drawback of the MIS, and more specifically of Al_2O_3, is its relative weakness to high electric fields. Those tend to destroy the oxide, thus making it useless once breakdown is reached. In this study, measurements were only made in favorable conditions, at low voltages, in order to avoid such problem. One solution could be to increase the thickness of the oxide layer, at the expanse of lowering the threshold voltage. One could also change the gate oxide, using for example HfO_2 which is much more resistant to high electric field and can even be combined with alumina through Al_2O_3/HfO_2 latices.

Another solution to achieve higher breakdown voltages would be the use of field plates, over the source, the gate or the drain. Such architecture were used at CEA-Leti on the 200 mm line process. They probably represent to date one of the best solutions to achieve viability by improving the performances without having to oversize components, while keeping a relatively simple architecture.

General conclusion

As was exposed at the beginning of this Ph.D., we have seen the necessity of switching from silicon to wide band gap materials for power converting technologies in order to respond to the current market needs. While they may necessitate further improvements still, the advantage they present are considerable and would prove a credible solution in order to limit energy losses. A lot of applications necessitating power conversion are already in use, and with new challenges coming up ahead, their numbers are bound to increase even more in the years to come. More specifically, high voltage (>1000 V) and high current (>100 A) supporting components can not be achieved with silicon devices due to the material's limitations, which leaves an opening for materials such as GaN and SiC to supply for those needs. And though growth of GaN on Si by MOCVD still needs further improvement, mostly in order to reduce dislocation levels, current state of research combined to the ability to process it on large wafers makes it an economically viable alternative. Should we manage to improve it sufficiently, its inherent superior properties could pave the way to a brand new era for power electronics. With current density, voltage withstanding, critical operating temperature and commutation frequency at high levels, HEMTs on GaN could become the spearhead of the power industry.

The present study approached a way to reduce losses by reducing gate leakage current levels, without degrading the switching quality of the transistor, through the introduction of an insulating layer between the gate and the AlGaN barrier.

In this Ph.D., the main focus was precisely on the development and optimization of that insulating layer that composes a MIS-HEMT. Alumina was the insulator that was selected and the used to create the different devices, mainly because of its high availability and ease of use within the seminconductor industry, and also because it is a native oxide to AlGaN.

What first appeared, is that interface quality between AlGaN and Al_2O_3 plays a key role in achieving a good insulation. Though it could not be put into place due to processing restrictions, chemical surface treatments using NH_4OH at high temperature proved to be a very efficient way in order to remove native oxide contamination. While N-containing plasma treatments led to good results regarding surface regeneration, the degradation they generated in terms of electrical results makes them devoid of practical interest. This was probably due to the roughness increases seen with AFM, which deteriorated the oxide/barrier interface, most probably by creating surface traps.

Regarding the use Al_2O_3 as a gate insulator, the obtained results were varying depending on the deposition method. Using water a oxidizer in the ALD process proved to be greatly inefficient, with poor results due to a bad AlGaN/Al_2O_3 interface. Detachment at the edges induced erratic behavior, and leakage levels were still too high to consider it a good candidate. However, it is important to keep in mind that this could be the consequence of working in a small clean room like the PTA where cross contamination due to other users is highly likely to happen.

Things improved dramatically when deposition method was switched to PEALD. Though as predicted the threshold voltage was shifted towards the negative biases, the gain in performance was nothing short of astonishing. In capacitance measurements, C(V) transitions were sharp and clean with no N_s degradation, proving very stable even at frequency as low as 1 kHz. As for the gate leakage current, it was reduced by several orders of magnitude, ensuring a very good I_{on}/I_{off} ratio of 10^{10} with a record subthreshold slope of 74 mV/dec. When reducing the alumina

thickness, those very good properties were conserved, with of course a slight degradation in leakage current levels. Staying under 100 mV/dec, the subthreshold slope remained quite good ensuring a fast transition from the off to the on state, even with only 25 cycles of PEALD. Regarding V_{th} evolution, it seemed to follow the predicted theory. The only drawback to this deposition technique is the time it takes to deposit : the oxidation step is 30 seconds long with oxygen plasma, whereas a pulse of water lasts only a few milliseconds. This could be a problem for large scale application.

The behavior difference between the two deposition techniques could be attributed to interface quality. Indeed, AFM analysis has showed that with only a few cycles of PEALD, AlGaN regained its natural terrace like aspect. Similarly, an oxygen plasma pre-treatment led to the same recuperation. It can be deducted from this observation that PEALD, through the use of O_2 plasma as oxidizer, cleaned the surface of the AlGaN barrier in the first cycles of the deposition process. This has most probably led to a better AlGaN/Al_2O3 interface, with fewer surface or oxide traps.

Finally, while post deposition thermal treatment proved a bad solution in order to increase the threshold voltage, gate recess etching produced tremendously good results. It was possible to greatly increase the threshold voltage, without degrading the insulating properties of the structure. Very fast transitions between the on and off state were also kept intact, and leakage levels were even reduced. However, a slight hysteresis was induced in the C(V) measurements. This could be explained by the fact that while ICP is a gentle approach to recess etching, it still might have increased the surface roughness, thus leading to behavior degradation.

All in all, even if processing conditions were not optimal, I was able through this Ph.D to achieve a very robust process, easily put into place and leading to very good results. Reproducibility was very high and always procured consistent electrical results, even when the quality of the wafers were unpredictable due to the lack of information. For example, even with a badly leaking Schottky diode

on the CEA wafer, PEALD insulation proved very efficient and led to very solid and good quality devices, with good performance capability. While the alumina sensitivity to photolithography developers was quite tricky, it was resolved through a challenging and original way of a chromium protective layer, without adding much complexity to the overall process, and particularly without compromising the structure integrity. Furthermore, availability of the all the different equipments on-hand at PTA or CIME ensured a full autonomy and fast processing capability, with only a few steps having to be made on the silicon platform.

Perspectives

The first perspective to improve this work would be to implement the cleaning steps that were studied at the beginning of chapter 4. Multiple studies have shown that surface contamination, such as a bad quality native oxide or carbon, are drawbacks to the device performance. Likewise, surface regeneration after recess etching using TMAH could be tested and eventually implemented in the device process.

The second one would be to make batches with different thicknesses of insulating layer, with and without recess. This would allow to find an optimum in electrical behavior and could definitely confirm the threshold voltage evolution towards both aspects. Another very interesting perspective would be to change the nature of the insulating layer. While this study was focused on alumina, it would be nice to see how the device behave with other materials. As such, hafnium oxide would be a strong candidate since it has higher electrical breakdown capabilities.

The last and overall most important perspective of this work, would be to make pulsated electrical measurements. This technique is widely used for power componenets and would allow to measure dynamic response of the transistor. Whether it be at high or low biases, these measurements could highlight important phenomenons such as R_{ON} degradation and trapping effects that occur, in the oxide or at the interface [42], [43], [44], [45]. Interface state density D_{it} and oxide charge density Q_{ot} could thus be evaluated, depending on parameters such off state polari-

zation bias and traps excitation frequency. Those types of measurement are crucial in power applications and it is especially true for GaN HEMTs ref a mettre. They would have to be implemented on a more conventional device than the circular transistors that were used. This would ensure the robustness of the developed process and assess the quality of the interface between AlGaN and PEALD deposited Al_2O_3, and would pave the way for its large scale application.

It has also been mentioned multiple times that electrical properties of HEMTs in general are greatly dependent on the insulating properties of the substrate buffer layers. Multiple studies have event shown that parasitic conduction phenomenons in the substrate could lead to dynamic R_{ON} degradation [46], [47]. As such, varying the buffer architectures would prove invaluable.

Bibliographie

[1] TransphormUSA. Transphormusa. *http ://www.transphormusa.com/gan-technology/.*

[2] AS Kyuregyan and SN Yurkov. Room-temperature avalanche breakdown voltages of p-n junctions made of Si, Ge, SiC, GaAs, GaP, and InP. *Soviet Physics–Semiconductors(English Translation)*, 23(10) :1126–31, 1989.

[3] T.P. Chow and Ritu Tyagi. Wide bandgap compound semiconductors for superior high-voltage unipolar power devices. *Electron Devices, IEEE Transactions on*, 41(8) :1481–1483, Aug 1994.

[4] Tatsuhiko Fujihira. Theory of semiconductor superjunction devices. *Japanese journal of applied physics*, 36(10R) :6254, 1997.

[5] A Nakagawa, Y Kawaguchi, and K Nakamura. Silicon limit electrical characteristics of power devices and Ics. 2008.

[6] B Ozpineci and LM Tolbert. *Comparison of wide-bandgap semiconductors for power electronics applications.*

[7] B.J. Baliga. *Modern power devices.* A Wiley-Interscience publication. Wiley, 1987.

[8] Stephen J Pearton, Cammy R Abernathy, and Fan Ren. *Gallium nitride processing for electronics, sensors and spintronics.* Springer Science & Business Media, 2006.

[9] Yasumasa Okada and Yozo Tokumaru. Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K. *Journal of Applied Physics*, 56(2) :314–320, 1984.

[10] Michael E Levinshtein, Sergey L Rumyantsev, and Michael S Shur. *Properties of Advanced Semiconductor Materials : GaN, AIN, InN, BN, SiC, SiGe.* John Wiley & Sons, 2001.

[11] Michael Shur, Michael Levinshtein, and Sergey Rumyantsev. *SiC materials and devices.* World Scientific, 2006.

[12] Yong Cai, Zhiqun Cheng, W.C.W. Tang, Kei May Lau, and K.J. Chen. Monolithically integrated enhancement/depletion-mode algan/gan hemt inverters and ring oscillators using CF_4 plasma treatment. *Electron Devices, IEEE Transactions on*, 53(9) :2223–2230, Sept 2006.

[13] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. *Journal of Applied Physics*, 85(6) :3222–3233, 1999.

[14] I. P. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra. AlN/GaN and (Al,Ga)N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy. *Journal of Applied Physics*, 90(10) :5196–5201, 2001.

[15] R. Coffie, Y.C. Chen, I. Smorchkova, M. Wojtowicz, Y.C. Chou, B. Heying, and A. Oki. Impact of AlN interalayer on reliability of AlGaN/GaN hemts. In *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International*, pages 99–102, March 2006.

[16] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra. Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors. *Applied Physics Letters*, 77(2) :250–252, 2000.

[17] G. Koley, Ho-Young Cha, C. I. Thomas, and M. G. Spencer. Laser-induced surface potential transients observed in III-nitride heterostructures. *Applied Physics Letters*, 81(12) :2282–2284, 2002.

[18] G. Koley and M. G. Spencer. On the origin of the two-dimensional electron gas at the AlGaN/GaN heterostructure interface. *Applied Physics Letters*, 86(4) :–, 2005.

[19] Luke Gordon, Mao-Sheng Miao, Srabanti Chowdhury, Masataka Higashiwaki, Umesh K Mishra, and Chris G Van de Walle. Distributed surface donor states and the two-dimensional electron gas at AlGaN/GaN heterojunctions. *Journal of Physics D : Applied Physics*, 43(50) :505501, 2010.

[20] Masataka Higashiwaki, Srabanti Chowdhury, Mao-Sheng Miao, Brian L. Swenson, Chris G. Van de Walle, and Umesh K. Mishra. Distribution of donor states on etched surface of AlGaN/GaN heterostructures. *Journal of Applied Physics*, 108(6) :–, 2010.

[21] M. S. Miao, J. R. Weber, and C. G. Van de Walle. Oxidation and the origin of the two-dimensional electron gas in AlGaN/GaN heterostructures. *Journal of Applied Physics*, 107(12) :–, 2010.

[22] D. Delagebeaudeuf, P. Delescluse, P. Etienne, M. Laviron, J. Chaplart, and Nuyen T. Linh. Two-dimensional electron gas M.E.S.F.E.T. structure. *Electronics Letters*, 16(17) :667–668, August 1980.

[23] Takashi Mimura, Satoshi Hiyamizu, Toshio Fujii, and Kazuo Nanbu. A new field-effect transistor with selectively doped GaAs/n-$Al_xGa_{1-x}As$ heterojunctions. *Japanese Journal of Applied Physics*, 19(5) :L225, 1980.

[24] Y.-F. Wu, B.P. Keller, S. Keller, D. Kapolnek, S.P. DenBaars, and U.K. Mishra. Measured microwave power performance of AlGaN/GaN MODFET. *Electron Device Letters, IEEE*, 17(9) :455–457, Sept 1996.

[25] S. Fanget and C. Bru-Chevalier. *Matériaux et hétérostructures à base de nitrures d'éléments III en phase cubique et hexagonale pour l'optoélectronique.* PhD thesis, INSA LYON, 2002.

[26] Kanjalochan Jena, Raghunandan Swain, and Trupti Ranjan Lenka. Modeling and comparative analysis of DC characteristics of AlGaN/GaN HEMT and MOSHEMT devices. *International Journal of Numerical Modelling : Electronic Networks, Devices and Fields*, pages n/a–n/a, 2015.

[27] J. Robertson and B. Falabretti. Band offsets of high K gate oxides on III-V semiconductors. *Journal of Applied Physics*, 100(1) :–, 2006.

[28] M. Asif Khan, Q. Chen, C. J. Sun, J. W. Yang, M. Blasingame, M. S. Shur, and H. Park. Enhancement and depletion mode GaN/AlGaN heterostructure field effect transistors. *Applied Physics Letters*, 68(4) :514–516, 1996.

[29] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura. Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications. *Electron Devices, IEEE Transactions on*, 53(2) :356–362, Feb 2006.

[30] R. Vetury, N.Q. Zhang, Stacia Keller, and Umesh K. Mishra. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. *Electron Devices, IEEE Transactions on*, 48(3) :560–566, Mar 2001.

[31] Tamotsu Hashizume and Hideki Hasegawa. Effects of nitrogen deficiency on electronic properties of AlGaN surfaces subjected to thermal and plasma processes. *Applied Surface Science*, 234(14) :387 – 394, 2004. The Ninth International Conference on the Formation of Semiconductor Interfaces,.

[32] Fernando González-Posada, Jennifer A Bardwell, Simona Moisa, Soufien Haffouz, Haipeng Tang, Alejandro F Brana, and Elías Muñoz. Surface cleaning and preparation in AlGaN/GaN-based HEMT processing as assessed by X-ray photoelectron spectroscopy. *Applied surface science*, 253(14) :6185–6190, 2007.

[33] Rakesh Sohal, Piotr Dudek, and Oliver Hilt. Comparative study of NH_4OH and HCl etching behaviours on AlGaN surfaces . *Applied Surface Science*, 256(7) :2210 – 2214, 2010.

[34] M.-F. Romero, A. Jimenez, F. Gonzalez-Posada Flores, S. Martin-Horcajo, Fernando Calle, and E. Munoz. Impact of N_2 Plasma Power Discharge on AlGaN/GaN HEMT Performance. *Electron Devices, IEEE Transactions on*, 59(2) :374–379, Feb 2012.

[35] A.P. Edwards, J.A. Mittereder, S.C. Binari, D.S. Katzer, D.F. Storm, and J.A. Roussos. Improved reliability of AlGaN-GaN HEMTs using an NH_3 plasma treatment prior to SiN passivation. *Electron Device Letters, IEEE*, 26(4) :225 – 227, 2005.

[36] M.F. Romero, A. Jimenez, J. Miguel-Sanchez, A.F. Brana, F. Gonzalez-Posada, R. Cuerdo, F. Calle, and E. Munoz. Effects of N_2 Plasma Pretreatment on the SiN Passivation of AlGaN/GaN HEMT. *Electron Device Letters, IEEE*, 29(3) :209 –211, 2008.

[37] Feng Qian, Tian Yuan, Bi Zhi-Wei, Yue Yuan-Zheng, Ni Jin-Yu, Zhang Jin-Cheng, Hao Yue, and Yang Lin-An. The improvement of Al2O3/AlGaN/GaN MISHEMT performance by N_2 plasma pretreatment. *Chinese Physics B*, 18(7) :3014, 2009.

[38] Ji Ha Kim, Hong Goo Choi, Min-Woo Ha, Hong Joo Song, Cheong Hyun Roh, Jun Ho Lee, Jung Ho Park, and Cheol-Koo Hahn. Effects of Nitride-Based Plasma Pretreatment Prior to SiNx Passivation in AlGaN/GaN High-Electron-Mobility Transistors on Silicon Substrates. *Japanese Journal of Applied Physics*, 49(4) :04DF05, 2010.

[39] S. W. King, J. P. Barnak, M. D. Bremser, K. M. Tracy, C. Ronning, R. F. Davis, and R. J. Nemanich. Cleaning of AlN and GaN surfaces. *Journal of Applied Physics*, 84(9) :5248–5260, 1998.

[40] Richard Lossy, Hassan Gargouri, Michael Arens, and Joachim Würfl. Gallium nitride MIS-HEMT using atomic layer deposited Al_2O_3 as gate dielectric. *Journal of Vacuum Science & Technology A*, 31(1) :01A140, 2013.

[41] O. Saadat and T. Palacios. Low temperature gate dielectric deposition for recessed AlGaN/GaN MIS-HEMTs. *Solid-State Device Research Conference (ESSDERC)*, pages 287 – 291, 2011.

[42] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry. Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy. *Applied Physics Letters*, 79(21) :3527–3529, 2001.

[43] Steven C Binari, Kiki Ikossi, Jason A Roussos, Walter Kruppa, Doewon Park, Harry B Dietrich, Daniel D Koleske, Alma E Wickenden, and Richard L Henry. Trapping effects and microwave power performance in AlGaN/GaN HEMTs. *Electron Devices, IEEE Transactions on*, 48(3) :465–471, 2001.

[44] Ramakrishna Vetury, Naiqain Q Zhang, Stacia Keller, and Umesh K Mishra. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. *Electron Devices, IEEE Transactions on*, 48(3) :560–566, 2001.

[45] Giovanni Verzellesi, Gaudenzio Meneghesso, Alessandro Chini, Enrico Zanoni, and Claudio Canali. DC-to-RF dispersion effects in GaAs-and GaN-based heterostructure FETs : performance and reliability issues. *Microelectronics Reliability*, 45(9) :1585–1592, 2005.

[46] Davide Bisi, Matteo Meneghini, Marleen Van Hove, Denis Marcon, Steve Stoffels, Tian-Li Wu, Stefaan Decoutere, Gaudenzio Meneghesso, and Enrico Zanoni. Trapping mechanisms in GaN-based MIS-HEMTs grown on silicon substrate. *physica status solidi (a)*, 212(5) :1122–1129, 2015.

[47] Gaudenzio Meneghesso, Matteo Meneghini, Enrico Zanoni, Piet Vanmeerbeek, and Peter Moens. Trapping induced parasitic effects in GaN-HEMT for power switching applications. In *IC Design & Technology (ICICDT), 2015 International Conference on*, pages 1–4. IEEE, 2015.