# Lateral porous silicon membranes for planar microfluidic applications

Yingning He

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# Lateral Porous Silicon Membranes for Planar Microfluidic Applications

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*The mass of a body is a measure of its energy content.*

Albert Einstein

*As heaven maintains vigor through movement,*
*a gentleman should constantly strive for self-perfection!*

I Ching

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# Introduction

Microfluidics consists in manipulating minute amount of liquid samples most frequently by means of microchannels. This field has emerged with the promise to greatly and mainly impact biological analysis and chemical synthesis, especially with the advent of miniaturized total chemical analysis systems (µTAS) and lab-on-a-chip that take advantage of the possibility to include and efficiently perform several functions routinely encountered in chemical/medical laboratories on a single chip.

Porous silicon has lately been considered as a material of choice and interest for microfluidics due to its intrinsic properties, *e.g.* tunable pore size and porosity, large active area, and convenient surface chemistry. It was first proposed as a sacrificial layer for the fabrication of fluidic channels, but quickly its high porosity, its biocompatibility and its reflectance properties were exploited for the realization of functional elements integrated into lab-on-chip, paving the way towards all-in-one answer in continuous fluidics for *e.g.* on-chip sample preparation and sensing for diagnosis applications.

Porous silicon membranes are always created perpendicular to the substrate surface. To integrate such membranes into microfluidic devices, the current integration techniques consist in sandwiching fabricated membranes between two encapsulating layers that bear the micro/nano fluidic channels, resulting in three-dimensional fluidic networks that lack the simplicity of operation and direct observation accessibility of planar microfluidic devices.

To tackle these drawbacks, this thesis work aims at proposing means to fabricate lateral porous silicon (LPSi) membranes and to integrate them into 2D planar fluidics. To this aim, we propose two original fabrication processes. The proposed approaches are based on the formation of pores tubes that are parallel to the substrate surface, thus connecting inlet and outlet microchannels lying in the same plane. The first method is based on the use of locally patterned electrodes to guide pore formation horizontally within the membrane in combination with silicon-on-insulator (SOI) substrates to spatially localize the porous silicon within the channel depth. The second method relies on the fact that the formation of porous silicon by anodization is highly dependent on the dopant type and concentration. While we still use electrodes patterned on the membrane sidewalls to inject current for anodization, the doping via implantation enables to confine the membrane analogously to but instead of the SOI buried oxide box. After successfully fabricating lateral porous silicon membranes using the two processes, we investigate the possibility to use these porous membranes for various applications: size-based filtering in lab-on-chip, pre-concentration of molecules by ion concentration polarization through the ion selectivity property of the lateral porous membranes and finally the possibility to carry out interferometry biosensing analogously to vertical membranes but in a flow-through configuration.

The dissertation consists of 4 chapters. Chapter 1 presents the background and motivation of our work that involves the study of porous silicon membranes for microfluidic applications. Chapter 2 describes two novel fabrication processes that enable the monolithic integration of lateral porous silicon membranes into planar microfluidics. Chapter 3 studies the ion selectivity properties of the fabricated membranes and the possibility to carry out on-chip sample preconcentration by means of ion concentration polarization. Chapter 4 concerns the transducing ability of lateral porous silicon membranes using optical interferometry.

# Chapter 1.

# Porous silicon and microfluidics

*In this chapter, we present the background and motivation of our work that involves the study of porous silicon membranes for microfluidic applications. To this aim, we first introduce porous silicon and present its unique properties that make it attractive for many fields of application ranging from optoelectronics to biomedicine. We focus on the various microfluidic applications of porous silicon that is mainly used in the form of membranes, and we then detail the various fabrication processes used to create porous silicon membranes. We discuss means of membrane integration within microfluidic systems that always result into three-dimensional microfluidics vs. planar lab-on-chips. We finally present the objective of this work that consists in developing fabrication processes for the creation of porous silicon membranes with lateral pores for their monolithic integration into planar microfluidics.*

## 1. Presentation of porous silicon

Porous silicon (PSi) is defined as a bulk semiconducting material, silicon (normally crystalline), that includes a network of voids. Porous silicon was accidentally discovered by the Uhlirs, a husband and wife team at Bell labs in the 1950s, when they were trying to develop an electrochemical method of machining silicon wafers for its use in microelectronics. They found that, under specific electrochemical conditions, the silicon wafer did not dissolve uniformly as expected, but instead fine holes appeared [1]. The regime turns out to be a selective dissolution of silicon in hydrofluoride acid (HF) using a relatively low electric current.

The discovery of porous silicon did not attract much attention until the 1970s, when the high surface area was found to be useful in FTIR spectroscopic studies [2, 3]. Around the same time, porous silicon was used as a dielectric layer for capacitance-based chemical sensor [4]. In the early 1990s, the quantum confinement effects were discovered by Ulrich Goesele [5] at Duke University and Leigh Canham [6] at the British Defense Research Agency almost simultaneously. Since then, a big amount of work has focused on creating silicon-based optoelectronic devices. In the mid-1990s, the unique properties of this material, such as large surface area, controllable pore dimensions and density, convenient surface chemistry and biocompatibility, inspired a boost of research into medical and biological applications.

## 2. Properties of porous silicon

### 2.1. Surface area and porosity

Compared to bulk silicon, porous silicon exhibits very large surface area due to the presence of voids into the material. The porosity is the fraction of the total pore volume to the apparent volume. For PSi materials with the same pore size, the higher porosity, the larger the surface area. The large surface area is one of the significant features of porous silicon that leads to more chemical reaction sites for surface chemistry. Besides, porous silicon biosensors normally rely on immobilization of bioreceptors to the PSi surface, followed by biorecognition event between bioreceptor and its biological analyte. The large surface area of porous silicon enables an effective capture of the analyte, leading to high sensitivity of the biosensor [7].

High porosity, which means large void volume, is very important for drug delivery because it determines the maximum drug ‘payload’ of the porous material [8]. Furthermore, there is excellent work using porous silicon as a template to create polymer replicas for drug delivery and sensing applications [9]. It was also discovered that the high porosity of porous silicon promotes solubility in biological media [10], which is useful for biomedical applications such as drug delivery and tissue engineering. Current fabrication techniques have enabled convenient control of porosity, normally ranging from 5% to 95% [11]. Images of PSi with different porosities are shown in Figure 1. The change of porosity has a dramatic effect on some properties of porous silicon, such as optical (refractive index) [12] and thermal isolation properties [13].

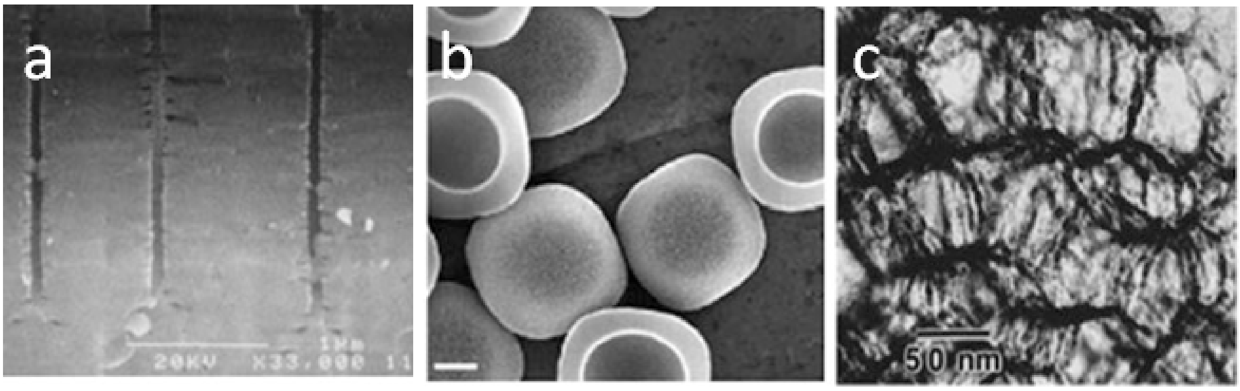


Figure 1. Low- to high-porosity silicon structures. (a) <5% macroporous wafer [11]. (b) microfabricated ~60% mesoporous microparticles [8]. (c) ~95% mesoporous ‘aerocrystal’ formed by silicon anodization with supercritical drying [14].

### 2.2. Pore size (diameter)

Based on the definition from the International Union of Pure and Applied Chemistry (IUPAC), pore size is classified into three regimes: micropores (<2 nm), mesopores (2–50 nm) and macropores (>50 nm). The control of pore size can be achieved with multiple fabrication processes such as silicon anodization and micromachining. Taking silicon anodization for example [15], the pore size can be controlled by monitoring the applied current density and the HF concentration of the anodization bath: increase of current density or decrease of the HF concentration will lead to an increase of pore size. Besides, the pore size is highly dependent on dopant type and concentration: p-type silicon tends to form micropores; highly doped p+, p++ , or n+ wafers normally yields to mesopores, and n-type silicon normally creates macroporous silicon.

The feature of controllable pore size is very useful for size exclusion-based applications. Figure 2 shows the size of different biomolecules/biological entities in comparison to the porous silicon pore size classification. This implies that porous silicon can be used as to separate biological samples based on their sizes [16]. In addition, the excellent biocompatibility of porous silicon makes it an ideal material for immunoisolation [17].

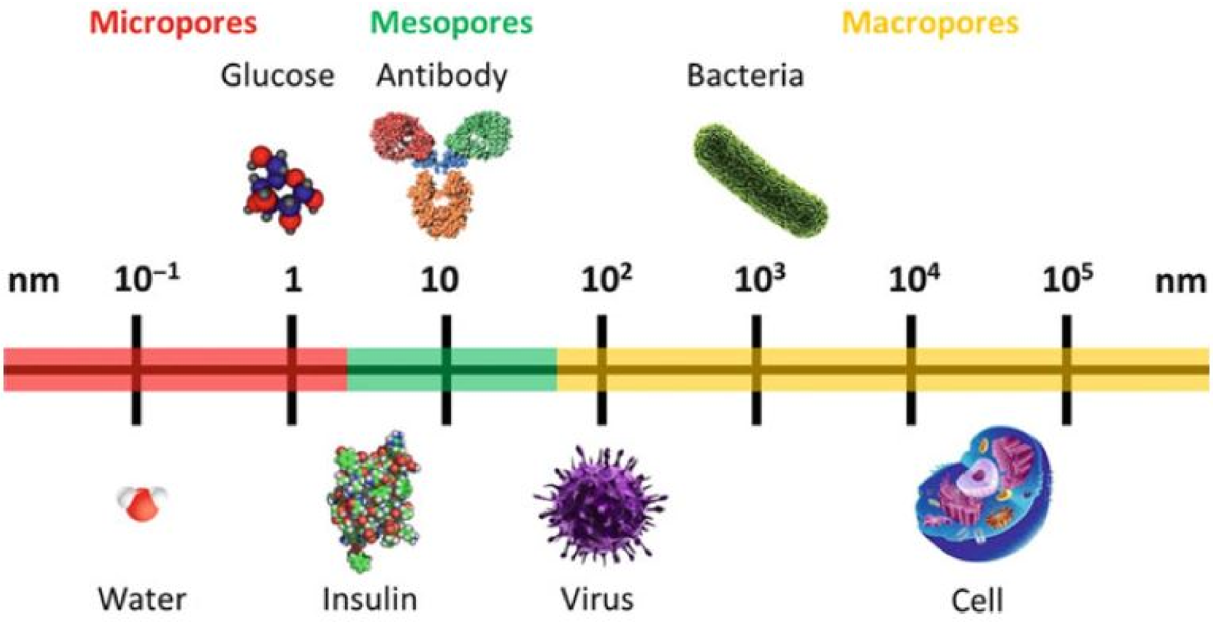


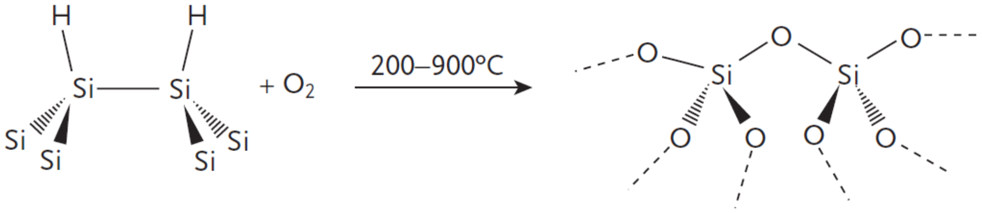
Figure 2. Size of different biomolecules and biological entities versus pore size classification [11].

### 2.3. Surface chemistry

The properties of porous silicon can conveniently be modified by tuning the surface chemistry according to the needs. Porous silicon slowly dissolves in aqueous solution due to the reductive nature of silicon surface, leading to the destruction of porous structure. This is a critical limitation for porous silicon optical biosensors because the aqueous corrosion leads to zero drift, which reduces their ultimate sensitivity. To solve this problem, oxidation processes, such as ozone oxidation [18] can be used to significantly improve the stability of porous silicon.

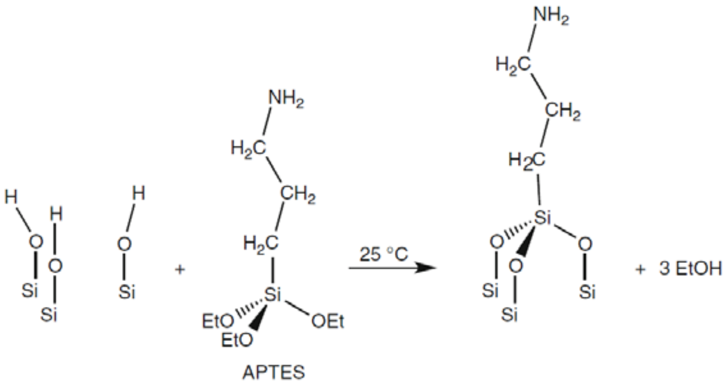
The reactivity of as-formed porous silicon is dominated by the chemistries of silicon-hydrogen (Si-H) and silicon-silicon (Si-Si) bonds, which are strong reducing agents. The surface chemical reactions mainly involve the formation of silicon-oxygen (Si-O), silicon-carbon (Si-C), and silicon-nitrogen (Si-N) bonds.

Si-O bonds enhance the aqueous stability, the electrical insulation property and the electrical double layer thickness of PSi surfaces. The formation of Si-O bonds can be achieved by various oxidation processes, such as thermal oxidation, chemical oxidation and electrochemical oxidation. Thermal oxidation is a commonly used to completely turn Si-H and Si-Si bonds into Si-O bonds by hot air or oxygen following [15]:



(1)

Chemical oxidation can be carried out by means of mild chemical oxidants, such as ozone [19] and dimethyl sulfoxide [20], which tends to produce thin oxide layers. Electrochemical oxidation is the electrochemical anodization of porous silicon in mineral acid such as aqueous $H_2SO_4$ that yields a fairly stable oxide [21]. Oxidized porous silicon can be further modified by the chemical protocols used to modify silica or glass surfaces due to a similar surface chemistry. One of the popular coupling reactions is salinization with 3-aminopropyltriethoxysilane (APTES), which results in reactive $–NH_2$ groups on the PSi surface [22]:

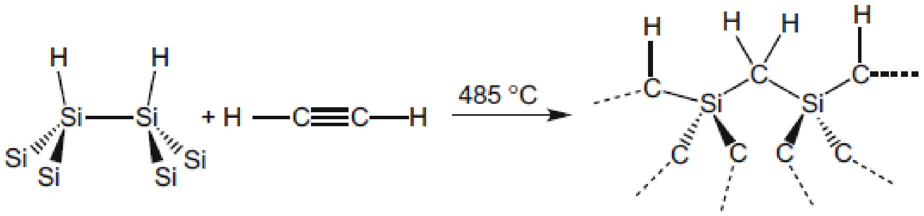


(2)

APTES is commonly used to link molecules such as proteins [23] and DNA [24] to porous silica for biological applications.

Si-C modified porous silicon surfaces show greater aqueous stability than that of Si-O bonds due to the lower electronegativity of C relatively to O [25]. The formation of Si-C bonds is normally done by hydrosilylation [26], electrochemical grafting [27] and carbonization [28].

Hydrosilylation reaction involves the addition of Si-H bond across C-C double or triple bonds (such as alkene and alkyne). Electrochemical grafting consists in covalently replacing Si-H bonds by saturated compounds (such as alkyl- or aryllithium reagents) with electrochemical assistance. Hydrosilylation and electrochemical grafting introduce a wide variety of organic functional groups on PSi surfaces. However, all Si-H bonds are not completely removed during these processes and are then susceptible to aqueous dissolution. By contrast, carbonization involves the decomposition and the partial pyrolysis of acetylene gas on a porous silicon sample, creating very stable 'hydrocarbonized' porous silicon with full surface coverage [28]:



(3)

Silicon nitride ($Si_3N_4$) is used as a common etch stop and dielectric layer in integrated circuit manufacture. Its refractive index is larger than $SiO_2$ (2.0 vs. 1.5, respectively), making porous silicon nitride an attractive alternative for optical device. Porous silicon can be nitrided by heating in $NH_3$ or $N_2$ ambient or by plasma-assisted CVD. A typical nitridation involves heating in pure $N_2$ at 1100 °C for 12 min [29]. However, high temperature preparation tends to create thick nitride films that decrease pore size, porosity, and surface area, analogously to plasma-assisted CVD that deposits nitride films into the pores. In contrast, a low temperature (520 °C) process has been developed using rapid thermal annealing with pure $N_2$ [30]. The $N_2$-based annealing process improves the stability of PSi samples, while preserving the porous structure.

The reducing ability of porous silicon also works with many metal ions, where the reactions involved are silicon oxidation and reduction of metal ions to their element states [31]:

$$\mathrm{Si} + 2\mathrm{H_2O} \rightarrow \mathrm{SiO_2} + 4\mathrm{H^+} + 4\mathrm{e^-} \qquad (4)$$

$$M^{n+} + ne^{-} \rightarrow M \tag{5}$$

As a result, porous silicon is a promising template for preparation of metal micro- and nanostructures. The resulting porous silicon-metal hybrid materials improve the luminescent property [32], magnetic property [33] and catalytic activity [34] of porous silicon.

### 2.4. Biocompatibility and biodegradability

The biocompatibility of porous silicon is critical for its biomedical applications. Biocompatibility refers to the ability of a material to perform with an appropriate host response in a specific situation [35]. A biocompatible material would have little or no toxic properties, and it should not induce violent host immune response. With its high reductive surface, porous silicon is unstable in aqueous environment and is readily degraded into orthosilicic acid ($Si(OH)_4$) [36]. The silicic acid is nontoxic and is the common form of bioavailable silicon in the human body [37]. *In vivo* experiments showed that implanted PSi membranes only induced a small amount of inflammation and was gradually degraded within weeks [38]. In fact, the biodegradability and the speed of dissolution of PSi can be easily controlled by the porosity and surface modification. Based on these facts, porous silicon is a good biocompatible material enabling its use both *in vivo* applications for therapy and diagnostics and *in vitro* application for biosensing and biofiltration.

Porous silicon has also been proved to be bioactive, which makes this material a suitable scaffold for tissue engineering [10].

### 2.5. Optical and luminescence properties

Porous silicon shows very interesting optical and luminescence properties leading to applications in several fields, ranging from micro-optics and optoelectronics to biosensing and biomedicine. The optical properties of a porous silicon layer are determined by its thickness and refractive index that depends on the layer porosity and the shape and size of the pores. Furthermore, the refractive index of PSi also depends on the relative volumes of silicon (porosity) and pore-filling medium [11]. A specific medium filling the pores (*e.g.*, gases and solutions) or binding/adsorption to the pore walls (*e.g.*, biomolecules and chemicals) results in a given index of refraction. Any change in medium or surface coverage results in a change of refractive index, which can be detected by reflectance-based transducers: in the most simple and common configuration, a PSi layer on silicon substrate is illuminated with white light perpendicular to the sample surface (Figure 3). The reflection of the incident light at the top and bottom of the PSi layer results in an interference spectrum, which is detected by a spectrometer.

A typical method to analyze the interference spectrum is to compute the frequency spectrum of an input waveform by fast Fourier transform (FFT). The FFT process yields a peak whose position along the x-axis corresponds to the effective optical thickness (EOT) which depends on the refractive index and thickness of the PSi layer. When the surface of the PSi layer is functionalized with bioreceptors, any biorecongnition event between the bioreceptor and its analyte results in a change of refractive index, which can be detected and quantified by the interference and FFT spectra. This mechanism was widely used for the detection of DNA [39], protein [40], enzyme activity [41] and bacteria [42].

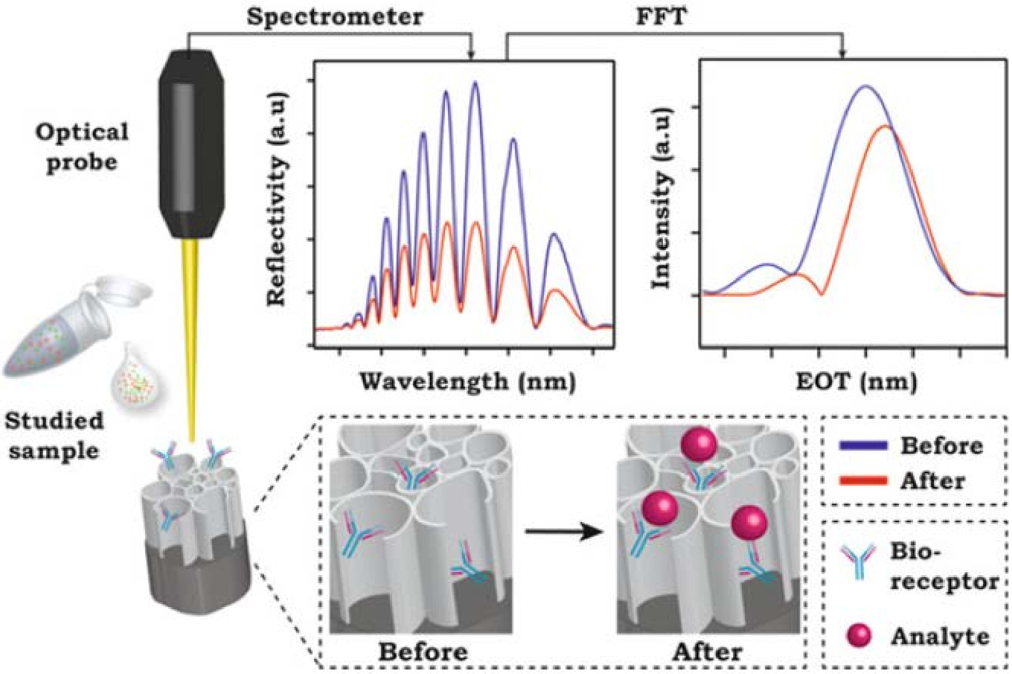


Figure 3. A schematic illustration of a reflectivity-based biosensor based on a single-layer PSi film and the sensing concept [11].

Porous silicon is a material allowing the realization of porous structures with periodic variations in refractive index. Figure 4a shows the linear relationship between the refractive index and the porosity of PSi which can be conveniently controlled by various microfabrication techniques. Figure 4b shows an example of PSi multilayer structure consisting of high porosity layers (low refractive index) separated by low porosity layers (high refractive index) obtained by electrochemically etching boron-doped silicon with alternating applied current densities.

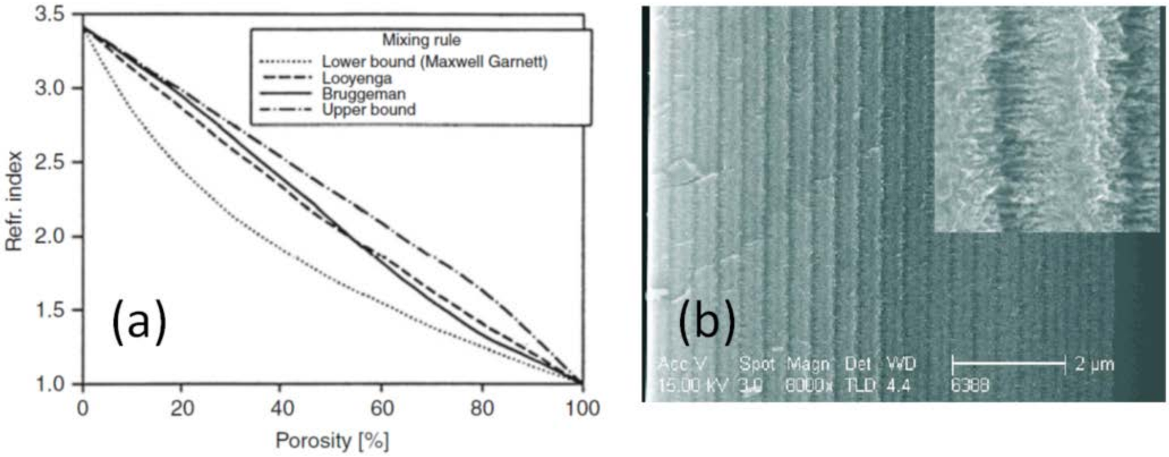


Figure 4. (a) Refractive index (real part) versus porosity, determined by different effective medium approaches (Maxwell–Garnett's, Looyenga's, and Bruggeman's) [43]. (b) Cross-sectional SEM image of PSi omnidirectional mirrors [44].

Since the refractive index determines how light travels through a medium, PSi structures can be precisely designed in the form of PSi photonic crystals to control the propagation of light. Using appropriate fabrication parameters, PSi-based photonic structures can be realized with a required width and location of the photonic bandgaps with one-dimensional (1D) [45], two-dimensional [46], and three-dimensional [47] periodic dielectric lattices. 1D structures are easy to fabricate and have been widely studied for sensing and photonic applications. The architectures that have been frequently studied are: double layer, Bragg mirror, micro-cavity and rugate filter. Figure 5 presents these structures made of porous silicon fabricated using various current density waveforms and their corresponding representative spectra. Similar to the single-layer optical biosensors, these multilayer structures can also be employed for sensing or biosensing based on reflectance-based interferometry [48-50], providing sharp spectral features and improved sensitivity. While most reflectance-based interferometers use bulk porous silicon layers, Sailor's team has developed porous silicon particles for the detection of chemicals, so called 'Smart Dust' [51]. PSi-based 1D photonic crystals were also used in various micro-optic devices, such as perfect mirror [44], image detector [52], negative refractor [53] and optical switch [54].

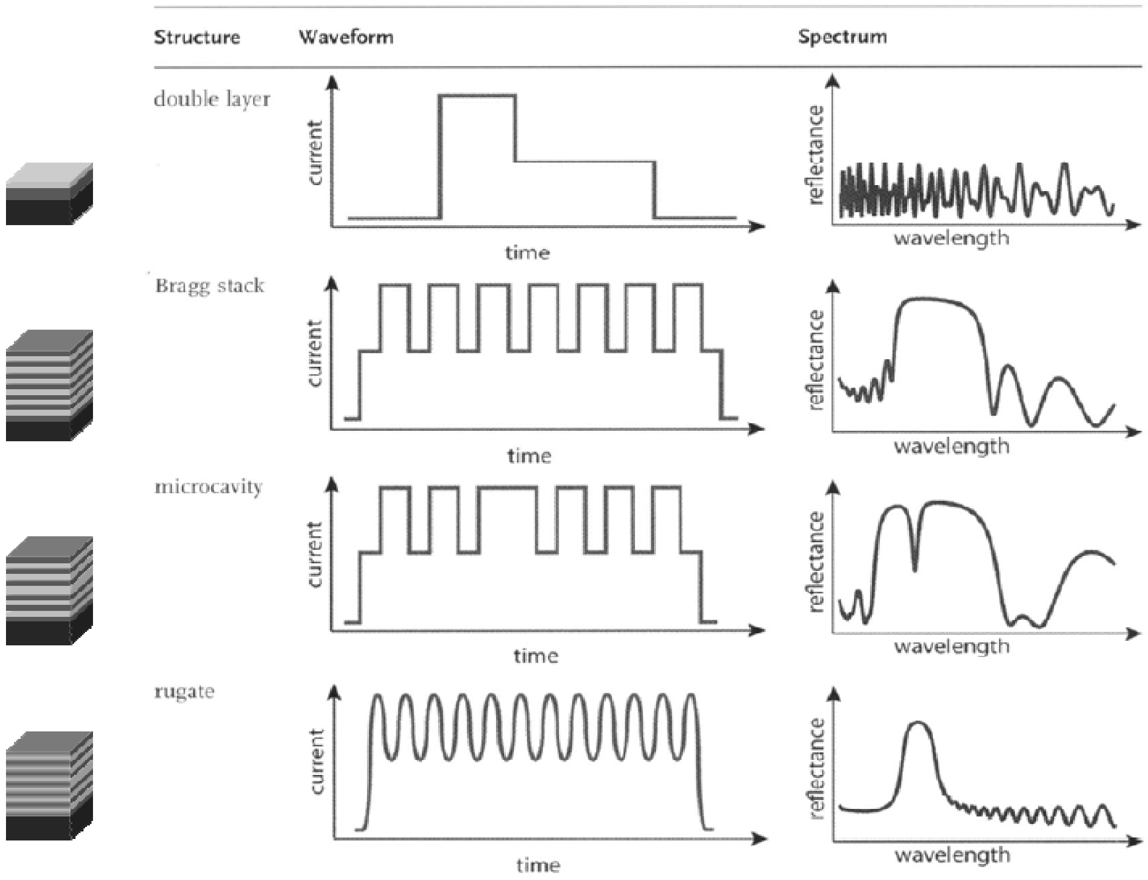


Figure 5. Porous silicon based 1D photonic crystals prepared with porous silicon including the approximate current density waveforms used for their fabrication and corresponding representative spectra [15].

Porous silicon possesses remarkable luminescence properties (*e.g.*, photoluminescence and electroluminescence) due to quantum confinement effects. However, the biggest challenges of PSi-based luminescence devices are luminescence efficiency and stability. In recent years, the photoluminescence (PL) quantum efficiency has reached more than 60% [55] and the PL stability was greatly promoted by surface modification [56].

The photoluminescence properties have been utilized for biosensing by exciting a sample and observing changes in the PL spectrum of PSi when affected by an analyte [57]. For example, the PL emission is quenched by the binding of molecules at the surface of PSi nanostructures due to energy-transfer [58].

Porous silicon has been discovered to have photosensitization and photoexcitation properties. Combining the advantages of its large surface area and good biocompatibility, porous silicon is considered as a good material for photodynamic and photothermal therapy. Mesoporous silicon is used in photodynamic therapy to generate oxygen species under illumination to kill nearby cells [59]. The PSi-based photothermal therapy uses near-infrared light-induced overheating (above 40–41°C) to kill the cancer cells without chemical toxicity. *In vivo* experiments suggest that the PSi-based photothermal therapy is rather efficient to selectively destroy cancer cells without damaging the surrounding healthy cells [60].

### 2.6. Electrical and thermal properties

Porous silicon was found very early on to exhibit electrical resistivities 5 orders magnitude higher than that of intrinsic silicon [61]. The electrical properties (capacitance and conductance) are remarkably influenced by the filling of chemical compounds in the pores. Capacitance-based vapor sensors have been developed based on the change of effective permittivity upon vapor condensation within the pores [4, 62]. Conductance-based gas sensors are based on the fact that the conductivity of porous silicon varies exponentially with the dipole moment of the filling gas [63].

Porous silicon has excellent thermal insulation properties. Although single crystalline silicon has a very high thermal conductivity comparable with metals, porous silicon has much lower thermal conductivity and heat capacity. As expected, the thermal conductivity decreases with the increase of porosity. At porosity around 90%, the thermal conductivity reaches 0.03 W/mK, which is over three orders of magnitude lower than the value of bulk c-Si [64]. The exceptional low thermal conductivity of highly porous silicon has led to its use as a thermal insulator within microsystems. For example, in a thermal flow sensor, thermopiles and heater are placed on porous silicon for thermal insulation [65].

## 3. Porous silicon and microfluidics

Microfluidics consists in manipulating minute amount of liquid samples most frequently by means of microchannels. This field has emerged in the 1980s with the promise to greatly and mainly impact biological analysis and chemical synthesis [66], especially with the advent, ten years later, of miniaturized total chemical analysis systems (µTAS) and lab-on-a-chip that take advantage of the possibility to include and efficiently perform several functions routinely encountered in chemical/medical laboratories on a single chip [67].

Due to its intrinsic properties, *e.g.* tunable pore size and porosity, large active area, convenient surface chemistry, porous silicon has lately been considered as a material of choice and interest for microfluidics. Porous silicon was first proposed as a sacrificial layer for the fabrication of fluidic channels [68], but quickly its high porosity, its biocompatibility and its reflectance properties were exploited for the realization of functional elements integrated in lab-on-chip, paving the way towards all-in-one answer in continuous fluidics for *e.g.* on-chip sample preparation and sensing for diagnosis applications, but also providing new solutions for digital fluidics. This section provides a quick survey of the various works where porous silicon is used for microfluidics applications.

### 3.1. On-chip filtration

In filtration, porous membranes acts as physical barriers where fragments larger than the pore size are prevented from entering the pores, while the rest of the fluid pass through the membrane by external forces (*e.g.* pressure, electrophoresis or electroosmosis) [69]. Among the materials used to make membranes, porous silicon membrane holds several advantages for filtration applications: (1) it has a narrow pore size distribution for filtering reliability; (2) its high porosity can lead to high fluid throughput for high filtering efficiency. PSi membranes for on-chip filtration were used for separation of cells from whole blood [70, 71], for sorting molecules according to their size differences [16, 72, 73], and for removal of particles in air [74]. Figure 6 shows an example of on-chip filter based on a PSi membrane. The porous silicon membrane was created via anodization right through a thin silicon membrane (Figure 6a). The membrane chip was sandwiched between two PDMS layers with inlet/outlet and flow channels. Filtering tests were conducted by flowing test solution of fluorescent polystyrene microspheres through the porous membrane: as shown in Figure 6c, the microspheres were completely filtered by the membrane.

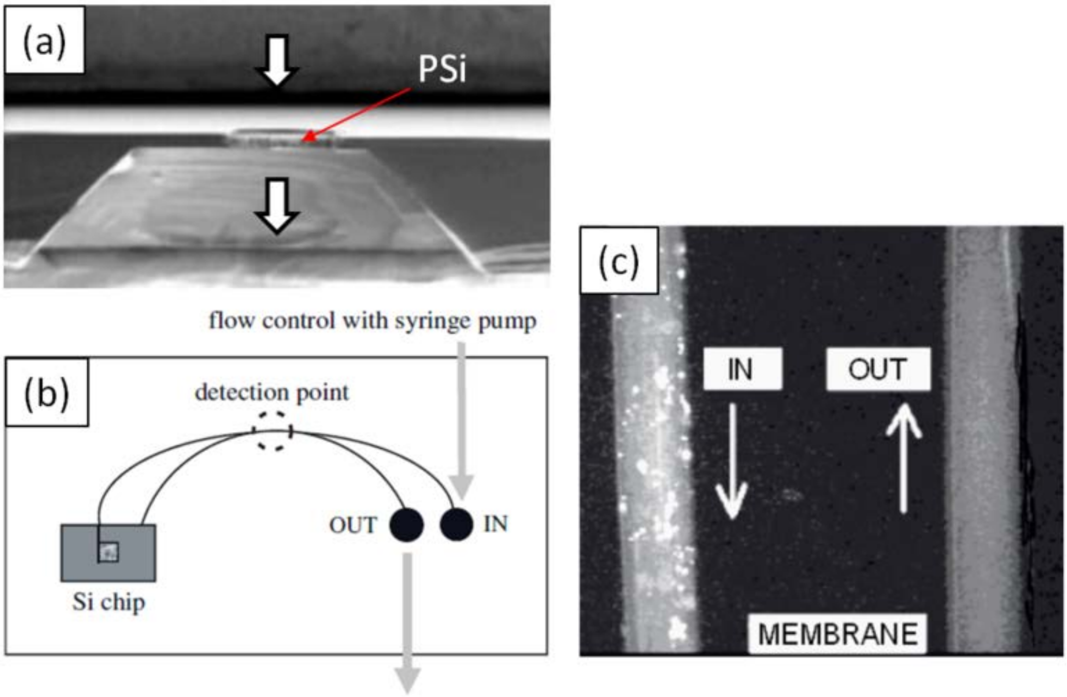


Figure 6. (a) SEM picture of the cross section (slightly tilted) of the filter with 1-mm backside opening and 300-µm front side membrane. (b) Filtration of polystyrene microspheres with porous membrane: a sketch of PDMS layers with Si chip between. (c) Fluorescence microscope picture of sample flow through inlet / outlet channels. [72]

### 3.2. On-chip separation

Aside for its filtration capability, porous silicon was also used in separation science. Figure 7 shows an example of porous silicon used to increase the retention capacity of stationary phase for shear-driven chromatography (SDC) [75, 76]. Porous silicon layers with very large porosities (~85%) can be exploited to obtain large stationary phase mass transfer rates. The effect of the porous layer was demonstrated by the strong increase in zone retention factor as compared to the reference mono-layer coated channel system. Porous silicon was also grown onto channel walls to create solid phase matrix for solid-phase extraction [77], and to insulate channel walls for on-chip electrophoresis [78].

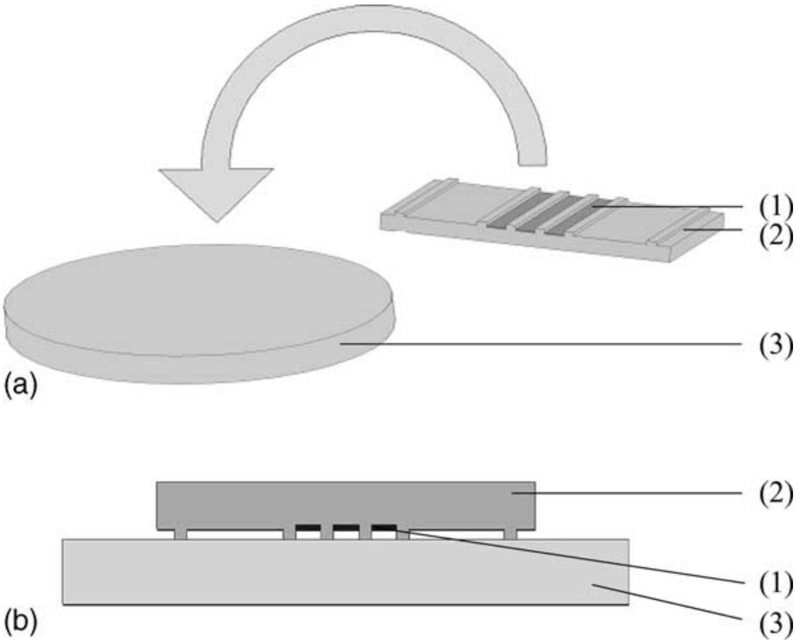


Figure 7. Schematic diagram of the employed channel system of shear-driven chromatography, consisting of a movable, ultra-flat fused-silica plate (3) and a silicon plate (2) carrying the porous silicon retentive layer (1). (a) Prior to the device assembly (bird's-eye view) and (b) after assembly (cross-sectional view). [75]

### 3.3. Biosensors

As stated in the previous section, one of the most interesting features of porous silicon is that it can be used for biosensing via reflectance-based interferometry [79], provided it is adequately functionalized with probe molecules. Porous silicon biosensors have been integrated into hybrid fluidics (flow cells) to enable real-time sensing [80]. A similar integration approach was taken with porosified fluidic channels used as biosensors [81, 82]. A higher level of integration was achieved by sealing the fluidic channel incorporating the porous silicon sensor with a glass cover [83, 84]. A similar strategy has allowed the integration of porous silicon sensor arrays in a single PDMS fluidic chip [85, 86].

### 3.4. Electroosmotic pumps

Taking advantage of their large surface/volume ratios, insulated porous silicon membranes have been demonstrated to be very promising for the realization of efficient electroosmotic pumps [87]. These pumps, allowing high flow rates with no moving parts, have been fabricated from macroporous silicon [88] and ultrathin nanocrystalline silicon membranes [89]. Figure 8 shows a schematic of an example of a porous silicon-based pump. Upon application of an electric field, an electroosmotic flow is induced in the porous membrane because of the pore surface charges.

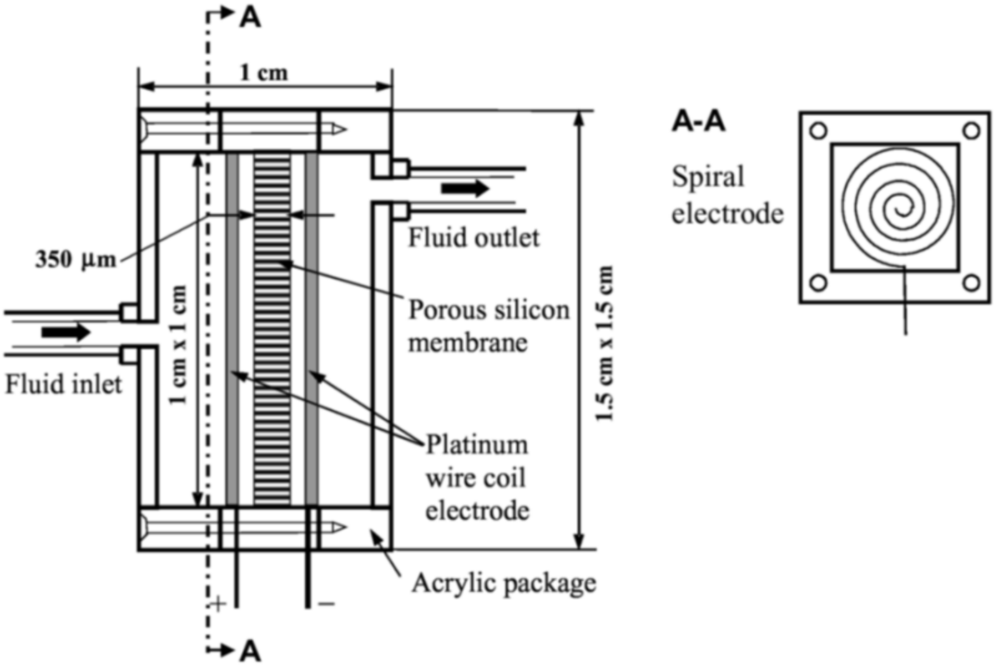


Figure 8. Schematic of porous silicon electroosmotic pump assembly and the spiral electrode configuration [87].

### 3.5. Microreactors

The large surface/volume ratio has also been the reason to use porous silicon for making efficient reactors. Examples can be found where porous silicon formed onto fluidic channel walls was used to increase the efficiency of enzyme reactors used in combination with mass spectrometry for protein analysis [90] and for enzyme kinetics [91]. Microreactors based on porous silicon were also used for gas pre-combustion [92] and gas pre-concentration [93]. Picoliter circular reaction chambers made of silicon and porosified using multi-scale lithography and cryogenic deep reactive ion etching techniques were fully integrated into a fluidic chip to conduct biochemical reactions [94]. Finally, the inner walls of silicon reaction chambers were porosified in order to improve the cell adhesion and biocompatibility [95, 96].

## 4. Fabrication of porous silicon membranes

Porous silicon for microfluidics applications is usually found in two configurations: porous silicon grown onto channel wall (silicon substrate) and porous silicon membranes. Porous silicon membranes are very useful for transport-related applications, such as on-chip filtration and electroosmotic pumps. Porous silicon membranes could provide promising solutions for on-chip sample preparation (*e.g.* filtration and concentration) within future lab-on-a-chip devices for clinical diagnostic and point-of-care applications. However, the fabrication of porous silicon membranes is complicated and limited mainly because of the difficulties in opening both sides of the membrane to the fluid. In this section, we present the various methods available for the fabrication of both porous silicon channels and porous silicon membrane.

### 4.1. Introduction to PSi fabrication

Various techniques developed during the last 50 years are available for the fabrication of porous silicon. Fabrication techniques can be generally classified into two routes: the 'top-down' and the 'bottom-up' approach [97]. The top-down route consists in creating pores within solid silicon (by means of *e.g.* electrochemical etching). On the other hand, the bottom-up route is based on the use of silicon atoms and silicon-based molecules to build up porous silicon (by *e.g.* sintering silicon powder).

#### 4.1.1. Top down fabrication techniques

'Top-down' fabrication techniques include electrochemical etching (anodization), photoetching, stain etching, metal-assisted etching, and lithography-assisted etching.

Electrochemical etching is the most common fabrication method of porous silicon. It relies on the local oxidation of silicon, due to the injection of holes, which is subsequently etched by HF [15]. Figure 9 shows a classical electrochemical etch cell, in which electrochemical reactions occur at both electrodes. Porous silicon formation happens at the silicon electrode (called 'working electrode'), where anodic dissolution of silicon in fluoride-containing solutions follows the oxidation reaction presented in the diagram of Figure 9. The cathode used in porous silicon etching cells is usually platinum, where hydrogen gas is produced from the reduction of protons.

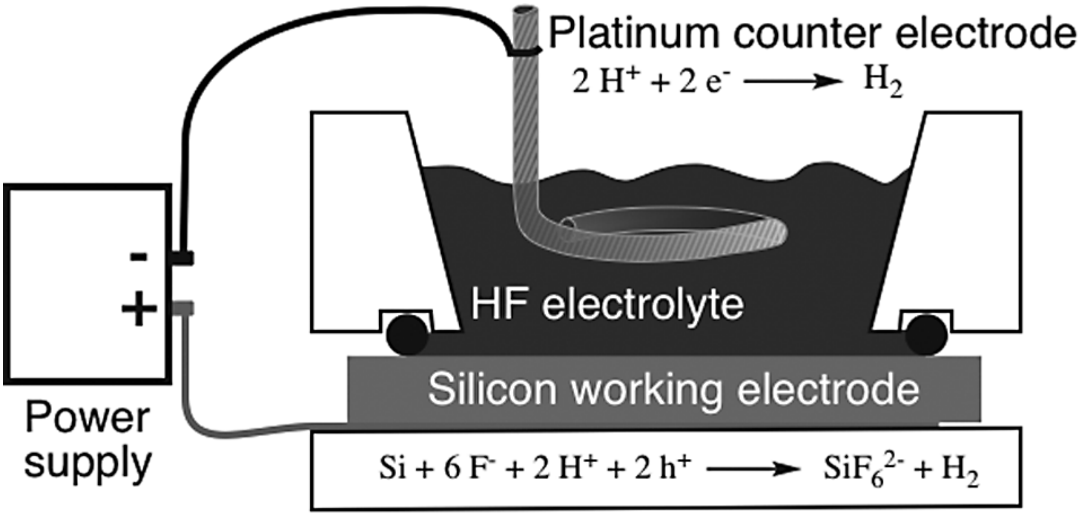


Figure 9. Schematic of a classical electrochemical etch cell used to make porous silicon [15].

In some situations, the supply of holes by electric current is not convenient or possible, *e.g.* for low doped n-type silicon that lacks carriers. In these cases, holes can be generated by illumination during the etching process, named photoetching [98].

In addition to using electric current and illumination as sources of holes, carriers can also be generated using chemical oxidants (stain etching and metal-assisted etching). Stain etching is the spontaneous electrodeless etching of silicon surface with chemical oxidants (*e.g.*, $HNO_3$ or $V_2O_5$) in HF solutions [99]. Metal-assisted etching is also based on the local oxidation and dissolution of silicon in HF with the presence of an oxidizing agent, where the metal (generally a noble metal) catalytically enhances the etching process [100].

Taking advantage of high-resolution microfabrication techniques, porous silicon can be created using masking layers deposited onto silicon substrates and patterned by lithography, followed by dry etching of silicon [101]. Porous silicon can also be fabricated by means of thermal-related processes where thermal effects assist the formation of pores within the silicon substrate. For example, a proper thermal annealing of ultrathin amorphous silicon layer results in the formation of pores due to the volume contraction from crystallization [16]. Another example of thermal-related fabrication processes is laser ablation where local heat induces the partial evaporation of the silicon substrate [102].

### 4.1.2. Bottom up fabrication techniques

‘‘Bottom-up’’ fabrication techniques include chemical conversion, mechanical means and deposition-based fabrication.

The chemical conversion technique is the chemical reduction of silicon-based molecules (*e.g.* porous silica) to silicon, such as magnesiothermic reduction. There are plenty of natural porous silica raw materials, such as stone and rice husk. As a result, the porous silica reduction is a promising and inexpensive route for the massive production of porous silicon. On the other hand, this approach enables the use of interesting structures of natural materials. For example, Bao et al [103] have converted diatom frustule into microporous silicon structures that show excellent photoluminescence and gas sensing properties (Figure 10). The mechanical means use high energy ball milling to create silicon powders, followed by pressing and sintering process for the formation of porous matrix [104]. This approach may create large-shaped porous structures for biomedical applications, such as tissue engineering scaffolds. Deposition-based fabrication is the production of porous silicon by controlling silicon deposition parameters. Instead of obtaining a dense layer, pores can be formed in the deposited layer by tuning the deposition conditions [105].

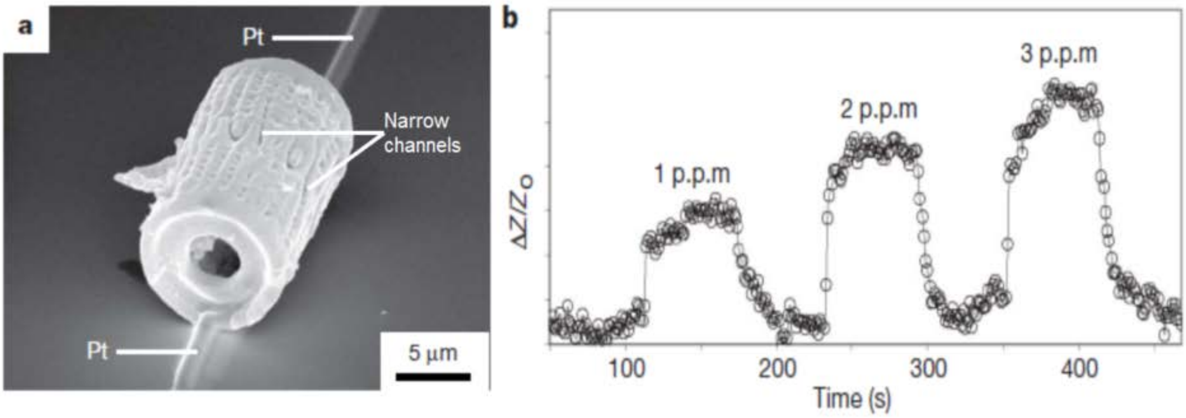


Figure 10. Gas sensor based on a silicon frustule replica [103]. (a) SEM image of a microporous silicon frustule replica, both ends of which were connected by platinum electrodes for obtaining electrical signal. (b) Electrical response of this single silicon frustule sensor to NO gas.

## 4.2. Review of fabrication approaches of PSi membranes

Although plenty of fabrication processes lead to the formation of porous silicon, routes to fabricate porous silicon membranes are quite limited. In this section, we describe the three top-down techniques usually used to realize porous silicon membranes from solid silicon: silicon anodization, micromachining, and film deposition/annealing.

### 4.2.1. Silicon anodization

Silicon anodization is the most common approach to fabricate porous silicon membranes. Since the porous silicon has to be open on both sides of the membrane to fluids, usually an additional process is done to 'separate' the membrane from the silicon substrate. In this section, we have classified the silicon anodization approach for membrane fabrication into three categories according to this additional process.

#### 4.2.1.1. One-step anodization

Anodization right through an entire silicon wafer is the most straightforward approach to fabricate macroporous silicon membranes since membranes are obtained in a single step. Figure 11 shows an example of such fabrication process where membranes are obtained by means of a sacrificial layer: the fabrication is carried out in a double-tank etch cell; the device sample (p-type silicon) and the sacrificial sample are first loaded into the etch cell and the electrolyte is pumped through both chambers; the anodization is then performed by injecting current through the Pt electrodes placed in each tank. The sacrificial sample is used to ensure that the pores are all open-ended on the backside of the device sample. The etch-through technique is available for both n- and p-type silicon wafers [106, 107]. This technique is suitable for wafer-scale processes that create large-area and thick macroporous membranes.

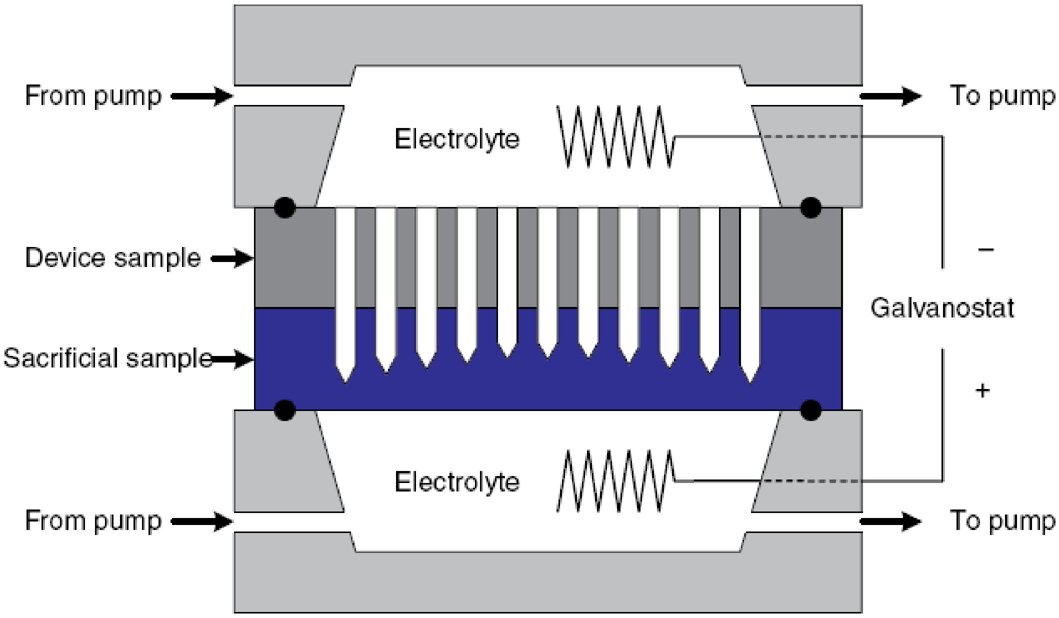


Figure 11. Schematic drawing of the etching setup used for macroporous membrane formation [106].

#### 4.2.1.2. Two-step anodization

The two-step anodization fabrication process includes a first anodization step to create porous silicon within a substrate followed by another anodization step to remove the bulk silicon on the backside of the membrane. There are two ways to etch away the backside bulk silicon: (1) create a cavity under the membrane by electropolishing; (2) create a sacrificial layer under the porous silicon membrane that is subsequently removed by chemical etchant.

In the mechanism of silicon anodization, silicon atoms can be removed from the substrate selectively (porosification) or isotopically (electropolishing) depending on the supply rate of holes (current density) and fluoride ions (HF concentration), as shown in Figure 12a. The electropolishing mode can be triggered by simply increasing the current density during the anodization, so it is possible to create a cavity under the formed porous silicon layer by electropolishing. However, the electrochemical etching direction follows the current flow lines, resulting in the lift-off the membrane from the substrate (Figure 12b). Therefore, a supportive material that is resistive to electrochemical etching is needed to hold the porous silicon membrane above the cavity.

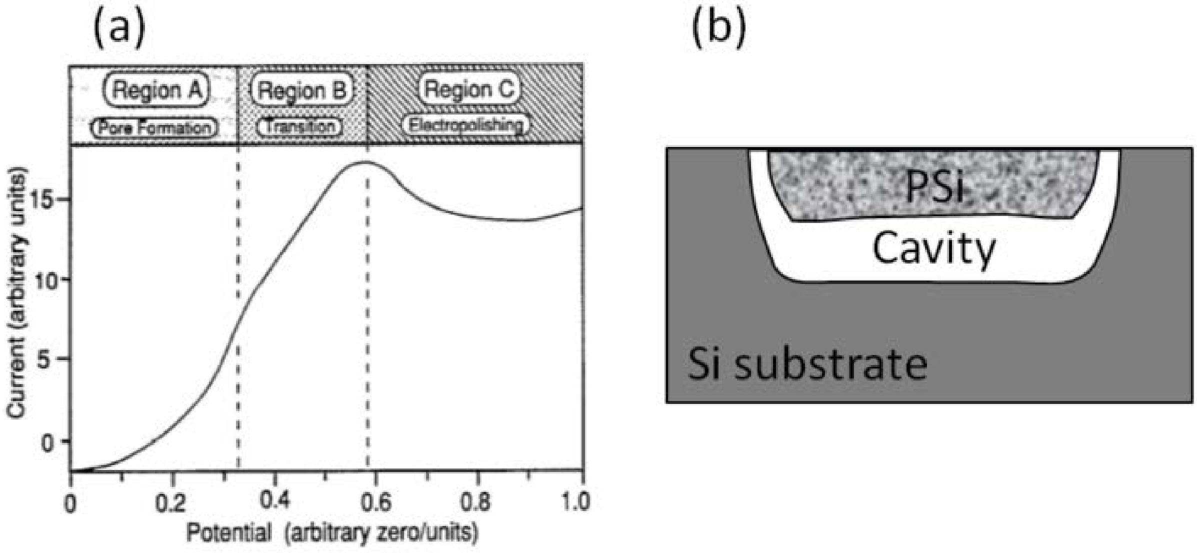


Figure 12. (a) Typical anodic current-potential relationship for silicon in HF showing the salient regions of dissolution. In region A pore formation occurs, and in region C silicon electropolishes. Region B is a transition zone between regions A and C. Scale units and zeros are arbitrarily chosen and depend on silicon sample and experimental conditions [108]. (b) The electropolishing process can be used to create a cavity under a porous silicon membrane.

The supportive material can be obtained through the deposition of a silicon nitride layer [109, 110] and $SiO_2$/polysilicon layers [111]. Silicon nitride is an electrical insulating material that is resistive to electrochemical/chemical etching to some extent. Using this material, a multi-membrane structure has been successfully fabricated by alternating high and low current densities during anodization (Figure 13a). This silicon nitride layer was also used to fabricate a semipermeable porous silicon membrane for miniaturized fuel cell. The use of $SiO_2$/polysilicon layer ensures both electrical isolation from the substrate (due to the oxide layer) and long-time etching resistance with minimum corrosion when exposed to the electrolyte (due to the polysilicon layer). Another way of fabricating the membrane support is to form an n-type silicon layer at the surface of a p-type silicon substrate by phosphorus implantation [112-114]. This n-type layer is used as an etch-stop layer since n-type silicon lacks holes and exhibits a high resistance for proper anodization. This approach does not need the deposition of an extra material (Figure 13b), which simplifies the fabrication and encapsulation processes.

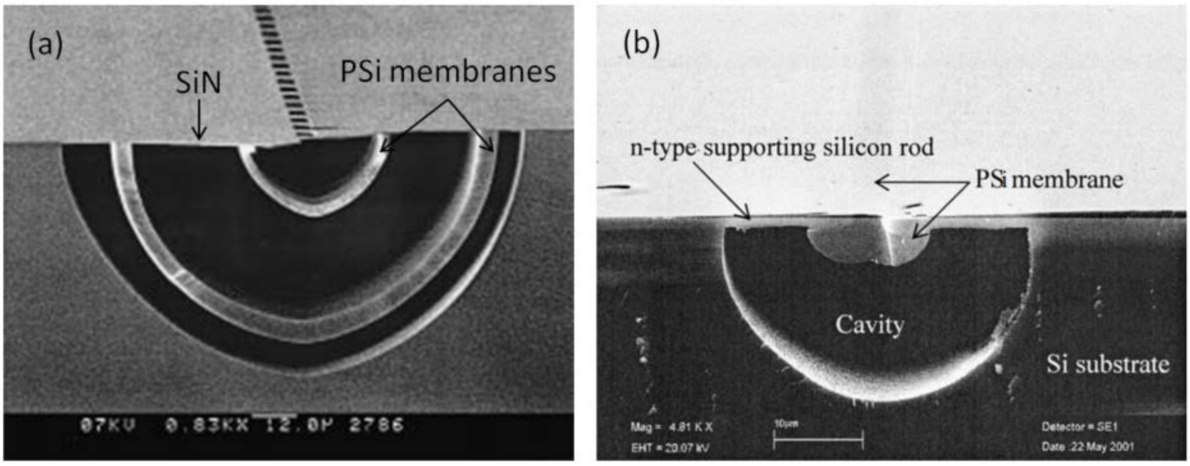


Figure 13. Porous silicon membranes hold by (a) a deposited SiN layer [109], (b) a implanted n-type silicon layer [113].

Fabrication and integration of porous membranes within microfluidics using the sacrificial layer method relies on the rapid dissolution of high porosity nanoporous (<100 nm) silicon in some chemical solution, while the dissolution of macroporous silicon membrane is very slow. The formation of macropores and nanopores in a p-type silicon is usually achieved by changing both the HF concentration of the electrolytic bath and the current density (Figure 14) [115].

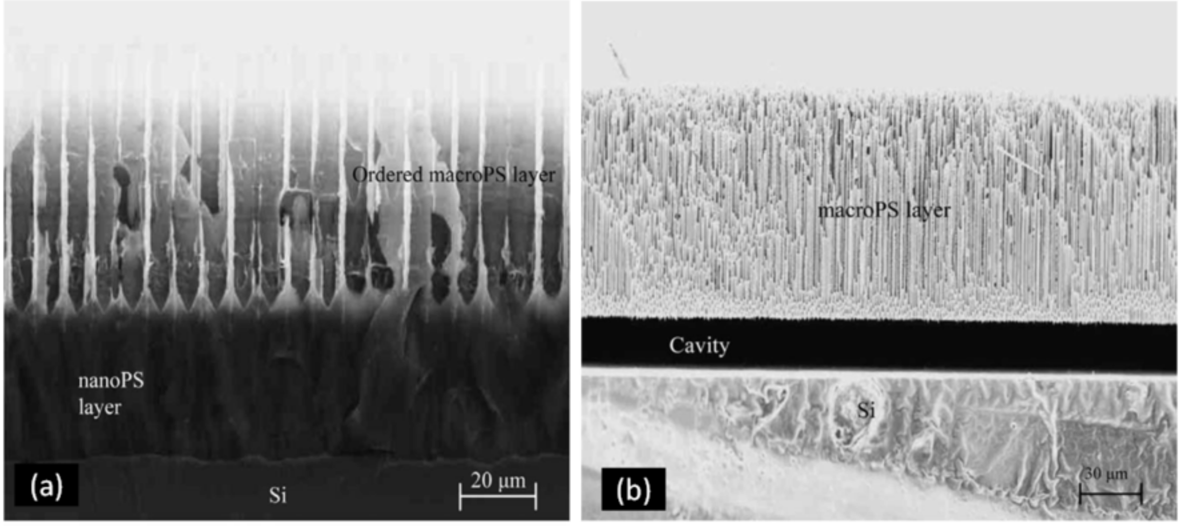


Figure 14. Cross-sectional SEM images of structures consisting of (a) macroporous silicon over nanoporous layers, (b) macroporous silicon membrane over a cavity after the dissolution of the nanoporous silicon layer [115].

### 4.2.1.3. Anodization + micromachining

The anodization process can be coupled to standard micromachining to create porous silicon membranes by dry or wet etching the silicon substrate which hosts a porous layer. The anodization step can be done either before [116-118], or after [119-124] the micromachining process. Figure 15 (I) shows a fabrication process where anodization is carried out before micromachining. After the creation of porous silicon, a protective oxide is normally created to avoid the influence of micromachining by dry or wet etching. Figure 15 (II) shows a fabrication process where anodization is carried out after micromachining. The general process consists in first thinning the wafer by photolithography and etching, then creating porous silicon by anodization. Because micromachining of silicon happens before anodization, there is no risk of etching porous silicon by micromachining process. However, since the anodization of the porous silicon stops when the metal on the backside of the membrane dissolves [119], this process can result in incomplete anodization of the membrane where some of the pores do not extend completely through the membrane. To avoid this issue and the use of metal back contacts, a double-tank etching cell can be used for anodization [122].

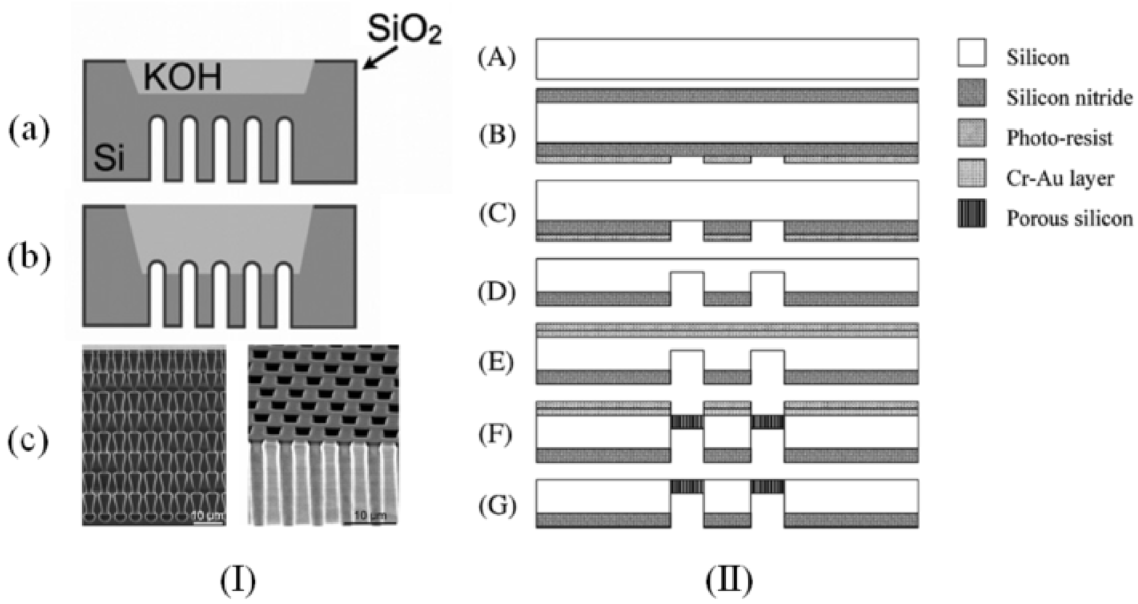


Figure 15. Fabrication of porous membranes by combining silicon anodization and micromachining. (I) (a) anodization process, (b) silicon wet etching by KOH where the membrane geometry is defined by a 140 nm thick thermally grown $SiO_2$ layer, (c) result of the fabricated membrane [116]. (II) (A) wafer cleaning, (B) deposition of a silicon nitride layer,

(C) photoresist patterning, (D) silicon deep reactive ion etching, (E) deposition of a Cr-Au layer for backside electrical contact, (F) anodization, (G) remove the Cr-Au layer [119].

### 4.2.2. Micromachining

With the fast development of nanotechnology and nanofabrication methods, silicon membrane with well-controlled pore morphologies can now conveniently be obtained by micromaching processes. Early work reports on the fabrication of a porous silicon sub-micron particle filter in the 1990s [125]. The fabrication process is shown in Figure 16. First, a sandwich structure of oxide/polysilicon/oxide is created in an n-type silicon substrate; then, holes are patterned into the sandwich structure by photolithography; boron diffusion through the hole pattern is done to form the heavily boron-doped silicon, which is used as an etch-stop [125] in EDP etchant (Ethylene Diamine-Pyrocatechol-Water Mixture); finally, the membrane with channel size of 200 nm is formed using the boron etch-stop technique followed by silicon dioxide undercut etching.

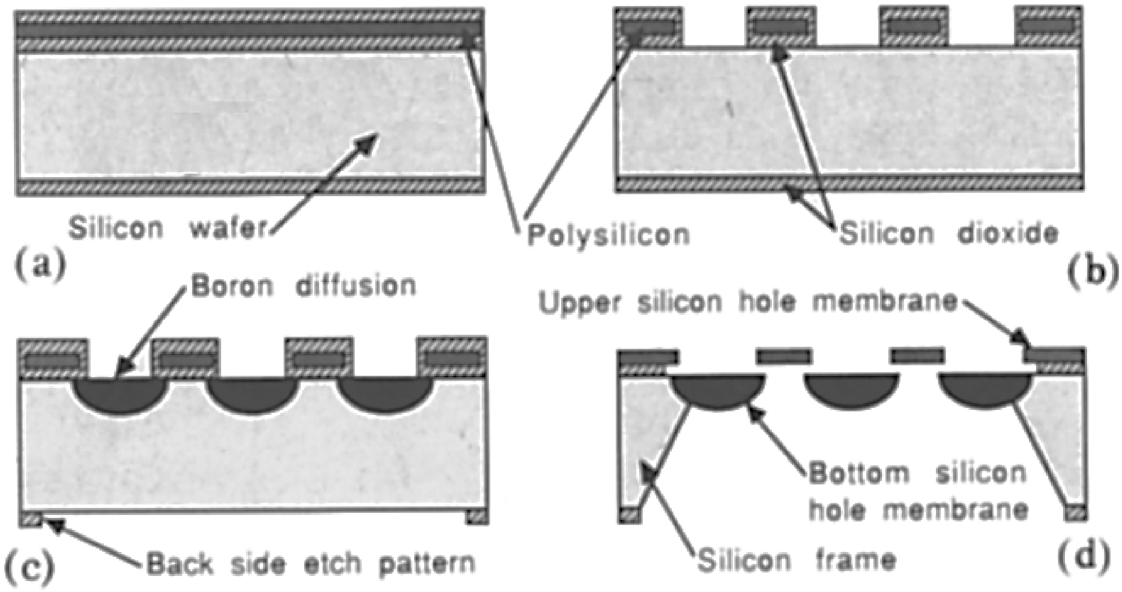


Figure 16. Fabrication process of a filter structure [125]. (a) Creation of oxide/polysilicon/oxide sandwich structure by polysilicon deposition and thermal oxidation. (b) Patterning of holes by standard photolithography and etching. (c) Boron diffusion through the hole pattern. (d) Formation of the single-crystal silicon membrane using etching techniques.

Later, Ferrari and coworkers developed another fabrication process to create nanoporous membranes with controllable pore size through standard micromachining techniques [126, 127]. The fabrication process is shown in Figure 17. The porous silicon membranes had shown excellent properties of size exclusion and biocompatibility, and were used in cell immunoisolation [17] and hemofiltration [70]. Besides, similarly fabricated porous silicon membranes were used in fuel cells [128]. The micromachining approaches enable the fabrication of porous silicon membrane with well-controlled pore size (<5% variation) and membrane thickness (0.5–5 μm). However, the way of defining the pores (*e.g.*, photolithography) results in an overall very low mesoporosity (~1%). The complexity of the fabrication process also implies higher cost than the electrochemical etching approach.

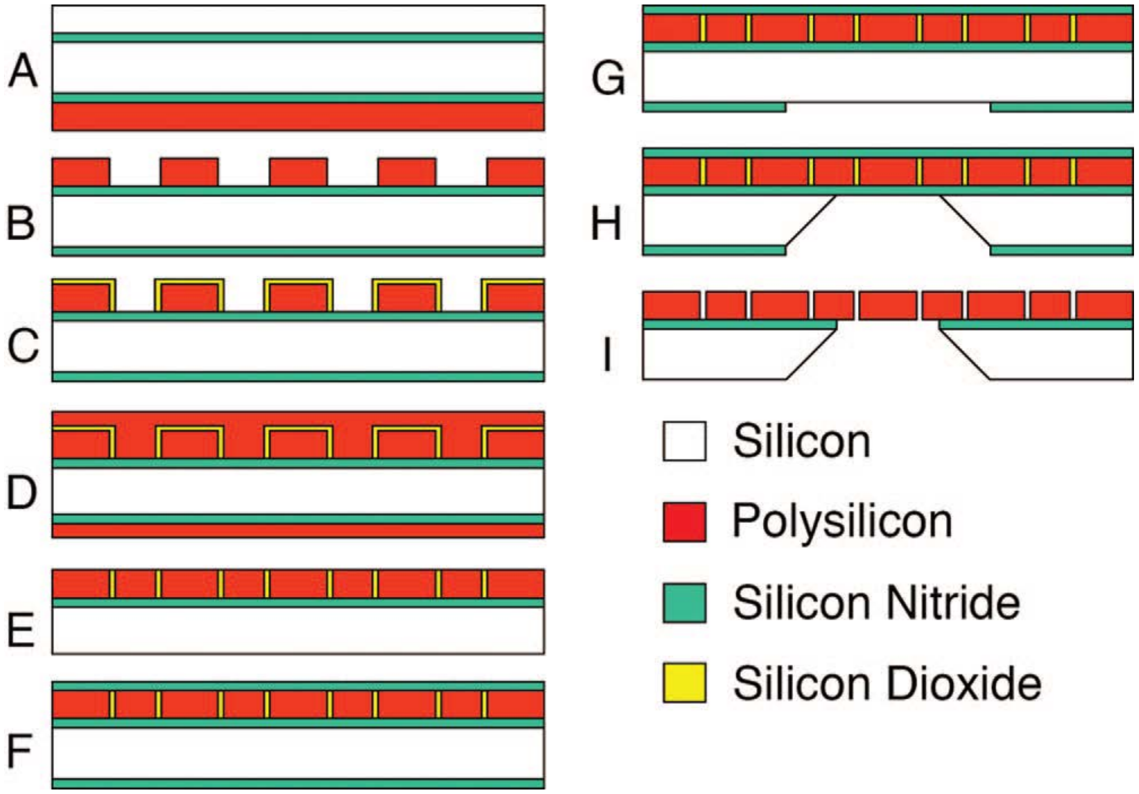


Figure 17. Fabrication process for nanoporous membranes [127]. (A) Growth of buried nitride layer and polysilicon deposition. (B) Creation of holes by photolithography and dry etching in polysilicon layer. (C) Growth of thin sacrificial oxide to determine channel size. (D) Deposition of polysilicon plug layer. (E) Chemical-mechanical polishing to remove any excess polysilicon. (F) Deposition of protective nitride layer. (G) Remove the back side nitride by photolithography and dry etching. (H) Wet etching to create suspended layer. (I) Final release of structure in HF.

### 4.2.3. Deposition + Annealing

Fauchet and coworkers have developed an interesting fabrication process that enables the creation of ultrathin (10–50 nm) mesoporous silicon membranes [16]. The approach relies on the deposition of ultrathin amorphous silicon, and then thermal annealing of the deposited silicon. The thermal annealing results in silicon crystallization that causes volume contraction, leading to spontaneous voids formation (Figure 18). The porous membranes cover openings of several hundreds of micrometres in a rigid crystalline silicon frame, thus they can be easily handled and used. Besides, the porosity can go up to 15% and it can be well controlled with the annealing temperature [129]. The ultrathin membranes have demonstrated high efficiency in size- and charge-based molecule separation, thus constituting promising uses in chromatography and dialysis [16].

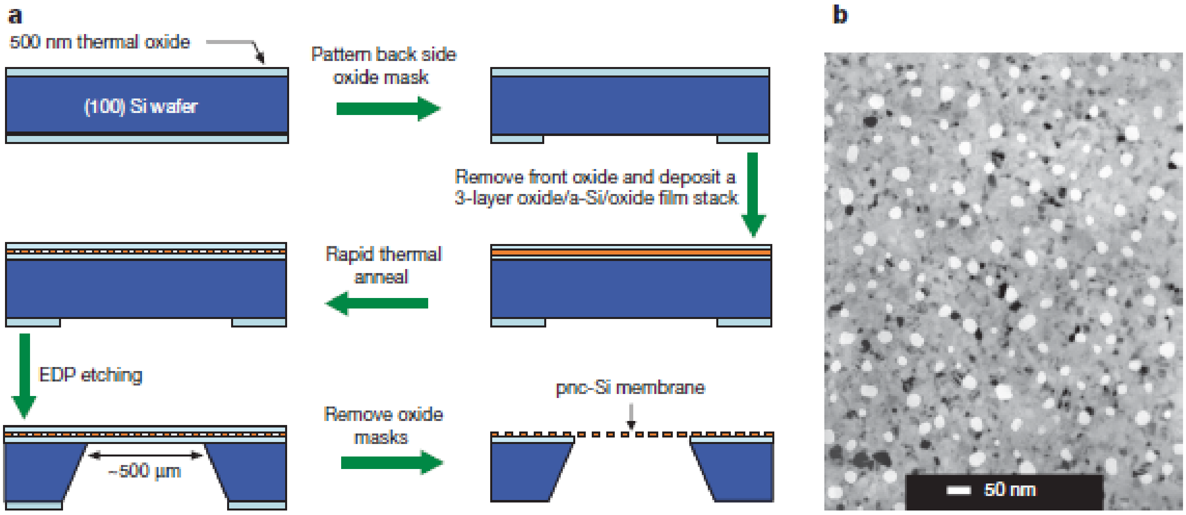


Figure 18. Fabrication and pore morphology of porous nanocrystalline (pnc) silicon membrane [16]. (a) Standard microfabrication tools are used to deposit, pattern and suspend pnc-Si films. (b) A plan-view TEM image of the porous nanostructure of a 15-nm-thick membrane. In this bright field image, pores appear as bright spots while nanocrystalline silicon is in grey or black contrast.

## 5. Integration of PSi membranes into microfluidics: challenges & motivations

The review of fabrication techniques used to create porous silicon membranes provided in the previous section shows that porous silicon membranes are always created perpendicular to the substrate surface. In the case of anodization approaches, this is due to the fact that, in a classical etch cell set up, the current is injected via the backside of (*i.e.* through) the silicon wafer so that the current flows in a direction perpendicular to the silicon surface, leading to the formation of vertical pores (with respect to the surface of the wafer). As for micromachining techniques, the vertical direction is the preferred direction for dry etching. Finally in the case of the annealing technique, the wafer surface provides the ideal plane for deposition of ultrathin silicon layer.

To integrate such membranes into microfluidic devices, the current integration techniques consist in sandwiching fabricated membrane between two encapsulating layers that bear the micro/nano fluidic channels [16, 70-74, 87-89] (Figure 19a). Such three-dimensional (3D) fluidic networks have some disadvantages compared to planar (2D) microfluidic devices (as Figure 19b): (1) the integration of the membrane into the sandwich structure might be more complicated and be prone to fluid leaks; (2) 3D fluidic systems lack design flexibility, while 2D fluidics offer the possibility to easily integrate various designs and functions on the same chip; (3) fluidic operation of a 3D network can be complicated, on the contrary, 2D networks can conveniently include multiple inlet/outlet access to apply pressure and electric signals; (4) 3D networks lack the direct observation accessibility of 2D approaches because the inlet- and outlet microchannels are not in the same observation plane.

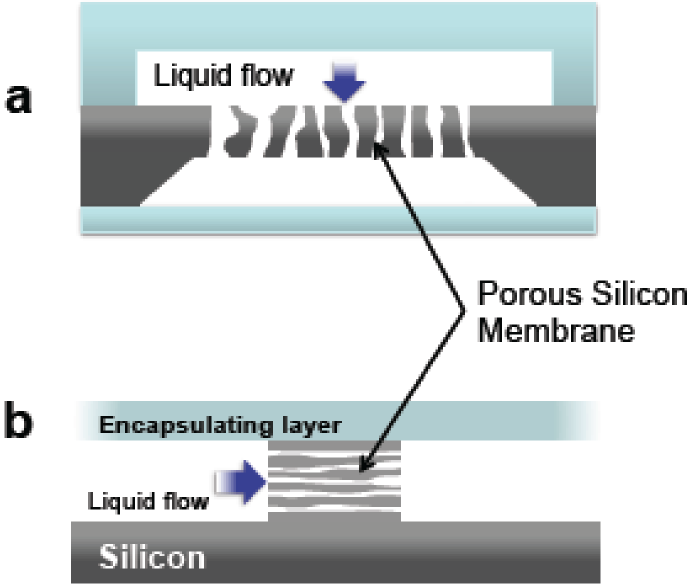


Figure 19. Schematics showing the difference between (a) transverse and (b) lateral porous membranes integrated into 3D and 2D fluidic systems, respectively.

To tackle these drawbacks, this thesis work aims at proposing means to fabricate lateral porous silicon (LPSi) membranes and their monolithic integration into 2D planar fluidics (Figure 19b). To this aim, we propose two original fabrication processes. The proposed approaches are based on the formation of pores tubes that are parallel to the substrate surface, thus connecting inlet and outlet microchannels lying in the same plane.

We then investigate the possibility to use these lateral porous silicon membranes for various applications: size-based filtering in lab-on-chip, preconcentration of molecules by ion concentration polarization through the ion selectivity property of the lateral porous membranes and finally the possibility to carry out interferometry biosensing analogously to vertical membranes but in a flow-through configuration.

## 6. Conclusion

In this chapter, we have first introduced porous silicon and its unique and useful properties such as large surface area, convenient surface chemistry, biocompatibility, and optical properties, which have inspired various applications especially in the biomedical field. We have also presented the various uses of porous silicon for microfluidic applications, including on-chip filtration and separation, biosensors, micropumps, and microreactors. Among the formats of porous silicon in microfluidic devices, porous silicon membranes are of special interest because of their high permittivity, selectivity and tuning properties. After quickly introducing the main fabrication routes to create porous silicon, we have reviewed the fabrication approaches to obtain porous silicon membranes. This review has shown that the current fabrication processes for porous silicon membranes imply their integration into 3D microfluidic systems, which are more disadvantageous than planar fluidic systems. Therefore, this thesis work proposes means to fabricate porous silicon with lateral pores, allowing the integration of porous silicon membranes into planar microfluidics for various applications such as on-chip filtration, on-chip concentration, and flow-through sensing.

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# Chapter 2.

# Fabrication and integration of lateral porous silicon membranes

*In this chapter, we present two novel fabrication processes that enable the monolithic integration of lateral porous silicon membranes into planar microfluidics. First, we study the feasibility of the processes by current flow analysis using finite element method. Then, we describe the chip design and etch cell setup used to try our fabrication approach. We present each fabrication process by describing the process flow, process control, and membrane characterization. Finally, we test the dead-end filtration capability of the fabricated membranes by filtering experiments, which demonstrate the interest of the presented fabrication process for microfluidic applications.*

# 1. Introduction

## 1.1. Transverse versus lateral porous silicon

Since porous silicon is almost exclusively realized with pores running perpendicularly to the surface of the silicon substrate (transverse pores) [1-4], the integration of such membranes into fluidic chips is usually done by sandwiching the fabricated membranes between two micromachined layers that bear inlet/outlet micro-fluidic channels. Such three-dimensional (3D) fluidic networks lack the simplicity of operation and the direct observation accessibility offered by planar microfluidic devices. Besides, these hybrid processes do not offer design flexibility and clearly limit membrane integration into lab-on-a-chip.

For those reasons, we propose two fabrication processes for the realization of lateral porous silicon (LPSi) membranes and their monolithic integrations into two-dimensional (2D) planar microfluidic systems. These two processes are based on the formation of pores tubes that are parallel to the substrate surface (lateral pores), thus connecting the inlet and outlet microchannels lying in the same plane.

## 1.2. General fabrication consideration for the creation of lateral pores

The most common and simple approach for fabricating porous silicon is the electrochemical anodization of silicon in hydrogen fluoride (HF) electrolyte. The mechanism leading to selective silicon dissolution and pore formation relies on the local electrochemical oxidation of silicon due to the injected current (holes), which is subsequently etched in HF [1]. Therefore, although the anodization mechanism involves a complicated mix of electronic and chemical factors, the propagation of pores tends to always follow the electrical current lines. This means that one can control the orientation of the pore tubes by monitoring the direction of the current flow.

In a classical anodization configuration, the current is injected through the backside of a silicon wafer and flows in the direction perpendicular to the silicon surface (Figure 1a), leading to the formation of vertical pores (with respect to the wafer surface). Likewise, the current flow has to be distributed horizontally in order to create lateral porous silicon with pores propagating in parallel to the surface of the substrate. To do so, our proposed approach relies on the use of an electrode patterned on one sidewall of a silicon step separating two microchannels, then injecting the current flow to the opposite sidewall with proper electrical insulation on the top and bottom of the step to localize the pore formation within the step only (Figure 1b). The electrochemical reaction occurs at the sidewall opposite to the electrode (opened) and the pores propagate along the current flow in a lateral fashion until they reach the electrode-patterned sidewall. Adequate sealing of the microchannels separated by the silicon step with horizontal pores then results in the monolithic integration of a lateral porous silicon membrane into planar microfluidics.

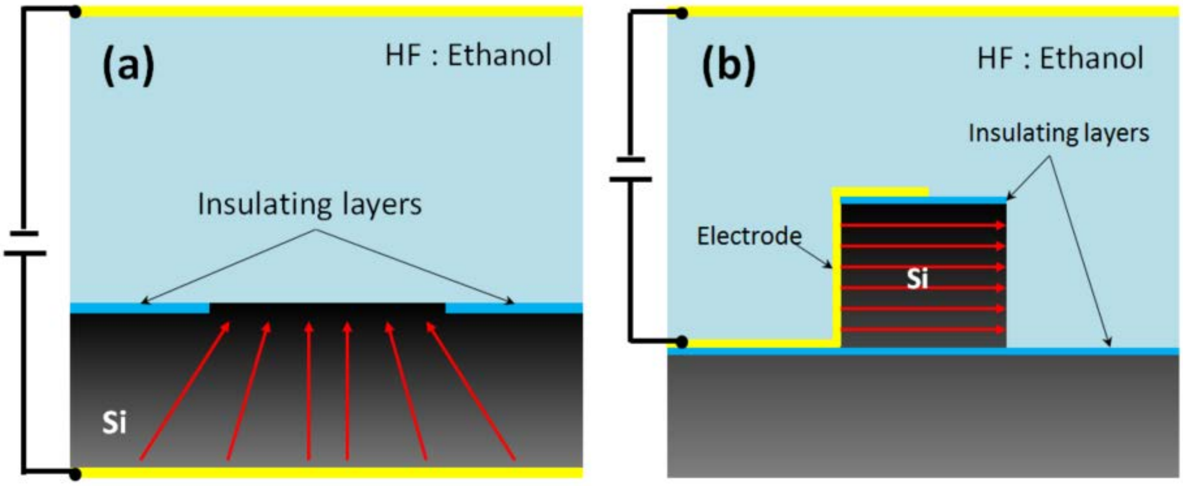

Figure 1. Schematic anodization configuration of (a) the classical model, (b) our proposed model. The red arrows represent the current flow lines.

## 1.3. Two proposed fabrication processes

### 1.3.1. Presentation

The two crucial elements that are needed to create a structure similar to the one shown in Figure 2b are the patterned electrodes and the insulating layers. After fabricating microchannels by etching the silicon substrate, electrodes can be patterned onto the silicon wall separating the channels by using standard metallization process optimized for thick structures. However, providing insulating layers with strong resistance to HF corrosion is more delicate. For this reason, we propose in our work two designs, which are presented in Figure 2, of various technical complexity and resulting advantages.

The first design (SOI process, Figure 2a) relies on the patterning of electrodes on the sidewall and the top of the step to guide the pore propagation within the membrane, and on use of silicon-on-insulator (SOI) wafer with a top p++-doped device layer to provide electrical insulation of the membrane by means of the buried oxide layer that ensures pore formation solely in the membrane.

The second design (implantation process, Figure 2b) relies on the fact that the formation of porous silicon by anodization is highly dependent on the dopant type and concentration [5, 6]. While we still use electrodes patterned on the membrane sidewalls to inject current for anodization, the doping via implantation enables to confine the membrane analogously to but instead of the SOI buried oxide box. A heavily doped p-layer is created by ion implantation within an n-type substrate to constitute the porous membrane by subsequent anodization. Then, in order to confine the pore formation to the p++-layer in a lateral fashion, a thin n-type layer is implanted at the surface of the wafer: this n-type silicon layer and the n-type substrate act as native etch-stops and prevent pore formation [7-9].

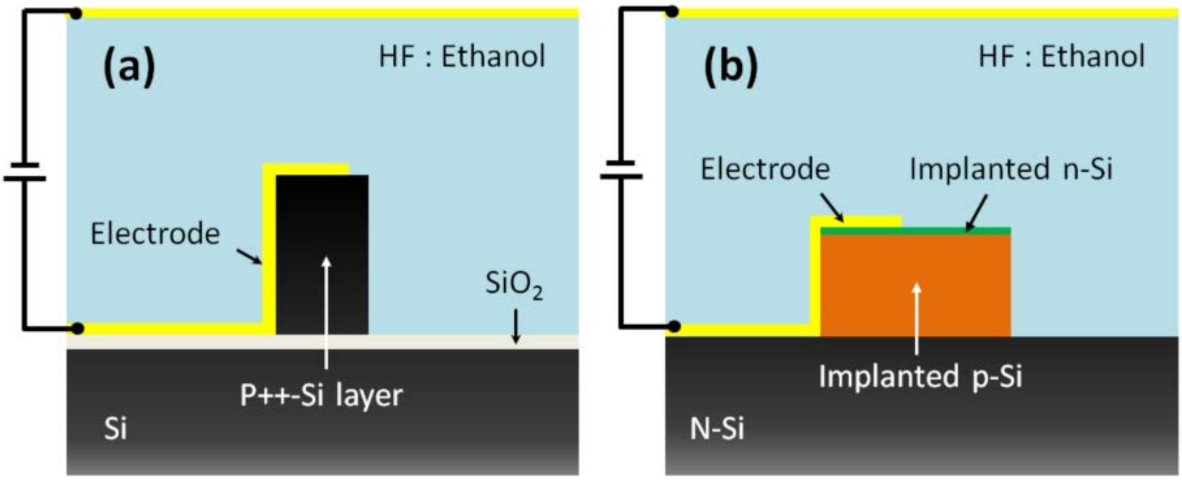

Figure 2. The two proposed approaches for the fabrication of lateral porous silicon membranes: (a) the SOI process, (b) the implantation process.

### 1.3.2. FEM analysis

In order to investigate the feasibility of these two processes, finite element analysis (FEA) was carried out with the simulation software COMSOL Multiphysics 4.2a. We have modeled three cases: the classical process (Figure 1a), the SOI process (Figure 2a) and the implantation process (Figure 2b). The electrochemical cell was simplified to a 2D model and the Electric Currents (ec) physics interface was used to compute electrical currents and potentials. The steady-state solutions were obtained for a 1 V potential difference applied between the electrodes located on the silicon and in the electrolyte and for electrical conductivity and relative permittivity values found in the literature [10, 11] and in the COMSOL material library (Electrolyte: $\sigma = 10^4$ S/m, $\epsilon_r = 80.1$; p++ silicon: $\sigma = 10^5$ S/m, $\epsilon_r = 12.1$; implanted n-Si: $\sigma = 10^4$ S/m, $\epsilon_r = 12.1$; N-type silicon substrate: $\sigma = 0.2$ S/m, $\epsilon_r = 12.1$). The interfacial boundaries of implanted n-Si/implanted p++-Si, implanted p++-Si/n-Si substrate and implanted n-Si/electrolyte were modeled with electrical insulation nodes because both the top n-layer and the substrate are prevented from anodization and thus act as electrical insulators: indeed, both the implanted n-layer and the substrate exhibit high electrical resistance, respectively because the top layer is thin and the dopant concentration is low; besides, the n-type silicon top layer and the electrolyte form a Schottky diode-like junction, which operates in a reverse bias for the corrosion current [1].

The simulation results are presented in Figure 3, which displays the current flow (white arrows) and potential (color scale) within the bulk silicon and electrolyte for the three models. For the classical process, the electric currents flow from the backside to the front side of the substrate in the vertical direction. For the SOI process, where the bottom of the step is insulated by the silicon oxide layer, and the top of the step is partially covered by patterned electrodes which inject current into the step and electrolyte, the current flow is guided laterally within the silicon step, except for its top corner. In the implantation process, because of the top and bottom insulating layers, the current is guided in a strictly lateral fashion. Both processes lead to the creation of lateral porous silicon solely in the steps while preventing the pore formation in the substrates, hence resulting in confined porous membranes within the channel depth.

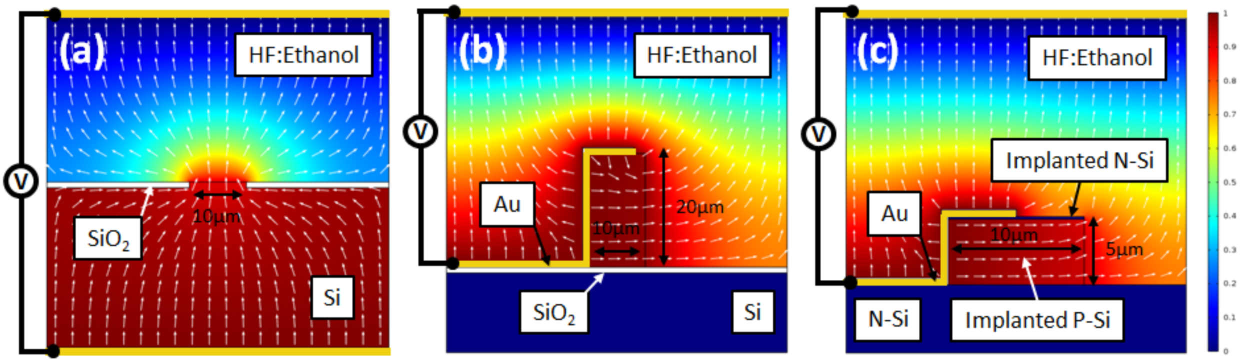

Figure 3. Simulation results of current flow (white arrows) and electrical potential (color range) in the case of 3 FEM models: (a) the classical process, where the current is injected at the backside of the silicon substrate leads to current flow in the vertical direction. (b) the SOI process, where the current is injected and guided by the patterned electrodes with electrical

insulation from the buried oxide layer mostly leads to horizontal current flow. (c) the implantation process, where the current is injected by patterned electrode and guided by implanted n-Si and n-Si substrate leads to horizontal current flow more regular than for the SOI model.

## 2. Chip design and setup

### 2.1. Design of microfluidic chips

We have designed two different chips to demonstrate different microfluidic applications: pressure-driven filtering, pre-concentration by ion concentration polarization and interferometric biosensing. All chips have a size of 16 mm×16 mm suited to the etch cell and the microfluidic sample holder (more details are provided in Chapter 3) used on the fluorescence microscope stage.  Figure 4 shows the design of the first type of chip that includes a membrane of 250 µm in width, which allows the transport of large volume of fluid for filtering and preconcentration purposes and large surface area for biosensing purpose. There are two inlet/outlet in both microchannels (that are separated by the membranes) that allow easy loading of liquid in the chip. The other chip design hosts a small membranes (20 µm×10 µm) and a shallow microchannels (Figure 5), the size of which is determined by related work [12, 13]: this design is used to test the preconcentration (by ion concentration polarization) capability of the porous silicon membrane. On each chip design, we have added two large circular openings (1 mm radius) in order to increase the anodization area on each chip; the anodization area of the lateral porous membrane being fairly small ($\leq 5000\ \mu m^2$), it is quite difficult to monitor the current density of that sole region. With the presence of the big anodization regions, the estimation of current density is much easier.

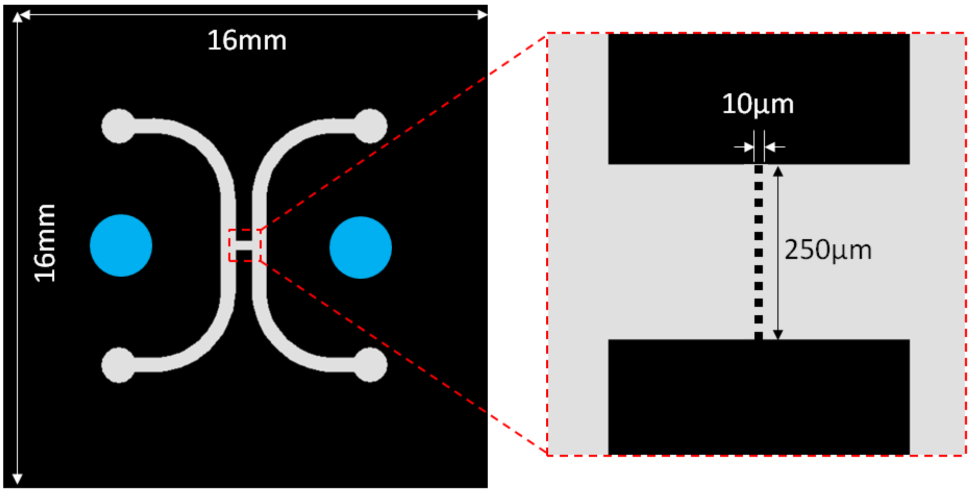

Figure 4. Chip design with a membrane width of 250 µm.

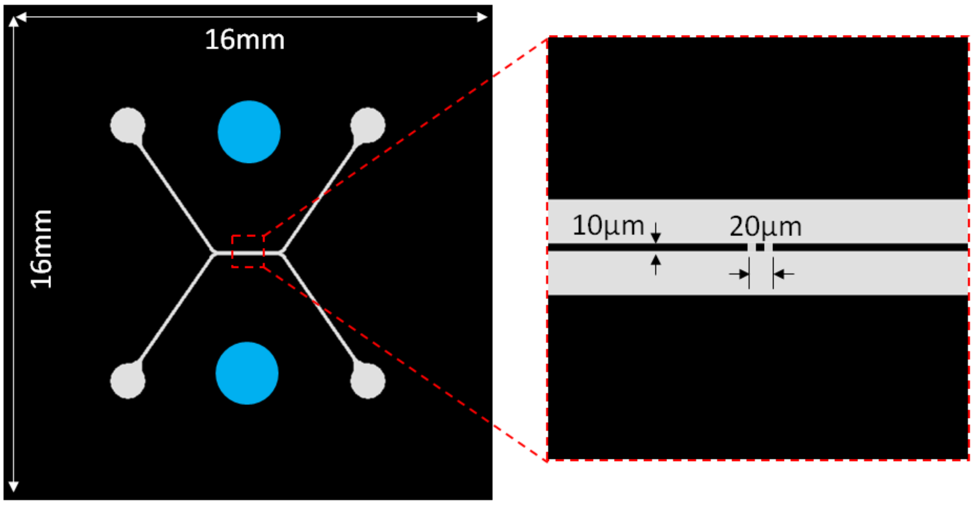

Figure 5. Chip design with a membrane width of 20 µm

## 2.2. Design of etch cells

Our proposed processes requires electric current to be injected by electrodes patterned on the front side of the sample immersed in HF. Special care has to be taken because of the manipulation of HF: easy means to load the sample and the HF solution into the etch cell must be provided, as well as a good electrical contact with the working electrodes and leakage of HF solution must be avoided. The schematic design is shown in Figure 6. The etch cell consists of two parts in order to load and unload the chips conveniently. We use stainless springs (RS Components) to provide an electrical contact between the sample and electric wires connected to the power supply. The stainless springs provide gentle and constant pressure to the sample surface, while being chemically resistant to HF solution and easy to replace. A Viton O-ring is used to avoid leakage of HF solution. A platinum electrode used as the cathode where hydrogen bubbles are released by consuming electrons is placed above the sample in the etch cell. A Keithley 2450 source meter is used as the power supply.

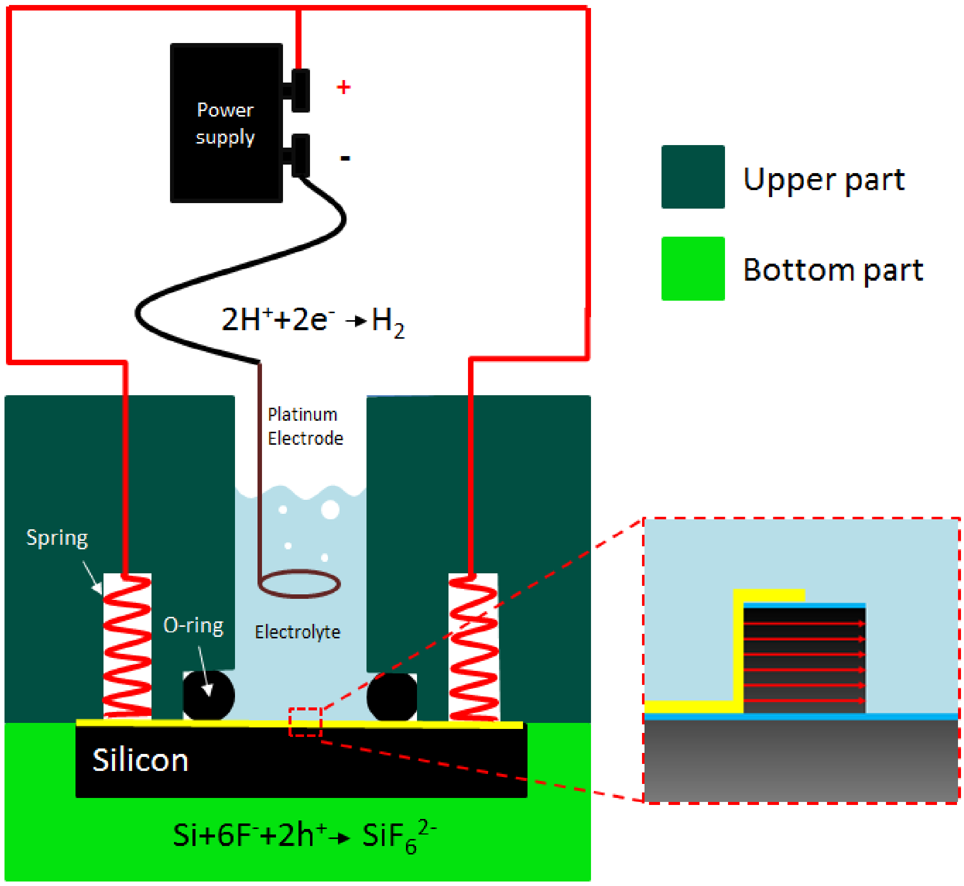

Figure 6. Schematic diagram of the anodization setup and the etch cell. The sample is placed between the upper part and bottom part of the etch cell and the cell is sealed with a Viton O-ring. After loading the electrolyte, the current is injected to the patterned electrodes through stainless springs.

Two etch cells were fabricated to accommodate two sizes of samples: a 16 mm×16 mm chip size (for single chip anodization, convenient to test various anodization parameters on one single wafer) and a 100 mm wafer size. The chip-scale etch cell (Figure 7b) is made of polyurethane (PU), a material resistant to HF corrosion. The upper and bottom parts are held with four Nylon screws. A ring-shape platinum electrode with a ring diameter of ~8 mm is placed ~1 cm above the chip to provide a good current distribution. The volume of the cell for

HF solution is >2 mL (this volume is referred from [1]). Four springs are used to have a good electrical contact with the patterned electrodes on the chip surface. A maximum area of ~1.1 $cm^2$ can be anodized using this etch cell. The wafer-scale etch cell (Figure 7c) is made of Teflon and uses four PEEK screws to adjust the top/bottom parts and the loaded wafer. A Teflon support holding a platinum mesh is used to suspend the mesh electrode at a distance of ~1 cm above the wafer for an even distribution of the current flow in the electrolyte due to the large surface area. Six springs are used to provide a good electrical contact with the patterned electrodes on the wafer surface. A volume of HF solution of ~80 mL is used for each anodization with a maximum anodization area of ~50 $cm^2$.

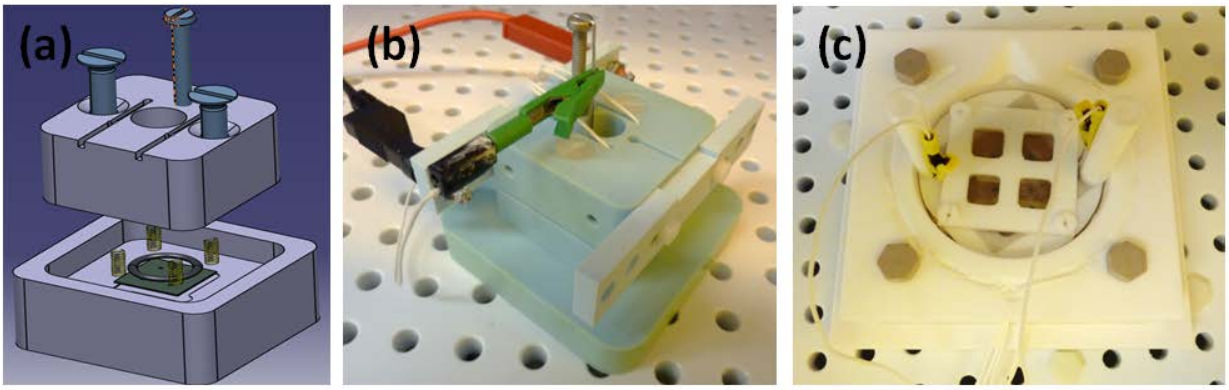

Figure 7. (a) 3D structural view of the chip-scale etch cell. (b) Optical picture of the chip-scale etch cell. (c) Optical picture of the wafer-scale etch cell.

## 3. Device fabrication

### 3.1. Device fabrication by the SOI process

To demonstrate the feasibility of the SOI process, microfluidic chips with integrated lateral porous silicon membranes were fabricated following the process shown in Figure 8. The key steps of this process are first the fabrication of a solid membrane bridging two etched microchannels and secondly, in a single step, the protection of the silicon surface except that of the membrane sidewall where pores are to be created and the patterning of an electrode to provide charges on the opposite membrane sidewall.

### 3.1.1. Fabrication process flow

In this process, SOI wafer is used as a starting substrate (<100> wafer, p-type, d = 100 mm, t = 20/2/450 µm, ρ = 0.01-0.02/0.015 Ω cm, Shin-Etsu), in which the dopant type and concentration of the top silicon layer were selected for the formation of mesoporous silicon by anodization without external illumination.

The fabrication process started by creating inlet and outlet microchannels using deep reactive ion etching (DRIE), in which the buried oxide was used as an etch-stop layer (Figure 8b). A conformal metal layer was then deposited by sputtering 100 nm/500 nm thick Cr/Au. After proper annealing (250 °C, 20 min), a thick photoresist (AZ 40XT 20µm) was applied and patterned in order to open a window on one sidewall of the step. The metal on the unprotected sidewall was then removed by wet etching in appropriate baths (Figure 8c). Silicon anodization can be carried out on chip scale or wafer scale using different etch cells. In this process description, the anodization was done on chip scale, which means that the wafer was diced into individual chips. For anodization purposes, the silicon chip was loaded into the etch cell and the cell was filled with electrolyte (48% aqueous HF:Ethanol = 1:1) . The etch cell was then connected to a power supply to conduct the anodization at 200 mA cm$^{-2}$ for 2 min (Figure 8d). It is important to note that the buried oxide was exposed to the HF solution which limited the anodization time due to the possible device failure. After the lateral porous silicon was created by anodization, the metal was totally removed by wet etching. In order to create fluidic inlet/outlets and connect the fluidic chip to external fluidic reservoirs, holes were drilled through the silicon chip by sandblasting (Figure 8e). To avoid the physical damage of the porous membrane and chip surface during the sandblasting, a 500 µm thick dry film of photoresist was laminated on the chip front side (64 °C, 2 MPa, DYNACHEM, SA 3024 OC). The channels were finally encapsulated by anodic bonding (370 °C, 5×10$^{-5}$ mBar, 600 V for 10 min) the silicon chip to a same size glass chip diced from a 500 µm thick borofloat 33 wafer (Schott) (Figure 8f).

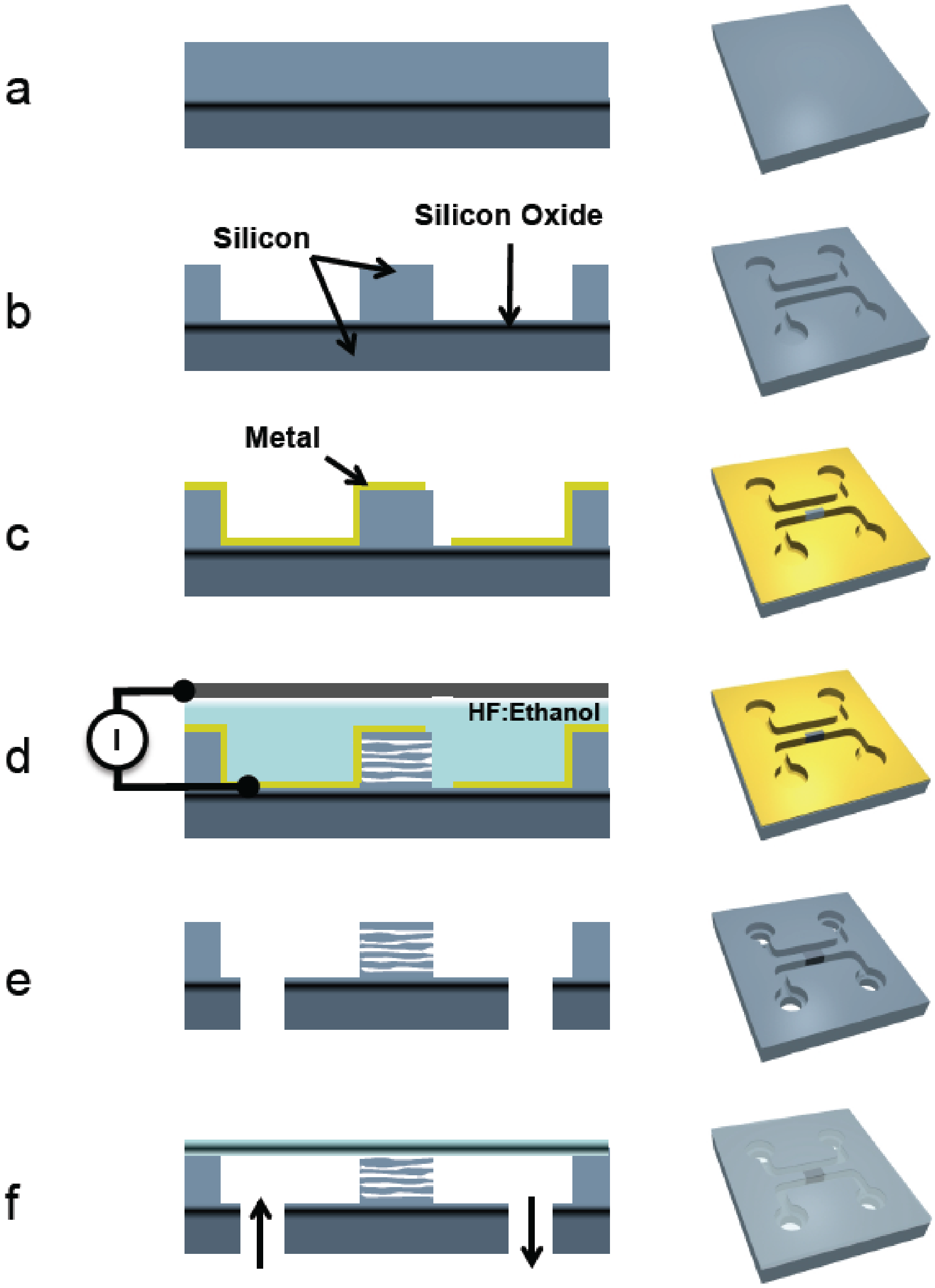

Figure 8. SOI fabrication process of a fluidic chip with an integrated lateral porous silicon membrane (Left: section view, Right: three-dimensional representation) [10]. (a) The starting substrate consists of a SOI wafer. (b) Dry etching of the top silicon layer down to the buried oxide is used to create microchannels. (c) A metal layer, used as the working electrode, is deposited in a conformal way and etched where anodization of silicon is to be initiated. (d) Silicon anodization is carried out in a HF:ethanol bath. (e) Fluidc inlets and outlets are realized by means of sandblasting. (f) The channels are sealed by anodic bonding.

### 3.1.2. Membrane characterization

Figure 9a shows a typical 16 mm×16 mm fabricated chip which bears two microchannels, each having two inlet/outlet holes. The microchannels with 20 µm depth are separated by a 10 µm thick porous silicon membrane (Figure 9b). The cross-sectional views of the membrane are displayed in Figure 9c and 9d, showing that the lateral mesoporous membrane adequately connects the microchannels. The pore size and porosity of the fabricated membranes are respectively ~25 nm and ~50%, estimated from the SEM picture.

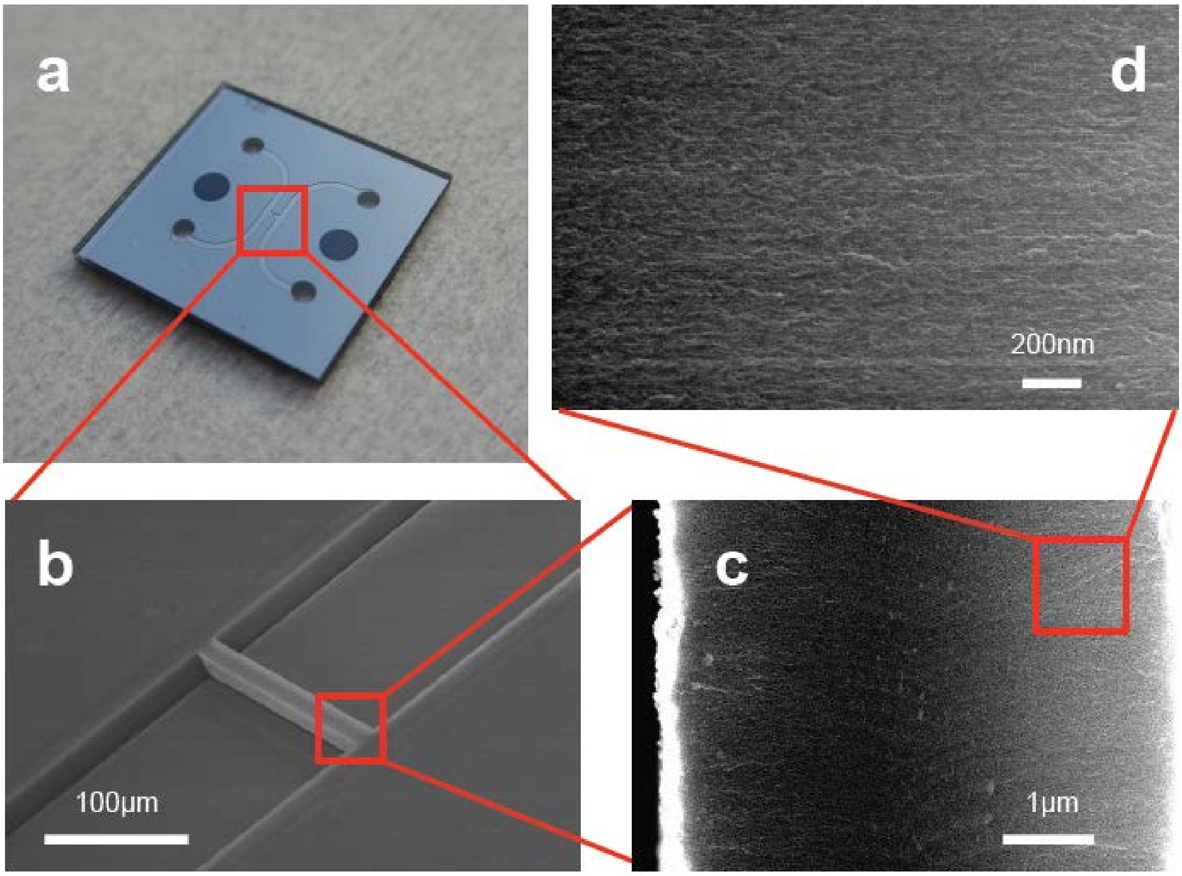

Figure 9. (a) Optical photograph of a fabricated fluidic chip integrating a lateral porous silicon membrane. (b) SEM picture of the lateral porous silicon membrane bridging two fluidic microchannels. (c), (d) SEM section views of the fabricated membrane. The membrane is 20 µm high and 10 µm thick [10].

### 3.1.3. Critical aspects of the process

#### 3.1.3.1. Optimization of the photolithography step for metal etching

As previously mentioned, the photolithography step used to protect the metal for the realization of the working electrode is one of the critical steps of the SOI fabrication process. To this aim, a thick photoresist (AZ 40XT), with a final thickness of 20 µm was used to make sure that the channels and the step were fully covered. Optimizations of the photolithography process were carried out in order to adequately open the photoresist at the desired location. Figure 10 presents some examples of photoresist patterning along with the morphologies of the metal after wet etching. Since the 20 µm thick photoresist was applied onto the 20 µm thick step, a total photoresist thickness of around 40 µm had to be adequately developed and removed from the bottom the microchannels (Figure 11a). This can normally be achieved by adding ~80% of the exposure time. However, even if this works fine for wide structures (Figure 10a), the large thermal stresses induced in small openings (Figure 10b) caused the photoresist to crack near the sidewalls (Figure 11b). These cracks allowed the etching solution to etch away the metal along the sidewall, leading to inappropriate electrode patterning. To solve this issue, we have added resting time (>1h) after each step of the photolithography process (spin-coating, and exposure and post-exposure bake) to release the thermal stresses.

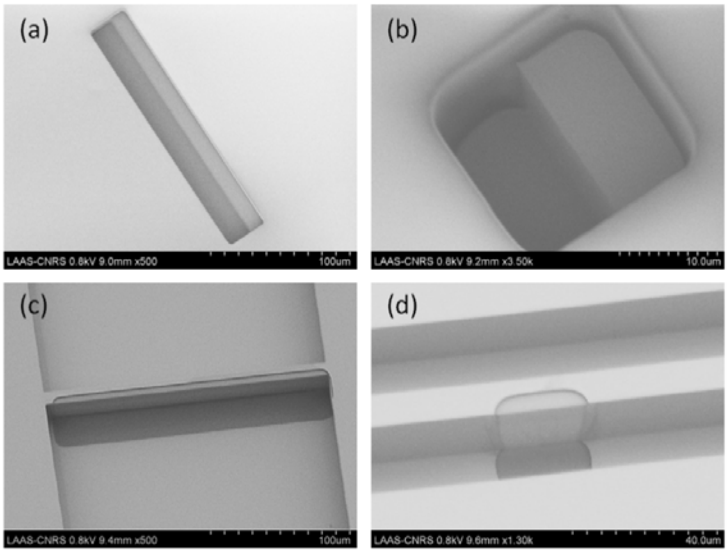

Figure 10. SEM pictures of silicon steps after photoresist patterning: photoresist AZ 40XT with a large opening of 240 µm×30 µm (a), and a small opening of 20 µm×20 µm (b). (c) metal morphology after wet-etching structure (a). (d) metal morphology after wet-etching structure (b).

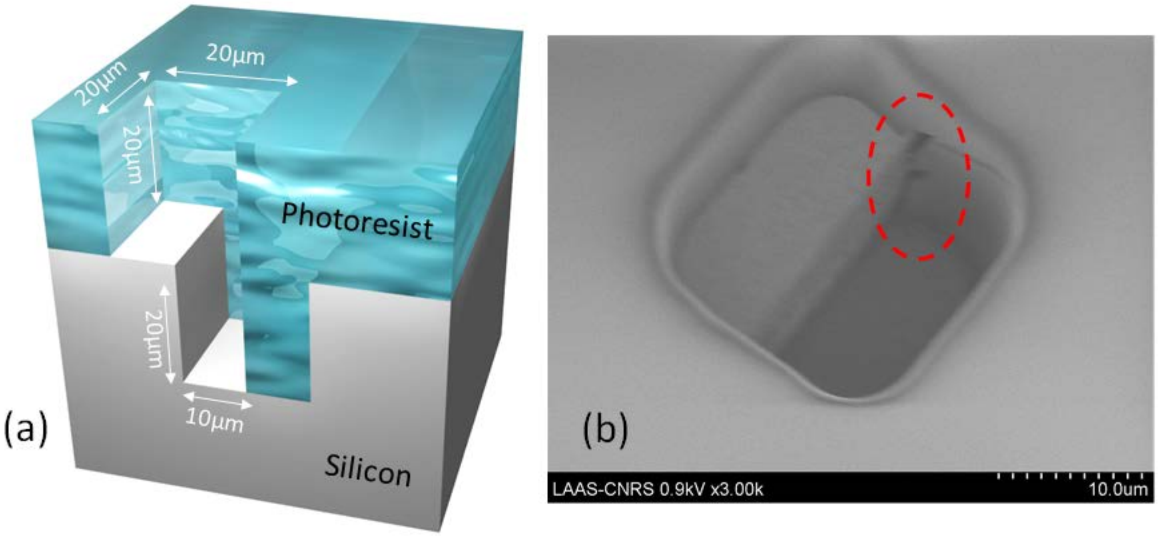

Figure 11. (a) Schematic diagram of the thick photoresist layer (AZ 40XT 20 µm) onto the step structure. (b) SEM picture showing cracks in the photoresist near the step.

#### 3.1.3.2. Alternative metallization method

The patterning quality of the metal electrode is critical for the creation of lateral porous silicon where a conformal coating is absolutely necessary for our process. In this case, a thick enough metal layer can be sputtered at the surface of the wafer. However, the wet etching of a thick metal layer is hard to control and easily leads to metal over-etching at the top of the step. Besides, the sputtering process is an expensive process. Therefore, we have developed an alternative metallization method suited to our process.

The idea of the process is based on gold electroplating to thicken the electrode after patterning: first, a layer of Cr/Au of 50 nm/50 nm was deposited by physical vapor deposition; after proper annealing (250 °C, 20 min), the metal was patterned and wet-etched; then, the photoresist was removed and the chip surface was cleaned in piranha solution ($H_2SO_4$:$H_2O_2$ = 1:1 for 2 min); finally, a gold layer of ~2 µm was electroplated. Figure 12a shows top view of patterned electrode before anodization. After the anodization process, the cross-sectional view of patterned electrode are shown in Figure 12b, demonstrating the adequate conformal coating of the metal layer. In this method, the seed metal layer can firstly be deposited by vapor deposition (vs. sputtering) since the subsequent electroplating step ensures the conformation of the final layer by isotropically thickening the metal.

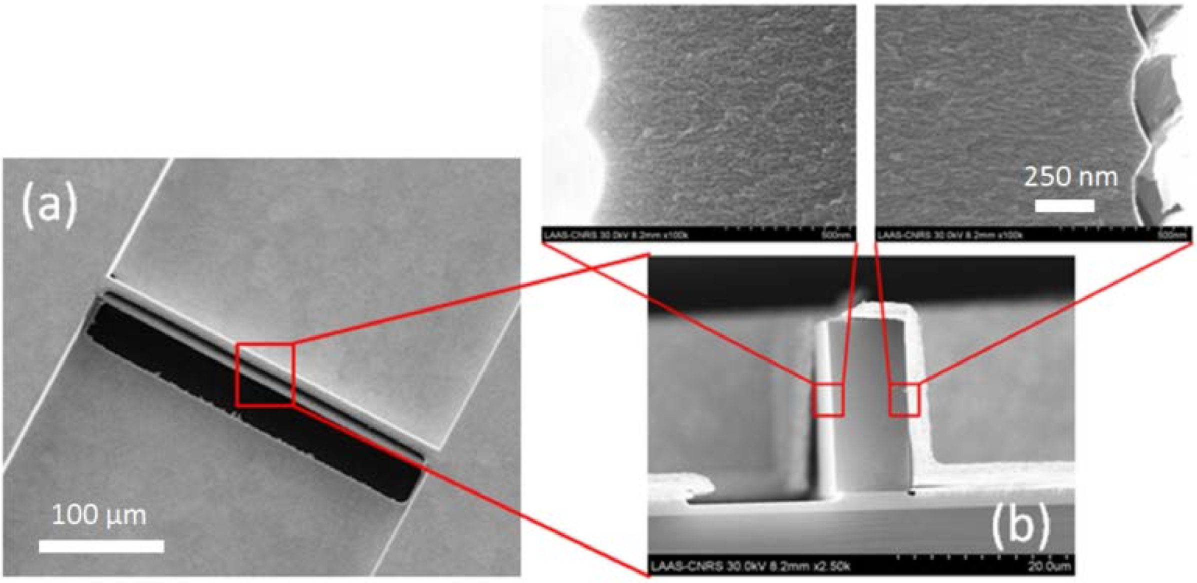

Figure 12. (a) Top view of patterned electrode thickened by the electroplating method (before anodization). (b) Cross-sectional view of the patterned electrode after anodization. The pictures show appropriate conformation for lateral porous silicon formation.

#### 3.1.3.3. Surface cleaning for anodic bonding

Anodic bonding, used for chip encapsulation, is based on the diffusion of sodium ions from a glass substrate (Borofloat) to the silicon chips driven by a voltage at high temperature. This process demands a clean surface condition for adequate contacting of the silicon with glass. However, the fabrication process, especially the drilling of holes by sandblasting, sometimes brings some particles that are very hard to remove because of the surface forces between silicon chip and particles [14]. Therefore, we have developed a specific cleaning protocol taking care of the fragility of the porous silicon: (1) ultrasonic cleaning of the chips and glass wafer at 35 Hz for 2 min in acetone to remove the large particles and the organic residues; (2) immersion of the chips and glass wafer in an APM solution ($NH_4OH:H_2O_2:H_2O$ = 1:1:5) at 80 °C for 5 min to remove the small particles and other organic residues; (3) immersion of the silicon chips in buffered HF (5%) for 20 s to remove the surface oxide; (4) immersion of the chips and glass wafer in piranha ($H_2SO_4:H_2O_2$ = 1:1) for 2 min; and just before bonding process, (5) 5 min oxygen plasma (400 W) on both the chips and glass wafer. This cleaning process has ensured nearly a 100% success rate of bonding.

In this cleaning protocol, care must be taken on the use of ultrasonic cleaning and APM solution. Both processes would lead to the destruction of porous structure if they are over-used. It is also important to note that the methods descripted in section 3.1.3.2. and 3.1.3.3. are also adaptable for the membrane fabrication by the implantation process.

## 3.2. Device fabrication by the implantation process

The fabrication and integration of lateral porous silicon membranes by the implantation process are shown in Figure 13. The key steps of this process are the uses of n-type silicon substrate and implanted n-type silicon layer as electrical insulation layers, while lateral porous silicon is solely created in the p-type implanted middle layer.

### 3.2.1. Fabrication process flow

The fabrication process of the lateral porous silicon membrane by means of ion implantation is detailed in Figure 13. The process started by creating a sacrificial oxide layer (40 nm) by thermal oxidation of an n-type silicon wafer (<100> type, d = 100 mm, t = 525 µm, ρ = 7 Ω cm), in order to prevent surface damage and channeling effects during subsequent ion implantation. Then, a thick and heavily doped p-layer was formed by boron implantation (dose = $2 \times 10^{15}$ $cm^{-2}$, energy = 150 KeV) and thermal annealing at 1150 °C for 8 h (Figure 13a). After removing the oxide layer in buffered HF (5%), phosphorus implantation (dose = $1 \times 10^{14}$ $cm^{-2}$, energy = 50 KeV) and rapid thermal annealing (1000 °C for 5 min) were carried out to form a ~150 nm thick n-type layer (Figure 13b). A masking layer (ECI 2.6 µm) was used during phosphorus implantation to provide large porosification areas on the chip surface for better control of the current density during subsequent anodization. Then, 5 µm deep inlet and outlet microchannels were created by reactive ion etching (Figure 13c). This specific channel depth is chosen in accordance to the thickness of the implanted p++-layer and thus the expected thickness of the porous membrane in order to fully integrate the membrane within the microchannels. It should be noted that while the boron-implanted layer is ~9 µm thick, only the top ~4 µm of the p++-layer turns into porous silicon because silicon anodization occurs in the region of highest dopant concentration.

Integration of the lateral porous silicon membrane was then achieved by anodizing the boron-implanted silicon lying in between the two channels. For this purpose, an electrode was first created by sputtering 100 nm/500 nm Cr/Au layers in a conformal way to ensure the presence of metal on the microchannel sidewalls. The native silicon oxide was etched away in buffered

HF 5% just before sputtering to ensure a good metal/silicon contact. After proper annealing (250 °C, 20 min), the metal was patterned by means of photolithography using a 5 µm thick photoresist (AZ 4562), followed by wet etching in appropriate baths in order to reveal the opposite silicon membrane sidewall (Figure 13d). The wafer was diced into individual chips before anodization so that different anodization parameters could be tested. For anodization purposes, the chip was loaded in the chip scale etch cell and the formation of pores within the membranes was achieved by the anodic dissolution of silicon in a 1:3 ethanol:48% aqueous HF solution (Figure 13e). The electric current was injected to the patterned electrodes (used as the anode) on the front side of the chip and was expected to flow within the p++-layer (sandwiched between the implanted n-layer and n-type substrate), while the cathode consisted of a platinum ring immersed in the electrolyte bath and facing the chip. Following the anodization step, both Cr/Au metal layers were removed in wet etch baths. In order to create fluidic inlet/outlets and connect the fluidic chip to external fluidic reservoirs, holes were drilled through the silicon chip by sandblasting (Figure 13f). The channels were finally encapsulated by anodic bonding (370 °C, $5\times10^{-5}$ mBar, 600 V for 10 min) the silicon chip to a same size glass chip diced from a 500 µm thick borofloat 33 wafer (Schott).

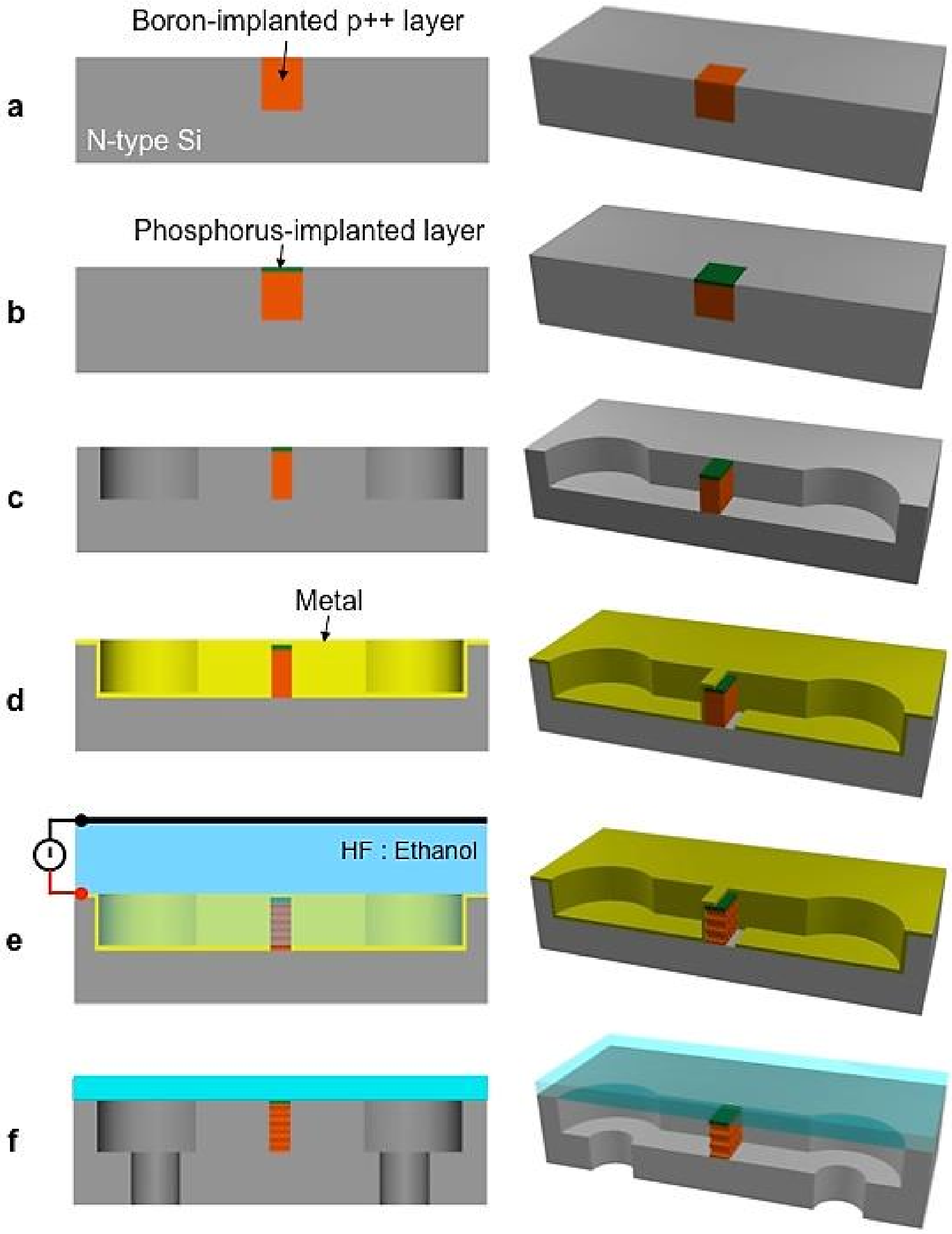

Figure 13. Fabrication process of lateral porous silicon membrane using ion implantation. (a) Boron implantation in an n-type substrate to create a heavily doped p-layer for pore formation by anodization. (b) Phosphorus implantation to create an n-layer at the surface of the wafer. (c) Dry etching to form microchannels. (d) Metal layer deposition and patterning to create a working electrode. (e) Silicon anodization carried out in a HF:ethanol bath. (f) Fluidic inlets/outlets realized by sandblasting and chip encapsulation by anodic bonding. For figure clarity, the implanted areas are only displayed at the membrane location.

### 3.2.2. Optimization of implantation parameters

The profiles of the n- and p-doped layers are precisely controlled by means of ion implantation to obtain confined membranes with lateral pores using the afore-described fabrication process. Precise location of the porous silicon formation is monitored by the dopant type and concentration: as a result, it is of paramount importance to be able to predict the profiles and select the appropriate implantation parameters in order to obtain the desired results. To this aim, we have obtained dopant profiles using two-dimensional (2D) process simulation using the mathematical simulation program ATHENA (Silvaco Int.) that takes into account all process steps influencing the final profile, *i.e.* the implantation, thermal annealing, thermal oxidation and de-oxidation steps.

At first, the 40 nm thermal oxide layer is simulated using the Fermi Compress model. Then, Pearson Implant model is used to model the boron implantation step, where a boron concentration of ~$8\times10^{18}$ cm$^{-3}$ is sought in order to create a thick heavily doped p-type layer in the n-type substrate. High ion energy is chosen (150 KeV) to allow a maximum depth of penetration into the silicon substrate and maximize the membrane thickness. The thermal annealing process, that activates the dopants and repairs the damages caused within the silicon crystal lattice by ion implantation is a dynamic diffusion process of dopant atoms that is prolonged in our case in order to increase the doped layer depth: as a result, a long time (8 h) and high temperature (1150 °C) are used for boron annealing. The Fermi Compress model is again used for this step. The oxide layer is then removed before the next step. The thin phosphorus implanted n-layer used to guide the current flow within the boron-doped layer is realized with low ion energy (50 KeV) and rapid thermal annealing (1000 °C for 5 min). The Pearson Implant model and Fermi Compress models are respectively used to model phosphorus implantation and annealing. An ideal phosphorus implantation dose of $1\times10^{14}$ cm$^{-2}$ is selected to be high enough to form n-type silicon, but low enough to avoid pore formation due to the tunneling of holes – not to mention that high dopant concentration could easily lead to silicon electropolishing because of overwhelming current density [15, 16].

The resulting simulated doping profile obtained with the afore-mentioned parameters is shown in Figure 14. The surficial n-type silicon layer is ~150 nm and the thickness the heavily doped p-type silicon layer is ~4 µm. In order to validate our model for process prediction, we have compared these simulation results with experimental data. To this aim, we have carried out the doping process, including all implantation and annealing steps on a fresh silicon wafer.

After processing, the doping profiles were obtained from Secondary Ion Mass Spectrometry (SIMS), which are shown in Figure 14: while the phosphorus profile is very similar to the simulated one, the boron concentration is slightly lower than as predicted. But in general, the 2D process simulation fits the experimental results very well, especially for the values of the junction depths.

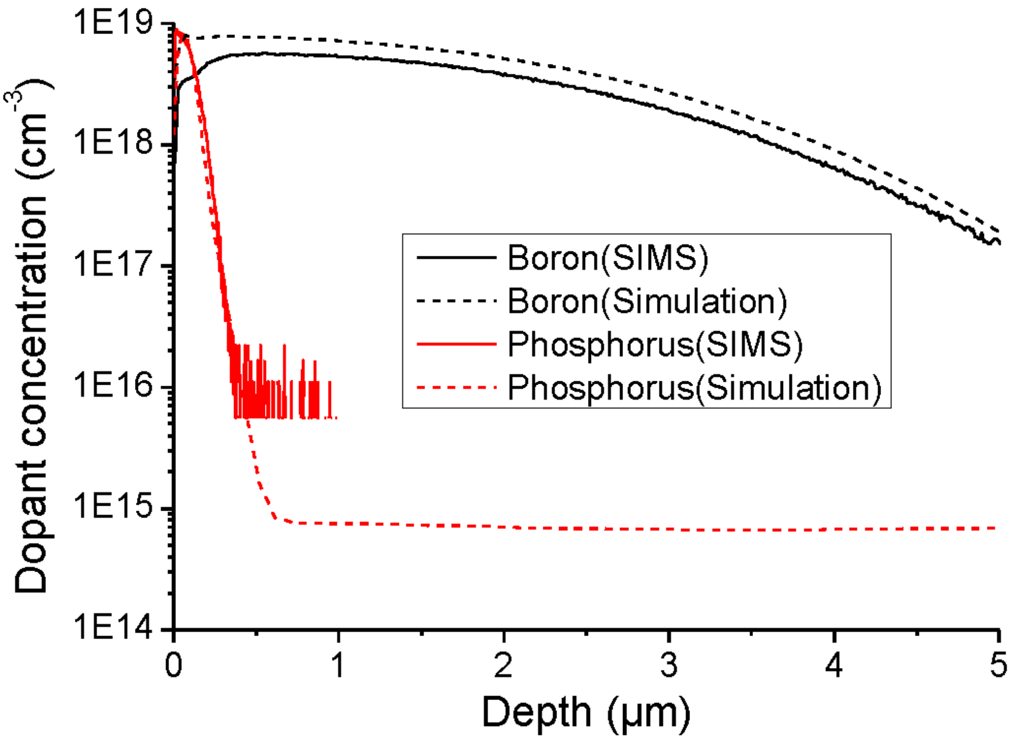

Figure 14. Boron and phosphorus doping profiles within the silicon substrate. Experimental values obtained from SIMS analysis are compared to theoretical data from 2D process simulation.

As previously mentioned, the final phosphorus concentration within the top implanted layer is crucial for our process to be successful. While SIMS analysis enables the accurate determination of the doping profile, it is a destructive process that can only be used for process implementation but not to characterize the device chips. As a result, we have rather used four-point probe measurement to assess the correct doping level. We have tested various samples consisting of previously boron-implanted silicon chips subsequently implanted with various doses of phosphorus. After proper annealing, the sheet resistances of implanted chips were obtained by means of a four-point probe, which show that as expected, phosphorus implantation changes the way the current flows and impacts the electrical measurement

(Figure 15). When the concentration of phosphorus is lower than boron in the surficial layer (cases 1-2), the net doping results in low-doped p-type silicon. During the four-point probe measurement the current goes through the low-doped p-layer and flows in the boron-implanted layer, so the sheet resistance is very low (Figure 15a). On the contrary, at sufficient phosphorus concentration (cases 3-4), a p-n junction is formed (Figure 15b) and the current flows in the surficial n-layer, so the sheet resistance is high. After the formation of p-n junction, a further increase of dose reduces the resistivity of the implanted n-layer. As a result, the sheet resistance declines.

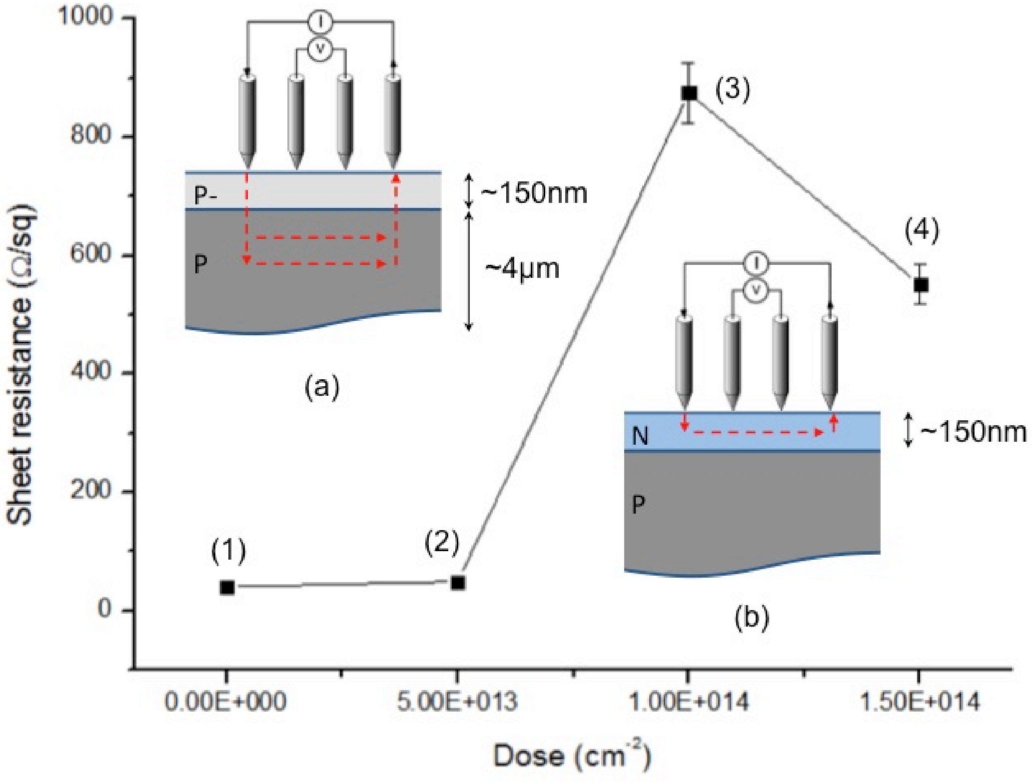

Figure 15. Sheet resistance values measured for various phosphorus implantation doses in a previously implanted boron layer.

The value of sheet resistance can be estimated from doping profiles obtained from SIMS analysis. This estimation can be considered as a confirmation of sheet resistance from four-point probe measurement. As a first approximation, we consider the implanted layer to be uniform in dopant concentration within a certain depth. The sheet resistance is then calculated by [17]:

$$R_s = \frac{1}{qN\mu t} \tag{1}$$

Where, $q$ is the carrier charge; $N$ is the net impurity concentration; $\mu$ is the mobility of majority carrier; $t$ is the thickness of implanted layer. The net impurity concentrations and thicknesses of implanted layer are derived from the SIMS analysis. The mobility values are obtained from [18]. Table 1 presents the resulting calculated values that are indeed close to the measured sheet resistance values.

Table 1. Calculated and experimental sheet resistances as a function of the implanted phosphorus dose.

| P dose (cm$^{-2}$) | 0 | $5 \times 10^{13}$ | $1 \times 10^{14}$ | $1.5 \times 10^{14}$ |
|---|---|---|---|---|
| Majority charge carrier | Boron | Boron | Phosphorus | Phosphorus |
| $q$ (C) | $1.6 \times 10^{-19}$ | $1.6 \times 10^{-19}$ | $1.6 \times 10^{-19}$ | $1.6 \times 10^{-19}$ |
| $N$ (cm$^{-3}$) | $3 \times 10^{18}$ | $3 \times 10^{18}$ | $3 \times 10^{18}$ | $8 \times 10^{18}$ |
| $\mu$ (cm$^2$/(V·s)) | 102 | 102 | 118 | 105 |
| $t$ (µm) | 4 | 4 | 0.14 | 0.15 |
| Calculated $R_s$ (Ω/sq) | 51 | 51 | 1261 | 496 |
| Experimental $R_s$ (Ω/sq) | 47 | 48 | 875 | 550 |

### 3.2.3. Membrane characterization

A fabricated chip (16 mm×16 mm) is shown in Figure 16a. The microfluidic chip bears two 5 µm deep microchannels separated by a 10 µm thick porous silicon membrane. Figure 16b and 16c display cross-section SEM images of the fabricated ~4 µm high mesoporous membrane created by anodization at 200 mA cm$^{-2}$ during 1 min. It is important to note that the dopant concentration drops ~10 times within the membrane depth (see Figure 14), which could result in inhomogeneous pore size and porosity. However, this effect was hardly noticeable on the SEM observations (Figure 16c). Because of low boron concentration below the depth of 4 µm, few micropores are created in that region, as shown in Figure 16b. As expected, the current flows in a lateral fashion within the p++-layer in between the implanted n-layer and substrate, thus resulting in lateral pores formed through the membrane.

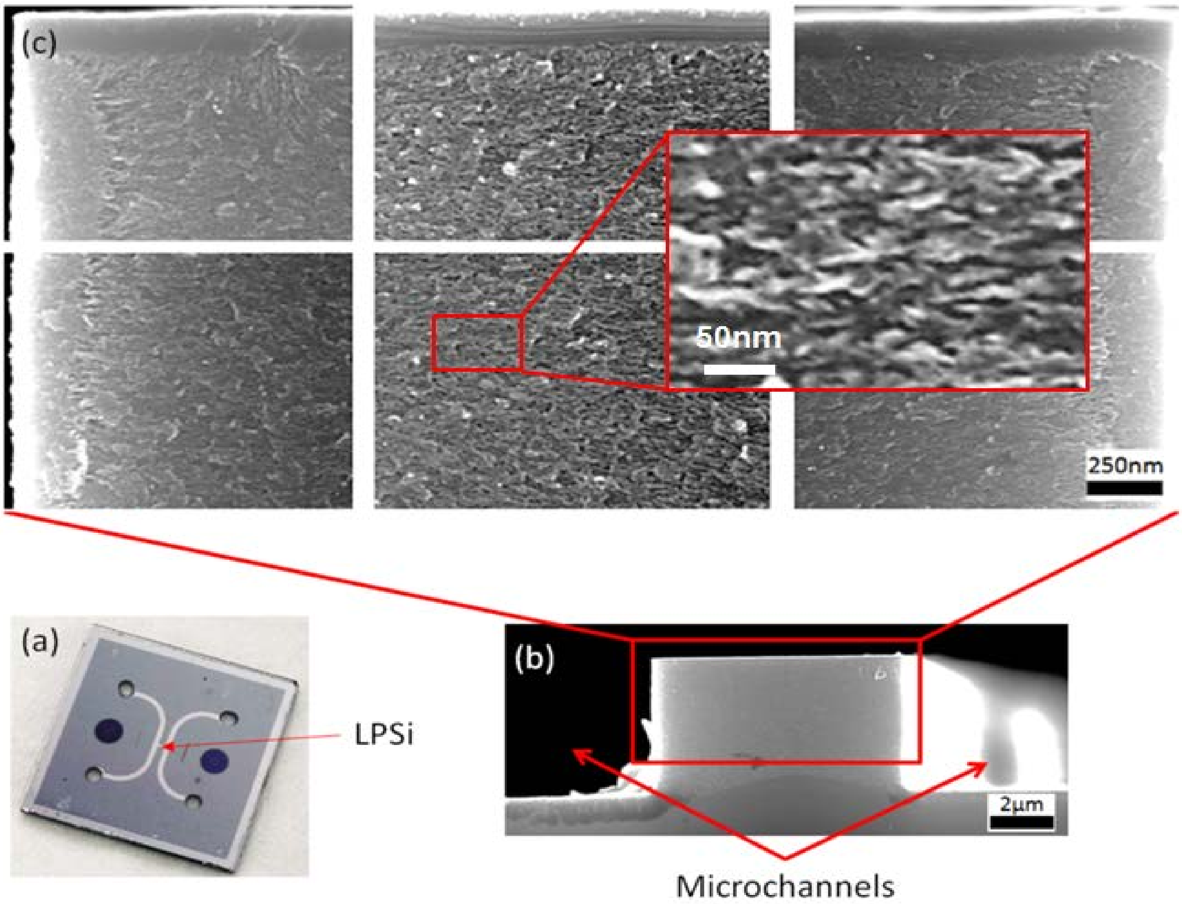

Figure 16. (a) Optical photograph of a fabricated fluidic chip integrating a lateral porous silicon membrane. (b) SEM picture of a lateral porous silicon membrane bridging two fluidic microchannels. The membrane is ~4 µm high and 10 µm thick (c) SEM close up images of the fabricated membrane including a ~150 nm thick protective n-type top layer without pores.

The current density represents the supply rate of holes during anodization, which greatly influences the pore morphologies. As a result, by manipulating the current density, we are able to tune the pore size and porosity of the fabricated membrane. Figure 17 shows SEM cross-sectional views of porous silicon created with current densities ranging from 20 mA cm$^{-2}$ to 500 mA cm$^{-2}$ (a-c). The resulting pore size and porosity of the fabricated membranes, estimated from the SEM pictures, respectively ranges from ~3 to ~30 nm and ~15 to ~65% (Figure 17d).

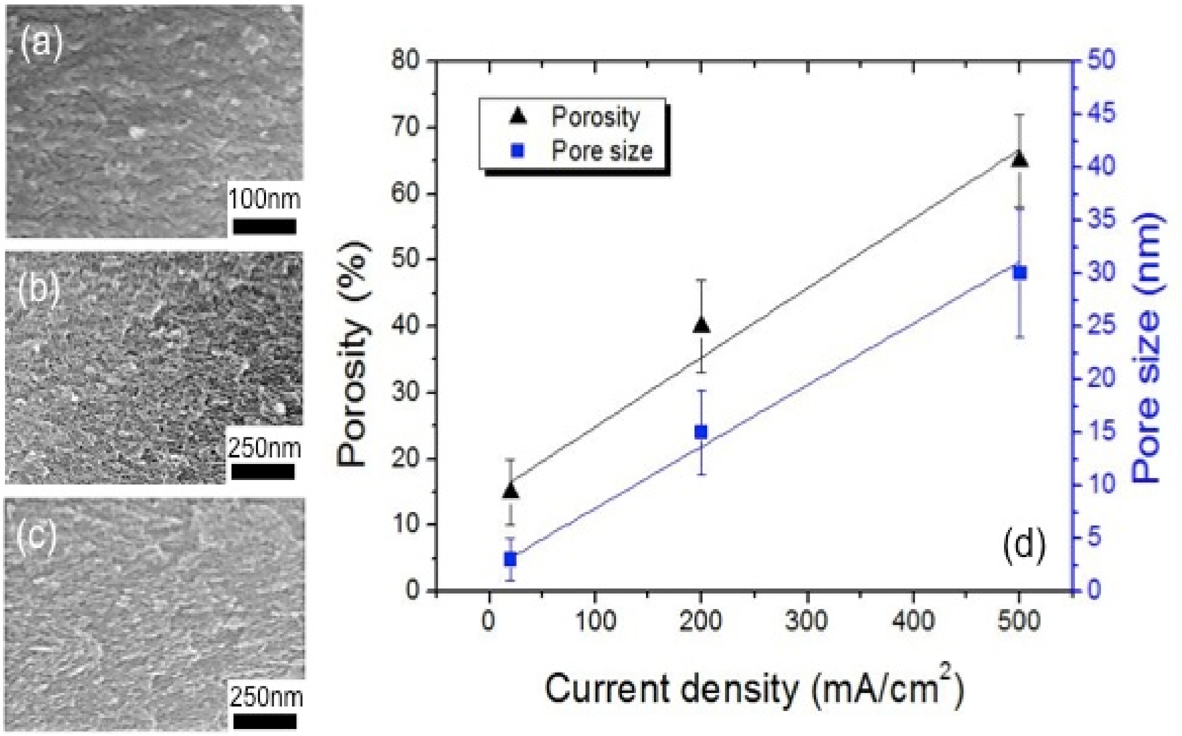

Figure 17. Lateral porous silicon membranes fabricated using different current densities: (a) 20 mA cm$^{-2}$ during 10 min. (b) 200 mA cm$^{-2}$ during 1 min. (c) 500 mA cm$^{-2}$ during 30 s. (d) Pore size and porosity as a function of current density.

## 4. Filtering capability and hydrodynamic resistance

In order to demonstrate that the fabricated pores are open-ended pipes that adequately connect the microchannels situated on both sides of the membrane. Test solutions containing various size objects were used to prove the dead-end filtration capability of the porous membranes (both the SOI type and the implantation type). Since the experimental procedures of both type membranes are similar, we focus on presenting the filtering experiments on the implantation type membranes. The hydrodynamic resistance of the fabricated membrane is an essential characteristic used in the design consideration of fluidic and lab on a chip devices. To this aim, the hydrodynamic resistance was estimated by the measuring pressure-driven flow velocity.

### 4.1. Filtering experiments

Filtering experiments on the implantation type membranes were carried out using solutions of various-size objects: fluorescein (Sigma, at 1µM diluted in PBS 1×), miRNA (Cy3-lablelled 26 bases single-stranded RNA from Eurogentec Inc., at 1 µM in PBS 1×), and 300 nm diameter beads (greenfluorescent polystyrene microspheres from Duke Scientific diluted in DI water at a concentration of $7.4 \times 10^5$ beads/mL). Phosphate buffered saline (PBS) 1× solution was loaded into one of the microchannels and test solutions were loaded into the opposite microchannel. A pressure generator (MFCS-8C, Fluigent) was used to push the test solution through the porous membrane with various pressures ranging from 0.1 to 1 bar. Fluorescein and miRNA solutions were prepared using PBS 1× to eliminate the electrostatic repulsion between negatively charged molecules and the negatively charged surface of the membrane as well as to minimize the Debye layer within the membrane [4]. All the solutions were degassed before use. Fluorescence images were recorded during the experiments by means of a IX70 Olympus inverted epifluorescence microscope equipped with 10× objective and dedicated filters (UMWIB3 from Olympus, U-M41007 and U-M41008 from Chroma), and an Andor iXon 885 EMCCD camera. The sequential images presented in Figure 18 show that fluorescein and miRNA molecules flow back and forth through the membrane while beads are stuck onto the membrane walls, thus proving the size-based separation capability of our membrane with a cut-off size >10 nm (hydrodynamic radius of Fluorescein and miRNA: ~1 nm and ~5 nm). These results are consistent with the average pore size of ~15 nm of the chip used for this experiment (membranes fabricated using a current density of 200 mA $cm^{-2}$).

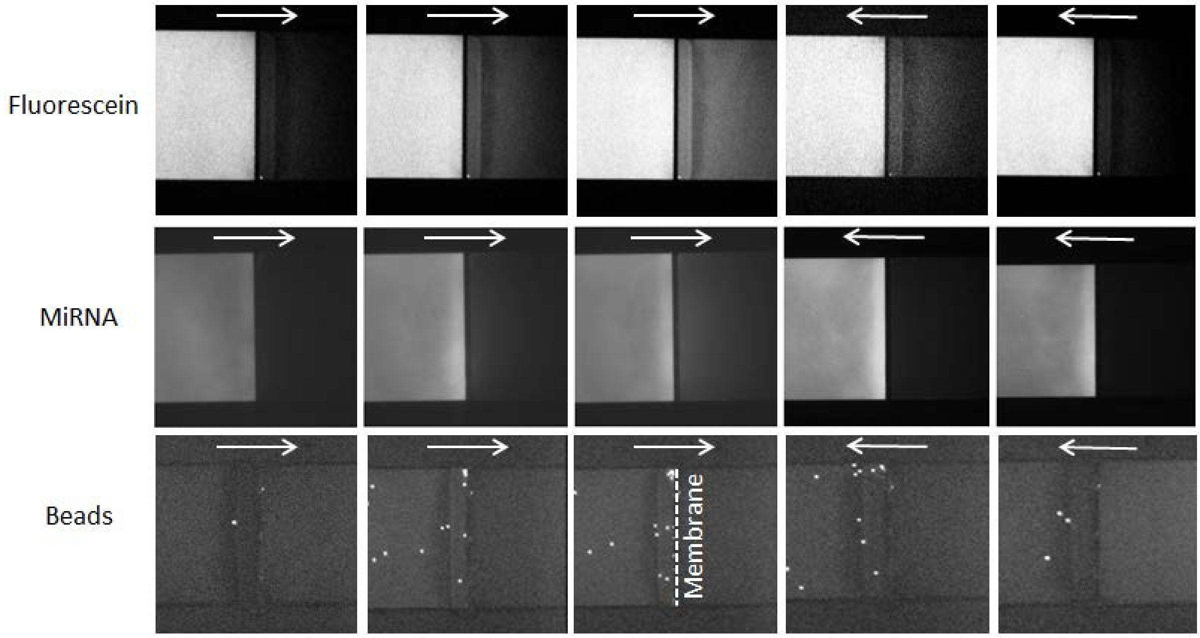

Figure 18. Filtering capability of the fabricated membrane tested by flowing solutions of fluorescein, short miRNA, and nanobeads. The white arrows indicate the direction of the fluid flow. Porous silicon membrane is located at the center of each image. Fluorescein and miRNA molecules can flow back and forth through the membrane unlike the nanobeads.

Filtering experiments on the SOI type chips were carried out using solutions of various-size objects: 300 nm diameter beads, 40-mers single stranded DNA (ssDNA) and immunoglobulin G (IgG) molecules. The outcome of these experiments is that full retention is achieved for 300 nm size beads, while small molecules (ssDNA and IgG) permeate the porous membrane. The experimental results indicate that the cut-off size of the fabricated membrane is larger than ∼10 nm (40-mer single-stranded DNA display a 4 nm minimum radius of gyration [19], and IgG molecules have a 5.29 nm hydrodynamic radius [20]), but much smaller than the 300 nm diameter of the beads. This range is consistent with the ∼25 nm average pore size of the fabricated membrane.

## 4.2. Measurement of the hydrodynamic resistance

The hydrodynamic resistance of the fabricated membrane, which is an essential characteristic used in the design consideration of fluidic and lab-on-a-chip devices, was experimentally estimated. To this aim, the pressure-driven flow velocity induced in the microchannels was measured by manually tracking the position of 300 nm fluorescein polymer microspheres for applied pressures ranging from 0.1 bar to 1 bar. In brief, following the experimental protocol described in the previous section, where beads were introduced into the left side microchannel, a constant pressure was generated at the inputs of the right hand side microchannel causing the particles to flow inward the left microchannel. This was conducted after ensuring that pressure was equilibrated between the various inlets/outlets (*i.e.* upon observation of a net null flow velocity with beads only experiencing Brownian motion). The particle velocity was measured in the straight channel and in the vicinity of the membrane by averaging the displacement of 6 nanobeads over time, where each particle position (pixel location) was directly extracted from the recorded images using ImageJ. To ensure that the measurements reflect the maximum flow velocity as adequately as possible, care was taken to position the focus plane in the middle of the channel depth and only beads in focus were tracked. Finally, giving the fact that particle velocity increases with applied pressure, measurements were carried out over 10 s at 1 bar applied pressure and up to 90 s at 100 mbar. The resulting increase of measured velocity with applied pressure is in shown in Figure 19.

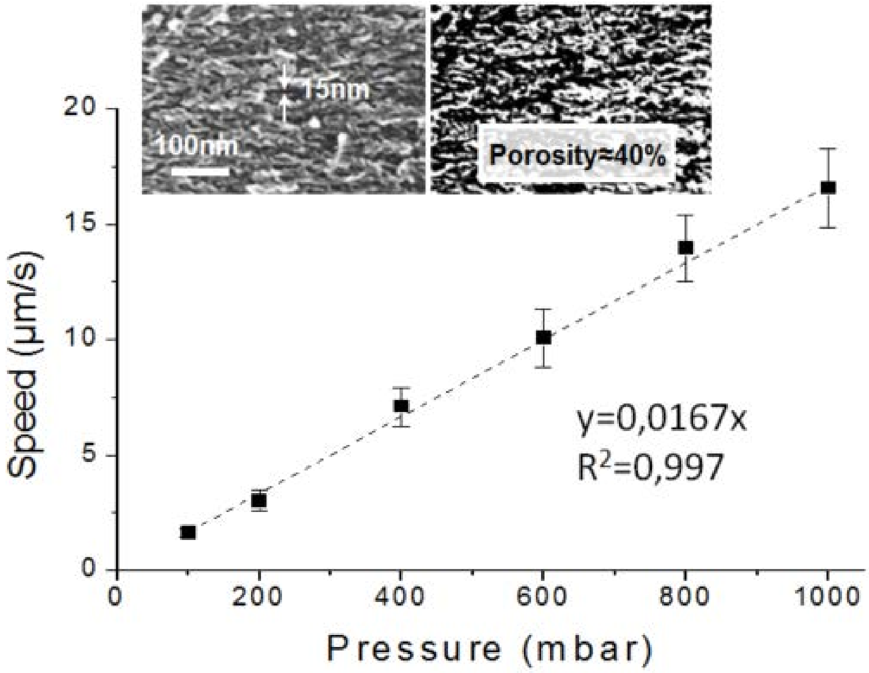

Figure 19. Graph showing the measured flow velocity as a function of the pressure applied across a membrane (implantation process). From the linear relationship, we can deduce the hydrodynamic resistance of the membrane. The two insets show SEM pictures of the porous membrane used to estimate the mean pore size and the layer porosity (the right inset shows a binary image after threshold conversion of the left inset image).

The hydrodynamic resistance of a fluidic network linearly relates the fluid flow, $Q$, to the applied pressure $\Delta P$. The resistance of the fabricated membrane, $R_h$, was thus extracted from the linear fit of the experimental data, by neglecting the resistance contribution of the microfluidic channels. This resulted in a value of 5.9 Pa s/µm$^3$ for the 10 µm thick porous membrane. Theoretically, the hydrodynamic resistance of an idealized membrane of cylindrical pores with the same radius can be obtained from the Hagen-Poiseuille equation [21], providing transport mechanisms other than laminar flow are neglected:

$$R_h = \frac{\Delta P}{Q} = \frac{8\eta l}{{r_p}^2 wh\phi} \tag{2}$$

where, $\eta$ is the fluid dynamic viscosity, $l$, $w$, $h$, and $\phi$ are the membrane length (*i.e.* thickness), width, height and porosity, respectively and $r_p$ is the pore radius. Neglecting the tortuosity of the pores and using the geometrical values for the fabricated membranes (where ~15 nm pore diameter and ~40% porosity were estimated from the SEM images shown in the inset of Figure 19), leads to a theoretical hydrodynamic resistance of 3.5 Pa s/µm$^3$. This value, which is more than 6 orders of magnitude higher than the resistance of a similar size microchannel without integrated membrane, is in accordance with the value obtained from flow velocity measurements and thus demonstrates that injected fluid indeed flows through the fabricated porous layer across the entire section of the microchannel.

For the SOI type membranes, the experimental value is $2.9\times10^{-1}$ Pa s/µm$^3$ which fit well with theoretical value ($2\times10^{-1}$ Pa s/µm$^3$), also proving that injected fluid flows through the entire section of the porous membrane.

## 5. Conclusion

In conclusion, we have presented two processes for the realization of lateral porous silicon membranes and their integration into planar microfluidic channels. The key ideas of the first process, the SOI process are to guide pore formation horizontally during anodization by means of electrodes patterned onto the silicon surface and to spatially localize porous silicon growth within a controlled depth through the use of silicon-on-insulator substrates. The feasibility of the SOI process is demonstrated by the fabrication of 10 µm thick mesoporous membranes with ~25 nm diameter pores bridging 20 μm deep microchannels. The second process, the implantation process relies on the local manipulation of dopant type and concentration by boron and phosphorus implantation. During anodization, pores propagate in a heavily doped boron layer sandwiched between a n-type surficial layer and the n-type bulk silicon in a strict lateral fashion along the current flow injected via a patterned electrode. We have modeled our process using a 2D simulation tool to estimate the dopant profiles after ion implantation and we have used four-point probe measurement to experimentally find the optimal doses by measuring the sheet resistance of the surficial layer. Membranes with lateral pores were successfully fabricated following this process and their functionality was demonstrated by conducting filtering experiments.

The main difference between the two proposed fabrication processes for lateral porous silicon membranes lies in the approach used to confine the formation of porous silicon where desired. The SOI process relies on the patterned electrodes in combination with the SOI buried layer to guide pore formation within the membrane. The disadvantage of this process is that the buried oxide layer is exposed to highly concentrated hydrofluoric acid during anodization, which limits the anodization time and thus the control of the membrane properties, such as pore size, porosity and membrane thickness. Moreover, since the top of the step is not fully insulated, part of the electrode situated on that top injects current vertically within the step: as a result, if the thickness of the step is smaller than its length, chances are high that the pores will mainly be connecting two areas on the top of the step vertically (from the electrode patterned on the top to the bare part of the top surface), rather than the sides of the step horizontally. As a result, the membrane will not adequately connect the side microchannels. This clearly limits the thickness to width ratio of membranes that can be fabricated by the SOI process.

The implantation fabrication process relies on the patterned electrodes as well, but it uses implanted n-type silicon layer and n-type substrate as native electric insulators and etch-stops, therefore avoiding the limitation of anodization time. In the presented work, we are thus able to obtain smaller pores by decreasing the current density while increasing the anodization time. Analogously, we can envision to obtain longer membrane by maintaining high current density while increasing the anodization time. The implantation process is however more complicated in terms of fabrication procedures due to the use of two ion implantation steps and the corresponding annealing processes. Also, the thickness of membranes fabricated by this means is limited by the implantation process (where increasing the junction depth is difficult to obtain even with longer annealing time) and is usually smaller that of the SOI process (however in this case, the metallization process much easier). Still, the results of both processes display their own advantages where the larger membrane depth obtained by the SOI process enables big volumetric flow rates through the membrane, while the shallower membranes obtained by the implantation process should provide better interferometric signal.

The two fabrication processes presented in this chapter enable the confinement of lateral porous silicon membranes at specific locations with desirable pore size and porosity into lab-on-a-chip devices. While obvious applications include on-chip sample preparation through size-based filtration as demonstrated here, such membranes could also be used for other purposes, such as sample pre-concentration and real-time biosensing. The two latter applications of lateral porous silicon membranes are investigated in the next two chapters of this manuscript.

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# Chapter 3.

# Lateral porous silicon membranes for on-chip sample preconcentration by means of ion concentration polarization

*In this chapter, we take advantage of the ion-selective property of our fabricated lateral porous silicon membrane to study the possibility to carry out on-chip sample preconcentration by means of ion concentration polarization (ICP). We first introduce the mechanism of ion concentration polarization and show how sample preconcentration can be achieved using this phenomenon. Then, we present a complete review of the various fluidic configurations for ICP preconcentrators including techniques to integrate ion-selective membranes (nanojunctions). We demonstrate the ion selectivity and counterion transport efficiency of the lateral porous silicon membranes by analyzing the ion depletion phenomenon and dedicated electrical characterizations. Finally, we present two configurations of lateral porous silicon devices to achieve ICP and hydrodynamic ICP preconcentration and compare our results to the state of the art.*

## 1. Introduction

Microfluidics is the science and technology of systems that process or manipulate small amounts of fluids ($10^{-9}$ to $10^{-18}$ liters), using channels with dimensions of tens to hundreds of micrometers [1]. The use of microfluidic lab-on-a-chip devices has enabled miniaturization of many biochemical techniques, leading to faster/cheaper/portable analysis using smaller amount of sample and reagents [2, 3]. Prior to sample analysis, sample pretreatment is normally required to obtain a purified/concentrated sample. The on-chip sample pretreatment includes many processes, such as separation, preconcentration and derivatization [4], among which sample preconcentration is a crucial step since first, it enables the detection and analysis of trace or low-abundance species, in another words, it improves the detection limit of biosensors, and second, it mends up the difference between volumes of samples available and those consumed for analysis.

On-chip sample preconcentration methods can be basically categorized into four groups [5, 6]: extraction, electrophoretic stacking, membrane filtration and evaporation, and ion concentration polarization. The extraction techniques are conventional sample pre-treatment methodologies where substances are extracted from a matrix by specific affinity. Solid-phase extraction [7] and liquid-liquid extraction [8] have both been introduced into miniaturized devices. Electrophoretic stacking is based on capillary electrophoresis (CE) where analytes are stacked by monitoring their electrophoretic mobility and the local electric field. Various CE techniques have been developed for preconcentration, including field-amplification stacking [9], isotachophoresis [10], and isoelectric focusing [11]. The membrane filtration and evaporation approach refers to the concentration of the analyte obtained using semipermeable membranes that remove the bulk liquid by filtration [12] or evaporation [13]. Ion concentration polarization (ICP) is an electrokinetic phenomenon based on selective charge transport through ion-selective nanojunction [14]. Recently, sample concentration based on the ICP phenomenon has been attracted great attention due to the following advantages for sample preparation [15]: it can achieve very high concentration factors and very fast stacking and it allows efficient electrokinetic trapping of molecules and releasing of collected molecules by electrical manipulation (without suffering from problems such as clogging, which can be the case for size-based concentration devices).

Ion concentration polarization devices make use of ion-selective nanojunction, which can take several forms as discussed in the next section. Porous silicon actually exhibits ion selectivity properties [16], this implies that it can be used for ICP preconcentration. In this work, we explore the possibility to use our fabricated lateral porous silicon membrane integrated into 2D microfluidics towards on-chip ICP for molecular concentration.

## 2. ICP preconcentration techniques

ICP preconcentration is a complicated method to implement because of the nonlinear nature of the electrokinetic phenomena used in the concentration process. In this section, we present the main mechanism involved in ICP preconcentration and the various device configurations. Since, the critical component of an ICP preconcentrator is the ion-selective nanojunction, we also review the fabrication methods used to integrate nanojunctions on chips.

### 2.1. Mechanism

An ion-selective nanojunction normally refers to a nanoporous membrane or a nanochannel that exhibits ion selectivity when the pore (or channel) size is comparable to the thickness of the electrical double layer (EDL) [15]. The EDL is due to the fixed surface charges at the solid surface that induces an oppositely charged region of counterions in the electrolyte to maintain the electroneutrality. The result is the formation of a screening region which is referred to as the EDL. In the nanojunction structures, the EDL can overlap under low electrolyte concentration (*e.g.*, <10 mM), resulting in a complete exclusion of co-ions (ions with the same polarity as the surface charges) due to the electrostatic repulsion, so-called the Donnan exclusion [17].

When a voltage is applied across a cation perm-selective nanojunction as shown in Figure 1, the ions migrate under the electric field according to their charges. On the anodic side, the cations pass through the membrane and the anions are driven away from the nanojunction. As a result, the concentration of both positive and negative ions decreases near the nanojunction, creating an ion depletion zone. On the cathodic side, the cations pass through the membrane and migrate towards the reservoirs, while the anions are hindered by Donnan exclusion. Thus, an ion-enrichment zone develops on the cathodic side of the membrane. It is important to note that the ICP is obtained even without the overlap of the EDL [18]. This is due to the fact that, although the nanojunction cannot fully prevent the transport of co-ions, the transfer of counterions is still much more important that of co-ion, leading to weak ion depletion at the anodic side of the nanojunction. This ion depletion phenomenon in turn increases the perm-selectivity of the nanojunction.

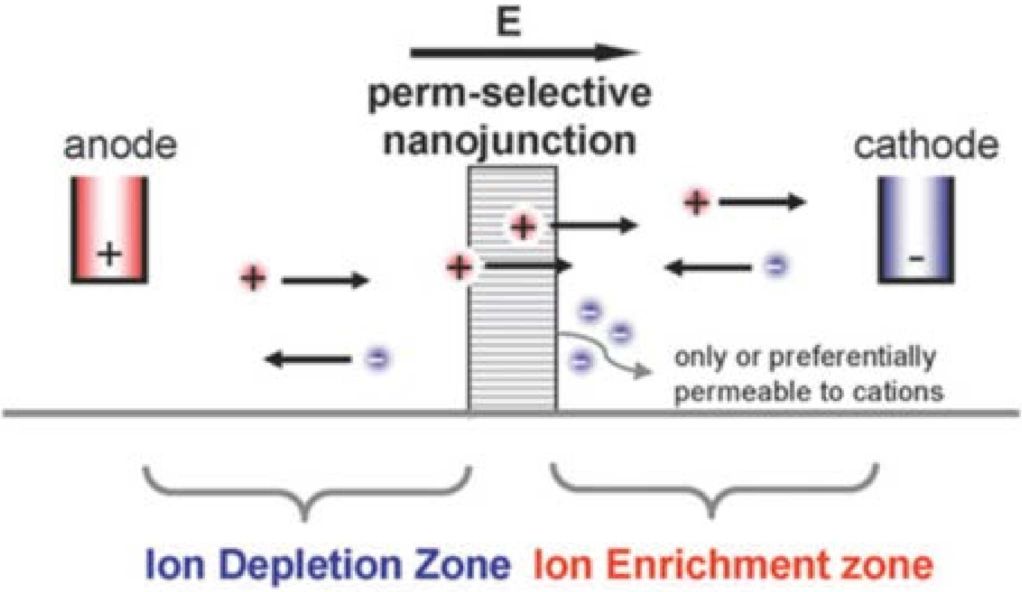


Figure 1. Schematic diagram of ion concentration distribution at the front and back of a cation perm-selective nanostructure which only lets cations pass through, resulting in ion depletion/enrichment zones [14].

It is well-known that the local electric field is influenced by the ionic concentration distribution. In the nanojunction, the concentration of counterions ($C_{counter}$) is higher than that of co-ions ($C_{co}$) due to the Donnan exclusion. Without any external electric field, the ion distribution in the microchannel is under equilibrium, which means that the cation concentration equals the anion concentration ($C_i$). Because $C_{counter} > C_i > C_{co}$ there is a local electric field at the nanojunction/microchannel interfaces (Figure 2a). On the other hand, the ICP phenomenon creates two concentration gradients at the anodic and the cathodic sides of the nanojunction. Thus, the electric field is enhanced in the ion depletion and ion-enrichment zones (Figure 2b).–Combining these two effects, the local electrophoretic flux of charged species, which is proportional to electric field, exhibits the particular shape shown in Figure 2c.

In addition to the electrophoretic flow (EPF), the electroosmotic flow (EOF) and hydrodynamic flow (HDF) are normally considered in a preconcentration fluidic system based on ion concentration polarization. The total flux ($J$) is governed by:

$$J = J_{EPF} + J_{EOF} + J_{HDF} = (\mu_{EP} + \mu_{EO})ES + J_{HDF} \quad (1)$$

Where $J_{EPF}$, $J_{EOF}$, and $J_{HDF}$ are the electrophoretic flux, electroosmotic flux and hydrodynamic flux, respectively; $\mu_{EP}$ and $\mu_{EO}$ are the electrophoretic mobility and electroosmotic mobility, respectively; $E$ is the local electric field; $S$ is the local section of the micro/nano/micro structure.

For a negatively charged nanojunction, the EPF of anionic species is in the opposite direction of the EOF (considered as a plug flow in both microchannel and nanojunction). If the EOF is smaller than the EPF and a HDF is added in the same direction as the EOF (from the anode to the cathode), the profile of electrophoretic flux of anionic species in Figure 2c will move up. The profile will thus intersect the x-axis, where the flow velocity of the analyte becomes zero and the preconcentration of anionic species occurs (Figure 2d). As a result, with the increase of EOF and HDF, four preconcentration regimes emerge, in order: cathodic stacking (CS), cathodic counter gradient focusing (CCGF), anodic counter gradient focusing (ACGF) and anodic stacking (AS) [19, 23]. Furthermore, in cases where EOF is larger than EPF, *e.g.*, when using buffers with high ionic strength, the four regimes can also be achieved by operating HDF in the reverse direction (*i.e.*, from cathode to anode). In fact, almost all the ICP preconcentration schemes are based on the competition of the fluxes, named counter-flow focusing [20]. Based on this general mechanism, different configurations of ICP preconcentration have been proposed and are discussed hereafter.

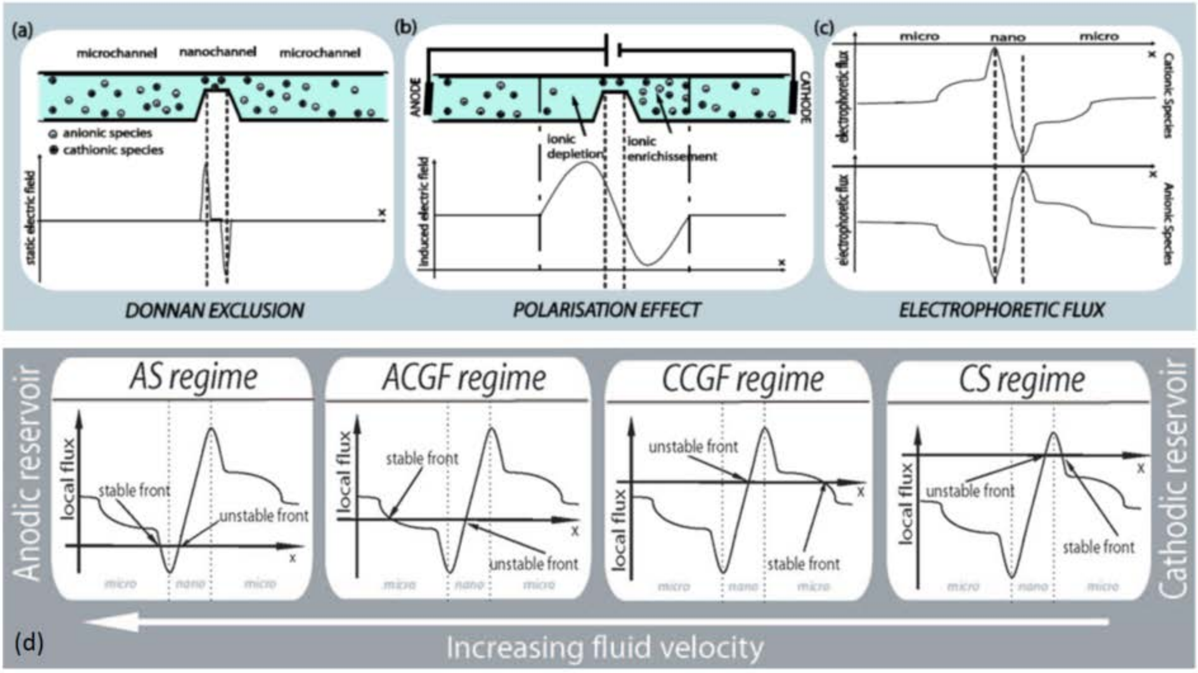


Figure 2. (a) Local electric field at the nanojunction/microchannel interfaces due to Donnan exclusion. (b) electric field distribution due to the concentration gradients by ICP. (c) electrophoretic flux of the cationic/anionic species in a the micro/nano/microchannel during a preconcentration process. (d) preconcentration regimes of anodic species under the dominance of electrophoretic flows as a function of electrophoretic vs electroosmotic vs hydrodynamic competition: cathodic stacking (CS), cathodic counter gradient focusing (CCGF), anodic counter gradient focusing (ACGF) and anodic stacking (AS) [19, 23].

### 2.2. Configurations of ICP preconcentrators

#### 2.2.1. Single-Channel preconcentrators with fully integrated Nanojunctions (SCN)

This configuration uses an integrated ion-selective nanojunction that fully connects inlet and outlet microchannels. Hlushkou et al., [21] have demonstrated the preconcentration performances of this configuration by using both negatively charged and neutral hydrogels as the nanojunction.  In the case of the neutral hydrogel membrane (Figure 3a), the negatively charged analyte is transported by electrophoresis and stopped by the membrane by size exclusion, resulting in concentration enrichment at the membrane–bulk solution interface. The ICP mechanism is not involved and the porous membrane only acts as a physical filter. In the case of negatively charged hydrogel membrane (Figure 3b), the ICP strongly affects the distribution of the local electrical field strength. The enrichment of analyte then is governed by electrophoresis, electroosmosis and Donnan exclusion.

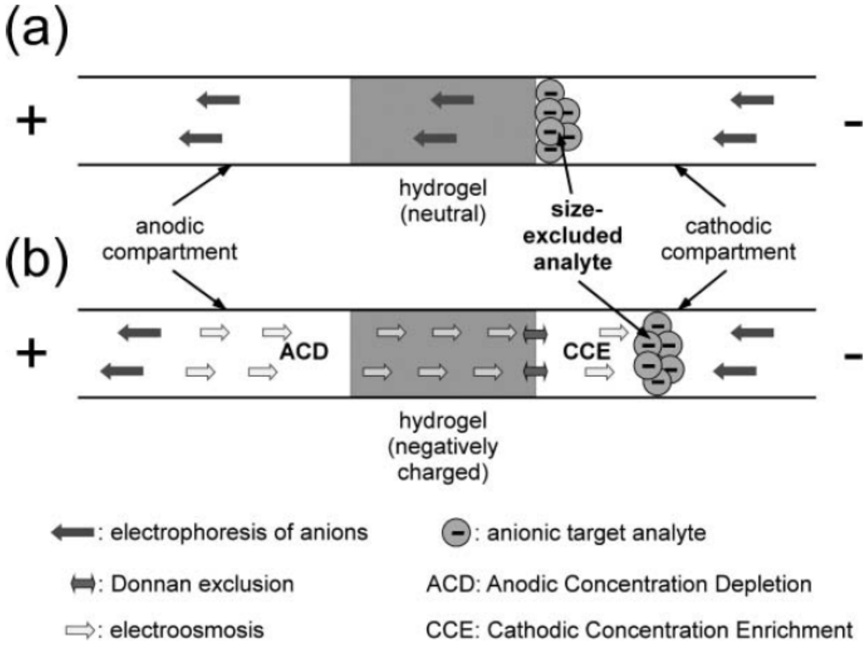


Figure 3. Electrokinetic concentration enrichment of negatively charged analyte at/close to the nanojunction of a neutral (a) and an anionic (b) hydrogel membrane [21].

### 2.2.2. Single-Channel preconcentrators with Surface-Patterned membrane (SCSP)

ICP preconcentration can also be achieved by patterning a piece of ion-selective nanoporous membrane in a single channel. Ko et al. [35] have compared this configuration to the fully integrated one (Figure 4a). When a voltage is applied at both reservoirs (Figure 4b), around the anodic side of the Nafion membrane, cations migrate through the membrane rather than through the microchannel due to its higher conductivity and anions migrate towards the anode, leading to the formation of an ion depletion region. With an additional flow (EOF or HDF) to counter the ion depletion, anions (and analytes) are trapped or accumulated in the region where the flow is balanced. This configuration has enabled the integration of a single membrane strip into multiple microchannels [35], and the integration of multiple membranes in a single channel [41]. For instance, Kwak et al. [41] have patterned two Nafion strips in a single channel to spatiotemporally locate the preconcentrated plug.

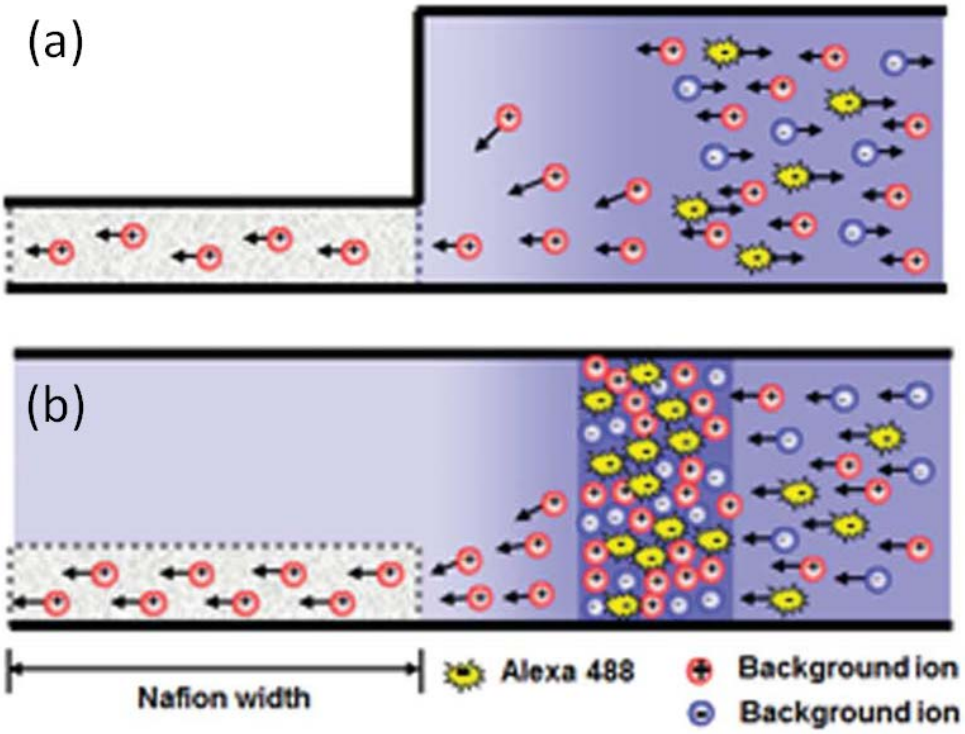


Figure 4. Schematic diagram of (a) fully integrated Nafion membrane and (b) surface-patterned Nafion membrane in a single microchannel [35].

### 2.2.3. Dual-Channel (DC) and Triple-Channel (TC) preconcentrators

The dual-channel preconcentrator consists of two parallel microchannels connected with a nanojunction. As shown in Figure 5, upon application of a voltage difference across the nanojunction, the ion depletion zone grows symmetrically and the zone propagates towards each reservoir. When there is a voltage difference between both ends of the anodic microchannel ($V_S > V_D$), the created tangential electric field ($E_T$) generates an EOF through the microchannel to transport the sample molecules into the ion depletion zone where they get trapped by the counter-flow focusing mechanism. Alternatively, instead of EOF, HDF can be applied at one end of the anodic microchannel for preconcentration. Compared to in the SCN configuration, the EOF or HDF are not applied through the nanojunction, thus enabling larger EOF or HDF for faster preconcentration.

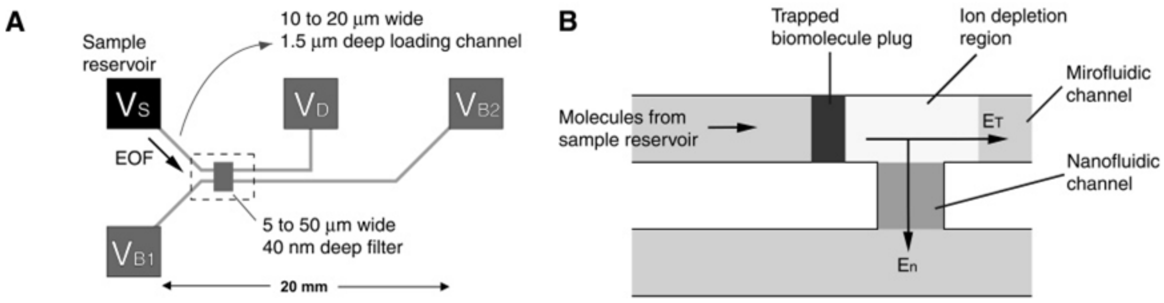


Figure 5. Schematic diagram of a dual channel preconcentrator [48]. (A) The layout of the device. (B) Schematic diagram that shows the concentration mechanism. Once proper voltages ($V_S > V_D > V_{B1} = V_{B2} = 0$ V) are applied, the trapping region and depletion region will be formed as indicated in the drawing. The $E_T$ specifies the electrical field applied across the ion depletion region, while the $E_n$ specifies the cross nanofilter electrical field.

An alternative to the dual-channel preconcentrator system, the triple-channel preconcentrator consists of three parallel microchannels connected with two nanojunctions as shown in Figure 6. The concentration mechanism is similar, but the TC provides a more stable and consistent performance in preconcentration due to the generation of symmetric and enhanced ion depletion zone [14, 18]. The TC configuration has been used for immunoassays [54, 60], where the assay sensitivity was proven to increase by more than two orders of magnitude.

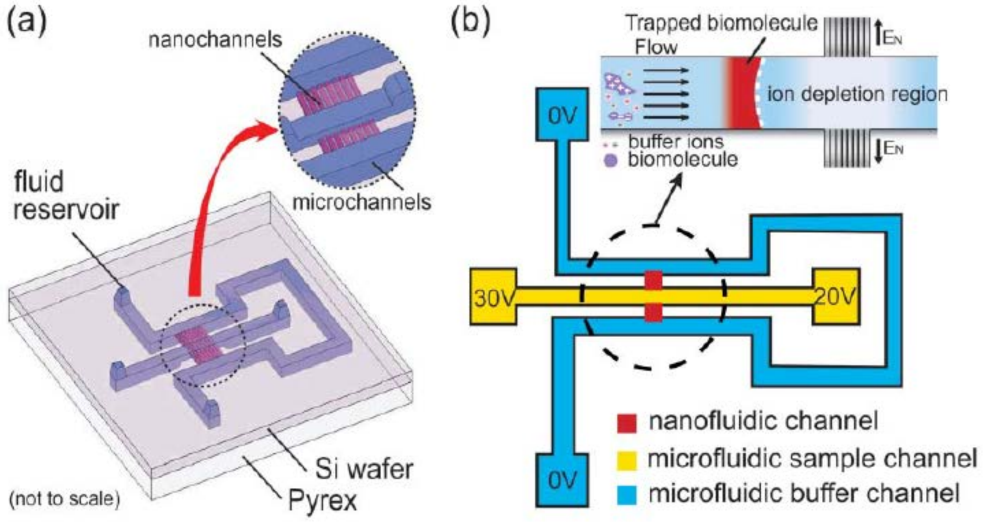


Figure 6. Schematic diagram of a triple channel preconcentrator and the electrical configurations under DC bias [60]. The middle sample channel is connected to the U shaped buffer channel by a nanochannel array (the nanojunction) with a depth of 40 nm. (b) Voltage scheme used for the biomolecule preconcentration and the electrokinetic trapping mechanism.

### 2.2.4. Performance review of ICP preconcentrators

The ICP preconcentration enables fast sample stacking, high preconcentration factors, without possible damage of the membrane by analytes flowing through. Table 1 reviews recent works on ICP preconcentration that focuses on the various configurations, the type of nanojunctions and the resulting preconcentration factors. Several conclusions can be made from this review: first, the nanojunction can be made from numerous materials but Nafion is the most popular one; second, the use of different analytes has proved a wide applicability of ICP preconcentration; third, in order to achieve high preconcentration factors, high voltage/pressure and long times (either or both) are normally needed.

Table 1. Review on ICP preconcentration (Abbreviations: SCN (Single-Channel preconcentrator with fully integrated Nanojunction), SCSP (Single-Channel preconcentrator with Surface-Patterned membrane), DC (Double channel preconcentrator), TC (Triple-Channel preconcentrator), $V_H$, $V_L$, and E represent high voltage, low voltage and electric field, respectively. P and F represent pressure and flow rate).

| Ref. | Type | Nanojunction | Analytes (initial concentration) | Factor (Time) | ($V_H$, $V_L$) (or E) /P (or F) | Comments |
|---|---|---|---|---|---|---|
| 21 | SCN | Anionic hydrogel | BSA (500 nM) | 400 (3 min) | 300 V | Comparison of neutral and anionic hydrogel membranes |
| 22 | SCN | Anionic hydrogel | Fluorescein (5 μM) | 100 (2 min) | 100 V | |
| 23 | SCN | Glass Nanochannel | Fluorescein (1.5 μM) | $10^3$ (4 min) | 80 V cm$^{-1}$ / 0.9 bar | Study of different EOF, EPF and HPF |
| 24 | SCN | Glass nanochannel | Fluorescein (30 μM) | 100 (0.5 min) | 1000 V | Demonstration of depletion and enrichment |
| 25 | SCN | Nanochannel formed between PDMS/glass | BSA (1 pM) | $10^6$ (30 min) | 200 V | EOF-dominated preconcentration |
| 26 | SCN | Nanofissures | FITC-DSA (100 pM) | $10^3$-$10^5$ (<10 min) | 80 V | |
| 27 | SCN | Nanofracture | λDNA (3.2 pg μL$^{-1}$) | $10^5$ (6 min) | 300 V | The use of fused silica capillary |
| 28 | SCN | Nafion-filled nanofracture | λDNA (0.32 μg mL$^{-1}$) | $10^3$ (15 s) | 200 V | |
| 29 | SCN | Nafion | Fluorescein sodium (1 μM) | $5\times10^3$ (5 min) | 20 V | Special EOF circulation |
| 30 | SCN | Zwitterionic polymer membrane | BSA (0.5 μM) | $10^4$ (<2 min) | 70-150 V | Electrophoretic filtration |
| 31 | SCN | Porous silicate | λDNA (10.7 | 100 (4 min) | 1000 V | Electrophoretic |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | layer | μg mL$^{-1}$) | | | filtration |
| 32 | SCN | PETE membrane | ssDNA (0.1 μg mL$^{-1}$) | 300-800 (5 min) | 100 V | Commercial membrane |
| 33 | SCSP | Nafion | FITC-BSA(1 pM) | 10$^{6}$ (40 min) | 25 V cm$^{-1}$ | |
| 34 | SCSP | Nafion | Fluorescein (0.01 μg mL$^{-1}$) | 4000 (30 min) | 100 V | Parallel concentrator |
| 35 | SCSP | Nafion | Fluorescent dye (10 ng mL$^{-1}$) | 10$^{3}$ (20 min) | 160 V | Parallel concentrator |
| 36 | SCSP | Nafion | Hemagglutinin (334 pg ml$^{-1}$) | 4 (15 min) | 80 V cm$^{-1}$/ 2 μL min$^{-1}$ | |
| 37 | SCSP | Nafion | Lipid vesicles | 160 (10 min) | 100 V | |
| 38 | SCSP | Nafion | Fluorescein (10 nM) | 944 (10 min) | 0-210 V | Paper-based preconcentration |
| 39 | SCSP | Nafion | Bromocresol green dye (10 μM) | 40 (2.5 min) | 50 V | Paper-based preconcentration |
| 40 | SCSP | Nafion | Fluorescein sodium (80 mM) | 60 (200 s) | 50 V | Paper-based preconcentration |
| 41 | SCSP | Nafion | FITC−albumin (1 μg mL$^{-1}$) | 10$^{5}$ (10 min) | 100 V | Spatiotemporally location of the concentrated plug |
| 42 | SCSP | Nafion coating in capillary | Fluorescent dye | 214 (12 s) | 400 V / 40 mL.min$^{-1}$ | |
| 43 | SCSP | Bipolar electrode | BODIPY$^{2-}$ (0.1 μM) | 560 (<4 min) | 90 V | |
| 44 | SCSP | Bipolar electrode | BODIPY$^{2-}$ (10 pM) | 5×10$^{5}$ (150 min) | 0-600 V | |
| 45 | SCSP | Bipolar electrode | [Ru-(bpy)$_3$]$^{2+}$ (10 μM) | 141 (300 s) | 60 V | Preconcentration of cations by Faradaic ICP |
| 46 | DC | Nafion | DNA (25 nM) | 1150 (4 min) | $V_H$-$V_L$=80 V | |
| 47 | DC | Nafion | BSA | 2×10$^{4}$ (7 min) | 15 V/5 V | |
| 48 | DC | Oxide nanochannel | GFP (33 fM) | 10$^{7}$ (60 min) | 10 V/5 V | |
| 49 | DC | Polystyrene nanoslits | BSA (10 nM) | 10$^{4}$ (60 min) | 120 V/1.52 kPa | |
| 50 | DC | Bipolar electrode | BODIPY$^{2-}$ (1 μM) | 264 (3 min) | 30 V | |
| 51 | DC | Porous titania membrane (sol-gel) | 2,7-dichlorofluorescein (31 nM) | 4×10$^{3}$ (7 min) | 300 V, 150 V | |
| 52 | DC | HEMA-AA, HEMA-DMAEMA, Nafion, Agarose | FITC-BSA (5 nM) | 10$^{3}$ (10 min) | 50 V, 25 V | Convenient integration of different membranes |
| 53 | TC | Nafion | Fluorescent dye (0.1 nM) | 10$^{4}$ (7 min) | 120 V / 35 nL min$^{-1}$ | |

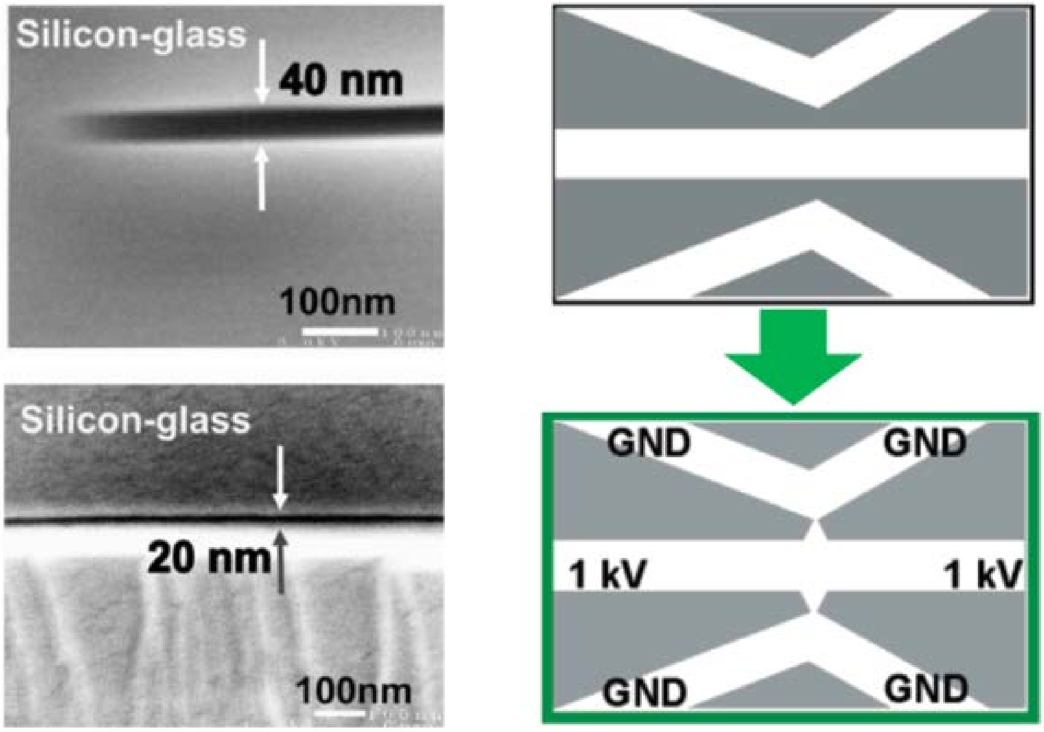
| | | | | | | |
|---|---|---|---|---|---|---|
| 54 | TC | Nafion | R-Phycoerythrin (1 ng mL$^{-1}$) | 1000 (5 min) | $V_H$-$V_L$=15 V/ 50 pL min$^{-1}$ | |
| 55 | TC | Nanofractures | Cy3-labeled cell lysate (7.2 ng µL$^{-1}$) | 5.6 (30 min) | 50 V, 47 V | Membrane generated by electric breakdown |
| 56 | TC | PDMS nanogap | R-phycoerythrin (400 pM) | $10^4$ (55 min) | 100 V, 90 V | Membrane generated by electric breakdown. |
| 57 | TC | Nafion | β-galactosidase (5µg/mL) | 100 (instant) | 50 V/ 0.03 µL min$^{-1}$ | |
| 58 | TC | colloidal silica beads | DNA (10 nM) | 1700 (10 min) | 30 V, 25 V | |
| 59 | TC | Nafion | β-phycoerythrin (40 pM) | $10^4$ (5 min) | 50 V, 25 V | |

### 2.3. Technical implementation

Nanojunctions can generally be classified into two categories: nanochannels and nanoporous membranes. As previously discussed, ICP can be achieved without a full overlap of the EDL. Therefore, the size of the nanochannels or pores does not have to be very precisely controlled and several techniques have been developed to create nanojunctions.

#### 2.3.1. Fabrication of nanochannels

The fabrication of nanochannels can be achieved by standard photolithography and etching techniques (Figure 7a) [23, 24, 48]. In that case, the channel dimensions can be precisely controlled, which is very useful for the study of the ICP phenomenon. Another approach is to obtain the nanochannel by electric breakdown after first creating inlet- and outlet microchannels that need to be very close at some location (Figure 7b) [26, 55, 56]. Nanochannels can also be created through PDMS-glass bonding. It has been demonstrated that during the bonding process, a nanoscale channel forms between the PDMS and the glass because of the weak reversible bond [25]. Besides, Wu et al. have created nanochannels by generating a nanofracture on a fused silica capillary [27]. Also, Yu et al. [49] have successfully fabricated a layer of nanoslits through lithography-free nanocracking on a polystyrene substrate, which was later bonded to a PDMS substrate.



(a) (b)

Figure 7. (a) Cross-sectional SEM images of nanochannels with different depths on silicon substrate (bottom wafer) bonded to a borofloat wafer (top wafer) [61]. (b) Schematic diagrams for nanogap formation by electric breakdown [56].

### 2.3.2. Fabrication of surface-patterned nanojunctions

Since nanoporous membranes are usually volumetrically larger than nanochannels, they lead to higher counterion transport efficiency and perm-selectivity. Thus, nanoporous membranes are more frequently employed for ICP preconcentration. Nafion is the most popular ion-selective membrane material. As previously described, surface patterning of Nafion membranes is an important technique for single-channel ICP preconcentration. In fact, surface-patterned Nafion membranes are also widely used in DC and TC [46, 59, 62]. Lee et al. [59] have recently proposed two promising patterning methods shown in Figure 8. In the 'micro flow patterning' method, liquid Nafion resin is first filled into, and then flushed out from microchannels in a PDMS mold, leaving a thin layer of Nafion on the substrate. After curing the resin, a PDMS chip with microchannels is bonded on top of the patterned glass substrate by standard plasma bonding. In the 'micro stamping' method, a PDMS microstamp is first inked with Nafion resin, which is then transferred to a glass slide by direct printing. The membrane integration is then obtained following the same process.

Besides, there are two methods for realizing paper-based preconcentrators: one consists in dropping Nafion solution onto a piece of paper and then drying [38, 39]; the other one consists in integrating a piece of Nafion membrane on an external substrate, while the paper acts as microchannels [39, 40].

On the other hand, there is an ICP-similar phenomenon called Faradic ICP [44]. The mechanism relies on the transfer of net charges via Faradaic reactions at a surface-patterned bipolar electrode. Bipolar electrodes are usually made from gold and are thus normally deposited and patterned using standard microfabrication techniques [43-45, 50].

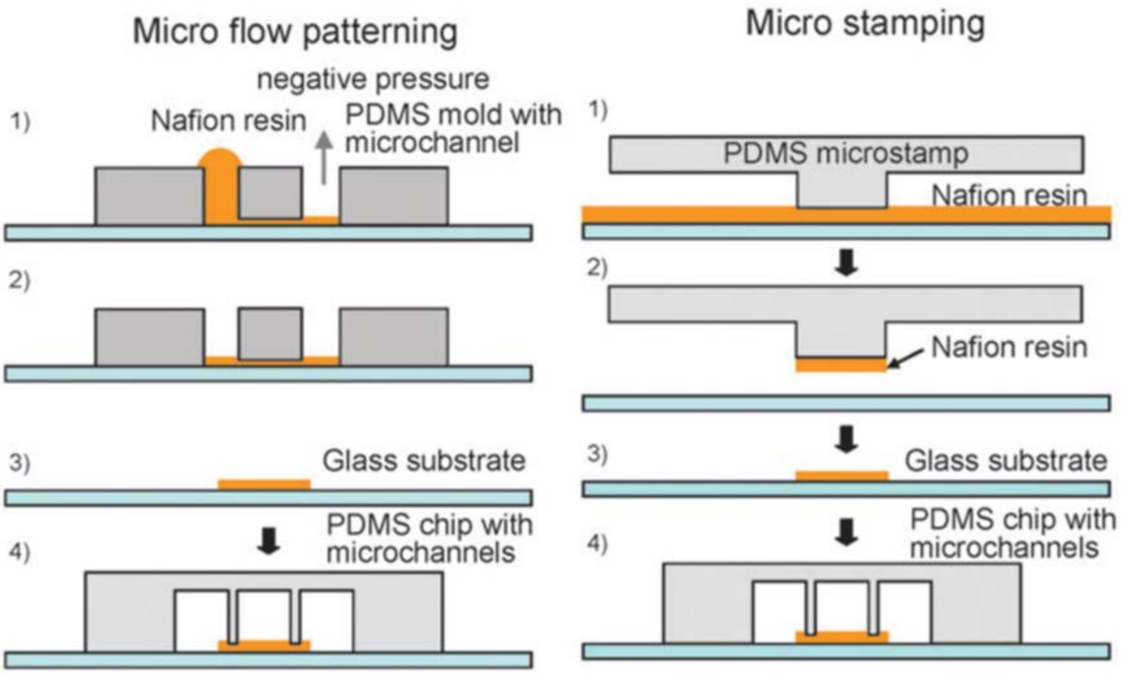


Figure 8. Fabrication of PDMS preconcentration chips with ion-selective membranes patterned using micro flow patterning in microchannel (left) and micro stamping technique (right) [59].

### 2.3.3. Fabrication of bulk membranes within microchannels

Although the surface patterning techniques have been widely used to fabricate ICP preconcentration devices, the thickness of the integrated membranes is quite limited and so is the counterion flow. As a result, means to integrate bulk Nafion membranes into microfluidics have been developed (Figure 9). First, the Nafion resin is pipetted into buffer channels and allowed to enter micro-junctions via capillary forces. Then, the excessive resin is removed by applying a gentle negative pressure in the buffer channels. Finally, the Nafion resin is cured. Alternatively, the resin can be filled in separate filling channels without the need to retreat the Nafion resin (Figure 9d). The key of this method is to control the viscosity of Nafion resin to achieve structural integrity of the membrane. If the viscosity is too high, the resin losses its flowability and filling the micro junction is hard to achieve. However, if the viscosity is too low, the shrinkage of the resin during the curing process can cause a leakage between the sample and buffer channels. This mechanism has been used in many works for the integration of Nafion membranes [54, 57, 62] and other ion-selective nanojunctions [52, 58].

Another popular integration method is photopolymerization. The process consists in filling the microchannel with a precursor solution first, followed by an UV exposure focused on the desired location to polymerize the precursors. The last step consists in removing the unpolymerized precursor solution. This technique has been used for the integration of hydrogel membranes [21, 22] and zwitterionic polymer membranes [30].

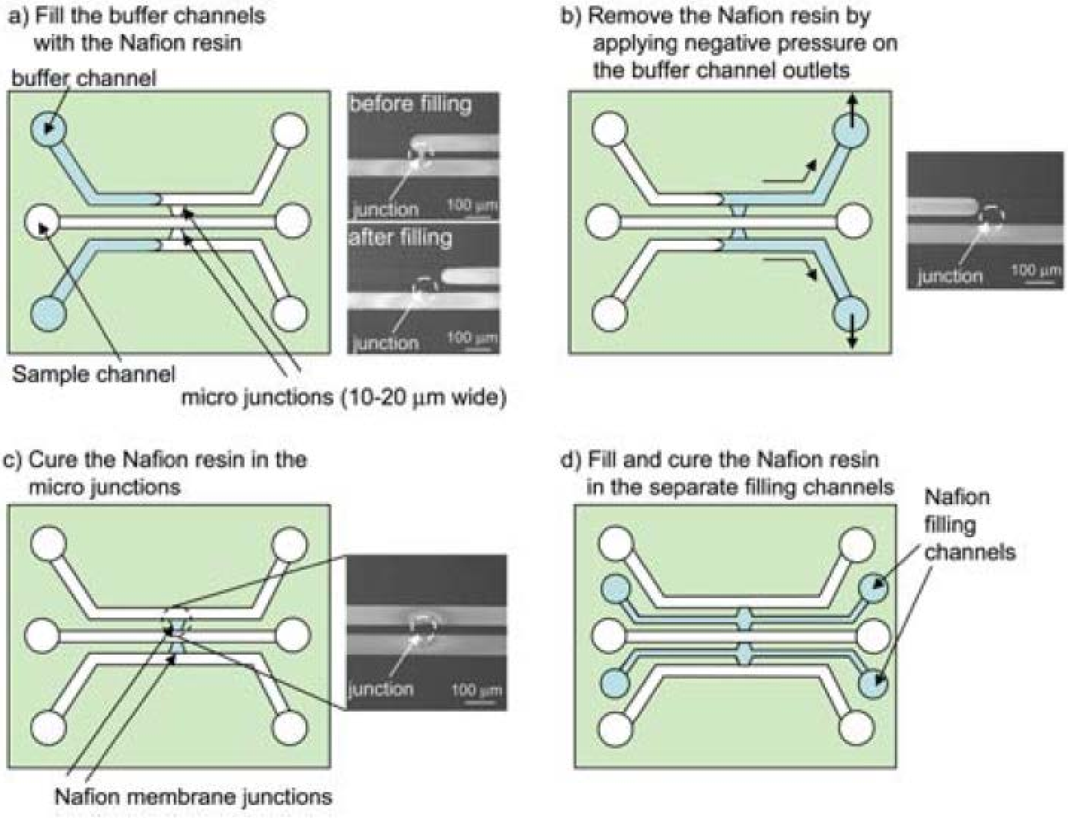


Figure 9. Schematics of the capillary-valve-based fabrication method [54].

## 3. Motivation for lateral porous silicon ICP preconcentrator and chip design

When analyzing the fabrication methods of ion-selective nanojunctions, we can notice that nanoporous membranes are always integrated into the microfluidic devices by introducing extra materials. This limits the reproducibility of membrane integration and preconcentration performances. In the previous chapter, we have presented two fabrication processes of lateral porous silicon membranes for their monolithic integration into microfluidic devices. The LPSi membranes are negatively charged in physiological solutions (*e.g.* pH≥7) due to the native silicon oxide (~1 nm) formed on the pore wall under atmospheric conditions, it should exhibit ion selectivity properties and enable ICP. The aim of the work presented in this chapter is thus to test the ion selectivity and ICP preconcentration capability of the fabricated membranes.

Between the two kinds of fabricated LSPi membranes (via the SOI and the implantation processes), the membranes fabricated by the SOI process displays larger membrane cross-sectional area and smaller hydrodynamic resistance, which is beneficial for larger hydrodynamic flow capability and theoretically higher concentration factors. Therefore, the ICP tests conducted in this work were mainly carried out with the SOI type devices. As discussed in Chapter 2, we have designed two kinds of chips: a ‘Dual-Channel’ (DC) type and a ‘Single-Channel with fully integrated Nanojunction’ (SCN) type. Figure 10 shows optical pictures of both types of chips: the DC type chip consists of two parallel microchannels connected by a lateral porous silicon membrane (where the gray circle under the membrane is the trace left from silicon anodization), and the SCN type chip consists of one microchannel that is obstructed by a lateral porous silicon membrane.

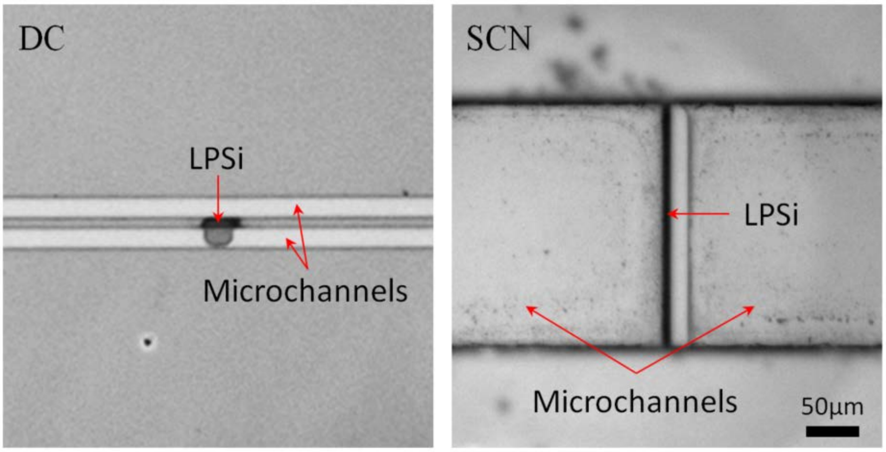


Figure 10. Optical pictures of the two types of lateral porous silicon chips: the ‘Dual-Channel’ (DC) type (left) and a ‘Single-Channel with fully integrated Nanojunction’ (SCN) type (right).

# 4. Materials and methods

## 4.1. Experimental setup

ICP experiments were carried out using the setup presented in Chapter 2, *i.e.* an IX70 Olympus inverted epifluorescence microscope equipped with an EMCCD camera (Andor) and a light source (Lumencore) (Figure 11a). The LPSi chips were mounted into a chip holder (Figure 11b) that enabled application of both pressure and electric potentials. The chip holder consisted of a bottom aluminum support, a middle PEEK part bearing the reservoirs and a top PEEK part for pressure input (Figure 11c). Four platinum wires of diameter 1 mm (Goodfellow, Cambridge, UK) were integrated into the reservoirs to apply electric potentials to the microfluidic device. O-rings and metal screws were used at each interface to ensure a good sealing performance. The pressure was managed by the pressure controller (MFCS-8C, Fluigent) and the electric potentials were monitored by two source meters (Keithley 2450 and 2430). Electrical characterizations were carried out using the Keithley 2450 source meter controlled by the KickStart software, and Ag/AgCl electrodes [56]. For ease of operation, the top PEEK part was removed and four Ag/AgCl electrodes were placed into the reservoirs and fixed onto the microscope stage.

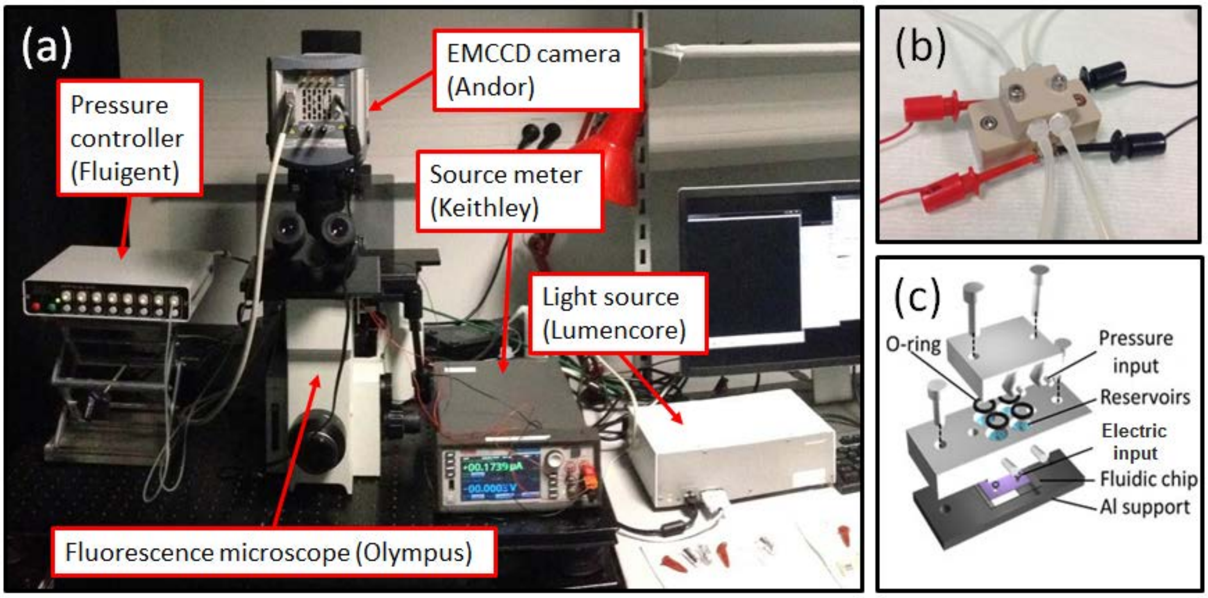


Figure 11. (a) Experimental setup for performing ICP experiments. (b) Fabricated chip holder. (c) Schematic diagram of the chip holder [66].

### 4.2. Test solutions

PBS solutions containing various concentrations of Fluorescein and miRNA were used in the ICP preconcentration tests. Fluorescein and miRNA are small molecules (hydrodynamic radius: ~1 nm and ~5 nm) that can freely pass through the LPSi membranes as was demonstrated in the filtering experiments presented in Chapter 2. Fluorescein has been widely used in ICP study [19, 22-24, 34, 38] as a negatively charged molecule (pI = 5.5~6 [63]). Micro-RNA (miRNA) are an important class of biomolecules that play a key role in the post-transcriptional regulation of gene expression [64]. It is also negatively charged (pI ≈ 6 [64, 65]) in PBS buffers (pH 7.4). The solvent ionic strength is very important for the ICP phenomenon mainly because it influences the Debye length in the membrane pores. In our experiment, we have used PBS buffer (Sigma-Aldrich) with 3 ionic strengths: PBS 0.1× (~15 mM, pH 7.4), PBS 1× (~150 mM, pH 7.4) and PBS 10× (~1.5 M, pH 7.4).

## 5. Experiments with LPSi Dual-Channel devices (DC)

### 5.1. Ion depletion phenomenon

Since ICP preconcentration is based on the perm-selectivity property of the nanojunction, it is of utter importance to first demonstrate the perm-selectivity of the LPSi membranes. In the former section, we have explained the mechanism of ICP in which the ion depletion phenomenon is the key feature. The observation of ion depletion phenomenon is thus a way to demonstrate membrane perm-selectivity.

In this experiment, the microchannels were filled with a solution of fluorescein (1 µM in PBS 0.1×). The chip was electrically connected as shown in Figure 12a and Ag/AgCl electrodes were used for electrical characterizations. Upon application of 2 V across the membrane, the initial depletion boundary indicated by a dark zone where fluorescein is not present reached the channel wall opposite to the membrane within 2 s (from Figure 12b to 12c, Figure 12d and 12e).

In the filtering experiment (Chapter 2), we have demonstrated that the membrane cut-off size is larger than 10 nm, so fluorescein (~1 nm) is small enough to pass through the membrane. Here, fluorescein is rejected from the membrane vicinity, which is not observed anymore at higher ionic strength (1.5 M, PBS 10×), where the disappearance of the ion depletion phenomenon is a demonstration of the cation perm-selectivity of the fabricated membrane.

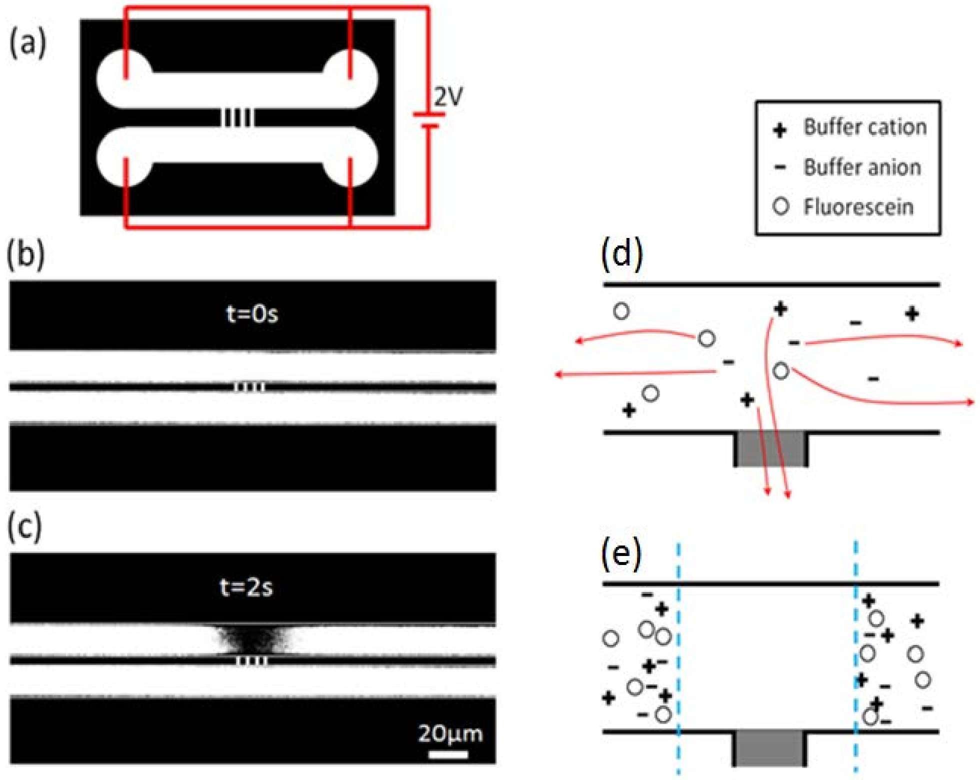


Figure 12. Ion depletion zone is formed at the anodic microchannel when 2 V is applied across PSi membrane using fluorescein 1µM in PBS 0.1× (pH 7.4). (a) Electrical connections. Optical pictures and schematics of the fluidic chip upon application (b, d) and 2 s after applying (c, e) 2 V across the membrane.

Compared to other works, it only takes 2 s to form the depletion zone across the channel, which is ~10 times faster and requires ~5 times lower voltage than silicon nanochannel-based devices with the same dimensions [18]. Here, we also report that the ion depletion zone can be created at an ion strength of 150 mM (PBS 1×) within 3 s by applying 4 V across the membrane, which is 15 times higher than the ionic strength conditions for the nanochannel device [18]. We believe that this is due to the high counterion transport efficiency of the LPSi membranes compared to silicon nanochannels. Indeed, the calculation of hydrodynamic resistance presented in Chapter 2 indicates that the volumetric flow rate for the LPSi membrane should be almost 40 times higher than that of a 40 nm thick silicon nanochannel [18], which implies the high counterion transport efficiency of the LPSi membrane.

## 5.2. Electrical characterizations

For further analysis of the ICP phenomenon in our fluidic device, we have measured the electric current passing through the membrane as a function of time and applied voltage. The formation of ion depletion zone implies that both cations and anions are repulsed from that zone, which turns into an insulating zone. Thus, the conductivity declines with the spread of the ion depletion area, as can be seen from the current drop observed in Figure 13 (recorded for PBS 0.1×, 1× and 10× with 1 µM fluorescein for fluorescence observation for an applied voltage of 2 V).

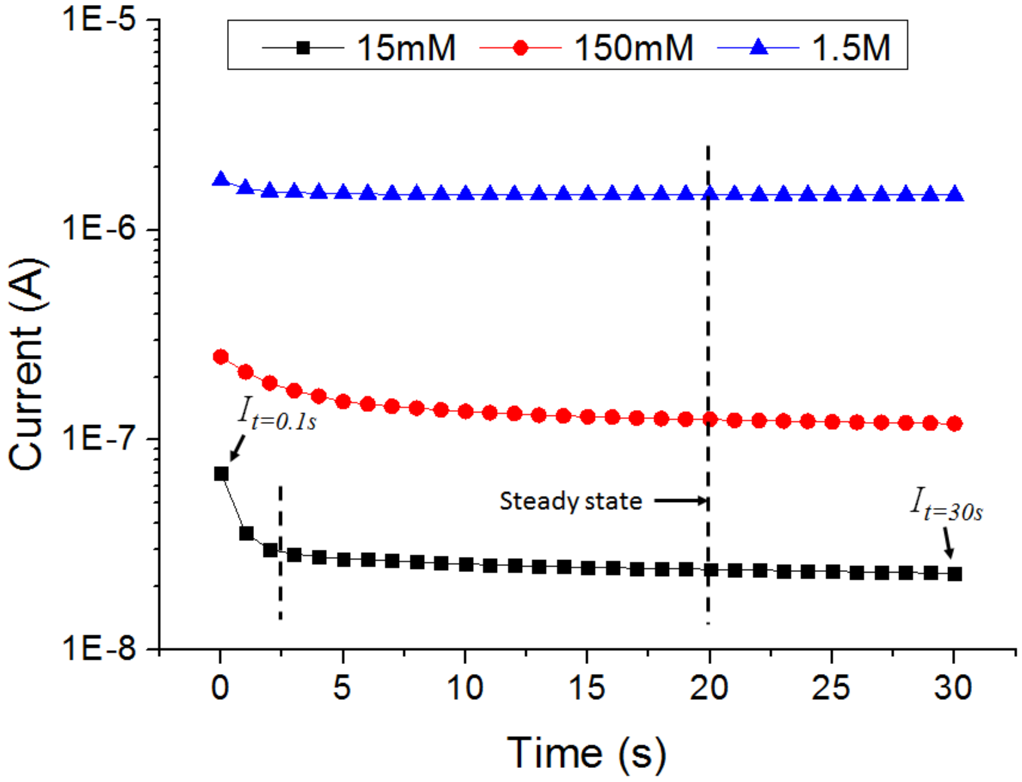


Figure 13. Ionic current-time curves recorded from the ion depletion tests for various PBS concentrations.

For PBS 0.1×, the current drops sharply from 70 nA to 29 nA within the first 2 s, which corresponds to the establishment of the ion depletion zone that indeed blocks the current. At higher ionic strength (150 mM), the current declines during the first 8 s but there is no sharp current drop: the fluorescence observation shows that the intensity near the anodic side of the membrane indeed decreases within the first 8 s, but a clear ion depletion boundary fails to develop. For the highest ionic strength (1.5 M), only a slight decrease of current happens and fluorescence detection shows no sign of ion depletion, which makes sense since the Debye length at 1.5 M is only of ~2.5 Å according to Debye-Hückel approximation [15], while the pore size is 25 nm.

Since the current decay is caused by the ion depletion phenomenon which originates from the permselectivity of the LPSi membrane, it seemed reasonable to assume that the current difference between the starting state ($I_{t=0.1s}$) and the steady state ($I_{t=30s}$) represents the membrane permselectivity. Therefore, we define the relative permselectivity ($\delta$) of the membrane for a given ionic strength as [52]:

$$\delta = \frac{I_{t=0.1s} - I_{t=30s}}{I_{t=0.1s}} \tag{2}$$

This yields relative permselectivities of 67%, 52% and 15% for ionic strength of 15 mM, 150 mM and 1.5 M, respectively. Using a similar method, Kim et al. [52] calculated a value of ~62% for Nafion membranes at ionic strength of 100 mM, which implies that the permselectivity of the LPSi membrane might be equivalent to that of Nafion membranes.

Next, in order to study the current-voltage (I-V) behavior of the LPSi device, we have ramped up the applied voltage from 0 V to 4 V (with 0.1 V increment) and the current was recorded every 3 s. The I-V curves are presented in Figure 14. When PBS 10× is used, the permselectivity of the LPSi membrane vanishes due to the high ionic strength, thus the I-V relationship is linear due to the dominance of electrical resistance of the membrane (ohmic regime). The ohmic regime is also observed at lower ionic strength (15 mM) when the applied voltage is very low (<1 V), before forming the ion depletion zone. As the voltage increases and the ion depletion zone forms, the current that can pass through the membrane is limited (limiting regime). Further increase of voltage (>3 V) leads to fast increase of current (overlimiting regime), which in previous studies using nanochannels junctions is attributed to strong irregular nonlinear flows merging and mixing for voltages >7 V [18]. However, since we observe this phenomenon at lower voltages, *i.e.* 3 V, we speculate that our overlimiting regime is rather caused by current leakage in our device because it might not be perfectly insulated. At medium ionic strength (150 mM), there is no obvious current-limiting state, however we observe ion depletion between 3 V and 4 V: this might also indicate that the current limiting and current leakage happens at the same time.

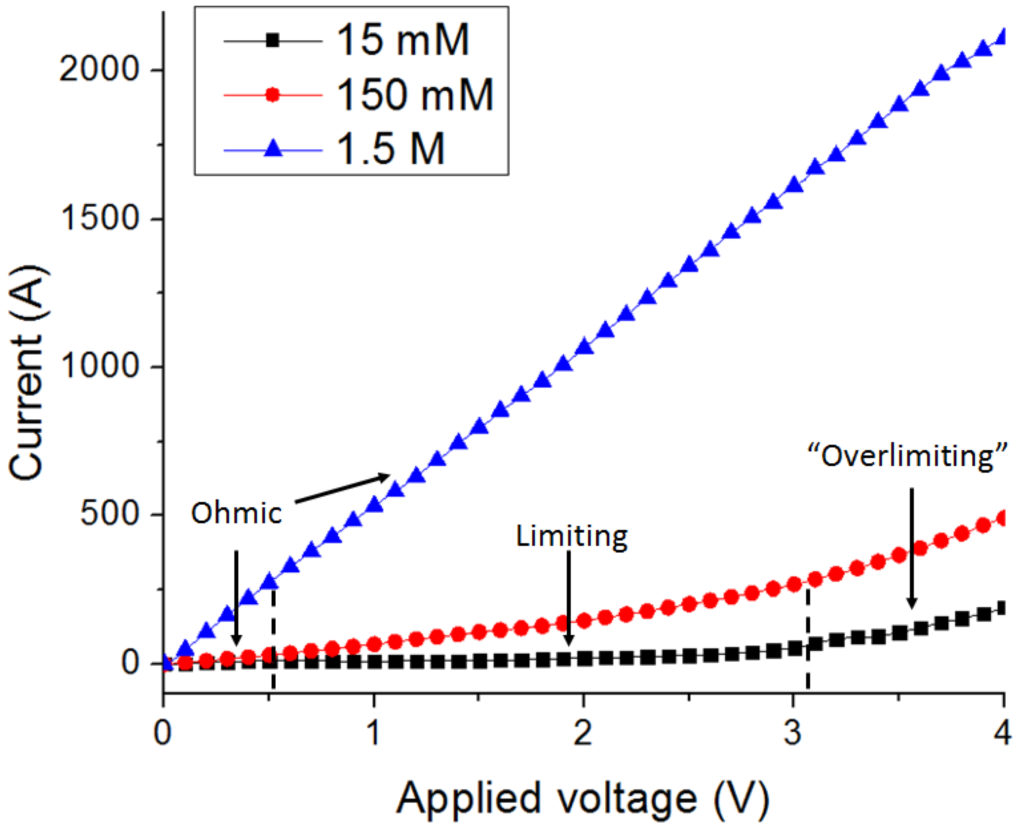


Figure 14. I-V plots using buffers with ionic strength of 15 mM, 150 mM and 1.5 M.

### 5.3. Operation of the LPSi DC preconcentrator

After loading the LPSi DC chip into the chip holder, the sample reservoir is filled with fluorescein solution and the other reservoirs are filled with PBS buffer solution (Figure 15). Then the platinum electrodes are connected to the two source meters Keithley 2450 and 2430 for the supply of high and low voltages ($V_H$ and $V_L$). The other two reservoirs are grounded (GND). The voltage difference across the LPSi membrane creates an electric field ($E_N$) that develops in the ion depletion zone. Since $V_H > V_L$, the voltage difference generates a tangential electric field ($E_T$) that forms an EOF through the microchannel and transports the sample molecules into the ion depletion zone where they get trapped by the counter-flow focusing mechanism.

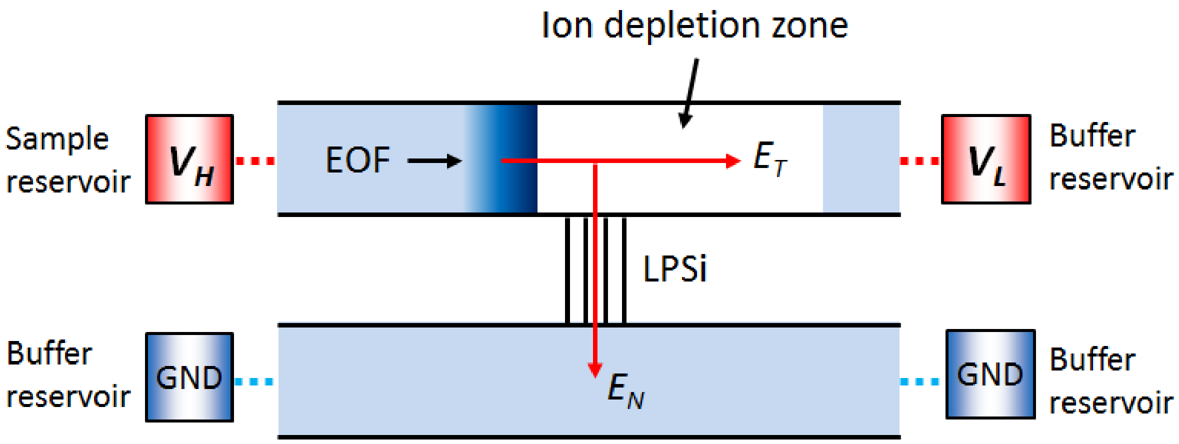


Figure 15. Schematic illustration of the DC ICP preconcentrator.

### 5.4. ICP preconcentration using fluorescein and miRNA

#### 5.4.1. Fluorescein preconcentration using constant applied voltages

First ICP preconcentration experiments with the LPSi DC device were done with 100 nM and 1 µM fluorescein in PBS 0.1×. The voltages were applied as is shown in Figure 16 with $V_H$ = 7 V and $V_L$ = 2 V. Fluorescence images were recorded every 10 s, and the shutter was only opened during the exposure (0.5 s) to minimize the photobleaching of fluorescence molecules. The resulting sequential images are shown in Figure 16 and 17. In the case of 100 nM fluorescein solution, the fluorescence intensity increases from 0 s to 150 s and the concentrated plug is stably located near the membrane. For 1 µM fluorescein solution, the concentrated plug is stacked and extends continuously until 90 s. Then, from 90 s to 150 s, the fluorescence intensity stabilizes and so the local molecular concentration, probably because of fluorescein overstacking due to electrical repulsion and molecule diffusion [28, 48].

Preconcentration factors were then estimated from image analysis using ImageJ where fluorescence intensity was measured in regions of interest (ROI of 10 µm×10 µm) picked up in the high-concentration plug (see Figure 17). Standard intensity of fluorescein at 10 µM and 50 µM were obtained by loading solutions in the microchannels and taking images under the same conditions. The fluorescence intensity as a function of time is shown in Figure 18: preconcentration factors of more than 100 and 50 were achieved within 90 s for 100 nM and 1 µM fluorescein, respectively.

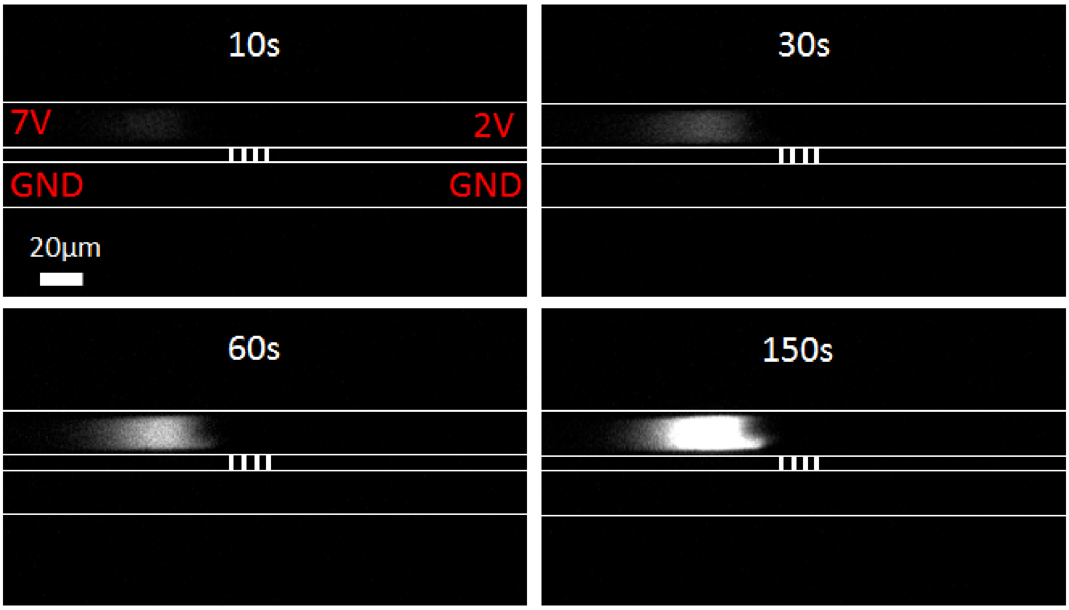


Figure 16. ICP preconcentration of 100 nM fluorescein.

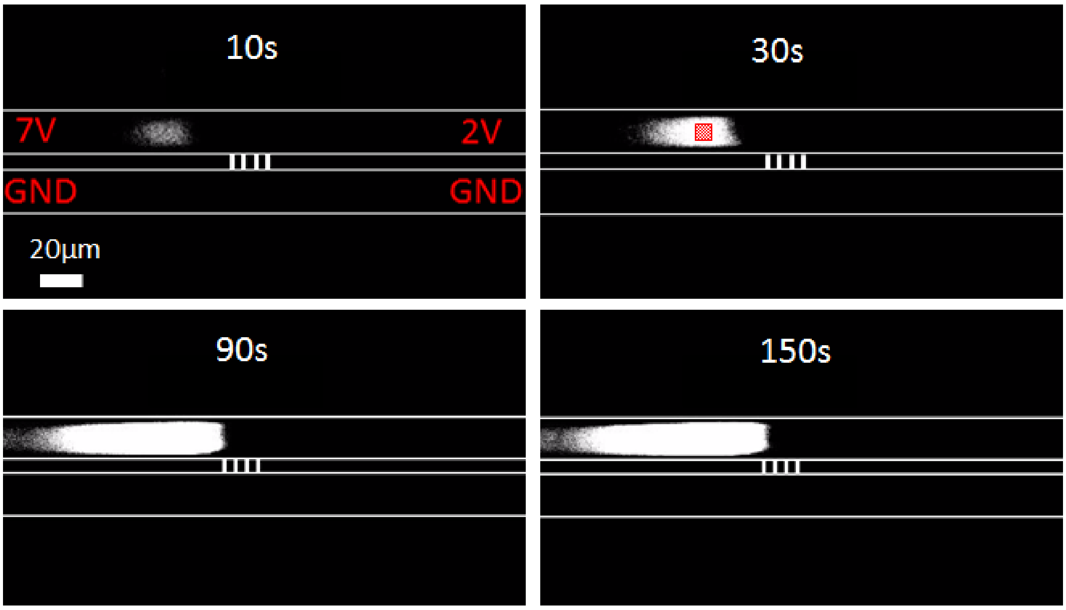


Figure 17. ICP preconcentration of 1 µM fluorescein (the red mesh is the region of interest used for measuring the fluorescence intensity).

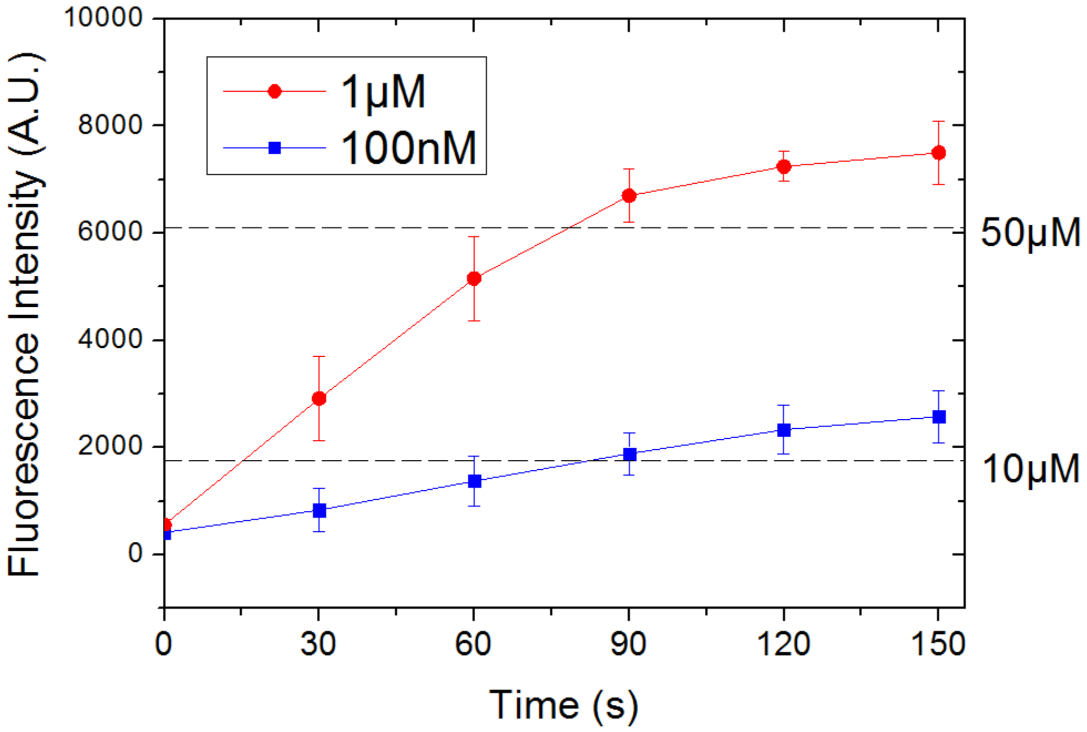


Figure 18. ICP preconcentration of fluorescein 100 nM and 1 μM as a function of time.

### 5.4.2. MiRNA preconcentration with varying voltages

In a second set of experiments, we have varied the two voltages ($V_H$ and $V_L$) during the concentration process in order to reach higher factors [14]. To this aim, solutions of miRNA with various concentrations (1 nM, 10 nM, and 100 nM in PBS 0.1×) were used. Typical operation voltages and switch times were ($V_H$/$V_L$/t): 2 V/0.5 V/0-2 min, 4 V/1 V/2-6 min, 7 V/2 V/6-10 min and 9 V/3 V/10-12 min. Beyond 9 V, the concentrated plug was very unstable. Normally, $V_L \geq V_H/2$ is recommended for a stable preconcentration process [14], but in our case, $V_L < V_H/2$ was sufficient, meaning that the voltage ($V_L$) needed to maintain the ion depletion zone was smaller (probably because of the higher counterion transport efficiency within the LPSi membrane). Figure 19 shows the resulting preconcentration factors achieved: 5000 in 10 min, 1000 in 10 min, and 500 in 7 min for the 1 nM, 10 nM, and 100 nM miRNA solutions.

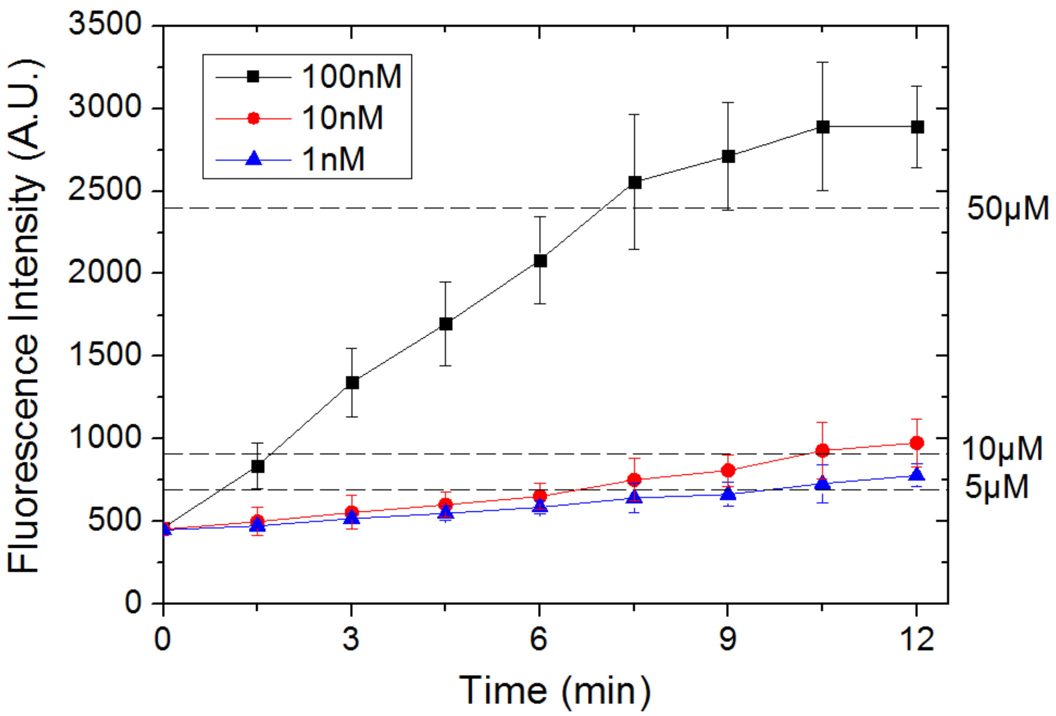


Figure 19. ICP preconcentration of fluorescein 100 nM, 10 nM and 1 nM as a function of time.

The influence of the buffer ionic strength on the preconcentration efficiency was also studied by carrying out experiments with 100 nM fluorescein and 1 nM miRNA in PBS 1× and PBS 10× (150 mM, 1.5 M). At 150 mM, a preconcentration factor of ~20 is achieved using fluorescein 100 nM at $V_H/V_L$ = 7 V/4 V. By varying the voltages, the preconcentration factor can reach up to ~500 using miRNA 1 nM. Since the permselectivity and ion depletion are weakened at higher ionic strength, it makes sense that maximum concentration factors are lower. In fact, at 1.5 M, the preconcentration is not even obvious to detect.

### 5.5. Comparison with other works

Table 2 presents results obtained with other ICP-based DC preconcentrators. In general, we have not been able to reach as high concentration factors in the constant voltage configuration because we did use lower applied voltages. However, when varying the applied voltages, were able to achieve results comparable to [51] or even better than [46, 52]. Still, one important feature of our approach is the use of much lower voltages that translates into lower power consumption favorable for portable applications.

Table 2. Comparison with similar works

| Ref. | Nanojunction | Analytes /Buffer (initial concentrations) | Factor/Time | Voltages ($V_H$,$V_L$) |
|---|---|---|---|---|
| 46 | Nafion film | DNA (25 nM)/ Tris_HCl (5 mM) | 1150 (4 min) | $V_H$-$V_L$=80 V |
| 47 | Nafion strip | AF-BSA (60 pM)/PBS (10 mM) | $2\times10^4$ (7 min) | 15 V, 5 V |
| 48 | Oxide nanochannel | GFP (33 fM)/ Phosphate (10 mM) | $10^7$ (60 min) | 10 V, 5 V |
| 51 | Porous titania membrane (sol-gel) | 2,7-dichlorofluorescein (31 nM)/Sodium phosphate (80 mM) | $4\times10^3$ (7 min) | 300 V, 150 V |
| 52 | Nafion | FITC-BSA (5 nM)/ PBS (5 mM) | $10^3$ (11 min) | 50 V, 25 V |
| This work | LPSi membrane | Fluoresein (100 nM)/PBS (15 mM) | 100 (90 s) | 7 V, 2 V |
| This work | LPSi membrane | miRNA (1 nM)/ PBS(15 mM) | $5\times10^3$ (10 min) | From 2 V, 0.5 V to 9 V, 3 V |

## 6. Experiments with LPSi Single-Channel devices (SCN)

### 6.1. Operation of the LPSi SCN preconcentrator

In Single-Channel preconcentrators with fully integrated Nanojunction (SCN), preconcentration takes place on the cathodic side of the membrane with an electrophoresis-dominated mechanism [21, 22, 30, 31]. High voltage is usually required to generate high enough electrophoretic flow, while the volumetric electroosmotic flow and hydrodynamic flow are limited by the membrane characteristics [14, 21]. Since our LPSi membranes enable relatively large hydrodynamic flows, the pressure-assisted ICP preconcentration configuration was used to achieve highest concentration factors.

The pressure-driven flow assisted preconcentration mechanism is presented in Figure 20. In our case, upon application of a voltage (≤ 4 V) across the LPSi membrane, the ion depletion forms at the anodic side of the membrane. The anionic species from the sample reservoir are driven by electrophoresis from the cathode to the anode, while the electroosmosis flow operates in the opposite direction. When applying an extra hydrodynamic flow from the anode to the cathode, the anionic species are transported from the anode to the front of the membrane and are then retained by the ion depletion effect near the membrane.

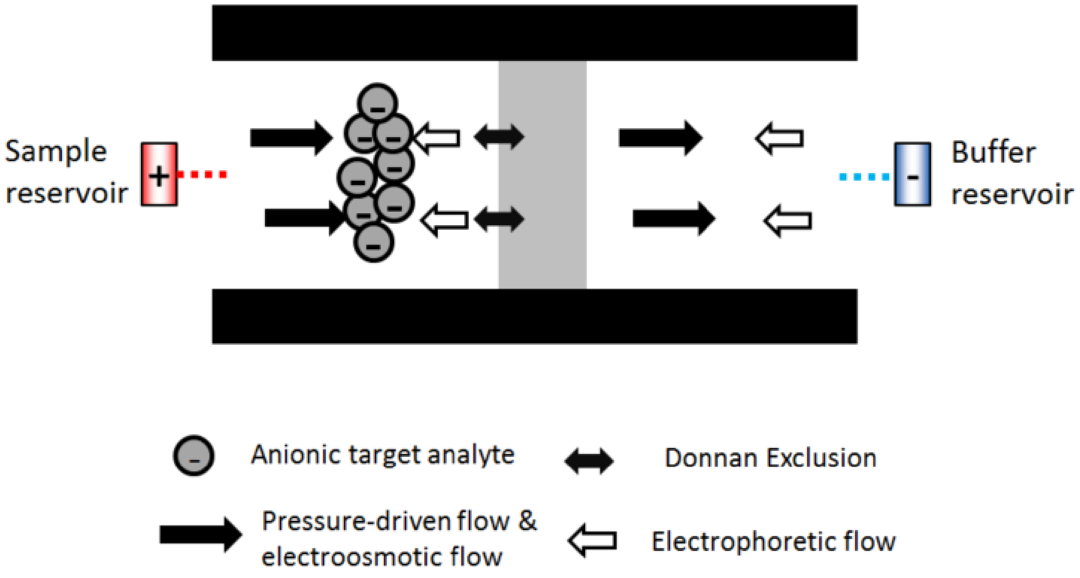


Figure 20. Schematic illustration of the hydrodynamic ICP preconcentration.

### 6.2. Hydrodynamic ICP preconcentration in SCN

Preconcentration experiments in SCN devices were carried out with 10 nM and 100 nM fluorescein solutions in PBS 0.1×. In these experiments, the anode microchannel was filled with the fluorescein solution, while the cathode microchannel was filled with PBS 0.1×. Voltages and pressures were generated by a Keithley 2450 and a pressure generator MFCS-8C (Fluigent). The experiment started by applying 4 V and 1 bar at the anodic side of the membrane. Fluorescence images were recorded every 30 s, and the shutter was only opened during the exposure time (0.5 s). Sequential images for the preconcentration of 10 nM and 100 nM fluorescein solutions are shown in Figure 21 and 22. To study the corresponding preconcentration factors, fluorescence intensity was analyzed with ImageJ onto 20 μm×20 μm ROI selected near the membrane. The fluorescence intensity as a function of time is shown in Figure 23: it takes 6 and 8 minutes for the concentration factors of 10 nM and 100 nM solutions to reach 100.

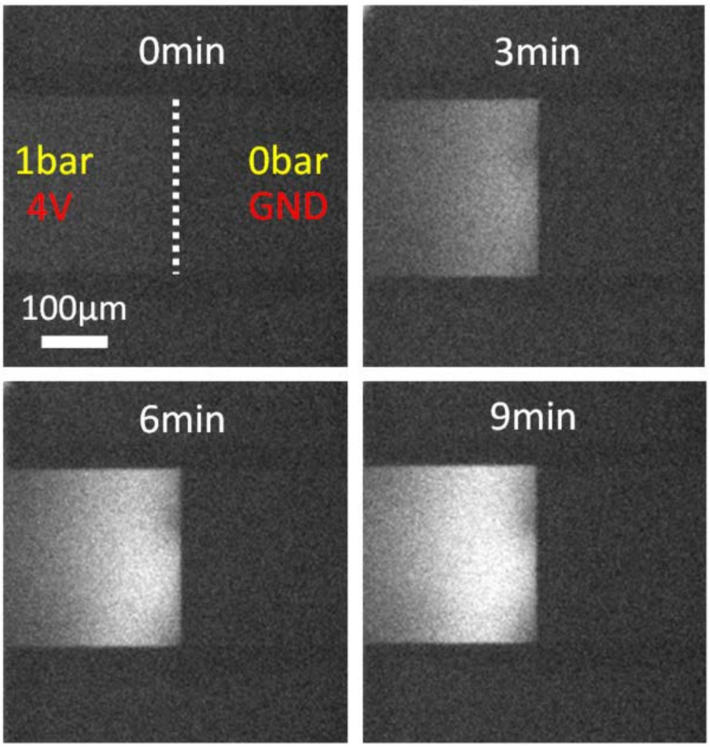


Figure 21. Preconcentration of 10 nM fluorescein solution as a function of time.

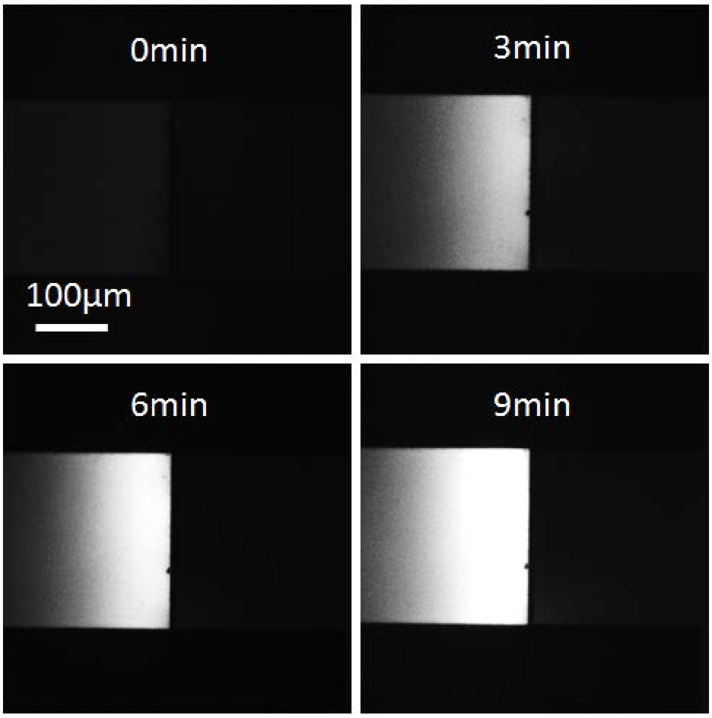


Figure 22. Preconcentration of 100 nM fluorescein solution as a function of time.

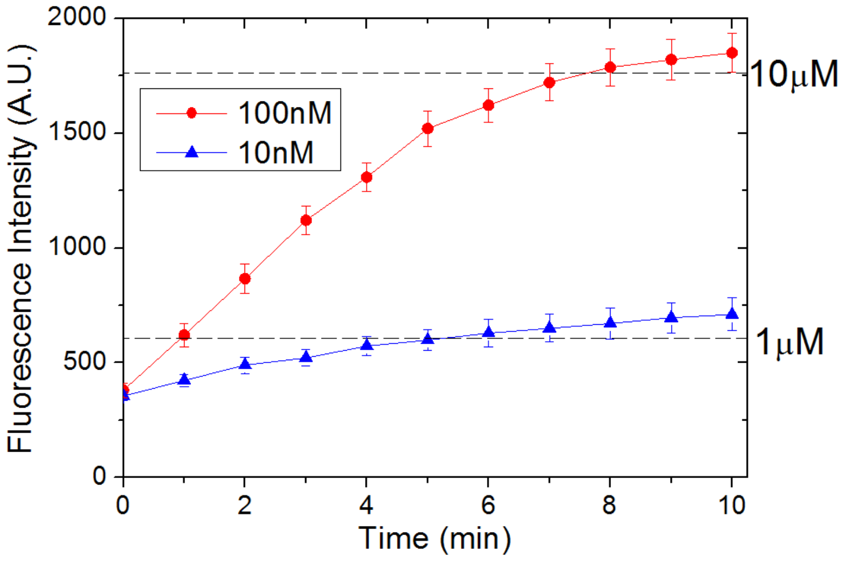


Figure 23. Hydrodynamic ICP preconcentration of fluorescein solutions as a function of time.

We have tried to estimate the total number of accumulated molecules during the preconcentration process rather than focusing on the concentration factor. To this aim, we have analyzed a much larger ROI (250 µm×250 µm, *i.e.* the size of the channel width). The result for the 10 nM fluorescein solution is presented in Figure 24: it turns out that we can reach an apparent local concentration of ~1 µM in the whole channel. This means that, although the concentration factor is only 100, the total concentrated volume is considerable.

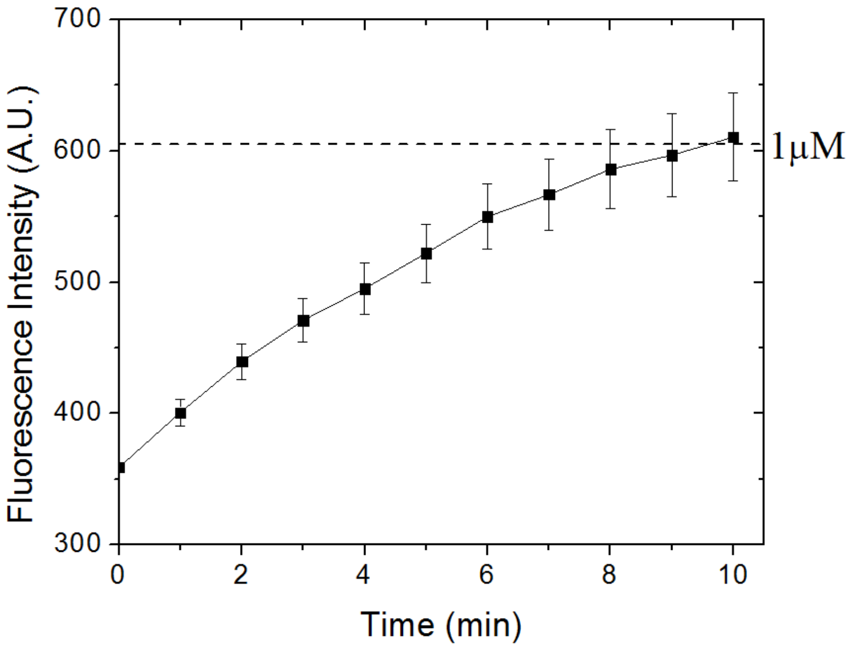


Figure 24. Hydrodynamic ICP preconcentration of fluorescein 10 nM as a function of time using the whole left-side microchannel as ROI.

Next, we tested the operation conditions of our concentration device in terms of applied voltages and pressures. When the voltage was reduced from 4 V to 2 V, while keeping a 1 bar pressure, the fluorescein molecules could not be prevented from passing through the membrane and the ion depletion region did not withstand the hydrodynamic flow. However, increasing the voltage from 4 V to 6 V, we noticed an increase of the ion depletion region on the anodic side of the membrane and a destacking effect that disturbed the stability of the ICP. Thus, for the 1 bar maximum pressure that can withstand the membrane, 4 V is the optimized applied voltage to achieve a maximum preconcentration factor. Lastly, as observed in the DC device, increasing the ionic strength of the buffer to 150 mM and 1.5 M led to a decreased efficiency of fluorescein stacking due to reduced ion depletion zone and Donnan exclusion effects.

### 6.3. Comparison with other works

There is only a very few work that has achieved the hydrodynamic ICP preconcentration on the anodic side of the nanojunction in the SCN configuration, which results are summarized in Table 4. The main reason is that it is difficult to generate large HDF or EOF through the nanojunctions. Compared to similar work [23], we have achieved comparable concentration factors using much smaller electric fields. This should, again, be due to the higher counterion transport efficiency and perm-selectivity of the LPSi membrane.

Table 4. Comparison with other works using SCN configuration

| Ref. | Nanojunction | Analytes /Buffer (initial concentrations) | Factor /Time | Electric field /Pressure |
|---|---|---|---|---|
| 23 | Glass Nanochannel | BSA (1.5 µM)/<br>Borate(50 mM) | 100 (4 min) | 70 V cm$^{-1}$ / 0.9 bar |
| 25 | Nanochannel formed between PDMS/glass | BSA (1 pM)/<br>PBS (10 mM) | $10^6$ (25 min) | ~125 V cm$^{-1}$ |
| This work | LPSi membrane | Fluorescein (10 nM)/<br>PBS (15 mM) | 100 (6 min) | ~4 V cm$^{-1}$/1 bar |

## 7. Conclusion and perspectives

In this chapter, we have presented experimental validations of the use of lateral porous silicon membranes as nanojunctions for the on-chip ion concentration polarization-based sample concentration. We have presented the mechanism of ICP and discussed the various configurations used to implement ICP preconcentration. After presenting a review of the performances of ICP preconcentrators found in the literature, we have introduced technological facts concerning the means to fabricate nanojunctions based on either nanochannels or porous membranes and incorporate them into microfluidic chips: in fact, ion selective membranes are all integrated into fluidic devices by introducing extra porous materials (Nafion), which differs from our platform where LPSi membranes is integrated monolithically during the fabrication process.

Here, we have tested our integrated approach for ICP concentration. To this aim, we have first demonstrated the ion selectivity of the LPSi membrane by experimentally studying the ion depletion phenomenon and carrying out dedicated electrical characterizations. We found that the permselecitivity of the LPSi membranes is comparable to that of Nafion membranes, and that the counterion transport efficiency of the LPSi membrane is, as expected, much higher than the silicon nanochannel, making our lateral porous silicon membranes a material of choice for on-chip ICP.

To demonstrate the ICP preconcentration capability of our device, we have studied two configurations of LPSi preconcentrators: double-channel devices have demonstrated preconcentration factors at least 100 by applying constant voltages and more than 5000 by varying the applied voltages, while single-channel devices with assisted hydrodynamic concentration have achieved a concentration factor of 100. The experiments presented here show that electrical leakage is the major obstacle to higher concentration factors that should be reached by applying high voltages: solutions to this issue would consist in improving the electrical insulation of the device by creating an oxide layer into the channels and within the pores by *e.g.* thermal oxidation or atomic layer deposition.

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# Chapter 4.

# Lateral porous silicon-based interferometric transducer

*In this chapter, we study the transducing ability of lateral porous silicon membranes (LPSi) using optical interferometry. To this aim, we use a FTIR setup coupled to a microscope stage equipped with an appropriate objective in order to overcome the difficulty to obtain interference signal from the LPSi membrane with small dimensions. Then, we describe the microfluidic setup and the protocol developed to carry out reproducible interferometric measurements. We record different reflectance spectra by filling the membrane with various solvents and we analyze them to estimate effective optical thicknesses and the resulting index of refraction of the filler in the NIR range. To demonstrate the validity of the acquired data and the possibility to use LPSi as interferometric transducers, we compare the experimental spectra to those obtained from simulation. Finally, we discuss the stability of porous silicon transducer in aqueous solution and study the interferometric detection at longer wavelengths.*

## 1. Introduction

Microfluidics and the miniaturization of sensors and actuators have enabled the emergence of lab-on-a-chip (LOC) devices that integrate medical laboratory functions on chip for biomedical applications, leading to faster/cheaper/portable analysis using smaller amount of sample and reagents [1]. These advantages arouse great interests in developing LOC devices for point-of-care testing and medical diagnostic [2]. In addition to point-of-care applications, the development of portable environmental analysis devices is gaining importance because the potential harmful byproducts from industrial, biochemical, and medical fields are threatening human health [3].

Sample analysis usually involves the detection and the dosage of a specific biochemical compound. This is achieved by transducing a biological recognition event into a measurable and quantifiable signal. Common signal transducers include electrical, electrochemical, optical, piezoelectric, and thermal sensors. The optical sensing scheme enables to probe surfaces and films in a nondestructive manner; it offers advantages in speed, sensitivity, and robustness, as well as permitting in situ sensing and real-time measurements [4]. Out of the various materials available to constitute optical-based biosensors, porous silicon has high surface area, convenient surface chemistry, and has been especially widely studied in interferometric sensing configuration [5]. Here, we investigate the possibility to use our developed lateral porous silicon membrane for interferometric biosensing.

## 2. Porous silicon interferometric transducers

### 2.1. Mechanism of interferometric measurement

A porous silicon (PSi) Fabry-Pérot interferometer consists of a thin PSi layer formed onto a silicon substrate that offers two parallel reflecting surfaces, at the air/PSi and PSi/silicon interfaces. When a beam of light strikes the porous silicon surface, light is successively reflected at the air/PSi and the PSi/silicon interfaces, as shown in Figure 1. The difference of optical path length (OPD) between two reflected beams is:

$$OPD = n\left(\overline{AB} + \overline{BC}\right) - n_1\overline{AD} \tag{1}$$

Where,

$$\overline{AB} = \overline{BC} = \frac{L}{\cos\theta} \tag{2}$$

$$\overline{AD} = 2L\tan\theta\sin\theta_1 \tag{3}$$

By applying Snell's Law:

$$n\sin\theta = n_1\sin\theta_1 \tag{4}$$

We obtain [6]:

$$OPD = 2nL\cos\theta \tag{5}$$

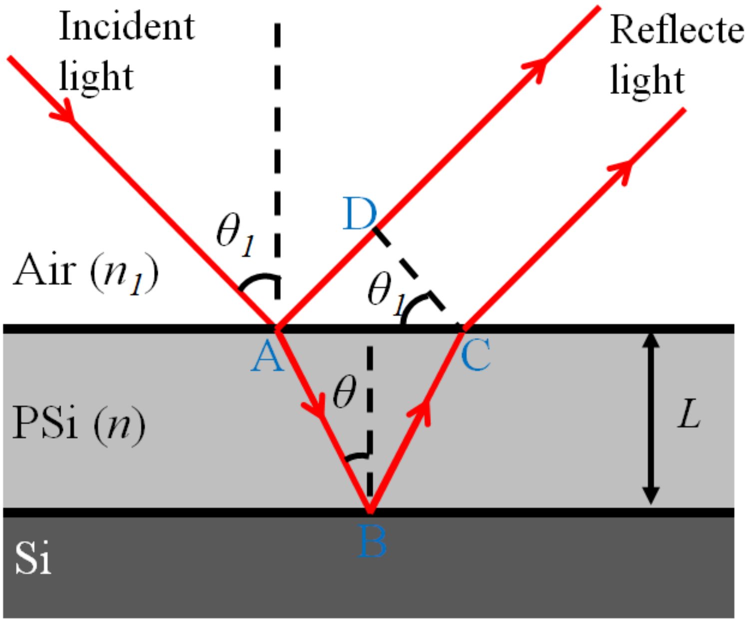


Figure 1. Description of the optical path length difference for light reflected from the upper and lower boundaries of a PSi layer. In the figure, $L$ is the thickness of the PSi layer, $n$ and $n_1$ are the refractive indices of PSi and air, respectively, $\theta$ *and* $\theta_1$ are the incident angles of the light at the PSi/Si and air/PSi interfaces, respectively.

The overlapping of the two reflected light waves having the same wavelength causes phase interactions, as shown in Figure 2. Considering two incident light waves A and B that produce their reflected waves (dashed) at the air/PSi and PSi/silicon interfaces: if the reflected waves are in phase (Figure 2a), they interfere constructively and the resultant wave C is strengthen;

on the contrary, if the reflected waves have opposite phase, they interfere destructively and the resultant wave C' is attenuated (Figure 2b). From here we can conclude that the maximum wave construction (*i.e.* Fabry-Pérot fringes maxima in an interference spectrum) happens when the additional total distance covered by the beam A is an integer multiple of the wavelength. Therefore, there is the relationship between the optical path length and the Fabry-Pérot fringes [6, 7]:

$$2nL\cos\theta = m\lambda_{max} \tag{6}$$

Where $m$ is an integer corresponding to the spectral order of the fringe and $\lambda_{max}$ is the wavelength of the fringe maxima.

The optical path length, $2nL\cos\theta$, is also referred to as the effective optical thickness (EOT). For a given PSi interferometer, the thickness $L$ and incident angle $\theta$ can be considered constant. Therefore, the EOT is solely a function of the refractive index, $n$. Since the refractive index of porous silicon depends on the type of medium filling the pores (*e.g.* gases and solutions) or binding/adsorption events happening to the pore walls (*e.g.* biomolecules and chemicals), PSi Fabry-Pérot interferometer can be used for the detection of vapors [8] and biomolecules [9].

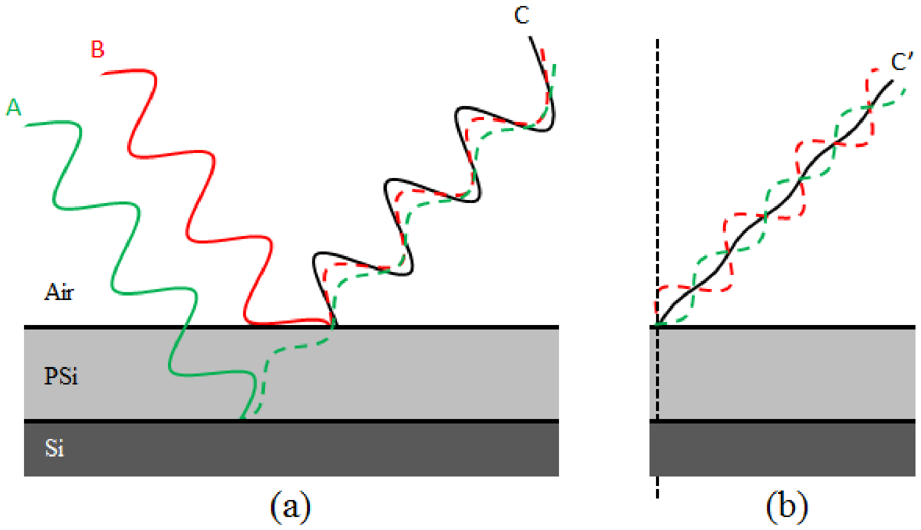
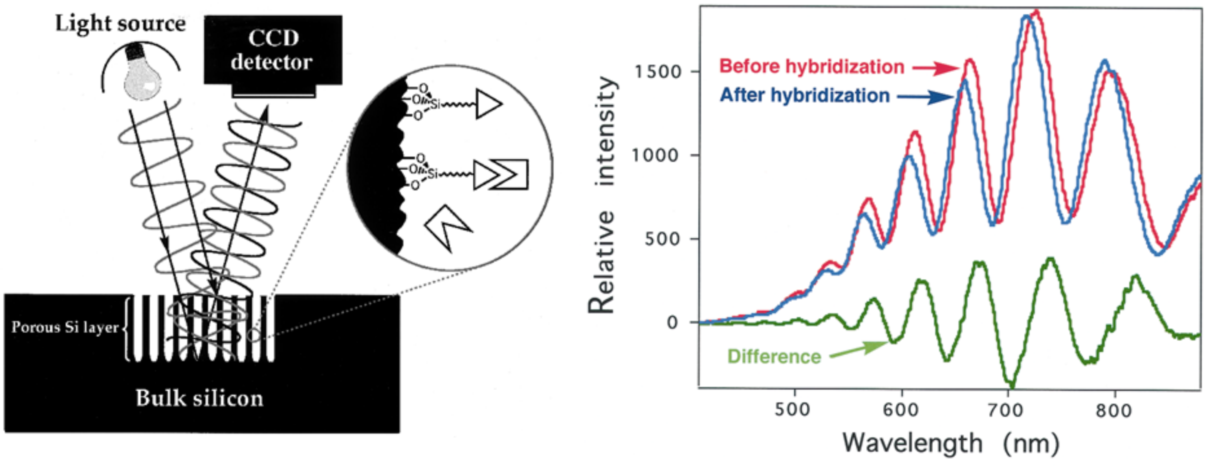


Figure 2. Phase interaction between two reflected waves (dashed) resulting from the incident light waves A and B. (a) The reflected waves are in phase and interfere constructively. (b) The reflected waves have opposite phases and interfere destructively.

## 2.2. Classical PSi interferometric configuration

PSi-based interferometric sensors and biosensors consist of vertical porous silicon layers created into a silicon wafer where the pores are oriented perpendicular to the surface plane [8-10]. Figure 3a shows a typical example of a PSi interferometric biosensor [11]. Vertical porous silicon is created by silicon anodization with the supply of hole current from the backside of the silicon wafer. The surface of the porous silicon is properly modified with molecular recognition elements (such as oligonucleotides, biotins, or antibodies). Reflection of white light at the top and bottom of the PSi layer results in an interference pattern (Fabry-Perot fringes), as shown in Figure 3b. The interference spectrum depends on the refractive index of the PSi matrix. Interactions of molecular species with their recognition partners immobilized onto the PSi surface induce a change in the refractive index of the nanocrystalline semiconductor, giving rise to wavelength shifts in the fringe pattern that can be easily detected and quantified. It is possible to carry out the optical measurement through a fluidic cell, as demonstrated by works where vertical porous silicon was integrated into microfluidics for real-time detection [12].

Similar to PSi single-layer interferometer, interference can be detected on PSi multilayer structures (*e.g.* double layer, Bragg stack, microcavity and rugate) and those structures had been vastly studied for biosensing (*e.g.* DNA, protein, enzyme activity and bacteria), as is described in Chapter 1 of this manuscript. Among these configurations, the PSi single-layer (Fabry-Pérot interferometer) is the simplest and the most straight-forward approach.



(a)

(b)

Figure 3. (a) Schematic of the PSi-based optical interferometric biosensor. (b) Interference spectra before and after hybridization of DNA [11].

### 2.3. Flow-over vs flow-through configuration

In this work, we have successfully fabricated and integrated lateral PSi membranes into lab-on-a-chip devices. After demonstrating that these structures are adapted to size-based filtration and ion concentration polarization, it would be interesting to explore their potential use for interferometric sensing. In fact, the use of vertical and lateral porous membranes in microfluidics results in two sensing configurations: the flow-over (FO) and flow-through (FT) configurations shown in Figure 4. Theoretical work [13] has shown that, with similar sensor footprints, FT sensor offers up to 20-fold improvement in response time. The comparison between FO and FT sensing has been investigated using PSi microcavities and free-standing PSi microcavity membranes [14]. The research reveals some issues encountered with FO sensors where analytes or contaminants can be trapped within the closed-ended pores, leading to an overestimation of the sensor sensitivity. The aim of the work presented in this chapter is thus to study the suitability of our fabricated lateral porous silicon to interferometric measurements, since this might lead to the future development of on-chip flow-through biosensors.

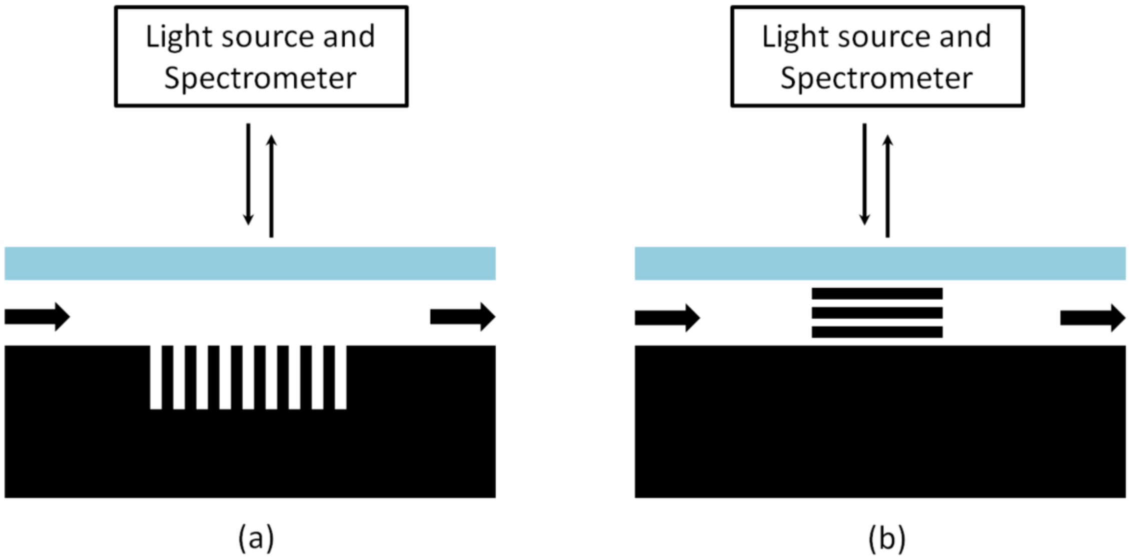


Figure 4. Two sensing configurations: (a) a typical flow-over configuration with a surface-based sensor within a microfluidic channel. (b) a flow-through configuration with an array of lateral nanopore tubes adequately connecting both microchannels.

## 3. Materials and methods

### 3.1. Experimental setup

Optical measurements were performed on a VERTEX 70 Fourier Transform Infra-Red spectrometer (FTIR) (Bruker Optics) (Figure 5) equipped, among others, with a tungsten light source, a Quartz beam splitter and a Si-diode detector (SiD 510), which covers a spectral range from 500 to 1100 nm. The spectrometer was connected to a HYPERION microscope holding various objectives (15×, and 36×) and apertures. The objective 36× was mainly used for measurements with the aim to collect a maximum signal from the micron scale membrane. The microscope enabled both visual observation (using a 4× objective and a camera), and spectral measurement of the PSi sample. A spectroscopy software, OPUS, was used to control the microscope and acquire data. This optical study was carried out with the help of Dr. Véronique Bardinal from LAAS.

Our porous silicon chip was loaded into a sample holder which was subsequently fixed on the microscope stage. The sample holder was connected to a 4-channel reservoir (FLUIWELL$^{TM}$, Fluigent) for fluid management. The reservoir allowed us to easily change test solution without having to move the sample holder, which was critical to ensure the reproducibility of the measurements. The reservoir was connected to a pressure source to control the fluid flow inside the chip: for operation simplicity, syringes were used to apply positive or negative pressure to fluid, which allowed us to load, evacuate, and elute test solutions conveniently. Besides, a pressure generator (MFCS-8C, Fluigent) was also used to generate constant pressure and offer air flow.

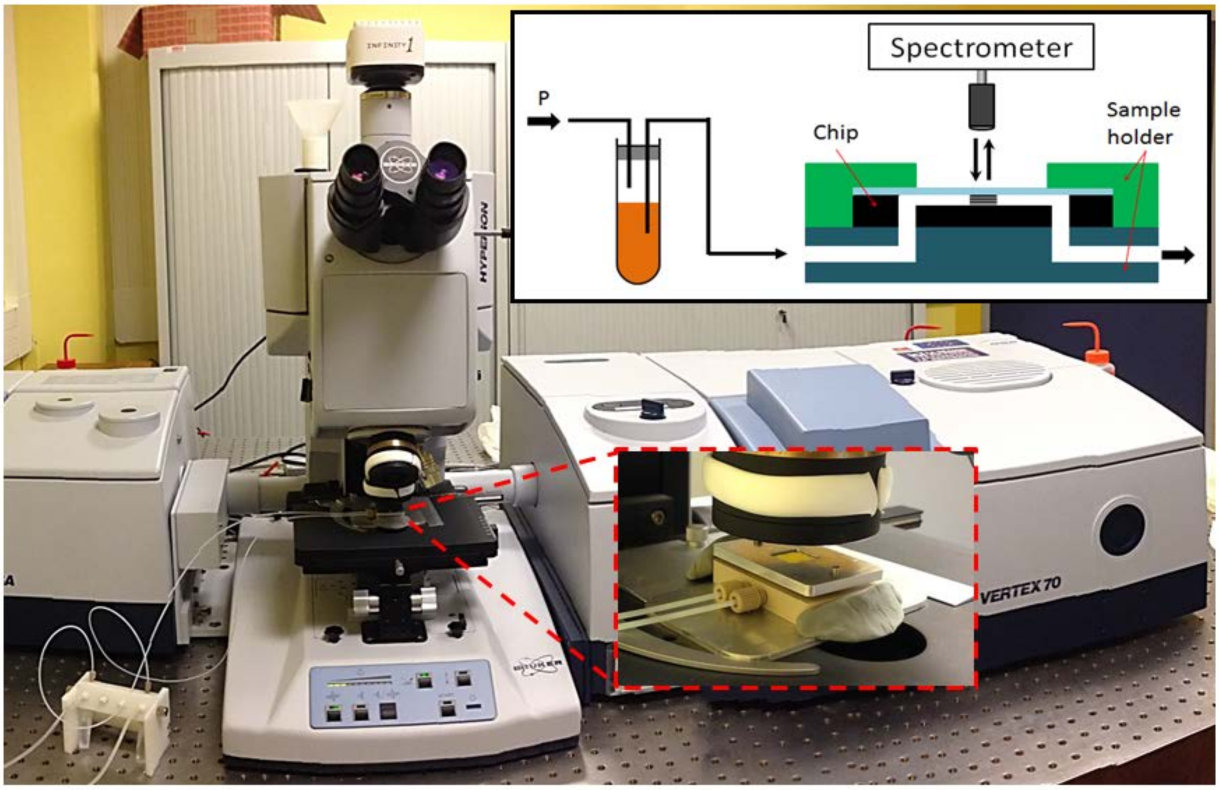


Figure 5. Experimental setup for microscale analysis and fluid-managing system used for optical detection.

### 3.2. Measurement procedure and test solutions

Test solutions were pumped into the microchannels and subsequently pushed through the LPSi membrane via positive pressure to ensure the full infiltration of the liquid into the membrane. Then, upon visual observation, the microscope was adjusted to focus on the top of the LPSi membrane and the observation window was downsized to a rectangle with dimensions of 20 × 120 µm$^2$ using adjustable x- and y-apertures. These dimensions were chosen according to the dimensions of the LPSi membrane (20 × 250 µm$^2$). After changing the microscope mode to spectral measurement, reflectance data acquisition was carried out with a wavenumber resolution of 4 cm$^{-1}$. Following data acquisition, the analyte solution was then flushed away to allow the measurement of another analyte.

In order to test the interferometric transduction capability of the LPSi membranes, three kinds of solutions were tested: various solvents (water, ethanol, acetone), salt solutions (NaCl 5%, 15%) and molecular solutions (fluorescein 50 µM and 100 µM). We used different flushing protocols for the various solutions: in the case of solvents, the liquid was pumped by continuous air flow; in the case of molecule and salt solutions, the liquid was replaced with DI water by flowing it into the microchannels and through the membrane.

It is important to note that, prior to each measurement, a reference spectrum was taken onto a gold mirror using the same experimental conditions (*i.e.* sample stage height and observation window size). Besides, before injecting test solutions, the chip was exposed to oxygen plasma in order to increase the wettability of the microchannels and the nanopores.

## 4. Results and discussion

### 4.1. Proof-of-concept of LPSi interferometry

There are some major differences between our optical measurement setup and the ones used in other porous silicon interferometer works: (1) from the literature, we notice that FTIR is rarely used in PSi-based interferometric sensing. So it is important to first demonstrate that this optical tool is adapted to PSi interferometric measurement. (2) In other works, reflectance spectra are normally recorded on porous silicon samples with large area (*e.g.* >1 $cm^2$ [15, 16]). Our fabricated lateral porous silicon membranes display significant smaller dimensions, with a typical footprint of 20 × 250 $\mu m^2$, which means that there is much less light reflected from the membrane to be received by the detector. (3) Similarly to PSi sensors integrated into microfluidics, our LPSi chip includes many layers with reflecting surfaces (*e.g.* the cover glass and microchannel) which could possibly form Fabry-Pérot interferometers with different fringe periods. It is important to make sure that the observed interferences are due to the LPSi membrane. Based on these considerations, we have carried out some experiments to address these issues and demonstrate the possibility to use LPSi membranes for interferometric sensing.

#### 4.1.1. Measurements with different configurations of PSi

In order to demonstrate the possibility to use our FTIR for interferometric measurements and to evaluate the quality of the signal obtained with LPSi samples, we have tested 3 porous silicon design configurations with 3 types of fabricated chips: vertical PSi, SOI type LPSi, and implantation type LPSi. Since the vertical PSi has been widely studied by other research groups, we can compare the reflectance spectrum from our FTIR with literature to verify the aptness of our optical setup. The optical measurement was carried out on bare vertical porous silicon (without any glass capping layer) and the observation window was not downsized to obtain the strongest signal. On the other hand, measurements on LPSi membranes were done after chip encapsulation, as described in Chapter 2, and followed the procedure given in Section 3.2.

The resulting reflectance spectra are shown in Figure 6. The vertical PSi displays very a smooth interference pattern due to the enhanced signal obtained from the large observation window and good uniformity of the PSi layer. The interference pattern ranges from 600 nm to 1000 nm, which is similar to the range (500-1000 nm) usually studied in the literature [16]. On contrary, the spectrum obtained from the implantation type LPSi is much rougher and the interference pattern cannot be detected in the range of 600 nm to 800 nm. Since the measurement was carried out with a small, downsized window, it is understandable that the reflectance signal is weaker. Moreover, researches on optical absorption of porous silicon [17, 18] have shown that the absorption coefficient in the visible range is larger than in the infrared range, which means that more light was absorbed by the PSi in the visible range. In addition, the tungsten light source has weaker emission intensity in the visible range. Although the interference signal from the implantation type LPSi is not as good as the one from the vertical PSi, it is important to note that the LPSi membrane can in fact display interference patterns. The SOI type LPSi was also tested but did not display significant interference patterns. Since the differences between the SOI type and the implanted type LPSi are the height of the membrane (20 µm vs 4 µm) and the presence of the additional silicon dioxide buried layer, it is possible that the light reflected from the bottom interface is too weak for proper interferences formation. Since only the implantation type LPSi membrane could display proper interference pattern, the rest of this study was solely conducted with the implantation type chips.

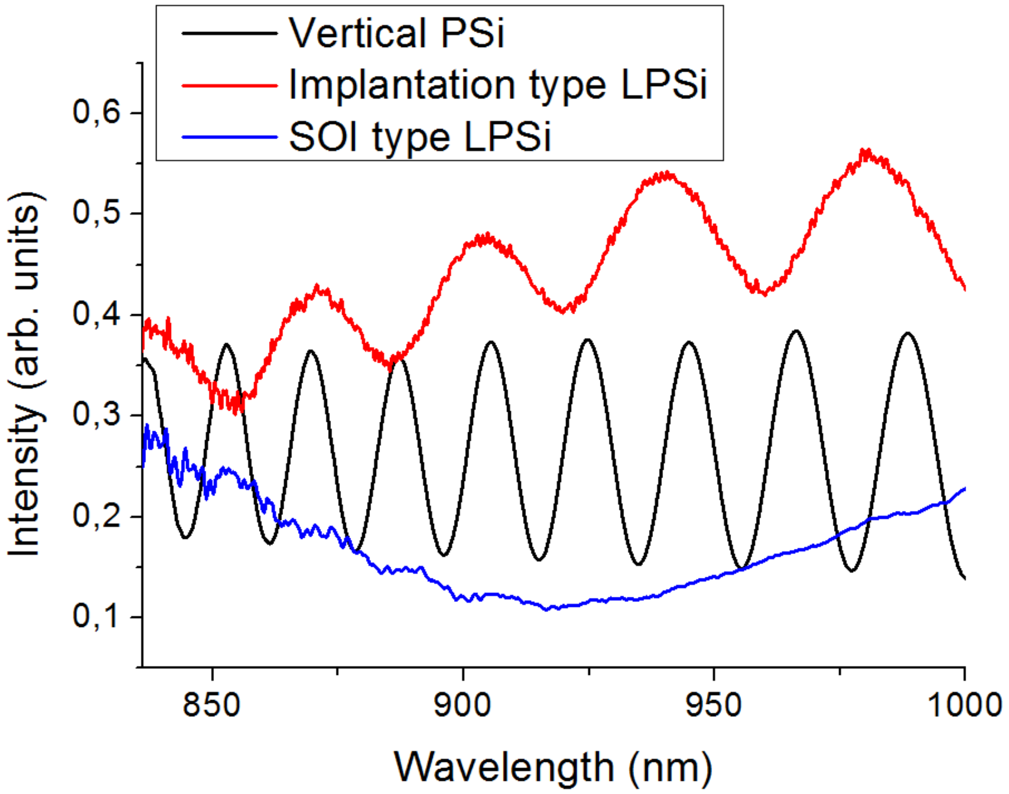


Figure 6. Reflectance spectra of different porous substrates: vertical PSi, implantation type lateral PSi, and SOI type lateral PSi.

### 4.1.2. Measurements at different locations on the chip

To ensure that the interference patterns were due to the porous silicon layer and was not generated by the microchannel layer, which is formed by the top glass layer and the bottom silicon substrate, we have compared the optical signal obtained from the microchannel and the LPSi membrane. To this aim, we conducted an experiment where one of the microchannels was filled with water that was gently pushed into the membrane, while the other microchannel was left empty. The optical measurement was first carried out onto the membrane (position 1 in Figure 7) following the measurement procedure. Then, the light beam was moved to the microchannel filled with water (position 2) and the measurement was done with the same experimental parameters. Finally, the same measurement was done on the other microchannel (position 3). The spectra (Figure 7) show that only the LPSi membrane leads to obvious interference patterns. We could speculate that the top and bottom interfaces of microchannel are not perfect enough to form an obvious Fabry-Pérot interferometer, which is probably not the case of the LPSi membrane interfaces.

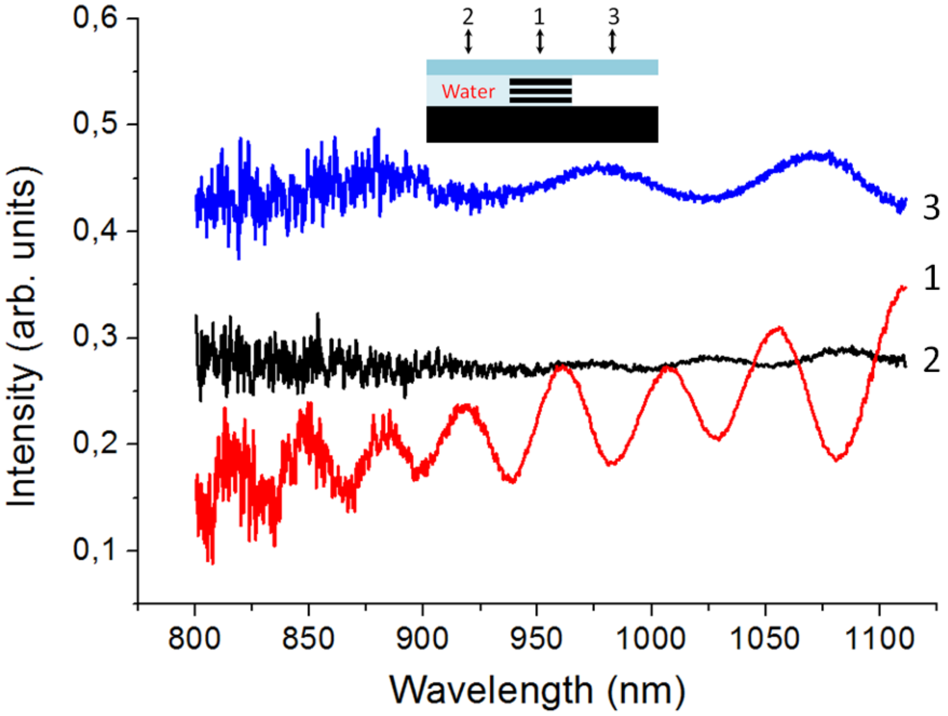


Figure 7. Reflectance spectra obtained at different observation locations on the implanted LPSi chip: (position 1) onto the LPSi membrane (infiltrated with water); (position 2) onto the left microchannel filled with water; (position 3) onto the right microchannel without water.

### 4.2. Experimental validation with various solvents

Since the refractive index of porous silicon membranes depends on the pore-filling medium, we have tested the ability of our setup to measure a change of refractive index, through the effective optical depth by loading the membranes with liquids of various optical properties. Evaporable solvents (water, ethanol and acetone) were chosen for this experiment since they can easily infiltrate the membrane and can easily be removed by evaporation. Before solvent injection in the chip, an optical measurement was carried out on the empty LPSi membrane. Then a first solvent was injected followed by an optical measurement at the same location. Afterwards, the liquid was cleaned out from the microchannel by flowing air into the chip and another solvent was used for testing. Figure 8 presents the resulting reflectance spectra. Compared to empty and dried porous silicon, the presence of all three liquids clearly led to a red shift of the spectrum. The wavelength shifts from bare PSi configuration are in the following order: water (n~1.328) < acetone ≈ ethanol (n~1.35). These results demonstrate that this optical measurement allows us to distinguish water from acetone/ethanol based on their differences in refractive index (in this case 0.02), which can be considered as a proof-of-concept of LPSi interferometric sensing.

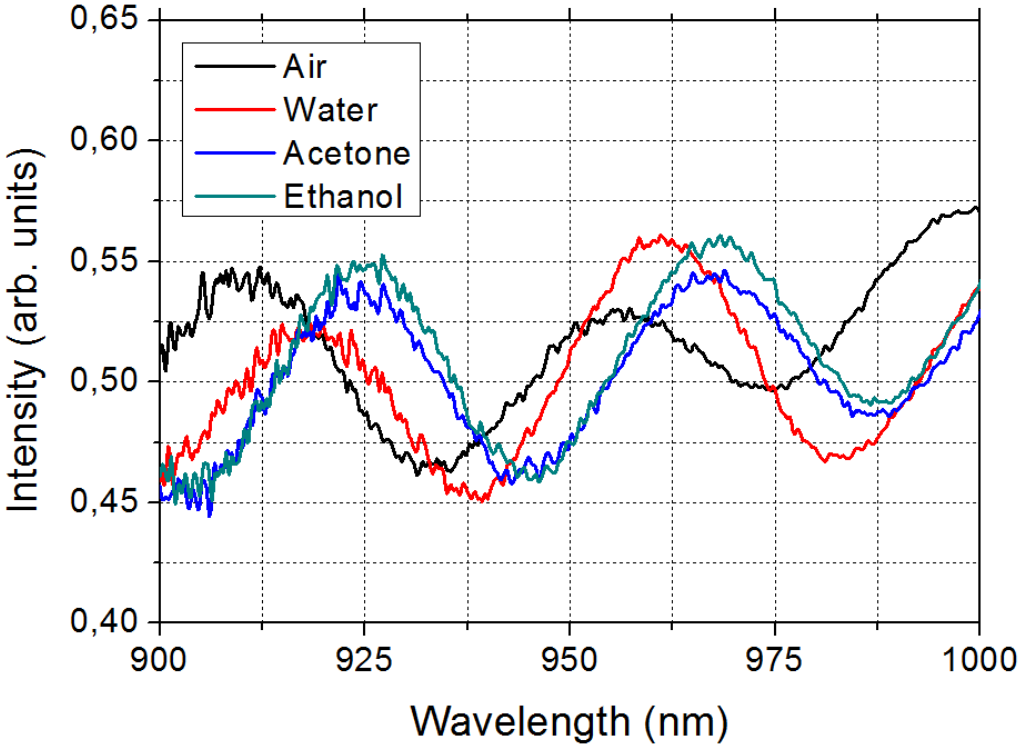


Figure 8. Reflectance spectra of a LPSi membrane filled with different solvents: water, acetone, and ethanol. The spectrum marked as air means that no liquid fills the pores.

### 4.2.1. Analysis of the experimental spectra

#### 4.2.1.1. Derivation of the refractive index by the fitting method

Since the shift in the interference pattern is related to the change of refractive index of the filling medium, it is important to use an analysis method for the estimation of that index of refraction. From equation 6, we know that the effective optical thickness can be derived from the spectral order of the fringe ($m$) and the wavelengths of the fringe maxima ($\lambda_{max}$). The effective optical thickness can thus be derived by analyzing the Fabry-Pérot fringes as following [16, 19]: first, we replot the spectrum in frequency unit and we determine the peaks (fringe maxima) of the interference pattern (using the peak analyzer from Origin 8 data analysis software). Then, each peak is numbered successively (*i.e.* 0, 1, 2, *etc.*) and we plot the peak number versus the frequency, as shown in Figure 9. The slope and the intercept of the linear fit equal the effective optical thickness ($2nL\cos\theta$, with the unit of cm) and the spectral order (*m*). The angle, *θ*, which depends on the numerical aperture of the objective, is around 8° for the 36× objective we used. If the membrane thickness (*L*) is known (it can be measured by SEM), we can derive an experimental value for its refractive index (*n*), which is displayed in Table 1.

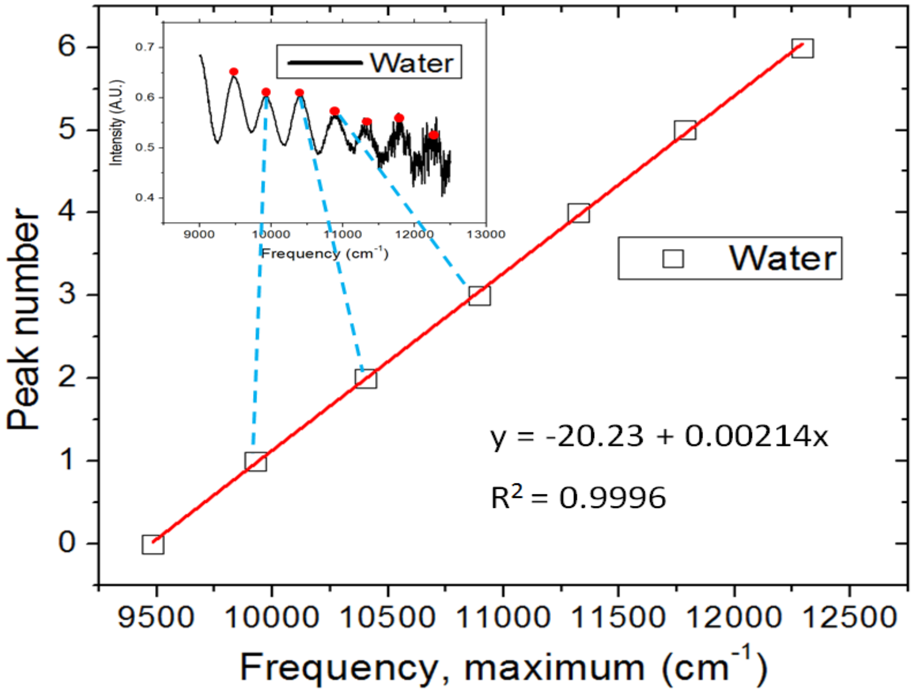


Figure 9. Fringe number as a function of corresponding frequency. The inset shows the spectrum replotted in frequency unit and the peaks of the interference pattern corresponding to successive peak number.

#### 4.2.1.2. Derivation of refractive index by the RIFTS method

The spectrum analysis can also be carried out by a procedure called Reflectometric Interference Fourier Transform Spectroscopy (RIFTS) [16]. This method computes the frequency spectrum of an input waveform by fast Fourier transform, yielding a peak whose position along the x-axis corresponds to the effective optical thickness. We used a program (Fringe_24_1.pxp, available at http://sailorgroup.ucsd.edu/software, written by M. J. Sailor for the IGOR PRO software package version 7.0, Wavemetrics, inc, www.wavemetrics.com) to process the interferometric spectra. The program processes the spectral files automatically and generates Fourier transformed spectra, as shown in Figure 10 in the case of our experiments. Although the peak positions of Fourier transformed spectra of water and ethanol are quite close, they are still distinguishable as marked in the figure. From these spectra, we have obtained the values of the effective optical thickness by carefully locating the peaks using Origin 8, and we have calculated the corresponding refractive index (Table 1).

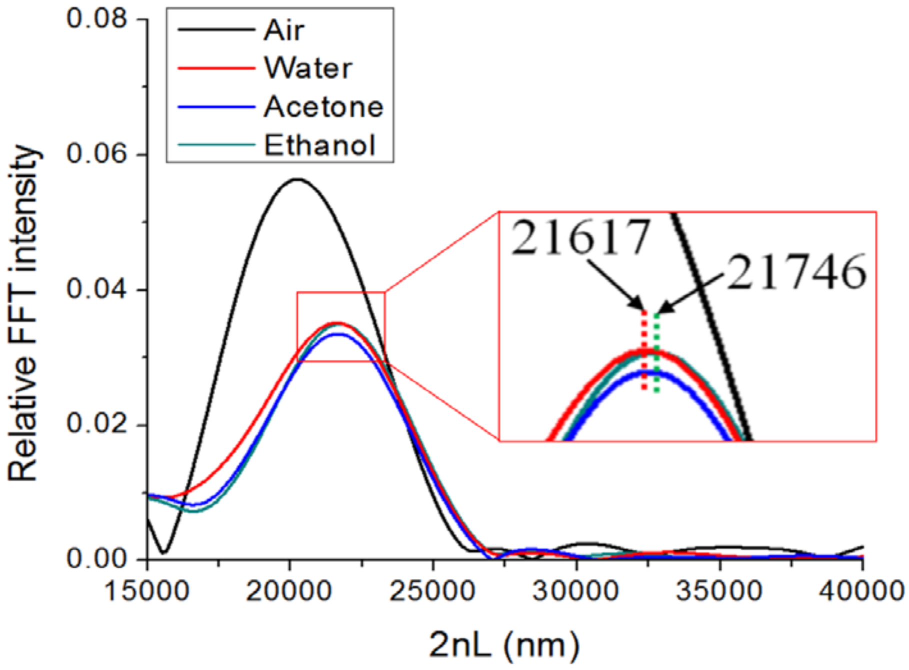


Figure 10. RIFTS of the reflectance spectra of the LPSi membrane filled with different solvents (provided in Figure 8).

#### 4.2.1.3. Derivation of the refractive index by the theoretical approximation

The theoretical refractive index of the porous silicon layer can be estimated by Bruggeman Effective Medium Model:

$$P\frac{n_{fill}^2 - n_{layer}^2}{n_{fill}^2 + n_{layer}^2} + (1-P)\frac{n_{skelenton}^2 - n_{layer}^2}{n_{skelenton}^2 + 2n_{layer}^2} = 0 \tag{7}$$

Where $P$ is the porosity of porous silicon (≈40% in the care of the fabricated implanted type LPSi membranes), $n_{fill}$ is the refractive index of medium filling the pores, $n_{skeleton}$ is the refractive index of the skeleton that makes up the porous material (*i.e.* the refractive index of silicon, 3.673 [21]) and $n_{layer}$ is the refractive index of the composite porous silicon.

Normally the index of refraction is wavelength-dependent. However, its dispersion is fairly small in the wavelength range considered in this study [16]. So the refractive index can be assumed constant and values are given at 830 nm and 20 °C [20]. The theoretical values of the refractive index of porous silicon as a function of the filling solvent are listed in Table 1.

#### 4.2.1.4. Comparison of the refractive index derived from the three methods

In Table 1, we have listed the refractive indices derived from the two experimental methods and from theory. From the table we can see that the values obtained from the two experimental methods are in accordance with the theoretical values. The composite refractive index ($n_{layer}$) is in order of air < water < acetone ≈ ethanol, which, indeed, corresponds to the shifts of interference patterns. This proves the accuracy of our experiments and the feasibility of the interferometric transduction.

Table 1. Index of refraction of the lateral porous silicon membrane filled with various solvent derived from two experimental methods and theory.

| Medium<br>Method | | Air | Water | Acetone | Ethanol |
|---|---|---|---|---|---|
| Experimental (fitting) | EOT (nm) | 20200±175 | 21400±174 | 21600±121 | 21600±108 |
| | Derived refractive index | 2.55±0.022 | 2.70±0.022 | 2.73±0.015 | 2.73±0.014 |
| Experimental (RIFTS) | EOT (nm) | 20255±158 | 21617±158 | 21706±158 | 21746±158 |
| | Derived refractive index | 2.56±0.020 | 2.73±0.020 | 2.74±0.020 | 2.74±0.020 |
| Theoretical approximation | $n_{fill}$ | 1 | 1,328 | 1,354 | 1,357 |
| | Derived refractive index | 2.56 | 2.69 | 2.70 | 2.70 |

### 4.2.2. Derivation of simulated spectra

In the previous section, we have derived refractive indices from experimental interference spectra. In this section, we reverse the process, *i.e.* we derive simulated interference spectra from refractive indices, in order to further confirm our results using a homemade simulation software ‘Reflex’ [22, 23]. In our simulation work, the incident medium was defined as Borofloat 33 glass (n = 1.467), the refractive index of the interferometry layer was defined as the experimental value obtained in the previous section (from the fitting method) with a thickness of 4 µm, the refractive index of the substrate was that of silicon, *i.e.* 3.673 and the angle ($\theta$ as shown in Figure 1) was set to 8°. Figure 11 shows two sets of calculated spectra compared with the experimental ones: the fringes of both spectra are at the same positions indicating that the calculated spectra match the experimental data very well. This is a strong evidence of accuracy of our analysis and proves furthermore that our LPSi membrane is indeed a Fabry-Pérot interferometer.

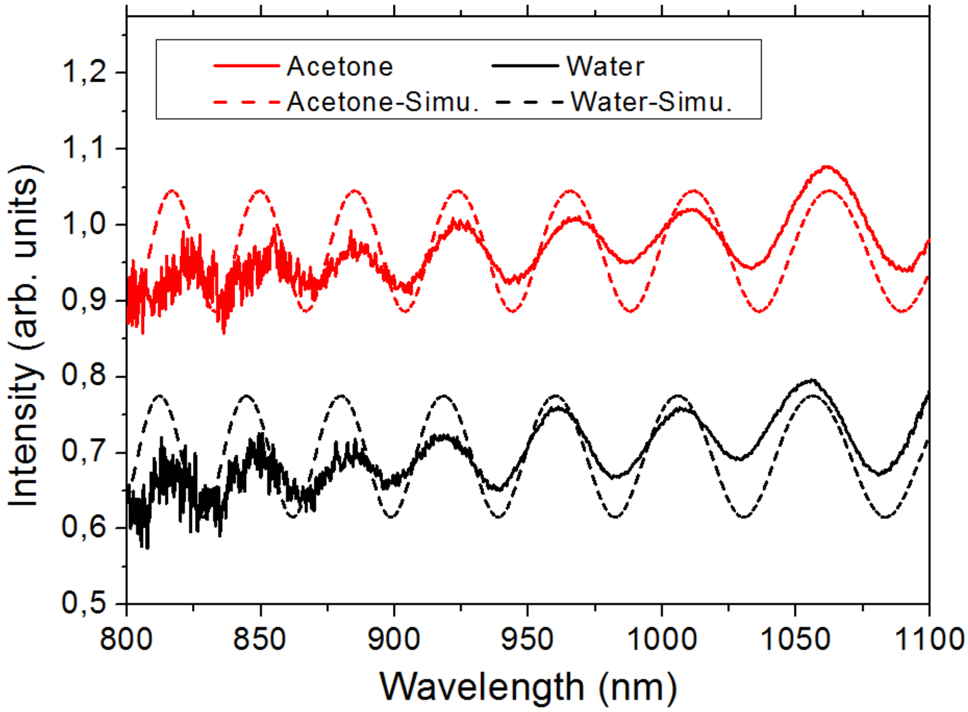


Figure 11. The calculated spectra for acetone- (marked as ‘Acetone-simu.’) and water- (‘Water-simu.’) filled LPSi compared with their experimental spectra.

### 4.3. Prospective applications: determination of salt & molecular concentrations

In addition to testing the LPSi interferometer with solvents, we have conducted some preliminary experiments using salt and molecule solutions as exploratory proof-of-concepts of the LPSi sensing capability. Indeed, the determination of salt/molecular concentrations might lead to useful applications, such as the detection of sugar level for diabetes. Such measurements rely on the fact that the refractive index of solutions containing molecules and salts varies with their concentrations [24]. For example, the increase of NaCl and glucose concentrations by 5% leads to ~0.01 and ~0.004 increases in refractive index of solutions, respectively.

We have tested the LPSi chip with NaCl solutions with salt concentration of 5% and 15% and the resulting spectra are shown in Figure 12. Both salt concentrations induce red shifts of the interference spectra, which is consistent with previous studies [11]. Analysis of the wavelength shift with the fitting method shows that the addition of 15% of NaCl in water results in a ~200 nm increase of the EOT. The theoretical change of refractive index obtained by applying the Bruggeman effective medium approximation, where the refractive index of 15% NaCl is ~1.370 [24], gives an increase in EOT of ~140 nm, which is in the range of experimental results.

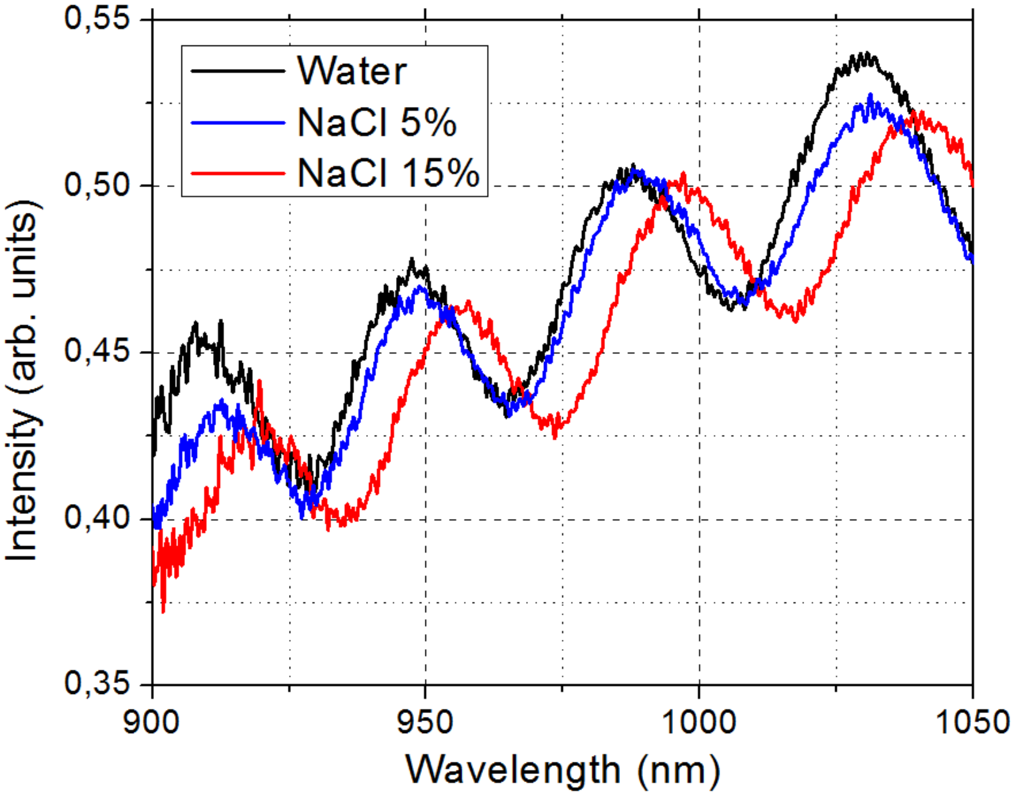


Figure 12. Reflectance spectra from the LPSi membrane filled with salt solution with different concentrations: pure water, NaCl 5% and NaCl 15%.

In Chapter 2, we have shown that fluorescein molecules can freely pass back and forth through the membrane: we have thus used the small molecules in the next experiments. Although fluorescein exhibits fluorescence that can perturb the optical measurement, the light emission (460-700 nm) and absorption (300-540 nm) spectra are located at wavelength <700 nm [25]: since measurements with our FTIR microscope are mostly efficient for wavelengths ≥800 nm, the influence of fluorescence should be negligible. 50 µM and 100 µM fluorescein solutions were tested on our LPSi platform and the results are displayed in Figure 13. The spectrum shift is barely detectable upon injection of the 50 µM fluorescein solution. But by using higher molecule concentration (100 µM), we start to see an obvious red shift. Through spectrum analysis (the fitting method), we derive an increase in EOT of ~100 nm. However, this does not agree with the calculation through Bruggeman effective medium approximation, because fluorescein 100 µM corresponds to a mass fraction of only ~0.0034%, while an EOT difference of 100 nm corresponds to an increase of molecule concentration of 10-15% [24, 26]. This discrepancy could be due to non-specific adsorption of fluorescein molecules on the pore wall when the molecular solution is pushed through the small pores by pressure.

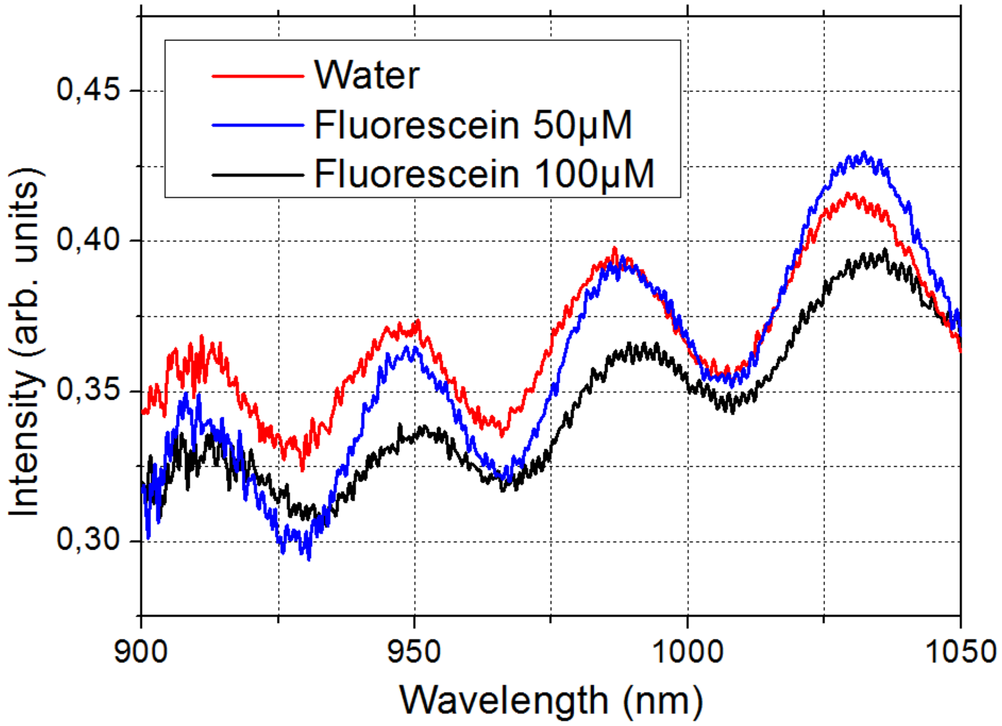


Figure 13. Reflectance spectra from the LPSi membrane filled with different molecule solutions: pure water, fluorescein 50 µM and 100 µM.

## 4.4. Problems and discussion

### 4.4.1. Stability of porous silicon membranes in aqueous solution

Fresh-etched porous silicon is not stable in aqueous solution because both Si–H and Si–Si reduce water. Our LPSi chip was left in atmosphere for days before use. A ~1 nm thick native oxide should thus be present in the nanopores, which enhances the stability of the membrane. However, since it is reported that the stability is still very poor [27], we have studied the influence of the membrane degradation on the stability of the sensor. The stability experiment consisted in filling the LPSi membrane with water and acquiring reflectance spectra regularly during 12 h. The results showed that the interference patterns experienced blue shifts and that the effective optical thickness was reduced by ~200 nm within 12 h. With an estimated 17 nm reduction of EOT per hour, we can conclude that the membrane degradation did not influence the experiments presented in the previous section that lasted less than 10 min and for which the change of EOT was an order of magnitude higher. However, future work should be conducted to improve the stability of porous silicon membranes to avoid drifts during measurements and current difficulty to provide adequate sensor calibration.

### 4.4.2. Interferometric detection at longer wavelengths

Looking at the interference patterns, we observe that the interference signal is better/cleaner at longer wavelengths. Therefore, we have tested the LPSi interferometer in a spectral range above 1 µm, with the intention to improve the quality of the interference spectrum for more accurate analysis and lower detection limit. To this aim, we decided to lead new experiments with the FTIR microscope using a mid-infrared detector (LN-MCT D316) under liquid nitrogen cooling conditions. Various liquids were again tested following the procedure previously described and Figure 14 shows a resulting example presenting an obvious spectrum shift (~1100 nm of EOT variation). Compared to the near-infrared range, the new considered range spectrum contains more fringes, which means an increased interference signal that should lead to better interferometry transduction and that should therefore be explored in the future.

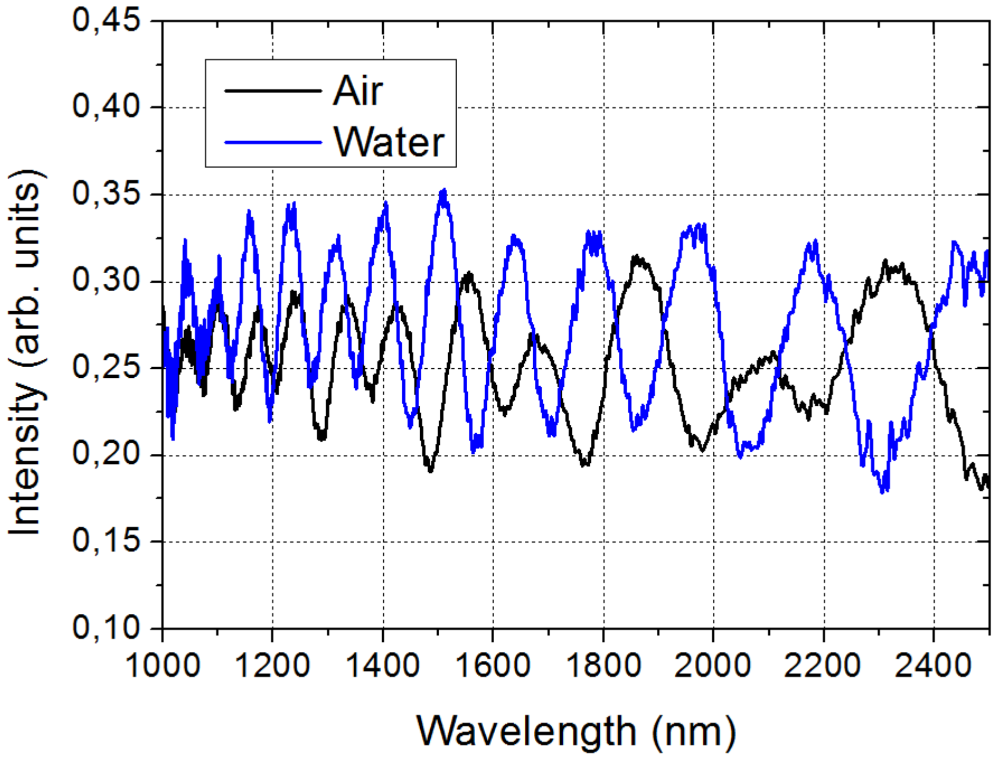


Figure 14. Reflectance spectra of the LPSi membrane filled with air and DI water in the short wavelength-infrared range.

## 5. Conclusion and perspectives

In this chapter, we have demonstrated the Fabry-Pérot interferometric transduction capability of the fabricated lateral porous silicon membranes. The specificity and difficulty of our study is that the LPSi membranes exhibit small dimensions, which has increased the difficulty to obtain clean and exploitable interference signals. Nevertheless, this issue was overcome by optimizing the experimental setup and the optical measurement conditions. We were able to identify the presence of solvents with different refractive index, after analyzing the experimental interference spectra and comparing them with simulated ones, thus providing a proof-of-concept of the LPSi interferometric transducer.

This study constitutes the first attempt to use a lateral porous silicon membrane in flow-through configuration for interferometric sensing. The achievement of flow-through as opposed to flow-over configuration should open the doors to improvements of the sensitivity of biosensors in the future. This work also demonstrates that the optical transduction can be achieved on a small porous membrane, which could be of great interest for the miniaturization of optical biosensors. However, the issue of the present device is its low sensitivity, which is limited to a 100 nm EOT resolution. Future work should be done to improve the detection limit. Besides, with the realization of flow-through biosensors in mind, where biomolecules are to be identified, we should first fabricate porous silicon membranes with larger pore size to allow most biological molecules to flow through, and second, we should develop biofunctionalization protocols to immobilize probe molecules at the surface of porous silicon. Finally, we should increase the stability of porous silicon in aqueous environment: oxidation processes could be used in future fabrication of LPSi membranes to tackle this constraint.

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# Conclusion

Microfluidics and the miniaturization of sensors and actuators have enabled the emergence of lab-on-a-chip (LOC) devices that integrate medical laboratory functions on chip for biomedical applications, leading to faster/cheaper/portable analysis using smaller amount of sample and reagents. Porous membranes are of great interest for on-chip sample preparation and analysis since they enable size- and charge-based molecule separation, but also molecule pre-concentration by ion concentration polarization. Out of the various materials available to constitute porous membranes, porous silicon offers many advantages, such as large surface area, convenient surface chemistry, biocompatibility, and optical properties, which have inspired various applications especially in the biomedical field. Among the formats of porous silicon in microfluidic devices, porous silicon membranes are of special interest because of their high permittivity, selectivity and tuning properties. The current fabrication processes for porous silicon membranes imply their integration into 3D microfluidic systems, which are more disadvantageous than planar fluidic systems.

In this thesis, we have presented two processes (the SOI process and the implantation process) for the realization of lateral porous silicon membranes and their integration into planar (2D) microfluidic channels. We have then investigated the possibility to use these lateral porous silicon membranes for various applications: size-based filtering in lab-on-chip, pre-concentration of molecules by ion concentration polarization through the ion selectivity property of the lateral porous membranes and finally the possibility to carry out interferometry biosensing analogously to vertical membranes but in a flow-through configuration.

The key ideas of the SOI process are to guide pore formation horizontally during anodization by means of electrodes patterned onto the silicon surface and to spatially localize porous silicon growth within a controlled depth through the use of silicon-on-insulator substrates. The feasibility of the SOI process was demonstrated by the fabrication of 10 µm thick mesoporous membranes with ~25 nm diameter pores bridging 20 µm deep microchannels. The implantation process relies on the local manipulation of dopant type and concentration by boron and phosphorus implantation. During anodization, pores propagate in a heavily doped boron layer sandwiched between an n-type surficial layer and the n-type bulk silicon in a strict lateral fashion along the current flow injected via a patterned electrode. We have modeled our process using a 2D simulation tool to estimate the dopant profiles after ion implantation and we have used four-point probe measurement to experimentally find the optimal doses by measuring the sheet resistance of the surficial layer. The feasibility of the implantation process was demonstrated by the fabrication of ~4 µm thick and 10 µm long mesoporous membranes with pore size and porosity respectively ranging from ~3 to ~30 nm and ~15 to ~65%.

To demonstrate the ICP preconcentration capability, we have studied two configurations of LPSi preconcentrators. Double-channel devices have shown a preconcentration factor of 100 by applying constant voltages and 5000 by applying increasing voltages. Single-channel devices have shown a factor of 100. We have also demonstrated the Fabry-Pérot interferometric transduction capability of the fabricated LPSi membranes. The specificity and difficulty of our study is that the LPSi membranes exhibit small dimensions, which has increased the difficulty to obtain clean and exploitable interference signals. Nevertheless, this issue was overcome by optimizing the experimental setup and the optical measurement conditions. We were able to identify the presence of solvents with different refractive index, after analyzing the experimental interference spectra and comparing them with simulated ones, thus providing a proof-of-concept of the LPSi interferometric transducer.

In conclusion, the two fabrication processes presented here enable the confinement of lateral porous silicon membranes at specific locations with desirable pore size and porosity into lab-on-a-chip devices. While obvious applications include on-chip sample preparation through size-based filtration as demonstrated here, such membranes could also be used for other purposes, such as sample pre-concentration and real-time biosensing. In fact, our study showed for the first time the use of LPSi membranes for ICP preconcentration purposes where LPSi membranes have proved to display high counterion transport efficiency and perm-selectivity. This could lead to lower energy consumption, which is of crucial importance for portable micro total analysis systems. The study constitutes also the first attempt to use a lateral porous silicon membrane in flow-through configuration for interferometric sensing. The achievement of flow-through as opposed to flow-over configuration should open the doors to improvements of the sensitivity of interferometric porous silicon biosensors in the future.

For future work, better pore regularity should be sought to improve filtering and biosensing capabilities and should be obtained by adapting the pore propagation to specific crystallographic directions. In this thesis, the direction of pore propagation is primarily in the

<110> direction (since this enables to conveniently access cross-sectional views of LPSi membranes by cleaving the wafer). However, the optimum direction should be <100> because the Si-H bonds on the (100) crystallographic faces tend to be more prone to dissolution than on other faces. Besides, in order to achieve higher ICP preconcentration factors, we should improve the electrical insulation of the membrane and channels. To do so, we should study various insulating methods leading to the creation of thick oxide layers. However, care must be taken to avoid clogging or breaking the porous membranes. Finally, to realize flow-through biosensors, we will need to overcome many difficulties: (1) The fabrication of LPSi membranes with larger pore size (*e.g.* 50 nm); (2) The biofunctionalization of the LPSi membrane; (3) The improvement of interference signal resolution for better sensitivity. These proposed studies should help reaching the ultimate goal of this work, which is to create an all-in-one solution for point-of-care testing.

# List of publications

Journal paper

- **Yingning He**, and Thierry Leïchlé. "Fabrication of lateral porous silicon membranes for planar microfluidics by means of ion implantation." *Sensors and Actuators B: Chemical* 239 (2017): 628-634.

Conference papers

- **Yingning He**, David Bourrier, Eric Imbernon, Adhitya Bhaswara, Xavier Dollat, Fuccio Cristiano, and Thierry Leichle. "Lateral porous silicon membranes with tunable pore size for on-chip separation." Proceedings of the *29th International Conference on Micro Electro Mechanical Systems (MEMS)*, 24–28 January, 2016, Shanghai, China, 497-500.

- **Yingning He**, and Thierry Leïchlé. “Lateral porous silicon membranes integrated to planar microfluidics for filtering applications.” Proceedings of the *10th Porous Semiconductors-Science and Technology (PSST)*, 6–11 March, 2016, Tarragone, Spain, 316-317. **(Oral presentation)**

- **Yingning He**, David Bourrier, and Thierry Leïchlé. “Lateral porous silicon membranes with tunable pore size and porosity for 2D microfluidics.” *41st Micro and Nano Engineering (MNE)*, 21-24 September, 2015, The Hague, The Netherlands. **(Oral presentation)**

**Author:** Yingning HE

**Title:** Lateral Porous Silicon Membranes for Planar Microfluidic Applications

**Thesis director:** Thierry LEICHLE and Liviu NICU

**Date and place of the defense:** LAAS-CNRS, 22nd November 2016

**Summary**

Lab on a chip devices aim at integrating functions routinely used in medical laboratories into miniaturized chips to target health care applications with a promising impact foreseen in point-of-care testing. Porous membranes are of great interest for on-chip sample preparation and analysis since they enable size- and charge-based molecule separation, but also molecule pre-concentration by ion concentration polarization. Out of the various materials available to constitute porous membranes, porous silicon offers many advantages, such as tunable pore properties, large porosity, convenient surface chemistry and unique optical properties. Porous silicon membranes are usually integrated into fluidic chips by sandwiching fabricated membranes between two layers bearing inlet and outlet microchannels, resulting in three-dimensional fluidic networks that lack the simplicity of operation and direct observation accessibility of planar microfluidic devices. To tackle this constraint, we have developed two methods for the fabrication of lateral porous silicon membranes and their monolithic integration into planar microfluidics. The first method is based on the use of locally patterned electrodes to guide pore formation horizontally within the membrane in combination with silicon-on-insulator (SOI) substrates to spatially localize the porous silicon within the channel depth. The second method relies on the fact that the formation of porous silicon by anodization is highly dependent on the dopant type and concentration. While we still use electrodes patterned on the membrane sidewalls to inject current for anodization, the doping via implantation enables to confine the membrane analogously to but instead of the SOI buried oxide box. Membranes with lateral pores were successfully fabricated by these two methods and their functionality was demonstrated by conducting filtering experiments. In addition to sample filtration, we have achieved electrokinetic pre-concentration and interferometric sensing using the fabricated membranes. The ion selectivity of the microporous membrane enables to carry out sample pre-concentration by ion concentration polarization with concentration factors that can reach more than $10^3$ in 10 min by applying less than 9 V across the membrane. These results are comparable to what has already been reported in the literature using e.g. nanochannels with much lower power consumption. Finally, we were able to detect a change of the porous silicon refractive index through the shift of interference spectrum upon loading different liquids into the membrane. The work presented in this dissertation constitutes the first step in demonstrating the interest of porous silicon for all-in-one sample preparation and biosensing into planar lab on a chip.

**Keywords**: Anodization, Filtration, Ion concentration polarization, Lab on a chip, Membrane, Microfluidics, Optical biosensor, Porous silicon

**Auteur:** Yingning HE

**Titre:** Intégration de membranes de silicium poreux à pores latéraux dans des systèmes microfluidiques planaires

**Directeur de thèse:** Thierry LEICHLE et Liviu NICU

**Lieu et date de soutenance:** LAAS-CNRS le 22 novembre 2016

## Résumé

Les laboratoires sur puce visent à miniaturiser et à intégrer les fonctions couramment utilisées dans les laboratoires d'analyse afin de cibler des applications en santé avec un impact prometteur sur le diagnostic médical au lit du patient. Les membranes poreuses sont d'un grand intérêt pour la préparation et l'analyse d'échantillon sur puce car elles permettent la séparation par taille/charge de molécules, mais également leur pré-concentration. Parmi les matériaux disponibles pour constituer des membranes poreuses, le silicium poreux présente de nombreux avantages tels que le contrôle précis de la taille des pores et de la porosité, une chimie de surface pratique et des propriétés optiques uniques. Les membranes de silicium poreux sont généralement intégrées dans des puces fluidiques en les montant entre deux couches comportant des micro-canaux, formant ainsi des réseaux fluidiques à trois dimensions, peu pratiques et peu adaptés à l'observation directe par microscopie. Dans ces travaux de thèse, nous avons développé deux méthodes de fabrication de membranes de silicium à pores latéraux qui permettent leur intégration monolithique dans des systèmes microfluidiques planaires. Le premier procédé est fondé sur l'utilisation d'électrodes localement structurées afin de guider la formation de pores de manière horizontale, en combinaison avec des substrats type silicium sur isolant (SOI) pour localiser spatialement la formation de silicium poreux dans la profondeur du canal. La deuxième méthode repose sur le fait que la formation de silicium poreux par anodisation est fortement dépendante du type de dopant et de sa concentration. Bien que nous utilisons encore le même type d'électrodes structurées sur les parois latérales de la membrane pour injecter le courant lors de l'anodisation, le dopage par implantation permet de confiner la membrane, de façon analogue mais à la place de l'oxyde enterré du SOI. Des membranes à pores latéraux ont été fabriquées par ces deux méthodes et leur fonctionnalité a été démontrée en réalisant des expériences de filtrage. En plus de la filtration d'échantillon, les membranes ont été utilisées pour étudier la possibilité d'effectuer de la pré-concentration électrocinétique et de la détection interférométrique. La sélectivité ionique des membranes microporeuse permet la pré-concentration moléculaire avec des facteurs de concentration pouvant atteindre jusqu'à $10^3$ en 10 min en appliquant moins de 9 V. Ces résultats sont comparables à ceux rapportés dans la littérature à l'aide par exemple de nanocanaux avec une consommation d'énergie beaucoup plus faible. Enfin, nous avons pu détecter une variation de l'indice de réfraction du silicium poreux par le décalage du spectre d'interférence lors du chargement de différents liquides injectés dans les membranes. Le travail présenté dans cette thèse constitue la première étape dans la démonstration de l'intérêt du silicium poreux pour la préparation d'échantillon et la biodétection dans des laboratoires sur puce planaires.

**Mots-clés**: Anodisation, Biocapteur optique, Filtration, Laboratoire sur puce, Membrane, Microfluidique, Polarisation de concentration ionique, Silicium poreux