Flexible substrate technology for millimeter wave applications

Zhening Yang

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Directeur/trice(s) de Thèse :

Daniela DRAGOMIRESCU, Professeur, INSA-Toulouse
Alexandru TAKACS, Maître de Conférences, Université Paul Sabatier

Jury :
Raluca MULLER, Directeur de Recherche, IMT Bucharest (Rapporteur)
George PAPAIOANNOU, Professeur, University of Athens (Rapporteur)
Anthony GHIOTTO, Maître de Conférences, IMS-Bordeaux (Examinateur)
Patrick PONS, Directeur de Recherche, LAAS-CNRS (Examinateur)
Invité(s) :
Alexandru MULLER, Directeur de Recherche, IMT Bucharest
Samuel CHARLOT, Ingénieur, LAAS-CNRS

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I. General introduction

This thesis is part of research effort to develop a 3D heterogeneous integration of wireless sensor node on flexible substrate for the high data rate communication in the unlicensed 60GHz band. The System in Package (SiP) should have a very low power consumption and very low cost to meet the stringent requirement of applications like Wireless Sensor Networks (WSNs). As shown in Figure I.1 and Figure I.2, the deployment of WSNs for Structure Health Monitoring (SHM) can allow better maintenance of the aircraft and predictive of the aircrafts in a long term approach [1].

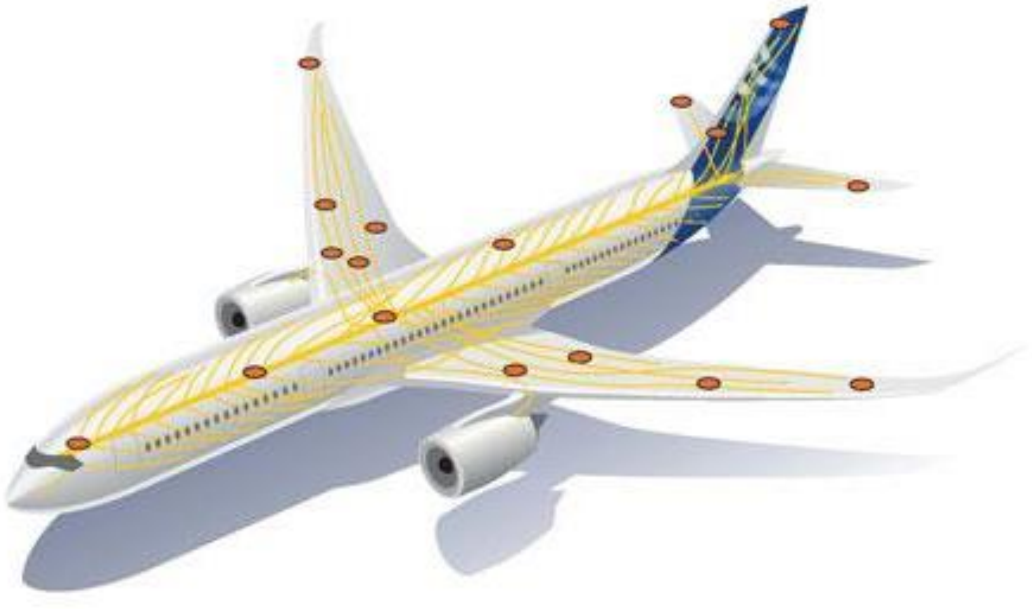


Figure I.1: Structural health monitoring (SHM) systems arrayed in keay areas where loads are highest. Source: Airbus

Using a flexible substrate for wireless sensor node integration can offer the advantage of being localized in areas with access difficulty especially in non-planar area or in difficult access places. Figure I.3 shows each node is composed of Nano-sensors, transceivers and TX/RX antenna. Nanotechnologies made it possible the development of ultra-sensitive nano-sensors based on nanoparticles deposition [2][3]. Transceivers become more and more miniaturized and hence enable the possibility of postpone them onto flexible substrate [4][5]. One can also take the benefits from nano-ink with silver nanoparticles to develop antenna directly on flexible substrate[6][7]. These antennas can be integrated on the flexible substrate along with the developed nano-sensors and miniaturized transceivers, which is the very innovative approach of this thesis.

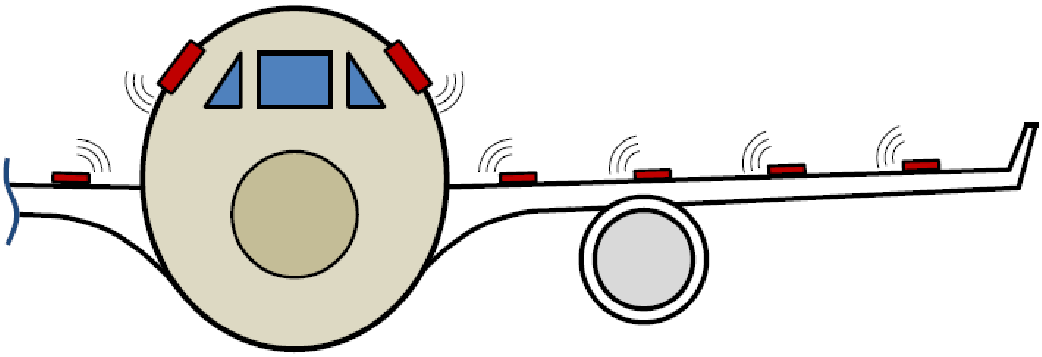


Figure I.2: WSNs deployed on aircraft wings for real-time in-flight testing.

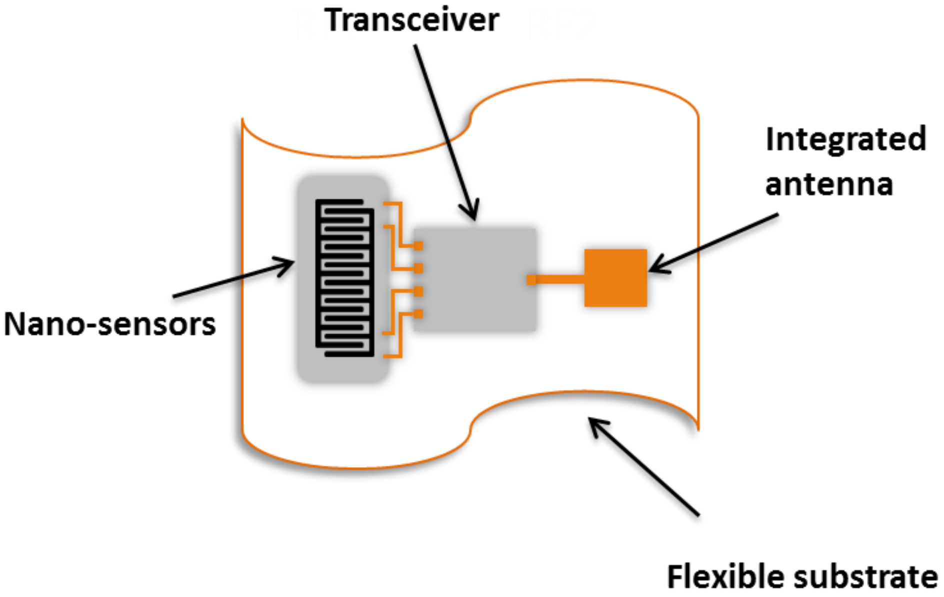


Figure I.3: Concept of the communicating nano-objects on flexible substrate.

In the following pages the research work accomplished during the three years of Ph.D. will be discussed.

Chapter II gives an introduction on flexible electronic technology. It contains discussions about materials for flexible electronic and different fabrication technology.

A theoretical discussion will also be given.

Chapter 0 describes about the RF characterization of the flexible substrate by using a ring resonator and the adopted microfabrication process in clean room. Then antennas design and its characterization, which including reflecting coefficient, gain and radiation pattern.

Chapter IV deals the implementation of Kapton technology at 60 GHz, including the substrate preparation the implementation of circuits with electrical patterns on single/both side of the substrate.

Chapter V presents the technique of heterogeneous integration on flexible substrate, the DC/RF tests and their results, also a new gold bump forming process is shown in this chapter.

Finally, Chapter VI concludes on integration of wireless sensor node on flexible substrate and shows perspectives towards a fully integrated TX/RX link.

II. State of art of flexible electronics technology

II.1 Introduction to Wireless Sensors Network (WSN)

The deployment of Wireless Sensors Network (WSN) for Structure Health Monitoring (SHM) will allow better maintenance of the aircraft, and predictive diagnosis for the aircrafts in a long-term approach.

The major driver for the aircraft industry development [8] nowadays is the eco-efficiency. That means the need of the development of future greener aircrafts with lowest carbon emission which pass by less weight in the aircraft while keeping the passenger’s comfort. The new generation of aircraft has to be also high performance while staying cost efficiency. That will be a global system challenge to develop the new generation aircrafts which can be solved only by a global system solution: rethink all the system architecture of the aircraft.

In this context, structure health monitoring (SHM) becomes a very important issue. The deploying of a whole sensor network on the structure of the aircraft is necessary. Nowadays, it is estimated that more than 40000 aircrafts will be in activity by the end of 2025 and more than 1000 sensors are necessary for each one. The facility of sensor deployment becomes also a main issue.

The introduction of sensor network for structure health monitoring will improve the maintenance system and will lead to safer aircrafts, which is another major topic together with eco-efficiency and also to lower airplane ticket cost for passengers. It is estimated that a decrease of 3% to 12% in the prices of airline tickets can be expected. Today the deployment of the sensors is limited by wired connections which lead to excess weight and carburant consumption (the major driver is eco-efficiency, greener aircrafts). The wired sensor put also a huge problem of installation. The wireless solution, Wireless Sensors Network (WSN), is imposed by these major constraints.

The aeronautic application impose severe constrains for the reliability, the ElectroMagnetic Compatibility (EMC), the immunity of the interferences and the power consumption. All these constraints lead us to choose to develop short distance wireless communications using ultra-wide band impulse radio technique (UWB-IR) followed by a RF front-end at 60GHz.

The 60 GHz band is chosen because it is ideally suited for applications required very high data rate, energy-autonomous Wireless Sensor Networks (WSNs) or Gbit/s multimedia links with low power constraints.

II.2 Introduction to flexible electronics

In the past decade, the interest from both academia and industry in the field of flexible electronics has risen enormously due to the unique properties of being bendable, conformably shaped, elastic, lightweight, and non-breakable. In fact, this research topic tops the pyramid of research priorities requested by many national agencies.

According to the market analysis, the total market of flexible electronics will grow from 26.54 billion USD in 2016 to 69.03 billion USD in 2026 [9].

Uncompressed digitized audio, video content can be transmitted in a short-range (below 10 m) with a data rate up to 10.7 Gb/s using unlicensed 60 GHz transceiver [10]. This technology enables applications like wireless personal area networks (WPANs), in-flight entertainment (IFE), and structure health monitoring (SHM). The need for integrating all function modules on a single chip or into a single package is emerging.

This chapter deals with the state of the art of materials and fabrication technologies for flexible electronics, especially in the 60 GHz millimeter-wave spectrum.

II.3 Materials for flexible electronics

Substrates that used in flexible electronics need meet various requirements as following [11][12]:

a) Thermal properties − Heat resistance is extremely important for flexible substrates, for example the glass transition temperature (Tg) of a polymer, must be compatible with the maximum fabrication process temperature (Tmax).

b) Chemical properties – The substrate should not release contaminants and should be inert against the process chemicals, and unlike glass substrates which are essentially gas-impermeable, plastic substrates are gas-permeable in a certain way, for organic light-emitting diode (OLED) application the water permeation rate should lower than 10^{-6} g/m^2/day and the oxygen permeation rate lower than 10^{-3} to 10^{-5} cm3/m^2/day.

c) Dimensional stability − Dimensional changes may result in deformation (especially warping) and distortion of device films, the causes can be moisture, solvents ueds during manufacture process, exposure to chemicals, and repeated heating and cooling cycles. That is to say, ensuring dimensional stability requires low moisture absorbency, chemical resistance, a low coefficient of thermal expansion, etc.

d) Electrical and RF properties – Electrically insulating substrates minimize the coupling capacitances. RF properties (permittivity and permeability) mainly determine the bandwidth and the efficiency performance of the planar antenna.

e) Mechanical properties – A high elastic modulus makes the substrate rigid, and a hard surface supports the device layers under impact.

f) Optical properties − In display applications, high transparency and optically isotropic substrates (with low birefringence) are required, especially for liquid crystal displays (LCDs).

g) Surface flatness and roughness − Poor surface flatness can cause the gap between top and bottom substrates to become irregular in the case of LCDs, for example, causing image distortion. The thinner the device films, the more sensitive their electrical function will depend on the surface roughness. Asperities and roughness over short distance must be avoided.

Materials used for flexible applications are generally classified into two categories: organic substrate, and inorganic substrate.

II.3.1 Organic substrate materials

a) Polyethylene terephthalate (PET)

PET is a plastic resin and the most common type of polyester. It can be obtained through the polycondensation of ethylene glycol and terephthalic acid. PET is often used in some printed circuit boards for large circuit not requiring soldering because the lack of heat resistance (Tg = 80 °C).

b) Polyethylene naphthalate (PEN)

PEN is chemically quite similar to PET, and is generally produced by polycondensating ethylene glycol and naphthalene-2.6-dicarboxylic acid, it has more heat resistance (Tg = 120 °C), more chemical resistance, and more dimensional stability than PET.

c) Polyimide (PI)

Polyimide is synthesized by polymerizing an aromatic dianhydride and an aromatic diamine. The most notable characteristics of polyimide are its excellent heat resistance (Tg between 360 °C and 410 °C) and excellent chemical resistance (no known organic solvents for the film). It also has excellent rigidity, flexibility and electrical properties.

The main problems of polyimide are water absorption and a high moisture absorption rate at 4% after 24 hours water immersion at 23°C [13], which result a poor dimensional stability. In our own test, the resonance frequency of a v-band patch antenna is shifted 5% to the lower frequency after 12 hours' water immersion at 23°C.

d) Liquid crystal polymers (LCPs)

LCPs are partially crystalline aromatic polyesters based on p-hydroxybenzoic acid and related monomers, and have good mechanical properties and high heat resistance (Tg = 145 °C), excellent chemical resistance, excellent moisture absorption rate, along with a low water absorption rate < 0.05% at 75% relative humidity (RH) in 40°C atmosphere.

e) Paper-based substrate

Paper-based substrate is a low-cost “green” substrate. It is extremely environment-friendly because it is cellulose in nature and renewable. But it has limitations in terms of high roughness, heat resistance, chemical resistance and water absorption make it problematic for electronics.

Table II.1: Comparative properties of organic substrates.

Material	PET	PEN	Kapton	LCP	Paper
Dielectric constant	3.3~3.4	~2.9	3.2~3.4	~3.1	~3.2
Loss Tangent	~0.01	~0.025	~0.002	0.002~0.005	~0.007
Melting Point	~260 °C	~265 °C	NA	285 °C~315 °C	NA
Glass-transition temperature	78 °C	121°C	410°C	NA	NA
Chemical resistance	Good	Good	Good	Excellent	NA
Mechanical properties	Good	Good	Excellent	Good	NA

II.3.2 Inorganic substrate materials

a) Thin glass

Glass is used as standard substrate for various types of devices. Plate glass becomes flexible when its thickness is reduced to 100 µm or 200 µm [14]. Glass foils as thin as 25 µm can be produced by the down-draw technology [15]. Glass has essentially excellent performance in nearly every aspect: resistance to most process chemicals, high temperature tolerance, dimensional stability, optical characteristics, no out-gassing, impermeability against oxygen and water. However, since glass lacks flexibility and is very fragile, it is very difficult to handle.

b) Metal foil

A typical stainless steel meets many requirements imposed on flexible substrates like high resistance to corrosion and process chemicals, very high temperature tolerance, and dimensionally stable, impermeable to moisture and oxygen. The drawback of metal substrates is that i) they are completely opaque, and thus cannot use for transmissive displays; ii) they are electrically conducting, an insulating layer must be coated to provide circuit isolation.

In conclusion, we have selected Kapton, a polyimide film developed by Dupont as substrate for the development of passive circuits due to its good RF and thermal properties, very good flexibility over a wide temperature range (-73 to +400°C), highly resistant to many chemical solvents, and most importantly for the price, hence we can deploy the WSNs nodes as many as possible at a relatively low cost.

II.4 Fabrication technology for flexible electronics

II.4.1 Conventional technologies

In conventional process, photolithography, chemical etching, and physical vapor deposition (PVD) coating process are usually combined to fabricate metallic patterns, on a substrate.

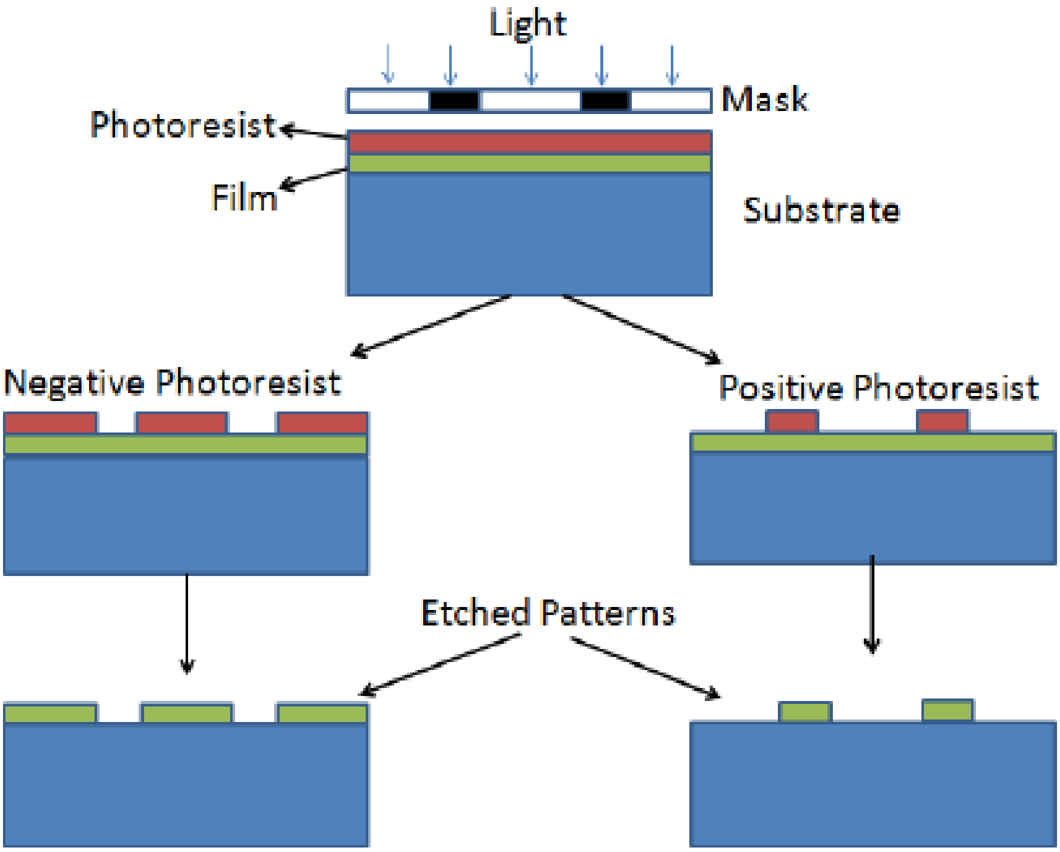

Light
Mask
Photoresist
Film
Substrate
Negative Photoresist
Positive Photoresist
Etched Patterns

Figure II.1: Process flow of the photolithography process [16].

There are two types of photoresist (organic polymers whose chemical characteristics change when exposed to UV light): positive and negative. For positive resists, the exposed area becomes more soluble in the developer. Negative resists behave in an opposite way, the exposed area becomes polymerized, and less dissolvable in the developer.

Negative resists were popular back in the early history of microfabrication process, a major disadvantage is that the exposed regions swell as the counterpart is dissolved by the developer, which compromise the resolution of resist, hence, positive resists became more widely used since they offer better process controllability and higher resolution than negative resists.

Despite the conventional process can produce high complexity and fine detailed patterns, its lengthy process, low throughput, involvement of dangerous chemicals massive vacuum system requirement are major drawbacks of this technology.

II.4.2 Direct printing technologies

The new emerged direct writing technologies that can significantly simplify the fabrication process and dramatically reduce the manufacturing costs became popular recently, this type of technology consist of patterning in a single shot semiconductor materials or metallic materials onto a substrate. Various writing methods, such as screen printing, flexographic printing, gravure printing, and inkjet printing will be described in detail on the following sections.

a) Screen printing

Screen printing is one of the simplest and most cost effective methods used for the fabrication of printed electronics. It is also commonly used for metallization of silicon solar cells.

To produce a printed pattern, the ink is pressed with a squeegee blade through a screen mesh (stencil) onto the affixed substrate. The stencil is defined on the mesh photochemically or manually, and the squeegee is made of a rubber and therefor easy to wear. Due to the simplicity of the process, it has been widely employed and is compatible with a wide variety of functional inks and substrates. Recently, screen printed electrolyte-gated transistors on polyimide (PI) with graphene patterns as narrow as 40 μm has been reported [17].

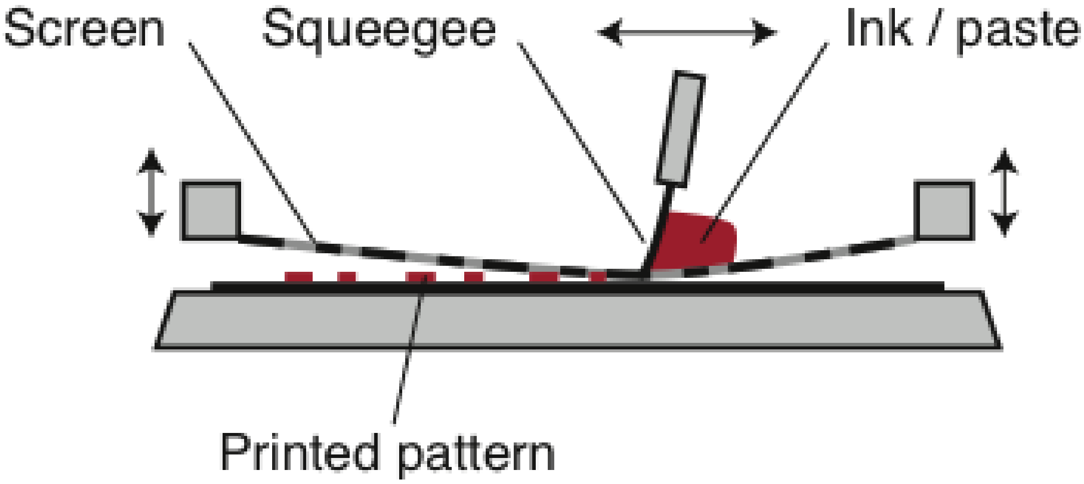


Figure II.2: Principle of screen printing[18].

b) Flexographic printing

Flexographic printing is a relief printing technique commonly used in the commercial printing industry, especially for foil substrates. The image is printed from protruding elements on a soft, rubber cylinder (plate cylinder), transferring the pattern on substrates.

In a flexographic printing process, the anilox cylinder is first immersed in an ink bath and a doctor blade is used to scrape off the excess ink from the non-engraved surface of anilox cylinder. The ink is then brought into contact with the soft printing plate, which is subsequently transferred to the substrate.

With flexography, RFID tags has been printed on paper substrate with silver ink [19]. Continuous conductive tracks of silver ink have also been reported on a indium tin oxide (ITO) coated, heat stabilized polyethylene terephthalate (PET) film with a minimal line widith of 74.6 µm [20]. The typical resolution limit is about 50 to 100 µm.

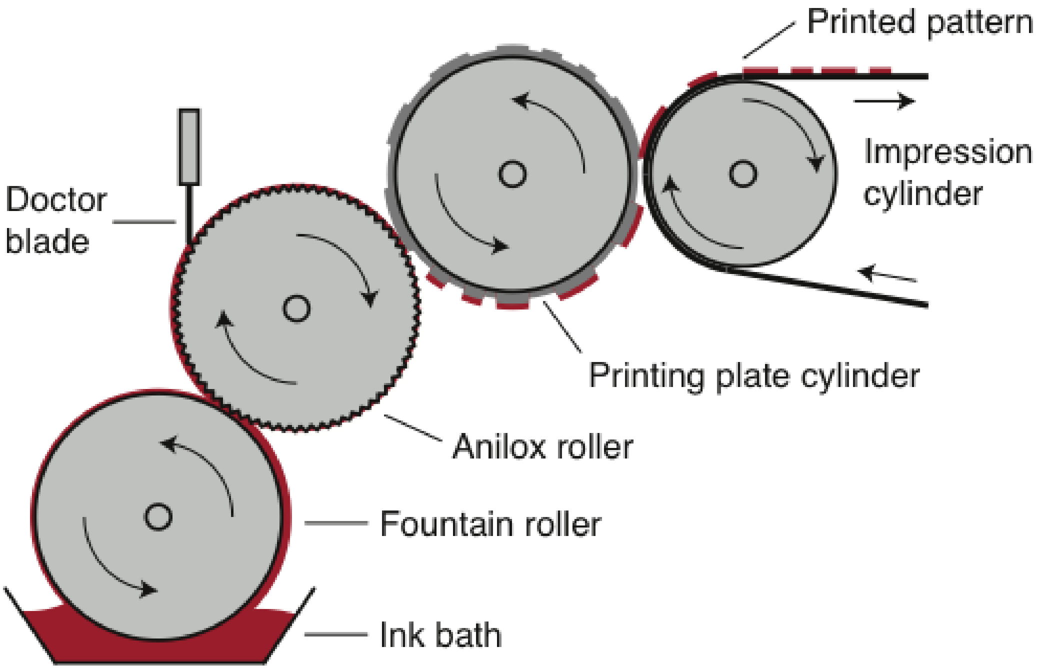

Printed pattern
Impression cylinder
Doctor blade
Printing plate cylinder
Anilox roller
Fountain roller
Ink bath

Figure II.3: Principle of flexographic printing [21].

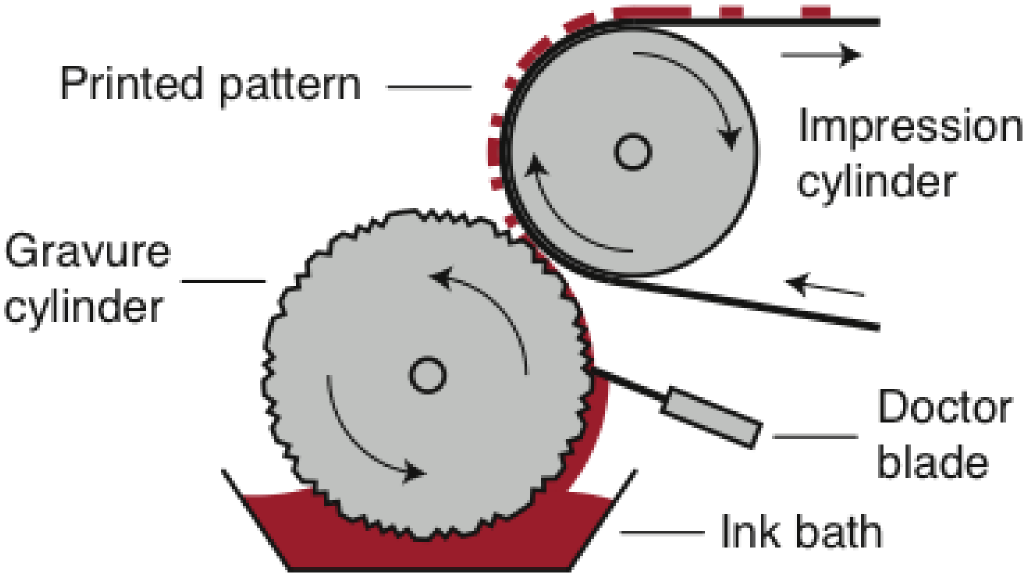

Printed pattern
Impression cylinder
Gravure cylinder
Doctor blade
Ink bath

Figure II.4: Principle of gravure printing[23].

c) Gravure printing

Contraire to the flexography, the relatively low viscous ink is transferred from the pits of the master to the substrate. It has four basi component to each printing unit: an engraved (gravure) cylnder, ink bath, doctor blade and the impression roller (cylinder). The key of a gravure printing is the gravure cylinder, which carries the image design (ink) to be printed. Excess of ink is removed from the protruding elements of the gravure cylinder by the doctor blade before transferred to the substrate. Grauvre printing of continuous graphene pattern as fine as 30 μm on Kapton substrate has been reported [22].

d) Inkjet printing

Inkjet printing of RF circuits and antennas using highly conductive inks have become very popular in recent years [24]. This new technology utilizes conductive inks baked on different nanostructure materials such as silver nanoparticle based ink to form pattern on the substrate from a digital image. It is a low-cost, non-impact and raid technique with a large potential to manufacture electronic circuits.

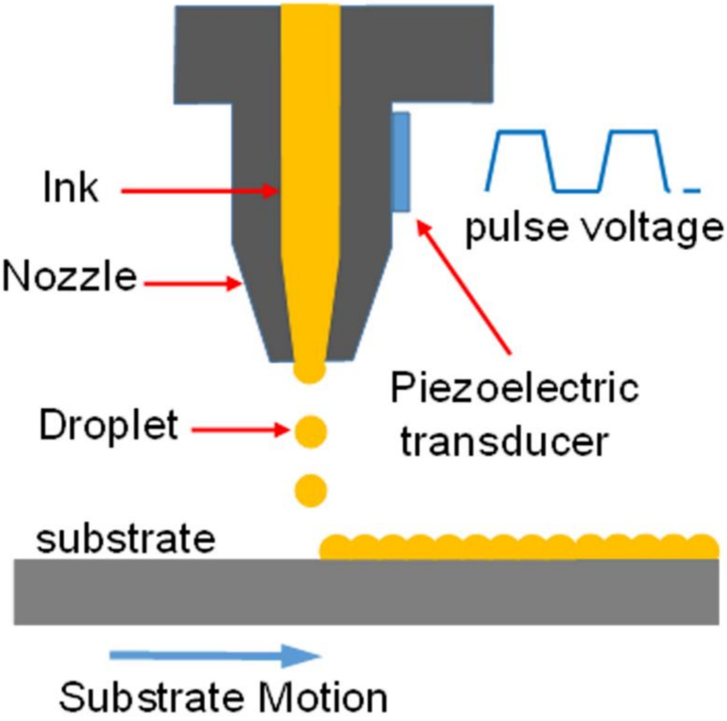


Figure II.5: Principle of inkjet printing process [28].

By using inkjet printing, a square monopole antenna on PEN has been reported on [25], a transmission lines with silver nano-particles has been printed on Kapton [26], and a 60 GHz CPW fed dipole antenna on PET substrate has been reported on [27].

II.5 Evolution of electronic packaging

Over the past decades, electronic assembly took different paths of evolution. Such as System on Chip, Chip on Board, System in Package, System on Package and Package on Package.

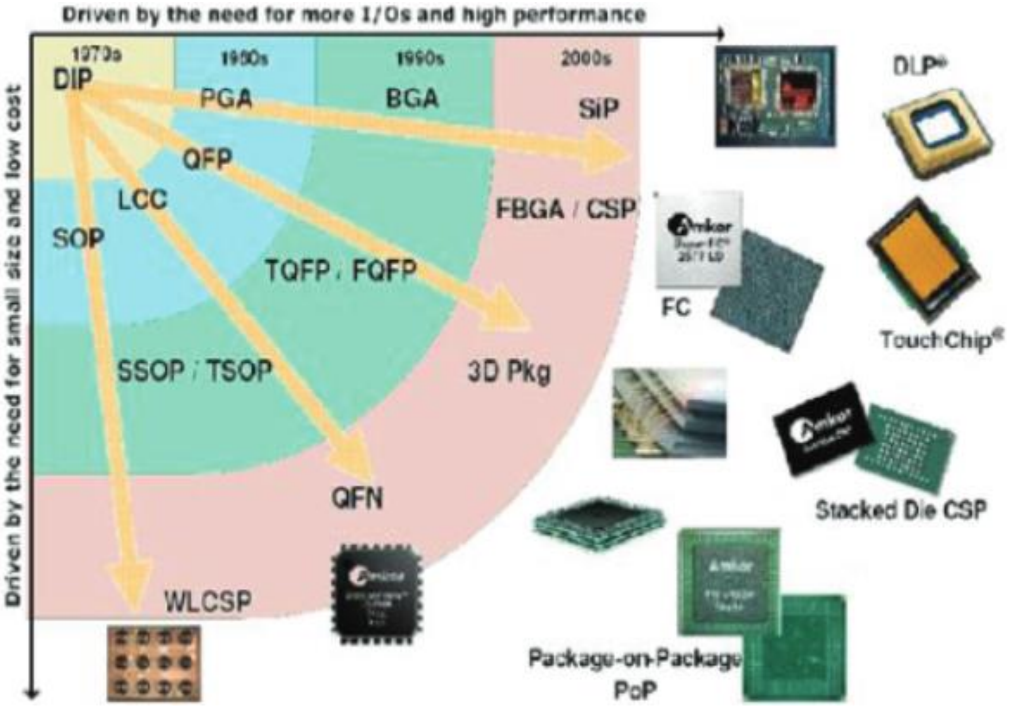

Driven by the need for more I/Os and high performance
Driven by the need for small size and low cost
1970s
1980s
1990s
2000s
DIP
PGA
BGA
SiP
QFP
LCC
SOP
FBGA / CSP
TQFP / FQFP
SSOP / TSOP
3D Pkg
QFN
WLCSP
DLP®
FC
TouchChip®
Stacked Die CSP
Package-on-Package
PoP

Figure II.6: Development of packages in the last decades [29].

II.5.1 System on Chip (SoC)

The System on Chip (SoC) is a technology operating at zero level packaging and answers to the More Moore domain. By its name, System on Chip is an integrated system implemented in CMOS (Complementary Metal Oxyde) technology. These modern technologies are the reasons that made possible the integration of a complete electronic system on a single silicon chip. This integrated circuit (IC), generally complex, contains a large number of different electronic functions. Recent SoC can contain several microprocessor cores, Digital Signal Processing (DSP) core, associated with hardware operators, memories and I / O interfaces (Figure II.7). This SoC technology is often used for embedded applications. On chip integrated antenna was reported in [30] for 60 GHz WPAN applications.

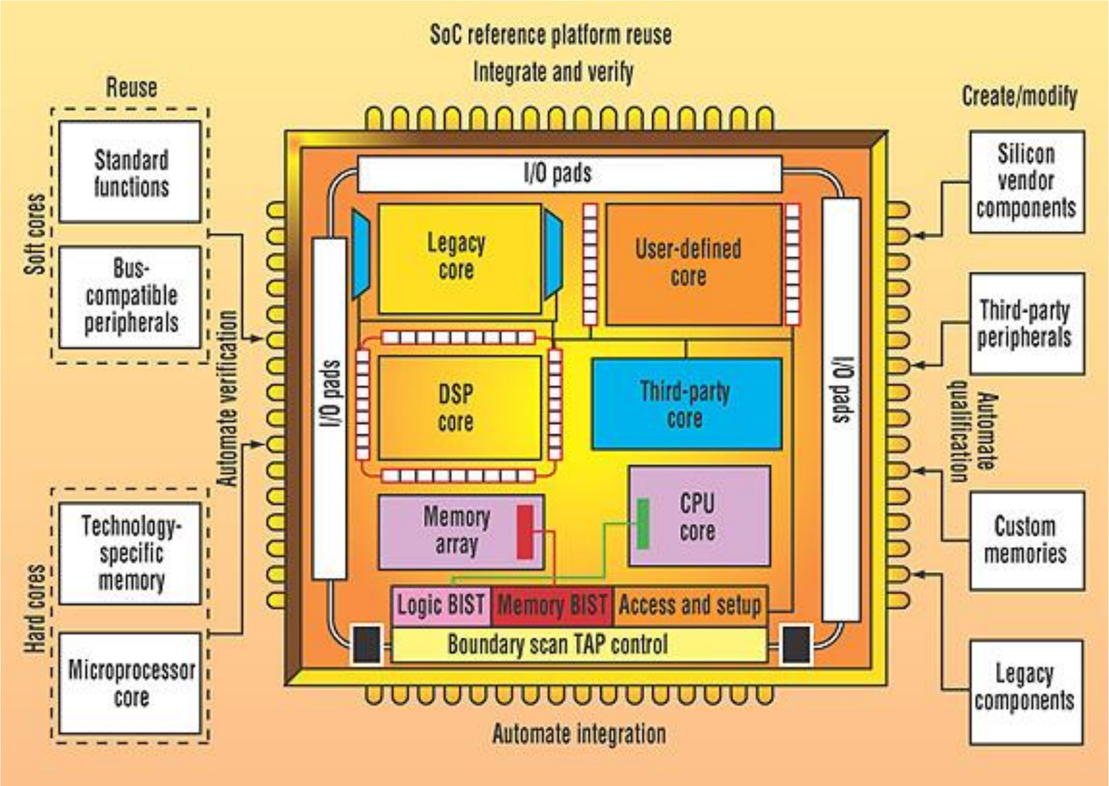

SoC reference platform reuse
Integrate and verify
Reuse
Create/modify
Soft cores
Standard functions
Bus-compatible peripherals
Hard cores
Technology-specific memory
Microprocessor core
Automate verification
I/O pads
Legacy core
User-defined core
DSP core
Third-party core
Memory array
CPU core
Logic BIST
Memory BIST
Access and setup
Boundary scan TAP control
Automate integration
Automate qualification
Silicon vendor components
Third-party peripherals
Custom memories
Legacy components

Figure II.7: Example of a SoC architecture (source: http://electronicdesign.com/).

II.5.2 Chip on Board (CoB)

it refers to the assembly technology in which the chip or die is directly mounted on its final circuit and electrically interconnected to the latter, instead of undergoing traditional assembly as an integrated circuit (IC) individual. Chip on Board (CoB) simplifies the entire design and manufacturing process of the final product and improves its performance due to the short interconnection paths. Figure II.8 shows two views of a memory module CoB product bonded with aluminum wire.

The term generally used for CoB technology is currently Direct Chip Attachment (DCA). Beside from the circuits used for CoB, various substrates are available for use of DCA. For example, ceramic and glass-ceramic substrates which exhibit excellent dielectric and thermal properties. The organic substrates also exist because of its light weight and low cost while offering a low dielectric constant. 60 GHz wireless chipsets was investigated in [31] by using the DCA method.

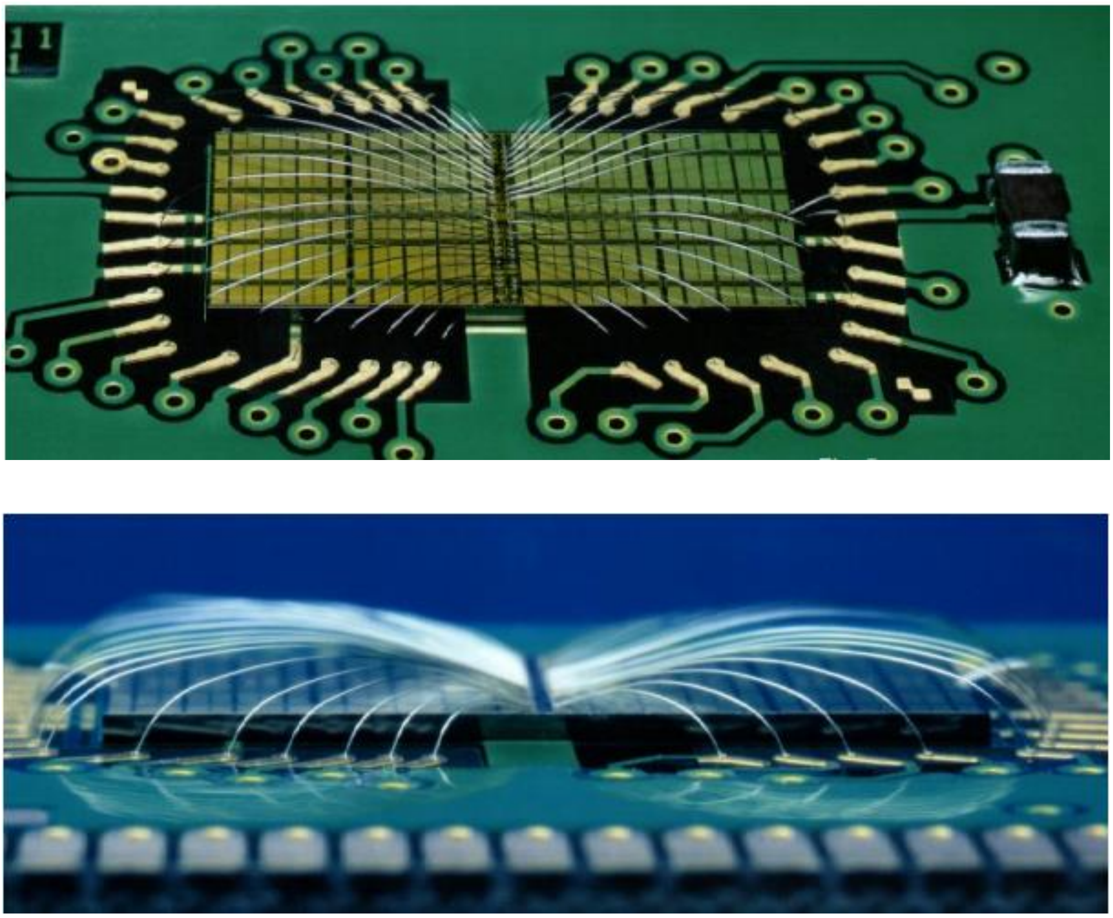


Figure II.8: Two views of a CoB technology memory module (source: MB Electronique).

II.5.3 MCM

A Multi-Chip Module (MCM) is a generally electronic assembly where multi integrated circuits (ICs), semiconductor dies and/or other discrete components are integrated on a single substrate (Figure II.9), which facilitates their use as single component (like a larger IC). The MCM itself is often referred to as a "hybrid IC”, which shows its integrated nature.

The MCMs come in a variety of shapes depending on the complexity and development philosophies of their designers. These can range from using pre-packaged ICs on a small printed circuit board (PCB) meant to mimic the package footprint of an existing chip package, to fully custom chip packages integrating many chip dies on a High-Density Interconnection (HDI) substrate. 60 GHz Antenna Array for Multi-Chip Communication was studied and shown in [31].

Multi-Chip Module packaging is an important facet of modern electronic miniaturization and micro-electronic systems. MCMs are classified according to the technology used to create the HDI (High Density Interconnection) substrate.

- MCM-L – laminated MCM. The substrate is a multi-layer laminated PCB (Printed circuit board).
- MCM-D – deposited MCM. The modules are deposited on the base substrate using thin film technology.
- MCM-C – ceramic substrate MCMs, such as LTCC.

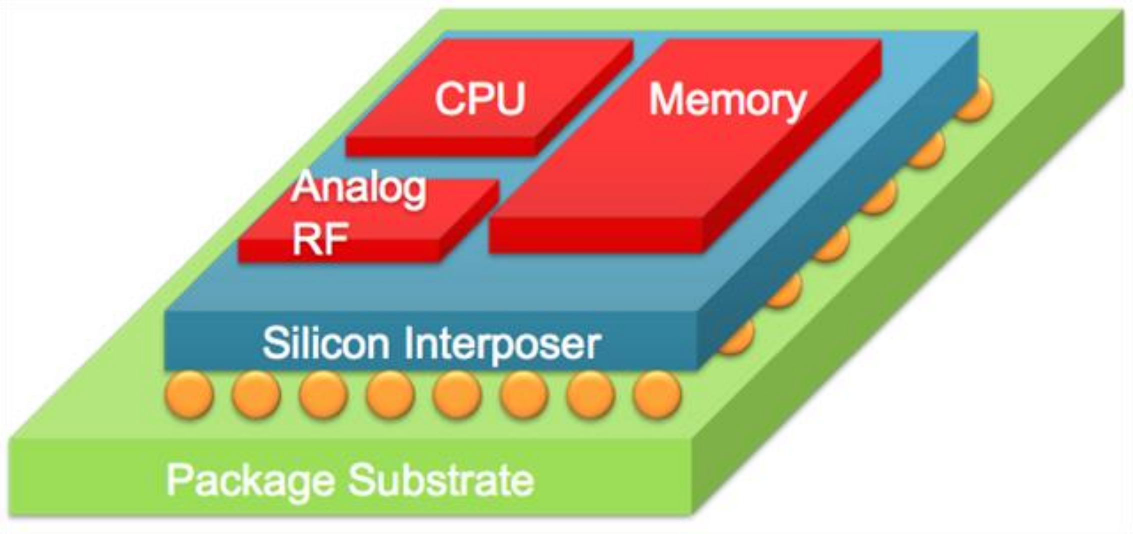


Figure II.9: Example of MCM structure.

II.5.4 System in Package (SiP)

As shown in Figure II.10, the System in Package (SiP) presents generally a vertical integration configuration. In this case, the different functionalities of the system are made via chips with different natures (standard bare silicon chip, microsystems, passive components and RF devices ...) interconnected to each other by stacking. It consists of a stack of electronic slices whose interconnection is made in three dimensions using the faces of the stack to make the connections between slices. A SiP micro-radar at 60 GHz was designed and measured for noncontact vital sign detection[32].

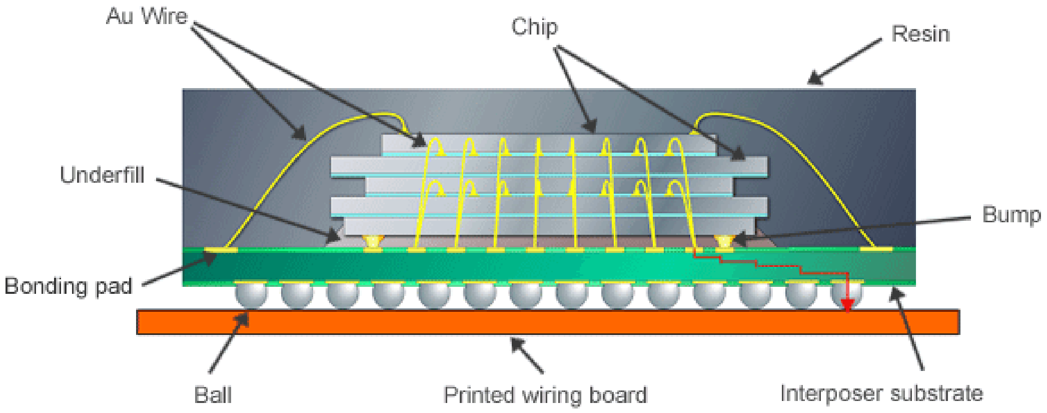

Au Wire
Chip
Resin
Underfill
Bump
Bonding pad
Ball
Printed wiring board
Interposer substrate

Figure II.10: Example of SiP structure (SiP technology of 5 stacked chips), source: renesas.com.

II.5.5 System on Package (SoP)

We can also cite the System on Package (SoP) as a new integration solution. The concept of SoP brings the idea of integrating inside the volume of the substrate, mainly used for electrical interconnections, passive element such as capacity, inductors, filters which are the general functionality of the system. This technique is also a 3D integration. This dimension is formed by the stack of organic substrate layers that have been functionalized beforehand. This technology then groups the previous (SoC, SiP and MCM) and therefore it is much more complete. 60 GHz SoP research activities including the integration and demonstration of a transmitter (Tx)/receiver (Rx) radio were presented in [33].

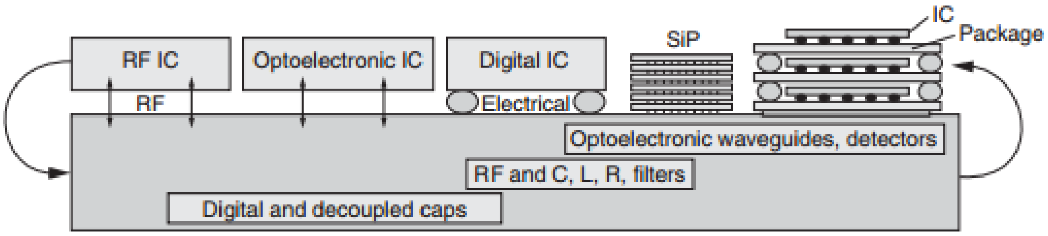

RF IC
RF
Optoelectronic IC
Digital IC
Electrical
SiP
IC
Package
Optoelectronic waveguides, detectors
RF and C, L, R, filters
Digital and decoupled caps

Figure II.11: Example of SoP structure [34].

II.5.6 Package on Package (PoP)

One of the latest innovations is the Package on Package (PoP) which is an assembly process of combining several vertically packaged modules. Two or more modules are stacked one above another, with a standard interface for routing signals between them. This allows to have a higher density of components. The most obvious advantage is saving space on the motherboard. The PoP uses much less board space, almost as little as the SiP. Electrically, PoP offers advantages in minimizing the length of track between different inter-operating parties, such as a controller and a memory. This provides better electrical performance of the devices, the return of interconnections between circuits, the speed of the signal and reducing noise and crosstalk. junction temperatures are lower in compared to those of SiP. The main advantage in terms of PoP returns is that the memory device is decoupled from the logic device and therefore, these two devices can be optimized and tested separately. From the perspective of manufacturing efficiency, only the components tested good are assembled, which is very favorable in terms of manufacturing cost. The Figure II.12 describes an example PoP designed by Shinko[35].

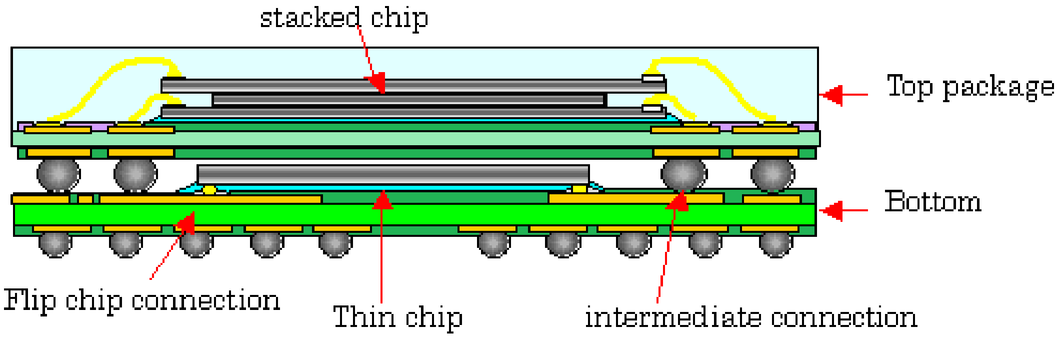


Figure II.12: Example of PoP structure, source: shinko.co.jp.

II.6 Conclusion

In conclusion, inkjet printing is a direct write technology which presents a low-cost advantage because the design pattern is transferred directly to the substrate and does not require masks. However, the liquid metal nanoparticles used for inkjet printing have much lower conductivity compared with the bulk conductor used for lithography [36][24], which can degrade the printed circuit's performances at RF and millimeter wave frequency. In addition, millimeter wave applications require high accuracy, and both screen printing and inkjet printing can only offer a highest resolution about 20 µm [37]. Antennas fabricated on Kapton at lower frequency have been reported in [38][39] using screen printing or inkjet printing, but the traditional photolithography remains the most suitable method for the microfabrication at millimeter frequency range.

The evolution of electronic packaging followed two major trends that are intertwined: the "More Moore" and the "More than Moore". The first trend is to miniaturize the components and the second is to diversify their duties. Combining the two trends allows the emergence of new innovations such as: SoC, the CoB, MCM, which are horizontal integrations and SiP, PoP and the SoP which are vertical or 3D integration.

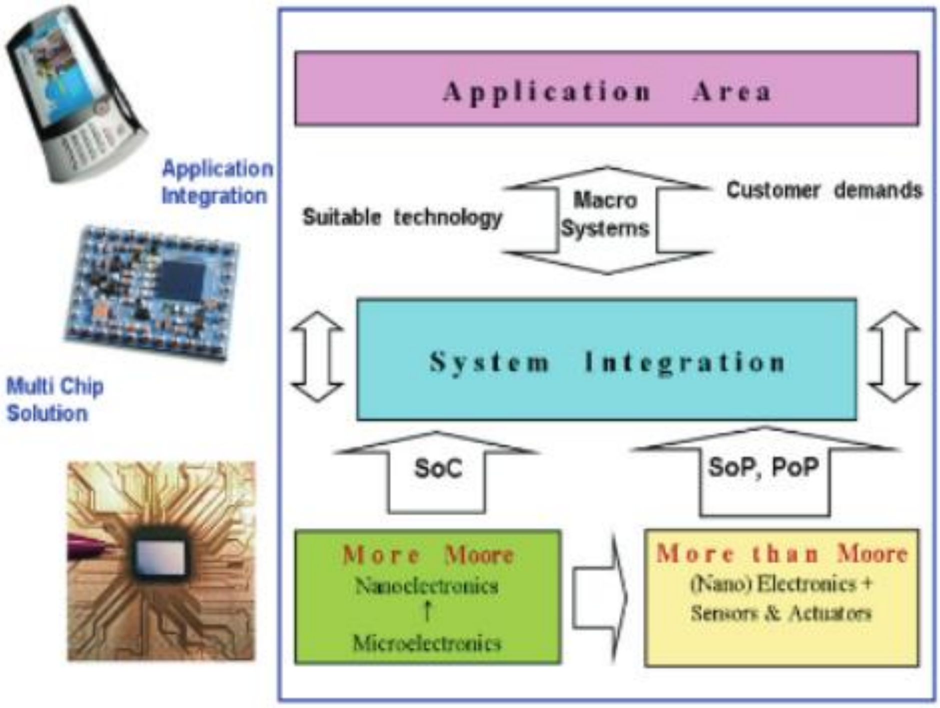

Application Integration
Multi Chip Solution
Application Area
Suitable technology
Macro Systems
Customer demands
System Integration
SoC
SoP, PoP
More Moore
Nanoelectronics
Microelectronics
More than Moore
(Nano) Electronics +
Sensors & Actuators

Figure II.13: Roadmap of system integration. [29].

III. Design and measurement of passive circuit elements on flexible substrate

III.1 Theoretical background

III.1.1 Reflection coefficient

Microwave measurements are usually made with a length of transmission line between the observation point and the terminals of the device under test (DUT) as shown in Figure III.1.

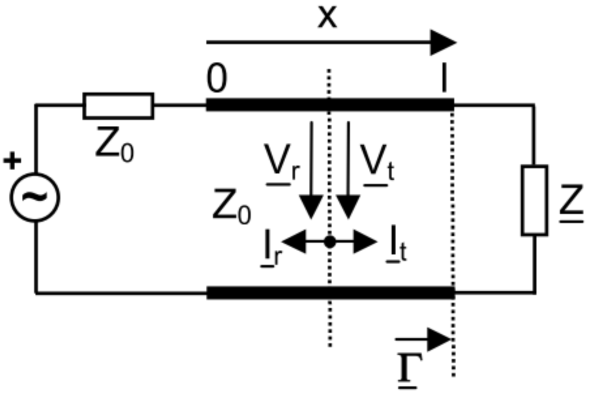


Figure III.1: Transmitted and reflected currents and voltages.

At a location x, the voltage the current on the line are [40] :

$$\underline{V}(x) = \underline{V}_t + \underline{V}_r \qquad \text{III.1}$$

$$\underline{I}(x) = \underline{I}_t - \underline{I}_r \qquad \text{III.2}$$

At the terminal x = l, the following equation must be satisfied:

$$\begin{aligned}\underline{Z} = \frac{\underline{V}(l)}{\underline{I}(l)} = \frac{\underline{V}_t + \underline{V}_r}{\underline{I}_t - \underline{I}_r} = \frac{\underline{V}_t + \underline{V}_r}{(\underline{V}_t - \underline{V}_r)/Z_0} = Z_0 \frac{1 + \underline{V}_r/\underline{V}_t}{1 - \underline{V}_r/\underline{V}_t} \\ = Z_0 \frac{1 + \underline{\Gamma}}{1 - \underline{\Gamma}}\end{aligned} \qquad \text{III.3}$$

The ratio of the reflected voltage amplitude to that of the transmitted voltage amplitude is the reflection coefficient which is given by:

$$\underline{\Gamma} = \frac{\underline{V}_r}{\underline{V}_t} = \frac{\underline{I}_r}{\underline{I}_t} \qquad \text{III.4}$$

$$\underline{\Gamma} = \frac{\underline{Z} - Z_0}{\underline{Z} + Z_0} \qquad \text{III.5}$$

When $\underline{Z} = Z_0$, $\underline{\Gamma}$ equals 0, the maximum power is transferred to the load, and in the case of $\underline{Z} = 0$ or $\underline{Z} = \infty$, $\underline{\Gamma}$ equals -1 and 1 respectively, the power is totally reflected to the source.

III.1.2 Fundamental parameters of antenna

a) Gain and efficiency

Gain of an antenna (in a given direction) is defined as the ratio of the intensity, in the direction of peak radiation, to the radiation intensity that would be obtained If the power accepted by an isotropic antenna. Antenna gain is more commonly used than directivity in antenna’s specification sheet because it takes into account the actual losses that occur.

Antenna gain (G) can be related to directivity (D) and antenna efficiency (η) by:

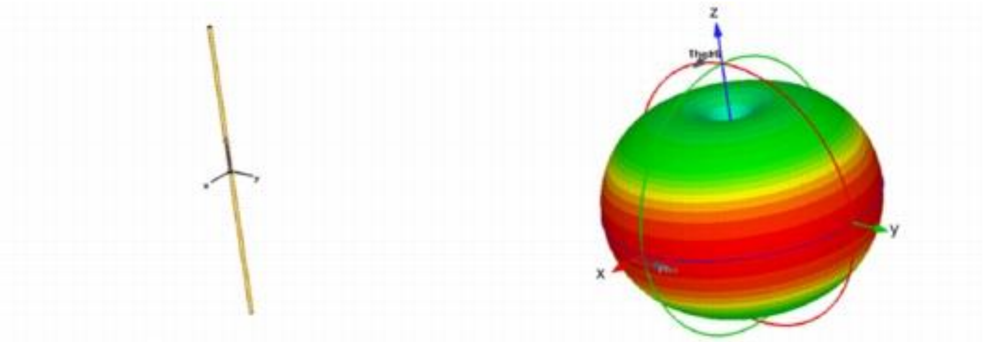
$$G = \eta . D \qquad \text{III.6}$$

If the antenna is lossless, than its gain and directivity is equal. So all the power delivered to the antenna can be radiate. In the real case, a high efficiency antenna has most of power present at the antenna’s input radiated away, a low efficiency antenna has most of the power absorbed as losses within the antenna, or reflected away due to impedance mismatch. So the efficiency of an antenna can be written as follows:

$$\eta = \frac{P_{\text{radiated}}}{P_{\text{input}}} \qquad \text{III.7}$$

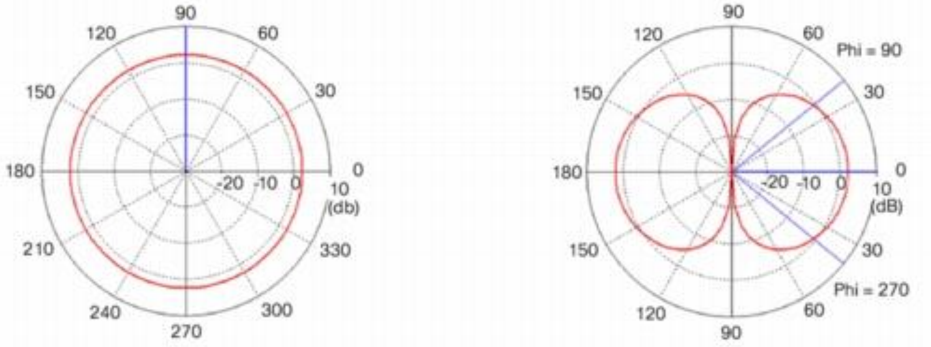
b) Radiation pattern

An antenna radiation pattern or antenna pattern defines the variation of the power radiated by the antenna as a function of the directional coordinates. Usually, they are observed in the far field.



(a) Dipole Antenna Model

(b) Dipole 3D Radiation Pattern



(c) Dipole Azimuth Plane Pattern

(d) Dipole Elevation Plane Pattern

Figure III.2: Dipole Antenna with 3D Radiation Pattern, Azimuth Plane Pattern and Elevation Plane Pattern, source Cisco.

Figure III.2 shows an example of a donut shaped radiation pattern for a dipole antenna. In this case, along the z-axis, which would correspond to the radiation directly overhead the antenna, there is very little power transmitted. In the x-y plane (perpendicular to the z-axis), the radiation is maximum. These plots are useful for visualizing which directions the antenna radiates.

III.1 Technological process for flexible substrate

To manufacture our circuits onto a flexible substrate, we have chosen the traditional photolithography, the main difficulty during the fabrication process lies on the flexible film handling and its use in micro-technology equipment. In order to overcome this difficulty, a 4-inch silicon wafer is used as a host carrier. One of the critical obstacles consists in finding a way to adhere the polyimide film on the Si support. This adhesion has to be compatible with the various technological stages (vacuum, solvent and temperature) and allows after manufacture a peeling without any physical or chemical constraint.

A matured fabrication process [41] is used where first a PDMS (PolyDiMethylSiloxane) spin coating is performed for the adhesion of the polyimide on the holding wafer. Then the Kapton polyimide is patterned on the PDMS-Si support using a Shipley 360N laminator (see Figure III.3). A resin spin coating is then realized in a fully automated resist processing tool EVG120 (see Figure III.4), followed by a photolithography process.

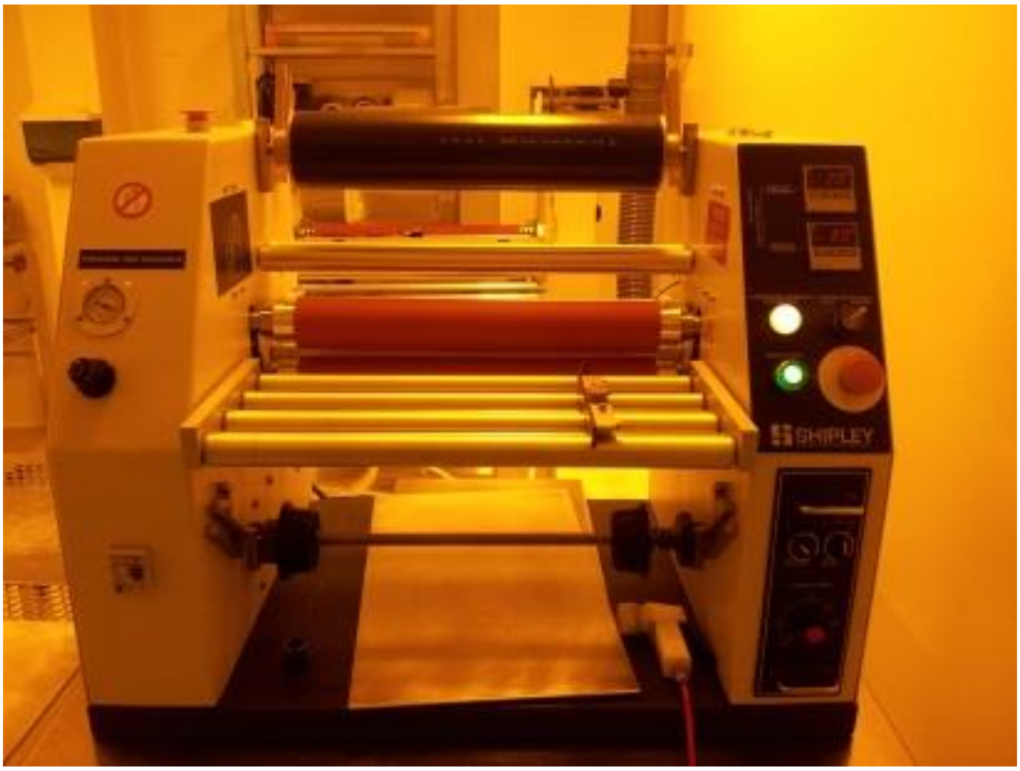


Figure III.3: Shipley 360N Laminator.

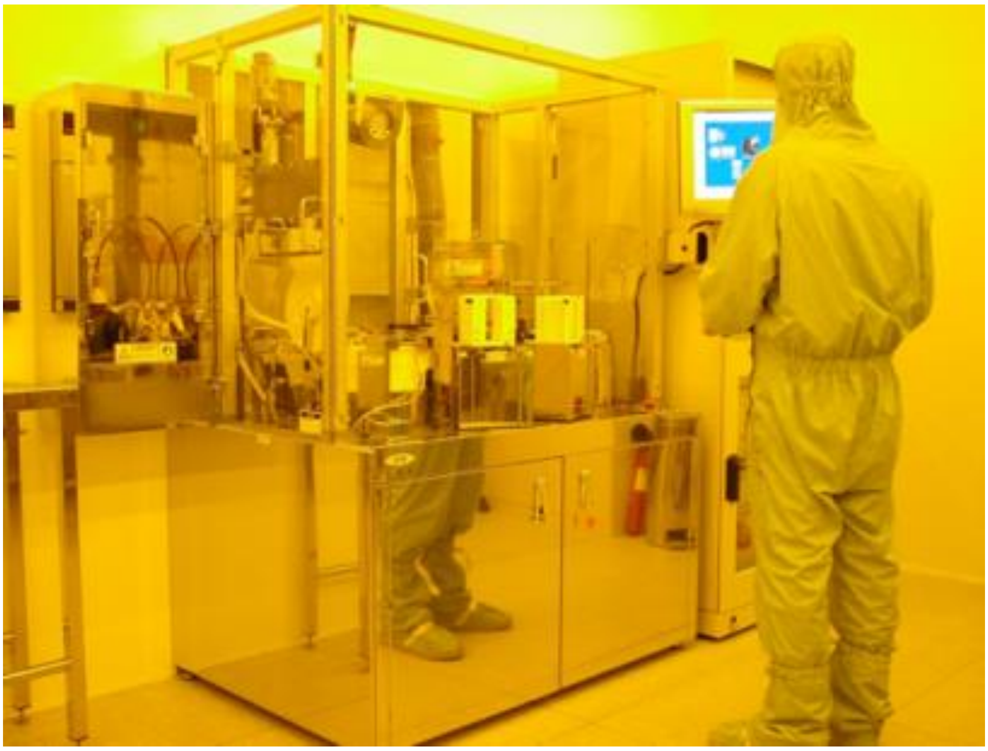


Figure III.4: EVG120 resist processing system.

During the different fabrication processes, Kapton polyimide is metallized with Ti/Au layers (50 nm/ 200 nm) or Ti/Cu layers (50 nm/500 nm) using the Electron Beam Physical Vapor Deposition (EBPVD). In case of Cu coating, the fabrication process will be terminated with a surface finishing (gold immersion deposits) to prevent Cu from oxidizing. Both wet-etching and lift-off methods were carried out during different tests, each of them is able to obtain a sufficient resolution for the metallization tracks.

The skin depths of gold and copper at microwave frequencies are given in Figure III.5. One can see the skin depth decrease with higher frequency. So with the metal thickness mentioned above, selected mainly for V-band applications, high losses at lower frequencies should be expected.

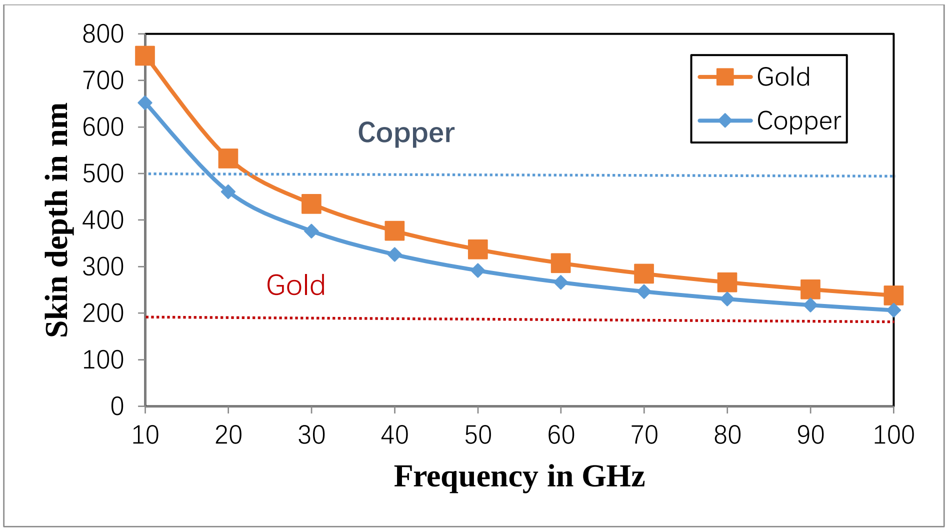


Figure III.5: Skin depth versus frequency, the horizontal lines show the selected metallization thickness.

III.2 RF characterization of Kapton

A commercially 127-µm Kapton (type 500HN) was chosen for our flexible substrate as discussed previously, which is the thickest product available in the HN series. In fact there is a minimum substrate thickness that must be respected for designing an effective patch antenna in V-band. As shown in Figure III.6, this type antenna is composed by a rectangular patch on the top side of the substrate and a ground plane on the back side. In order to avoid undesired capacitive effect and to ensure a highly-efficient radiation mechanism of a patch antenna, a quick parametric study is done. It shows the influence of substrate thickness versus maximum antenna gain in HFSS simulation (Figure III.7). One can see that the thicker the substrate, the better the antenna gain, regardless its metallization layer: Perfect Electric Conductor (PEC), copper or gold.

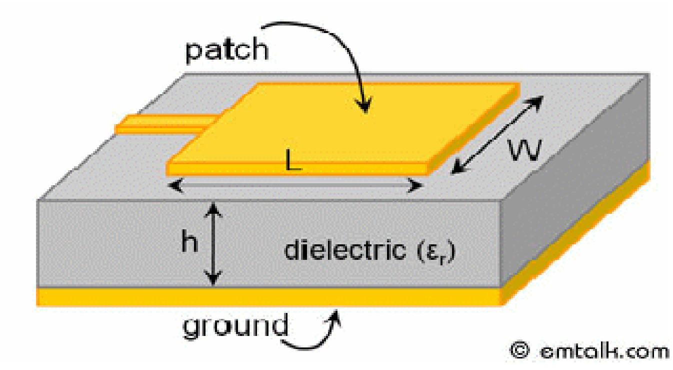


Figure III.6: Microstrip Patch Antenna, source emtalk.com.

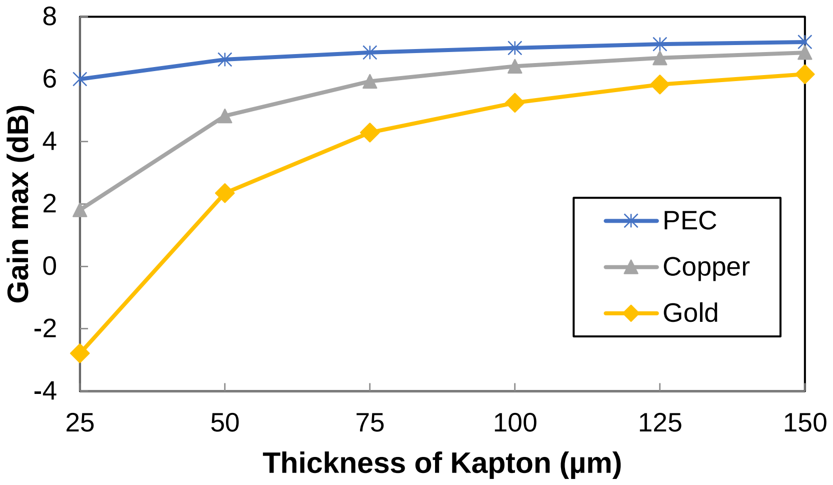


Figure III.7: Maximum simulated antenna gain versus substrate thickness at 60 GHz.

III.2.1 Ring resonator

To design properly any high-frequency structure on this 127-µm Kapton by using numerical simulation, the knowledge of dielectric properties of substrate becomes necessary. The dielectric properties of Kapton: the relative permittivity ε_r and the loss tangent tan δ were extracted from S-parameters measurement of a ring resonator as illustrated in Figure III.8 [42].

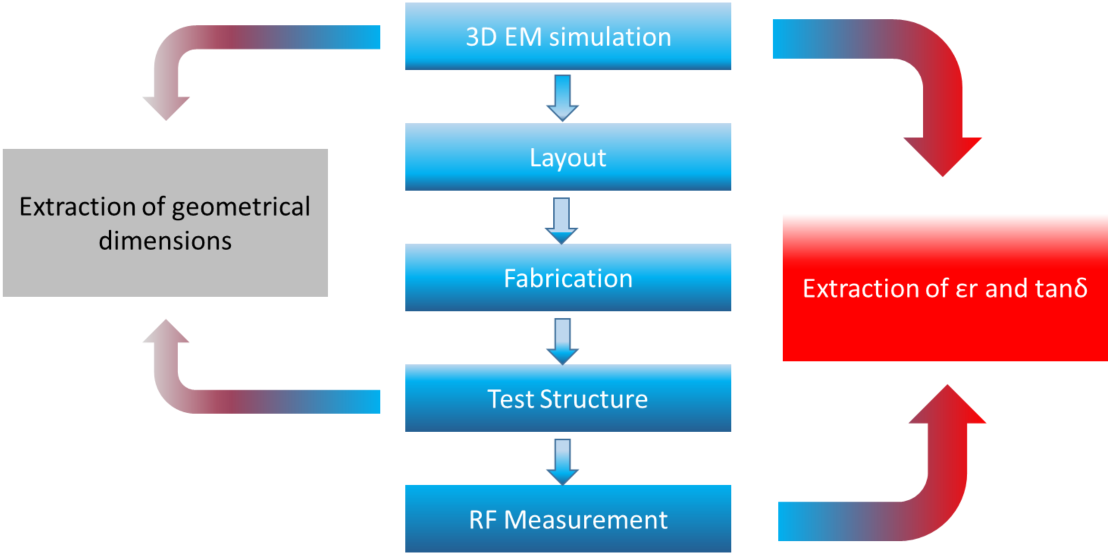

3D EM simulation
Layout
Fabrication
Test Structure
RF Measurement
Extraction of geometrical dimensions
Extraction of εr and tanδ

Figure III.8: Procedure for extraction of dielectric parameters.

This resonator is composed by a ring with mean radius of 2.95 mm. The width of the microstrip on the Kapton surface is 310 µm to give us a characteristic impedance in the range of 50 Ω. Additionally, a grounded coplanar waveguide (GCPW) to microstrip transition was optimized with the help of HFSS electromagnetic (EM) software to minimize the impedance mismatch. There are two 70 µm gaps at the edges of the ring to couple the resonator with the measurement system, which provides us sufficient coupling to measure the resonator without overload the test equipment (see Figure III.9).

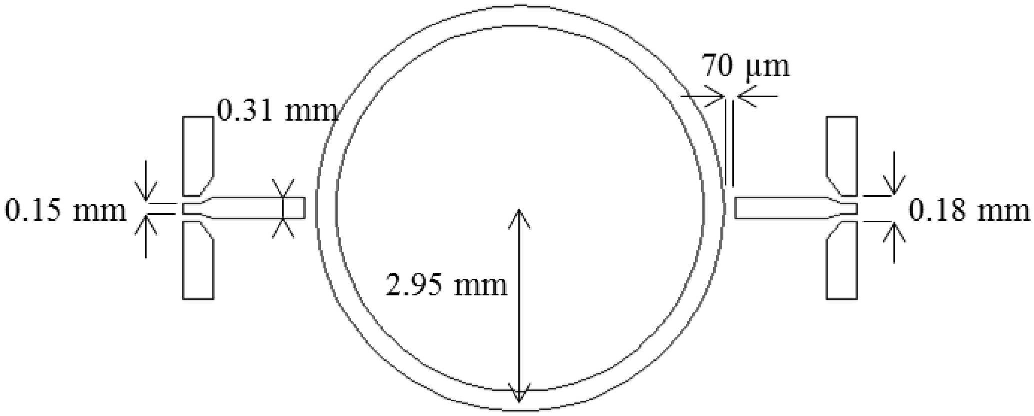


Figure III.9: Ring resonator design.

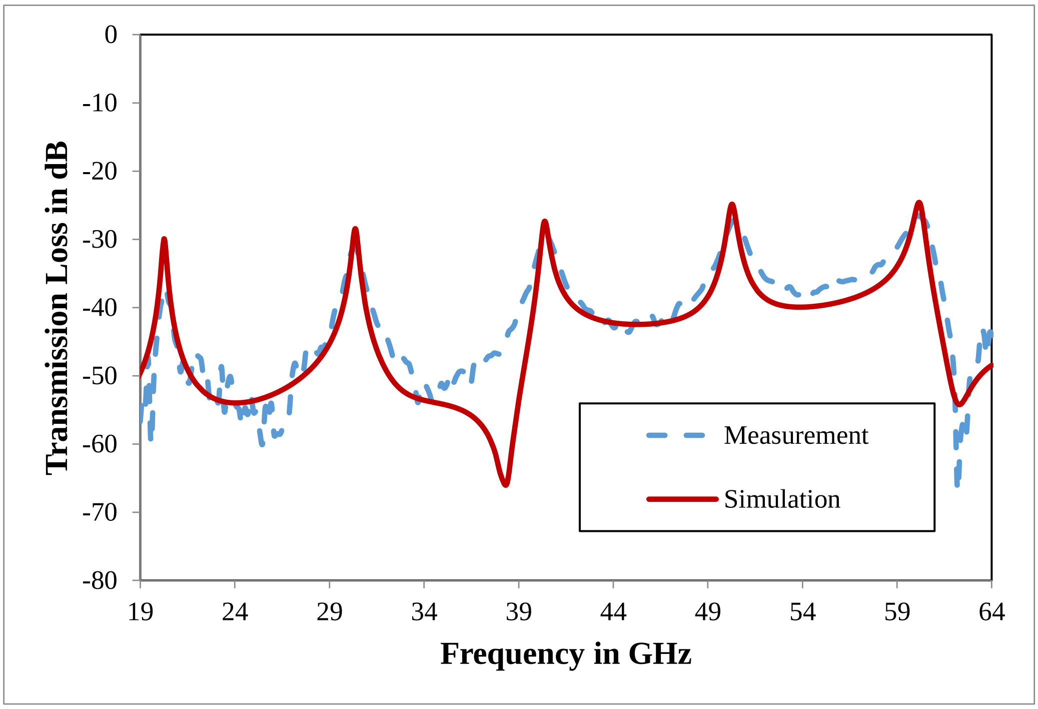


Fig. III.10: Simulated and measured insertion loss of the ring resonator.

The same structures were also modeled using ADS Momentum software. In order to fit measured and simulated data for the entire frequency band, we tuned the dielectric parameters. It is clear that the full 3D Finit Element Method (FEM) used in HFSS software is more accurate than the Method of Moments (MoM) used in ADS Momentum, but in our case, a simulation from 10 to 65 GHz with ADS Momentum is much faster. The correlation between experimental and simulation results is depicted in Fig. III.10. Simulated and measured resonant frequencies and quality factors are given in Table III.1. The experimental results were obtained by using an Agilent PNA network analyzer and Cascade Microtech GSG probe with a 150 µm pitch. A 2-port on-wafer SOLT calibration method was used. The dielectric properties found for this Kapton polyimide are $\varepsilon_r = 3.2 \pm 0.03$ and $\tan\delta = 0.012 \pm 0.004$ within the entire frequency band.

Table III.1: Resonant frequencies & quality factors.

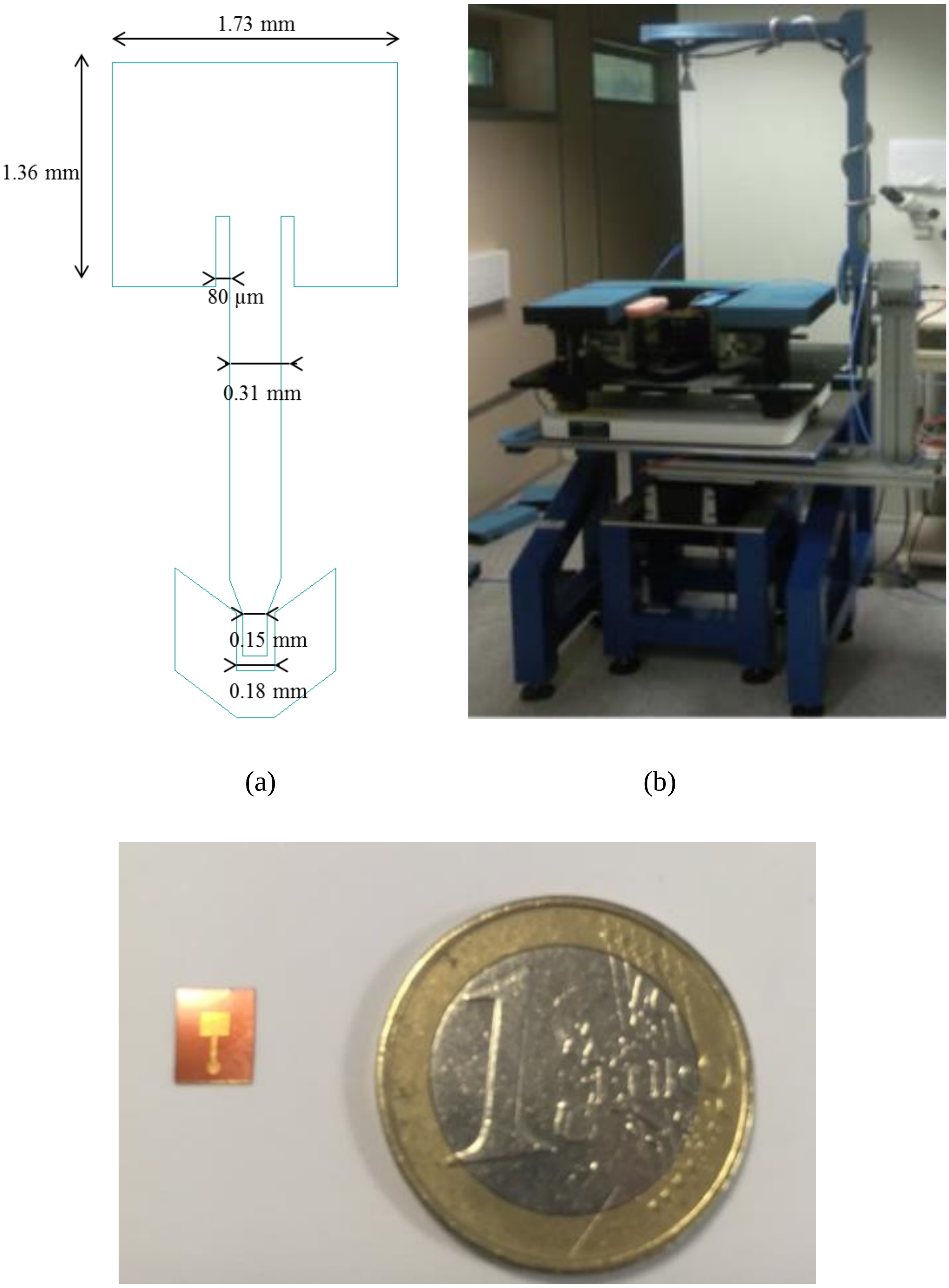
Simulation		**Measurement**	
Resonant Frequency	Q factor	Resonant Frequency	Q factor
20.27	72.4	20.345	36.7
30.36	89.3	30.265	39.1
40.37	98.5	40.34	42
50.28	104.7	50.415	44.4
60.17	114.6	60.18	50.2

III.3 Antennas

A high gain antenna at 60 GHz is required to enable an ultra-low power consumption radio interface, and this antenna must also have a relative large bandwidth (500 MHz to 2 GHz) to ensure the Ultra-Wide Band Impulse Radio (UWB-IR) communications.

III.3.1 Patch antenna

A 60 GHz grounded coplanar waveguide (GCPW) feeding rectangular patch antenna (see Figure III.11 a) was designed, fabricated, and measured on a flexible 127-µm-thick polyimide substrate (Kapton). The GCPW-to-microstrip transition was optimized to reduce the impedance mismatch. The antenna was then characterized in terms of return loss, gain, and radiation pattern.


1.73 mm
1.36 mm
80 µm
0.31 mm
0.15 mm
0.18 mm

(a) (b)

(c)

Figure III.11: (a) 60GHz GCPW feeding rectangular patch antenna; (b) Measurement setup; (c) Manufactured patch antenna on Kapton.

The simulated and the measured return loss of the patch antenna versus frequency are presented in Figure III.12. The agreement between experiments and simulations is very good: a relative frequency shift of only 0.7% is observed between the simulated (HFSS) and measured results. The difference is due to the uncertainties of the substrate permittivity/permeability value and under/over etching of the conductive patterns. The measured impedance bandwidth, defined by return loss less than -10 dB, is from 60.05 GHz to 61.8 GHz (3% of relative bandwidth).

The far-field radiation pattern and gain measurement were performed with a probe based antenna measurement setup at LAAS (Figure III.11 b). The antenna is fed through a 150-µm Ground-Signal-Ground (GSG) probe, and this probe is directly connected to a 65 GHz VNA (Anritsu 37397D) with a flexible V-cable. Dielectric foam from Rohacell was used below the antenna to prevent reflections from the metallic part of the setup. The Antenna Under Test (AUT) was illumined by the field generated by a calibrated VT-15-25-C horn antenna from Vector Telecom.

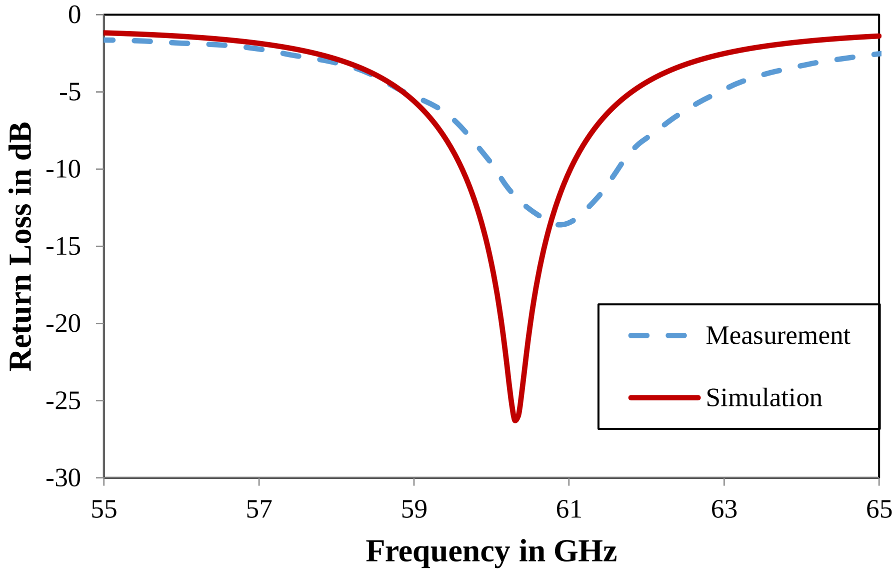


Figure III.12: Simulated and measured return loss of the patch antenna.

Under these conditions, a maximum gain of 5 dBi was measured in the perpendicular direction of the antenna at 60.3 GHz. The simulated and measured radiation patterns in the H- and E-plane are given in Figure III.13 and Fig. III.14. The difference of gain between simulation and measurement is about 1.7 dB, which may due to insertion loss introduced by the CPW probe and the metallization quality of conductive tracks. The E-plane radiation pattern has a restricted range due to architecture of the measurement setup because the probe was placed in the E-plane. Ripples observed in the E-plane are due to reflection and diffraction effects on the metallic micro-positioner and the probe. The 3-dB beamwidth is 56° for the H-plane.

The results demonstrate the quality of fabrication on flexible polyimide substrate and the accuracy of measurement setup for millimeter-wave antenna.

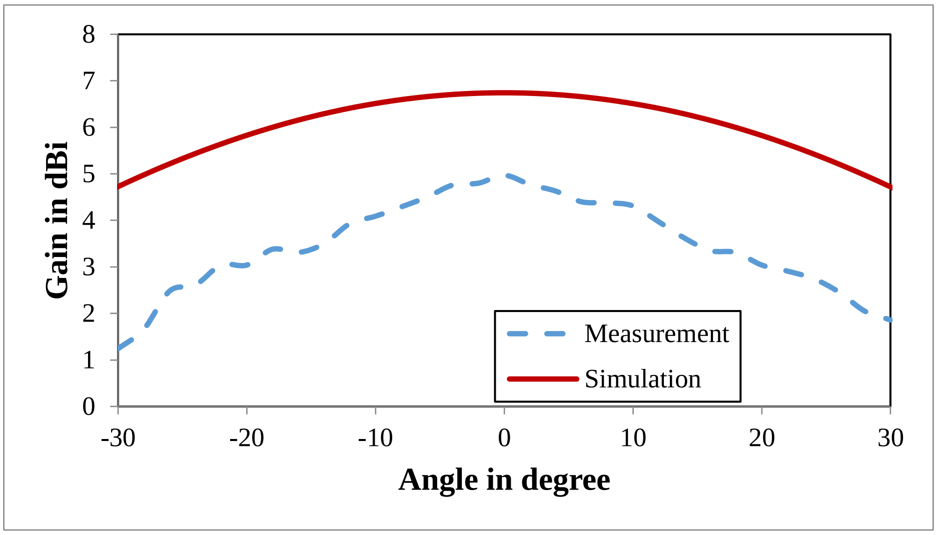


Figure III.13: H-plane radiation patterns of the patch antenna at 60.3 GHz.

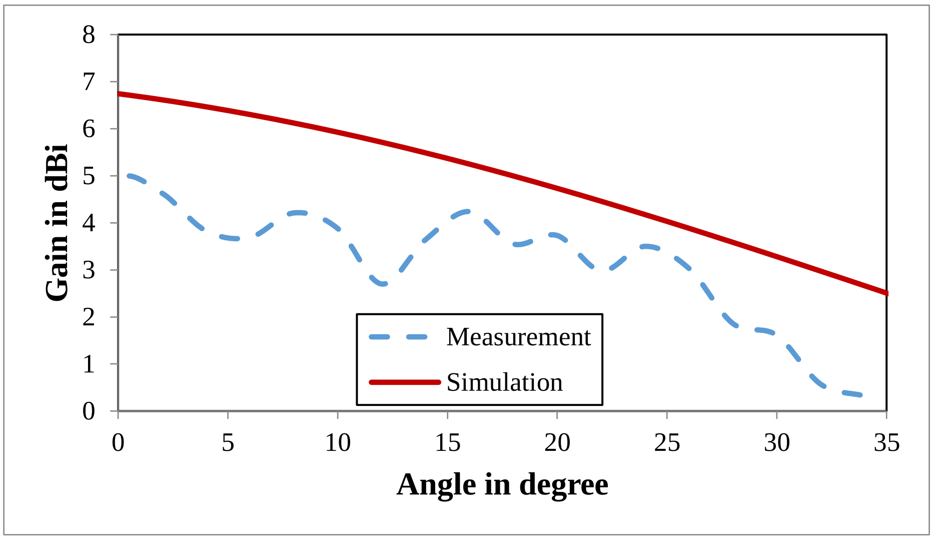


Fig. III.14: E-plane radiation patterns of the patch antenna at 60.3 GHz.

III.3.2 Crossed-dipoles array antenna

For the interest of energy harvesting for satellite health monitoring, the cross dipoles array antenna (CDAA) on Kapton polyimide is proposed, which consists of four printed half-wave dipoles arrays on the top side of substrate. As shown in Fig. III.25 to Figure III.17, CDAA is a coplanar stripline (CPS) structure. A T-junction CPS-to-microstrip was designed and optimized by using intensive electromagnetic simulations to allow the excitation of the CDAA by a microstrip and the proper connection with a K "end launch" connector from Southwest for measurement purposes [43].

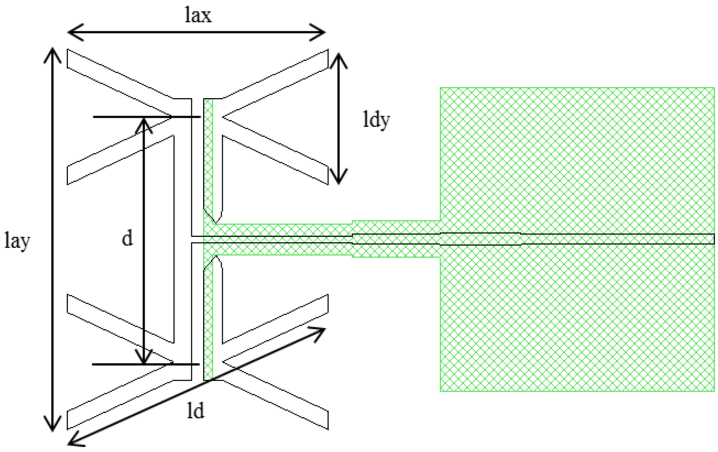


Figure III.15: Cross dipoles array antenna: top view of the layout (the bottom layout is represented in filled with green trellis.

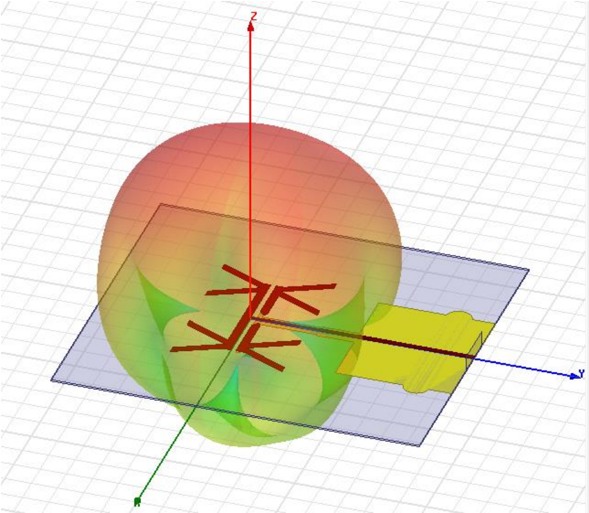


Figure III.16: Simulation model of Cross dipoles array antenna.

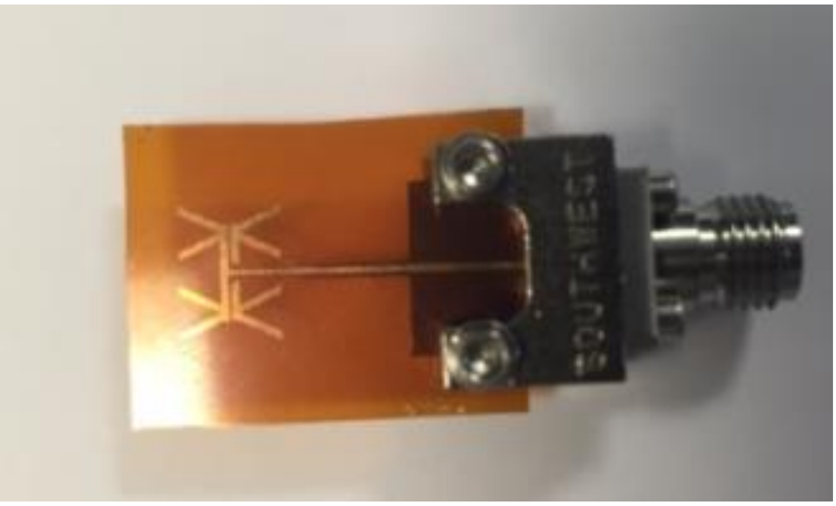


Figure III.17: Manufactured Cross dipoles array antenna.

Table III.2: Cross dipoles array antenna dimensions.

Band	lax (mm)	lay (mm)	d (mm)	Ld (mm)	Ldy (mm)
Ku	8.5	12.42	8	93.18	4.42
K	5.7	7.5	4.5	6.26	3

Two CDAAs operating in Ku and K band are fabricated and measured respectively, their dimensions are summarized in Table III.2. S-parameter measurement and simulation results are reported in Figure III.18 and Fig. III.19. One can see a large impedance bandwidth is obtained (measured at S11 = -10 dB) for two proposed antennas, 15.45 GHz to 19.35GHz for the Ku band CDAA (22% of relative bandwidth), and 21.7GHz to 25.7GHz for the K band CDAA (17% of relative bandwidth).

The radiation pattern characterizations were performed in an anechoic chamber. Fig. III.20 and Fig. III.21 report the measured and simulated radiation patterns in two orthogonal planes at 17 GHz for the Ku band CDAA. Fig. III.22 and Fig. III.23 report the measured and simulated radiation patterns at 22 GHz for the K band CDAA. We note that the simulation results were obtained in HFSS and the “end-launch” connector was not included in the model. The difference of gain between measurement and simulation is about 2.7 dB may due to (i) the losses introduced by the “end-launch” connector (estimated to be in the range of 1 dB); (ii) the assembling mechanical process for connecting the Kapton structure to the connector that can lead to an imperfect contact; (iii) the skin effect. Metallization layers are composed by: (a) adherent layer of Ti about 50 nm; (b) cooper layer (thickness: 500 nm); (c) gold layer (thickness: a few nanometers). As mentioned in section II, the skin depth of copper at 20 GHz is 460 nm which is comparable with the total metal thickness of 600 nm, thus unexpected RF losses may occur. The ripples observed in the YOZ plane (phi = 90°) are due to reflection and diffraction effects on the connector and the coaxial cable. The 3dB beamwidth is 52° in the XOZ plane and 65° in the YOZ plane for the Ku band CDAA at 17 GHz. For the K band CDAA, The 3dB beamwidth is 58° in the XOZ plane and 62° in the YOZ plane at 22 GHz. As depicted from Figure III.18 to Fig. III.22, the proposed CDAAs are wideband antennas (22% of relative bandwidth in Ku band and 17% of relative bandwidth in K band). The radiation pattern does not change significantly in the relative bandwidth and the measured maximum gain is about 4.3 dBi (included the losses added by the end lunch connector and the associated mounting process and by CPS-to-microstrip T junction). We note that the gain can be increased by 3dB if a metallic plate acting as reflector is properly putted below the CDAA.

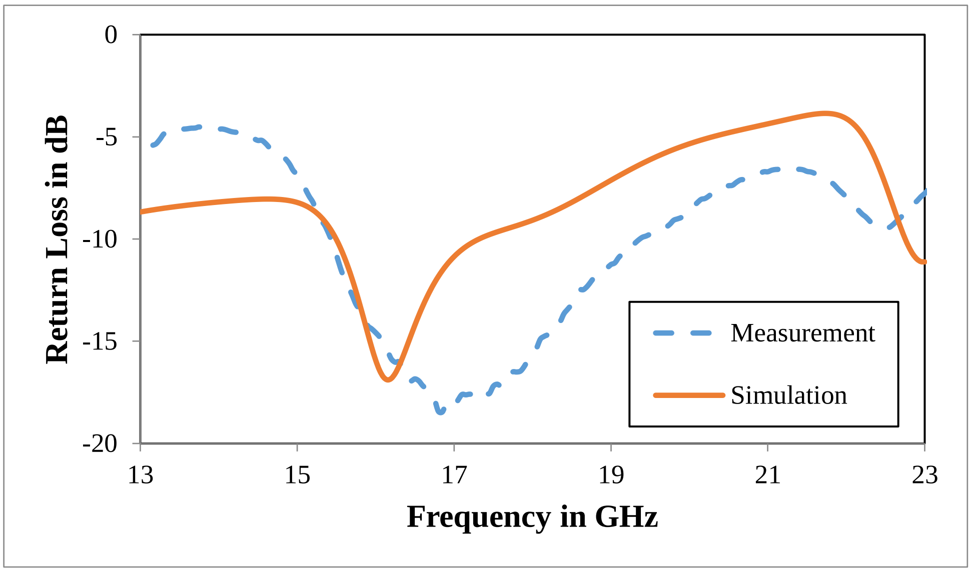


Figure III.18: Simulated and measured return loss of the Ku band CDAA.

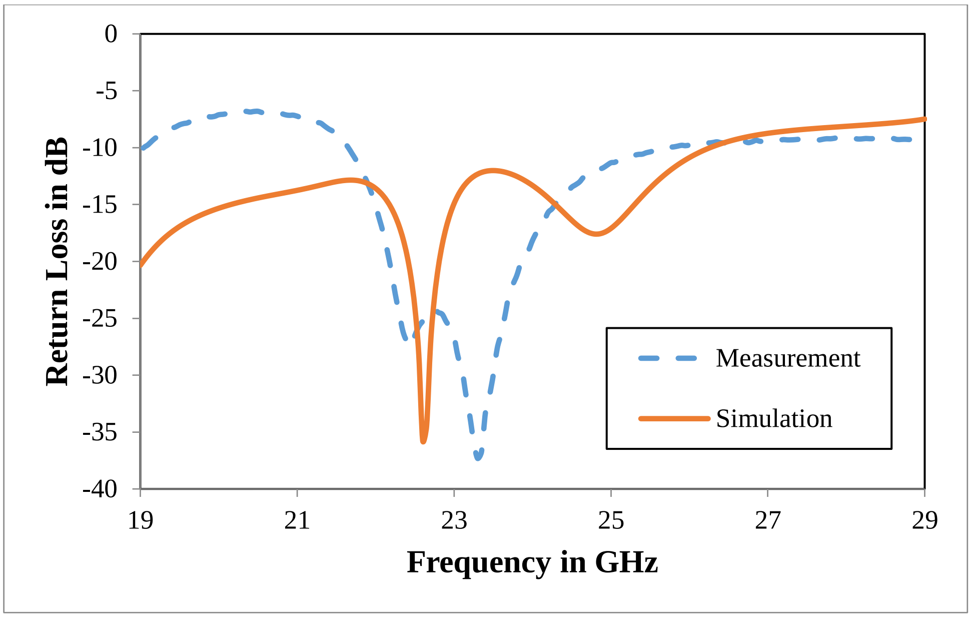


Fig. III.19: Simulated and measured return loss of the K band CDAA.

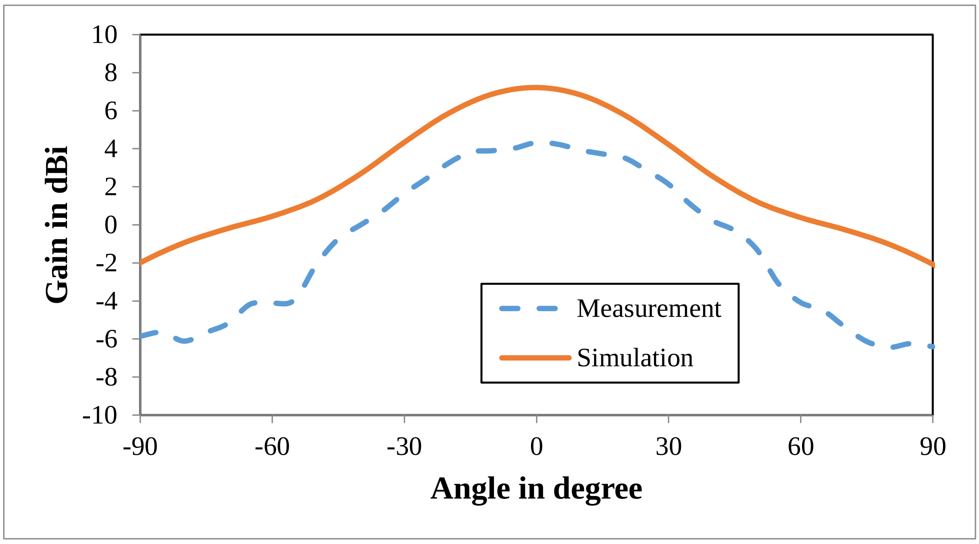


Fig. III.20: XOZ plane (phi = 0°) radiation patterns of the K_u band CDAA at 17 GHz.

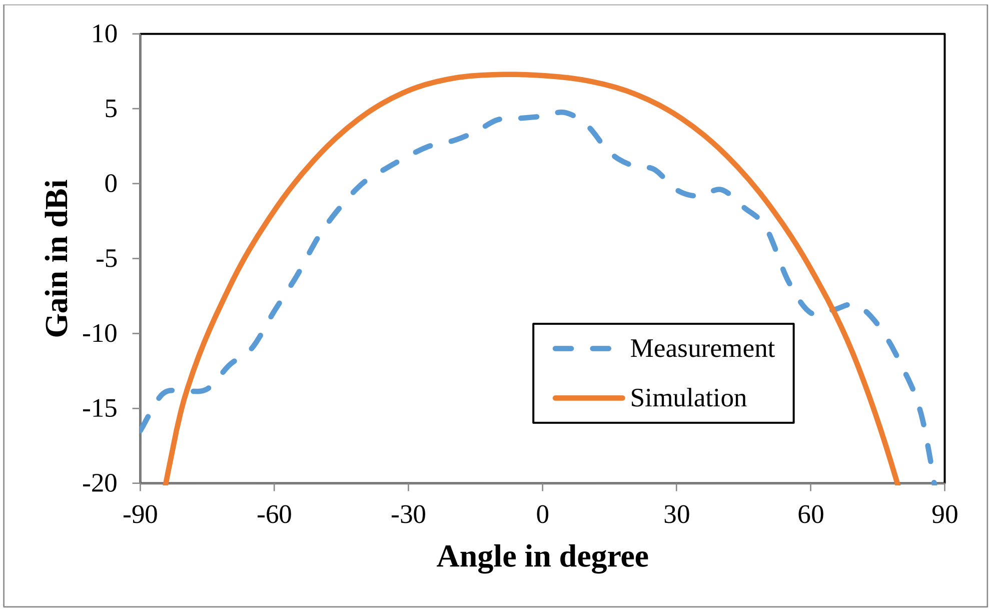


Fig. III.21: YOZ plane (phi = 90°) radiation patterns of the K_u band CDAA at 17 GHz.

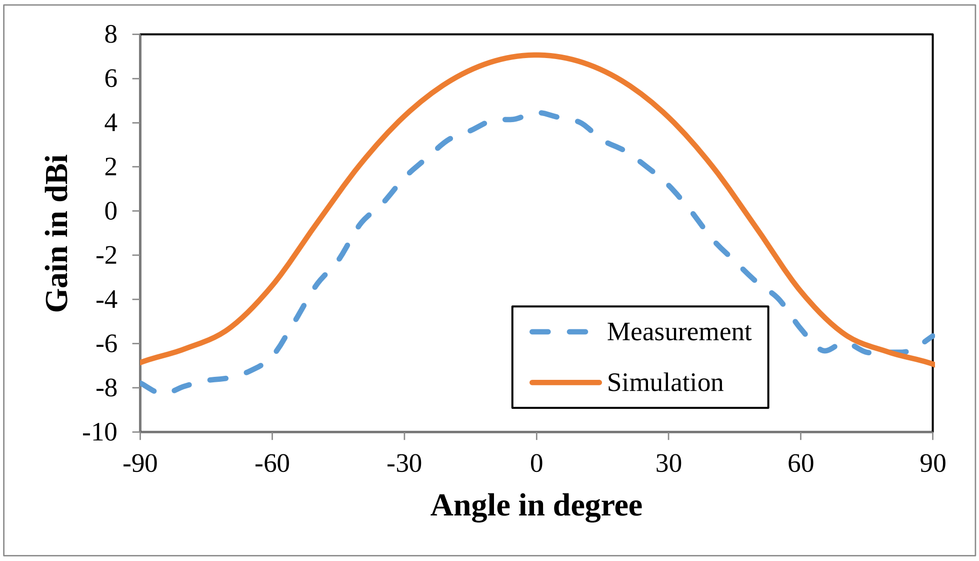


Fig. III.22: XOZ plane (phi = 0°) radiation patterns of the K band CDAA at 22 GHz.

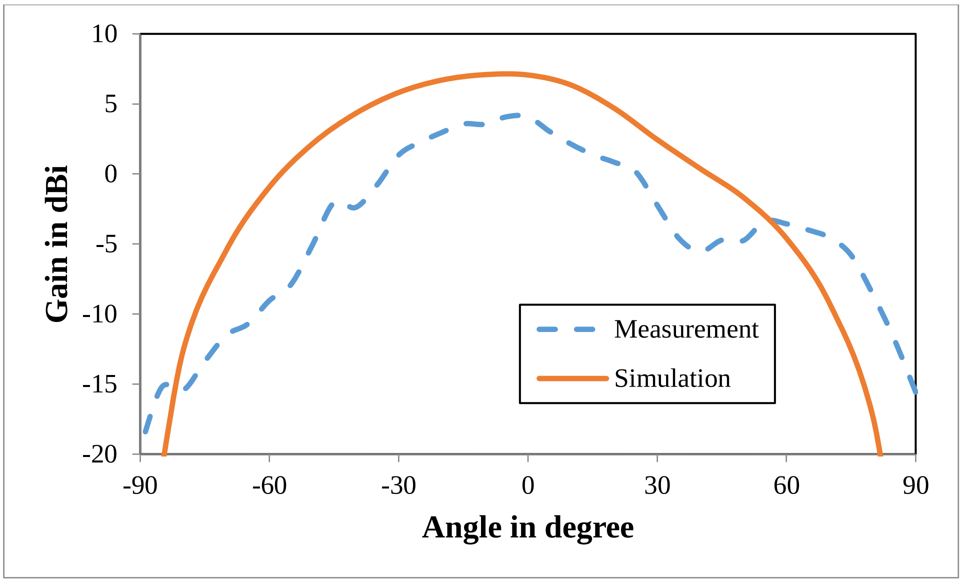


Fig. III.23: YOZ plane (phi = 90°) radiation patterns of the K band CDAA at 22 GHz.

III.3.3 Cross slot dipole antenna

Inspired by the design of CDAAs at Ku band and K band, and the Babinet's principle which relates the radiated field and impedance of a slot antenna to a printed (strip) antenna, a first prototype of Crossed Slot Dipole Antenna (CSDA) in V band is proposed shown in Fig. III.24 and Fig. III.25. The antenna is designed on a 127-µm thick Kapton with a dielectric constant 3.2 and a loss tangent 0.006. CPW feed dimensions of S = 170 µm and G = 12 µm were selected corresponding to the 50 Ohm GSG probe. The slot length L is fixed to 1.3 mm (quarter wavelength for 60 GHz) for the simulation, the slot width w, the stub length d and the angle between slots α were set to 40 µm, 0.69 mm and 45° as default respectively.

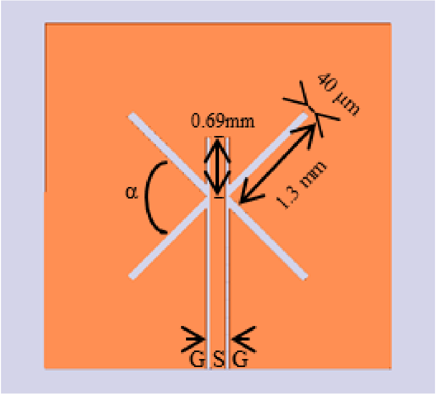


Fig. III.24: Design of crossed slot dipole antenna.

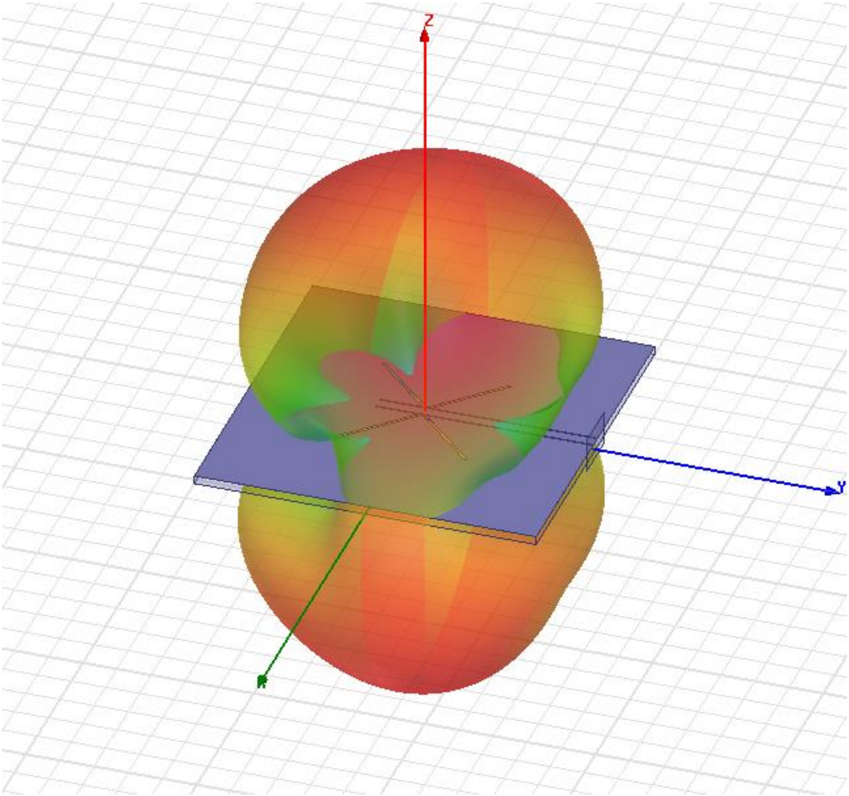


Fig. III.25: Simulation model of slot dipole antenna.

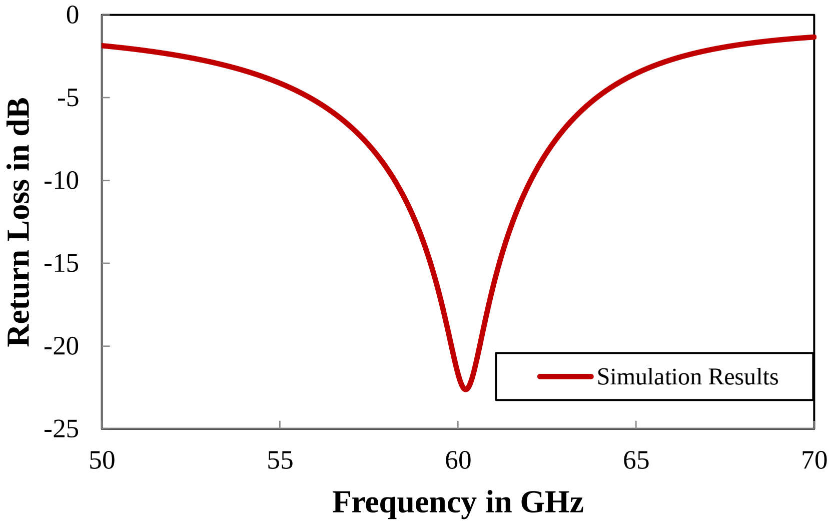


Fig. III.26: Simulated return loss of the cross slot dipole antenna.

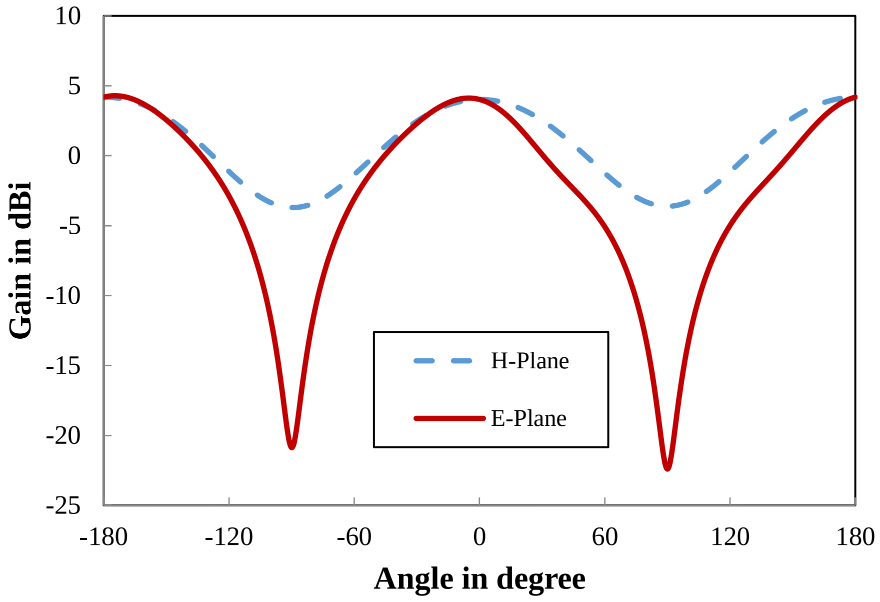


Fig. III.27: Simulated (HFSS) radiation patterns in E-Plane and H-Plane at 60.2 GHz.

Fig. III.26 shows the simulated return loss. The center frequency is 60.2 GHz, and the -10 dB bandwidth is from 58.2 GHz to 62.05 GHz (6% of relative bandwidth). The antenna radiation patterns were also presented in Fig. III.27, a peak antenna gain of 4.02 dB is obtained at 60.2 GHz.

A parametric study for the angle between slots is shown in Table III.3. It is seen that when the angle α increase, the peak antenna gain decrease along with a larger half power beamwidth (HPBW) on H-plane. This phenomenon can be explained by the increase of the coupling effect when the slots approach each other.

As demonstrated by the simulation, CSDA has interesting performances in 60 GHz band. This antenna has no ground plane and in V band its performances (input matching and radiation pattern) can be impacted by the surrounding environment placed behind the antenna (the metallic chuck of the probe station used for S-parameters measurement or the dielectric supporting plate of the antenna setup shown in Figure III.11). In order to avoid such issues and obtain a good correlation between simulation and measurements two solutions can be envisaged: (i) redesign this antenna by using a reflector/ground plane properly positioned behind the antenna and (ii) re-simulate the antenna taking into account a representative 3D model of the surrounding environment.

Table III.3: Parametric study of angle α effect on radiation.

α (°)	fc (GHz)	Return Loss (dB)	Maximum Gain	HPBW (°)
40	59.7	-21.09	4.14	82
45	60.2	-22.76	4.02	86
50	61.15	-27.48	40.8	90

III.4 Humidity test

The humidity test method is based on IPC-TM-650 2.6.2.1 standard technique[44]. The test samples were firstly dry out in an oven for over 30 minutes at 150 °C, each of them was individually weighed immediately. Then the test samples were immersed in a crystallizing dish filled with deionized water for 12 hours (hr). Each sample was removed independently from the water and sprays dried with nitrogen and weighed again. The same process was repeated for 24 hr and 48 hr respectively. The weight was increased with 1.64% after 12 hr, 1.78% after 24 hr and 1.81% after 48 hr.

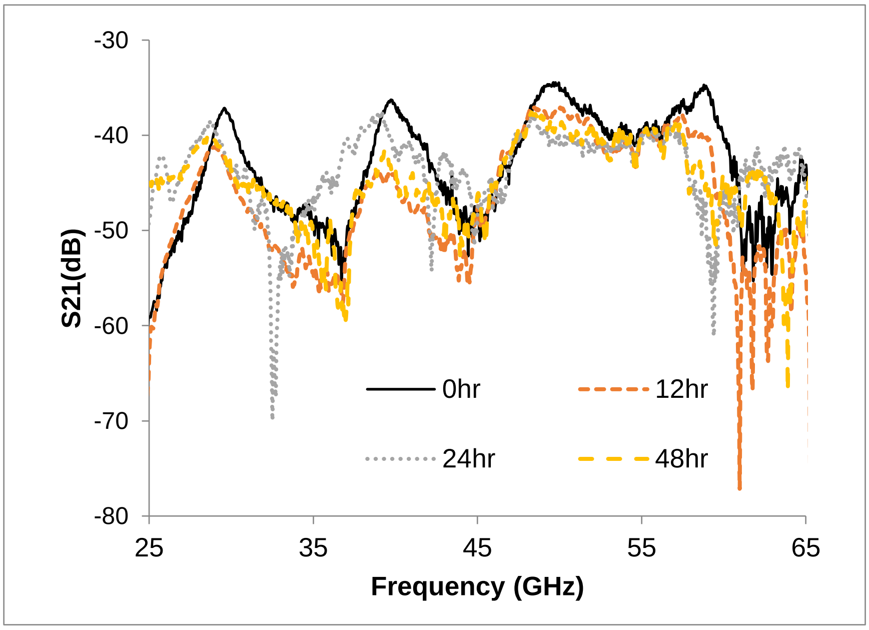


Figure III.28: Measured transmission coefficient of the ring resonator: initial state/0hr (continuous black line), measure after 12hr (red line, square dot), measure after 24hr (green line, circular dot), measure after 48hr (violet, dashed line).

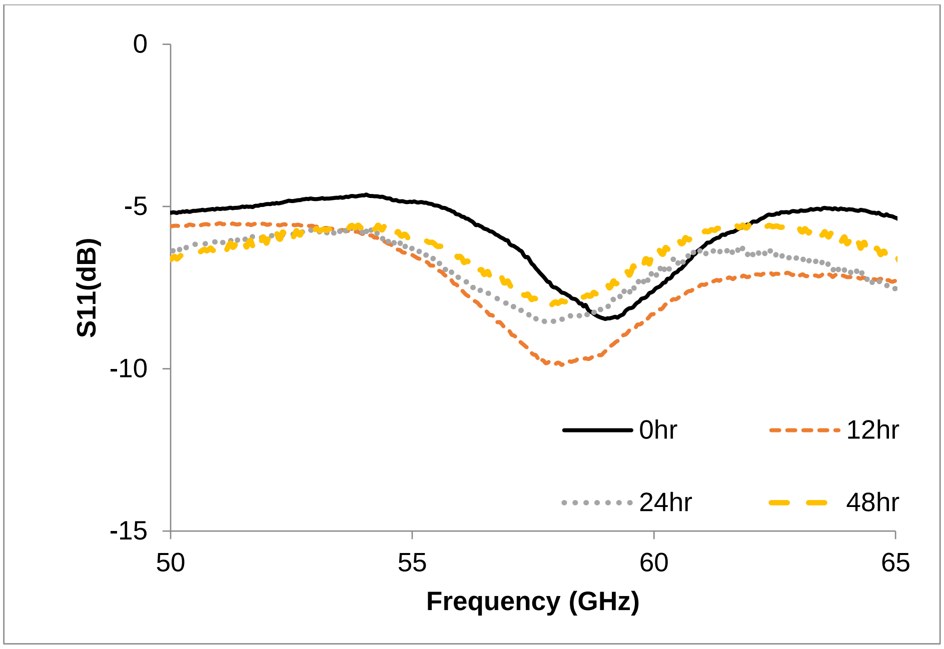


Figure III.29: Measured reflection coefficient of the microstrip patch antenna: initial state/0hr (continuous black line), measure after 12hr (red line, square dot), measure after 24hr (green line, circular dot), measure after 48hr (violet, dashed line).

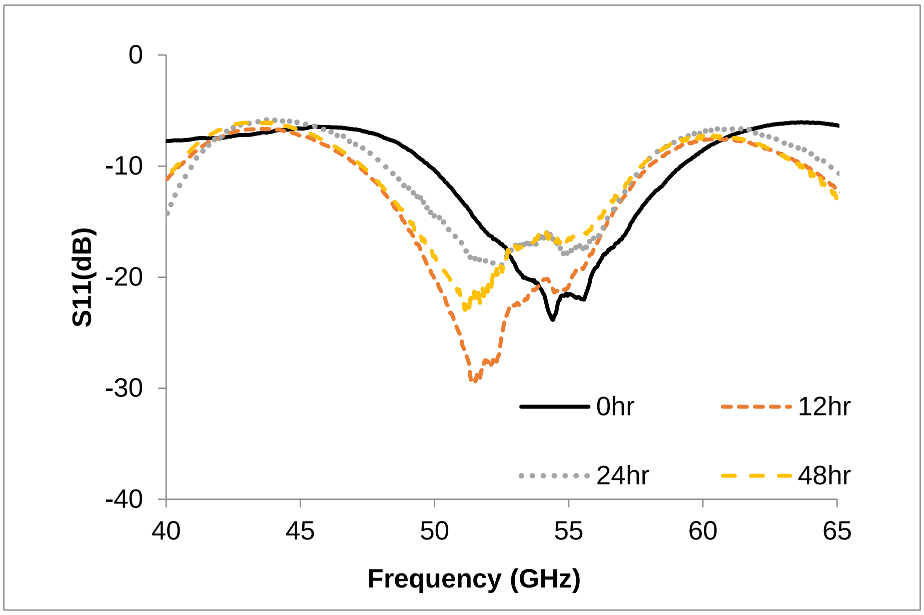


Figure III.30: Measured reflection coefficient of the crossed slot dipole antenna: initial state/0hr (continuous black line), measure after 12hr (red line, square dot), measure after 24hr (green line, circular dot), measure after 48hr (violet, dashed line).

The S-parameters measurements were carried out right after the weighing of the samples. Figure III.28 shows the results obtained for the ring resonator, the patch antenna and the crossed slot dipole antenna. The extracted values for the relative dielectric permittivity are reported in Table. II taking into account the associated tolerances.

Figure III.29 and Figure III.30 show the measured reflection coefficient for the patch and the crossed slot antenna respectively. One can see that the frequency resonance is shifted to the lower frequency because the relative permittivity of the substrate was increased after water immersion as depicted in Table III.4. Also, the S11 decreases because the dielectric losses increase due to water exposition. The input matching of the patch antenna is (only) -8.2 dB mainly due to the transition between microstrip and CPW line. This input matching should appear to be poor but it is not unusual for V-band antennas. For example, the coplanar square monopole antenna proposed in [25] presents a measured S11 in the range of -11 dB at 58 GHz despite of the use of an ‘intrinsic’ CPW excitation. The second antenna (shown in Figure III.30) exhibits better performances: S11 < -20 dB in a 2 GHz bandwidth mainly due to its intrinsic CPW excitation and wideband behavior.

Table III.4: Extracted dielectric constant and dielectric loss.

Time	ε_r	Tolerance of ε_r	tanδ	Tolerance of tanδ
0 hr	3.2	+/- 0.08	0.016	+/- 0.005
12 hr	3.4	+/- 0.06	0.03	+/- 0.008
24 hr	3.6	+/- 0.08	0.04	+/- 0.006
48 hr	3.7	+/- 0.09	0.045	+/- 0.008

III.5 Conclusion

This chapter provides the prerequisites for the heterogeneous integration of wireless communicating node. First, the RF characterization of Kapton is given by measuring a ring resonator. Then, several antennas were designed, fabricated and measured for the implementation of WSN. These antennas will be later combined with the transceiver block.

A standard humidity test was performed in the V band. The experimental results demonstrate that the dielectric constant of the Kapton increases with maximum 15.6 % (up to 3.7 from 3.2 the initial value) and the dielectric losses increases with maximum 181% (up to 0.045 from the initial value of 0.016) when the Kapton structure were immersed in water after 48 hours. A limitation of the water absorption was also observed after 24 hours of the water immersion.

Based on the devices described in this chapter, the following chapter describes the microfabrication process adopted for circuit with electrical patterns on single/both side of the substrate.

IV. Technological process for passive elements on flexible substrate

IV.1 Introduction

The previous chapter presented the implementation of the antennas on flexible substrate, which are the key building components to build a wireless communicating node. For the device which has electrical patterns on only one side, such as patch antenna or cross slot dipole antenna, wet etching process is adapted. For the device which has electrical patterns on both side of the substrate, wet etching process is used for the top side pattern, and lift off process is used for the backside.

This chapter presents in detail the microfabrication process used to implement RF circuits on flexible substrate, including the wet etching, and the lift off.

IV.2 Substrate preparation

As discussed in chapter II.4, we use the PDMS to make adherence between polyimide film and the substrate host. The electrostatic forces between the Kapton film and the PDMS allow a free adhesion without adhesive and an easy peeling after manufacture.

IV.2.1 PDMS layer deposition

The PDMS deposition is generally done on a wafer which will be used in a spin coater to realize the PDMS membrane. A classical cleaning process is required for the host carrier (Silicon wafer or glass wafer). First, we need to clean the wafer with piranha solution, which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), the H_2SO_4 can help reduces organics to carbon while H_2O_2 can oxidize carbon to form CO_2. Then an oxygen plasma treatment (optional) during 5 minutes can help remove all moisture on the surface.

The PDMS membrane is made by spin coating the PDMS on the substrate, so the PDMS has to be prepared. It means, mixing of the monomer and the curing agent and degassing the PDMS. The PDMS we used is the Sylgard 184 from Dow Corning. For this PDMS the usual ratio between the PDMS and the curing agent is 10:1 (weight). The order is put first the PDMS then the curing agent, doing the opposite may lead to a bad cross linkage of the polymer. Once the PMDS is mixed, it is placed in a vacuum desiccator for degassing (30 minutes).

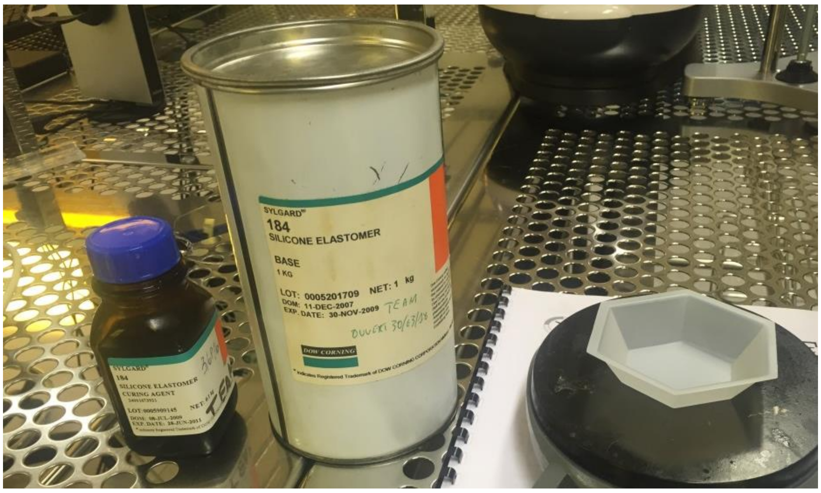


Figure IV.1: Sylgard 184 part A and Part B.

Figure IV.2: Vacuum desiccator.

The most relevant step is the spin coating of the PDMS since the speed, the acceleration and the time of the spin coating will define the thickness of the layer. In this work, the recipe employed is 5000 rpm, 5000 rpm/s and 30 seconds, to obtain a PMDS layer as thin (5 µm) as possible:

- To guarantee the best homogeneity thickness

- To limit the vacuum degassing
- To limit swelling on the chemical stages

Finally, the film of deposited PDMS is polymerized in an oven at 120°C during 2 hours, or a rapid curing on a hotplate temperature to 150°C for 10 minutes.

IV.2.2 Kapton film preparation

First, we need to cut the Kapton tape into shape of 4-inches wafer, so we can later laminate the polyimide onto the Silicon wafer. We made the choice of 4-inches wafer as the host carrier respect to our micro technologies equipment.

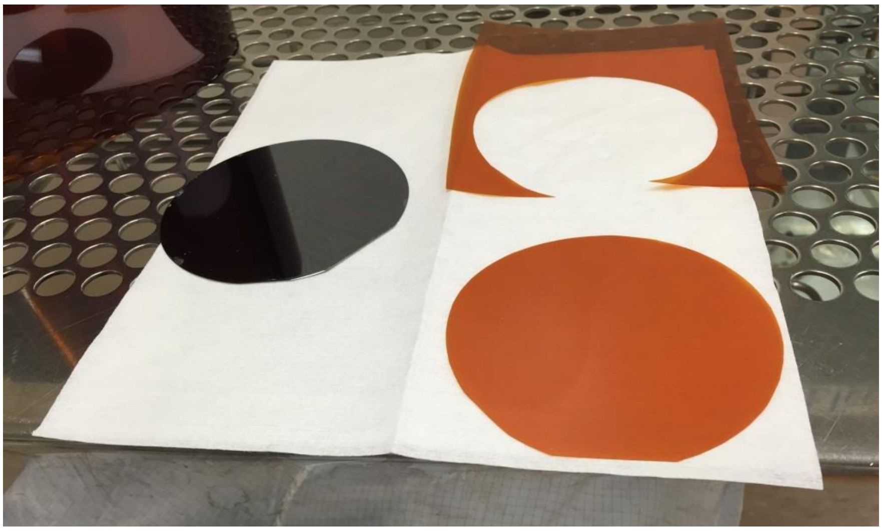


Figure IV.3: Cut Kapton tape into a 4-inches wafer shape.

The substrate need to be properly cleaned to prevent a poorly adhesion of the deposited metal on the substrate, and obtain a higher purity of metal deposition. But unlike the classical cleaning process used for silicon wafer, to remove all the moisture on Kapton, we need:

1. Soaking Kapton in a crystallizing dish filled with Xylene during 5 minutes to remove any hydrocarbon contamination.
2. Rinsing with wash bottle contains Xylene.
3. Soaking Kapton in a crystallizing dish filled with Acetone during 5 minutes to remove Xylene.
4. Rinsing with wash bottle contains Acetone.

5. Soaking Kapton in a crystallizing dish filled with Ethanol during 5 minutes to remove Acetone.
6. Rinsing with wash bottle contains Ethanol.
7. Rinsing with deionized water to remove all trace of previous chemical.
8. Blow drying with a nitrogen gun.
9. Bake out Kapton in an oven at 150°C for at least 12 hours.

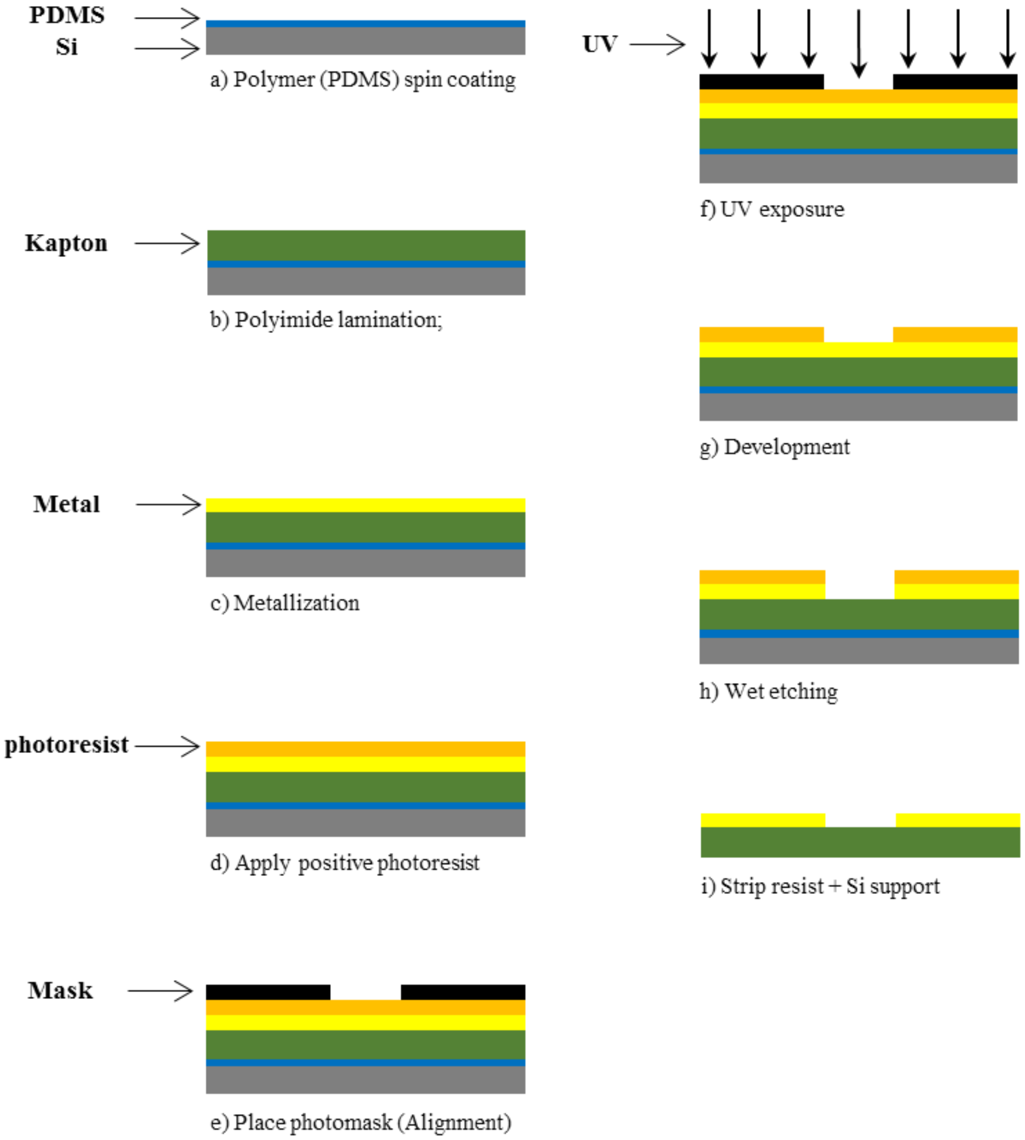
All the previous soaking steps can be performed in an ultrasonic cleaner to obtain the optimum result.

Once the Kapton plaque is prepared, it will simply roll on the PDMS-Si support using a Shipley 360N machine from Rohm and Haas. This technique limits the presence of bubbles between the two surfaces. The substrate to be handled is then appeared as a sandwich: silicon, PDMS, Kapton.

IV.3 Implementation of circuits with electrical pattern on topside

Before performing a wet etching technique to obtain electrical pattern, the Kapton film is coated with a Titanium-Gold (Ti/Au) of 50/200 nm or Titanium-Copper (Ti/Cu) of 50/500 nm in an Edwards Auto 500 electron-beam evaporation system. In case of Ti/Cu coating, the fabrication process will be terminated with a surface finishing (gold immersion deposits about a few nanometers) to prevent Cu from oxidizing.

The choice of positive photosensitive resist was the ECI 3012, as mentioned previously, the speed, the acceleration and the time of the spin coating will define the thickness and the homogeneity of the deposit layer. To obtain a thickness of 1.1 µm of ECI, a recipe of 3600 rpm, 5000 rpm/s during 30 seconds is applied. After resin coating, place the Kapton on a hotplate at 90°C during 1 minute, this softbake will reduce the remaining solvent content and prepare the substrate for UV exposure (405 nm). Then we use a Karl Suss MA150 aligner to exposure the resist during 9 seconds. The following step is the Post Exposure Bake (PEB) is performed before development on a hotplate at 110°C during 1 minute, this baking step can be applied above the softening point of the resist without destroying it. The development step will remove the exposure part of the photoresist to form the pattern. Final step of this process is to etching the metal with correspond chemical solution.


PDMS
Si
Kapton
Metal
photoresist
Mask
UV

a) Polymer (PDMS) spin coating

b) Polyimide lamination;

c) Metallization

d) Apply positive photoresist

e) Place photomask (Alignment)

f) UV exposure

g) Development

h) Wet etching

i) Strip resist + Si support

Figure IV.4: Fabrication sequence of wet etching process.

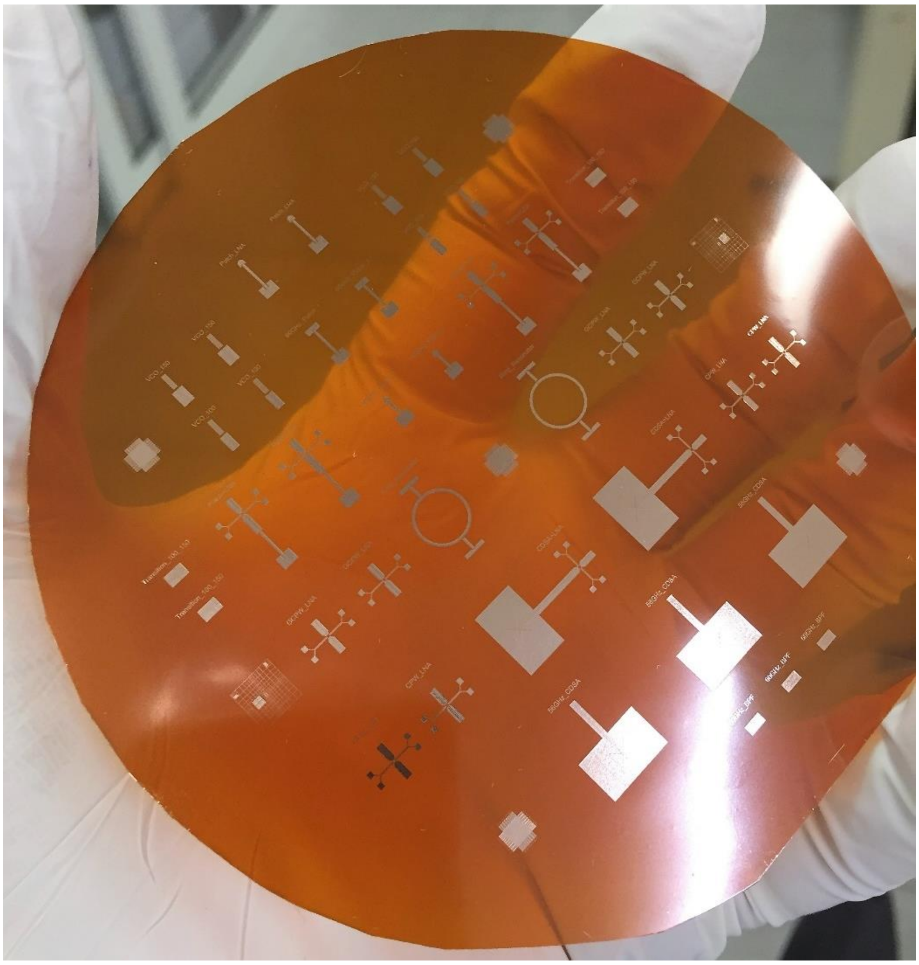


Figure IV.5: Realized Kapton wafer with topside electrical pattern.

IV.4 Implementation of circuits with electrical patterns on both topside and backside

In order to realize a double-sided wafer like the crossed-dipoles array antenna in chapter III.3.2, the process flow is described as following, the backside electrical patterns are fabricated by using the wet etching technique, for the topside electrical patterns, we used a lift-off process for two reasons:

- No need to protect the backside patterns since no chemical etching will be applied on the topside.
- A backside alignment is required (see Figure IV.7), and the Kapton has low light reflection, if the metallization layer is presented on the topside, we can hardly see the align marks on the backside.

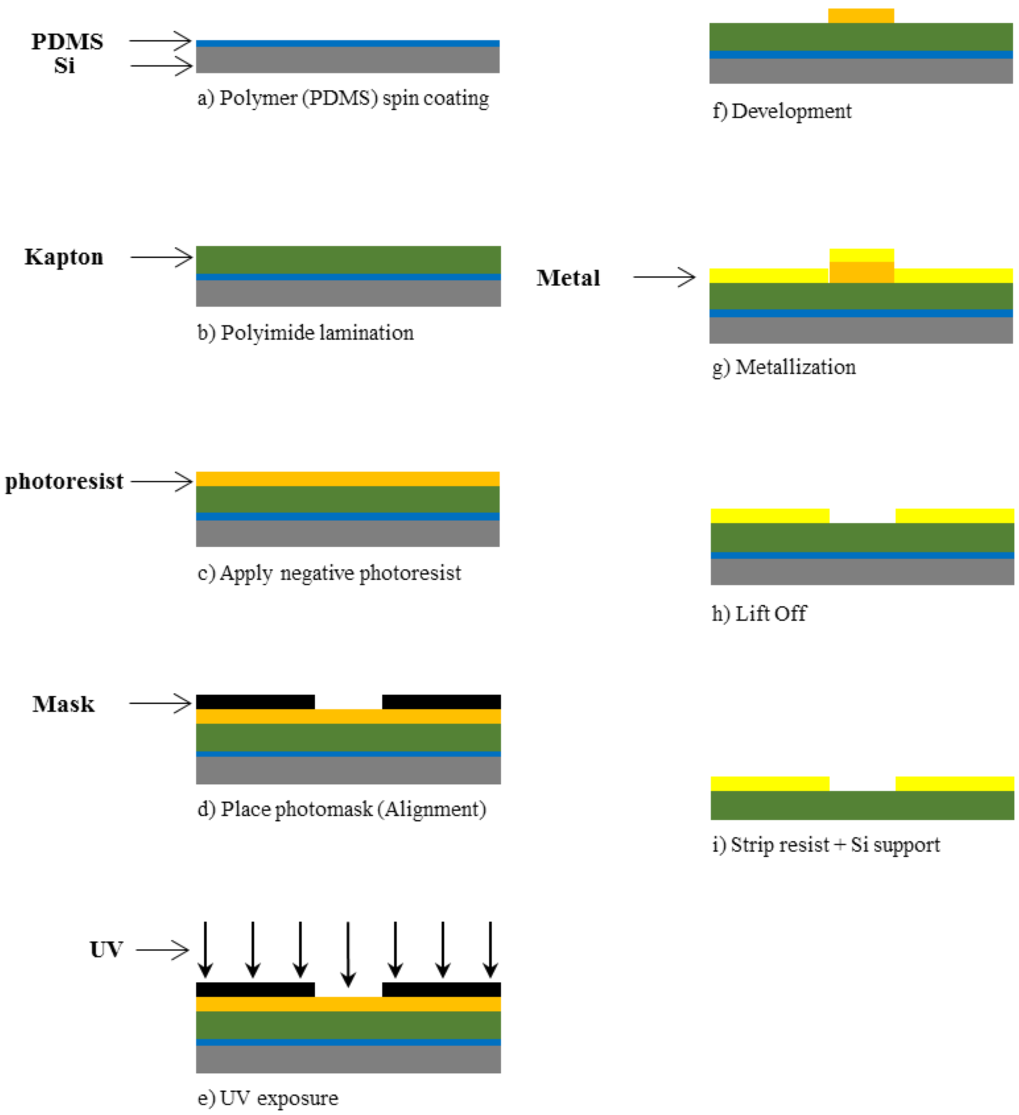

PDMS
Si
a) Polymer (PDMS) spin coating
Kapton
b) Polyimide lamination
photoresist
c) Apply negative photoresist
Mask
d) Place photomask (Alignment)
UV
e) UV exposure
f) Development
Metal
g) Metallization
h) Lift Off
i) Strip resist + Si support

Figure IV.6: Fabrication sequence of lift-off process.

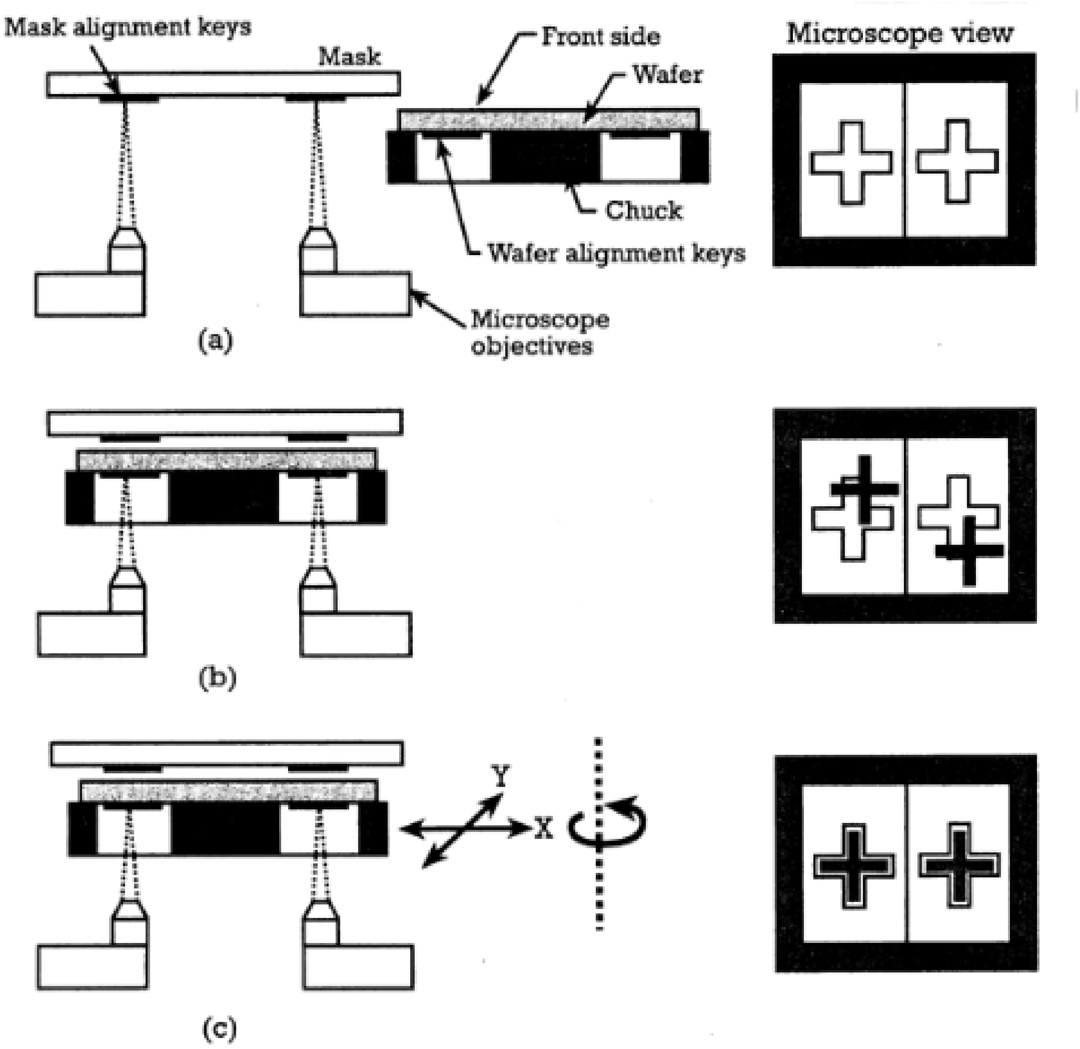

Mask alignment keys
Mask
Front side
Wafer
Microscope view
Chuck
Wafer alignment keys
Microscope objectives
(a)
(b)
Y
X
(c)

Figure IV.7: Double-sided alignment scheme: (a) The image of mask alignment marks is electronically stored; (b) The alignment marks on the back side of the wafer are brought in focus; (c) The position of the wafer is adjusted by the translation and the rotation to align with the stored image [45].

The choice of negative photosensitive resist was the nLof 2035, the thickness of resin layer is 2.5 µm. The speed, the acceleration and the time of the spin coating are 5000rpm, 5000 rpm/s and 30 seconds respectively. After resin coating, place the Kapton on a hotplate at 105°C during 1 minute. Then a UV exposure (365 nm) during 5 seconds is needed in the MA150 system. The following PEB on a hotplate at 110°C during 1 minute. The development step will remove the non-exposure part of the photoresist to form the mold. The metallization layer is then deposit on the mold before lift-off. The final electrical patterns on the substrate matching the exposure part of the resist.

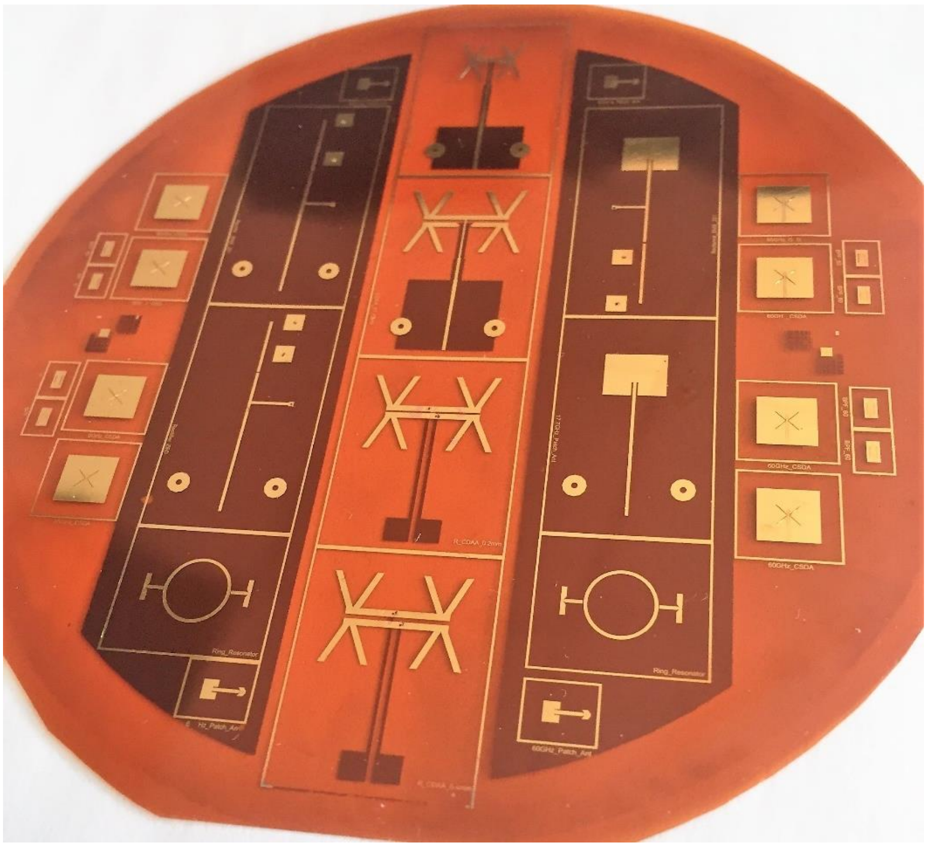


Figure IV.8: Realized Kapton wafer with double sided electrical patterns.

IV.5 Conclusion

This chapter provided the microfabrication process used to implement RF circuits on flexible substrate, if there are only electrical patterns on a single side of the substrate, the wet etching is preferred, otherwise, the lift off is strongly advised for realization of the second side of the substrate.

Different realized Kapton wafer were successfully reproduced to validate these processes. The match between simulation results and measurement results of the ring resonator from 10 GHz to 60 GHz, the 60 GHz patch antenna with a gain of 5 dBi, and the rectenna for energy harvesting prove that this technology is reliable and reproducible for the RF applications from several GHz up to 94 GHz.

Though inkjet technique has always been considered as a low cost process, but for a high-volume application like the node deployment of Wireless Sensor Networks (WSN), wafer cost reductions can significantly lower the total cost per node and became comparable to the cost of inkjet.

V. Heterogeneous integration on flexible substrate

V.1 Introduction

In this chapter, the technique of 3D heterogeneous integration of miniaturized communicating modules used for wireless network application will be presented. As described in the general introduction, the goal is to realize a low power System in Packaging (SiP) including both the radio interface (with baseband and RF circuitry) and the antenna to transmit and receive a 60 GHz signal. The antenna was designed directly on the flexible substrate (see chapter III.3) and the CMOS transceiver will be added by using the flip chip technique. This technique will be discussed and detailed in this chapter.

V.2 IC packaging choice

V.2.1 Wire bonding vs flip chip

To establish an electrical interconnection between the integrated circuit (IC) and the package, wire bonding has always been a dominant method because it is generally considered the most cost-effective and flexible interconnect technology[46]. This technique provides electrical interconnections directly from the terminals on a chip to those on a chip carrier circuit by using a fine wire. The structure of a wire bond assembly is shown in Figure V.1.

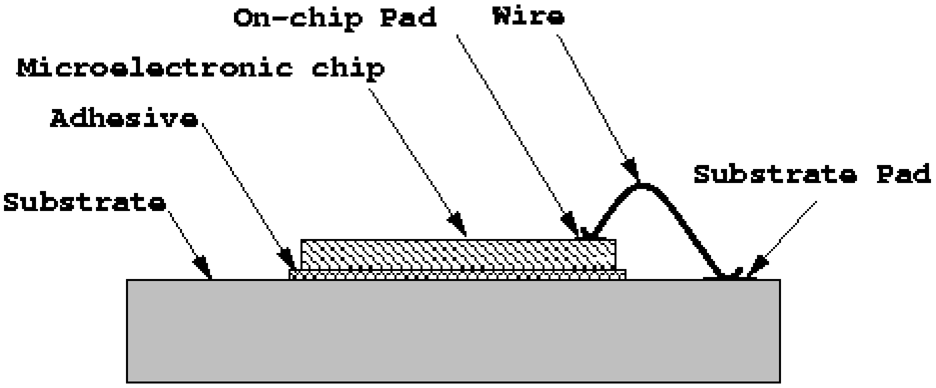


Figure V.1: Generic configuration of wire-bond packaging, source : [47].

Despite its simplicity, this technique used most for conventional IC packaging which deals with electrical signal only while RF system packaging need to deal with electrical signal as well as microwave signal.

Flip chip is another method for interconnecting semiconductor devices (such as IC chips and MEMS) to external circuitry with solder bumps that have been deposited on the chip pads. This assembly technique was first introduced commercially by IBM in the 1960s [48], originally the it was known as Controlled Collapse Chip Connection (C4) but later the technology and its variations have been known just as flip chip. As shown in Figure V.2, the solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and the solder is flowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry.

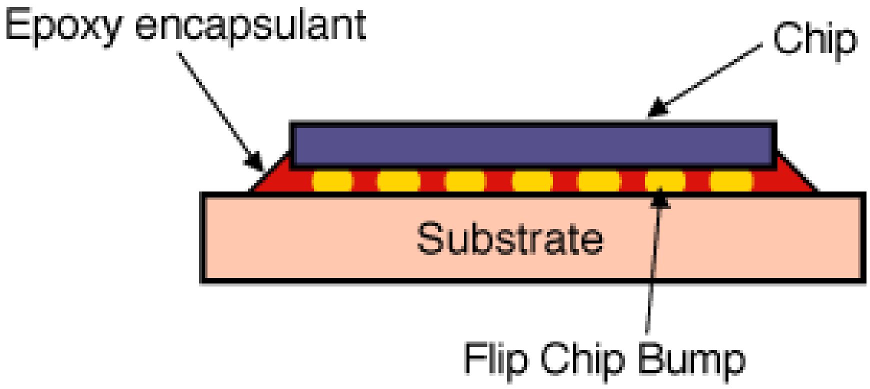


Figure V.2: Generic configuration of flip chip packaging with underfill.

It is widely understood that flip chip offers a variety of benefits compared to traditional wire bonding, the main advantage is that the chip sits directly on the circuit board, and the completely flip chip assembly is much smaller than a traditional carrier-based system, the short bumps can reduce greatly the parasitic inductance, allowing higher-speed signal, and better heat dissipation[49][50].

So, we choose the technique of flip chip over wire bonding as our System in Package (SiP) technique, because it can allow us to work on applications in microwave frequency bands, and it meets perfectly to today's electronic industry needs which are to make products more compacts while at the same time increasing their functionality.

V.2.2 Au stud bumping

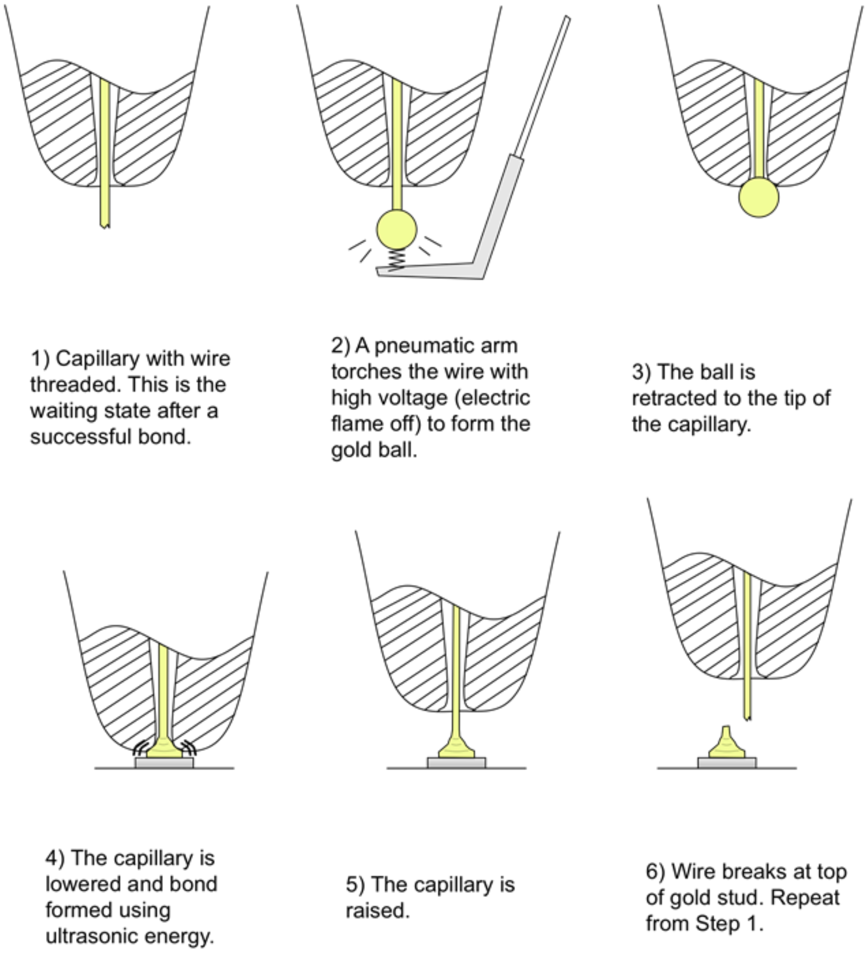
In flip chip assembly, the IC die is mounted face-down on a substrate which may be either a chip carrier, or a circuit wiring board (in our case). Electrical interconnection between chip and substrate is achieved by creating conductive gold bumps either on the chip or the substrate.

Stud bump bonding process is a "modified" wire bonding process. As like wire bonding, there is bonding of the ball on the chip pad. Unlike wire bonding, there is no second wire bond to a substrate carrier. The wire is terminated after the first bond, so there is only a bump on the chip pad. To complete the interconnect, the chip is inverted onto a substrate which ultimately enable the electrical interconnection using an adhesive or an ultrasonic flip chip attach process.

As illustrated in Figure V.3, the process of stud ball bumping is the following: an electric shock comes to soften a gold wire of ball bonding with the creation of a ball. A thermosonic welding between this ball of gold and the substrate created followed break of the wire to the base of the gold ball. The size of the gold bump is determined by the electric field brought. The quality of the welding depends on the force and the power of the ultrasounds as well as temperature implemented and varies according to the nature of material. The length of the tail once the stud deposited (wire which exceeds gold ball creates) depends on the composition of the wire.

The main reason that we choose a gold stud bumping over a conventional solder bumping is following:

Under Bump Metallization (UBM) of the bond pads is required for a solder bump process to ensure that the solder bump will adhere effectively. In the case of Au stud bumping the only requirement is that the bond pad has to be suitable for a wire bonding process, so the UBM is no longer required, and it fit perfectly for our case where transceivers are using 65 CMOS technology of STMicroelectronics, there is no UBM but aluminum as final metallization on the chips.



1) Capillary with wire threaded. This is the waiting state after a successful bond.

2) A pneumatic arm torches the wire with high voltage (electric flame off) to form the gold ball.

3) The ball is retracted to the tip of the capillary.

4) The capillary is lowered and bond formed using ultrasonic energy.

5) The capillary is raised.

6) Wire breaks at top of gold stud. Repeat from Step 1.

Figure V.3: Gold stud bumping process, source: [51].

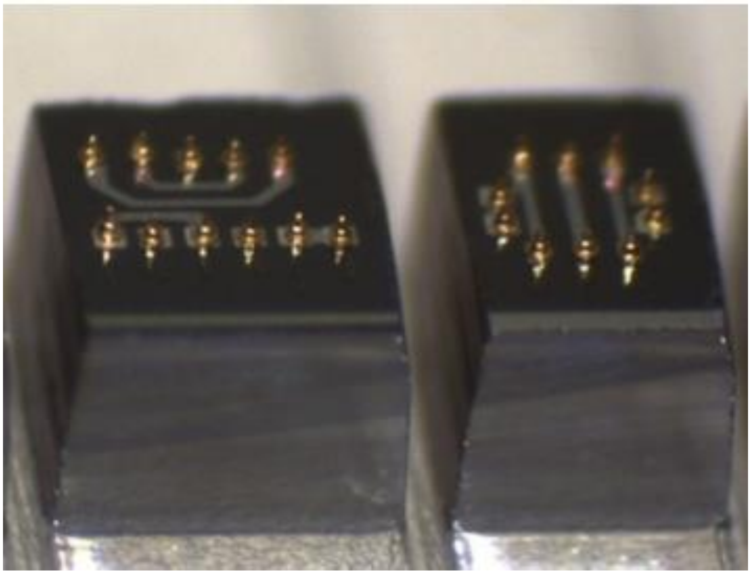


Figure V.4: Gold stud bump realization on silicon dummy.

V.3 Assembly process

For the work reported here, we used a non-conductive adhesive (NCA) method as flip chip bonding technique, it is composed of an adhesive polymer resin (EPO-TEK 353ND-T[52]) and its curing agent, it does not contain any conductive particles. The main reason of using this polymer resin is because it has a relative low crosslink temperature (≤ 150°C), which can help to limit Kapton's elongation.

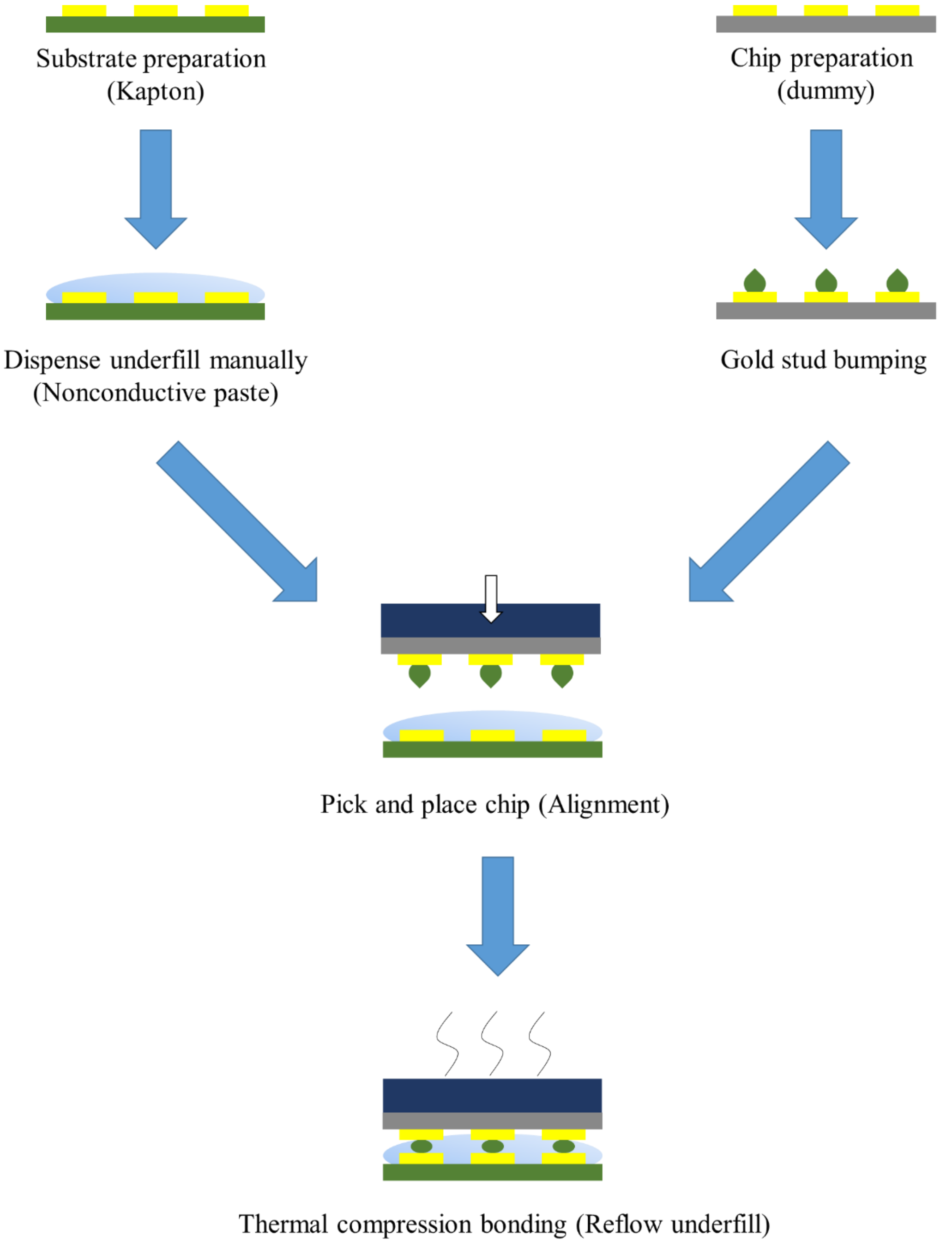

Substrate preparation
(Kapton)
Chip preparation
(dummy)
Dispense underfill manually
(Nonconductive paste)
Gold stud bumping
Pick and place chip (Alignment)
Thermal compression bonding (Reflow underfill)

Figure V.5: Process flow of flip chip.

During the bonding process, the bumps on the chip are in contact directly with the corresponding pads on substrate with a face-down configuration as presented in Figure V.5. When the adhesive is cured by the heat, it shrinks and maintains the mechanical contact between the bumps and the corresponding pads under compression, thus making the electrical interconnection [53].

For a first step, a serial of reliability tests (including RF and DC tests) will be performed to check if all the interconnections are established properly and that there is no breaking problem between the chip and the substrate. To perform these tests, the chips will be mounted on Kapton circuit by using the flip chip technique. Given the cost of chips with 65nm technology, VCOs and LNAs dummies were first manufactured with a conventional wet-etching process. In order to simulate precisely the situation of a real chip integration, the dummies were coated with aluminum lines (500-nm-thick) and have the same pad dimensions and placement as real chips. These dummies first used high-resistivity silicon substrate then later switched to a thin glass substrate for a better visual observation, the design of dummies on both substrates have been taken care of to obtain a 50 Ω coplanar waveguide (CPW) line for the RF test.

V.3.1 Reliability test

V.3.1.1 DC interconnection test

To investigate the effects of Au bump size on the electrical properties of the NCA joint, contact resistances of Au bumps were measure. Figure V.6 shows the four-point probe method used for single Au bump contact resistance measurement [54]. By sending a current to the pad at point 3 and 4, the voltage across the connection bump at point 1 and 2 can be measured, the resistance of the Au bump can be deducted as following: $\rho = \frac{V_+ - V_-}{I_+ - I_-}$.

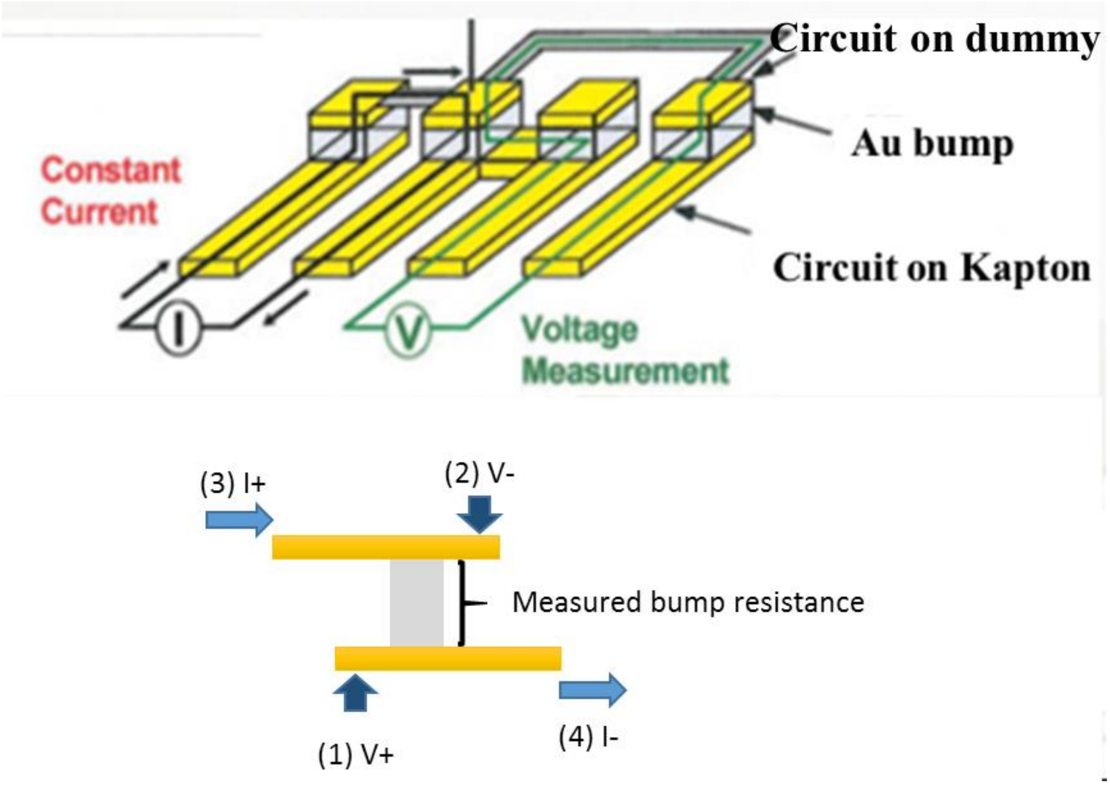

Circuit on dummy
Au bump
Circuit on Kapton
Constant Current
I
V
Voltage Measurement
(3) I+
(2) V-
Measured bump resistance
(1) V+
(4) I-

Figure V.6: Four-point probe resistivity measurement.

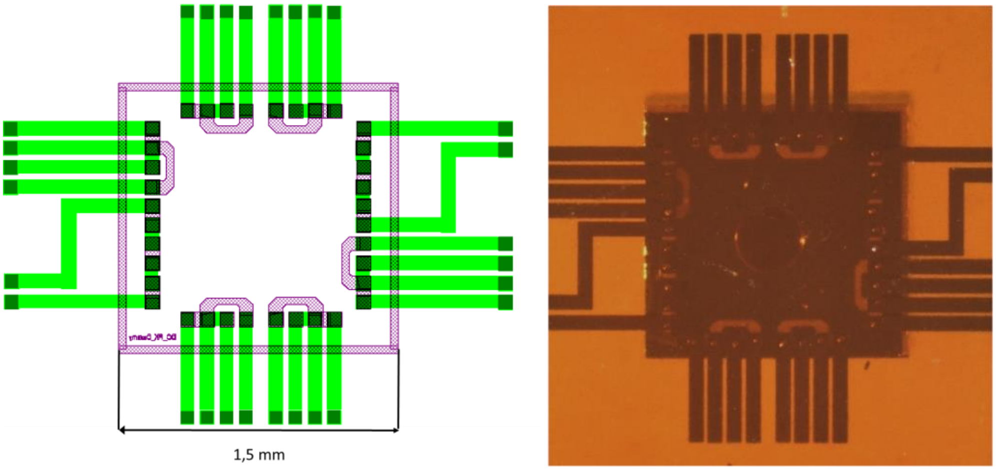


Figure V.7: Design and bottom view of 4-point probe and daisy chain structures.

The results of 4-point probe measurement are given in Figure V.8, A resistance about 10 mΩ was obtained for a single gold bump.

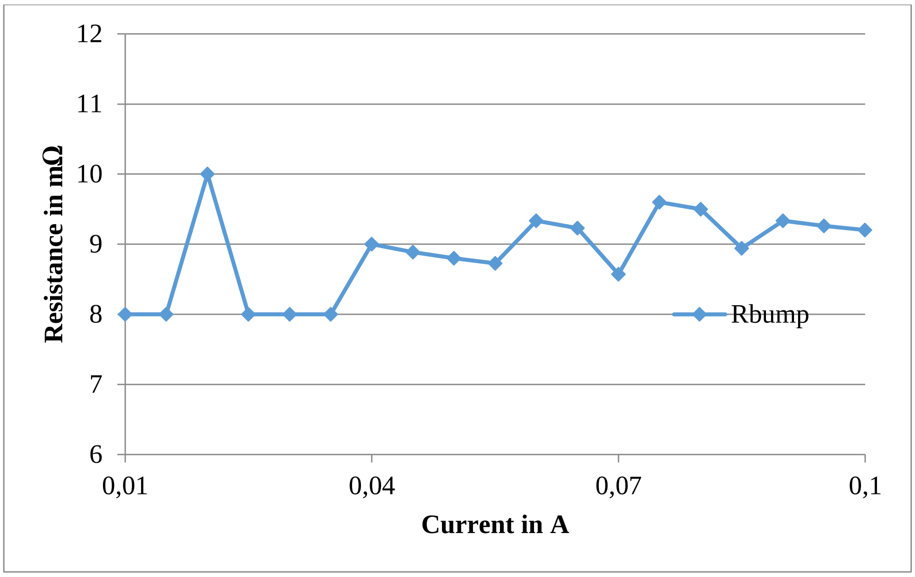


Figure V.8: Measurement of Au bump resistivity using 4-point probe method.

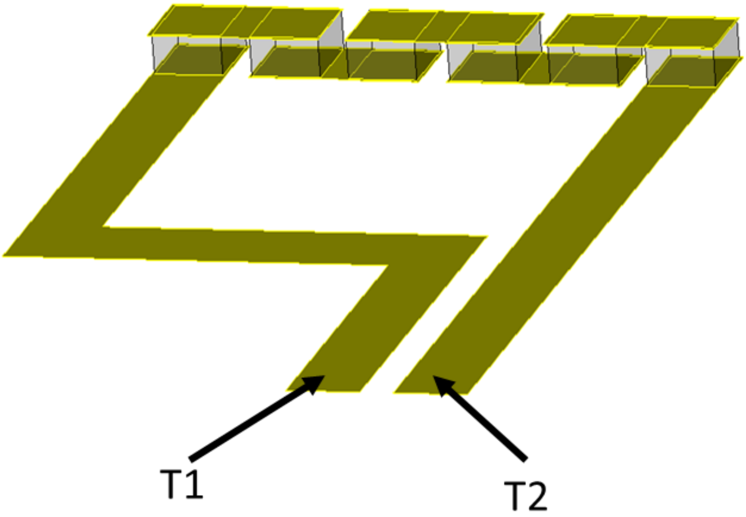


Figure V.9: Daisy chain test.

Another interconnection test technique is daisy chain method [55], electrical continuity is made between patterns on dummy and those on Kapton, it has three functions: a) to measure the total series contact resistance of daisy-chain connections, b) to detect the interconnection quality at each individual bonding positions, and c) to examine the overall integrity of the flip chip assembly.

Applying electrical probes to the two measuring pads T1 and T2, the total series resistance of the daisy chain is obtained, and any open failure can be detected.

- “Pass” when short circuit (≈ 0 Ω) is measured between T1 and T2.
- “Fail” when an open circuit is measured (∞ Ω) between T1 and T2.

Through 4-point probe and daisy chain test, we can take benefits for leaning and improving assembly process. A resistance about 10 mΩ was obtained for a single gold bump, which proves a very good DC contact has been achieved using flip chip technique.

V.3.1.2 RF interconnection test

High frequency measurement up to 70 GHz were also performed on the flip chip structures in order to test the reliability of assembly process. Dummies circuits with 50 Ω CPW line were fabricated on a 500-µm-thick SCHOTT AF32 glass (Figure V.10) to replace the 65 nm CMOS LNA chip (Figure V.11). The modifications on the access of CPW lines are aimed to simulate the actual difficulty we may have when assembling the real chip (chip dimension as small as 400 µm × 400 µm, pad size as small as 40 µm × 45 µm). The Kapton structure with 50 Ω CPW line is presented in Figure V.12, the width of central track is 130 µm and the gap between central track and ground plane is 10 µm.

As shown in Figure V.13, The two ends of the CPW lines on Kapton are connected to each other by using an intermediate glass dummy chip on which CPW transmission line is performed. The glass dummy chip is mounted on Kapton using the NCA technique with Au bump pre-deposited on glass chip (see Figure V.14).

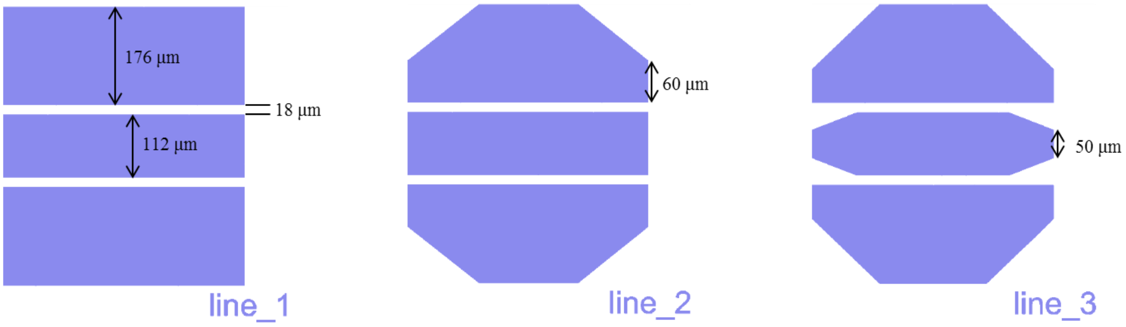


Figure V.10: Designed 50-Ω-CPW lines (LNA dummy) on glass AF32.

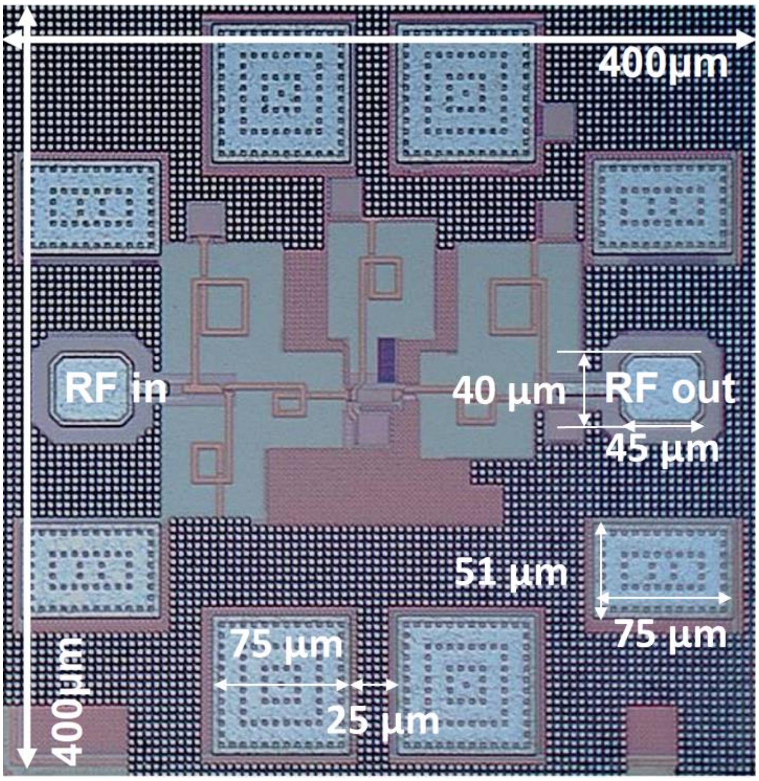

400µm
RF in
40 µm
RF out
45 µm
51 µm
75 µm
75 µm
25 µm
400µm

Figure V.11: Photo of the LNA, circuit dimensions 400 µm × 400 µm including pads.

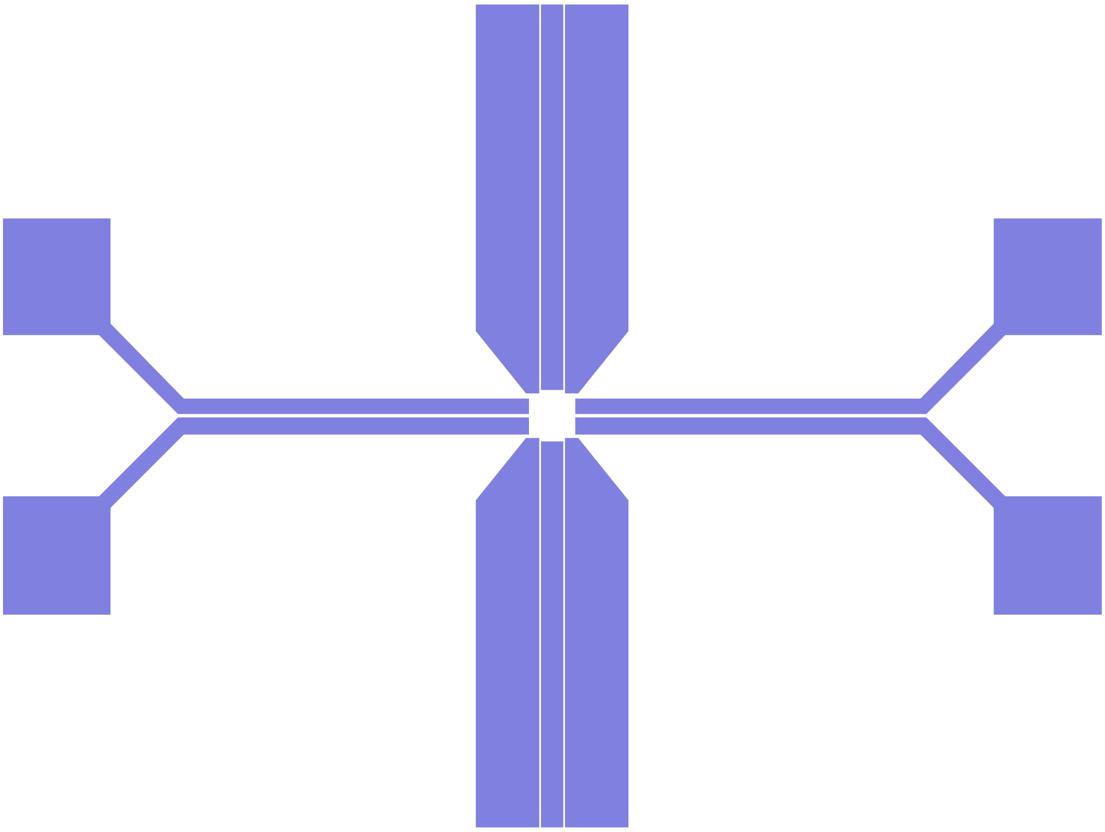


Figure V.12: Design of 50-Ω-CPW structure on Kapton.

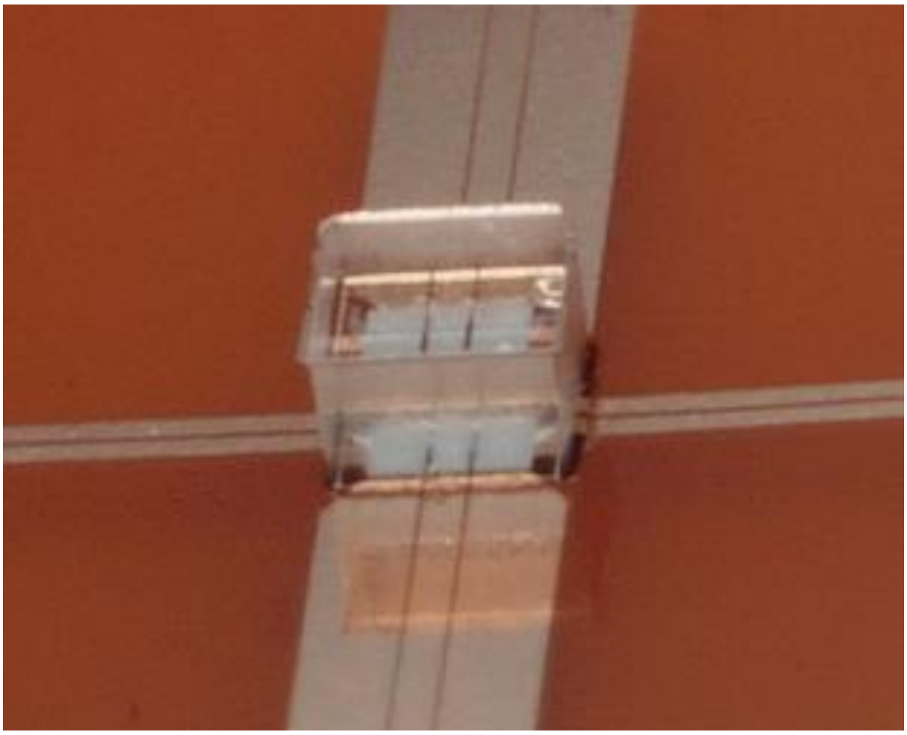


Figure V.13: Photograph of LNA dummy mounted on Kapton.

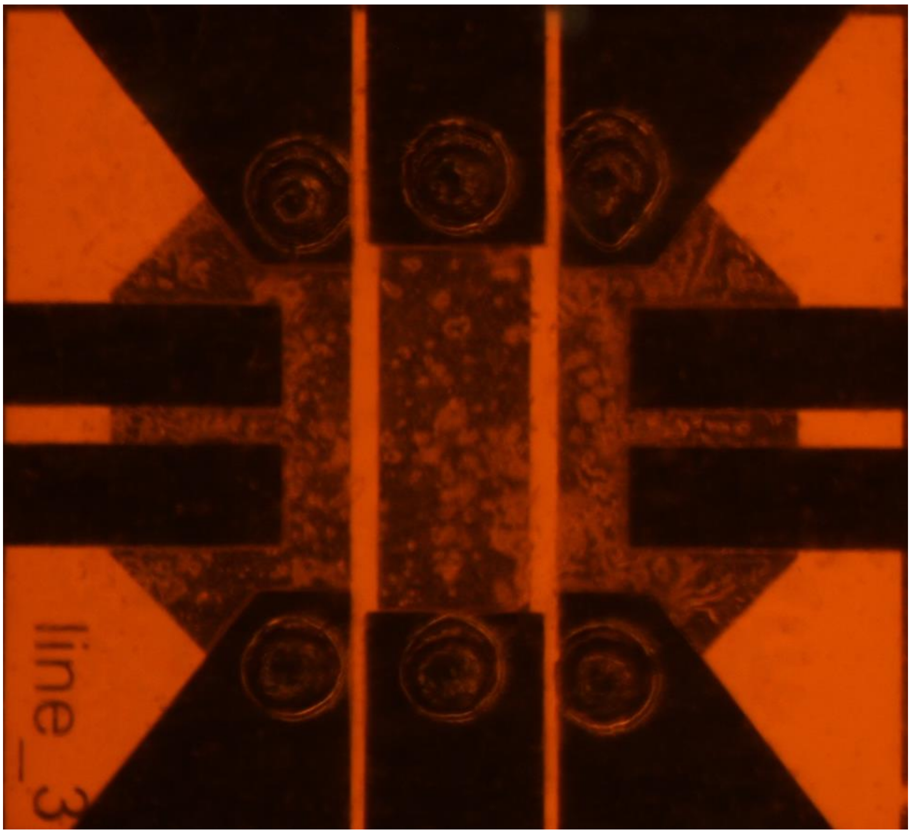


Figure V.14: Bottom view (through Kapton) of a LNA dummy mounted by the flip chip technique.

As illustrated Figure V.15, these structures have been designed and simulated in HFSS, from 50 GHz to 70 GHz, and then characterized with a Vector Network Analyzer (VNA) Anritsu Vectorstar and 150-µm-pitch Infinity probes from Cascade Microtech. A SOLT (Short-Open-Load-Thru) calibration process is done before each measurement. This calibration process consists of replacing the device under test (DUT) by a short circuit, an open circuit, a thru line and finally a load circuit at 50 Ω. After this calibration, the loses caused by the equipment (probes, cables, …) will be omitted.

As shown in Figure V.16 and Figure V.17, a transmission loss about −2 dB and a return loss about -20 dB was measured at 60-GHz-band, these results bring a proof of concept of such integration technique is feasible for V-band applications.

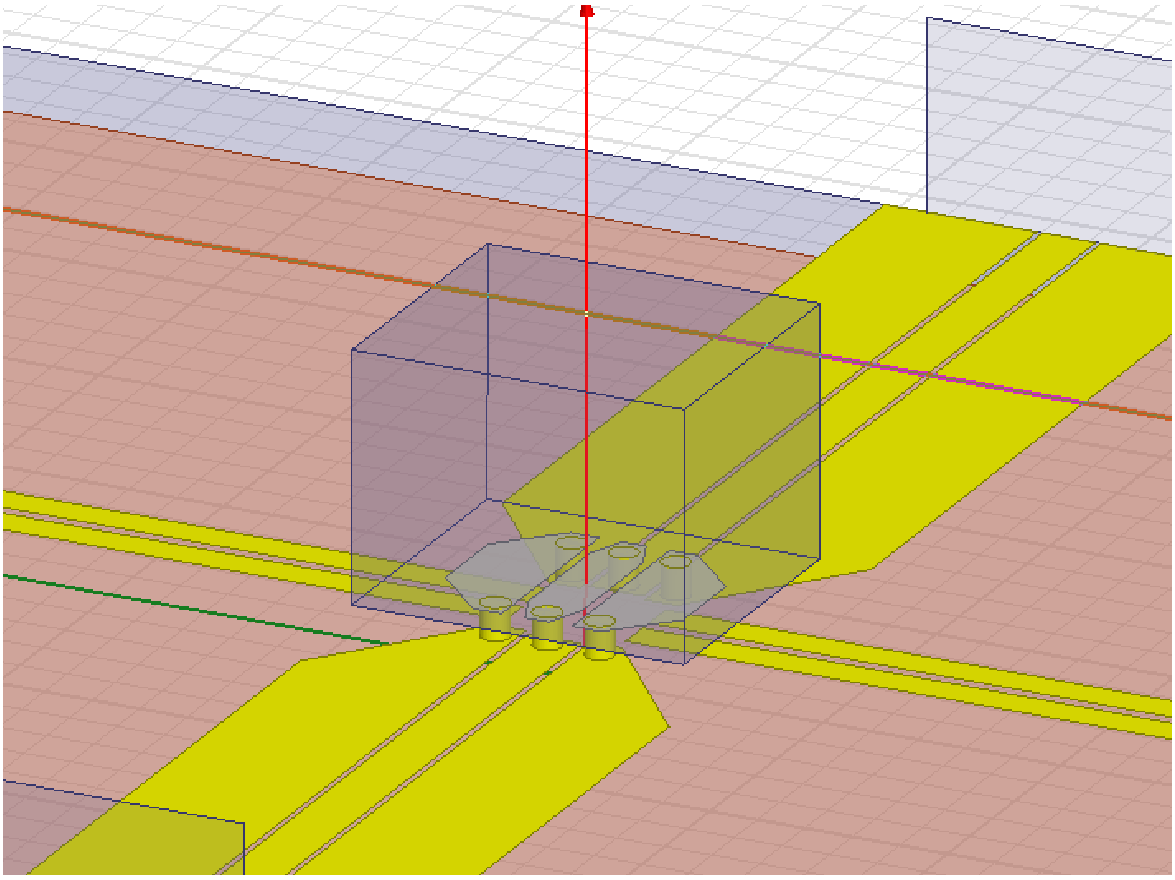


Figure V.15: Designed LNA dummy chip mounted on Kapton in HFSS.

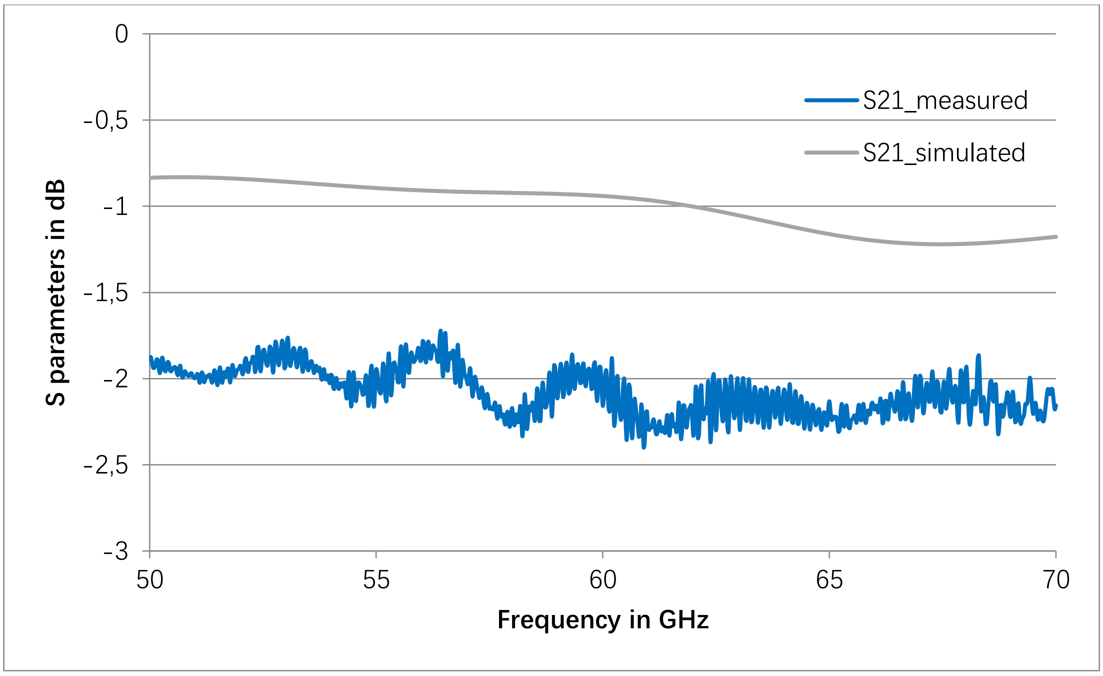


Figure V.16: Measured and simulated insertion loss S21 of LNA dummy on Kapton.

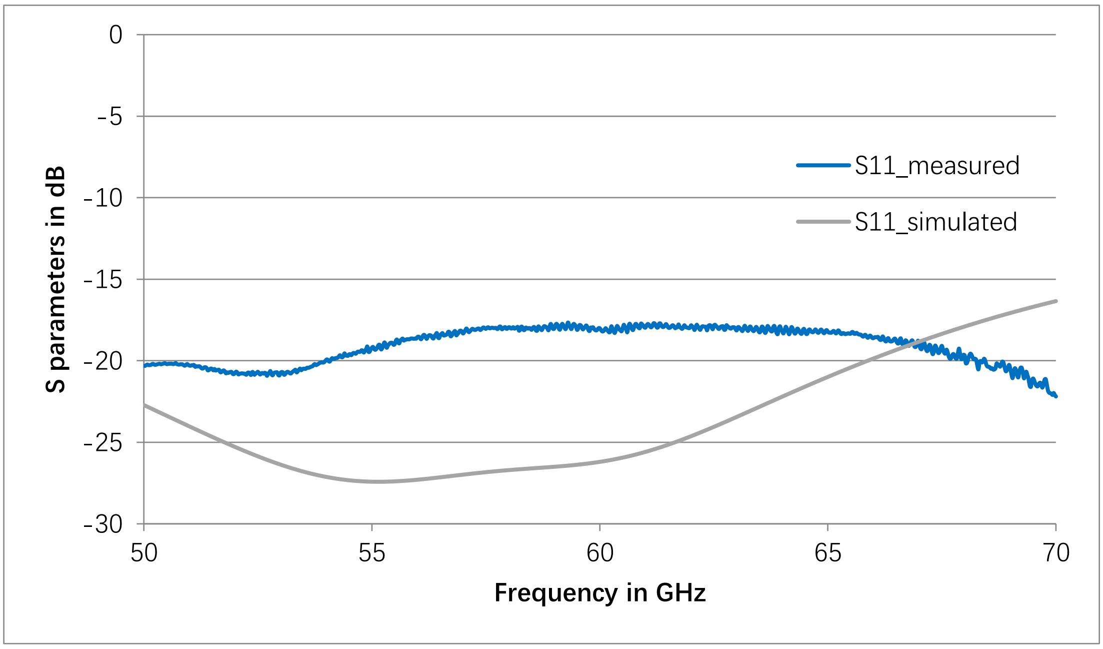


Figure V.17: Measured and simulated return loss S11 of LNA dummy on Kapton.

Despite of good RF performances can be obtained by using this technique. A short-circuit problem was revealed during these tests as shown in Figure V.18. The excess Au bump size and its tail can easily cause a short-circuit failure between two adjacent contact pads. The LNA chip is as small as 400 µm × 400 µm, and the smallest size of the contact is 40 µm × 45 µm, the gap between two adjacent pads can be as small as 25 µm. Also, on the other side, the gap between central track on Kapton and its ground plane can be as small as 10 µm.

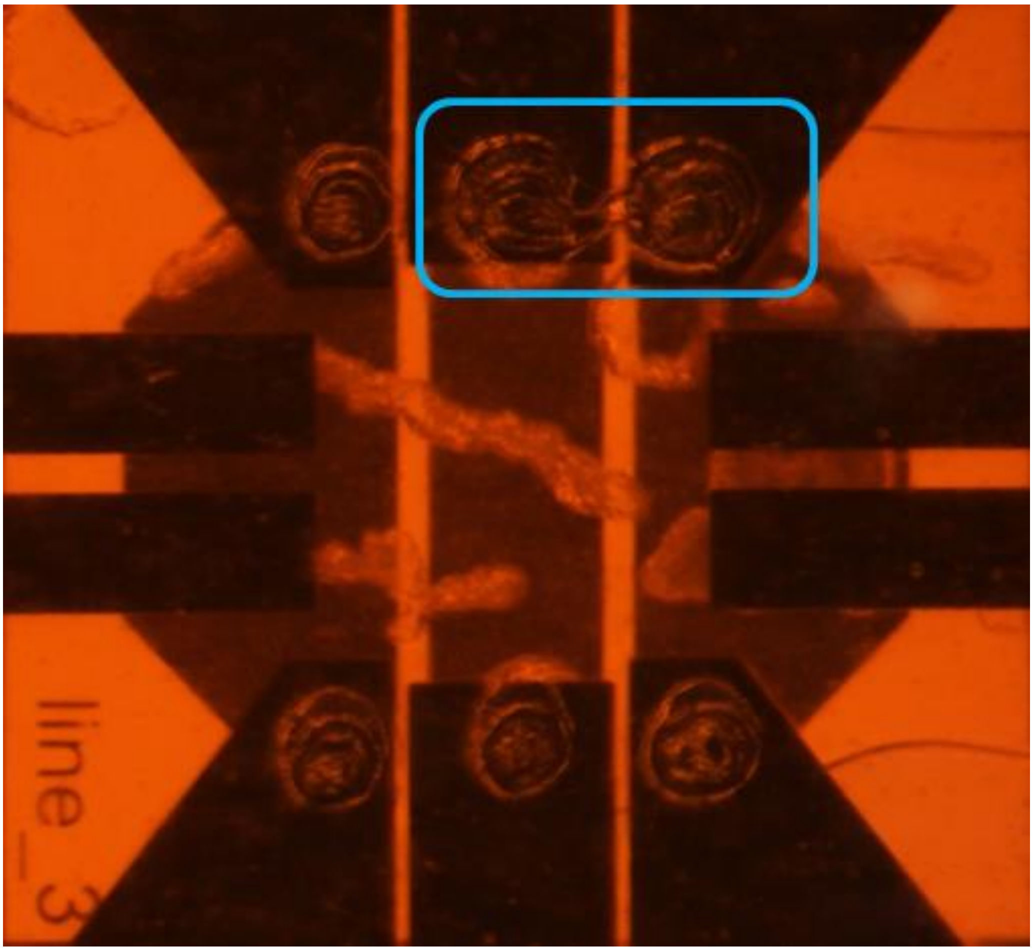


Figure V.18: Short-circuit situation of Au bump deposited by gold stud bumping process.

In fact, these Au bumps were deposited on dummy chip by using semi-automatically wire bonder HB16 from TPT [56], and in order to re-create the reel situation/challenge, where our 65-nm CMOS chips were delivered in a size of 1 mm × 1 mm, the dummy chips were also cleaved individually before Au stud bumping. A slightly misplace of Au bump can increase the uncertainty of chip-alignment and make current processing technique unreliable.

For the first time, we tried to postpone the real LNA chip only as presented in Figure V.19. Its dimension is about 400 µm × 400 µm large and 800 µm height with the smallest contact pad of 40 µm × 45 µm, this chip is a “worst case” from an assembling point of view because of its size, aspect ratio and pads size. During this first test, only the interface between chip and substrate was filled with nonconductive adhesive paste, which is not robust enough to maintain the system, the chip was fallen apart from the substrate after several bending test.

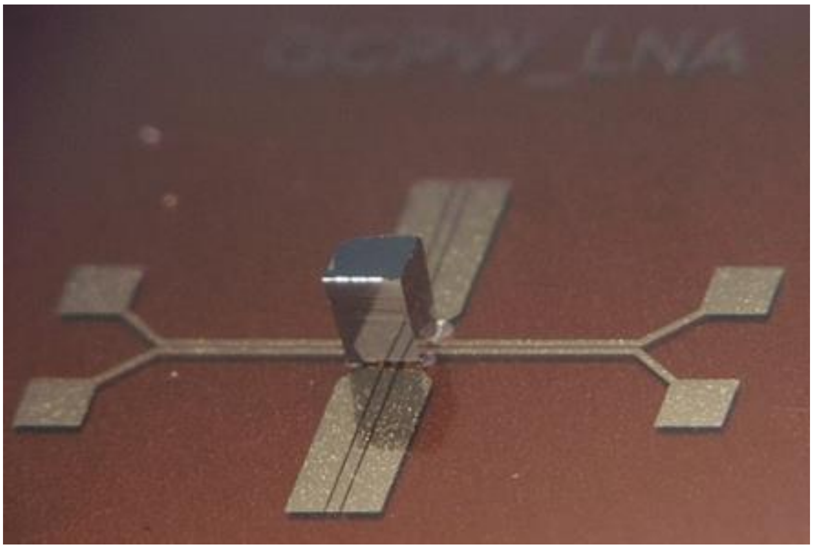


Figure V.19: 65nm CMOS technology LNA mounted on Kapton structure.

In conclusion, we have proven the dummies chips can be mounted with the flip chip technique, but we need to think another process for Au bumping process to resolve the short-circuit problem and a solution to mount the real LNA chip regarding its size and aspect ratio.

V.4 Bumping process by electroplating

The main problem with gold stud bump is they need to be deposit on each contact pad of the chip. The contact pad has as small as 40 µm * 45 µm pad size, which can cause an alignment difficulty later. Especially in our case, the chip was not supplied in a bumped format, we need to use a stud ball bumping technique to form bumps on each contact pads.

As mentioned in chapter V.2.2, flip chip bumps can be deposited either on the chip or the substrate, most flip chip processes have adopted the former approach because of its simplicity. But in our case, there can be advantages in forming the Au bumps as part of the circuit board manufacturing process, particularly for in terms of its rather high deposit rate, well understood chemistry and especially good deposition uniformity.

In the literature, pattern electroplating or electroforming with a photoresist mask is an effective method of bump fabrication [57]. The main difficulty lies on the choice of thick photoresist and its manufacturing process on Kapton. After a little research, we decided to use a chemically amplified ultrathick positive resist AZ 40 XT, which is a optimized photoresist for electroplating, wet- and dry etching [58].

V.4.1 Optimization of thick resist processing

Once the photoresist is chosen, we need to find an optimum process flow for this thick resist on Kapton. The speed of spin coating, the different temperature of baking, the dose of UV exposure, and last but not least, the optimum developing duration.

a) Spin coating

We aimed an Au bumps height about 30 µm, so a thickness of 40 XT at least of 40 µm is required for a uniformed Au electroplating. Generally, with lower spin speeds, higher resist film thickness can be attained, but as illustrated in Figure V.20, at lower spin speed, the edge bead increases, thus the resist film homogeneity will decrease.

As shown in the Table V.1, different tests were perforemed according to the test plan. The process we have chosen is as following: a suited spin profile with start speed of 1400 rpm (low acceleration at 100 rpm/s) followed by a high spin speed 3000 rpm and an acceleration 3000 rpm/s for 1 second to suppress the edge bead. So we can obtain a resist thickness of 45.3 µm in the center and 45.7 µm at the edge for 40 XT.

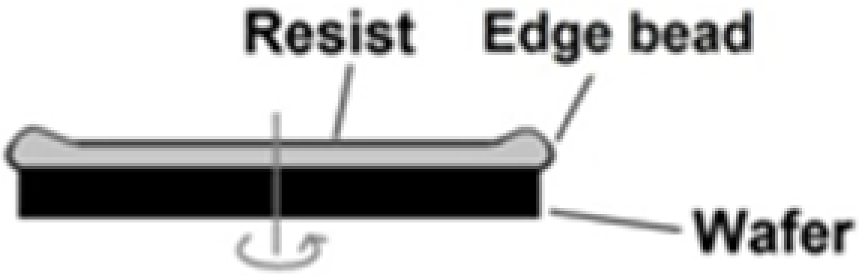


Figure V.20: Formatting of edge bead during spinning[59].

Table V.1: Test plan of spin coating.

Spin profile (speed/acceleration /duration) (rpm/rpm.s^{-1}/s)	1400/100/30 then 5000/5000/1	1400/100/30 then 3000/3000/1	1700/100/30 then 3000/3000/1
Resist thickness (µm)	35.5	45.7	37.8

b) Softbake

After coating, the thick resist film still contains a substantial amount of residual solvent which depends on the respective film thickness. The subsequent bake is performed in order to dry the resist film which would otherwise stick to the mask (mask contamination). Furthermore, the resist layer is hardened during this bake, making it more resistant. Besides an improvement of resist adhesion to the substrate, the dark erosion will be reduced during development step.

However, a softbake too cool/ short increases the dark erosion during development due to the high remaining solvent concentration. And if it is too long/ hot, then it will destroy a certain amount of the photo active compound in the resist. As indicated in the datasheet of the AZ 40XT, the maximum softbake temperature must not be applied abruptly, a temperature ramp on a contact hotplate need to be used.

The softbaking profile that we adopted is as following: first we set the temperature of the hotplate at 65°C, and put resist-coated substrate onto it and increase the temperature to 105°C, then to 126°C, stay at this temperature for 3m30s. When softbake is done, put the substrate onto another hotplate at 70°C for cooling to prevent the resist cracks.

c) UV exposure

If the exposure duration is too low, the development time of positive resists WILL increase, until a certain depth where the development almost stops, thus an over-development might be happened. If the exposure duration is too high, an undesired part of the resist which should not be exposed, will be exposed by scattering, diffraction and reflection of. As a consequence, too much of the positive resist will be cleared during development.

Using a MA6 aligner (25 mW/cm^2), a test plan as following is performed. Below 30.2s exposure, some residue of resist can be found on substrate after development.

Table V.2: Test plan of UV exposure duration.

Exposure duration (s)	Measurement of a 50-μm-gap (μm)
41.2	56.9
40.2	56.4
39.2	56.1
38.2	55.6
37.2	55
36.2	54.5
35.2	53.9
34.2	53.6
33.2	53.1
32.2	52.7
31.2	52.2
30.2	51.6
29.2	51.1
28.2	50.2

d) Post Exposure Bake (PEB)

For a chemically amplified ultrathick positive resist like the AZ 40 XT, a post exposure bake is strongly recommended in order to complete the photoreaction and make this resist developable. The recommended PEB for AZ 40 XT is at 105° for 100 seconds.

The PEB profile that we adopted is: Set the temperature of the hotplate at 95°C, put substrate onto it and increase the temperature to 105°C, stay at this temperature for 80 seconds. When PEB is done, put the substrate onto another hotplate at 70°C for cooling to prevent the resist cracks.

e) Development

One of the last steps in the photolithographic process is development. The amount of development time increases with the ratio of exposure surface/ total surface. Once the process is finished, the wafer sample was observed in a Scanning Electron Microscopy (SEM) S-4800 from Hitachi. As shown in Figure V.21, a cross opening on 45.3-µm-thick 40 XT is clearly developed on Kapton, no visible residue is observed.

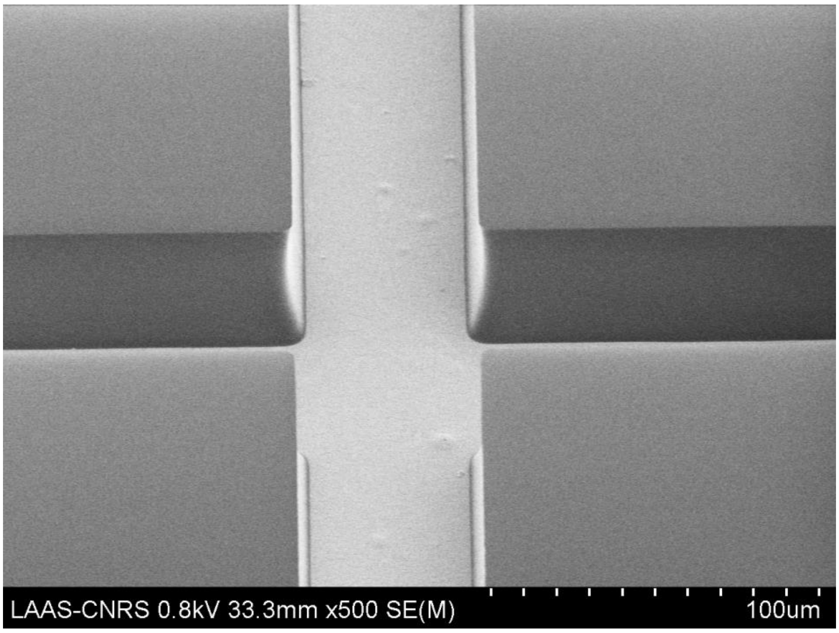
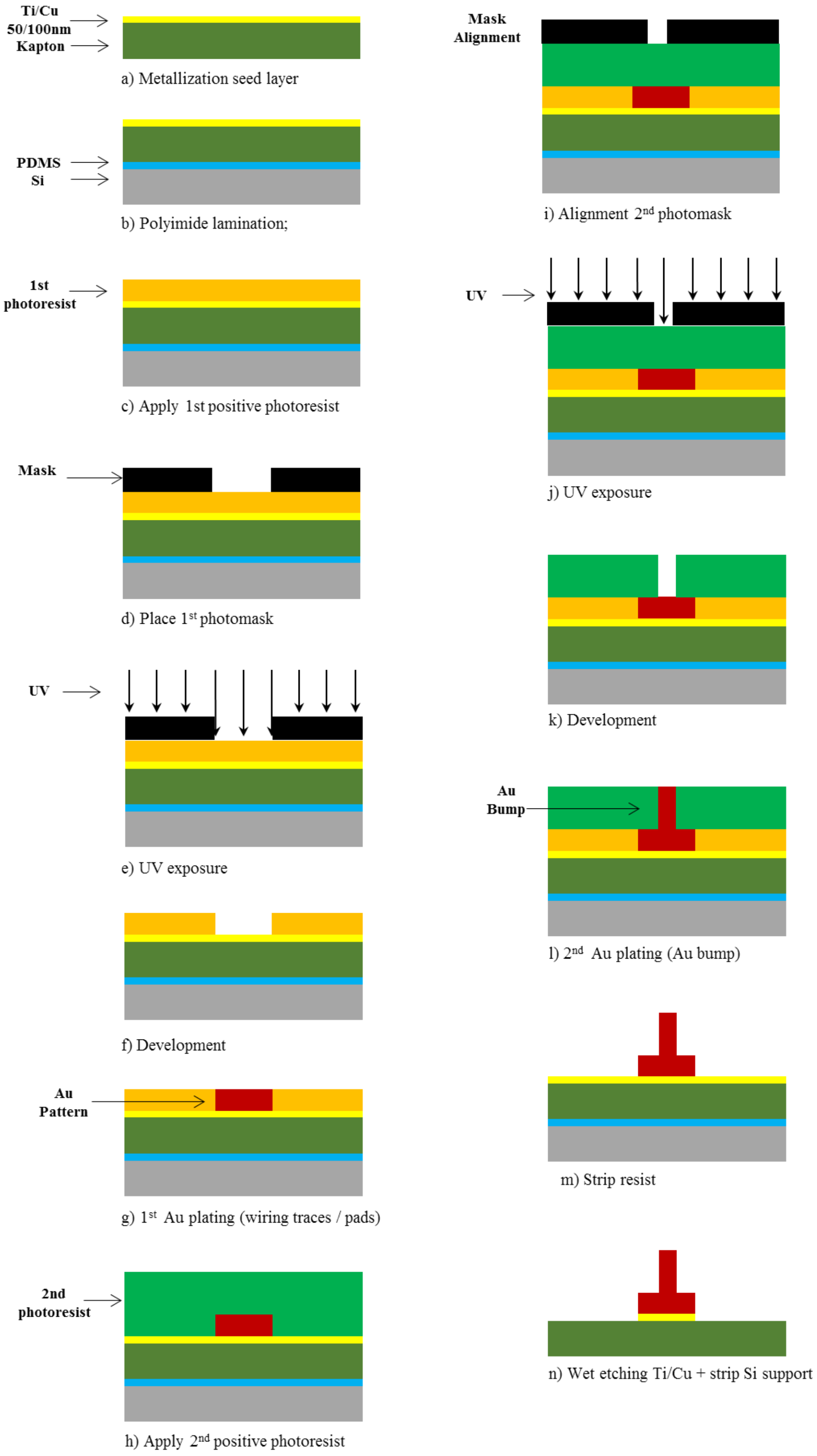


Figure V.21: SEM photo of a cross opening of 40 XT on Kapton.

V.4.2 Electroplating process

The electroplating process on test boards for bump forming were fabricated as following (see Figure V.22):

a) First, thin adhesion layers of seed layer titanium (50 nm) and copper (100 nm) were deposited onto a 4-inches Kapton wafer to act as an adhesion layer and a plating base, respectively.
b) Lamination of Kapton on PDMS-Si support carrier.
c) ~ f) A positive photoresist (ECI 3012) was the spin-coated onto the wafer and patterned to form a 1.1-µm-deep plating mold with a receipt of speed/acceleration/time as 3600 rpm / 5000 rpm. s^{-1} / 30 seconds.
g) The mold was filled with gold to a depth of 1 µm to form the wiring traces.
h) After stripping the 1st photoresist, a thicker photoresist layer (AZ 40 XT) was applied with a thickness of 40 µm. Generally, higher resist film thickness can be attained with lower spin speeds, but at low spin speed, the edge bead increases, and the resist film homogeneity decreases. So a suited spin profile is start with 1400 rpm / 100 rpm. s^{-1} / 30 seconds follow by a high spin 3000 rpm / 3000 rpm. s-1 for a short time (few seconds) to suppress the edge bead.
i) Soft bake on a hotplate with a heating profile: from 65°C to 105 °C during 2 minutes, then from 105°C to 126 °C during 2 minutes, finally stay at 126 °C during 3 minutes.
j) UV exposure (405nm) with MA 150 aligner (intensity: 20 mW/cm^2) during 39 seconds. PEB on a hotplate with a heating profile: from 90°C to 105 °C during 1 minute, then stay at 105°C during 80 seconds.
k) Development for approximately 2 minutes will remove the exposure part to form a mold for the connection bumps.
l) Electroplating of gold to a depth of 30 µm to produce the connection bumps.
m) ~ n) After stripping the 2nd photoresist, and removing the exposed areas of the seed layer (Ti/Cu) by wet etching, the wafer was ready to use.


Ti/Cu
50/100nm
Kapton
PDMS
Si
1st
photoresist
Mask
UV
Au
Pattern
2nd
photoresist
Mask
Alignment
UV
Au
Bump

a) Metallization seed layer

b) Polyimide lamination;

c) Apply 1st positive photoresist

d) Place 1st photomask

e) UV exposure

f) Development

g) 1st Au plating (wiring traces / pads)

h) Apply 2nd positive photoresist

i) Alignment 2nd photomask

j) UV exposure

k) Development

l) 2nd Au plating (Au bump)

m) Strip resist

n) Wet etching Ti/Cu + strip Si support

Figure V.22: Fabrication sequence of electrodeposition.

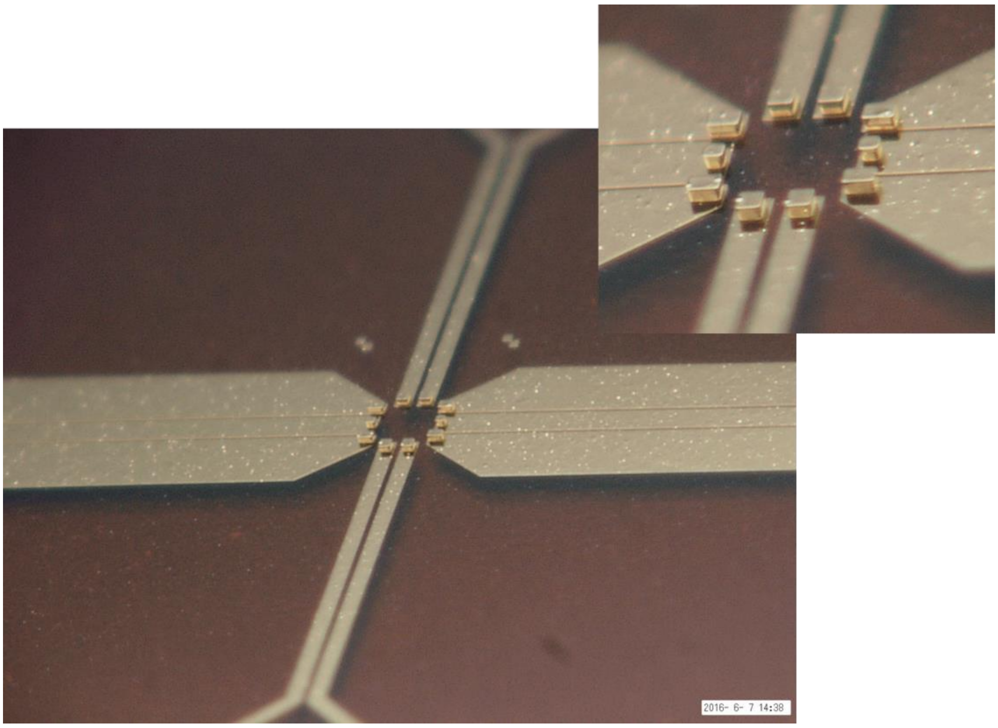


Figure V.23: Realized 30-µm-height Au bump on Kapton.

V.4.1 Reliability test

The same DC test using 4-point probes and daisy chain methods as described in V.3.1.1was performed, no practically problem was observed. Then the RF test with LNA dummy mounted on Kapton was also performed.

As mentioned in chapter V.3.1.2, we need to find a solution to postpone the real LNA chip regarding its size and aspect ratio. In the left picture of Figure V.24, one can see the LNA block is right in the bottom right corner of the 65nm CMOS chip, so we decided to cut the whole chip in two in order to have more space for adhesive dispensing. The corresponded LNA dummy chip on glass AF32 is presented in the right photo of Figure V.24.

The non-conductive adhesive polymer resin EPO-TEK 353ND-T is needle-dispensed on the Kapton as shown in Figure V.25. the very first dummy chip was mounted on Kapton, but it is leaning to one side (see Figure V.26) due to the force applying. After several test, the dummy chip was successful mounted and keep a non-leaning configuration.

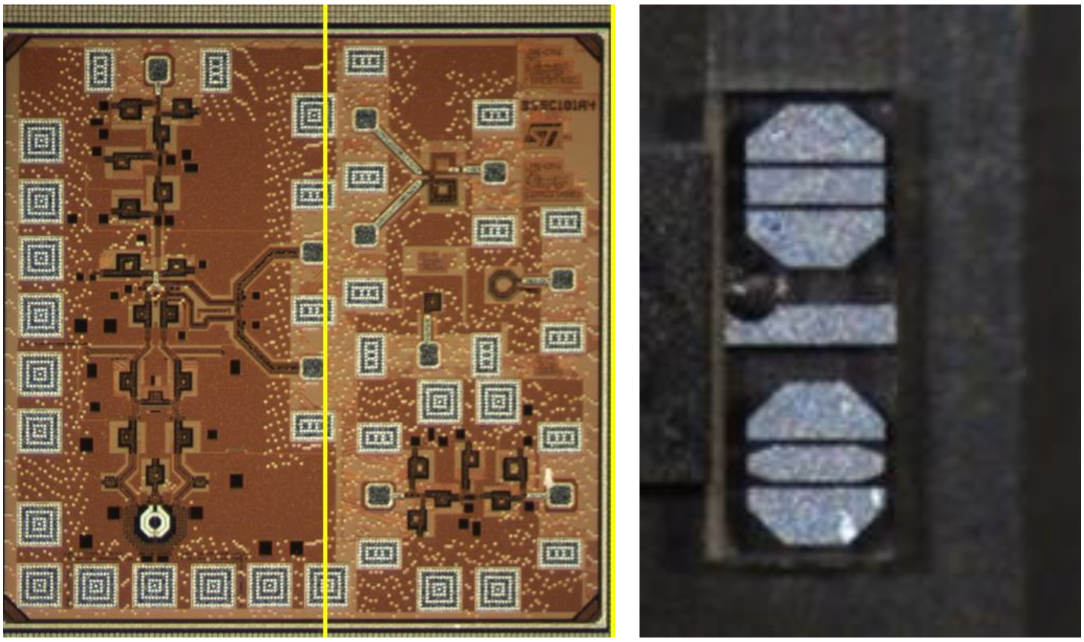


Figure V.24: 65nm CMOS chip contains LNA block (left) and LNA dummy on glass (right).

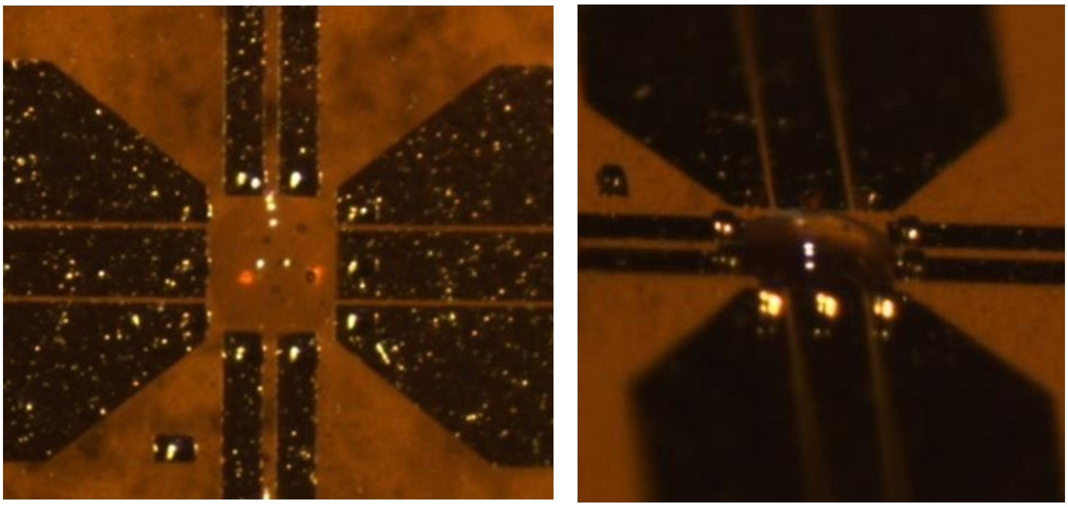


Figure V.25: Needle-dispensed adhesive polymer resin on Kapton.

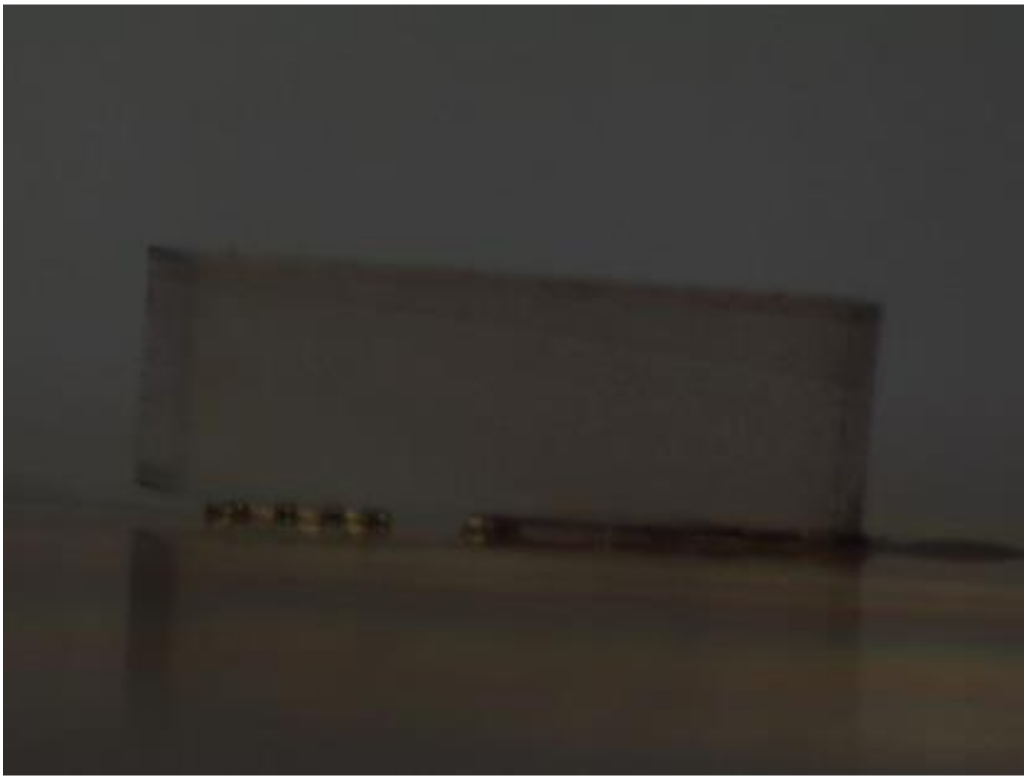


Figure V.26: Leaning LNA dummy mounted on Kapton.

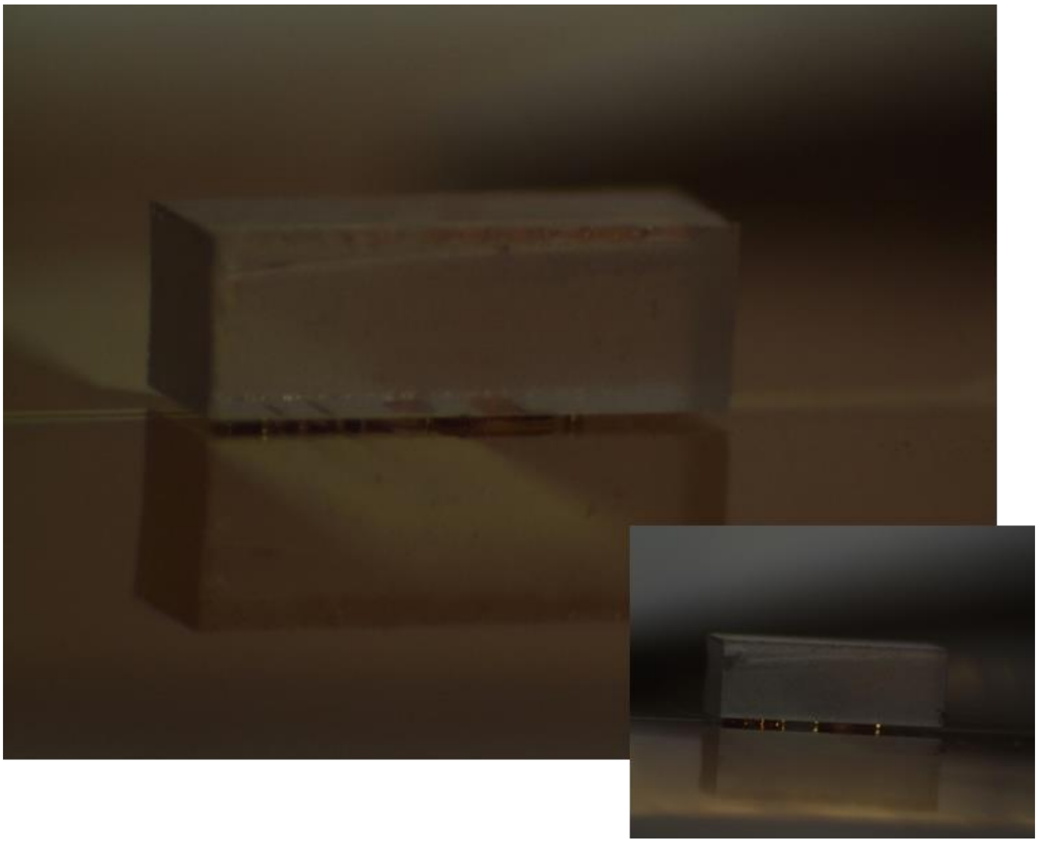


Figure V.27: Non-leaning LNA dummy mounted on Kapton.

But the RF tests on these non-leaning LNA dummy chips are not satisfying, half of the contact pads were open circuited in the daisy chain test, so we decided to investigate the reason of this poor interconnection. The failed dummy chips were removed from the Kapton structure, one can see in Figure V.28, a comparison of Au bumps before and after the NCA flip chip process. In fact, unlike the Au stud bump, which has a short protruding ductile fracture tip on the top of the ball, the Au bumps formed by electroplating on Kapton substrate have a flat top, and they cannot in contact with dummy chip if there is non-conductive adhesive presented on the surface of Au bump.

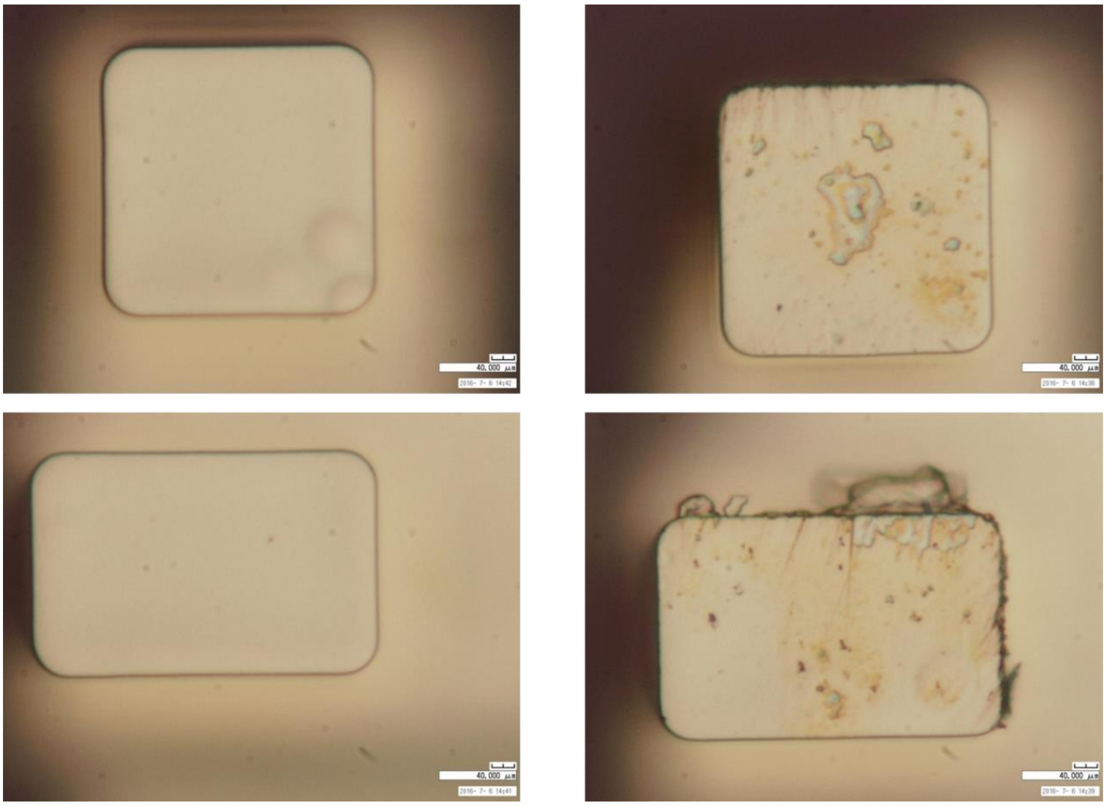


Figure V.28: Au bumps before (left) and after (right) NCA process.

As shown in Figure V.29, the difficulty of deposition the non-conductive adhesive on Kapton is that we can only have an area less than 240 µm × 250 µm to operate, it is nearly impossible to prevent the non-conductive adhesive flow onto the Au bumps once the chip is in contact with the Kapton structure.

To work around this problem, the first option is, first assembly the chip onto the substrate, then dispense the underfill between them, but our chip is so small that the syringe contains underfill cannot have access in a vertical position, but it may work if we can raise the chuck and then inject the underfill [60]. Unfortunately, the flip chip machine FC150 we used do not have this option.

Another solution is to deposit a photosensitive adhesive polymer on Kapton, BisbenzoCycloButene (BCB) resin is often used for these applications, but it requires an annealing temperature at 250°C, which is largely exceeded maximum temperature allowed when assembling a 65nm CMOS technology chip.

A start-up called 3DiS Technologies, which is spin-out company of LAAS-CNRS, they have developed a novel photoresist adhesive which only requires an annealing temperature at 105°C. This new photoresist adhesive may be the ultimate solution for our problem in the near future.

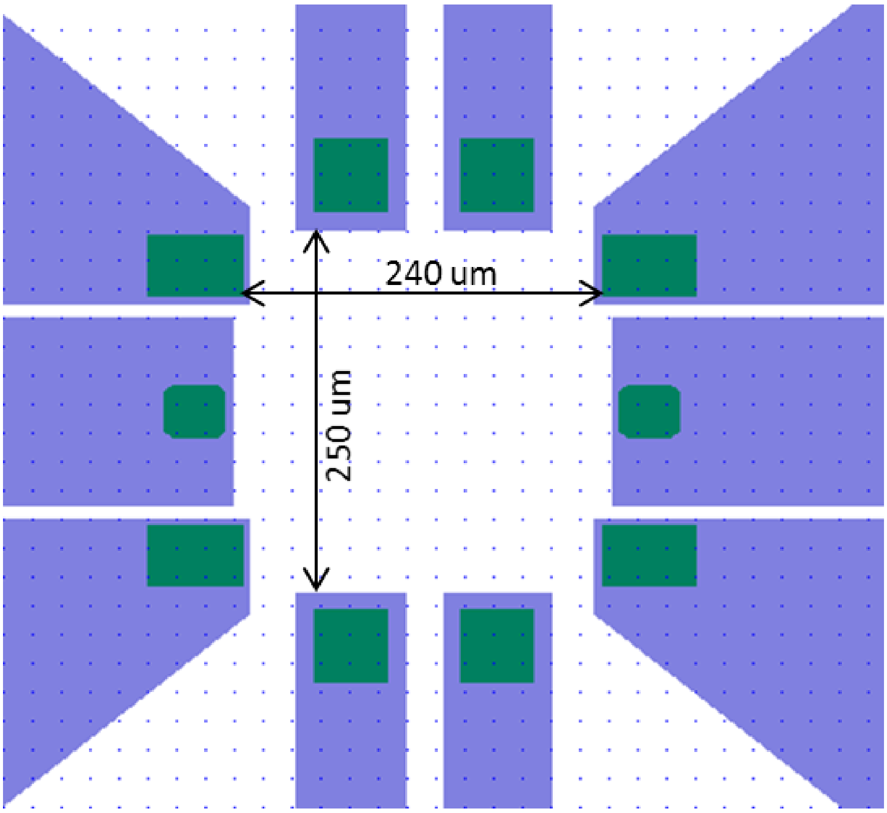


Figure V.29: Footprint of Kapton structure.

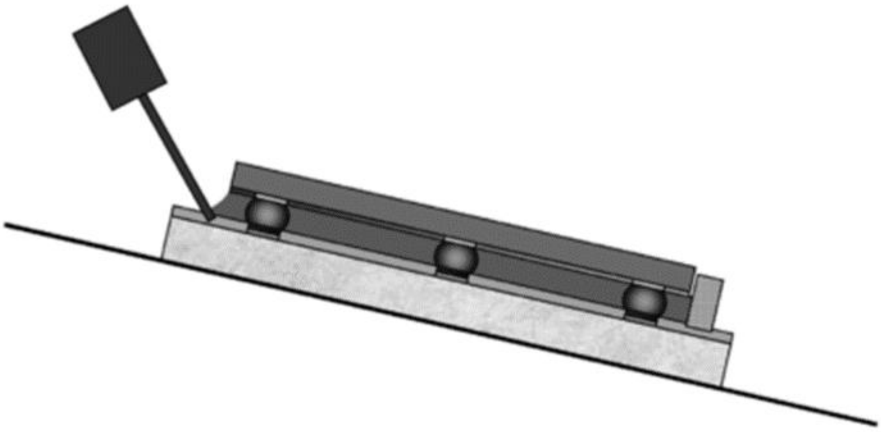


Figure V.30: Schematic of raised-die underfill, source [60].

V.5 Conclusion

In this chapter, flip chip test with Au stud bump was performed, DC and RF tests bring a proof of concept of such integration technique is feasible for V-band applications. The resistance of a single Au bump is measured as 10 mΩ, and an insertion loss of – 2 dB is observed for RF transmission.

Then a novel technique to form Au interconnection bump directly onto the flexible substrate by using electroplating process is presented here for the first time. And the optimization of thick resist processing is also discussed in this section.

The biggest challenge remains how to deposit a non-conductive adhesive polymer on a surface as small as 240 µm × 250 µm. We need find an alternative way to overcome this problem, like using a raised-die underfill configuration flip chip, or using a Low-K adhesive photoresist from 3DiS Technologies.

VI. General conclusions

Because of the fundamental importance of the dielectric parameters on RF circuit design, this work starts with characterization of Kapton film followed by extensive antenna performance investigation. The different passive technological approaches to realize adequate passive circuits and flip chip process by in this work, are tested and validated by the measurement results.

The first part of this thesis work has been focused on passive element implementation on flexible substrate. A 127-µm-thick Kapton polyimide film (type 500HN) was chosen as our flexible substrate due to its good RF and thermal properties, also because it has very good flexibility over a wide temperature range (-73°C to +400°C) and is resistant to many chemical solvents. The dielectric properties of Kapton, the relative permittivity ε_r and the loss tangent $\tan\delta$ were characterized by using a ring resonator method. Then a 60 GHz patch antenna with a gain of 5 dBi, and a bandwidth (return loss less than -10 dB) from 60.05 GHz to 61.8 GHz was designed, fabricated and measured on Kapton film. In addition, a standard humidity test performed in the V band. The experimental results demonstrate that the dielectric constant of Kapton increases as high as 15.6 % (up to 3.7 from 3.2 the initial value) and the dielectric losses increases with maximum 181% (up to 0.045 from the initial value of 0.016) when the Kapton structure were immersed in water after 48 hours. A limitation of the water absorption was also observed after 24 hours of the water immersion. Detailed photolithography processes used to manufacture the passive element circuits: the resonator, the antennas and the rectennas were tested and validated for the applications from several GHz up to 94 GHz. A quite good concordance between the simulations and the measurements is observed, which proves the reliability and reproducibility of such process technique. Furthermore, for a high-volume application like the node deployment of Wireless Sensor Networks (WSN), wafer cost reductions can significantly lower the total cost per node and became comparable to the cost of inkjet. The main advantage of the photolithography is that it can offer us the best resolution and the compatibility with other process like Au bump forming using electroplating.

The second part of this thesis is on heterogeneous integration of WSN node with flip chip technique, 60 GHz dummy circuits were successful mounted and measured on

Kapton with Au stud bumps. A novel technique to form Au interconnection bump directly onto the flexible substrate by using electroplating process is presented here for the first time. The main challenge is how to deposit a non-conductive adhesive polymer on a surface as small as 240 µm × 250 µm on Kapton. Alternative methods to overcome the adhesive problem have been proposed, like using a raised-die underfill configuration flip chip, or using a Low-K adhesive photoresist from 3DiS Technologies.

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List of publications

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- Z. Yang, A. Takacs, S. Charlot and D. Dragomirescu., “Flexible substrate technology for millimeter wave wireless power transmission”, Wireless Power Transfer, Volume 3, Issue 1, March 2016, pp. 24–33. Cambridge University Press 2016.

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