Contribution to the development of massively parallel radio frequency SoC architectures in advanced CMOS technologies

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Contribution au développement d'architectures SoC radio fréquences massivement parallèles en technologies CMOS avancées

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Contents

Introduction

Motivation and objectives

Parallel radio reception stands for a system capable of extracting, from the electromagnetic spectrum, more than one signal data stream, carried by different and arbitrary distributed carrier frequencies. This definition can be extended to massive parallel reception, where the system purpose is to receive a large number of channels. Behind this definition, we can recognize some well known applications:

- Digital TV reception (terrestrial, satellite or cable) where a hundred of programs are transmitted in a 1 GHz band.
- Internet Of Things (IOT), where a sensor node must wait for signals coming from different relays.
- Cellular communications, where LTE (4G) standard uses aggregation of carriers, which may be located in different frequency bands, to increase the data-rate. 5G standards will even push this principle further, enabling the aggregation of non exogenous signals (WiFi and LTE, mmW and RF ...)[1], [2].

Of course, when addressing massive parallel reception, energy efficiency and monolithic integration constraints have to be fulfilled:

- Energy efficiency, because solution must be compatible with portable devices.
- Monolithic integration for cost and volume constraints. This monolithic integration has to be compliant with a System On Chip approach (SOC), meaning that the technology must be an advanced CMOS.

Finally, parallel reception is already linked to hot research areas:

- Re-configurable radio receivers or Software-defined radio (SDR).
- Wide band reception.

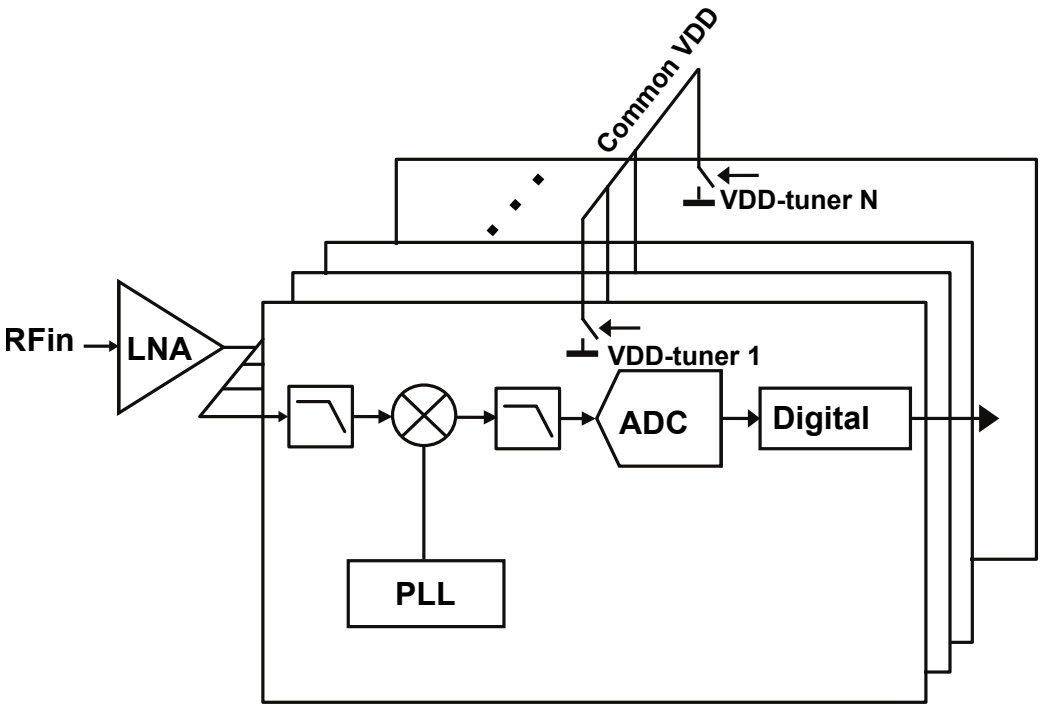

FIGURE 1: N RF traditional receivers in parallel.

Design challenges

The straight forward way to tackle massively parallel reception would be to put in parallel as many RF traditional receivers as needed (Fig. 1). With the latter solution, the total signal would be first amplified by a common Low Noise Amplifier (LNA), then every single receiver would down-convert its wanted signal to baseband, where it undergoes filtering and digitization through a baseband Analog-to-Digital Converter (ADC).

However, the integration of multiple uncorrelated clocks on the same chip leads inevitably to some issues:

- In case of a monolithic integration, the harmonics of all operating VCOs and all the spurs of the fractional dividers will couple to LNA input. The number of these spurs will become too large to consider interference mitigation schemes.
- Having multiple Voltage Controlled Oscillators (VCO), on the same chip, with frequencies in the same range, will produce Voltage Controlled Oscillator (VCO) pulling, degrading reception [3]–[6].

- LNA and mixer, which have to handle the full RF band, will exhibit a poor linearity degrading the overall Signal-to-Noise Ratio (SNR).
- High area, mainly for clock generation.

To conclude this section , we can state that monolithic integration of parallel receivers will force to solve two challenges:

- Generation of arbitrarily distributed clock frequencies while keeping a "reasonable" amount of spurs.
- Management of the wide band aspects, meaning low harmonic mixing and high linearity constraints.

Thesis outline

In chapter 1 we show the main existing solution solving part of massively parallel reception challenges. In chapter 2, the N-path receiver is presented along with the problems it faces when used in a massively parallel configuration. Some solutions to these problems are then provided and a massively-parallel-friendly solution based on N-path is finally proposed.

Power efficiency comparison, with respect to the number of received channels, between a traditional solution and the latter N-path based solution will be done in chapter 3.

In chapter 4, a circuit, demonstrating the feasibility of the proposed architecture and its compatibility with massive parallel reception is proposed. The details of the implementation as well as simulations and measurements results are discussed.

Finally, a conclusion and future work in the last chapter.

Chapter 1

State of the art of massively parallel reception

1.1 Introduction

Massively parallel reception started to be an area of interest only in the past few years, it combines two difficulties:

- Designing a reconfigurable radio receiver (which was already targeted in SDR researches).
- Managing the cohabitation of a large number of such a receiver on the same chip (Spurs, Area, energy efficiency ...).

In this chapter, we will report studies addressing at least one of these aspects, describe principle involved and point limitations.

1.2 Digital-to-Analog Converter+Direct Digital Frequency Synthesis in the reference path of PLL

One partial solution to the massively parallel reception is the "Digital-to-Analog Converter (DAC)+Direct Digital Frequency Synthesis (DDFS) in the reference path of Phase Locked Loop (PLL)" [7]. This solution exploits a DAC+DDFS combined to a Band Pass Filter (BPF) at the PLL reference path. This DAC+DDFS+BPF combination, allows to generate any wanted low frequency clock, that can be used in the reference path of an integer frequency-divider PLL. The frequency flexibility is therefore obtained by the combination of a tunable reference frequency and integer frequency-divider, and not through the combination of a fractional frequency divider and a fixed frequency reference as usually done. Thus, we can afford a wide range flexible PLL without using a fractional divider that comes inevitably with interferences. Therefore, if compared to a classical solution that includes

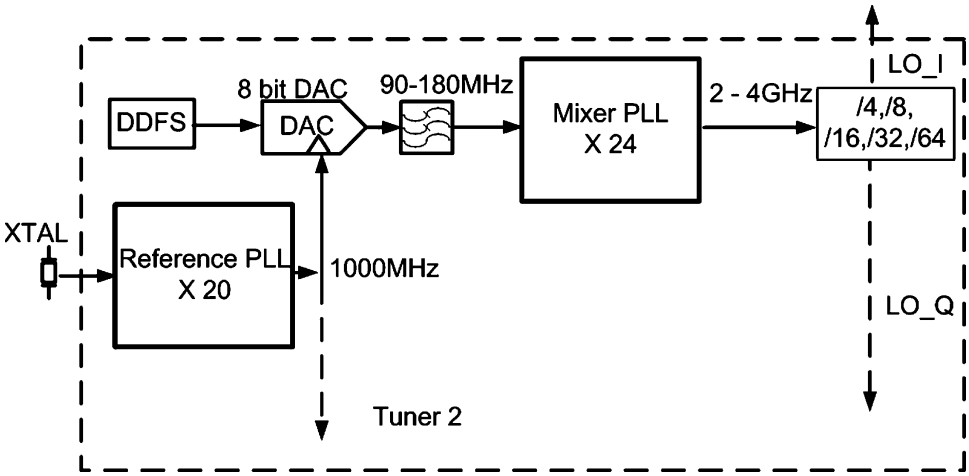

FIGURE 1.1: F. Gatta [7] LO generation block.

fractional dividers, this solution is more robust to interferences, even if it still suffers from the VCO harmonics that will couple to other VCO and may lead to VCO pulling.

This solution proposes a novel idea to get rid of fractional dividers and thus reduce the amount of spurs, but it is only a part of the problem: one PLL per receiver is still needed, and this will impact circuit area. Moreover, having a sine-wave reference, involves inevitably the use of a mixer-based PLL, instead of the traditional, low phase-noise, Charge Pump based PLL.

1.3 A Direct Digital Frequency Synthesis driving segmented Gilbert mixer

The figure Fig 1.2 present a DDFS driving a segmented Gilbert mixer [8]. This solution exploits a 10 binary weighted Gilbert mixer set, realizing a mixer-DAC behavior. This mixer-DAC is driven by a 10 bit DDFS. Many parallel receivers can thus be put in parallel while still being driven by a single analog-clock, which prevents clock interference problems from occurring.

The Direct Digital Frequency Synthesis (DDFS) is generally based on a Static Random Access Memory (SRAM), in which are stored the samples of a walking sine-wave, thus the interferences that a DDFS can cause are very low compared to the ones that can be created using an analog-clock. Indeed the interference inter-analog-clocks are mainly due to:

- the use of an inductor in the VCO that will produce an electromagnetic field that could disturb other working VCO's inductors, known as VCO pulling [3].

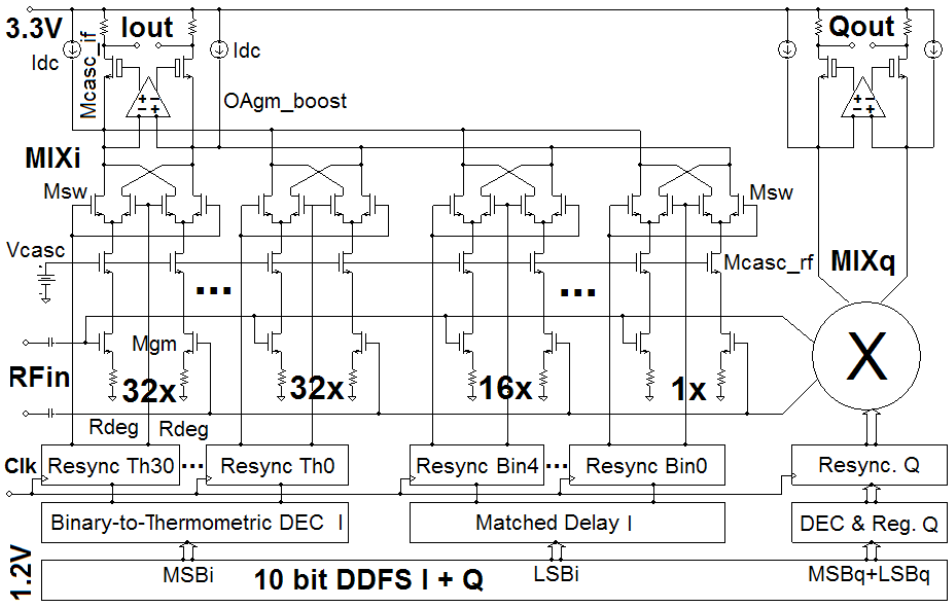

FIGURE 1.2: A. Maxim [8] receiver architecture.

- the high current drawn by the frequency dividers, at Local Oscillator (LO) frequency, that transform to voltage drop at the different VDD nodes of the circuit due to the VDD wire resistance. That can also disturb other working VCO's that will see a variation in their own VDD and can cause VCO pulling [3].

A DDFS do not have an inductor, preventing it from the first source of interference. The current drawn by the DDFS would be at the sampling frequency and not at the sine wave LO, providing to the DDFS based receivers much more robustness to interference.

Drawback of this solution is the difficulty to obtain sufficient linearity. No RF filtering is present, meaning that LNA output and mixer input signal is the sum of all signals present at the antenna and thus both will need to be extremely linear. This linearity constraint will translate in current consumption: The circuit presented in the paper consumes 500 mW for a single I/Q receiver. This solution proposes to generate the LO signal from a DDFS, which is a good solution to avoid spurs coming from LO path, but segmented Gilbert-cell approach make it incompatible with massive parallel reception.

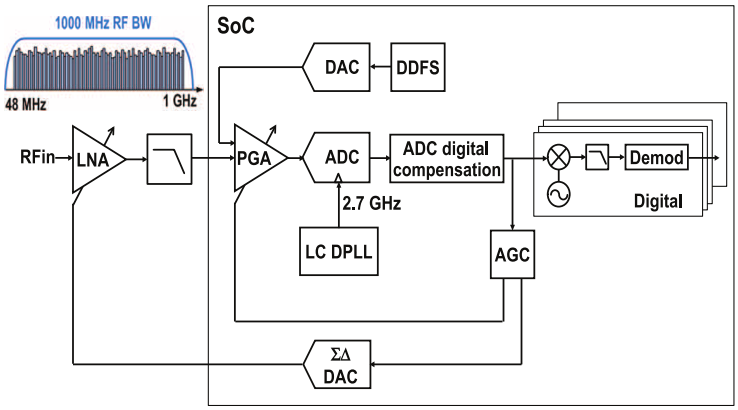

FIGURE 1.3: Full spectrum capture architecture [9].

1.4 Full Spectrum Capture

The Full Spectrum Capture (FSC) shown a in fig. 1.3 is an ADC-first receiver, that digitizes the full antenna spectrum. Every received channel is then processed digitally through a Digital Channel Selection (DCS) block. This architecture solves the need of a clean LO-generation by using a unique clock and DCS blocks; mixing in digital with a DDFS helps overcome the harmonic mixing problem (harmonic mixing level can be lowered by properly selecting the number of bits). This solution simply translates the analog processing blocks to the digital domain, giving them an ultimate flexibility. Moreover, a digital filter or mixer block consumes less power compared to its analog counterpart with the same performances. However, the power consumption reduction at the digital blocks is replaced by a very high power consumption of the ADC[1].

FSC receiver was long considered as a solution for cognitive radio. It was first introduced in [10] (Mitolla sofware radio), but the high bandwidth and high resolution ADCs it required were impossible to achieve at the time. For example, digitizing the frequency band from 800 MHz to 5.5 GHz, where all of today's cellular and WLAN channels lie, will require a 12 bit, 11 GS/s ADC [11].

To conclude, the challenge in the analog design becomes an ADC design challenge (example: 12 bits and $f_S = 2.7$ GHz for DOCSIS). This solution suffers from drawbacks:

- The consumption remains almost the same, for whatever number of really used channels.

[1] this is a general remark for receivers architecture, that digital blocks consume less than RF ones, but the high power consumption of the ADC that had to digitize the whole spectrum, binds us to use RF pre-processing of the signal

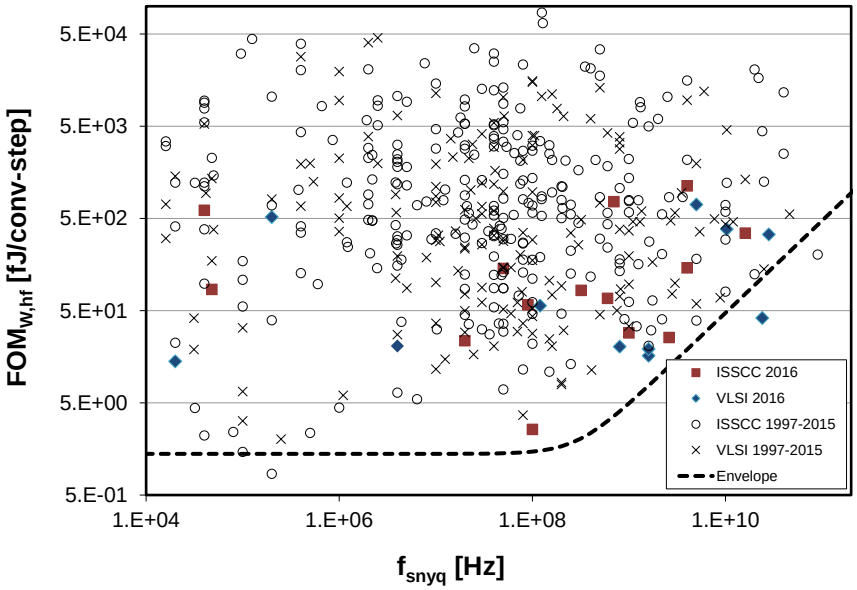

FIGURE 1.4: B. Murmann ADC survey [12].

- If the standard only uses some portions of the spectrum (cellular as an example), efficiency reduces (as the power consumption remain the same).
- The power consumption grows in a quadratic fashion with sampling frequency [12] (fig. 1.4 for frequencies above 100 MHz and thus the maximum signal frequency (the sampling frequency must be two time higher than the maximum signal frequency).

1.5 Conclusion

None of the presented solutions will be the ultimate solution for massive parallel reception. FSC has advantages, but can be considered relatively power hungry when only few channels are really used at the same time or when the useful spectrum is sparse. The two other solutions do not have this issue, but both are based on traditional (mixer based) receivers capable of working on a wide band (and thus without RF filtering) with a large quantity of blockers. This will put a linearity constraint on the mixer that will be solved with additional current consumption. To get rid of this problem, solution must provide some RF (before mixer) filtering. This characteristic is provided by N-path receivers, motivating to start the seek for a new architecture with detailed N-path study.

Chapter 2

G_m N-path based receiver genesis

2.1 Introduction

In the last chapter we presented the state of the art for parallel receivers, where the FSC drawbacks motivated us to look for an alternative receiver architecture, of which power consumption scales with the number of received channels and which includes RF filtering. One promising architecture that include RF filtering along with power and area efficiency is the N-path receiver. In the first section, we present the N-path filter and the N-path receiver along with its drawbacks, that are mainly the input impedance and the harmonic mixing. Then in the second section, an intuitive way to calculate input impedance is presented, and some solutions to get rid of the input impedance drawback are presented. one solution to the input impedance problem is to combine a G_m block to the N-path receiver, presented in the section 2.3. This G_m N-path receiver still suffer from harmonic mixing, which can be solved by the use of a G_m N-path based mixer-DAC that is presented in section 2.4.

2.2 N-path based receiver presentation

2.2.1 N-path filter definition

The N-path filter is a BPF circuit, illustrated in fig. 2.1(a) [13], where the first set of switches realizes a multi-phase passive mixer that down-converts the input RF signal to baseband. Then, this down-converted signal is low-pass filtered through the LPF. Finally the filtered signal is up-converted through the second set of switches. This implements, when both pairs of switches are driven with the same frequency (LO frequency) a BPF with a center frequency of LO and a 3 dB bandwidth equal to twice the BPF bandwidth. The main benefit of this architecture is that the cut off frequency of the Low

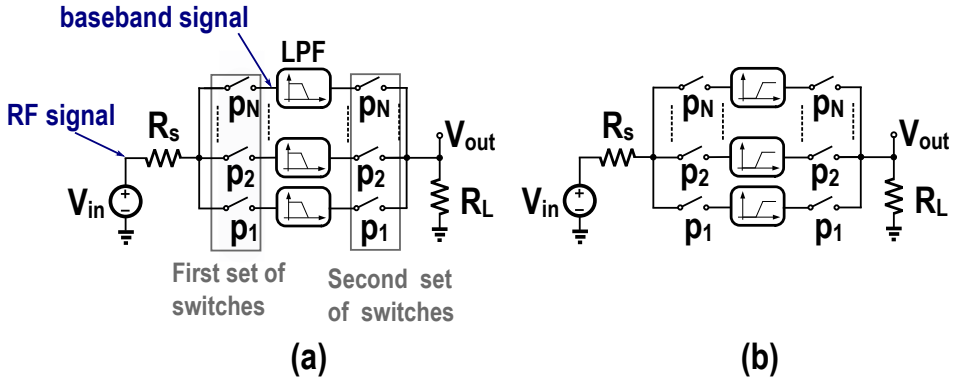

FIGURE 2.1: N-path architecture: (a) BPF (b) BSF

Pass Filter (LPF) is independent of the mixing frequency, resulting in a high selectivity BPF (high Q)[1]: $Q = \frac{f_{\text{mixer}}}{\Delta f}$ where f_{mixer} is both down-conversion and up-conversion frequency and Δf is the full width at half maximum of the filter transfer function (in this case equal to 2 times the cut off frequency of the LPF). For example, using a 1 MHz cut off frequency low pass filter, along with a 1 GHz mixing frequency, result in a $Q = 500$ BPF.

Similarly with BPF, fig. 2.1(b) [13] shows an N-path Band Stop Filter (BSF). It follows the same principal of the BPF, except that instead of using a LPF to pass the low frequency signals, it uses a High Pass Filter (HPF) to pass the high frequency signals, realizing a BSF behavior.

An implementation of an N-path BPF [13] is illustrated in fig. 2.2(a), where a simple capacitor is used to realize a LPF when combined to the switch and source resistors. In this implementation, the second set of switches are not needed, because by nature, a passive mixer is bidirectional and thus a single mixer can play both roles: down-mixer (from RF to baseband) and up-mixer (from baseband back to RF).

In a passive mixer implementation, it is forbidden to have the switches of two baseband sections on at the same time (this would short-circuit both and thus kill the filtering function). For this reason, square-LO signals must be non overlapping and thus will have a duty cycle of $1/N$. The mixing signals are illustrated in fig. 2.2(b) along with its spectral decomposition (the dashed curve): this $\frac{100}{N}\%$ duty cycle signal contain on top of the fundamental f_{LO}, all its harmonics except $k\,N\,f_{\text{LO}}$.

The N-path can be intuitively seen as a passive mixer that translates the low-pass behavior of the RC network to create a band-pass behavior around the switching frequency, as shown in fig. 2.2(c), where the LPF

[1]The quality factor (Q factor) is a dimensionless parameter that characterizes a resonator's bandwidth relative to its center frequency

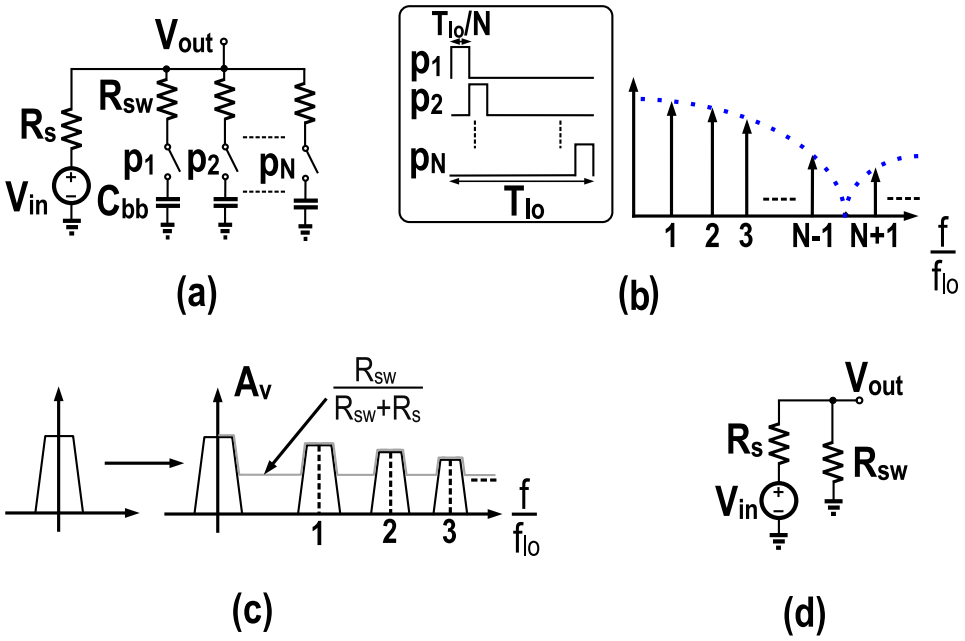

FIGURE 2.2: (a) N-path implementation (b) Mixing signals: time and spectrum BPF (c) Transfer function (d) Equivalent circuit for out-of-band signals

transfer function is being translated around every one of the mixing signal spectral components. The input signals see either a high or low impedance, depending on its frequency as follow [14]:

- An input signal at f_{LO} or its harmonics sees a LPF behavior (or high input impedance as shown in fig. 2.2(c)), where the baseband capacitor holds the mean value of this in-band signal.
- An input signal at a different frequency sees only the switch resistance R_{sw}(or low input impedance as shown in fig. 2.2(c)), resulting in a simple voltage divider, as shown in fig. 2.2(d).

N-path filters are tunable low-power and low area filters, where the center frequency is totally tunable and independent of the filter sharpness. Indeed, the N-path filters present very good performances compared to other RF filters or receivers topologies[2] [15], making this architecture suitable for receiver architecture previously targeted in chapter 1.

2.2.2 N-path filter used as a receiver

An N-path receiver is illustrated in fig. 2.3. It has the same implementation as fig. 2.2, with $N = 4$ and considering the voltage at the capacitance nodes

[2]We only consider tunable and low power low area topologies

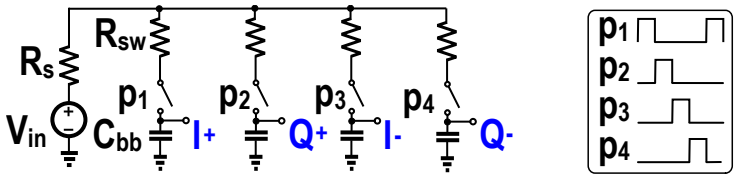

FIGURE 2.3: N-path receiver

as output. This implementation benefits of the properties of N-path filter (filtering), while taking outputs on capacitors will bring baseband signal out of the circuit. On the other hand, the choice of $N = 4$ will drive us towards 90° shifted LO signals. By properly choosing the outputs, one can construct in-phase differential and quadrature signals. An image reject mixer can thus be implemented simply by digitizing I and Q and calculating, in digital domain the $I + jQ$ function.

The N-path has multiple advantages when used as a receiver, namely:

- Low power consumption: the circuit include both I and Q at the same time, using passive mixer and passive LPF, where the only power consumers are the clock generation block and the different switches drivers (not shown in the fig. 2.3).
- High linearity: the N-path implementation exhibits two major advantages in term of linearity:
  - Passives mixers, as they only use the transistors in ON or OFF modes are inherently very linear.
  - The fact that input impedance is low out of the bands is also a major advantage. All blockers will see a low impedance, resulting in a low voltage swing on the input, relaxing linearity constraints on switches and active devices, if any.

The N-path also have some disadvantages when used as a receiver, and some when used as parallel receivers:

- Harmonic rejection: the N-path down-converts the RF signals present at the fundamental frequency along with its harmonics, which results in the superposition of signals present in the antenna spectrum at f_{LO} harmonics, with the wanted signal.
- Low selectivity: selectivity of the N-path shown in fig. 2.2(a) cannot exceed $\frac{R_{sw}}{R_{sw}+R_S}$ (voltage divider mentioned above, for input frequencies different from the mixing frequency).

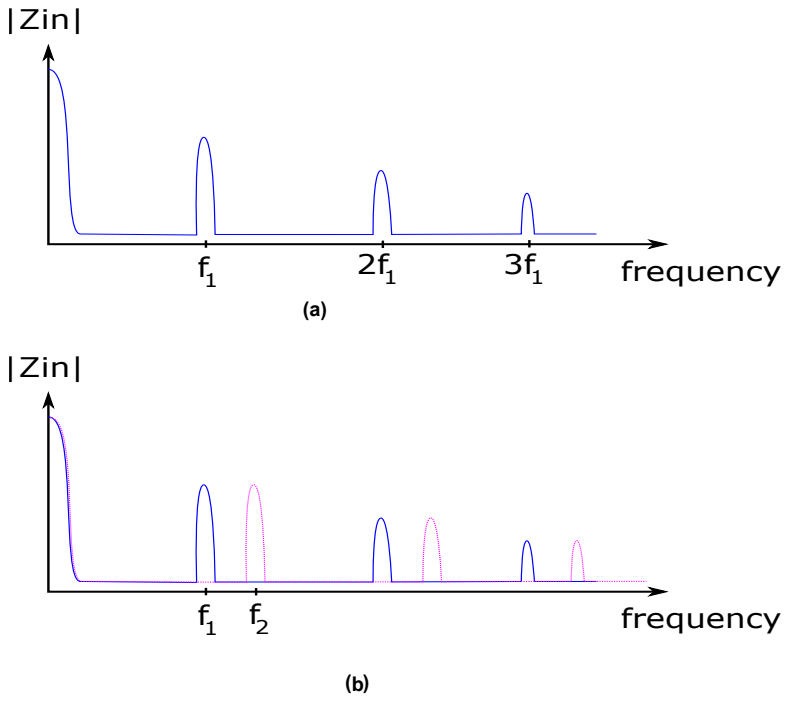

FIGURE 2.4: N-path input impedance of: (a) single N-path (b) 2 parallel N-paths at 2 different frequencies

- N-path input impedance: input impedance of a single N-path filter is depicted in fig. 2.4(a), while in fig. 2.4(b), two parallel N-paths with two different center frequencies are depicted. At f_1 the first N-path have a high input impedance while the second N-path input impedance is very low: the second N-path acts like a shunt for the first one, around its receiving frequency. Putting two N-path receivers in parallel will thus cancel any signal present at the antenna.

We have three problems if we want to implement parallel reception with N-path filtering: harmonic mixing, selectivity and input impedance. N-path harmonic mixing and selectivity problems seems not that severe, and have been addressed and solved in [13], [16]. Input impedance become the bottleneck, that can be summarized as follow: it is obvious now that implementing parallel reception with N-path receivers built with simple RC filters, leads to shorting both receivers to ground, due to low out-of-band input impedance. Is there any other filter implementation that can solve this problem? In other words, can we, by carefully choosing the baseband filter, shape the N-path receiver so that input impedance becomes compatible with parallel reception?

For that study, a general analytic calculation of N-path receiver input impedance is needed. In next section, we will develop the input impedance

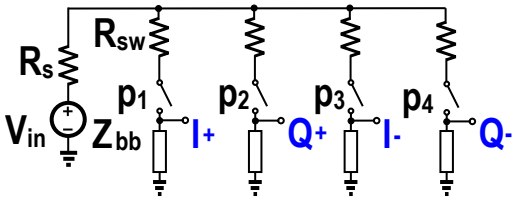

FIGURE 2.5: N-path receiver: general baseband impedance case.

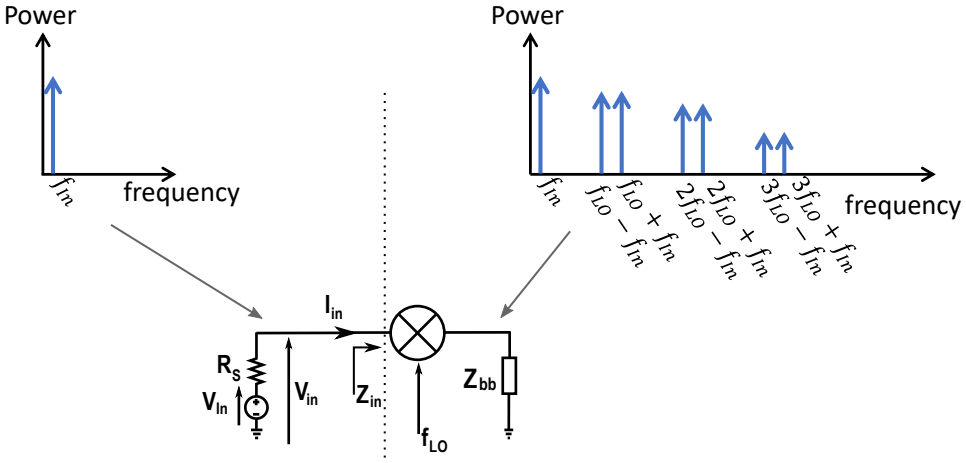

FIGURE 2.6: LTI N-path input impedance: general circuit

formula of a general N-path shown in fig. 2.5, where the capacitor was replaced by a general impedance, that could be replaced by capacitor, inductor, resistor or a combination of two or more of them. First we assume Z to be replaced only by a combination of inductors and resistors (where the N-path remains an Linear Time-Invariant (LTI) system), then in a second time we introduce an intuitive method to calculate capacitor based N-path input-impedance.

2.3 N-path filter input impedance calculation

2.3.1 Input impedance of Linear Time-Invariant N-path filter

For LTI N-paths input impedance calculation, we consider the circuit shown in fig. 2.6, which is a single path ($\frac{1}{N}$ of the N-path). Before the mixer, the input signal is a single spectral tone, that will transform after mixing with the $\frac{100}{N}$% duty cycle square-LO, to many spectral tones at $f_{\text{in}} \pm k\, f_{\text{LO}}$.

For this circuit we consider the power conservation equation 2.1, i.e. the input power is equal N time the power in one branch[3], which is the sum of the power of tones at $f_{\text{in}} \pm k\, f_{\text{LO}}$:

[3] The N branches are the same and do not overlap

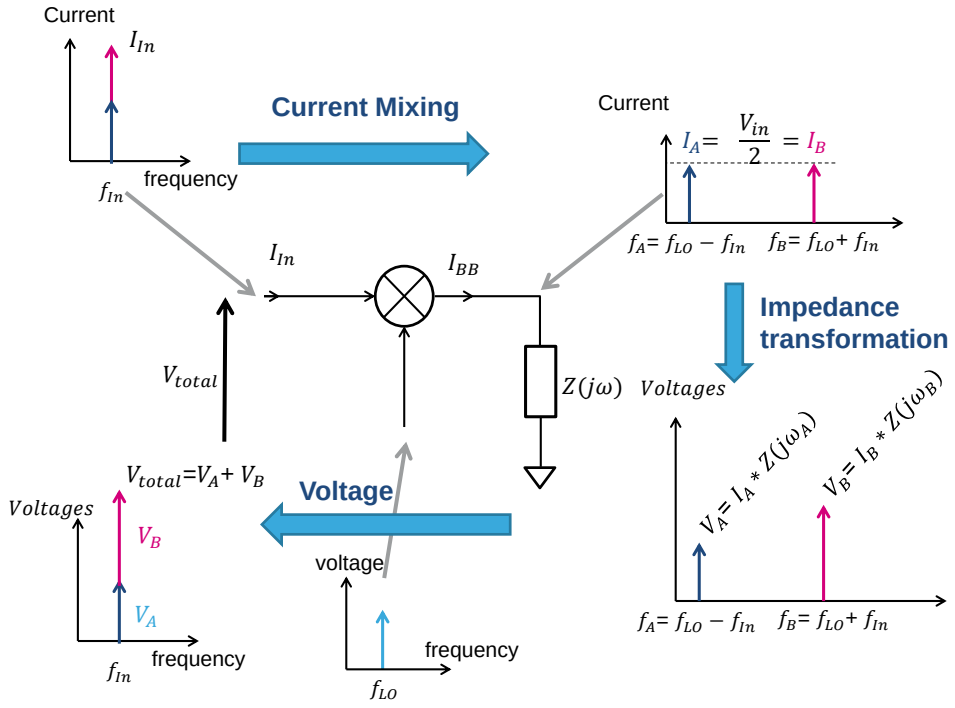

FIGURE 2.7: N-path mixer: current mixing

$$\begin{aligned} P_{\text{in}} &= N \cdot P_{\text{one path}} \\ &= N \cdot \sum_{k=0}^{\infty} P_{\text{BB},k} \end{aligned} \tag{2.1}$$

where $P_{\text{BB},k}$ is the power of the k^{th} tone in one branch.

This passive mixer is considered as a current mixer [13], meaning that it's the RF current that splits into many baseband currents, at different frequencies, following the LO signal Fourier decomposition. Then, this different currents are transformed through the baseband impedance to voltages which sum up to produce the output voltage, as shown in fig. 2.7 for a single RF tone mixing with a single LO-tone. In opposition a voltage mixer is shown in in fig. 2.8 for a single RF tone mixing with a single LO tone. In other words, due to mixing, we consider the input current that split in two equal tones, and not the RF voltage.

For a square-LO the RF current will splits in many baseband currents according to the square-LO signal Fourier decomposition (and it is not the RF voltage that split):

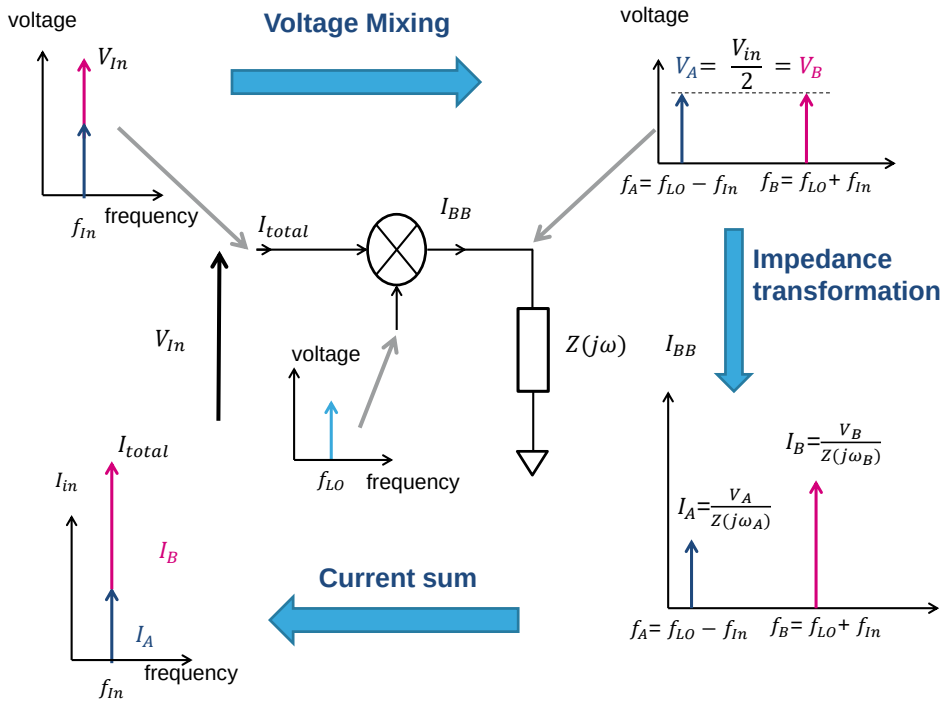

FIGURE 2.8: N-path mixer: voltage mixing

$$I_{\mathrm{BB},k} = \alpha_k \, I_{\mathrm{in}} \tag{2.2}$$

where α_k is the k^{th} coefficient of the LO signal one-sided Fourier decomposition[4].

The k^{th} baseband power expression $P_{\mathrm{BB},k}$ can be deduced from:

$$P_{\mathrm{BB},k} = I_{\mathrm{BB},k}^2 \, Z_{\mathrm{BB},k} \tag{2.3}$$

combining 2.1, 2.2 and 2.3 we get :

$$P_{\mathrm{in}} = N \, I_{\mathrm{in}}^2 \sum_{k=0}^{\infty} \alpha_k^2 \, Z_{\mathrm{BB},k} \tag{2.4}$$

P_{in} can also be expressed as $I_{\mathrm{in}}^2 \cdot Z_{\mathrm{in,LTI}}$, resulting in:

$$I_{\mathrm{in}}^2 \cdot Z_{\mathrm{in,LTI}} = N \, I_{\mathrm{in}}^2 \sum_{k=0}^{\infty} \alpha_k^2 \, Z_{\mathrm{BB},k} \tag{2.5}$$

[4]For a rectangular signal with amplitude A and duty-cycle d: $\alpha_k = \frac{2A}{k\,\pi} \sin(k\,\pi\,d)$

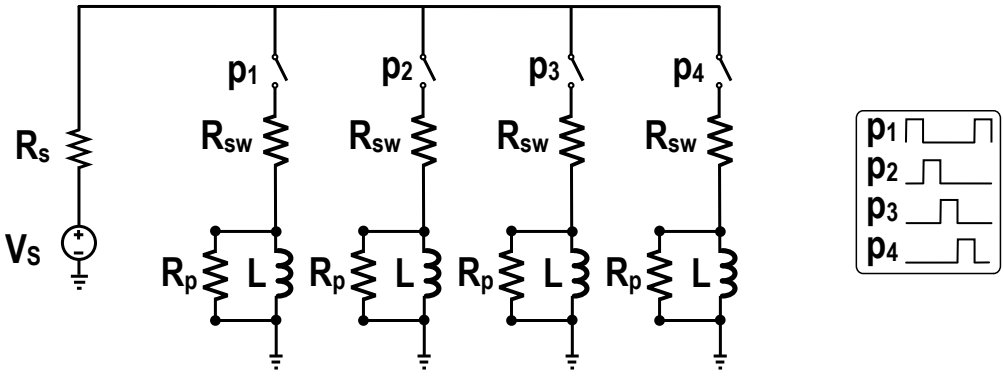

FIGURE 2.9: LTI N-path input impedance: baseband inductors

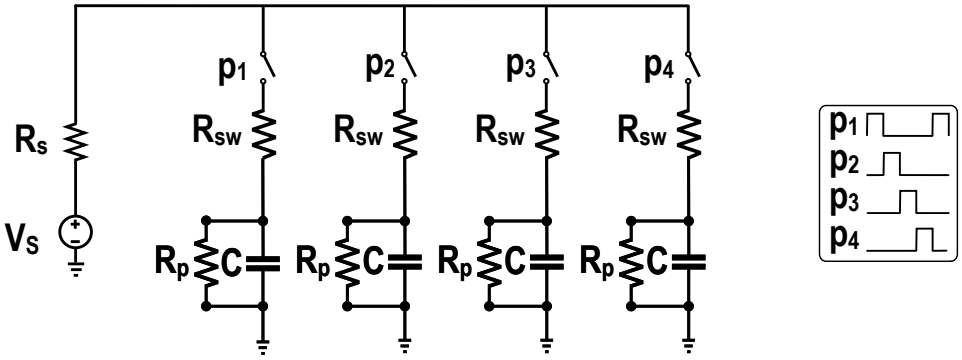

FIGURE 2.10: LTI N-path input impedance: baseband capacitor

Finally if we simplify by I_{in}^2, we get:

$$\boxed{Z_{\text{in,LTI}} = N \sum_{k=0}^{\infty} \alpha_k^2 \, Z_{\text{BB},k}} \tag{2.6}$$

The later formula has been tested for an inductive baseband impedance shown in fig. 2.9, where a parallel resistor R_p was added to limit the impedance increase over frequency of the inductor (adding a parallel resistor is a more realistic case, moreover it helps the Spectre RF simulator to converge). Then, both simulated (Spectre RF) and calculated (Matlab using eq. 2.6) input impedance are plotted in fig. 2.11, where $R_s = 50\,\Omega$, $R_{\text{sw}} = 20\,\Omega$, $L = 10\,\mu\text{H}$, $R_p = 10\,\text{k}\Omega$ and $f_{\text{LO}} = 1\,\text{GHz}$.

Note that when Z_{BB} is replaced by a resistor, the equation 2.6 simplifies to $Z_{\text{in}} = N \left(\sum_{k=0}^{\infty} \alpha_k^2 \right) R_{\text{BB}}$ where the parenthesis is equal to the LO amplitude, which is equal to $1/4$ for one path. Finally, for a resistive N-path, the input impedance is equal to:

$$Z_{\text{in,resistor}} = R_{\text{BB}} \tag{2.7}$$

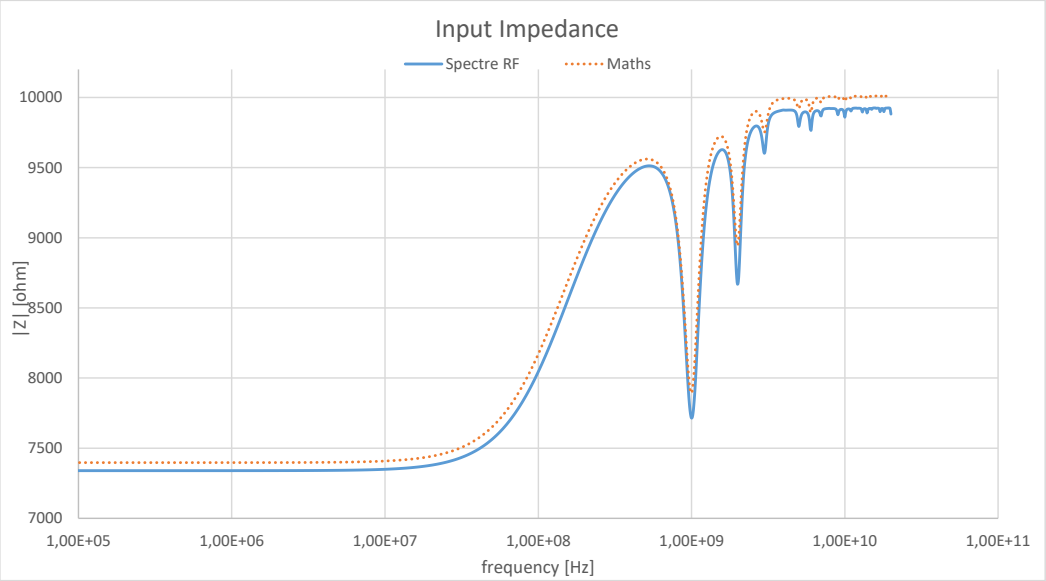

FIGURE 2.11: LTI N-path input impedance(simulation Vs calculus): inductors

Our model now being confirmed for LTI N-path, we tried the same formula for a capacitive baseband impedance N-path shown in fig. 2.10, and again both simulated (Spectre RF) and calculated (Matlab using eq. (2.6)) input impedance are plotted in fig. 2.12, where $R_s = 50\,\Omega$, $R_{sw} = 20\,\Omega$, $C = 100\,\text{pF}$, $R_p = 10\,\text{k}\Omega$ and $f_{LO} = 1\,\text{GHz}$. In this figure, we can see that the mathematical calculus done through formula (2.6) does not fit simulation, especially around the mixing frequency and its harmonics, i.e. showing that more current is flowing in the simulation than in the calculated one. This difference was expected due to the use of an LTI model for this Linear Time-Varying (LTV) N-path. In the next section, we will investigate the input impedance of an LTV model through calculating the later "extra floating current" when using an LTI model for calculating LTV N-path.

2.3.2 Input impedance of Linear Time-Varying N-path filter

For an input signal at the same frequency as f_{LO}, each capacitor will always see the same quarter of the input sine-wave, for every switch-on window. The capacitor will thus hold the mean value of this quarter sine-wave. The combination of switch resistance and source resistance then sees a voltage difference equal to the input voltage minus its mean value held by the capacitor, resulting in a current flow equal to this voltage difference over the sum of resistances, as shown in fig. 2.13. This current average is equal

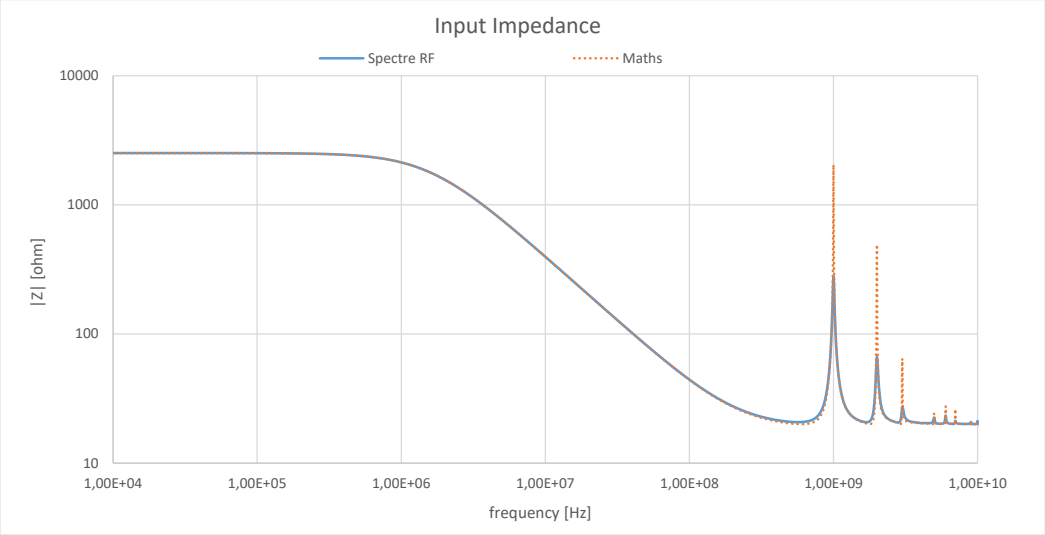

FIGURE 2.12: LTI N-path input impedance (simulation Vs calculus): capacitors

to zero, nevertheless it should be counted in the input impedance calculus, where the LTI model does not include the capacitor voltage "memory-effect".

The input impedance resulting from this current is calculated in the case of $N = 4$ (4-path) in Appendix. A and the input impedance value depends on the value of the harmonic following 4 cases:

Input impedance for $k = 4l$

$$\boxed{Z_{\text{in,mem}} k \cdot f_{\text{LO}}) = R_{\text{sw}}} \tag{2.8}$$

Input impedance for $k = 4l + 1$ **or** $k = 4l + 3$

$$\boxed{Z_{\text{in,mem}}(k \cdot f_{\text{LO}}) = \frac{k^2\,\pi^2}{k^2\,\pi^2 - 8}\,(R_{\text{source}} + R_{\text{sw}}) - R_{\text{source}}} \tag{2.9}$$

Input impedance for $k = 4l + 2$

$$\boxed{Z_{\text{in,mem}}(k \cdot f_{\text{LO}}) = \frac{k^2\,\pi^2}{k^2\,\pi^2 - 16}\,(R_{\text{source}} + R_{\text{sw}}) - R_{\text{source}}} \tag{2.10}$$

To validate this formula, we replace the values of R_{source} and R_{sw} by those of the simulated circuit of fig. 2.10 giving: $Z_{\text{in,mem}}(f_{\text{LO}}) = 321\,\Omega$. As

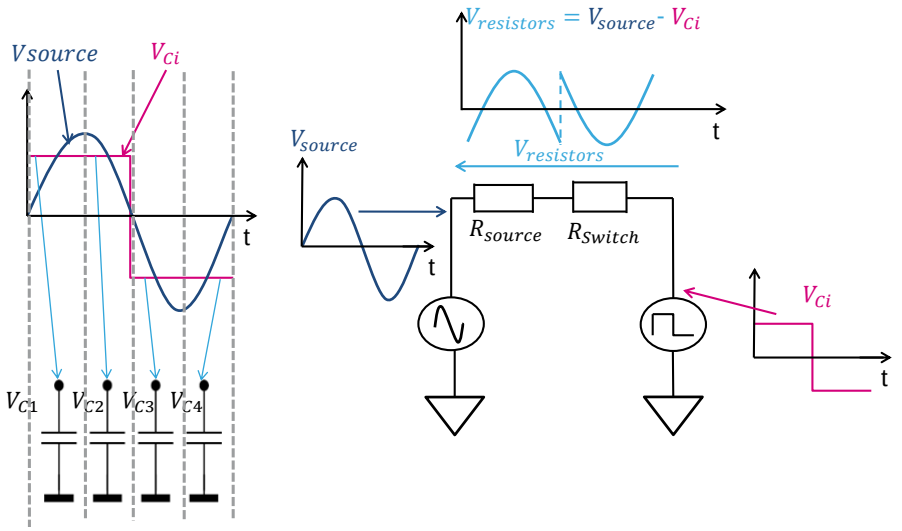

FIGURE 2.13: LTV N-path input impedance

stated before, the capacitor memory-effect impedance calculated in this section is not the total input impedance, it's only the impedance resulting from the voltage held in the baseband capacitor, and not the baseband impedance itself. The total input impedance is therefore the parallel combination of $Z_{\text{in,mem}}$ and the baseband impedance equal to $\frac{R_p}{4}$: $Z_{\text{in}}(f_{\text{LO}}) = Z_{\text{in,mem}}(f_{\text{LO}})//\frac{R_p}{4} = 321//2500 = 284\,\Omega$ which is close to the simulated input impedance value $Z_{\text{in,Sim}}(f_{\text{LO}}) = 283\,\Omega$. The same for $2f_{\text{LO}}$: $Z_{\text{in}}(2f_{\text{LO}}) = Z_{\text{in,mem}}(2f_{\text{LO}})//\frac{R_p}{4} = 67.5//2500 = 65.7\,\Omega$ which is close to the simulated input impedance value $Z_{\text{in,Sim}}(f_{\text{LO}}) = 66\,\Omega$. Finally $3f_{\text{LO}}$: $Z_{\text{in}}(2f_{\text{LO}}) = Z_{\text{in,mem}}(2f_{\text{LO}})//\frac{R_p}{4} = 27//2500 = 26.7\,\Omega$ which is close to the simulated input impedance value $Z_{\text{in,Sim}}(f_{\text{LO}}) = 27\,\Omega$.

This calculated $Z_{\text{in,mem}}$ is the impedance resulting from the memory-effect of the capacitor, that is present only at the N-path center frequency and its harmonics. Thus, outside of the center frequency and harmonics, it is the LTI impedance (eq. 2.6) which is valid.

Now that we calculated Z_{in}, we propose in the next section a solution for the problem of N-path input impedance when used in parallel, i.e. the second N-path presents a shunt in parallel to the first one, at its center frequency as shown in fig. 2.4.

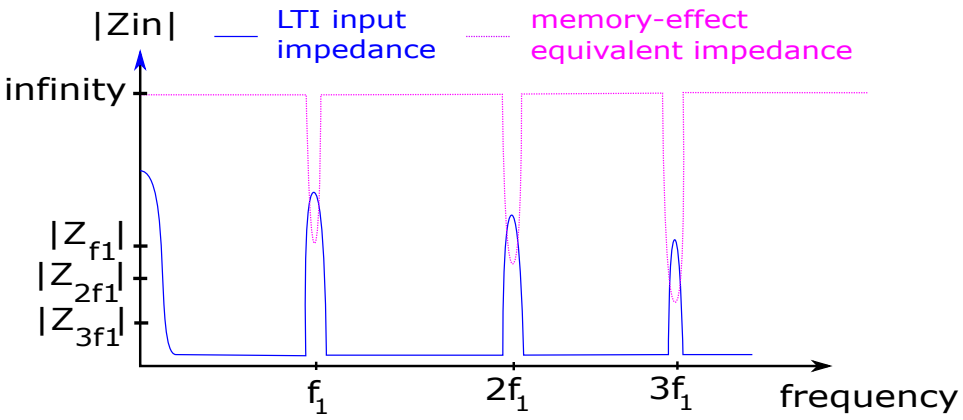

FIGURE 2.14: N-path input impedance, merging LTI and LTV models.

2.3.3 Use of switch resistance (R_{sw}) for input impedance tuning

A solution to the parallel N-path presenting a low input resistance (R_{sw}), to the receiving one at its center frequency is to use $R_{sw} = M\,R_{source}$. Therefor, M parallel N-paths would have an input impedance equal to the source impedance as shown in fig. 2.15.

In the one hand, a large R_{sw} value means a small switch. In the other hand, for a fixed bandwidth, increasing the resistance reduces the capacitor size, leading to both a low power and low area N-path, exactly as targeted. However, increasing R_{sw} value increases the NF accordingly (for a fixed bandwidth). This solution is suitable for low power and low area receivers.

In this section, we developed and validated the analytic expression of the input impedance of a N-path receiver. We came up with a novel solution for parallel reception using N-path receivers, counting on increased switch resistance to shape the impedance according to parallel reception constraints. If this solution can be used for ultra low power reception, taking advantage of a full passive scheme, it is limited in term of noise: increasing switch resistance will result in increased NF and make the solution incompatible with most of radio standards. For this reason, it has been decided to explore another trade-off: allow ourselves to use an active block (G_m) in our N-path arrangement. This will bring us extra flexibility (but with a consumption and linearity penalty) in the system optimization.

2.4 G_m N-path receiver

Full N-path receiver appears to be a promising solution for parallel reception, for the low power and high linearity aspects. On the other hand, as demonstrated in previous chapter, this kind of solutions suffers from input

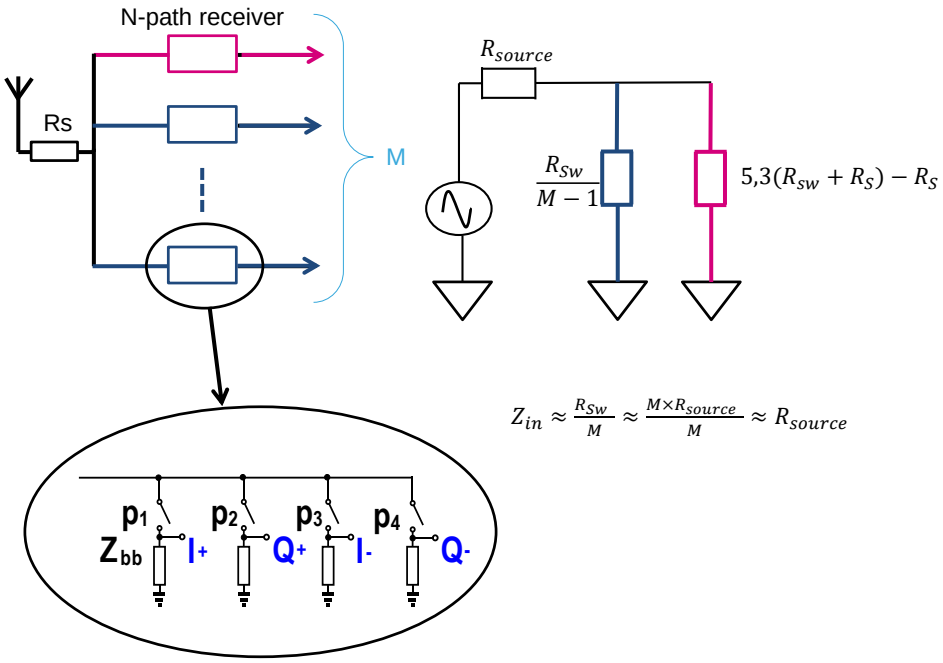

FIGURE 2.15: Solution for N-path input impedance : $R_{sw} = M \cdot R_s$

impedance management constraints, which, in conjunction with parallel reception constraints, become unfeasible when targeting low noise solutions. Adding a transconductor block (G_m) at the N-path input will split the problem. N-path will be responsible for filtering and frequency translation, whereas G_m will define the input impedance and noise.

The implemented G_m block at the input of the N-path is placed as shown in fig. 2.16. It results in a low NF receiver as shown in fig. 2.17, along with avoiding the input impedance problem of parallel N-paths.

Need for a harmonic rejection receiver

The basic operation of the N-pathreceiver (as any mixer based receiver) is to multiply the input (RF) signal with an LO signal. The LO being a square wave, not only the "useful" RF signal (located at LO frequency) is down converted to baseband, but also any harmonic, corrupting the output signal.

In parallel reception context, it is not possible to have filtering prior to receiver input, obliging the receiver to reject harmonics, as the Harmonic Rejection Mixer (HRM) does.

The principle of Harmonic Rejection Mixer (HRM) is well known [17]. As mixer can only operate with square LO waves (for noise and linearity

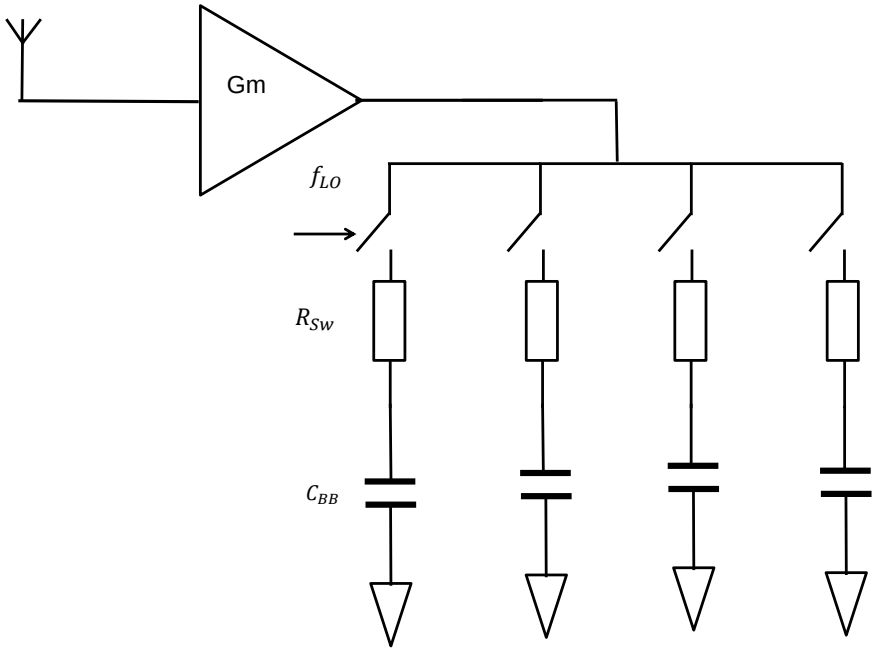

FIGURE 2.16: G_m N-path

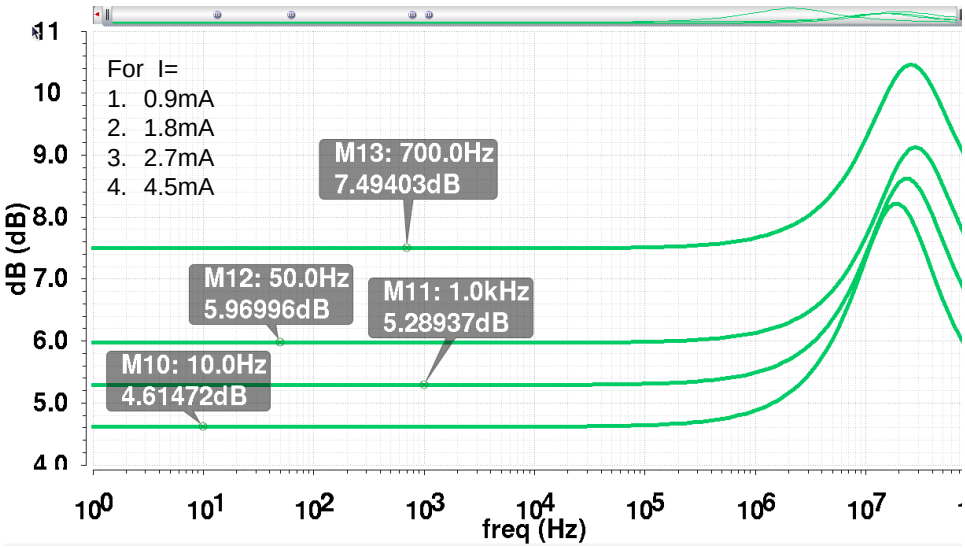

FIGURE 2.17: G_m N-path NF

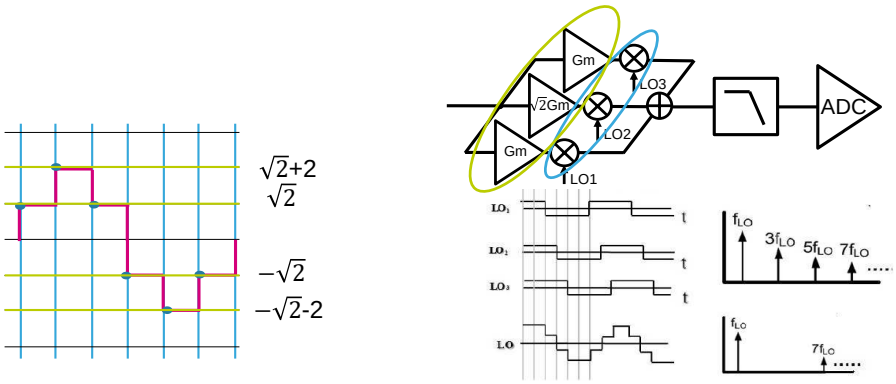

FIGURE 2.18: Traditional Harmonic Rejection Mixer (HRM) [17]

reasons), it is not suitable to multiply input signal with a sine wave to prevent any harmonic mixing. An alternative solution is to mix the input signal with multiple square waves, all with the same frequency, but with different phases and amplitudes so that, when combining all mixers output, fundamental contributions are added and harmonics contributions are canceled. One example is presented in fig. 2.18, where 3 mixers are used with $\frac{\pi}{3}$ phase shift and 1, $\sqrt{2}$, 1 weights [17]. Behavior of HRM can be understood both in frequency and time domain. In frequency domain, one can observe that the Fourier transform of the weighted sum of the 3 LO signals does not contain any 3^{rd} and 5^{th} harmonics. This explains why this HRM does not mix around 3^{rd} and 5^{th} harmonics. In time domain, drawing the weighted sum of the LO signal reveals a signal mimicking a sine wave. This observation really makes sense: the more the LO signal is close to the sine wave, the less harmonics it contains and the better he performs as HRM. This HRM scheme can be extended to the G_m N-path receiver, adding multiple G_m-switch path to the same output capacitance as shown in fig. 2.19.

This scheme is nevertheless not fully compliant with the context of parallel reception because it still relies on the availability of a signal at LO frequency. This means that having M parallel receivers will require M LO frequencies (M PLL's) which is not practically feasible for large M.

Our proposed solution to get rid of the need of multiple LO frequencies

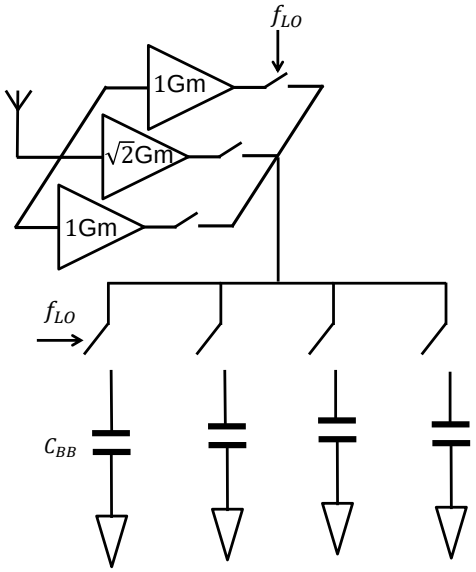

FIGURE 2.19: G_m N-path Harmonic Rejection Mixer (HRM)

is to mimic a sine wave at a given frequency by summing square waves, at LO frequency with different amplitudes. In other words, LO signal is digitized with a given sampling frequency. Nyquist criteria tells us that this is possible, as soon as sampling frequency is strictly higher than twice LO frequency.

This solution open the way for parallel reception: Parallel receiver can be built with a single PLL, generating sampling frequency, chosen to be slightly higher than the two times maximum frequency to be received. Thus, each receiver will be G_m-N-path based, including a HRM driven by a Direct Digital Frequency Synthesis (DDFS).

2.5 Novel architecture introduction: Mixer-DAC G_m N-path

The architecture shown in fig. 2.20 is a practical implementation of the proposed solution. G_m + switch arrangement has been replaced with a "switchable G_m" and the bank of G_m, initially all with the same amplitude, has been replaced with a binary weighted G_m bank to reduce the complexity. The G_m value varies over time as walking sampled sine-wave. Thus, the mixing is done in the G_m by modulating its value. The output current is therefore the multiplication of the RF input voltage and the modulated G_m,

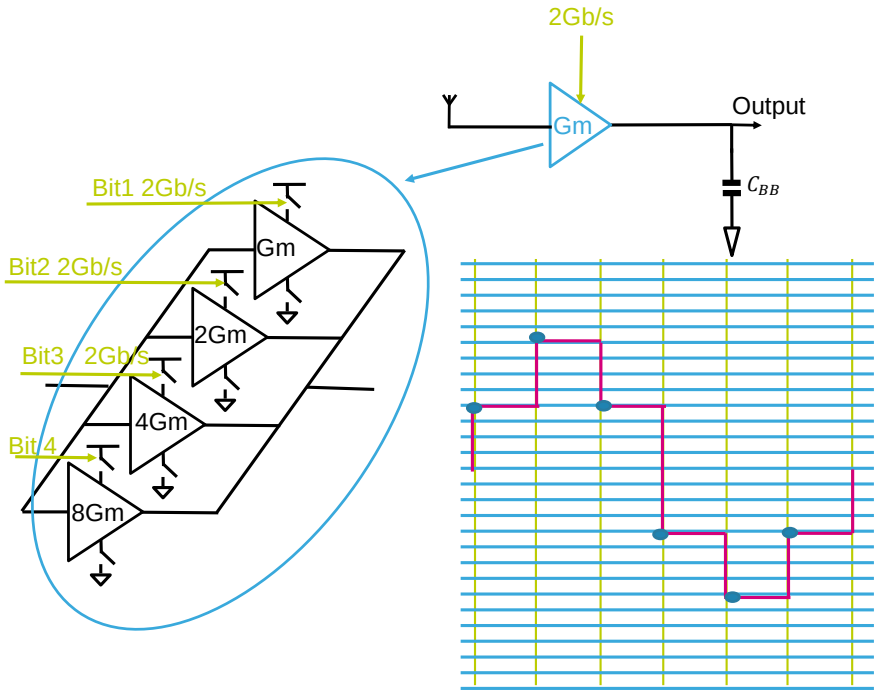

FIGURE 2.20: Harmonic rejection G_m N-path based mixer-DAC

resulting in a baseband current that will be integrated over the baseband capacitor. The G_ms are driven by a DDFS. For M parallel tuners, each tuner will include a mixer-DAC along with its DDFS, all driven by a single PLL as shown in fig. 2.21. Moreover when duplicating many G_m-N-pathreceivers in parallel only the receiving ones would be on, the others could be shunt off, meaning that this architecture power consumption scales with the number of received channels.

This architecture is power scalable and resilient to interference [5]. However, this architecture has to be compared to the FSC to determine in an analytic way, and for a Figure Of Merit (FOM) based comparison, which one of these two architectures is more power efficient for massively parallel reception. Comparison is drawn in chapter 3.

2.6 Conclusion

In this chapter, we introduced the N-path filter and it's correspondent N-path receiver, we listed N-path issues: input impedance and harmonic mixing. Then, we developed an intuitive input impedance calculation, along with solutions to get rid of the input impedance issue, as the G_m-N-path that is described in section 2.4. in the last section a G_m-N-path based mixer-DAC

[5] Uses one analog clock and as much DDFS as needed tuner

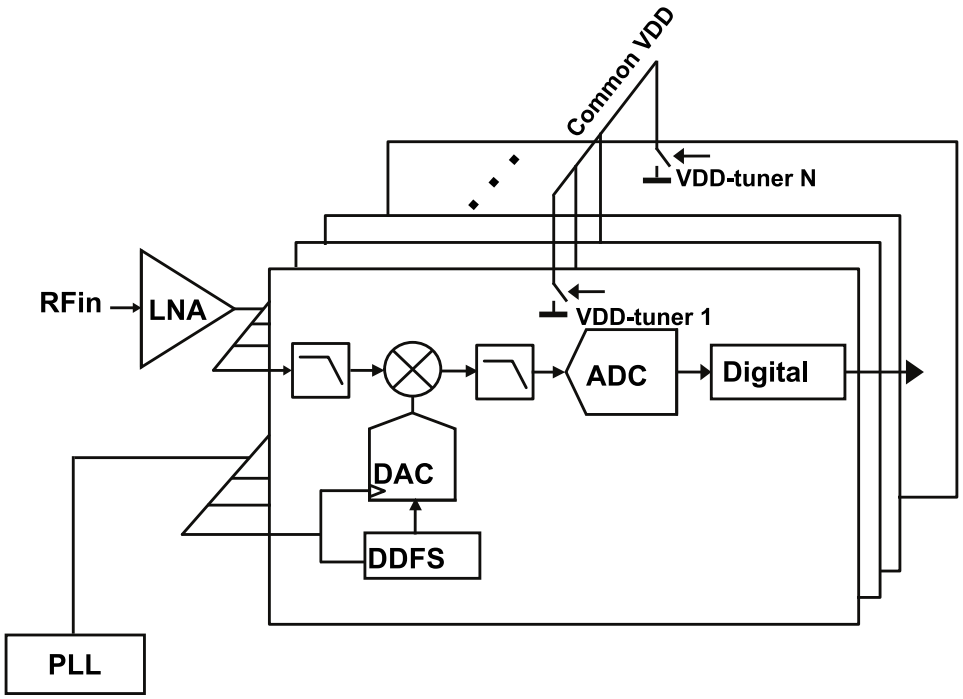

FIGURE 2.21: Mixer-DAC parallel tuners architecture

is proposed to get rid of the harmonic mixing issue. This proposed solution take advantage from the low power and area G_m N-path receiver as well as the interference robustness of the DDFS driving mixer-DAC architecture. Moreover, this architecture is power scalable, which make it a promising candidate for massively parallel reception. However, this architecture has to be compared to the FSC to determine in an analytic way, and for a FOM based comparison, which one of these two architectures is more power efficient for massively parallel reception. Comparison is drawn in chapter 3.

Chapter 3

Massively Parallel Reception: a Power Efficiency Comparison of Mixer-DAC and Full Spectrum Capture

3.1 Introduction

In the last chapter we developed a G_m N-path based mixer-DAC, that features all the targeted constraints, i.e. robustness to interferences, low power and area per receiver, and a power consumption that scales with the number of received channels (§ 2.5). Nevertheless, this architecture would be duplicated as many times as needed for each parallel tuners, making the total power increase with the number of received channels. This total power consumption could then exceed the FSC power consumption for a high number of received channels (the power consumption of the FSC is fixed and slightly depends on the number of received channels). These two architectures have therefore to be compared analytically to determine the more power efficient one.

In this chapter, we present two main massively parallel receivers architectures: FSC and Mixer-DAC. Then, we compare their power consumption for a given test case. In section 3.2, the two architectures are presented along with each one's advantages and drawbacks. In section 3.3, we present the assumptions on which the comparison was based, and the standard of comparison Data Over Cable Service Interface Specification (DOCSIS) 3.0. This standard was chosen just as a starting point to compare the two architectures, as it represents a realistic test case. The comparison will be widened to more general cases later on. Within this section, we present a detailed study of the noise contribution of each block of the two architectures and the way it is related to that block's power consumption. Then, we explain the way

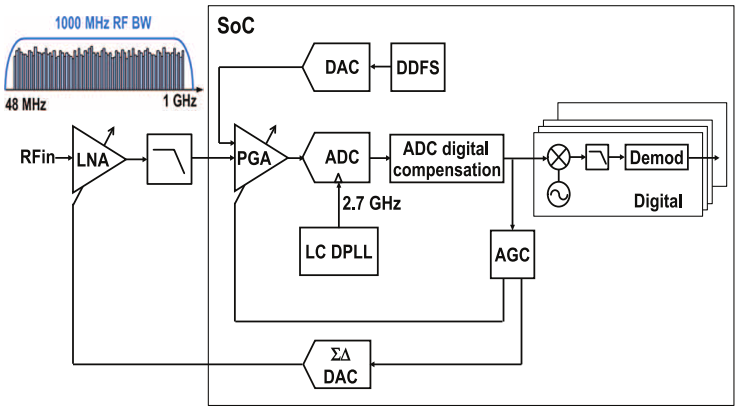

FIGURE 3.1: Full Spectrum Capture architecture [9].

the total architecture power budget is split between the different blocks, and conclude on the total noise contribution of the two architectures. We finally present the power consumption comparison results based on the noise contributions study, and with respect to DOCSIS 3.0 standard. The comparison outcome targets is to define an "efficiency limit", i.e. a number of channels above which FSC is more power efficient than mixer-DAC. In section 3.4, a comparison of the two architectures with respect to standards other than DOCSIS 3.0 is presented. We choose for that to simply compare the two architectures for sweeps on DOCSIS 3.0 parameters, which is equivalent to comparing them for a wide spectrum of standards. The goal is here again to show how the efficiency limit changes over every swept parameter.

The final conclusion is that the efficiency limit for the first comparison case is 11 channels. For standards other than TV, this limit is expected to be even higher, which makes the choice of mixer-DAC architecture, for these cases, even more beneficial than FSC.

3.2 Presentation of the two compared architectures

3.2.1 Full Spectrum Capture

The FSC shown in fig. 3.1 was introduced in chapter 1 as an ADC-first architecture, where the ADC digitizes the whole spectrum so that the signal processing is entirely done in digital [9]. As mentioned previously, this architecture solves the problem of clean LO-generation by using one clock and DCS blocks: mixing in digital with DDFS helps overcome the harmonic mixing problem (DDFS high number of bits). However, the FSC has a high power consumption that does not scale with the received bandwidth.

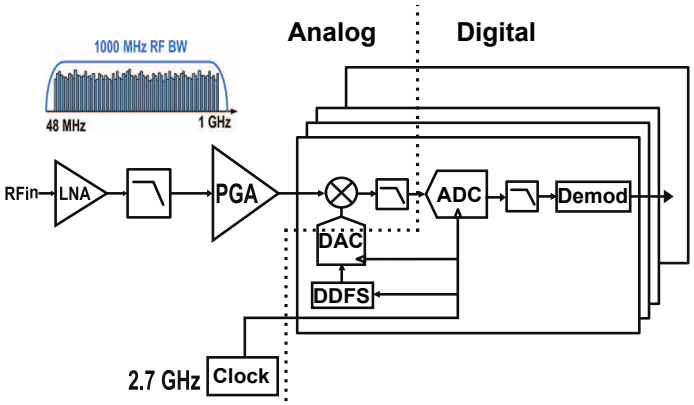

FIGURE 3.2: Mixer-DAC architecture

3.2.2 Mixer-DAC receiver

The mixer-DAC architecture relies on a single central clock that drives one DDFS per channel, as shown in fig. 3.2. For each channel, the DDFS drives a mixer-DAC which downconverts the wanted channel to baseband. The channel is first selected through a LPF and then, digitized by an ADC. This architecture, being based on one central clock and DDFS blocks, allows for a clean LO generation without interference problems. The resolution of the DDFS clock determines the harmonic rejection ratio: the higher the number of bits, the higher the harmonic rejection ratio. This architecture was used in [8] to target a 60 dB dynamic range single TV receiver application, and in [18] as an alternative solution to FSC. This architecture is power scalable and uses low FOM ADCs (bellow 100 MHz f_s, as shown in fig. 1.4). However, each channel includes a high sampling frequency (f_s) mixer-DAC. If duplicated many times, as for the massively parallel reception case, the power consumption of all the mixer-DACs can rise very high and exceed the FSC one. The mixer-DAC power consumption should therefore be compared to the FSC one, for the same input antenna spectrum and the same output SNR constraint.

3.3 Full Spectrum Capture and mixer-DAC power efficiency comparison in DOCSIS context

3.3.1 Comparison assumptions

In fig. 3.3, the blocks that will be compared are surrounded by a dashed line. The blocks surrounded by a solid line are those that will not be taken into account in the comparison, as they are used by both architectures, and can

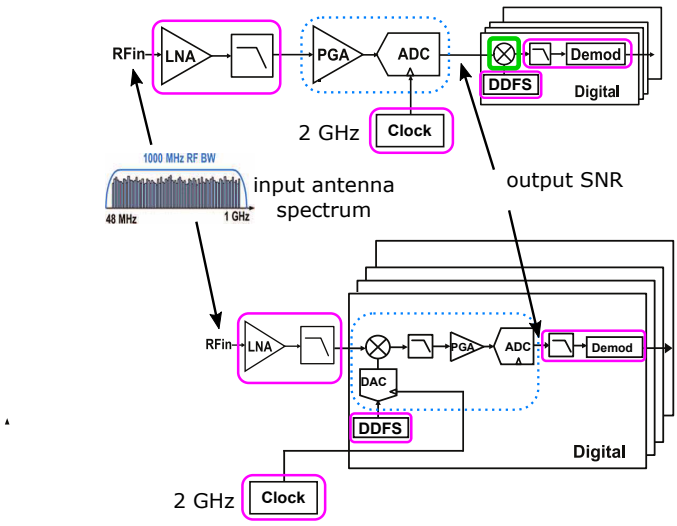

FIGURE 3.3: Comparison of the two architectures: FSC and mixer-DAC.

therefore be suppressed from both architecture for this comparison. The blocks surrounded by a bold line, FSC mixer and decimation blocks, will also be discarded from comparison, but at the advantage of FSC as they run at a very high frequency, which means a big power consumption and noise contribution. The aim of this paper being to prove that the mixer-DAC architecture is more adapted to the massively parallel reception, we can afford advantaging FSC. Moreover, the digital blocks power consumption is directly related to the technology, so that eliminating them avoids having a comparison that is bound to technology and makes it more general. The two architectures will be compared with respect to a custom standard derived from the DOCSIS 3.0 standard that we will call "comparison values". All values are equal to those of DOCSIS 3.0 except the number of channels where we use $\frac{f_{\max}}{\mathrm{BW}} = 250$, in order to have a dense spectrum, meaning that there is no single frequency band that is unused from 0 to $f_{\max}$. Also, the output SNR was changed from the DOCSIS value of 33 dB to 60 dB to consider the uncounted blocks: for example, the first LNA is generally one of the biggest noise contributors in a receiver chain. Both "comparison values" and DOCSIS 3.0 values are depicted in table .3.1. The Peak-to-Average Power Ratio (PAPR) value, given in the table, is for one channel only. For N channels, the $\mathrm{PAPR}_{N\ \mathrm{Channels}} = 10\log(N) + \mathrm{PAPR}_{\mathrm{Single\ Channel}}$.

In the forthcoming comparison, the goal is to sum up the noise contributions of each architecture at a node that is common to both. In our case, we chose the input of the Demod blocks as the reference node, where all noise contributions will be summed up at, and where the output SNR will be calculated.

parameter	DOCSIS 3.0	Comparison values
output SNR [dB]	33	60
$\text{PAPR}_{\text{Single Channel}}$ [dB]	10	10
Channel bandwidth (BW)[MHz]	5.2	5.2
$f_{\max}$[GHz]	1.3	1.3
Number of channels	158	$\frac{f_{\max}}{\text{BW}} = 250$

TABLE 3.1: DOCSIS 3.0 parameters values

To compare the two architectures, the same input spectrum will be considered: M stacked channels with equal amplitudes and with a total power of 1 V. Each channel amplitude is then $\frac{1}{\sqrt{\text{M}}}$ V. We consider, for simplicity sake, that the signal at the comparison reference node has an amplitude of 1 V for both architectures. This way, the signal undergoes, for both architectures, an amplification of gain $\sqrt{M}$.

Throughout the comparison, we go by the rule that SNR is preserved along the reception chain, i.e. for any given block. The block output signal and its noise undergo the same amplifications and therefore preserve their ratio. So, whenever it is possible, noise contribution of a given block will be expressed as a function of the output signal of that same block. When it is not the case, as for noise contributions that are independent of the signal, i.e. KT/C noise and Programmable Gain Amplifier (PGA) noise, the noise contribution has to be multiplied by the amplification gain it underwent before reaching the output node. This way, we can sum up all the noise contributions at the comparison reference node.

There are two amplification steps for both architectures:

- Amplification 1: after mixing and low pass filtering, the signal amplitude changes from $\frac{1}{\sqrt{\text{M}}}$ V to 1 V at the reference node, so that $\sqrt{M}$ gain is needed to get back to the 1 V amplitude at reference node.
- Amplification 2: at ADC input the signal amplitude is equal to $\frac{1}{\sqrt{\text{PAPR}}}$ V which is the maximum value it can have before the ADC (in order to reduce the quantification noise). At reference comparison node, the signal amplitude is directly equal to 1 V, so another $\sqrt{\text{PAPR}}$ gain is needed and will be provided digitally.

For each of the two compared architectures, the power consumption will be derived as a function of the standard parameters, such as output SNR, PAPR ...

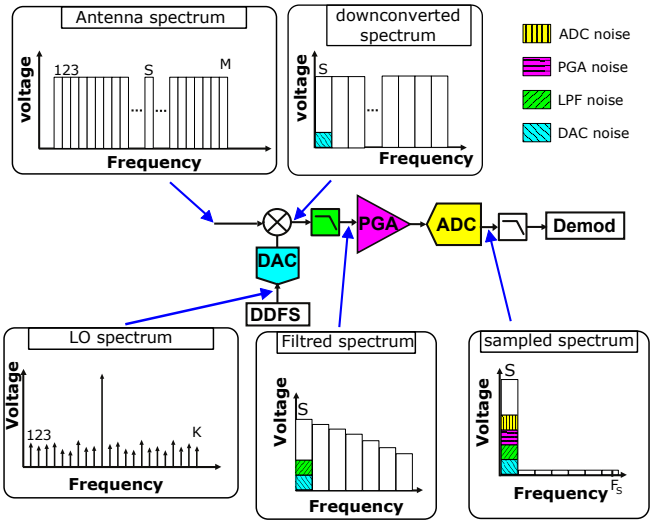

FIGURE 3.4: Mixer-DAC noise

3.3.2 Mixer-DAC: noise contributions vs power consumption

As mentioned above, for the mixer-DAC architecture, we only consider 4 blocks in this comparison (fig. 3.4). Each of these blocks has its own noise contribution to the output signal and its own power consumption. The mixer-DAC block noise contribution results from mixing the antenna's spectrum channels, other than the wanted channel, with the DDFS signal spurs. These fall down to baseband on top of the wanted channel, then they add up to the low-pass filter and PGA noise contributions, and eventually to the ADC noise contribution where both quantification noise and aliasing noise should be considered.

Given a power consumption budget, in order to achieve the minimum output SNR, this budget has to be split in the optimal way between the four blocks. This is achieved through an optimization loop. Along the loop, we try to establish diagrams of minimum total noise contribution versus power budget, for a set of power budget values. The minimum total noise contribution matches the best power split scenario for a given power budget. This optimization loop is divided into two phases:

- Phase 1: establishing minimum noise contribution versus power consumption diagram for the blocks ADC+LPF.
- Phase 2: establishing minimum noise contribution versus power consumption diagram for the blocks PGA+DAC+ADC+LPF. To do so, we use the diagram established in Phase 1. Phase 2 final diagram is therefore used to interpolate the total power budget for a given output SNR value for the whole chain.

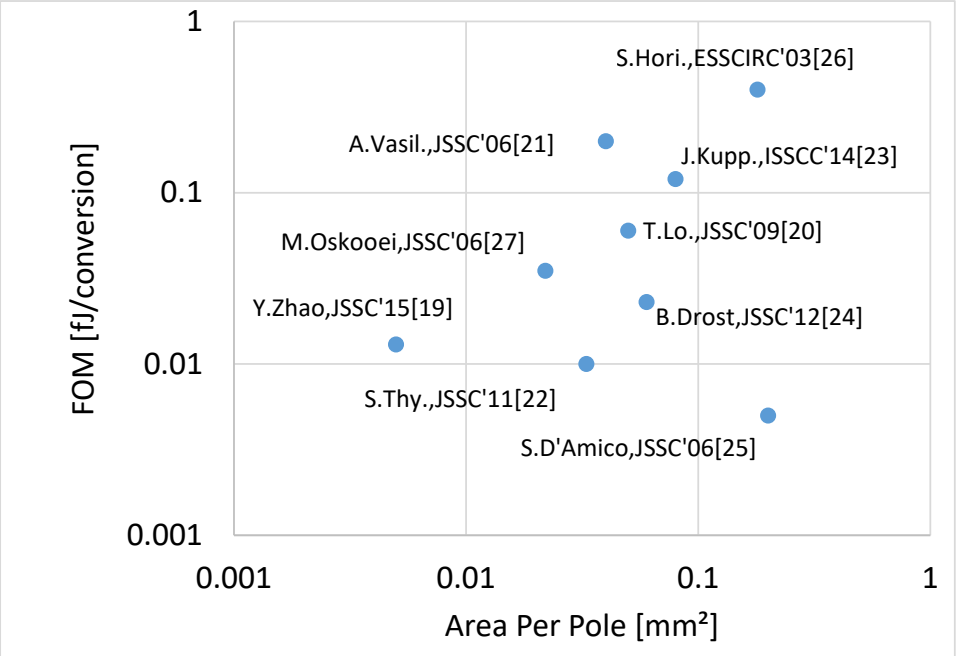

FIGURE 3.5: Low pass filters state of the art.

The final comparison between the two architectures is done by comparing the necessary power budget for a given output SNR constraint. The ADC and LPF cannot be optimized separately as the choice of ADC parameters depends on and influences the LPF parameters choice. Therefore, it is necessary to start with these two blocks in phase 1, while the order of choice for the other two blocks is arbitrary.

Phase 1

Low Pass Filter noise contribution To calculate the Low Pass Filter (LPF) noise contribution as a function of power consumption, and to keep this study general and not bound to one precise LPF architecture, we use LPF FOM [19]:

$$\mathrm{FOM}_{\mathrm{LPF}} = \frac{P_{\mathrm{LPF}}}{\mathrm{BW}\,\mathrm{SFDR}\,O^{7/3}} \tag{3.1}$$

where:

P_{LPF} : LPF power consumption
SFDR : LPF output Spurious Free Dynamic Range (SFDR)
BW : Signal bandwidth
O : LPF order

A LPF FOM survey [19]–[27] is shown in fig. 3.5, the held FOM value for our comparison is $\mathrm{FOM}_{\mathrm{LPF}} = 0.01$ fJ/conversion.

ADC noise contribution for the ADC noise contribution we also use the ADC FOM (eq. 3.4)

The integrated quantization noise error from 0 to $\frac{f_s}{2}$ interval can be expressed as a function of the ADC Full-Scale voltage (FS) and the number of bits (N) [28]:

$$N_{\left[0,\frac{f_s}{2}\right]} = \frac{2^{-N}\,\mathrm{FS}}{\sqrt{12}} \tag{3.2}$$

Approximating the quantification noise to be a white noise (the same approximation holds for the FSC architecture), the quantification noise over the wanted bandwidth is therefore:

$$\begin{aligned} N_{[0,\frac{\mathrm{BW}}{2}]} &= \frac{2^{-N}\,\mathrm{FS}}{\sqrt{12}}\sqrt{\frac{\frac{\mathrm{BW}}{2}}{\frac{f_s}{2}}} \\ &= \frac{2^{-N}\,\mathrm{FS}\,\sqrt{\mathrm{BW}}}{\sqrt{12\,f_s}} \end{aligned} \tag{3.3}$$

The ADC FOM formula [12] is:

$$FOM_{\mathrm{ADC}} = \frac{P_{\mathrm{ADC}}}{f_{\mathrm{snyq}}\,2^N} \tag{3.4}$$

where:

P_{ADC} : ADC power consumption
f_{snyq} : ADC Nyquist frequency
N : Number of ADC bits

including the last formula in the equation 3.3 gives:

$$N_{[0,\frac{\mathrm{BW}}{2}]} = \frac{\mathrm{FS}\,\mathrm{FOM}_{\mathrm{ADC}}\,\sqrt{\mathrm{BW}\,f_s}}{\sqrt{12}\,P} \tag{3.5}$$

The full scale voltage is the sum of the wanted channel and the attenuated unwanted channels, and is equal to:

$$FS = S\,\sqrt{\mathrm{PAPR}}\cdot\left(\frac{\Delta f}{f_{-3\,\mathrm{dB}}}\right) \tag{3.6}$$

Where:

S : One channel amplitude
Δf : Equivalent brick-wall filter cutoff frequency
$f_{-3\,\mathrm{dB}}$: Actual LPF cutoff frequency

This sum depends on the LPF cutoff frequency and order. As mentioned before, the different channels are assumed equal to each other. Then, we

calculate the cutoff frequency of the equivalent brick-wall-filter[1] to our LPF as for Equivalent Noise Band-Width (ENBW) of an LPF, we use equation 3.7:

$$\int_0^\infty |H(\mathrm{j}\omega)|^2 \,\mathrm{d}\omega = H_{\max}^2 \, 2\,\pi\,\Delta f \tag{3.7}$$

where:

$H(\mathrm{j}\omega)$: LPF transfer function
$H_{\max}$: Maximum value of $H(\mathrm{j}\omega)$

Finally, the ADC quantification noise contribution to the comparison reference node can be expressed as follows:

$$N_{[0,\frac{\mathrm{BW}}{2}]} = \frac{S\,\sqrt{\mathrm{PAPR}}\cdot\left(\frac{\Delta f}{f_{-3\,\mathrm{dB}}}\right)\,\mathrm{FOM}_{\mathrm{ADC}}\,\sqrt{\mathrm{BW}\,f_s}}{\sqrt{12}\,P} \tag{3.8}$$

The ADC FOM value used for this comparison is not a fixed value. As explained above, for high frequencies, the FOM grows linearly with f_s. So, for $f_s < 100\,\mathrm{MHz}$, a fixed value was used: $\mathrm{FOM}_{\mathrm{ADC}}(f_s) = 1.4\,\mathrm{fJ/conversion}$, and for $f_s > 100\,\mathrm{MHz}$, $\mathrm{FOM}_{\mathrm{ADC}}(f_s) = 1.4\,\frac{f_s}{100\,M}$. It is the value of $\mathrm{FOM}_{\mathrm{ADC}}$ used in the mixer-DAC architecture. The aliasing noise is given by the following equation:

$$N_{\mathrm{Aliasing}} = S\left(\frac{1}{1+\left(\frac{f_s}{\mathrm{BW}}\right)^2}\right)^{O/2} \tag{3.9}$$

Phase 1 optimization In order to optimize the total power consumption, a set of total power consumption values was considered, and for every value, the optimal way of splitting this power was found, i.e. we find the ADC number of bits, sampling frequency and LPF order that give the minimum noise contribution for this given total power. Then, we get a list of noise contributions as a function of power consumption of the combination ADC and LPF.

Phase 2

At this step of the optimization, like in phase 1, we find the optimum power distribution, but this time we have 3 blocks: PGA, DAC and the last block is the combination of ADC+LPF. For this last block, we use the diagram obtained at phase 1; one more parameter is introduced and optimized at this

[1] brick-wall-filter means an ideal filter that would have a transfer function with only two distinct region: a totally pass region and a totally reject region, and nothing in between them. As a transfer function made by brick-wall.

phase: the hold capacitor of the ADC. The reason why this capacitor noise contribution is included with PGA, and not ADC, is explained below.

To determine the PGA noise versus power consumption equation, we use the following equation [29]:

$$SINAD = \frac{P_{\text{signal}}}{P_{\text{noise}} + P_{hn}} = \frac{P_{\text{signal}}}{\frac{KT}{C_{\text{load}}} + \frac{1}{2}(H_n)^2(C_{\text{load}})^2} \tag{3.10}$$

The Signal-to-Noise And Distortion ratio (SINAD) of a simple MOS follower is a trade-off between noise and distortion depending on C_{load} value. When C_{load} goes high, the thermal noise goes high and when it goes low, the distortion power goes high. C_{load} value depends on the sizing and the technology. However, given that PGA is loading an ADC, i.e. a hold capacitor, the main contributor to the parasitic capacitor at the load node is the ADC's hold capacitor. Considering the only contributor to this node to be the hold capacitor, makes the study unbound to a specific technology.

In order to evaluate SINAD, we use the following equation [29]:

$$\begin{aligned} P_{h3} &= \frac{h_3^2}{2} \\ &= \frac{1}{2}\left(\frac{\hat{V}}{2}\right)^6 \frac{(2\,\pi f_{\text{sig}})^6 (C_{\text{load}} + C_{\text{tot},w}\,W)^6}{I_D^6} \left(\frac{2V_{GT1}}{64}\right)^2 \end{aligned} \tag{3.11}$$

where:

f_{sig}	: signal frequency
P_{h3}	: harmonic 3 signal power
h_3	: harmonic 3 signal amplitude
$\hat{V}$	: output signal swing
W	: width of the output transistors
I_D	: bias current of the output transistor
V_{GT}	: overdrive voltage
$C_{\text{tot},w}$	: parasitic capacitance, per width unit

As we only consider the capacitance contribution of C_{hold} at the load node, the up said equation becomes:

$$P_{h3} = \frac{1}{2}\left(\frac{\hat{V}}{2}\right)^6 \frac{(2\,\pi f_{\text{sig}})^6 (C_{\text{load}})^6}{I_D^6} \left(\frac{2V_{GT1}}{64}\right)^2 \tag{3.12}$$

This output distortion is calculated at the PGA output node, meaning that the noise in (3.11) will be amplified only by the $\sqrt{\text{PAPR}}$ gain to be

counted at the comparison reference node, resulting in a noise contribution to the comparison reference node to be:

$$N_{h3} = \sqrt{\frac{\text{PAPR}}{2}} \left(\frac{\hat{V}\, \pi\, f_{\text{sig}}\, C_{\text{load}}}{I_D} \right)^3 \left(\frac{V_{GT1}}{32} \right) \tag{3.13}$$

Where N_{h3} is the distortion contribution of the PGA at the comparison reference node.

The KT over C noise is the thermal noise produced by the PGA and the sampling switch or block resistance, that will be integrated over the hold capacitor. Generally, the cutoff frequency of the sample-and-hold RC LPF, is fixed at $f_s/2$. The integrated thermal noise, at ADC output, is then given by the equation below

$$N_{\frac{KT}{C},[0,\frac{f_s}{2}]} = \sqrt{\frac{KT}{C}} \tag{3.14}$$

The KT over C noise being produced after the PGA in the mixer-DAC architecture, its noise contribution should not be amplified, resulting in a noise contribution for the channel bandwidth and at the comparison reference node as follows:

$$N_{\frac{KT}{C},[0,\frac{\text{BW}}{2}]} = \sqrt{\frac{KT\,\text{BW}\,\text{PAPR}}{C_{\text{hold}}\, f_s}} \tag{3.15}$$

DAC noise contribution The DAC noise contribution vs power consumption is defined through a FOM_{DAC}.

$$FOM_{\text{DAC}} = \frac{P_{\text{DAC}}}{f_s\, 2^N} \tag{3.16}$$

The DAC power consumption is split into a dynamic and a static power, the latter being the DC current sources that charge the load. Given FOM equation, both power consumption types, static and dynamic, are directly proportional to f_s and to 2^N. While this is obvious for dynamic power consumption and for static power with respect to 2^N, it is less intuitive for the static part to be proportional to the sampling frequency. It can be explained as follows: the DC current is inversely proportional to the settling time of the signal, say: $I_{\text{DC}} = cst/T_{\text{settling}}$. The signal must be completely settled within half of the DAC clock period, i.e. $T_{\text{settling}} < 1/(2f_s)$. This implies: $I_{\text{DC}} > cst \cdot 2f_s$. Given the fact that we try to optimize power consumption, we choose:$I_{\text{DC}} = cst \cdot 2f_s$. The static power consumption is therefore directly proportional to sampling frequency. A DAC state of the art

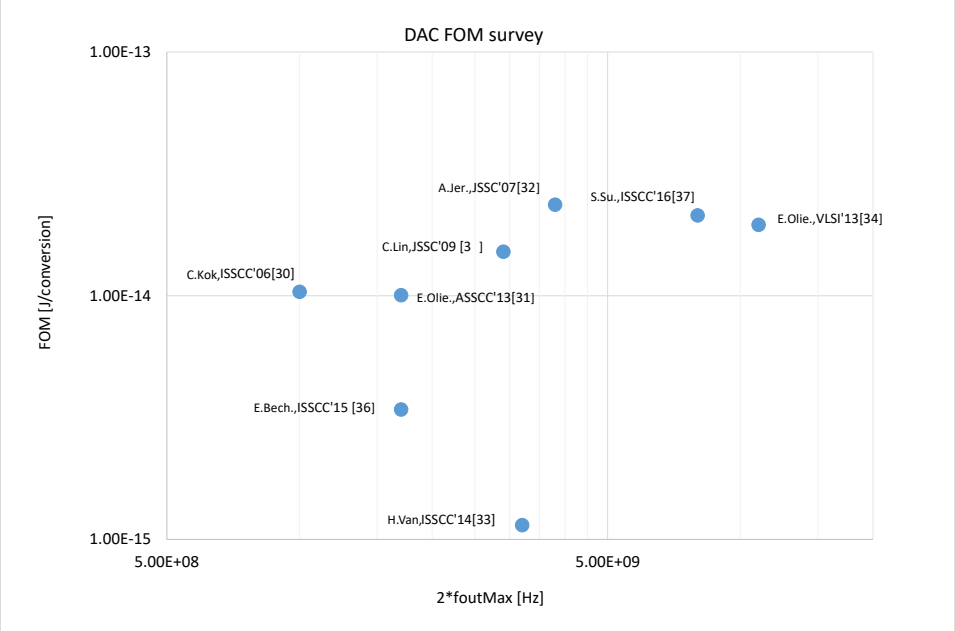

FIGURE 3.6: DAC FOM state of the art.

was assembled and plotted in fig. 3.6 [30]–[37]. The FOM_{DAC} state of the art does not resembles the ADC shown in chapter 1: the DAC FOM is flat or at least flat till a high frequency, here 5 GHz, compared to the 100 MHz corner frequency for the ADC FOM. The hold FOM value for our comparison is $\text{FOM}_{\text{DAC}} = 3.5\,\text{fJ/conversion}$.

The considered noise contribution of the DAC is the quantification noise present in the sampled LO signal that DDFS generates. Every spur of this quantification noise mixes with the channel that has the same frequency. The outcome is a baseband noise whose amplitude is equal to the sum of spurs multiplied by one channel amplitude. The sum of the spurs is equal to the integrated quantification noise in equation (3.8), where Full Scale (FS) is considered to be 1, because the sampled signal is the output of the DDFS. We assume that the DDFS driving an RF DAC will obviously reach the full scale. The DAC f_s is fixed to 2.7 GHz.

The integrated mixer-DAC noise is then:

$$N_{\text{mixer-DAC}} = \frac{S\,2^{-N}}{\sqrt{12}} \tag{3.17}$$

When we combine (3.16) and (3.17), the mixer-DAC integrated output noise expression becomes:

$$N_{\text{mixer-DAC}} = \frac{S\,FOM_{\text{DAC}}\,f_s}{\sqrt{12}\,P_{\text{DAC}}} \tag{3.18}$$

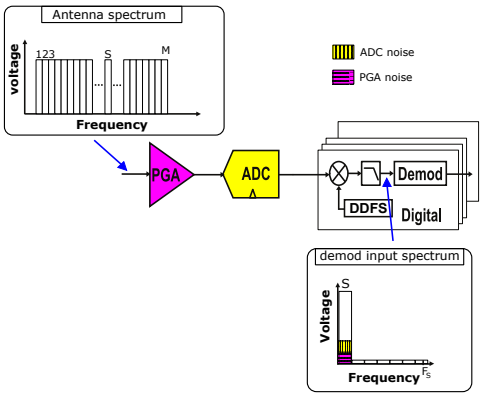

FIGURE 3.7: FSC counted blocks and noise contributions

This is the integrated noise contribution of the mixer-DAC over $[0, \frac{BW}{2}]$ bandwidth, at the comparison reference node.

Finally, through an optimization loop, we calculate the minimum power consumption for the mixer-DAC architecture, as to be $P_{\text{mixer-DAC}} = 2.9mW$. The main power consumer in the chain is the mixer-DAC as expected.

3.3.3 Full Spectrum Capture: noise contributions vs power consumption

In fig. 3.7, the counted blocks of the FSC are presented along with their respective noise contributions, i.e. the PGA distortion and the hold capacitor noise contribution, as done for the mixer-DAC PGA. Then, we add the quantification noise of the ADC. Finally, the optimal way of splitting a given power budget is calculated. Note that f_s of the ADC is fixed for this architecture and is equal to 2.7 GHz. One more parameter is added to this power optimization, as in phase 2 optimization of the mixer-DAC architecture, which is the hold capacitor value.

Programmable Gain Amplifier

As for the mixer-DAC architecture, the Programmable Gain Amplifier (PGA) noise contribution at the PGA output is given by equation (3.13). But, for the FSC architecture, the gain is placed after the PGA block, meaning that the noise should be amplified by $\sqrt{M}$ to be counted at the comparison reference node which results in the equation below:

$$N_{h3} = \sqrt{\frac{M\,\text{PAPR}}{2}} \left(\frac{\hat{V}\,\pi f_{\text{sig}}\,C_{\text{hold}}}{I_D} \right)^3 \left(\frac{V_{GT1}}{32} \right) \tag{3.19}$$

The KT over C noise used in (3.15) applies also at the output of the ADC block, in the FSC architecture, except that here it must be amplified by $\sqrt{M}$ to be counted at the comparison reference node, resulting in the equation below:

$$N_{\frac{KT}{C},[f-\frac{\mathrm{BW}}{2},f+\frac{\mathrm{BW}}{2}]} = \sqrt{\frac{M\,\mathrm{PAPR}\,KT\,\mathrm{BW}}{C_{\mathrm{hold}}\,\frac{f_s}{2}}} \tag{3.20}$$

ADC noise contribution

For the FSC architecture, we only consider quantification noise. As the maximum existing channel at antenna input is assumed to be in the $[0,\frac{f_s}{2}]$ interval, the aliasing noise is supposed to be null. The quantization noise equation is same as (3.2) where FS is now expressed as follows:

$$\mathrm{FS} = \sqrt{M\,\mathrm{PAPR}}\,S \tag{3.21}$$

The integrated ADC quantification noise over the wanted channel bandwidth, can thus be expressed depending on signal amplitude as follows:

$$N_{[f_w-\frac{\mathrm{BW}}{2},f_w+\frac{\mathrm{BW}}{2}]} = \frac{S\,\sqrt{M\,\mathrm{PAPR}\,\mathrm{BW}\,f_s}\,FOM_{\mathrm{ADC}}}{\sqrt{6}\,P_{\mathrm{ADC}}} \tag{3.22}$$

The ADC FOM used for the FSC architecture is equal to $FOM_{\mathrm{ADC}}(2.7G) = 1.4\,\frac{2.7G}{100M} = 37.8fJ/conversion$ which is approximately equal to a 2.7 GHz sampling frequency ADC FOM in fig. 1.4

Optimization Finally, through an optimization loop, we calculate the minimum power consumption for the FSC architecture, as to be $P_{\mathrm{ADC}} = 63mW$. For FSC the main power consumer in the chain is the ADC as expected.

3.3.4 Power consumption comparison: introduction of efficiency limit concept

In fig. 3.8, we plot the power consumption of both architectures versus the number of received channels. The mixer-DAC power consumption used to draw the fig. 3.8 is equal to 2 times the one calculated above, because every image rejection receiver should include two duplicates of the mixer-DAC architecture: I and Q The mixer-DAC power consumption is proportional to the number of received channels, while the FSC has a fixed power consumption: power consumption of the digital part, which is proportional to the received channels number, has been neglected, and the only two

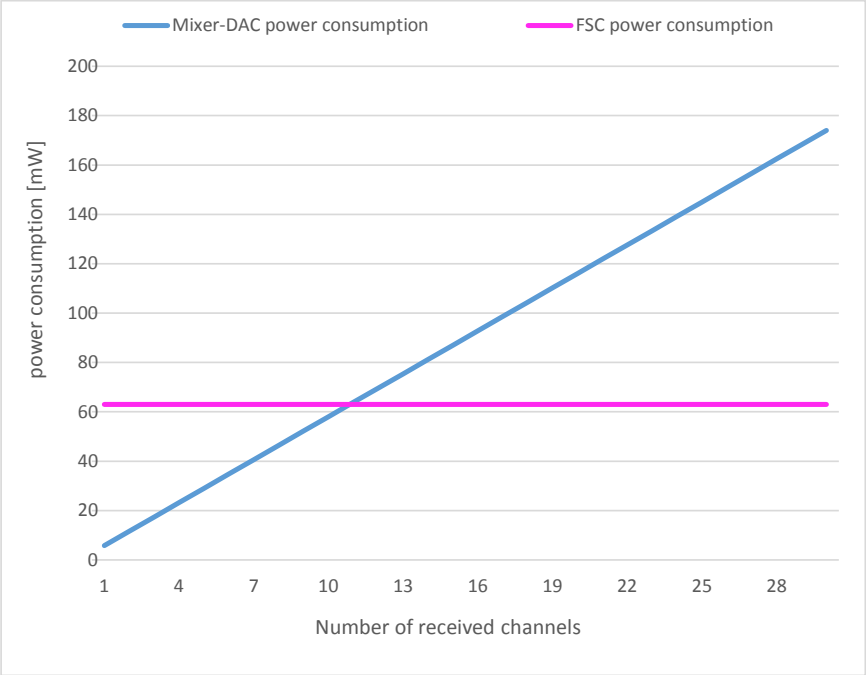

FIGURE 3.8: FSC and mixer-DAC power consumption as a function of number received channels

blocks kept have a power consumption that is independent of the number of channels. Fig. 3.8 shows that the mixer-DAC is less power consuming than the FSC architecture for up to 11 received channels simultaneously. This defines an efficiency limit equal to 11. Moreover the mixer-DAC architecture has a scalable power consumption with the number of received channels, making this solution more adapted to practical use cases, i.e. where the user needs to use 2 or 3 simultaneous channels most of the time, while for short time-slots a higher number of channels could be needed. The FSC is less power consuming than the mixer-DAC only if we receive more than 11 channels 100 % of the time, meaning that the mixer-DAC is still more power-efficient than FSC if we receive 54 channels for 10 % of the time, and 2 channels simultaneously for the remaining 90 % of the time. In general we can conclude that the mixer-DAC is more power efficient than the FSC up to 11 average-simultaneously-used-channels.

3.4 Comparison for other standards

Instead of repeating this comparison for a series of other standards, here we choose to sweep the comparison parameters of table 3.1 and the different given FOM values. For every sweep, we will plot the up said efficiency limit

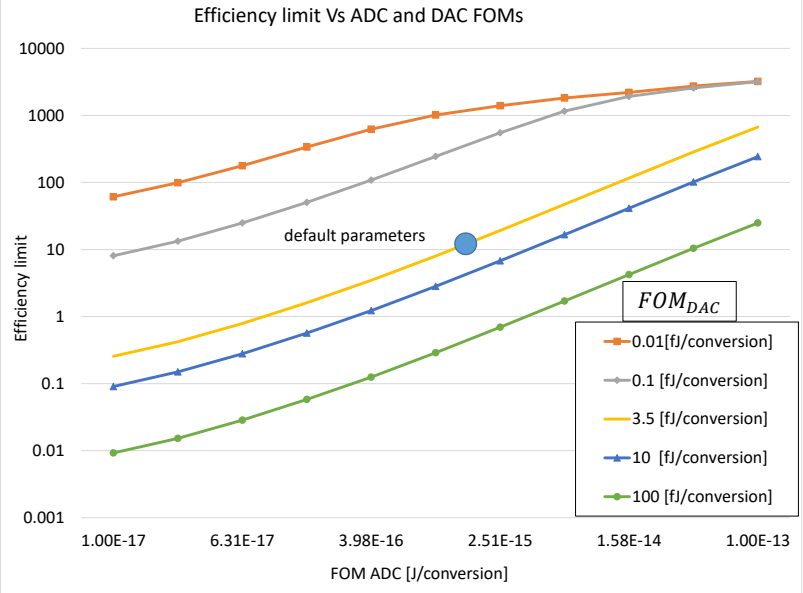

FIGURE 3.9: the efficiency limit as a function of the ADC FOM, for different DAC FOM values.

versus the swept parameters, to see what is their effect on this efficiency limit. While for all the upcoming parameters sweeps in this section the antenna input spectrum's first assumption is still held, for each step of this parameters sweeps, the unswept parameters will be fixed to their values depicted in table(3.1). The same goes for FOM values. The initial value of each swept parameter below will be mentioned by a big dot and the mention: "default parameters".

3.4.1 Efficiency limit versus ADC and DAC Figures Of Merit

Given their importance, we start the parameters sweep by ADC FOM and DAC FOM sweep. Indeed, as mentioned above, the main power consuming block in the FSC architecture is the ADC, whereas in the mixer-DAC architecture, it is the DAC, which makes these two blocks the master blocks in their respective architectures. Therefore, the efficiency limit is directly proportional to these two blocks' FOMs' ratio, as it can be seen in fig. 3.9. This holds for all the FOMs values, except when $FOM_{\text{ADC}} >> FOM_{\text{DAC}}$: in this particular case, the DAC is no more the main power consumer of the architecture it is rather the mixer-DAC ADC.

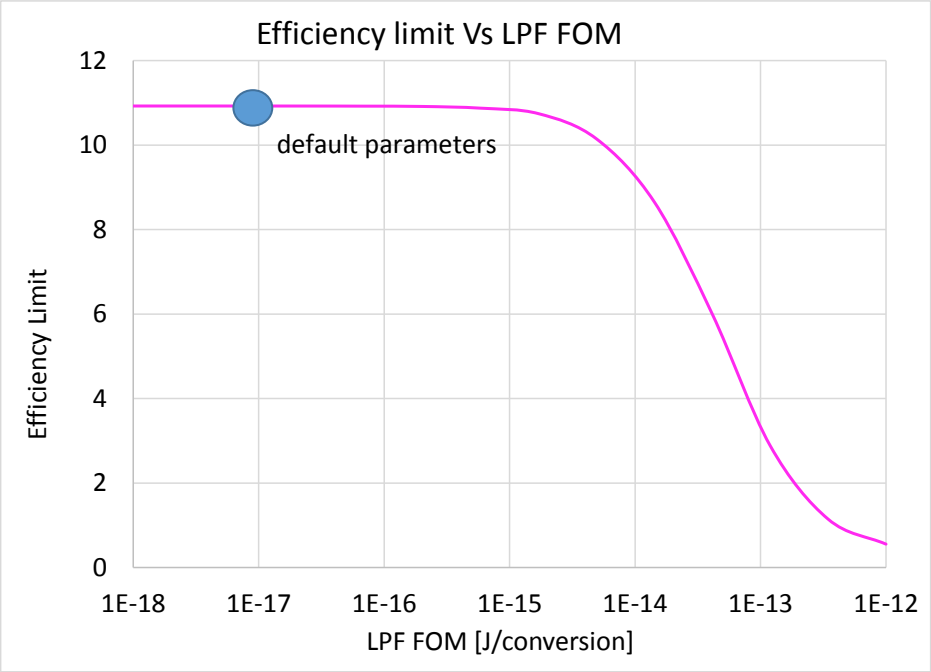

FIGURE 3.10: the efficiency limit as a function of LPF FOM.

3.4.2 Efficiency limit versus Low Pass Filter Figure Of Merit

As mentioned above, the LPF power consumption is very small compared to the DAC one. Even when we increase LPF FOM, the efficiency limit is still the same, and remains the same till the FOM exceeds the initial FOM by 3 orders of magnitude, as can be seen in fig. 3.10.

3.4.3 Efficiency limit versus Signal-to-Noise Ratio

We plotted in fig. 3.11 the efficiency limit changes for a varying SNR constraint, the "default parameters" circle being the first section comparison case. We can see in this figure that the efficiency limit increases with an increasing SNR. This means that for standards other than TV, like GSM and 4G which call for very high SNR constraints, the choice of mixer-DAC solution becomes even more relevant. The difference between the two architectures comes primarily from the difference between ADC FOM and DAC FOM. This difference is the reason why when SNR increases, the efficiency limit increases as well.

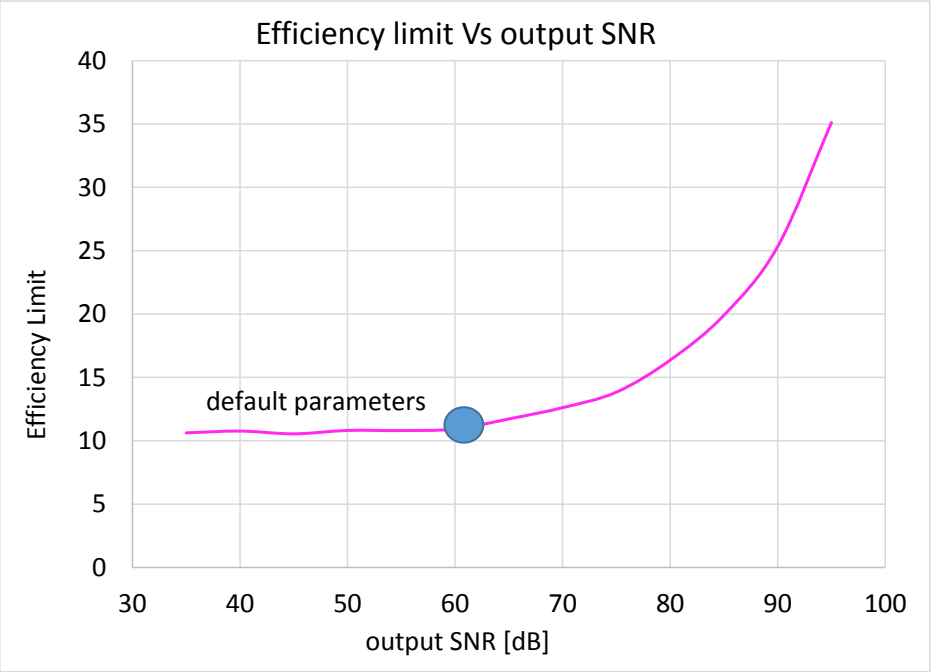

FIGURE 3.11: the efficiency limit as a function SNR.

3.4.4 Efficiency limit versus Peak-to-Average Power Ratio

In a reception chain, only the ADC is affected by Peak-to-Average Power Ratio: when PAPR increases, the ADC power consumption increases as well. So the efficiency limit in this case will only depend on FSC ADC and on mixer-DAC ADC. However, since the ADC in the FSC architecture is the main power consuming block, which mixer-DAC ADC is not, increasing the PAPR increases the power consumption of the FSC architecture considerably compared to mixer-DAC. This is why the efficiency limit increases when PAPR increases in fig. 3.12.

3.4.5 Efficiency limit versus number of channels and maximum frequency channel

In fig. 3.13, we sweep the bandwidth for a set of f_s values, while keeping the number of channels always equal to $\frac{f_{max}}{BW} = \frac{f_s}{2\,BW}$(table 3.1), this assumption simplifies considerably the comparison. In order to understand the importance of this assumption, let's examine the following cases:

Suppose we increase the bandwidth with a fixed f_s and a fixed number of channels. In this case, we run the risk of working outside of Shannon-Nyquist theorem requirements. In this case actually, the total bandwidth,

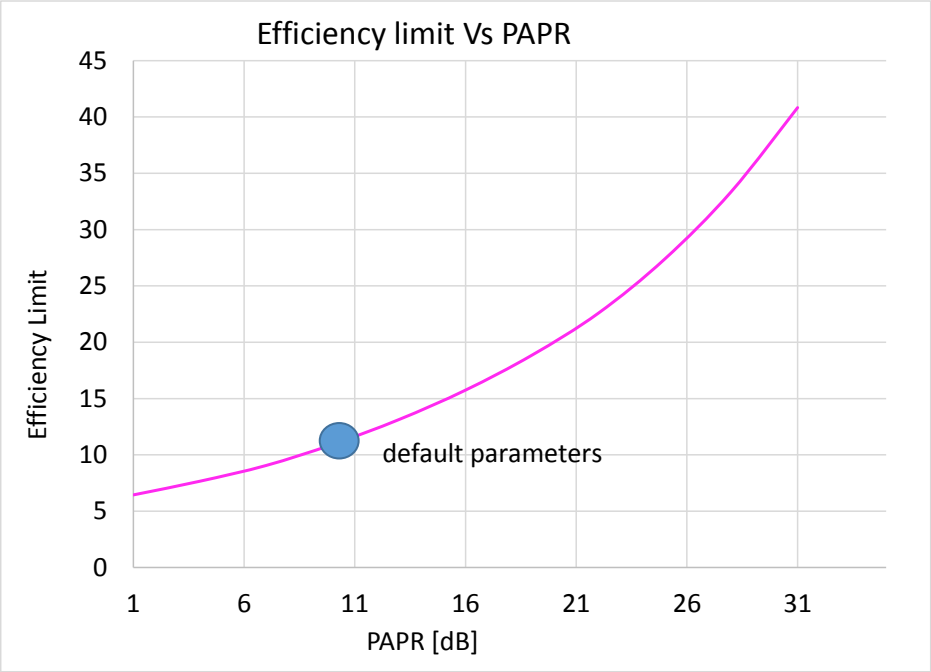

FIGURE 3.12: the efficiency limit as a function of the PAPR.

sum of all the channels bandwidths, will eventually exceed $\frac{f_s}{2}$ and then Shannon-Nyquist theorem will no more apply.

Suppose now that we decrease the bandwidth with again a fixed f_s and a fixed number of channels. In this case, we eventually get to the point where the total input spectrum is confined in a less than $\frac{f_s}{2}$ bandwidth. This means that mixer-DAC architecture will have an advantage over FSC as the DDFS spurs noise spectrum will not be totally down-converted to baseband. As the opposite case that would advantage FSC cannot be studied, we choose to discard this category of cases for the comparison to be fair, i.e. we choose to change the number of channels whenever we sweep the bandwidth for the different f_s values.

In fig. 3.13, we can see that the efficiency limit decreases when the bandwidth increases. This can be explained as follows: when the bandwidth increases, the number of channels decreases because we fixed its value according to: Number of channels $= \frac{f_s}{2\,\mathrm{BW}}$. For FSC architecture, the ADC digitizes the whole input spectrum. This means that the more channels we have, the less space each channel has on the ADC's full scale i.e. the more the wanted channels get closer to the quantification noise floor. Therefore, the SNR constraints on FSC become higher and the architecture becomes overall less power efficient compared to mixer-DAC architecture.

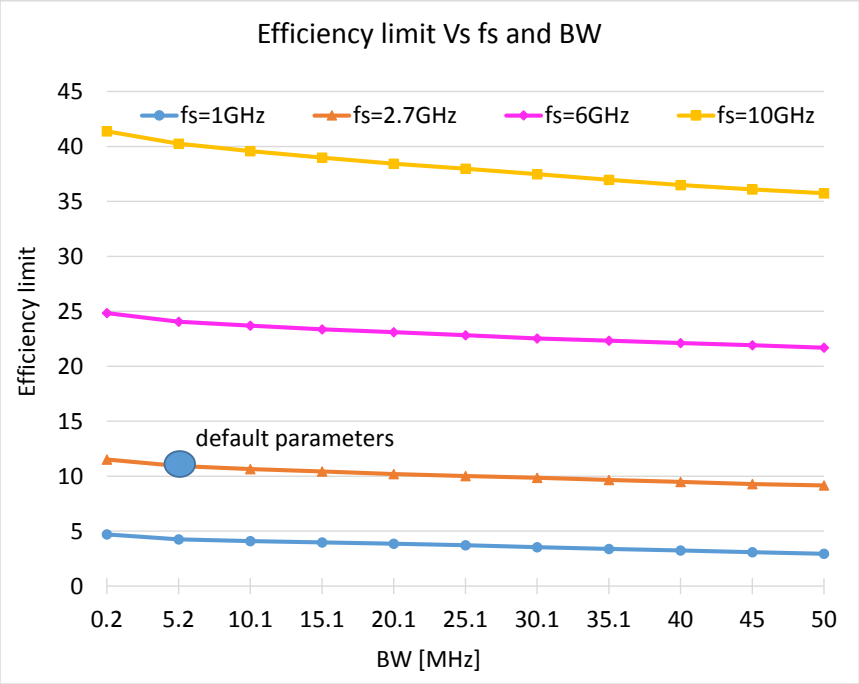

FIGURE 3.13: the efficiency limit as a function of the BW, for different fs values.

3.4.6 Comparison results for other spectrum cases

In the previous comparison, we considered a very particular case of input signal spectrum to simplify the study. Within this section, we tackle input spectrum cases that are more complicated and closer to real reception scenarios. We will show in this section that each one of these cases can be easily related to the comparison case, stated as Case 0 throughout the forthcoming discussion.

Case 1

Case 1 is depicted in fig. 3.14. It is an input spectrum with stacked channels where all the unwanted channels have the same power amplitude, say A, while the wanted channel has a different amplitude B, where: $A > B$. In fig. 3.14, we can see that the difference between wanted and unwanted channels can be translated to noise floor, where the dashed line represent Case 0 and the solid line Case 1, thus this difference can be translated to the targeted SNR to get back to Case 0: $\text{SNR}_{textCase1} = textSNR_{Case0} + (B - A)$. Therefore, Case 1 can be treated as a Case 0 with a higher SNR constraint.

So, in this case, we have to work with sensibly the same input noise than Case 0, but with a signal level that is inferior to Case 0. Therefore, if we

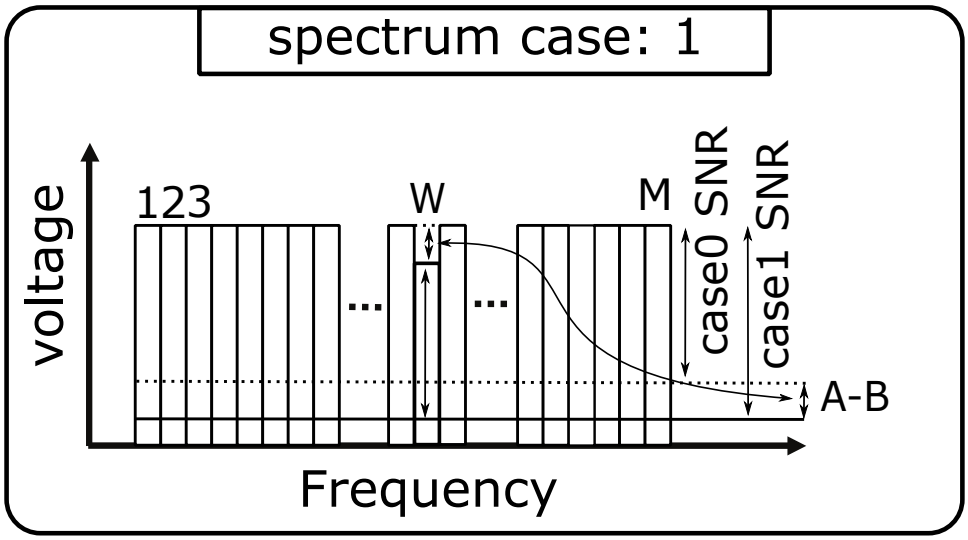

FIGURE 3.14: spectrum with equal channels amplitude, except the wanted channel "W" that have a lower amplitude.

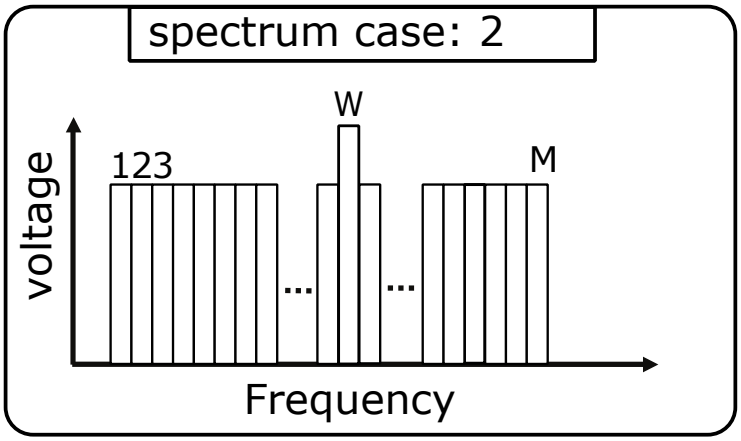

FIGURE 3.15: spectrum with equal channels amplitude, except the wanted channel "w" that have a higher amplitude.

simply increase the constraint on SNR for Case 1 as follows: $textSNR_{Case1} = textSNR_{Case0} + (B - A)$, we end up having the same conditions than in Case 0. So Case 1 is a Case 0 with a higher SNR constraint.

Case 2

Case 2 is depicted in fig. 3.15. This case is very similar to case1, but this time the wanted signal amplitude is higher than the unwanted channels amplitude, i.e. $A > B$. In this case again, we need to replace the SNR constraint on the reception chain by a new one: $textSNR_{Case2} = textSNR_{Case0} - (B - A)$: Case 2 is then a Case 0 with a lower SNR constraint.

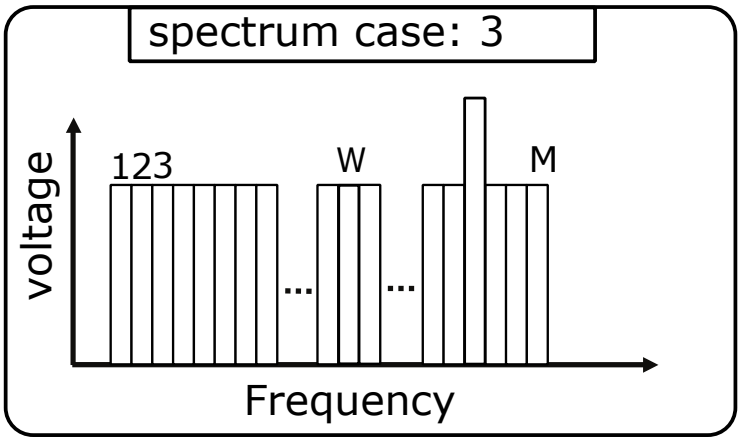

FIGURE 3.16: spectrum with equal channels amplitude, except one unwanted channel that have a higher amplitude.

Case 3

Case 3 is depicted in fig. 3.16. In this case, the input spectrum contains stacked channels, all of which have the same amplitude, say A, but one unwanted channel has a different amplitude, say B, where: $A < B$.

For this case and all the upcoming ones, we assume the noise to be uniformly distributed over the channels. This can be done for quantization noise with jittering, while noise and distortion, are not uniform [29], but their sum can be approximated to be uniform over frequency. We will consider below the impact of this spectrum on the main noise contributing blocks of both architectures: mixer block for the mixer-DAC and ADC for FSC.

With mixer-DAC architecture, the unwanted channels mix with DDFS spurs and fall at the base band. We make the assumption that all the spurs have the same amplitude: this assumption is not always true but holds with jittering. With this assumption, we can easily see that if the amplitude difference between the exceptional channel and the other unwanted channels was equally distributed between all the unwanted channels, we will end up with a Case 1 spectrum that is equivalent to our spectrum case, with unwanted channels power of $A + \frac{B-A}{textNumberofchannel}$. Since Case 1 is just a Case 0 with a higher SNR constraint, then we can consider that case3, for mixer-DAC architecture, is a Case 0 with a higher SNR constraint.

For FSC architecture, the ADC digitizes the full input spectrum. Therefore, the impact of the unwanted channels is mainly that they consume space on the full scale of the ADC input: the bigger this space is, the smaller is the space the wanted signal takes and then the more it is affected by the quantification noise. This means that the frequency distribution of the unwanted channels power does not matter as much as their total power does.

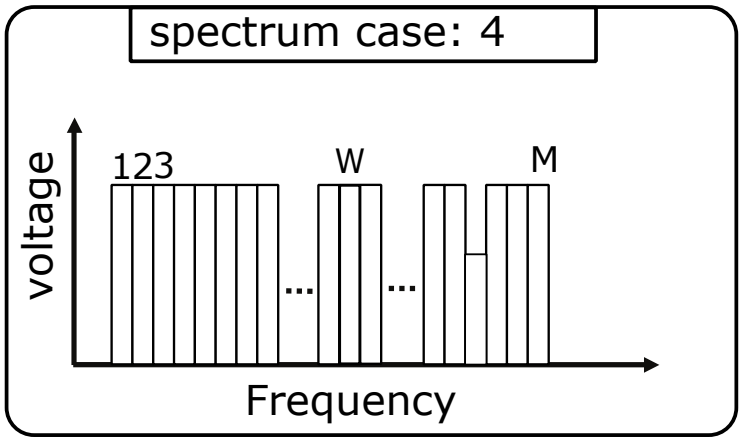

FIGURE 3.17: spectrum with equal channels amplitude, except one unwanted channel that have a lower amplitude.

So, here again, we can consider this spectrum as equivalent to one where the difference $A - B$ is distributed equally between the unwanted channels. Therefore, Case 3 spectrum is, for FSC architecture as well, a Case 0 with a higher SNR constraint.

Case 4

Case 4 is depicted in fig. 3.17. In this case, the input spectrum contains stacked channels, all of which have the same amplitude, say A, but one unwanted channel has a different amplitude, say B, where: $A > B$. This case can be treated similar to case3: since for both architectures only the total power of the unwanted channels matters, we can consider this case as equivalent to a Case 2 where the unwanted channels amplitude is equal to the average unwanted channels power. Here again, since Case 2 is a Case 0 with a lower SNR constraint, we can consider Case 4 as a Case 0 with a lower SNR constraint.

Case 5

Case 5 is depicted in fig. 3.18. This is the most general case of the input spectrum: in this case, the channels power amplitudes are random. For this case again, we can fall back to either Case 1 or Case 2 by considering an equivalent spectrum in which the unwanted channels power amplitudes are all the same and equal to the average amplitude of the unwanted spectrum channels. Case 5 is therefore a Case 0 with a different SNR constraint. Moreover, as stated above (§ 3.4.5), when the spectrum is spars the comparison gives more advantage to the FSC as in the comparison we suppose that all

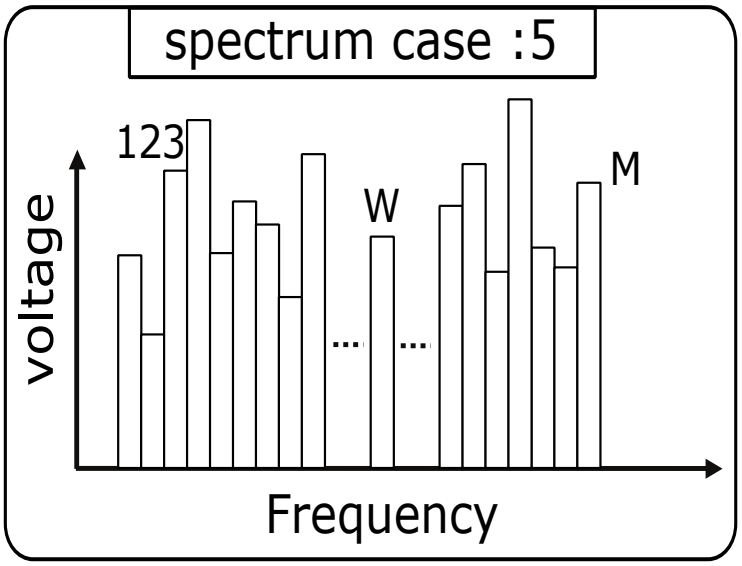

FIGURE 3.18: spectrum of random channels amplitude

DDFS spurs in the mixer-DAC solution, would mix, each with the corresponding antenna channel and down-convert on top of the wanted signal, while in the case of spars spectrum there will be some unoccupied spectrum bands, thus their corresponding spurs will not mix.

In this case also we can get back to the right number of channels of DOCSIS, simply by splitting a part of the 150 DOCSIS channel power, on the 100 unused frequency bands, to get back to Case 0 with a different SNR, in this precise case the SNR target has to be decreased by $10\log(\frac{150}{100}) = 1.76\,\text{dB}$

finally from this case we can conclude that what ever spectrum we have, we only need to get the difference between the wanted channel power and the average power of the unwanted channels(which equal to the sum of all unwanted channel divided by $\frac{f_s}{2\,\text{BW}}$), and subtract this difference from the targeted SNR of our comparison or Case 0.

3.5 Comparison conclusion

Within this chapter, we have compared the power consumption of two architectures: mixer-DAC and FSC. For the test case we considered, the conclusion is that below 11 channels received simultaneously, mixer-DAC architecture is more power efficient than FSC architecture along with the benefit of it being power scalable, which FSC is not. Above 11 channels FSC is more efficient. This holds if the user receives all of the 11 channels simultaneously 100 % of the time. However, this is not generally the case: the most common use scenarios are of a user who receives 2 or 3 simultaneous channels most of the time with short time slots in which the user receives a

higher number of channels simultaneously. In this case then, the mixer-DAC architecture becomes more power efficient than the FSC. This number of channels limit, which was named the efficiency limit, is directly and for most related to ADC and DAC FOM, and more precisely to the ratio of both. Moreover, we found that the efficiency limit goes high for high f_s standards. It also increases with the number of the antenna existing channels and with high SNR constraints. Now, given that the first comparison was conducted for a TV standard, and that all the other standards, like GSM, call for higher f_s, higher SNR, smaller channel bandwidth and larger number of channels, we can easily expect the efficiency limit to be even higher for these standards, making the mixer-DAC architecture the way to go for them.

Chapter 4

Chip implementation and measurements

4.1 Introduction

In chapter 2 we presented a G_m N-path based mixer-DAC, that exhibits promising performances when used as parallel receiver. In chapter 3 this receiver was compared, in an analytic way, to its main competitor for massively parallel reception : FSC. this comparison concluded that our proposed solution is more power-efficient than FSC up to 11 average simultaneous-received-channels. In this chapter, we will present the implemented proof of concept of the up said G_m N-path based mixer-DAC. Along this work, we capitalize on the 28 nm FDSOI technology for a compact and low power Integrated Circuit (IC).

The targets for the demonstrator are as follow:

Two receivers will be implemented on the same chip to be able to demonstrate that the proposed solution is immune to inter-receiver perturbations. The specifications are consistent with DOCSIS 3.0 definition (table 3.1):

- 5 MHz channel width.
- 100 MHz to 1 GHz total band.
- 40 dB dynamic range
- Less than 10 mW per receiver (to be consistent with chapter 3 studies)
- 13 dB maximum Noise Figure (NF).

13 dB NF is calculated to have a full chain 5 dB NF when using a 40 dB gain, 3 dB NF LNA between antenna and mixer-DAC and assuming 29 dB NF for the rest of the chain (buffer, filter, ADC...). 40 dB gain and 3 dB NF is the performances of the LNA used together with FSC in [9].

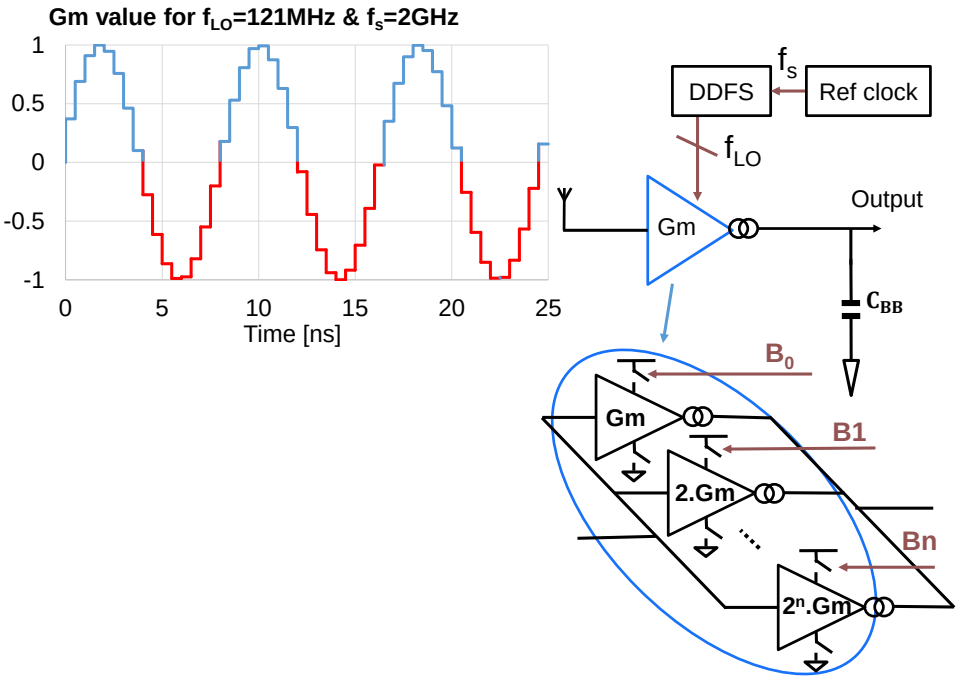

FIGURE 4.1: The wanted mixer-DAC architecture

In section (§ 4.2) we present the proposed circuit along with its design choices, sizing and simulations. In section (§ 4.3) we present the measurement test bench specifications : Ball Grid Array (BGA) and Printed Circuit Board (PCB). In section (§ 4.4) we finally present the measurement results.

4.2 Proposed circuit

After proving that the mixer-DAC solution is the most adapted to our target (§ 3.5), we implemented a novel mixer-DAC circuit based on switched-G_ms. Each G_m cell in this new architecture is a switched inverter, using inverter based G_m cell allow for implementation for low supply technologies. Switched-G_ms do also exhibit a low power consumption compared to Gilbert mixer. Our proposed solution is a low Vdd switched-G_m mixer-DAC, driven by a quantized digital sine or DDFS as proposed in 2.5 and illustrated in fig. 4.1. However, in fig. 4.1, we assume that we can create a single-ended G_m having both negative and positive values, as can be seen in the G_m value graph in fig. 4.1. This cannot be done practically though. Moreover, this architecture will also suffer from Flicker noise of the G_m cells as they are directly connected to the base band outputs.

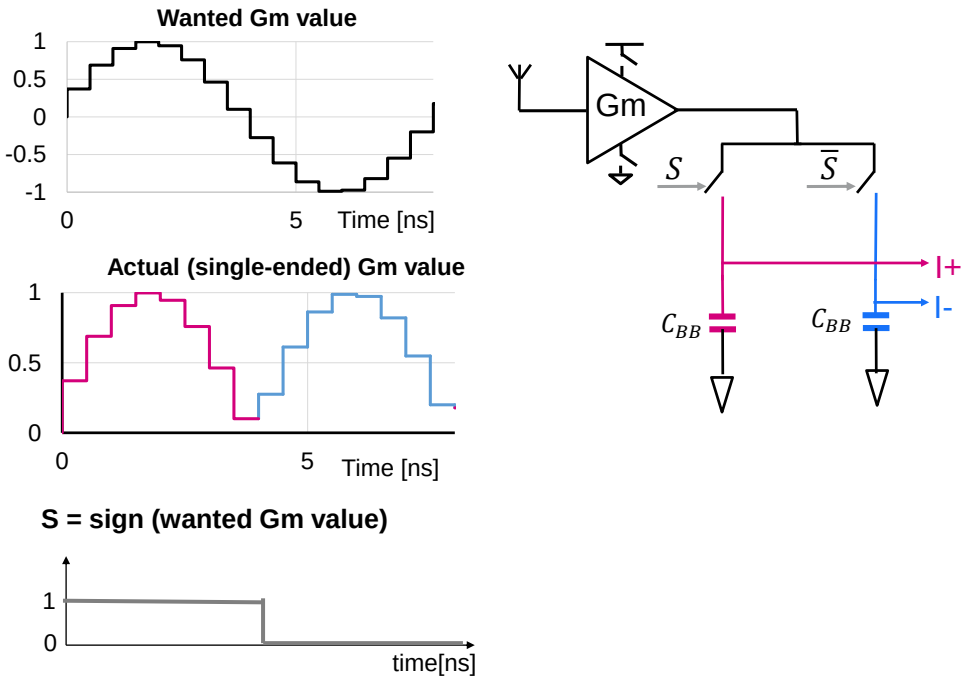

FIGURE 4.2: A 2-path filter that was introduced to cope with negative G_m and Flicker noise.

Here is a solution to cope with negative G_m and Flicker noise: we introduce a single input differential output mixer-DAC, where we replace the single output capacitance by a 2-path filter. This mainly amounts to replacing the single output capacitance by two differential capacitors, where the first one holds the positive part of the sine, and the second one the negative part. These capacitors switches are driven by the Most Significant Bit (MSB) of the sampled sine-wave and function as follows: when the positive output capacitor (I+) is connected to the G_m-bank output, we multiply the input signal with $\sin(\omega t)$, and when the negative output capacitor is connected, we multiply the input signal by $-\sin(\omega t)$. Since the output is probed in a differential way, the total output signals are brought back to the right sign. The output switched capacitors allow us to achieve a chopper behavior on the output signal, which cancels Flicker noise, while using only one single sign G_m [1]. Moreover, the combination of inverter based G_m and N-path enhances the G_m linearity, which will be explained below.

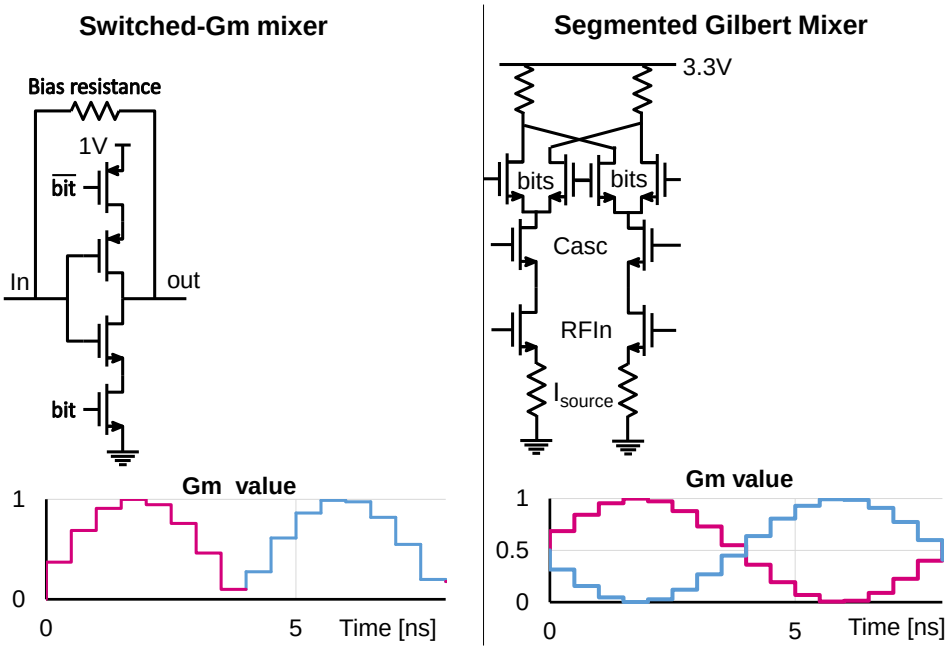

FIGURE 4.3: Switched-G_m mixer compared to segmented Gilbert mixer

4.2.1 Switched-G_m mixer low power benefit over segmented Gilbert mixer

One Switched-G_m slice is depicted in fig. 4.3, where it is the combination of one CMOS inverter, and switches on the Vdd and ground nodes, which are meant to turn on each segment when wanted, and turn it off when not. This switched-G_m transconductor, was proven to be one of the most power efficient transcoductor architectures, for a given output SNR [38]. The switched-G_m mixer is compatible with low supply voltage technologies which Gilbert mixer is not, since it contains multiple transistor levels. The switched-G_m mixer is also more power efficient since the switches it features allow for having current only in the active segments, while in Gilbert mixer, all the segments are always turned ON. To create a low value of G_m, in Gilbert mixer, two high values of G_m are subtracted, unlike in the switched G_m case, where only the low value of G_m is turned ON. Finally, the inverters in the switched-G_m mixer are a class AB biasing with current reuse. This means that they are more power efficient than Gilbert mixer which features a class A biasing.

For the inverter Nmos and Pmos sizing, we start by fixing roughly the Nmos width over Pmos width coefficient for an equal G_m, then we sweep

[1]The G_m value was kept positive here for simplicity, while the used G_m cell i.e. an inverter has a negative G_m value. This is because the value of the sign of the created G_m is not important as we need a single-sign G_m; the G_m can either be always positive or always negative

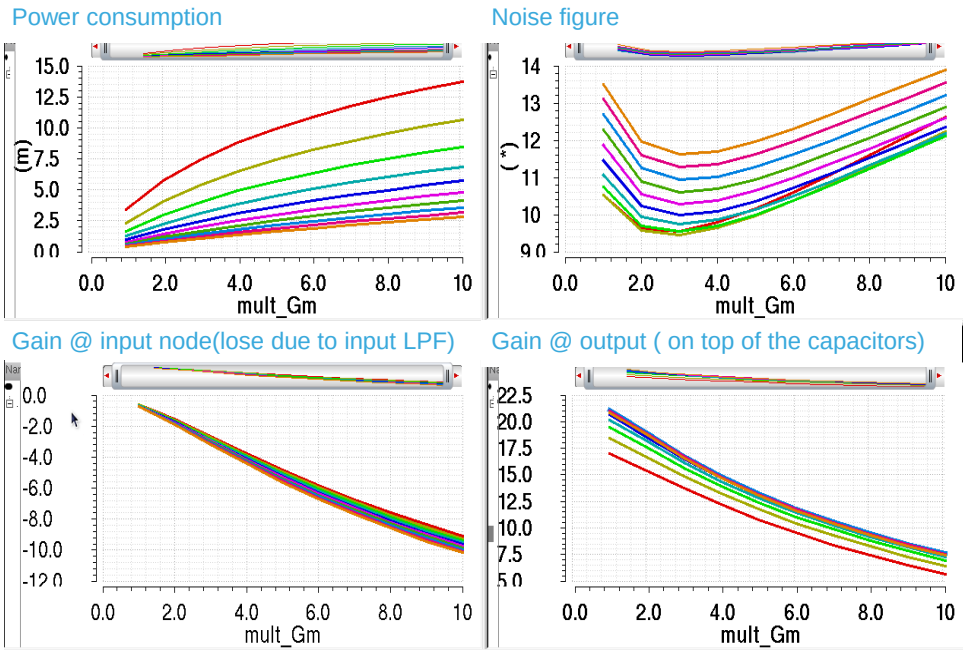

FIGURE 4.4: The simulated power consumption, NF, input and output gain, as a function of mult_G_m for a bench of MOS length (L).

both :

- L : equal to both Nmos and Pmos gate length
- mult_G_m : equal to both Nmos and Pmos number of parallel slices of the same width (1 µm for the Pmos and 300 nm for Nmos)

In fig. 4.4, we plot for every value, the simulated power consumption, NF, input gain (gain to the antenna input node, the low pass filter made of the 50 Ω antenna resistance and the G_m parasitic capacitor, can filter out the high frequency received signal) and the output gain (the input gain combined with the G_m gain). The simulated values of power consumption and NF were combined to get the NF of the G_m as a function of its power consumption, where the chosen point is shown at the same figure. Finally, a comparison table is presented in table 4.1, where the chosen size is surrounded. We can see on this table that for the other sizing, the power consumption is more than twice as high for a less than 1 dB NF enhancement.

Note that the Nmos width over Pmos width was finally fine-tuned based on the final MOS length (L) and mult_G_m values, in order to have the minimum IIP2 and IIP3 of the G_m. Moreover, the back-gate of the PMOS

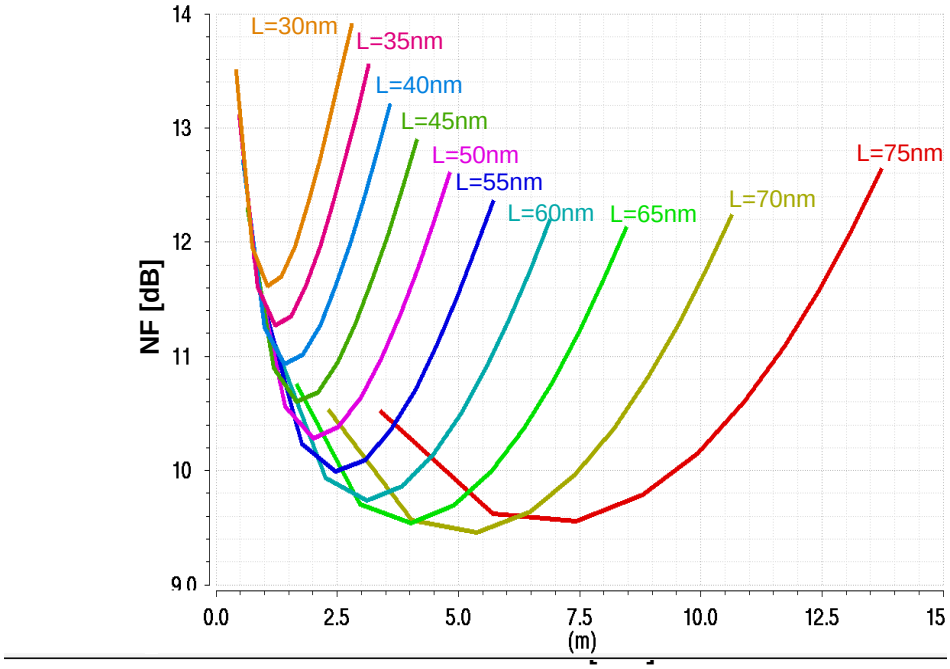

FIGURE 4.5: The simulated NF, as a function of power consumption in [W], for a bench of MOS length (L).

was connected to a pin, in order to calibrate process and mismatch effect on the Nmos and Pmos G_ms mismatch.

4.2.2 The 2-path also filters the RF signal

The combination of a G_m-inverter and the RF 2-path filter enhances the inverter linearity. Indeed, first the G_m turns the antenna input voltage into an output current. Then, due to the input impedance of the 2-path filter, which is high only around the mixing frequency and very low elsewhere as mentioned in 2, the only channel current that develops into voltage is the wanted channel. This results in a limited voltage swing at the G_m output, which enhances the G_m linearity. This applies particularly to the cross-terms $v_{\text{gs}}^2\, v_{\text{ds}}$ and $v_{\text{gs}}\, v_{\text{ds}}^2$, which tend to dominate the inverter non-linearity. Thus, the combination of an inverter-based G_m and N-path filter improves the robustness of the receiver to other interfering channels induced non-linearity.

4.2.3 The implemented demonstrator

To demonstrate switched-G_m parallel reception ability, we implemented 2 parallel I/Q receivers, even if we target a very high number of concurrently

		Rvt-30nm	Rvt-45nm	Rvt-45nm+Bgtun	Lvt-60nm+ BGTun
Power [mW]	GM	2.46	0.9	2.1	2.36
	Switch/Mem			0.5/2	
NF(100M-900M) [dB]		10.7/12. 3	10/11.8	9.75/11	10/12-14
Input LPF loss [dB]		-0.3	-0.4	-0.4	-0.9
IIP3 [dBm]		1	0	-0.5	-2
Gain(100M-900M) [dB]		21/17	26/20	26/21	35/25
Gm [mS]		50	31	46	50
Cbb for HR3 =30/35/40/43dB [pF]		76/133/230/315	26/47/83/119	41/78/124/169	14/23/45/76
BW for HR3 =30/35/40/43dB [MHz]		5/3/1.9/1.4	3.3/2.2/1.4/1	3.7/2.8/1.5/1.1	2.7/2.05/1.33/0.9

TABLE 4.1: Comparison table of 4 sizing points.

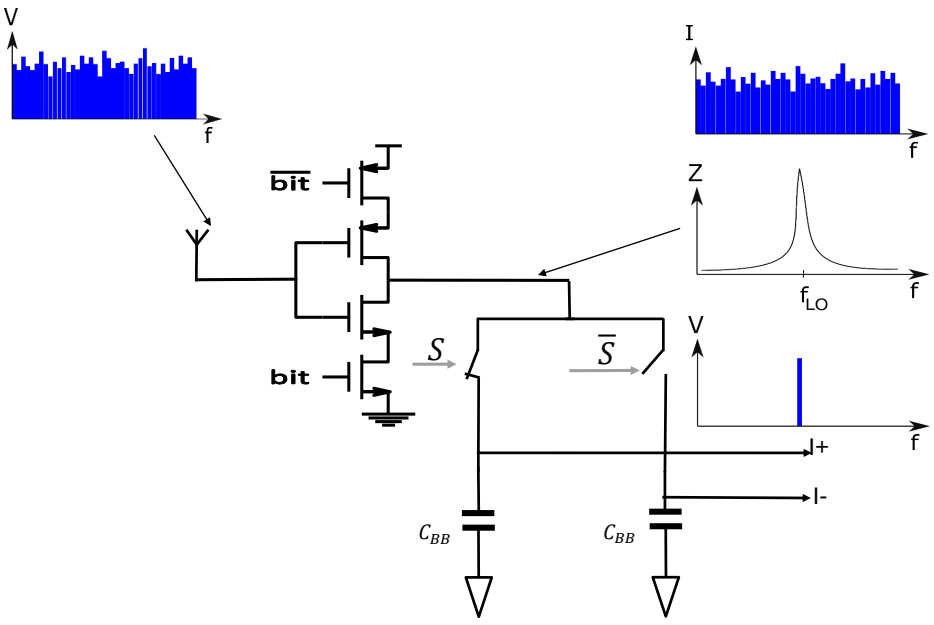

FIGURE 4.6: The 2-path benefit on the G_m linearity when added at its output.

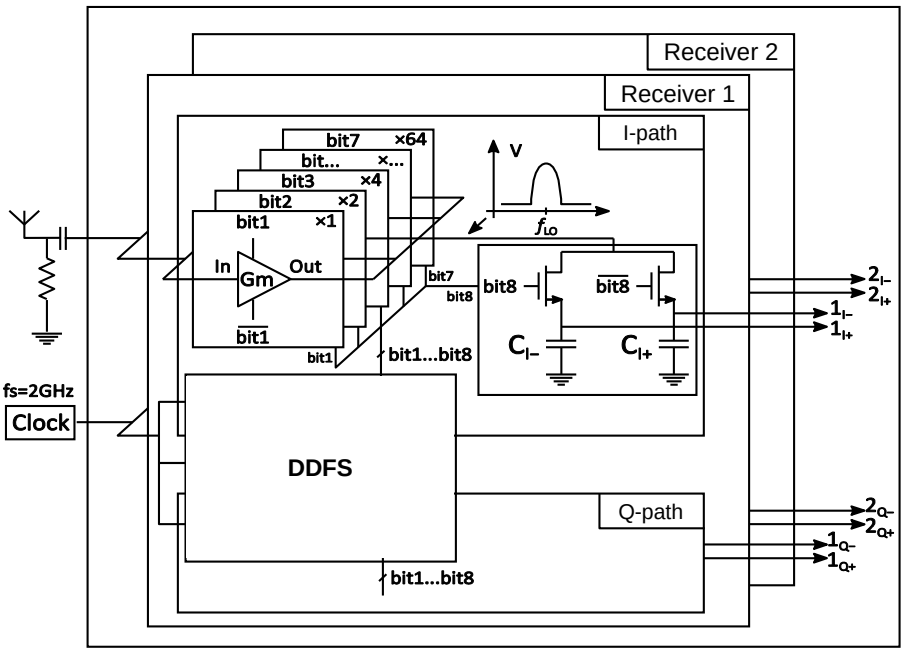

FIGURE 4.7: The implemented demonstrator IC: 2 x I/Q receivers.

working receivers. We can afford this mainly because we use DDFS, as stated before (§ 1.3). Moreover, the two receivers cross-talk will be measured, and we expect to have a very high rejection of receivers cross-talk (higher than 60 dB, which is more than what the most of telecommunication standards call for). Fig. 4.7 shows the implemented demonstrator test-chip of 2 parallel receivers, each one with I and Q path. Each parallel path is a combination of 7 binary weighted G_m bank that charges a 2-path filter, where we directly probe the output down-converted differential voltage. The 7 bits and sign bit are delivered by an internal DDFS. Please note that this is not a true 8 bits implementation. MSB nature is different form the others. If bit-8 "amplitude" does not need any particular caution (it is just a sign bit) its phase can be problematic. As the N-path transistors are not matched to the G_m transistors, it is important to balance the delays between control bit-8 and others controls. To make that, proper extraction of the parasitic has been performed.

The harmonic rejection ratio as a function of the delay between bit-8 and other bits, is presented in fig. 4.8, it shows an optimum delay of 150 ps that was implemented using two properly sized inverters in series. The added delay cell is shown in fig. 4.9 where the complete schematic of the implemented demonstrator is depicted, including 2 parallel I/Q receivers. Another delay cell is shown in the same figure, it is needed for the clock

FIGURE 4.8: The harmonic rejection ratio versus delay between bit-8 and other bits.

signal refreshing the SRAM-data after the mux. The fig. 4.10 shows the signal after the mux and both the clock before and after delay, this delay is normally meant for a better robustness against process and mismatch variations, it was also implemented using properly sized series inverters.

4.2.4 The implemented Direct Digital Frequency Synthesis

The used DDFS is a 64k bit SRAM, using a 10 bit counter to change the SRAM address. The sampled sinewave is filled externally through a Serial Peripheral Interface (SPI). To reduce power consumption, the DDFS runs at 250 MHz and a parallel to series block is used. To divide the clock frequency from 2 GHz to 250 MHz, a 3 bit counter is used instead of a frequency divider, in order to re-use those 3 signals in the parallel to series block. Indeed, the parallel to series block needs 3 non-phase-shifted signals to ensure the reconstituted data integrity. Moreover, two separate power supplies were used to reduce the SRAM power consumption as shown in fig. 4.12, where vddmp is the vdd of memory peripherals and vddma is the vdd of memory arrays, and they can be set at lower values than the nominal 1 V supply

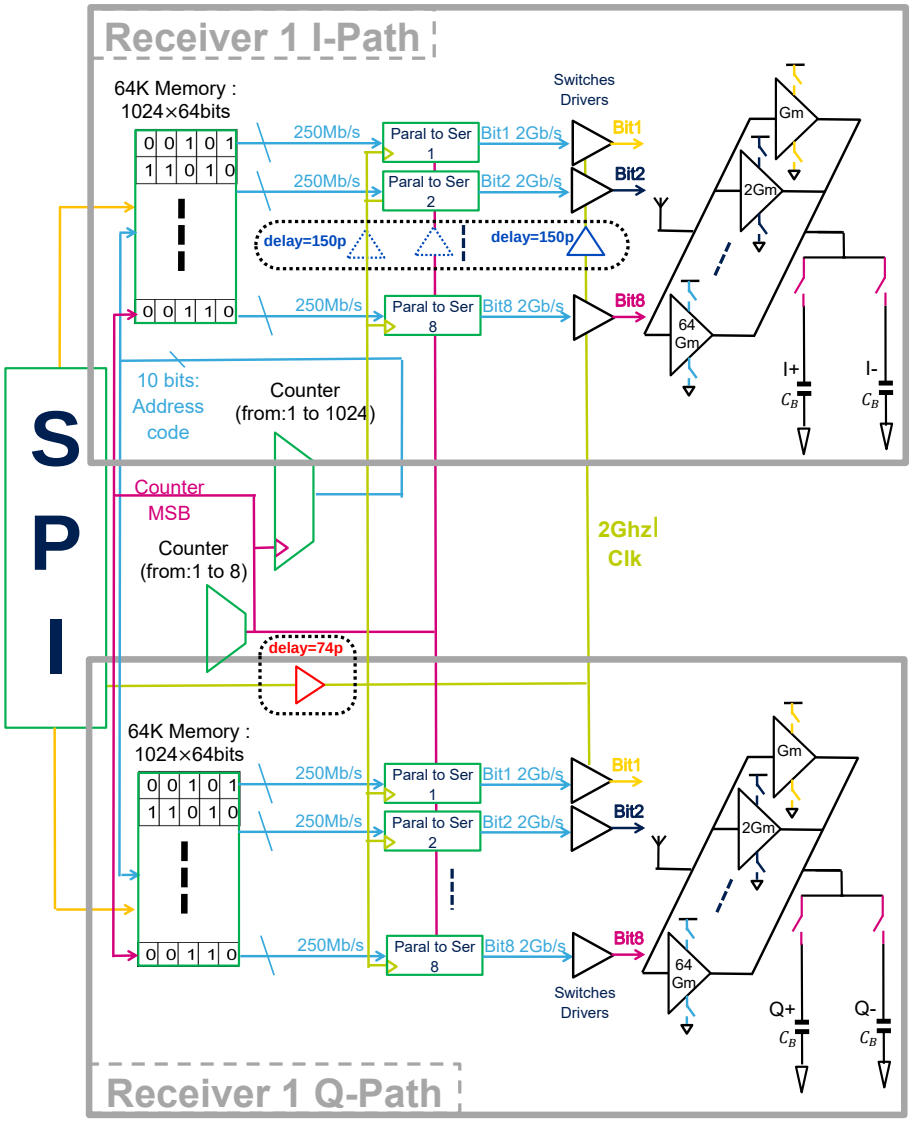

FIGURE 4.9: Half of the schematic of the implemented demonstrator including one I/Q receivers.

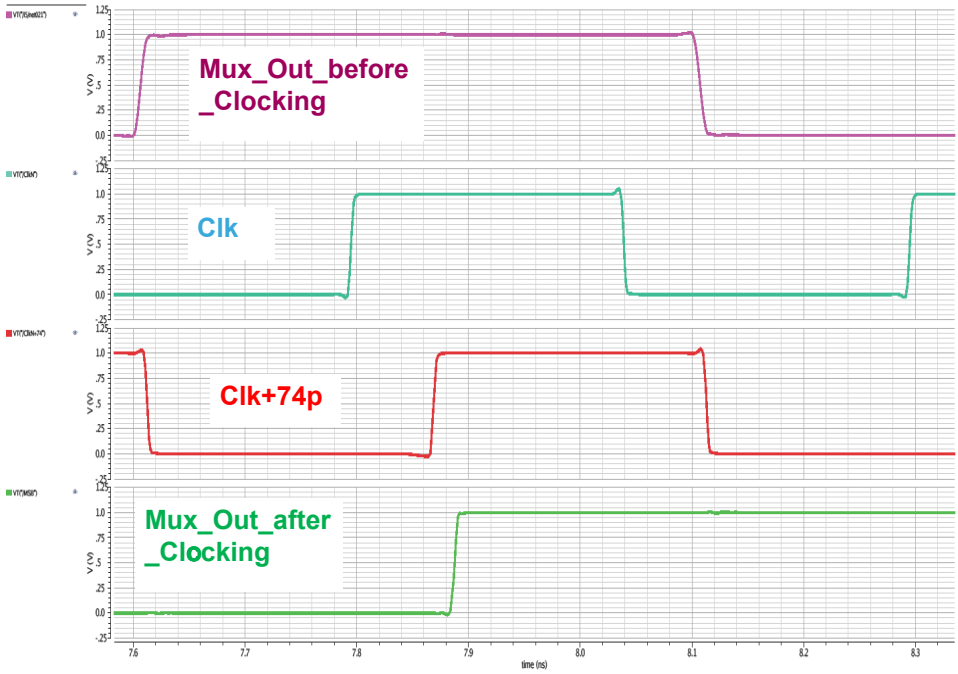

FIGURE 4.10: The need of adding 74 ps delay after muxs.

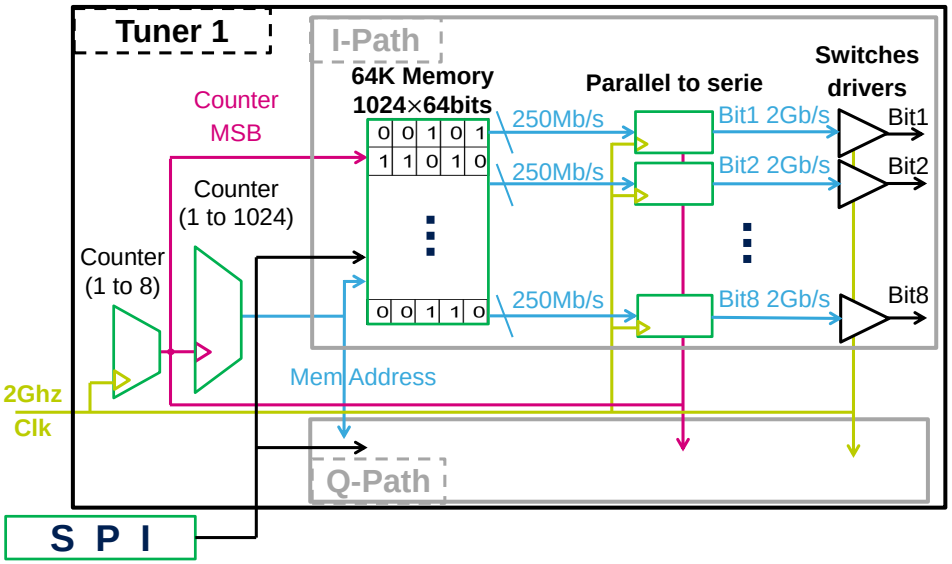

FIGURE 4.11: The implemented DDFS.

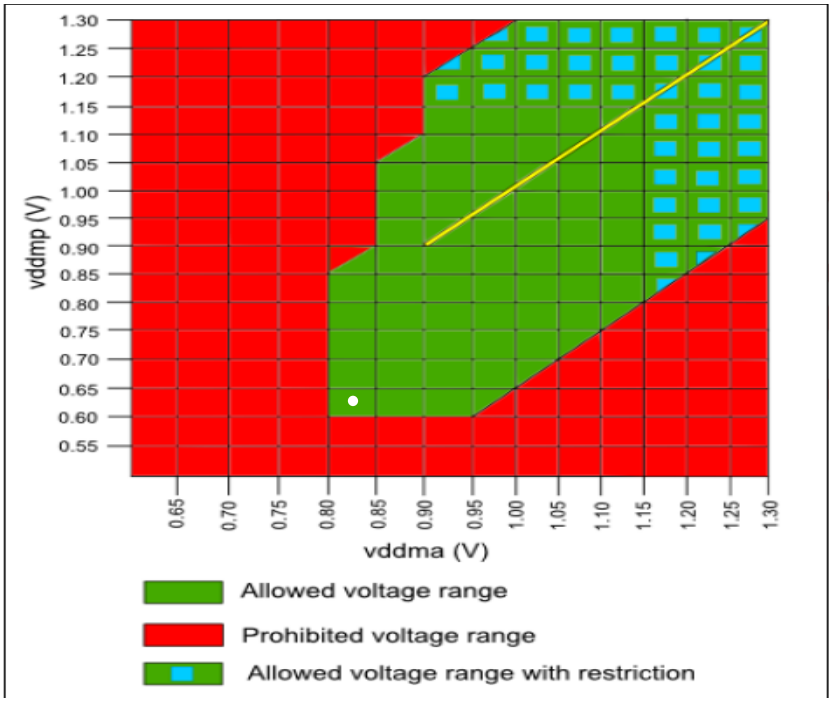

FIGURE 4.12: SRAM supported voltage range,
Vddmp is the vdd of memory peripherals and vddma is the vdd of memory arrays.

voltage. To reduce phase mismatch, one single counter is used for both I and Q paths, and the same re-clocking is shared between I and Q through a symmetric clock tree. Using an SRAM as DDFS instead of traditional DDFS [39]–[41] gives us more flexibility, which allows for using:

- pre-distorted sine-wave for mismatch correction. This means that instead of calibrating the set of G_ms, we can optimize the sine-wave codes by giving a kind of pre-distortion to the sinewave, in order to match the set of G_ms mismatch and process errors.

- quantization noise shaping, similar to what happens in sigma-delta ADC [42], [43], where the real time signal is digitized after adding the error of the last few digitization steps. This allows for pushing the quantification noise to unwanted frequency bands (generally at high frequency), called quantization noise shaping. In our case, the signal is stored, which allows for more complex calculus to shape the quantization noise. The latter can even be shaped according to the received spectrum, i.e. we can put all the quantization noise in the bands where the unwanted channels have the minimum power levels.

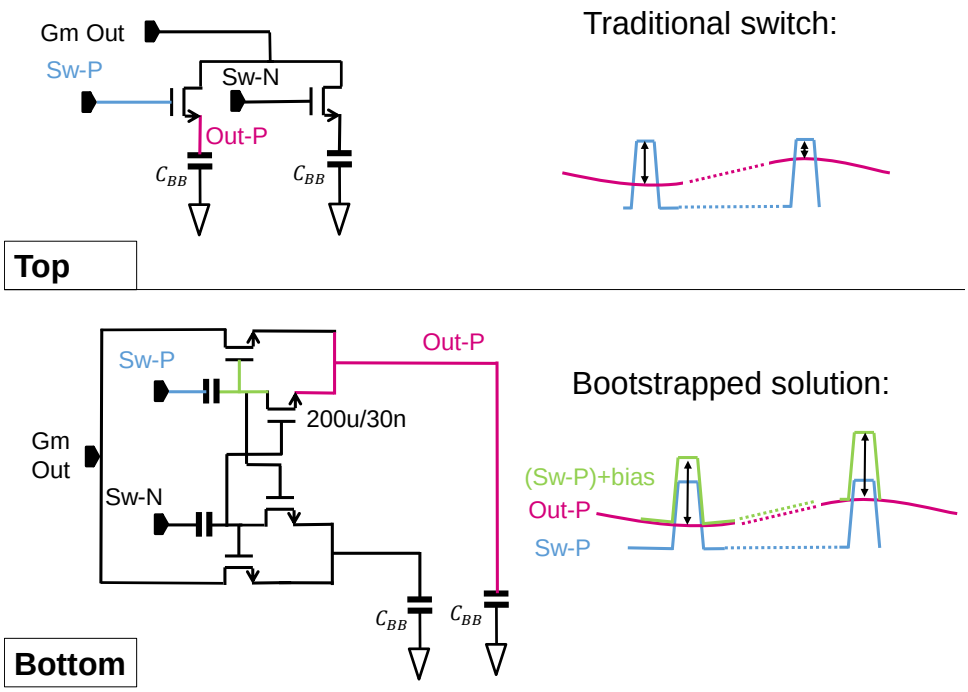

FIGURE 4.13: The implemented bootstrapped solution compared to a simple switch.

4.2.5 Capacitor switch

When using a simple Nmos transistor as the base band capacitor switch, the V_{gs} voltage will change significantly over time as shown in fig. 4.13 (Top). This results in switch non-linearity. To cope with this changing V_{gs}, we exploit a bootstrapped solution in which a second switch is added and copies the capacitor voltage to the switch gate node. This allows for a V_{gs} signal equal to the supply voltage, as shown in fig. 4.13 (Bottom). This bootstrapped solution prevents thus from switch non-linearity.

To prevent the baseband capacitors from charge sharing, we should use non-overlapping signals to drive switches. For this sake, we exploit the back-gate capabilities of FDSOI technology. The used circuit is depicted in fig. 4.14, where each of the inverters in the chain has both his back-gates connected either to:

1. ground: to increase the threshold voltage. This helps reducing the ON time of the signal that is followed by this inverter.

2. the supply voltage: to reduce the threshold voltage, which increases the ON time of the signal that is followed by this inverter.

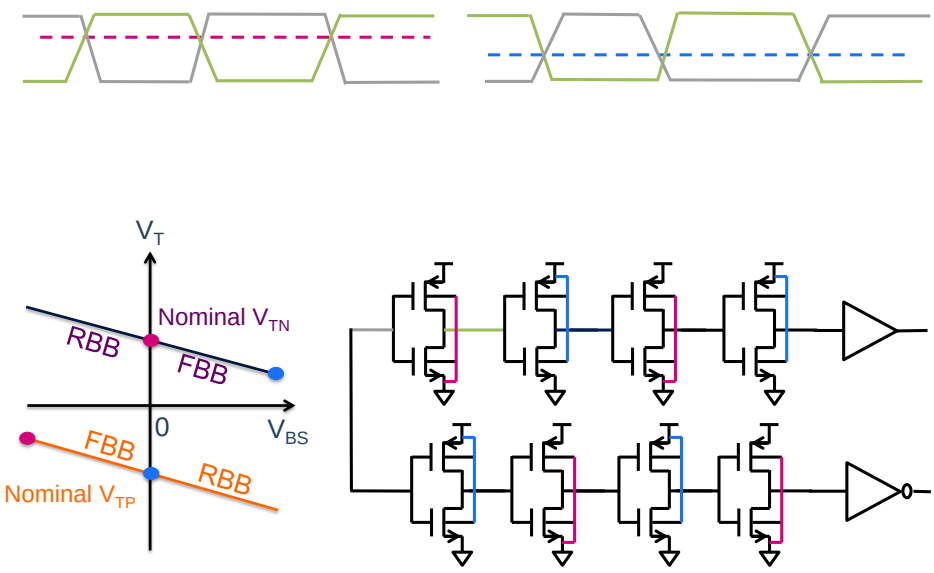

FIGURE 4.14: The used overlapping to non-overlapping circuit transformer.

Every inverter inverts the ON time and OFF time. The series combination of the inverter 1 driving the inverter 2, results finally in increasing the ON time of the initial signal by 2 times. The opposite effect happens for the series combination of the inverter 2 driving the inverter 1. Finally, we use two series combination of 8 inverters connected as shown in the fig. 4.14 to create the wanted differential non-overlapping signals.

As the charge sharing is very problematic for our circuit, it can cause gain drop that will automatically cause NF to increase, so we implemented a post-layout-simulation to make sure that the signals do not overlap due to process or mismatch variations. The simulation results are shown in fig. 4.15, where the X axis is the time delay difference between both switching signals crossing the V_{th}. This difference is equal to 3 ps and remains very close to this value for 200 simulated samples.

Even if we use non-overlapping switch signal, this circuit still suffers from charge sharing. Indeed, for one equivalent LO period, the parasitic capacitance of the G_m is half of the time connected to I+, and the other half of the time connected to its opposite signal, I-. This results in a charge sharing effect for every switching on and off, which leads to a gain drop that increases with increasing frequency.

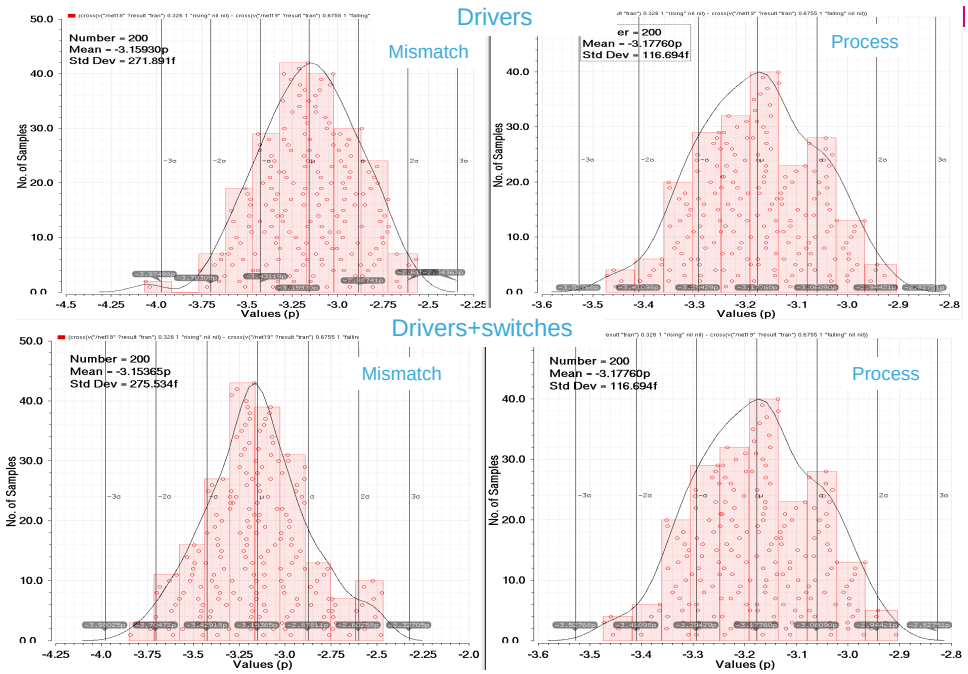

FIGURE 4.15: capacitors switches and switch drivers process and mismatch simulations.

4.2.6 G_m switch driver

The SRAM output is single ended, and every unit G_m needs two opposite signals to drive both NMOS and PMOS switches. In order to create a differential signal out of the single ended output of the SRAM, we use the circuit in fig. 4.16. In the latter circuit, two transmission gates stages followed by an inverter latch or flip-flop each, are used to ensure the signal integrity along with the minimum phase shift between NMOS and PMOS switches.

4.2.7 Mixer-DAC layout and chip photo

The common centroid mixer-DAC implemented is shown in fig. 4.17. It is made of 7 binary weighted G_m slices. The decoupling capacitors were put as close as possible to the G_m slices. For the inverter to act as a G_m, a low capacitor-switch resistance is needed, therefore a large switch transistor is chosen. The parasitic capacitance of the switch transistor is in parallel with big base band capacitors, which means it has no real impact.

In fig. 4.18 the chip micrograph is depicted.

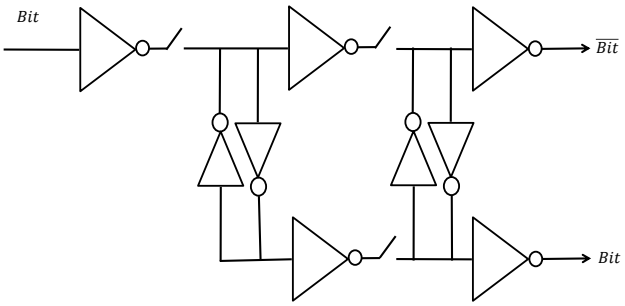

FIGURE 4.16: The used single to differential G_m-switch driver.

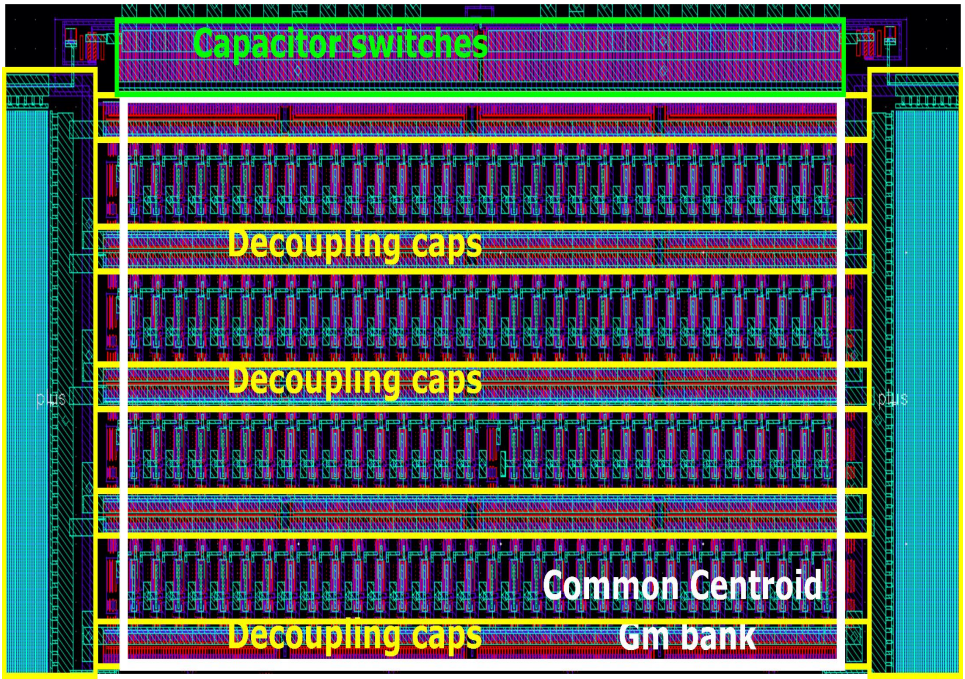

FIGURE 4.17: Common centroid mixer-DAC layout.

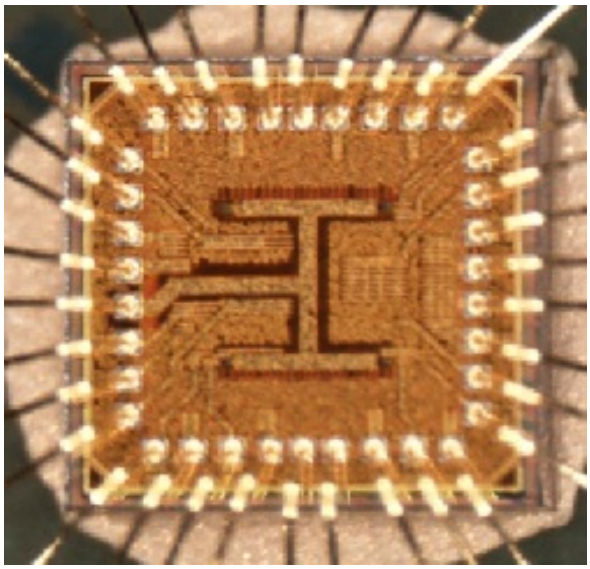

FIGURE 4.18: Chip micrograph.

4.3 Test bench

4.3.1 Ball Grid Array design description

A low-parasitic dedicated BGA package was developed in collaboration with [44], for demonstrator testing. The connection of the BGA to the test board should be maintained by pressing the chip on the PCB solder footprint. This is a socket-less solution, which helps avoiding additional parasitics. The size of the provided solution is a compromise between the connections' parasitics, which require the smallest possible size and the feasibility of the solder footprint on the test board. Therefore, the BGA is designed with:

- 8x8 balls - 4.6mm x 4.6mm
- 0.5mm pitch, 0.3mm ball diameter

The BGA packaging contains IC wire-bonded to the package substrate. Most of the circuit pads are connected to the peripheral BGA balls in order to enable easier PCB routing. The rest of the central BGA balls is used as an equi-potential ground plane. All the different supply nodes have a multiple ball contact to lower the resistance. fig. 4.20 and fig. 4.19 shows the BGA balls distribution and the BGA layout respectively.

The packaging RF inputs were simulated and the results for the clock input are show in fig. 4.21: the transfer function shows that the signal is fully transmitted to the chip till 2 GHz, which is the input clock frequency. The

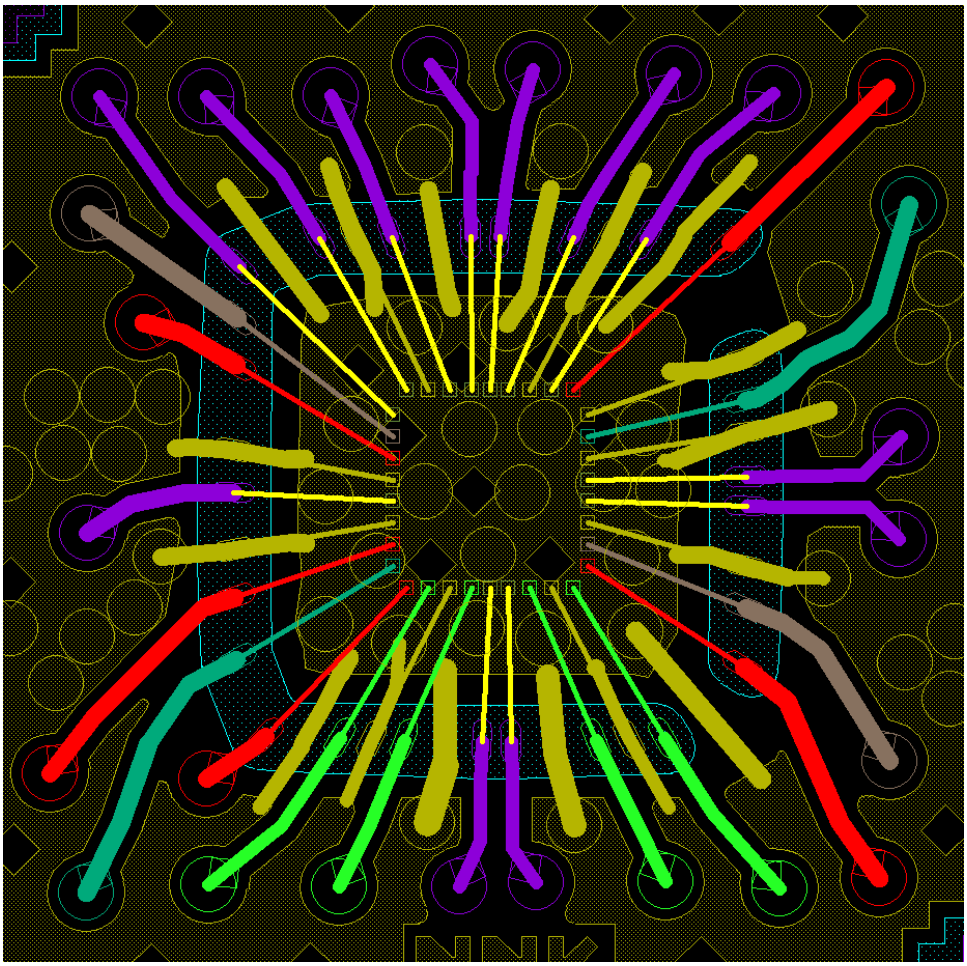

FIGURE 4.19: BGA layout view.

results of the antenna input simulation are shown in fig. 4.22, showing a maximum rejection of 0.2 dB for the maximum antenna signal at 1 GHz.

4.3.2 Printed Circuit Board design description

A dedicated PCB was designed for testing the implemented demonstrator in proper environment. The PCB is shown in fig. 4.23, it provides the necessary off-chip components, such as:

- 50 Ω SMA connectors used for RF antenna input, LO sine input and IF outputs, where RF paths are designed as 50 Ω impedance co-planar wave guides.
- LO and RF input are provided by a 50 Ω matching resistance

	1	2	3	4	5	6	7	8
A	BG	Out_IP1	Out_IN1	NSS	MISO	Out_QN1	Out_QP1	Vdd
B	Vdd_mp	Vdd_mp	Vdd_mp	GND	GND	Vdd_ma	Vdd_ma	Vdd_ma
C	Vdd	Vdd	Vdd	GND	GND	GND	GND	GND
D	GND	GND	GND	GND	GND	GND	GND	LO_P
E	RF_In	GND	GND	GND	GND	GND	GND	LO_N
F	GND	GND	GND	GND	GND	GND	GND	GND
G	Vdd	Vdd	Vdd	GND	GND	Vdd_mp	Vdd_mp	Vdd_mp
H	Vdd_ma	Out_IP2	Out_IN2	MOSI	SCK	Out_QN2	Out_QP2	Vdd

FIGURE 4.20: BGA ball netlist and distribution.

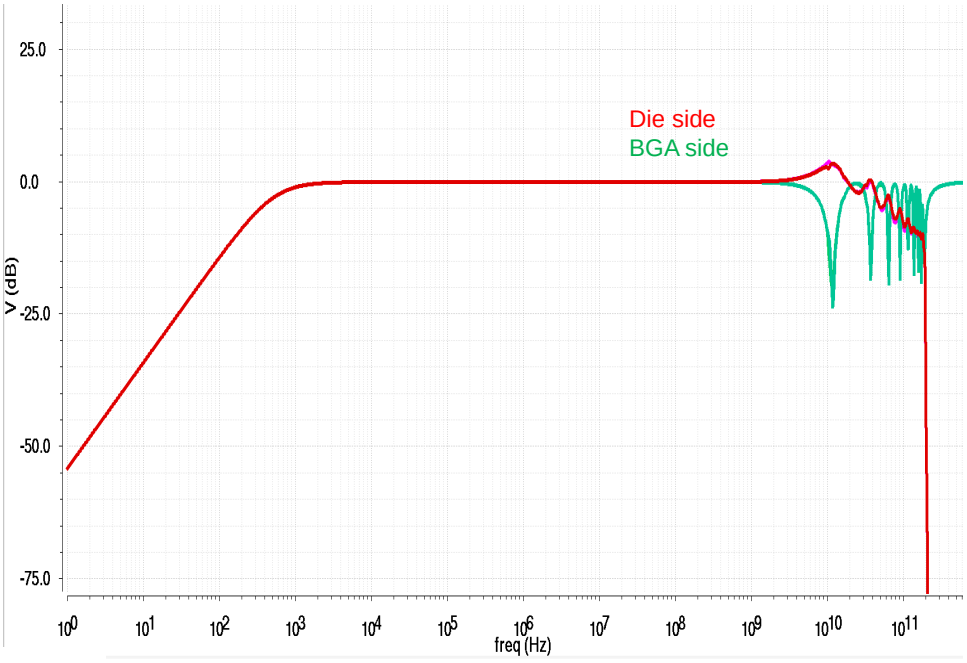

FIGURE 4.21: Package RF simulation of both clock inputs P and N (that are superposed).

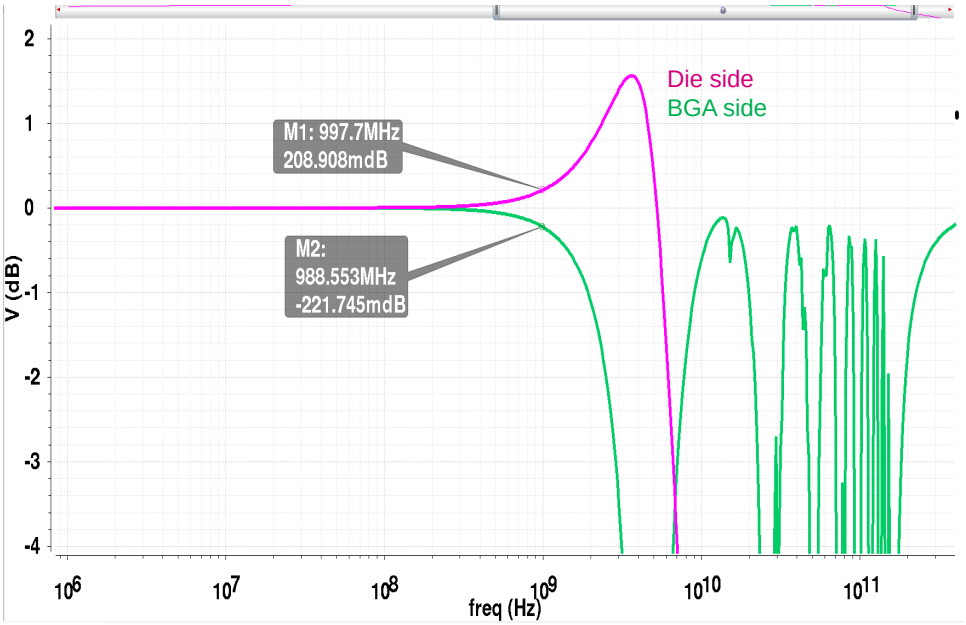

FIGURE 4.22: Package RF simulation of antenna input.

- both IF I+ and I- or Q+ and Q- outputs can be combined and measured through a low noise differential amplifier in unity gain configuration or can be probed directly through vertical SMA
- Voltage supply can be provided in two ways, either directly from the external voltage source or through a voltage regulator (Low-dropout regulator, LDO) . The choice is made by placing the set of jumpers in proper positions as shown in fig. 4.24. Many decoupling capacitors were added near to the chip and the LDO for every different voltage supply.

4.3.3 Measurement bench

The LO data samples are calculated in Matlab. To be able to load this data to the chip, a nucleo interface[2] was used as an SPI-master. For every simulation data, the LO samples must be calculated, then transferred to the chip through SPI. The SPI does also read back the different SRAM data, to ensure that

[2]The nucleo interference can be found in market, it comes with built-in SPI master, that need only few tuning to match its communication protocol to the precise kind of SPI communication protocol used in the SPI slave

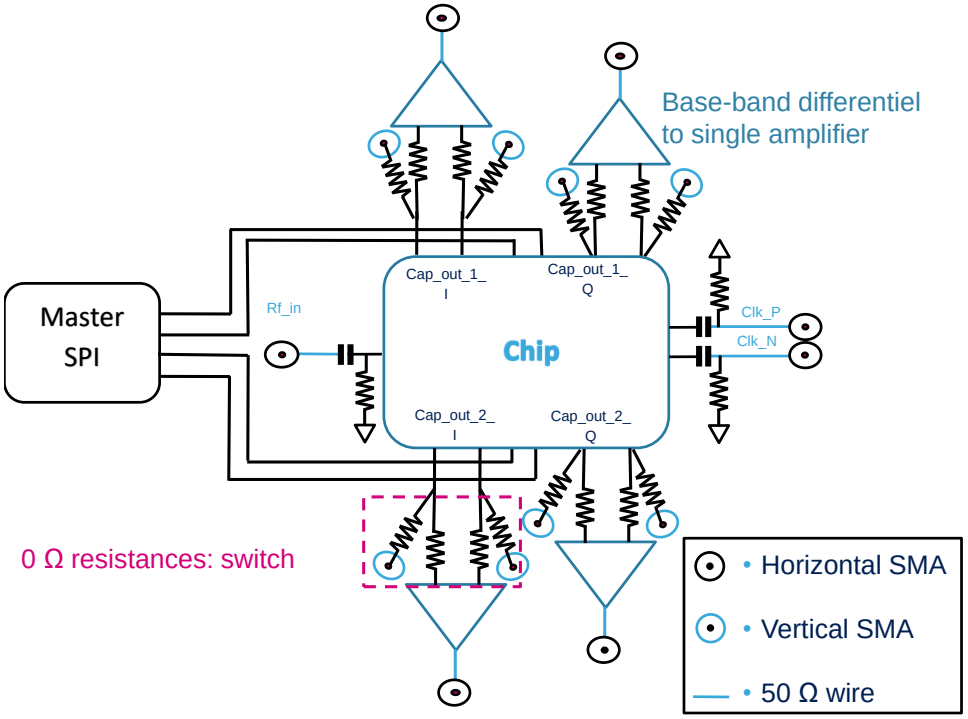

FIGURE 4.23: PCB schematic of functional components.

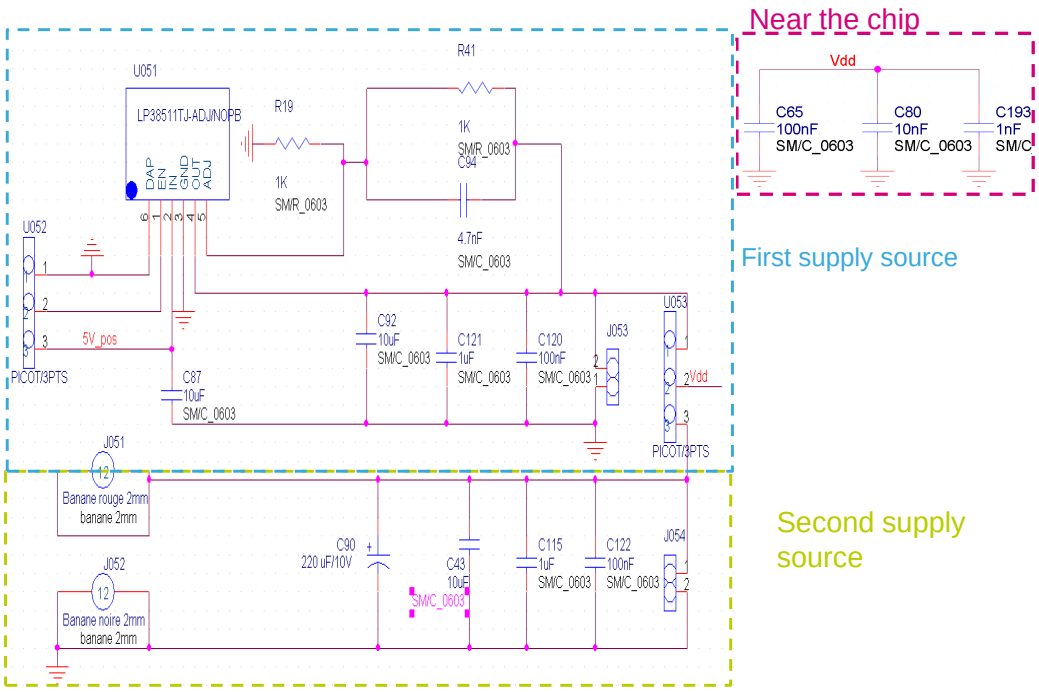

FIGURE 4.24: PCB schematic of the dedicated power supply
to each one of the 4 different power supplies.

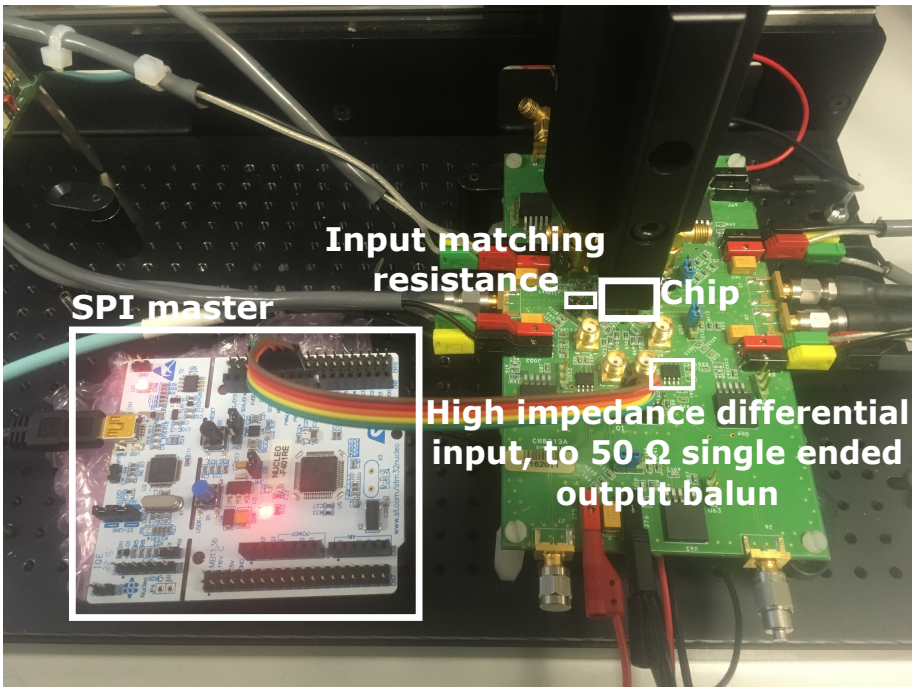

FIGURE 4.25: Measurement bench.

no errors were made during writing, and spots the errors addresses. To be able to run optimization loops on measurements, some measurements were automated.

Samples calculation along with SPI communications verification and measurements automation were implemented using a Python code.

The fig. 4.25 shows the measurement bench that includes the PCB, the nucleo board and the chip in the PCB along with the mechanical system used to press the chip on the PCB in order to have good electrical contacts.

4.4 Measurements results

The presented measurements results are at PCB connector level and thus include losses and noise coming from PCB and off-chip matching-resistance and are based on the use of an external clock of 2 GHz. fig. 4.26 shows the measured gain versus LO-frequency. It drops gradually from 33 dB at 0.1 GHz to 23 dB at 1 GHz due to charge sharing between the baseband capacitors and the parasitic output capacitance of the G_m-blocks mentioned earlier. The NF increases according to the gain drop from 7 dB at 0.1 GHz to 13 dB at 1 GHz. In fig. 4.27, the NF and gain versus IF-frequency are depicted. Thanks to the bit-8 chopping, the Flicker noise corner frequency is measured at 20 kHz instead of the usual hundreds of MHz in short length technologies such as 28 nm FDSOI. The 1st order G_m-C low pass filtering

shape is also depicted in the same figure, with a 3 MHz cut off frequency. To measure the Harmonic Rejection Ratio (HRR), we use an optimization loop. This optimization loop introduces a phase shift between both the positive and the negative parts of the sine-wave [3], then measures the different HRR. The algorithm chooses then the optimal new phase-shift based on three point results, which amounts to calculating the middle of the best two points out of three. This operation is then repeated until the HRR enhancement is less than 0.1 dB. The optimized HRR is shown in fig. 4.28 and remains above 44 dB for the 100 MHz-1 GHz spectrum band. Each HR-'N' is plotted from 100 MHz to $\frac{1}{N}$ GHz. We can notice that for frequencies above 333 MHz, the HR-2 enhances, because the algorithm considers only the HR2 from 333 MHz to 500 MHz, and the same goes for the other HR-'N' shown in the figure.

fig. 4.29 shows the IIP2 versus offset frequency, where $\Delta f = f_2 - f_1$, $f_1 = f_{LO} + 500\,\text{kHz}$ and $f_{LO} = 106\,\text{MHz}$, f_1 f_2 being the two tones present at the input and used to measure the IIP2. The measured values vary from 20 dB at $f_{-3\,\text{dB}}$ to 20 dB at $90 \cdot f_{-3\,\text{dB}}$. The measured IIP3 is shown in fig. 4.30, it is also plotted versus Δf, i.e. the offset frequency where Δf, f_1 and f_2 keep the same values than for the IIP2. The measured IIP3 values varies from -10 dB at $f_{-3\,\text{dB}}$ to 18 dB at $110 \cdot f_{-3\,\text{dB}}$. Both IIP2 and IIP3 plots show the linearity benefits obtained from the combination of 2-path and inverter based G_m, which filter out the unwanted channels, reducing their non-linearity contribution.

In fig. 4.32, the image rejection of the receiver is plotted versus equivalent LO frequency or bit-8 frequency. This IRR drops over frequency, due to the central clock phase mismatch between I and Q paths, which becomes more important at higher frequencies.

The inter-receiver LO coupling rejection, versus the difference between the two receivers' bit-8 frequencies is shown in fig. 4.31. Rx1 LO (LO1) was set to 100 MHz and Rx2 LO (LO2) to 100 MHz+Δf. Two tones were set at RF input: f_{in1} at LO1 + 80 kHz and f_{in2} at LO2 + 90 kHz. The rejection ratio is then the ratio between the output signal of Rx1 at 80 kHz and the output of the same receiver at 90 kHz that is down-converted due to the coupling of LO2 to Rx1. The inter receiver LO coupling rejection shows a better than 75 dB rejection. That, combined to the use of a single central clock, makes the proposed solution suitable for parallel reception. Demonstrator performance/consumption can thus be extrapolated to an N-parallel tuner.

[3] Positive and negative here means before applying the absolute value on the sinewave, which was mentioned earlier

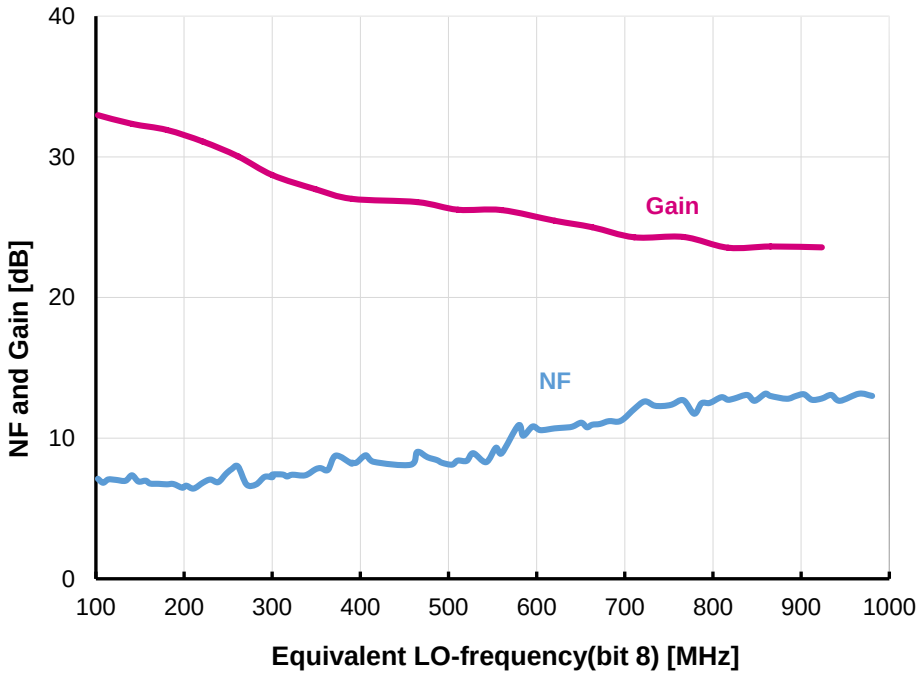

FIGURE 4.26: Measured NF and conversion gain versus equivalent LO-frequency (bit-8), for a constant IF-frequency=500 kHz.

Fig. 4.33 compares the demonstrator to the state of the art receivers for the same frequency range. The achieved noise figure is in the same range as the others, but as expected/targeted, the clean dynamic range is narrower (roughly >40 dB versus >60 dB for others) to reduce power consumption. Each I/Q receiver consumes 9.5 mW: 5 mW for analog (Mixer DAC plus drivers) and 4.5 mW for digital (SRAM plus counter), which is 26x-34x lower than for the high performance targeted designs. Note that with a Dynamic Range (DR) of 56 dB our solution would consume 25 mW approximately (as explained later on in (§ 4.5)), which is 12 times less than FSC power consumption[4], which is near to the 11 power efficiency calculated in 3.

[4] 12 in this case would be for a mixer-DAC having 4 dB less in harmonic rejection and 12 db more NF than FSC [9]

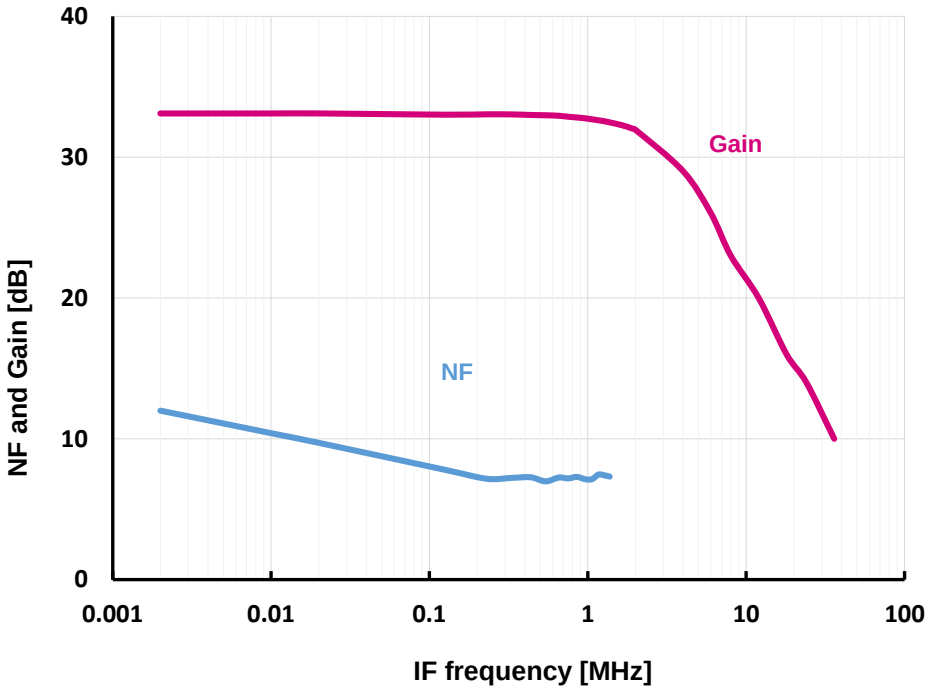

FIGURE 4.27: Measured NF and conversion gain versus IF frequency at constant equivalent LO-frequency (bit-8)= 100 MHz.

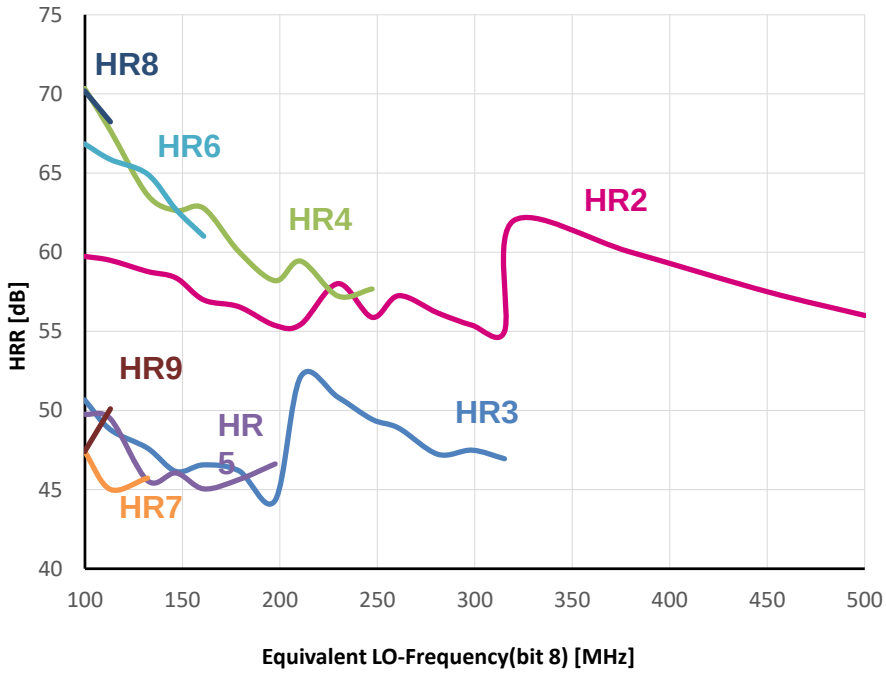

FIGURE 4.28: Measured harmonic rejection ratio of all harmonics from 2 to 9.

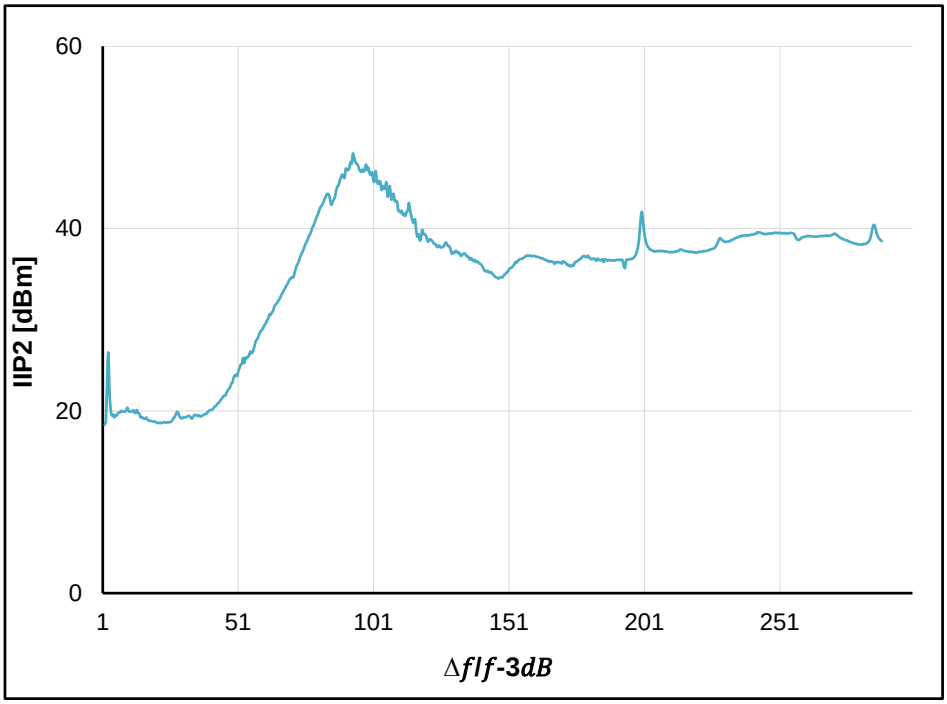

FIGURE 4.29: Measured IIP2 versus offset frequency where $\Delta f = f_2 - f_1$ and $f_1 = f_{LO} + 500\,\text{kHz}$ and $f_{LO} = 106\,\text{MHz}$.

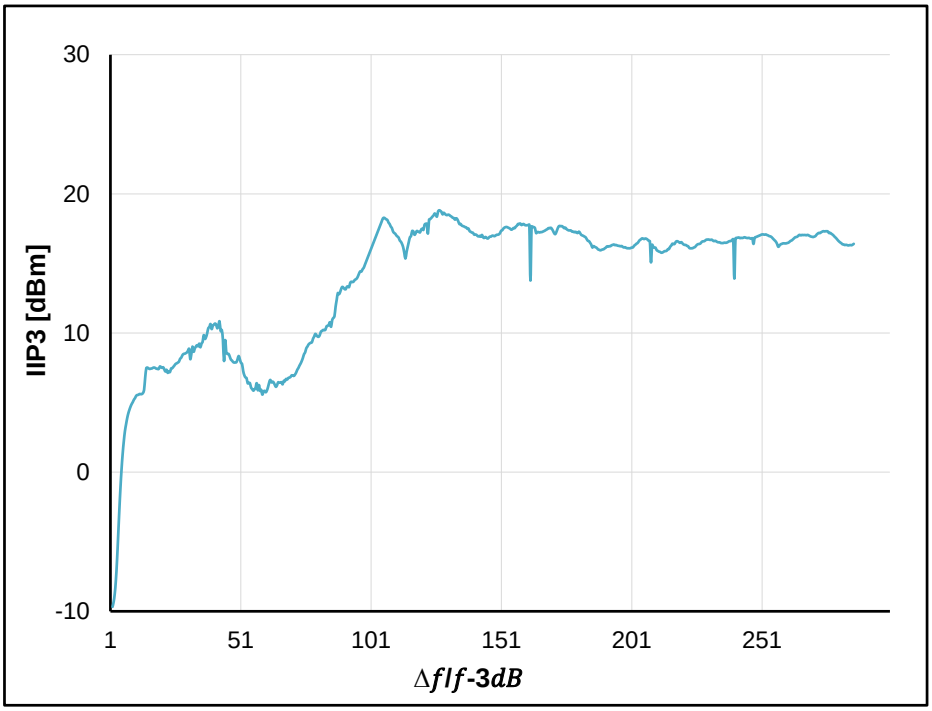

FIGURE 4.30: Measured IIP3 versus offset frequency where $\Delta f = f_2 - f_1$ and $f_1 = f_{LO} + 500\,\text{kHz}$ and $f_{LO} = 106\,\text{MHz}$.

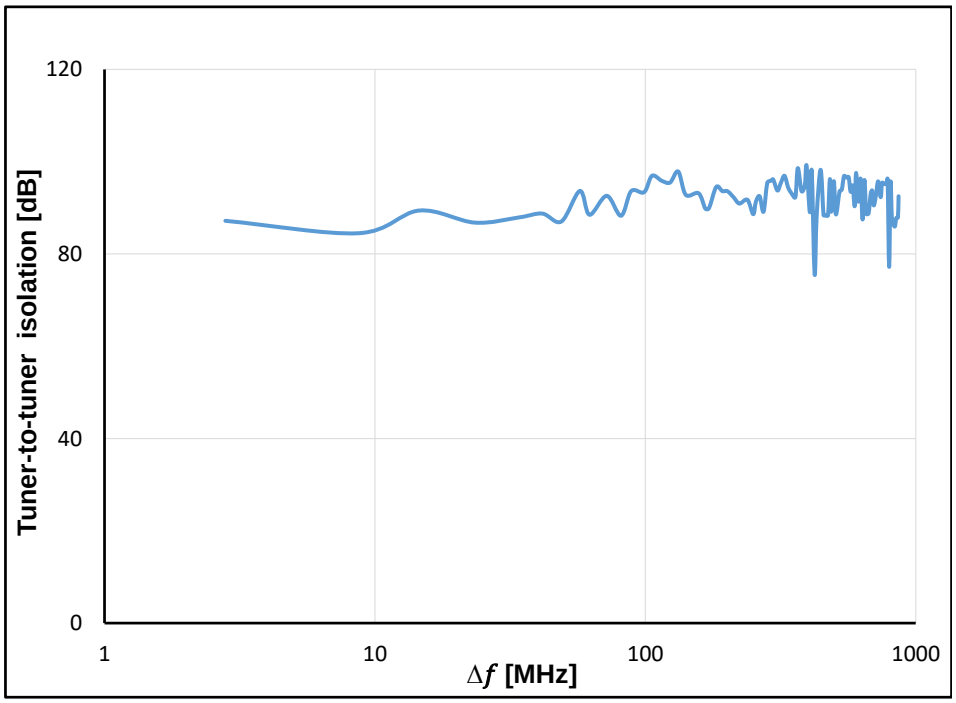

FIGURE 4.31: Measured rejection of Rx2-fundamental coupling to Rx1.

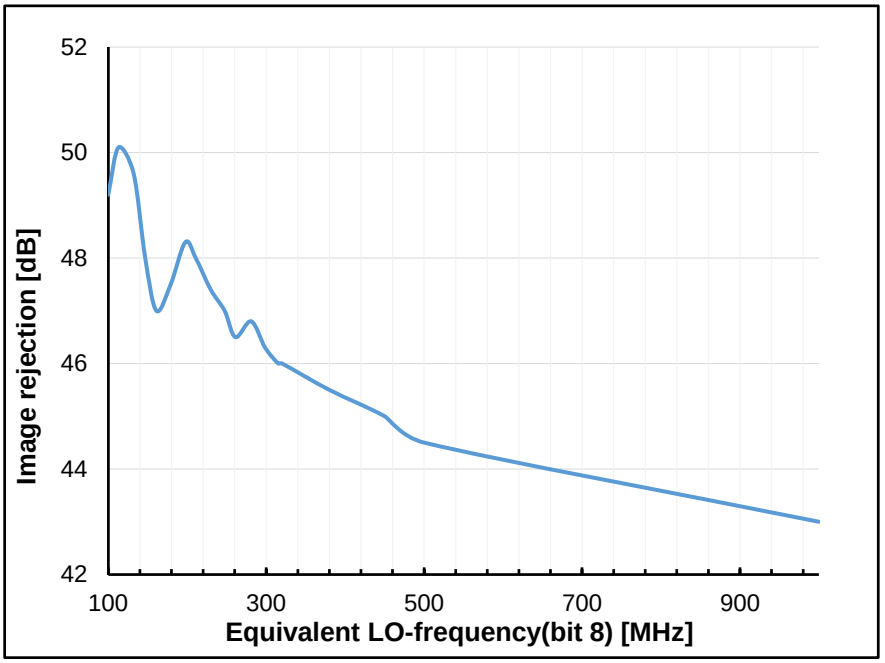

FIGURE 4.32: The measured image rejection of the receiver , versus equivalent LO frequency or bit-8 frequency.

	This work	F.Gatta	J.Wu	A.Maxim
Architecture	Low IF mixer DAC	Low IF mixer	Full Spectrum Sampling	Low IF mixer DAC
Numbre of DDFS bits	8		>12	10
Frequency range [MHz]	100-1000	48-1000	48-1000	48-1000
Gain [dB]	23-33	-	-	-
HRR [dB]	44	65(w/ RF Filter)	-	60
Image Rejection [dB]	42	62	70	65
IIP3 [dBm]	2-16	-	-	20
NF [dB]	7-13	5-7	25.4 w/ digital	13
Isolation[dB]	<-75	-	-	-
Number of channel	2	2	158	1
Power consumption [mW]	19(w/ DDFS)	650	300(only ADC)	450
Power/channel [mW]	9.5(w/ DDFS)	325	1.9(only ADC)	450
Scalable power	yes	yes	no	yes
Total die area [mm²]	1	10	1	1.2
IC Technology	28nm FDSOI	65nm CMOS	28nm CMOS	0.13umCMOS

FIGURE 4.33: comparison table.

4.5 Conclusion

In this chapter, we presented the implemented circuit along with its sizing, simulation and measurements. The architecture exploits a digital sine-weighted switched-G_m Mixer-DAC for power efficiency, followed by a current mixer with embedded 2-path filter for improved interference robustness and low $1/f$ noise. The digital sine is generated via a look-up table that drives the Mixer-DAC. Two 6 MHz receiver channels were realized on a demonstrator chip covering 100 MHz-1000 MHz, achieving 23 dB-33 dB Gain, 7 dB-13 dB NF, >42 dB Image Rejection, >41 dB worst case harmonic rejection, and better than 75 dB cross-talk rejection between the channels. Each channel consumes <9.5 mW, 5 mW for analog and 4.5 mW for the SRAM and counter (digital sine generation).

General conclusion and perspectives

Conclusion

In this thesis, the target was to explore the best solution for massively parallel reception. The first aim was to find a power scalable solution (consumption decreases when you need less data rate) while preserving the advantages of existing solutions (low chip area and robustness to interferences).

High level idea was to implement power efficient channelized receivers (the RF band is divided into channels and circuit is composed of multiple receivers each capable of processing one channel), all driven by a single clock to avoid interferences.

Using channelized receivers is a flexible solution where the number of active receivers matches the number of really needed channels, making power consumption dependent on needs. This is a clear advantage compared to FSC (Full Spectrum Capture), which consumption is constant, whatever the number of carriers is needed. To be able to create such a solution, it was needed to propose a "parallel reception friendly" receiver with following characteristics:

- Reconfigurable, to be able to address any channel.
- Driven by a central clock (not related to the channel center frequency).
- Robust to the other channels perturbations (seen as blockers).

We started by exploring the N-path based receiver, getting benefit from its low power and area along with its RF filtering capabilities.

As N-path limitation in parallel reception context is input impedance, we developed an intuitive and simple way to calculate it in a general case.

This novel way to calculate input impedance has been used to explore new N-path arrangements. One original N-path receiver solution has been proposed, compatible with parallel reception. This receiver architecture nevertheless has a penalty in term of NF and has not been selected as solution for our research.

To find another trade-off between input impedance and NF, we introduced an active Gm element (with the consumption and linearity drawback) in the structure.

A novel receiver architecture based on G_m N-path that include harmonic rejection capabilities has been proposed: G_m N-path based mixer-DAC.

The architecture exploits a digital sine-weighted switched-Gm mixer-DAC for power efficiency, followed by current mixer with embedded 2-path filter for improved interference robustness and low $1/f$ noise. The digital sine is generated via a look-up table that drives the Mixer-DAC. this architecture was patented (§ 4.5).

This G_m N-path based mixer was compared, in a DOCSIS context, to its main competitor (FSC) in an analytic way, where we proved the power efficiency of our proposed solution up to an average of 11 simultaneously received channels, which is representative of the general usage of a cable TV-box. Moreover the comparison shows that the up-said efficiency limit of 11, increases with:

- the maximum received signal frequency.
- the targeted output SNR
- the input PAPR
- Spectrum sparsity
- Blockers dynamic

which make our solution even more attractive for other standards such as cellular communications (4G and 5G)

A silicon demonstrator of our architecture, including two parallel receivers was implemented in 28 nm FDSOI technology. This demonstrator include both RF/analog part and digital part, thus the circuit was simulated using proper mixed mode simulation test bench.

A complete test environment has been created to validate the demonstrator.

- Dedicated BGA
- Dedicated PCB
- Dedicated SPI communication interface
- Dedicated measurement automation software.

Measurement results, conform to expectations, demonstrate the validity of the concept and it's adequation with parallel reception constraints.

Circuit and it's results have been presented in Custom Integrated Circuits Conference (CICC) 2017 [18].

Future work

The circuit developed in this work is very close to DOCSIS requirements. This is because the best solution (before this work) to address parallel reception was the FSC, and FSC is DOCSIS dedicated.

- One first perspective is to create a DOCSIS product and thus increase the dynamic up to 60 dB.

  As dynamic range of the receiver is fixed by the SNR equation:

  $$\text{SNR} = 6.02N + 1.76 \tag{4.1}$$

  Thus, an extra 12 dB on dynamic range means 2 more bits in the mixer-DAC(from 8 to 10), i.e. 4 times analog power consumption and $\frac{2}{8}$ more digital power consumption, meaning a total power of 25 mW approximately.

- One other open research area can be explored with current hardware. As the sine wave, used for the down-conversion, is store in a SRAM, the circuit can be programmed to make a multiplication with a non sine wave. This feature has already been used to add some pre-distortion (to compensate for mixer-DAC non linearity). similarly, this feature can be used to shape the quantization noise, the same way a sigma-delta ADC does, to reduce the LO signal power, in the band where the blockers are present. It is possible also to generate "two-tones" signals to down-convert two carriers with a single mixer-DAC.

- Finally, architecture can be further optimized for the 5G perspective. 5G specifications will be very demanding, in term or blockers levels. Two topics can be explored:

  - Changing the nature of the BB filtering (capacitor only up to now) to implement higher order filtering.
  - Change the gm function to be able to create a filtering function (notches) at the input of the Gm

List of publication

International Conference paper

Reda Kasri, Eric Klumperink, Philippe Cathelin, Eric Tournier, Bram Nauta, "A Digital Sine-Weighted Switched-G_m mixer for Single-Clock Power-Scalable Parallel Receivers" CICC 2017 [18].

Patent

Bram Nauta, Reda Kasri, Eric Klumperink, Philippe Cathelin, Eric Tournier, : "Système de réception radio parallèle à mélangeurs-amplificateurs analogiques commandés numériquement." patent.

Poster

- Reda Kasri, Eric Klumperink, Philippe Cathelin, Eric Tournier, Bram Nauta, : "Massively parallel reception" Poster STMicroelectronics (Crolles).
- Reda Kasri, Eric Klumperink, Philippe Cathelin, Eric Tournier, Bram Nauta, : "Massively parallel reception" Poster University of Twente (Twente, The Netherlands).

Appendix A

Input impedance of LTV N-path calculation

For an input signal at the same frequency as f_{LO}, each capacitor will always see the same quarter of the input sine-wave, for every switch-on window. The capacitor will thus hold the mean value of this quarter sine-wave. The combination of switch resistance and source resistance, then sees a voltage difference equal to the input voltage minus its mean value held by the capacitor, resulting in a current flow equal to this voltage difference over the sum of resistances, as shown in fig. 2.13. This current average is equal to zero, nevertheless it should be counted in the input impedance calculus, where the LTI model does not include the capacitor voltage "memory-effect".

To calculate the amplitude of the "extra-current". First, we calculate the average value of each quarter of the sine-wave that will be held by each capacitor. Then, we can calculate the voltage across the combination of source and switch resistors, to finally get the flowing current in this combination of resistors and thus in every capacitor as illustrated in fig. A.1.

The voltage across the first capacitor V_{C1} is a fixed voltage equal to the average of the quarter of the sine-wave as illustrated in fig. A.1(in this figure the input signal and the LO signal have the same initial phase. To calculate $Z_{\text{in, mem}}(k\, f_{LO})$ in a general case, let us suppose that the input signal is phase-shifted by θ over the LO signal. Then, the average voltage across the different capacitors can be expressed as follows:

$$V_{Ci}(k\, f_{LO}) = \frac{4}{T} \int_{(i-1)\frac{T}{4}}^{i\frac{T}{4}} A\, \sin(k\, \omega_{LO} t + \theta)\, \mathrm{d}x.\ \ i = 1, 2, 3, 4 \tag{A.1}$$

Then the values of V_{Ci} depending on θ and k are :

- $V_{C1} = \frac{2A}{\pi} \left(\cos(\theta) - \cos(\frac{k\pi}{2} + \theta) \right)$

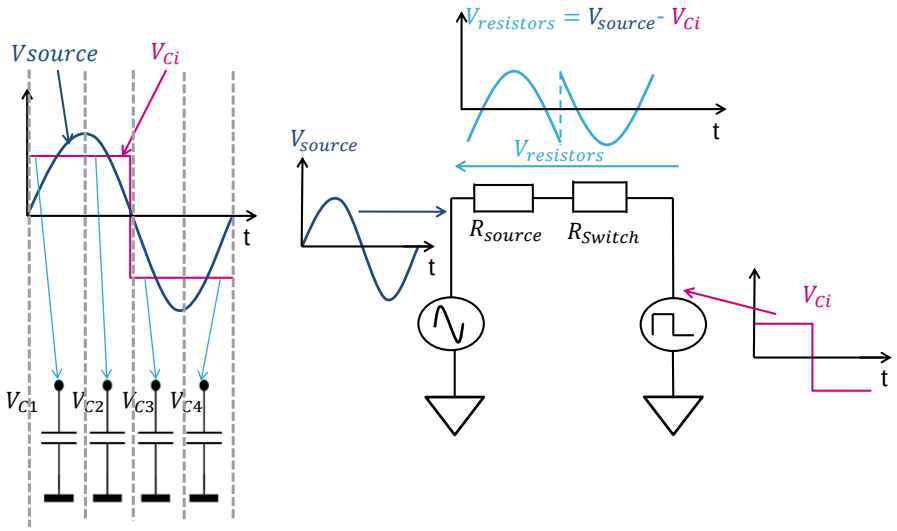

FIGURE A.1: LTV N-path input impedance

- $V_{C2} = \frac{2A}{\pi}\left(\cos(\frac{k\,\pi}{2} + \theta) - \cos(k\,\pi + \theta)\right)$
- $V_{C3} = \frac{2A}{\pi}\left(\cos(k\,\pi + \theta) - \cos(\frac{3\,k\,\pi}{2} + \theta)\right)$
- $V_{C4} = \frac{2A}{\pi}\left(\cos(\frac{3\,k\,\pi}{2} + \theta) - \cos(2\,k\,\pi + \theta)\right)$

The up-shown equation can be split to 4 different cases of V_{Ci}, depending in k value. k can take one of the following values :

- $k = 4\,l$
- $k = 4\,l + 1$
- $k = 4\,l + 2$
- $k = 4\,l + 3$

For each value of k the V_{Ci} values would be developed then its Fourier decomposition will be developed, which will be used to calculate $V_{\text{resistors}}$, then I_{source} and finally $Z_{\text{in,mem}}(k\,f_{\text{LO}})$

Input impedance for $k = 4l$

The V_{Ci} values are all equal to zero. therefore the switch is connected to ground and we only see R_{sw}. this result was expected since the LTV holds only when the capacitor is charged, giving it a "memory-effect".

$$\boxed{Z_{\text{in,mem}}(k\, f_{\text{LO}}) = R_{\text{sw}}} \tag{A.2}$$

Input impedance for $k = 4l + 1$

The expressions of V_{Ci} values in this case, are equal to :

- $V_{C1} = \dfrac{2A}{k\,\pi}\,(\cos\theta + \sin\theta)$
- $V_{C2} = \dfrac{2A}{k\,\pi}\,(\cos\theta - \sin\theta)$
- $V_{C3} = -\dfrac{2A}{k\,\pi}\,(\cos\theta + \sin\theta)$
- $V_{C4} = -\dfrac{2A}{k\,\pi}\,(\cos\theta - \sin\theta)$

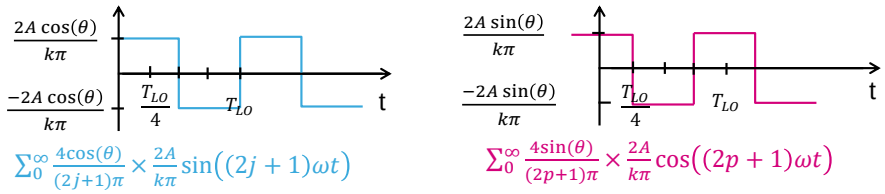

FIGURE A.2: two square signals that constitute the capacitors voltage for for $k\, f_{\text{LO}}$, where $k = 4l + 1$

The combination of those voltages V_{Ci} is therefore the sum of the two square signals illustrated in fig. A.2, along with their respective Fourier decomposition. V_{Ci} can thus be expressed as follows:

$$V_{Ci}(k\, f_{\text{LO}}) = \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4\,\cos\theta}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\text{LO}}\,t) + \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4\,\sin\theta}{(2\,j+1)\pi}\,\cos((2\,j+1)\,\omega_{\text{LO}}\,t)$$

$$V_{Ci}(k\, f_{\text{LO}}) = \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\text{LO}}t + \theta) \tag{A.3}$$

Then $V_{\text{resistors}}$ is equal to :

$$\begin{aligned} V_{\text{resistors}}(k\,f_{\text{LO}}) &= V_{\text{source}}(k\,f_{\text{LO}}) - V_{Ci}(k\,f_{\text{LO}}) \\ &= A\sin((k\,\omega_{\text{LO}}t+\theta) - \sum_{j=0}^{\infty}\frac{2\,A}{(k)\,\pi}\,\frac{4}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\text{LO}}t+\theta) \\ &= \left(A - \frac{8A}{k^2\,\pi^2}\right)\sin(k\,\omega_{\text{LO}}t+\theta) - \sum_{j\neq 2l}^{\infty}\frac{2\,A}{k\,\pi}\,\frac{4}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\text{LO}}t+\theta) \end{aligned} \tag{A.4}$$

Using A.4 in the source current expression :

$$I_{\text{source}}(k\,f_{\text{LO}}) = \frac{A}{R_{\text{source}}+R_{\text{sw}}}\left[\left(1-\frac{8}{k^2\,\pi^2}\right)\sin(k\,\omega_{\text{LO}}t+\theta) - \sum_{j\neq 2l}^{\infty}\frac{2}{k\,\pi}\,\frac{4}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\text{LO}}t+\theta)\right] \tag{A.5}$$

This current expression includes the current at the input signal frequency along with other currents at harmonics. In this first step, we are calculating the input impedance at one point ($f_{\text{in}} = f_{k\,\text{LO}}$). Then current contribution other than $I_{k\,\omega_{\text{LO}}}$ should not be considered:

$$\begin{aligned} I_{\text{source}}(k\,f_{\text{LO}}) &= \frac{A}{R_{\text{source}}+R_{\text{sw}}}\left(1-\frac{8}{k^2\,\pi^2}\right)\sin(k\,\omega_{\text{LO}}\,t) \\ R_{\text{source}} + Z_{\text{in,mem}}(f_{\text{LO}}) &= \frac{V_{\text{source}}}{I_{\text{source}}} = \frac{R_{\text{source}}+R_{\text{sw}}}{1-\frac{8}{k^2\,\pi^2}} \end{aligned} \tag{A.6}$$

Resulting finally in :

$$\boxed{Z_{\text{in,mem}}(k\,f_{\text{LO}}) = \frac{k^2\,\pi^2}{k^2\,\pi^2-8}\,(R_{\text{source}}+R_{\text{sw}}) - R_{\text{source}}} \tag{A.7}$$

Input impedance for $k = 4l + 2$

V_{Ci} values :

- $V_{C1} = \frac{4A}{k\,\pi}\cos(\theta)$
- $V_{C2} = -\frac{4A}{k\,\pi}\cos(\theta)$
- $V_{C3} = \frac{4A}{k\,\pi}\cos(\theta)$
- $V_{C4} = -\frac{4A}{k\,\pi}\cos(\theta)$

The Fourier decomposition of V_{Ci} is therefor :

$$V_{Ci}(k\,f_{\mathrm{LO}}) = \sum_{j=0}^{\infty} \frac{4\,A}{k\,\pi}\,\frac{4\,\cos\theta}{(2\,j+1)\pi}\,\sin\left((2\,j+1)\,\omega_{\mathrm{LO}}t\right)$$
$$= \sum_{j=0}^{\infty} \frac{4\,A}{k\,\pi}\,\frac{2}{(2\,j+1)\pi}\left[\sin\left((2\,j+1)\,\omega_{\mathrm{LO}}t+\theta\right)+\sin\left((2\,j+1)\,\omega_{\mathrm{LO}}t-\theta\right)\right] \tag{A.8}$$

Again, we consider only the current flowing in the switch resistance, resulting from the difference between the voltage held in the capacitor and the source voltage and not the current flowing in the capacitor. So we only focus on the real impedance, i.e. the impedance resulting from the current at the same frequency and phase of source voltage. Thus, in the $V_{\mathrm{resistors}}$ expression we only keep the tones at the same frequency and phase as the source voltage:

$$V_{\mathrm{resistors}}(k\,f_{\mathrm{LO}}) = V_{\mathrm{source}}(k\,f_{\mathrm{LO}}) - V_{Ci}(k\,f_{\mathrm{LO}})$$
$$= \left(A - \frac{16\,A}{k^2\,\pi^2}\right)\sin(k\,\omega_{\mathrm{LO}}t+\theta) \tag{A.9}$$

The current source is therefore :

$$I_{\mathrm{source}}(k\,f_{\mathrm{LO}}) = \frac{A}{R_{\mathrm{source}}+R_{\mathrm{sw}}}\left(1-\frac{16}{k^2\,\pi^2}\right)\sin(k\,\omega_{\mathrm{LO}}t+\theta)$$
$$R_{\mathrm{source}} + Z_{\mathrm{in,mem}}(k\,f_{\mathrm{LO}}) = \frac{V_{\mathrm{source}}}{I_{\mathrm{source}}} = \frac{R_{\mathrm{source}}+R_{\mathrm{sw}}}{1-\frac{16}{k^2\,\pi^2}} \tag{A.10}$$

Resulting finally in :

$$\boxed{Z_{\mathrm{in,mem}}(k\,f_{\mathrm{LO}}) = \frac{k^2\,\pi^2}{k^2\,\pi^2-16}\,(R_{\mathrm{source}}+R_{\mathrm{sw}}) - R_{\mathrm{source}}} \tag{A.11}$$

Input impedance for $k = 4l + 3$

- $V_{C1} = \frac{2A}{k\,\pi}\,(\cos\theta + \sin\theta)$
- $V_{C2} = \frac{2A}{k\,\pi}\,(\cos\theta - \sin\theta)$
- $V_{C3} = -\frac{2A}{k\,\pi}\,(\cos\theta + \sin\theta)$
- $V_{C4} = -\frac{2A}{k\,\pi}\,(\cos\theta - \sin\theta)$

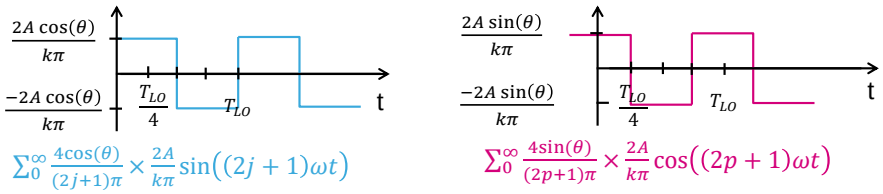

FIGURE A.3: two square signals that constitute the capacitors voltage for $k\ f_{\mathrm{LO}}$, where $k = 4l + 3$

As for $Z_{\mathrm{in,mem}}(f_{\mathrm{LO}})$ calculus in the case of a phase shift θ, V_{Ci} is the sum of the two square signal illustrated in fig. A.3, along with their respective Fourier decomposition. V_{Ci} can thus be expressed as follows:

$$V_{Ci}(k\ f_{\mathrm{LO}}) = \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4\,\cos\theta}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\mathrm{LO}}\,t) + \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4\,\sin\theta}{(2\,j+1)\pi}\,\cos((2\,j+1)\omega_{\mathrm{LO}}\,t)$$

$$V_{Ci}(k\ f_{\mathrm{LO}}) = \sum_{j=0}^{\infty} \frac{2\,A}{k\,\pi}\,\frac{4}{(2\,j+1)\pi}\,\sin((2\,j+1)\omega_{\mathrm{LO}}t + \theta) \tag{A.12}$$

As done previously, we consider only the impedance resulting from the current at the same frequency and phase of source voltage. Thus, in the $V_{\mathrm{resistors}}$ expression we only keep the tones at the same frequency and phase as the source voltage $V_{\mathrm{resistors}}(k\ f_{\mathrm{LO}})$:

$$\begin{aligned} V_{\mathrm{resistors}}(k\ f_{\mathrm{LO}}) &= V_{\mathrm{source}}(k\ f_{\mathrm{LO}}) - V_{Ci}(k\ f_{\mathrm{LO}}) \\ &= \left(A - \frac{8A}{k^2\,\pi^2}\right)\sin(k\,\omega_{\mathrm{LO}}t + \theta) \end{aligned} \tag{A.13}$$

The current source is therefore :

$$\begin{aligned} I_{\mathrm{source}}(k\ f_{\mathrm{LO}}) &= \frac{A}{R_{\mathrm{source}} + R_{\mathrm{sw}}}\left(1 - \frac{8}{k^2\,\pi^2}\right)\sin(k\,\omega_{\mathrm{LO}}t + \theta) \\ R_{\mathrm{source}} + Z_{\mathrm{in,mem}}(2f_{\mathrm{LO}}) &= \frac{V_{\mathrm{source}}}{I_{\mathrm{source}}} = \frac{R_{\mathrm{source}} + R_{\mathrm{sw}}}{1 - \frac{8}{k^2\pi^2}} \end{aligned} \tag{A.14}$$

Resulting finally in :

$$\boxed{Z_{\mathrm{in,mem}}(k\ f_{\mathrm{LO}}) = \frac{k^2\,\pi^2}{k^2\,\pi^2 - 8}\,(R_{\mathrm{source}} + R_{\mathrm{sw}}) - R_{\mathrm{source}}} \tag{A.15}$$

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