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# Monolithic Integration of Multiple Porous Silicon Membranes for Lab-on-a-chip Applications

Douglas Silva de Vasconcellos

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# THÈSE

En vue de l'obtention du  
**DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE**  
Délivré par l'Université Toulouse 3 - Paul Sabatier

---

Présentée et soutenue par  
**Douglas SILVA DE VASCONCELLOS**

Le 30 septembre 2020

**Intégration monolithique de multiples membranes de silicium  
poreux pour laboratoires sur puce**

---

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## Introduction

The leading cause of mortality worldwide is due to undiagnosed treatable diseases. The underlying reason is the cost and complexity of most diagnostic processes, as they are often carried out in medical centers and require expensive and complicated equipment that involve trained operators and frequent maintenance. To tackle this issue, the development of point-of-care technology using miniaturized and low-cost lab-on-a-chips is thus of great importance.

The analysis of a sample includes different steps that can be classified in two categories: sample preparation (i.e. sample separation, sample preconcentration) and sample analysis (i.e. biosensing). Different technologies have been successfully developed to carry these steps on chip, however, combining them in a single device introduces major obstacles because the integration strategy has to be compatible with the different technologies used to implement each step. Since there is no known simple and universal solution that can tackle all the obstacles presented in integrating all the sample analysis steps, they are usually integrated in a hybrid fashion, where the biosensor and the sample preparation module are realized separately and then combined, which increases the device complexity and possibly its final cost.

An obvious way of simplifying the integration is to develop a monolithic fabricated lab-on-a-chip device that provides the necessary and compatible technology for each stage of the sample analysis. The easiest way to implement this fully integrated lab-on-a-chip is to use a generic and single technological response for on chip sample preparation and sensing.

Porous silicon is a nanostructured material, suitable for monolithic microfabrication processes, that displays interesting properties such as photoluminescence due to quantum confinement, high thermal and electrical insulation, and biocompatibility. In addition to the obvious size-based filtering capabilities, its ion-selectivity property and the small pore size (under 100 nm) make porous silicon a strong candidate for sample concentration using ion concentration polarization. Past works have also demonstrated its capabilities to perform as an optical transducer, making it an interesting technology to be used for biosensing via reflectance-based interferometry when properly functionalized. With its capability of being used in different stages of sample analysis, a porous silicon-based lab-on-a-chip becomes an interesting candidate for point-of-care applications.

Classically, the porous silicon pores are formed following a vertical direction within the silicon substrate due to the mechanisms behind its fabrication by electrochemical anodization. For microfluidic operations, this causes limitations because of requiring the use of three-dimensional microfluidic designs to integrate porous silicon membranes into lab-on-a-chips. However, in previous works, our research team has developed



fabrication methods to create porous silicon membranes with lateral pores, enabling their integration into planar microfluidic systems.

In this work, we push this technology further by demonstrating the monolithic fabrication of planar microfluidic devices with various porous silicon elements (in the form of both lateral porous silicon membranes and classical vertical porous silicon layers) of different morphologies, paving the way toward the implementation of all sample analysis functions on a single chip. Because porous silicon is mainly fabricated through electrochemical anodization, the doping condition of silicon is one important factor that can be used to tune the morphology of the pores. Here, we study the use of selective ion implantation to manipulate locally the conductivity of different regions of the silicon wafer and reach variations in pores morphology. After presenting various technical approaches to reach this aim, we successfully developed a fabrication process that led to multiple membranes with different characteristics on a single chip. We then proposed chip designs that use these membranes to carry out sequentially sample preparation by ion concentration polarization and biosensing. Finally, we carried out simulation studies and preliminary experiments in order to validate the fabrication process and trace the direction we will have to go to turn this technology into a working lab-on-a-chip.

This manuscript is divided in three chapters. In chapter one, we present the motivations of this work, what should be taken into consideration when developing a lab-on-a-chip platform for bioanalysis, and we introduce the porous silicon technology. In the second chapter, we detail the development of the fabrication process for multiple membrane integration onto a single chip, including alternatives we have studied, obstacles we have faced and characterizations of fabricated chips. Lastly, in chapter three we apply the developed process to the fabrication of microfluidic devices to be used for both sample preparation and sample analysis; we also present optical simulation studies on thin film coatings and preliminary experimental results used to validate the device functionality, and we discuss perspectives for the full implementation of biosensing on the platform.

# Chapter 1. Lab-on-a-chip for point-of-care diagnosis: the interest of porous silicon

## 1. Microfluidic-based point-of-care diagnosis

Despite the medical advances we have witnessed during the last decades, death from treatable diseases/conditions is still one of the main mortality causes, for both developed and developing countries [1]. In the European Union countries alone, 422000 people aged less than 75 years died in 2016 due to treatable diseases/conditions, a mortality rate of 92.7 per 100000 inhabitants (figure 1 presents this information in more details regarding the considered countries), which is the equivalent of around 36% of the total death rate for avoidable mortality in EU Member States for this same age group [2].

Standardised deaths rates for avoidable mortality, persons aged less than 75 years, 2015 and 2016  
(per 100 000 inhabitants)

	Avoidable diseases/conditions		Treatable diseases/conditions		Preventable diseases/conditions	
	2015	2016	2015	2016	2015	2016
<b>EU-28</b>	<b>259.8</b>	<b>254.2</b>	<b>95.1</b>	<b>92.7</b>	<b>164.8</b>	<b>161.5</b>
Belgium	234.6	226.3	73.9	71.4	160.7	154.9
Bulgaria	442.2	426.4	197.4	194.3	244.8	232.1
Czechia	341.7	323.1	135.1	128.1	206.6	195.1
Denmark	241.9	236.6	77.7	75.9	164.2	160.7
Germany	249.1	244.4	89.3	86.8	159.8	157.6
Estonia	418.8	405.0	148.2	142.8	270.5	262.2
Ireland	220.6	218.2	83.8	80.1	136.9	138.1
Greece	241.8	236.3	96.6	94.9	145.2	141.4
Spain	187.7	184.6	68.3	66.8	119.4	117.8
France	199.5	195.8	62.9	62.5	136.6	133.4
Croatia	393.7	371.2	149.3	139.5	244.3	231.7
Italy	184.9	176.7	71.3	66.7	113.6	110.0
Cyprus	189.7	171.0	79.6	71.1	110.1	99.9
Latvia	547.9	534.9	206.9	203.1	341.0	331.7
Lithuania	556.4	541.6	212.9	205.6	343.5	336.0
Luxembourg	205.5	211.2	70.6	70.9	134.9	140.3
Hungary	518.2	501.2	183.9	176.0	334.3	325.3
Malta	200.8	202.5	86.6	87.4	114.2	115.2
Netherlands	205.9	202.8	70.7	68.9	135.3	133.9
Austria	245.8	238.8	79.0	77.7	166.8	161.1
Poland	352.5	348.2	131.2	129.8	221.4	218.5
Portugal	228.6	229.3	86.9	88.9	141.7	140.5
Romania	522.9	517.5	208.9	207.7	314.0	309.8
Slovenia	285.0	263.6	92.3	79.6	192.8	184.0
Slovakia	434.8	411.7	176.6	167.9	258.2	243.8
Finland	238.2	242.8	74.9	76.8	163.3	166.0
Sweden	193.3	188.9	70.9	67.6	122.4	121.2
United Kingdom	242.9	244.3	89.5	90.1	153.4	154.2
Iceland	192.9	201.7	66.8	62.4	126.1	139.4
Liechtenstein	165.8	178.9	75.3	59.8	90.6	119.1
Norway	192.6	191.8	64.3	62.9	128.2	129.0
Switzerland	172.4	163.8	55.7	52.6	116.6	111.2
Serbia	417.5	408.1	178.6	172.7	238.9	235.4
Turkey	325.7	328.3	139.2	141.1	186.5	187.2

Source: Eurostat (online data code: hlth\_cd\_apr)

euostat 

Figure 1 – Standardized deaths rates for avoidable mortality, including treatable diseases/conditions, in the European Union [2].

Ischemic heart diseases, respiratory infections, diabetes, and bacterial infections are among the diseases with a considerable high mortality rate that can be prevented if diagnosed in time. This statement is particularly true as, at the time of writing this thesis, the COVID-19 pandemic hit the world [3].

Being caused by a novel type of coronavirus, named SARS-CoV-2 [4], COVID-19 is an infectious disease that can cause critical lung complications, such as pneumonia and

even an equivalent to acute respiratory distress syndrome (ARDS) in more severe cases [5,6]. Although in most cases the symptoms are mild or non-existent (according to the World Health Organization [WHO] at the time of writing, 80% of people infected with SARS-CoV-2 recover from the disease without needing hospital treatment [7]), COVID-19 is dangerous mainly because of its high infectious rate (with preliminary estimation of its reproduction number between 2.2 and 3.5 [8,9] on average when no contingency policy is put in place) and its particular characteristic of being infectious during the virus incubation stage, before any symptoms are shown (because of a high level of SARS-CoV-2 shedding in the upper respiratory tract even in presymptomatic patients [10,11]), stage that lasts a median of 5 days [12]. This combination results in an urgent need of diagnostic tests to be able to identify infected patients and properly isolate them, in order to reduce the reproduction number and contain the virus.

These diagnostic processes are often carried out in medical centers and require expensive and complex equipment that involve trained operators and frequent maintenance. For the aforementioned case of COVID-19, for example, while the development of point-of-care (POC) tests have been of essential help, mainly for antibody testing, laboratory tests based on reverse transcription polymerase chain reaction (RT-PCR) are still the most reliable for viral testing [13]. Decreasing the costs and complexity with technological advances is crucial to improve the diagnostic efficiency in terms of analysis time and access to the largest number of people.

Since the last century, technology is on the trend of miniaturizing systems in different fields of application, ranging from communication tools to physical sensors. Being able to have a small device that works as a portable laboratory by monitoring different parameters, which can be used to diagnose different diseases, makes this trend very valuable for the medical field. Figure 2 compares miniaturized laboratories developed by research teams (when the platform is on its developing stage), to the so called point-of-care devices (available to end-users) and central laboratories, by illustrating the characteristics and trade-offs of each system.

Some types of POC devices have already been made widely available for the public in the last decades. For example, glucose meters can determine the glucose concentration in a few microliters of blood to notify the diabetic patient. Another extensively known example is the pregnancy test, which is a nanoparticle-based lateral flow biosensor device fabricated on paper substrates [14]. In general, POC devices are based on the analysis of a small volume fluid sample, making the use of microfluidic based lab-on-a-chip devices essential for their development.

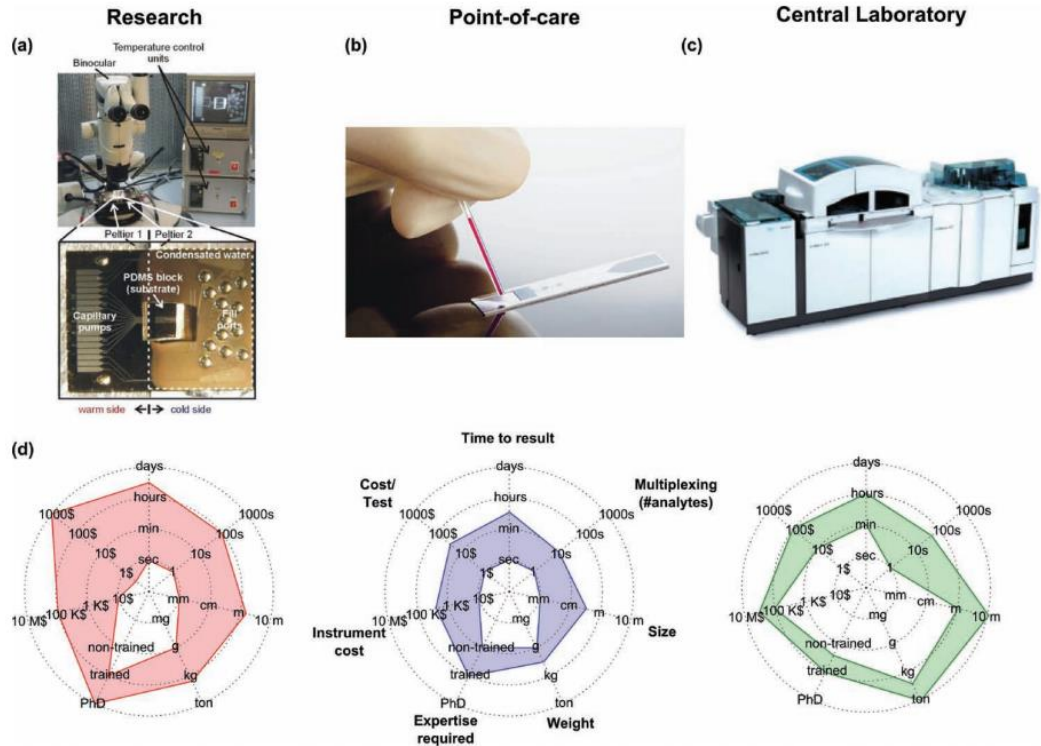


Figure 2 – Photos of (a) miniaturized diagnosis devices on their developing stage, (b) miniaturized diagnosis devices when they are ready for end-user manipulation, and (c) central diagnosis laboratory. (d) Radar charts comparing the characteristics and trade-offs of each system [15].

### 1.1. Microfluidics and lab-on-a-chip devices

Microfluidics is the field that studies the manipulation of micro to nanoliters of liquid samples, most frequently by means of microchannels of ten to hundreds of micrometers [16] (a schematic comparing the scale of micro and nanofluidics to different biological elements can be seen in figure 3). The main advantage of microfluidics is that by processing a small volume of complex fluids, it is possible to achieve high efficiency, speed and sensitivity, without the need for an expert operator, while keeping the costs low by reducing the consumption of reagents.

A further step for POC technology is to combine microfluidics with pre-analytical and analytical methods in the form of a lab-on-a-chip (LOC) [17,18]. LOC devices ought to be capable of performing the different sample handling steps and measurements (e.g. filtering, sample concentration, biochemical reactions, biosensing) while keeping their reduced size, cost and weight [19-22]. Most analytical measurements rely on the detection of a biomarker in the sample to analyze that provides information of the patient’s medical state [23].

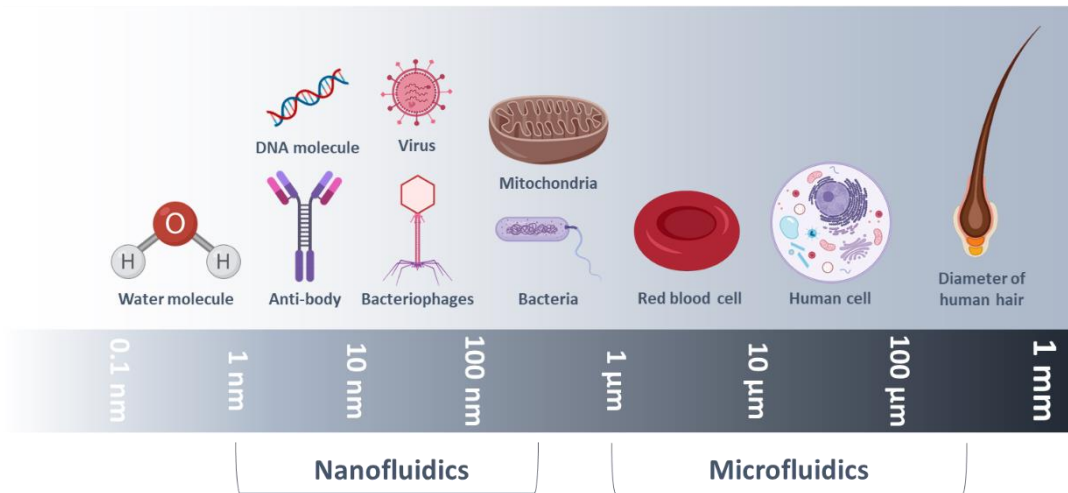


Figure 3 – Schematic presentation of a scale comparing micro and nanofluidics to different biological elements. Adapted from [24].

## 1.2. Biomarkers

According to WHO, a biomarker is any substance, structure, or process that can be measured in the body (or in its products), and influences or predicts the incidence of a clinical outcome or a disease [25].

In the recent years, an extensive number of scientific studies have identified numerous biomarkers, which have become the basis for the diagnosis and prognosis of different disorders, such as cancer, diabetes, AIDS, tuberculosis, cardiovascular diseases. In fact, thousands of biomarkers candidates have been identified, but only a few hundreds have been successfully implemented into clinical use [26,27].

An overview on different biomarkers, their use and where they are found can be seen in figure 4. A first example of biomarkers include proteins as cardiac troponin I (cTnI) which is the gold standard biomarker for acute myocardial infarction (AMI) [28], produced only in the myocardium and showing high specificity to cardiac injury [29]. Another example of class of biomarkers is oligonucleotides: for instance Zhang et al. [30] discovered and validated twelve messenger RNA salivary biomarkers by profiling transcriptome in saliva samples of pancreatic cancer patients. Those biomarkers present high sensitivity and specificity, as they can discriminate pancreatic cancer from other types of cancer and from chronic pancreatitis as well. Other types of cancer also have already established biomarkers, such as micro-RNAs miR-125a and miR-200a in saliva for oral cancer [31], and free circulating plasma DNA can be used to diagnose lung cancer in early stages [32].

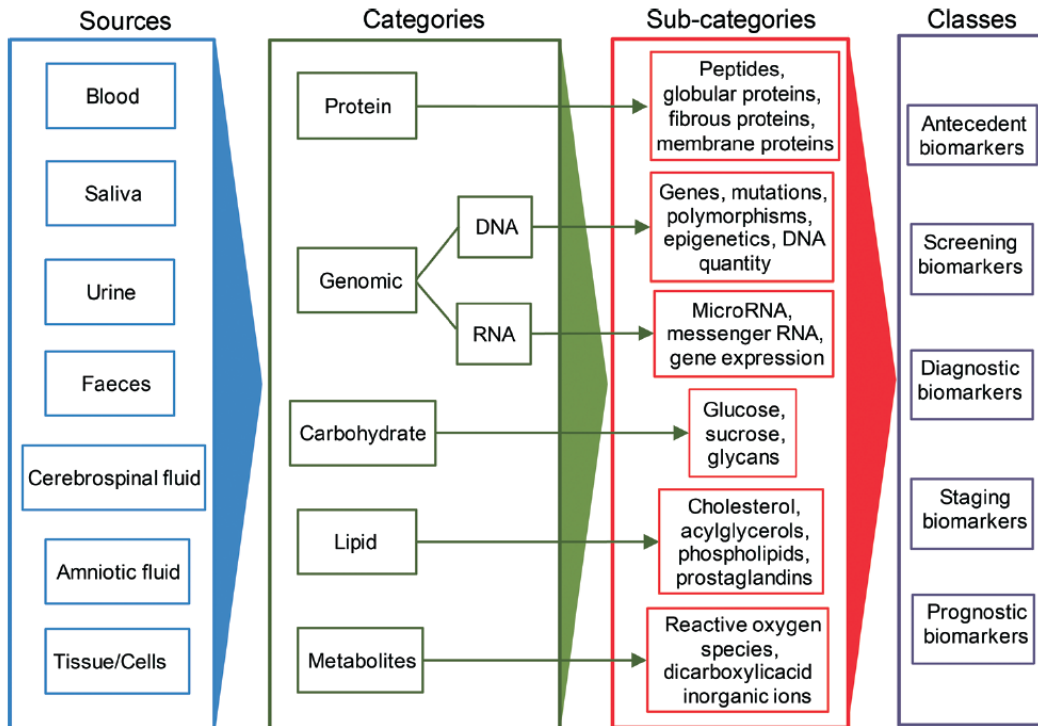


Figure 4 – Overview of biomarkers and where they are found [26].

Being of different natures, with distinct characteristics and sampled from various sources, the analysis of these biomarkers call for various analytical methods: not only from a detection point of view, but also the sample preparation protocol must obviously be adapted to the sample as well as the type of biomarker.

### 1.3. Sample preparation

A single drop of blood can contain numerous and distinct elements, among cells, molecules, antibodies. In fact, the amount of information in a single drop is such that Xu et al. [33] detected over 1000 strains of viruses and 206 species using a platform based on phage immunoprecipitation sequencing (PhIP-seq) technology called VirScan. Many of those elements can cause disruption of the fluid handling by fouling or blockage of the analytical system. Also, the target analyte can be available in trace amounts, making it difficult, or even impossible, to detect its signal over the background noise, depending on the sensitivity of the detector [34]. Those reasons make real-world sample not suitable for direct analysis, requiring the use of sample preparation techniques.

### 1.3.1. Sample separation

Sample preparation involves different steps. First, the sample has to be purified in order to remove components that can disrupt the analytical steps, e.g. blockage of the analytical system due to the size of elements found in the sample, reduced detection sensitivity because of non-specific interactions with the sensor. The most common techniques used in this step are centrifugation, size-based separation and charge-based separation.

As the name suggests, centrifugation uses the centrifugal force caused by a high velocity rotation to mechanically separate the components based on their density. Ultracentrifuges, which work at high velocities, are mostly used to separate macromolecules based on molecular weight, while vacuum centrifuges are used to evaporate solvents, while keeping the solution at the bottom of the vial [35,36]. The use of centrifugation on a blood sample is represented in figure 5.

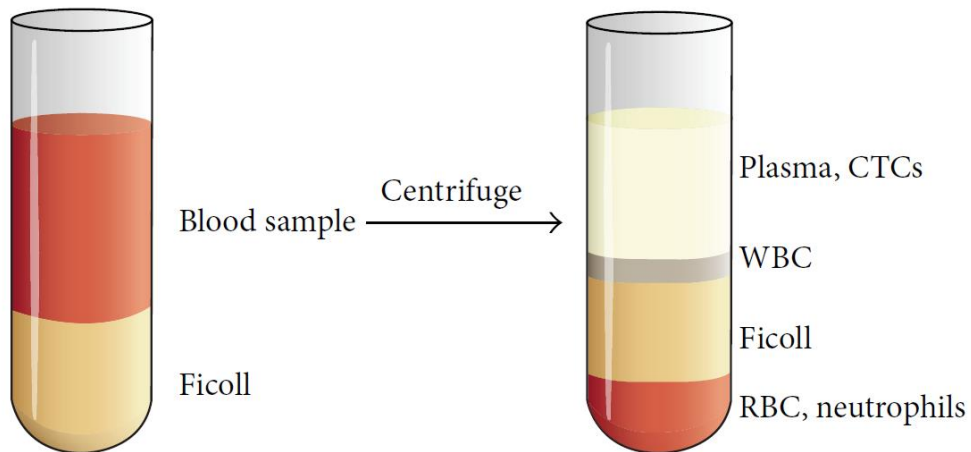


Figure 5 – Schematic representation of plasma separation of a blood sample by means of centrifugation. CTCs are circulating tumor cells, WBC are white blood cells and RBC the red blood cells [36].

When comparing to both size and charge-based separations, centrifugation has the disadvantage of requiring to be done before the sample is introduced to the LOC, while also demanding a larger quantity of sample.

Size-based separation relies on the use of porous membranes to remove undesirable components in a sample. Membranes exhibit pores that are big enough to let the target analyte pass while blocking bigger components [37], as seen in figure 6, where a filter for dialysis is represented, allowing urea and middle-molecular-weight toxins to pass, while retaining albumin.

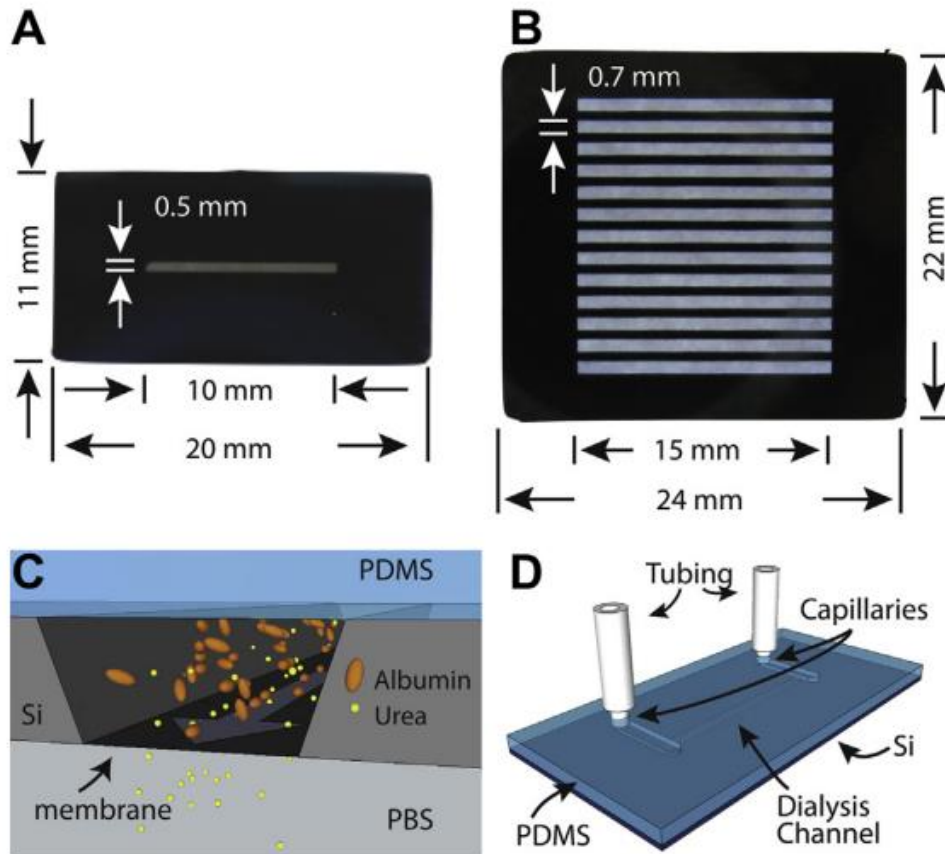


Figure 6 – Schematic representations of a porous silicon filter for microfluidic dialysis [38].

Two approaches can be taken for size-based separation techniques. Dead-end filtration (figure 7 left) works by flowing the fluidic sample perpendicularly to the filter element, passing the fluid through it while retaining undesirable bigger components, forming a cake layer on the filter's surface [39]. This first approach has the advantages of having a low cost and being simple to operate [40], while the cake formation causes decrease in permeability and flux, which makes the filter lifespan quite limited. Crossflow filtration (figure 7 right) uses the combination of the pressure in the perpendicular direction of the filter surface with a feed flow parallel to it, creating turbulent conditions capable of removing the cake layer while the sample is filtered. This approach is most used to filter samples with a higher concentration of filterable matter, although it requires a more complex operation [41].



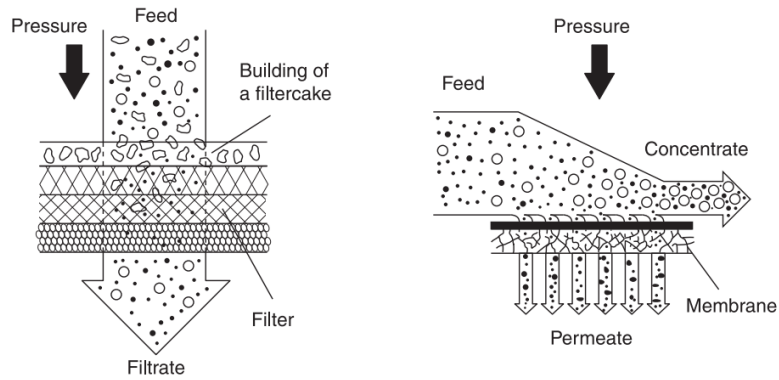


Figure 7 – Schematic representations of dead-end filtration (left) and crossflow filtration (right) [42].

Various materials can be used to make filtration membranes, from simpler ones such as filter paper and polymer-based membranes, to more complex ones such as silicon nanowires [43] and porous silicon [38,44].

Charge-based separation (or electrofiltration) combines the pressure already used in the previous described size-based separation with electrokinetic forces created by applying an electrical potential gradient across a perm-selective membrane. This mechanism involves an electrical double layer (EDL) formation at the filter surface due to the ability of the membrane to acquire a charge when immersed in an aqueous solution. The EDL has an associated mobile diffuse layer of opposite charge which, on experiencing an electrical potential gradient, moves through the pores [45]. This causes an extra force on charged particles, as they are brought closer together in the polarized layer. This flux augmentation can be significant for particles under 100 nm in size [39]. Figure 8 shows the use of charge-based separation for electrodialysis.

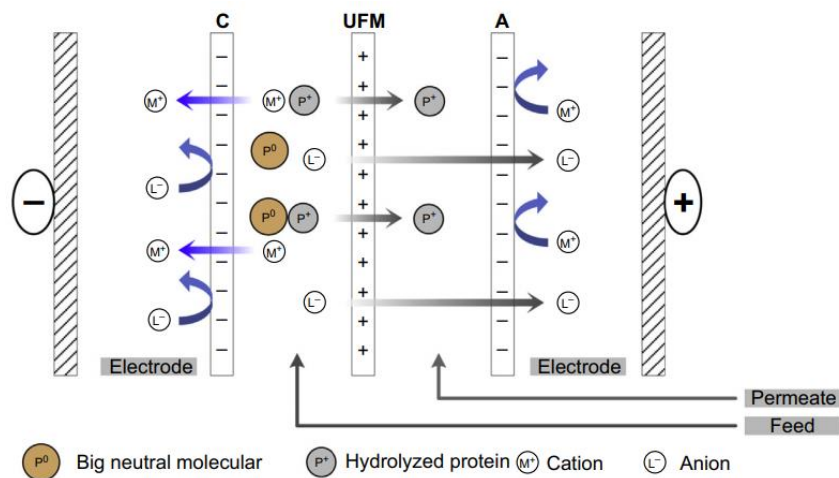


Figure 8 – Schematic representation of charge-based separation being used for electrodialysis. C and A represents the cathode and anode, respectively. UFM is the ultrafiltration membrane [46]

### 1.3.2. Sample preconcentration

Another task of sample preparation is to increase the concentration of targets to analyze, that is used to lower the apparent limit of detection and analysis time of the analytical device. There are various ways to tackle this step.

In addition to performing sample separation, membrane based techniques can improve target concentration by reducing the volume of analysis, either by size-based filtration [47,48], or by evaporation [49]. Non-electrical extraction techniques are also used as a way to increase the target concentration by separating it from the sample [50], including techniques such as solid-phase extraction [51,52], and liquid-liquid extraction [53].

Various techniques utilize capillary electrophoresis (CE) as the basis for target concentration [54]. Field-amplified sample stacking (FASS) is the most common of them. FASS works by injecting a low-conductivity sample solution into a capillary filled with a high-conductivity buffer solution, and by applying an electric field to the sample zone that provokes a target stack at the boundary due to the different electrophoretic migration of ionic analytes [55-57]. Field-amplified sample injection (FASI) is similar to FASS, but it uses the electrokinetically injection of ionic analytes from the inlet vial, filled with a sample solution, to the capillary, providing the introduction of a larger amount of analyte [58]. By coupling isotachopheresis (ITP) with CE, it is possible to simultaneously do both preconcentration and separation steps [59].

When selective charge transport is applied through an ion-selective nanojunction connecting two microfluidics compartments, an electrokinetic phenomenon named ion concentration polarization (ICP) occurs, resulting in an accumulation of charged species in one compartment (ion enrichment) and an ion depletion in the other. Similar effects can also be obtained via charge transfer reactions at an electrode (faradaic ICP, or FICP) [60], or by applying both concentration enrichment and separation of charged analytes with the technique called counter-flow focusing (ICP CFF) [61]. Schematics for the mentioned ICP techniques are seen in figure 9.

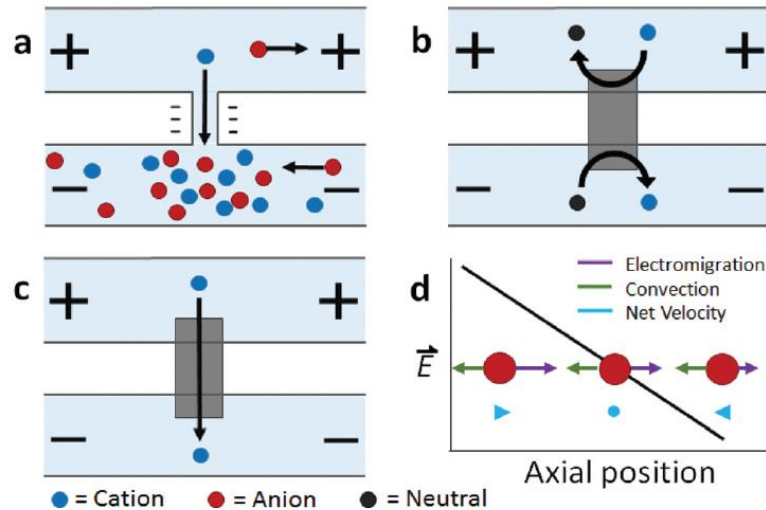


Figure 9 – Schematics for (a) ICP, (b) and (c) FICP, and (d) ICP CFF [61].

With its very high concentration factors, ICP has been attracting a lot of attention in the past years, and different configurations and applications of this approach have been discussed and presented. Yang et al. [62] performed ICP on paper-based microfluidic devices with a Nafion membrane. Pi et al. [63] introduced the fabrication of an ICP preconcentrator using a three-dimensional printed layer, easily integrating the ion exchange membrane within the microchannels. Fan et al. [64] used triboelectric nanogenerator (TENG) to trigger ICP for the preconcentration of antigens. Han et al. [65] demonstrated the utilization of a Nafion-reservoir-Nafion (NRN) paper-based structure as a high-ionic-concentration ICP preconcentrator for blood-based samples.

#### 1.4. Biosensing

With the sample properly treated, the analysis stage is conducted in order to detect and identify the target biomarker. First introduced by Clark and Lyons in the 1960s [66], biosensors are integrated bioreceptor-transducer devices able to provide analytical information using a biological recognition element (bioreceptor). While the transducer can be considered the main component of the sensor, which is mostly made from inorganic materials, its surface needs to be chemically modified, also known as functionalized, in order to bind the bioreceptor that is able to properly capture the target. To put it briefly, biosensors combine a bioreceptor with a suitable signal transduction method (figure 10), translating the interaction between the target and the recognition element into a physical signal [67-69].

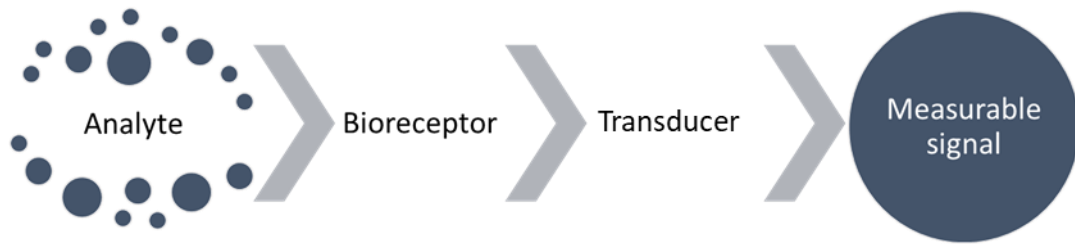


Figure 10 – Schematic representation of how a biosensor works. Adapted from [70].

Biosensors can be characterized by eight parameters [71]. (i) Sensitivity measures the response of the sensor according to the unit change in analyte concentration. (ii) Selectivity is their ability to respond only to the target analyte, not being influenced by other undesired elements found in the sample. (iii) Range defines the concentration range in which the sensitivity of the sensor is enough to detect the target. (iv) Response time is the time required for the sensor to reach 63% of its final response due to a step change in analyte concentration. (v) Reproducibility is the accuracy of the sensor's output. (vi) Detection limit is the lowest concentration of the analyte which the sensor is capable of detecting. (vii) Lifetime represents how long the sensor can be used without losing significant performance. (viii) Stability characterizes the changes in their baseline or sensitivity over a fixed period of time.

All those parameters need to be considered when developing a miniaturized biosensor, that consists in selecting the bioreceptor, the immobilization method, the device design, and integrating the biosensor into an instrument.

#### 1.4.1. Surface modification

The immobilization of the bioreceptor on the transducer's surface can be tackled in different ways: physical adsorption, entrapment in a polymer or within a membrane-sealed bag, and covalent attachment, the latter being the most popular method used for biosensors. Covalent attachment offers notable advantages, i.e. high reproducibility and stability, possibility to control the density and environment of immobilized species, generation of uniform structures, and a high number of receptors on a transducer surface [69].

One of the main obstacles in the functionalization of transducers integrated into lab-on-a-chips is the unwanted adsorption of the target molecules throughout the device, causing drastic decreases in sensitivity and selectivity of the sensor [72,73]. The strategies taken to address this obstacle, i.e. to provide localized and selective functionalization of the sole sensing element, have to be compatible with the materials in question, the sample, and the fabrication process of the device. Examples of different strategies can be seen with the use of specific chemical

reactions that only affect the transducer material [72], the use of inkjet printing techniques [74], photo-induced chemical synthesis [75], and also the local deposition of droplets or the use of liquid meniscus for molecular transfer [76-78].

#### **1.4.2. Biosensors classification**

Miniaturized biosensors can be classified either according to the type of bioreceptor, or to the category of the transducer. Four different groups of bioreceptors can be used for the classification: nucleic acid/DNA, enzymes, antibody-antigen and cells. In the case of the transducer, the biosensors can be classified as optical, thermal, piezoelectric, and electrochemical [79]. While electrochemical biosensors still dominate the biosensing field [80], optical biosensors (plasmonic) have attracted a lot of attention because of various advantages compared to other technologies, such as delivering label-free quantitative analysis and showing exceptional potential for multiplexing and miniaturization [81].

Transducers are built from various technologies and made with different materials. For example, optical biosensors have been made using technologies such as glass optical fibers [82], porous silicon [83] and silicon cascaded-microring resonators [84]. Other technologies lead to more categories of transducers, such as HCR-based (hybridization chain reaction) electrochemical transducers [85], heat-transfer method (HTM) for thermal-based sensors [86], and quartz crystal microbalance (QCM) devices being used as piezoelectric transducers [87].

#### **1.5. Lab-on-a-chip integration**

The sample preparation protocol and process need to be adapted to the transducing schemes and technologies used for the analytical step. This one imposes tight specifications, more or less restrictive, in terms of sample format and composition. For example, the amplification of DNA by PCR requires the presence of numerous biomolecules in solution (such as primers and DNA polymerases), and direct electrical detection on silicon nanowires can only be carried out in low ionic strength buffers that offer a fairly long Debye length. Ideally, most of the sample preparation steps should be done as close to the analysis step as possible, and long processes that require large sample volume are not adapted (e.g. non-electrical extraction for sample preconcentration), as they are not easily miniaturized. In addition, moving nano or picoliter samples around in a branched microfluidic device, a system in which solutions of different compositions have to be localized to different areas, is not always trivial [34].

As there is no known simple and universal solution that can tackle all the obstacles presented in integrating all the sample analysis steps, they are usually integrated in a hybrid fashion, where the biosensor and the sample preparation module are

realized separately and then combined, which increases the device complexity and possibly its final cost. An obvious way of simplifying the integration is to develop a monolithic fabricated LOC device that provides the necessary and compatible technology for each stage of the sample analysis. The easiest way to implement this fully integrated LOC is to use a generic and single technological response for on chip sample preparation and sensing: the best example of this all-in-one approach is the platform developed by Fernando Patolsky's team, which uses a dense forest of silicon nanowires as input chip for filtration, molecular separation and pre-concentration, as well as nanowire transistors downstream for the detection of protein biomarkers directly in a blood sample [88].

Porous silicon is a nanostructured material, suitable for monolithic microfabrication processes, and that displays interesting properties such as photoluminescence due to quantum confinement, high thermal and electrical insulation, and biocompatibility. In addition to the obvious size-based filtering capabilities [38,44], its ion-selectivity property [89] and the small pore size (under 100 nm) make porous silicon a strong candidate for sample concentration using ICP. Past works have also demonstrated its capabilities to perform as an optical transducer, making it an interesting technology to be used for biosensing via reflectance-based interferometry when properly functionalized [83,90]. Thus, the porous silicon technology possibly offers solutions for all analytical steps and could probably serve as a single-technological brick for a LOC integrating the full sample analysis procedure.

In the second section of this chapter, we are going to introduce porous silicon's properties and characteristics, to better understand its potential as a technology for a complete lab-on-a-chip analysis.

## **2. Porous silicon for microfluidics**

Accidentally discovered in the 1950s by Arthur Uhlir Jr. and Ingeborg Uhlir, at the Bell Labs in the United States, porous silicon is a semi-conductor material formed by a crystalline silicon skeleton and a network of voids. The finding happened when the Uhlirs were developing a technique to polish silicon wafers through an electrochemical method in hydrofluoric acid (HF) medium [91,92]. They noted that while using relatively low current densities during this process, instead of polishing the material, a thin layer of a crude material was being formed. In the 1970s and 1980s, groups of researchers around the globe started studying the formed film, finding out that silicon was riddled with an array of small holes. In this same period, the scientific interest on the material had a significant increase because its high surface area made porous silicon a relevant material for spectroscopic studies, and as a dielectric layer in capacitance-based chemical sensors.

In the early 1990s, Leigh Canham, working at the Defense Research Agency in England, realized the material could display quantum confinement effects, and, in consequence, revealed that silicon wafers can emit light when subjected to electrochemical and chemical dissolution, as it would report bright red-orange photoluminescence [93]. This event marked the transition of porous silicon into an important material in optoelectronics.

The first applications of porous silicon in microfluidics started emerging late in that same decade, when Steiner et al. [94] proposed using porous silicon as a sacrificial layer for the fabrication of suspended structures due to its high selectivity in potassium hydroxide (KOH) etching when compared to crystalline silicon, and, then, in the following year, Bell et al. [95] used this strategy for fabricating free-standing structures suspended above microfluidic channels (figure 11) [96].

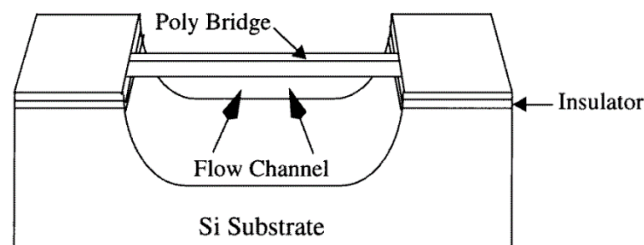


Figure 11 – An example of a suspended polysilicon bridge fabricated over a microchannel that was formed using a sacrificial porous silicon layer [95].

## 2.1. Porous silicon properties

Over the following years, different properties of the material were studied, creating paths for many others microfluidic applications. In the following subsections, I will present those properties and their role in microfluidics applications.

### 2.1.1. Pore size and porosity

The two main properties of the porous silicon describe the morphology of the material. Pore size is the approximate diameter of the voids contained in the silicon skeleton. According to the International Union of Pure and Applied Chemistry (IUPAC) [97], the pores can be classified in three categories according to their diameter:

- Micropores: for pore size under 2 nm (figure 12a);
- Mesopores: for pore size between 2 and 50 nm (figure 12b);
- Macropores: for pore size above 50 nm, going to over a few micrometers (figure 12c).

The term nanopores has also been widely used, including all pores from up to 100 nm in size [98].

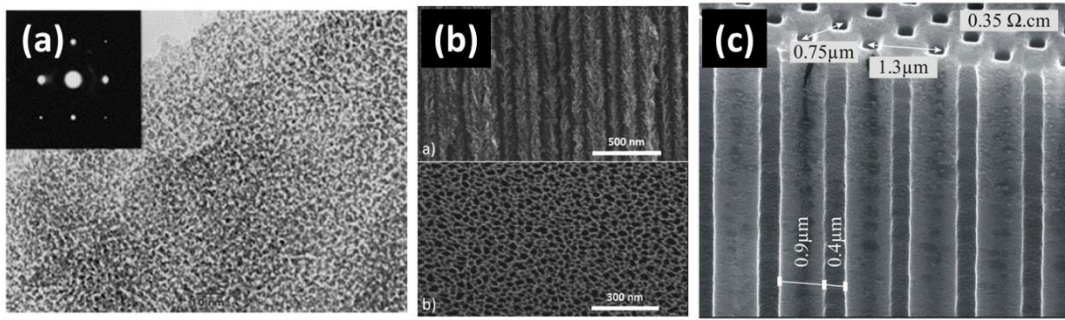


Figure 12 – Examples of the different classifications of porous silicon based on the pore size. (a) Micropores fabricated by anodization of p-type silicon in 50% aqueous HF solution [99]; (b) Mesopores for the electrochemical synthesis of mesoporous Si/Fe nanocomposites [100]; (c) Macropores formed by electrochemical etching of n-type silicon and nanoimprint lithography [101].

Tunable pore size makes porous silicon an interesting material to work with different biological entities (figure 13).

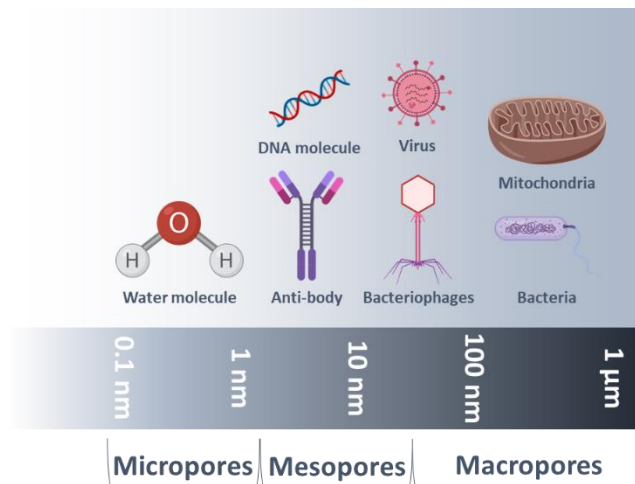


Figure 13 – Scale comparing the size of different biological entities with the pore size classification. Adapted from [17].

Porosity is defined as the ratio of the volume occupied by the void over the total apparent volume of the material. It is another tunable property, and it can vary from less than 1% to 97% [102]. With the increase in porosity, the surface area of the material also increases, leading to more chemical reaction sites for surface chemistry.

Combining tunable pore size with high porosities makes porous silicon very interesting material for different microfluidic applications. Size-based sample filtration is the obvious one, as the pore size can be used or to accommodate or block different types of elements, which has been extensively demonstrated in the literature [38,44,103-105]. The high surface area and porosity have also an impact in the sensing capabilities of the porous silicon, as they allow more active species to



be chemically attached to the surface [106]. High porosity makes porous silicon a good technology to be used for drug delivery as well, as it permits a high drug payload [107-109] and promotes solubility in biological media [110]. Finally, the large surface/volume ratios of porous silicon have made the material very promising for the realization of efficient electroosmotic pumps [111]. These pumps allow high flow rates with no moving parts, and have been fabricated from microporous silicon (represented in figure 14) [112] and ultrathin nanocrystalline silicon membranes [113].

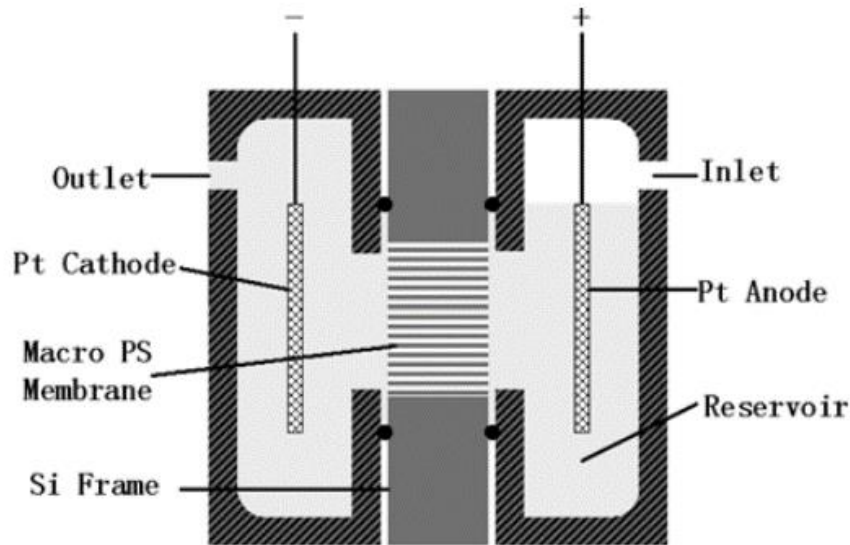


Figure 14 – Schematics of an assembled porous silicon-based electroosmotic pump [112].

### 2.1.2. Surface chemistry

Porous silicon reactivity is dominated by two strong reducing functions: silicon-hydrogen (Si-H) and silicon-silicon (Si-Si) bonds. For this reason, the material is not stable in aqueous solution. While this property can be useful for microfluidics applications such as *in vivo* drug delivery or imaging material, as they rely on the degradation of the material into biocompatible constituents [109,114,115], it can be a critical limitation in its use for other microfluidics applications [92]. In the case of optical biosensors, for example, the aqueous oxidation and subsequent dissolution of mesoporous silicon leads to zero-point drift, reducing the ultimate sensitivity [116]. The most common method to solve the lack of stability is the thermal oxidation of the porous silicon, as stabilized silicon-oxygen (Si-O) bonds improve the aqueous stability, while also enhancing the electrical insulation and the electrical double layer thickness. Several oxidants can be used for the thermal oxidation of silicon, but the simplest one is air. Depending on the temperature during the atmospheric oxidation, different species can be produced because the Si-Si bond is weaker than the Si-H bond. To completely convert the porous silicon

surface into silicon dioxide ( $\text{SiO}_2$ ), temperatures over  $200^\circ\text{C}$  is required, as seen below in figure 15.

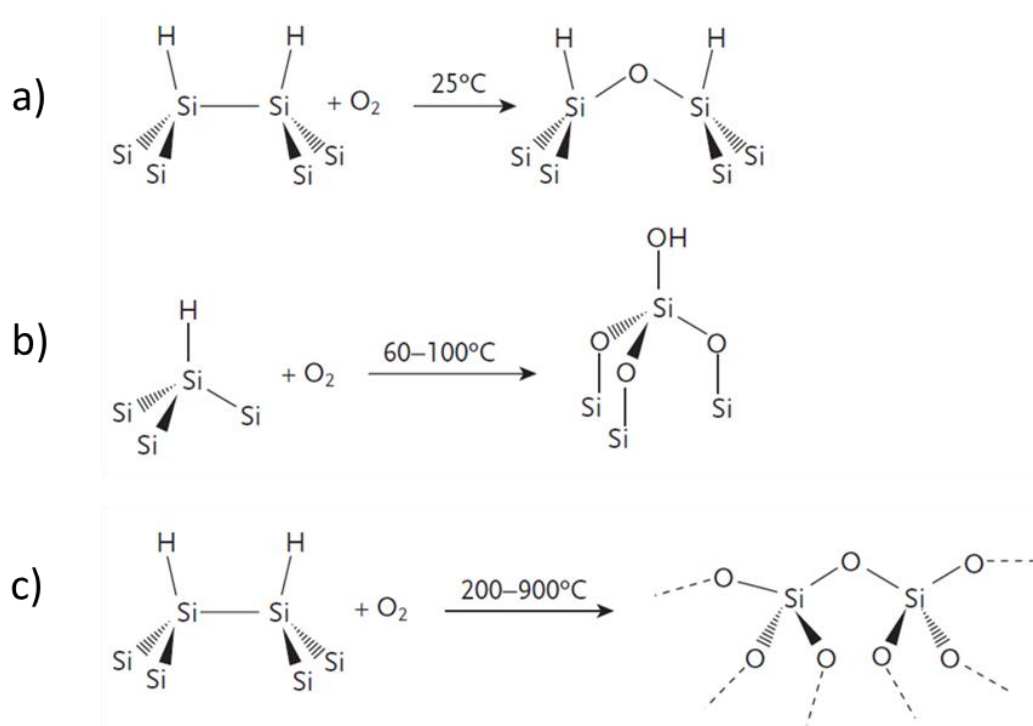


Figure 15 – Mechanisms of the thermal oxidation of silicon for different temperature ranges. (a) At  $25^\circ\text{C}$ , (b) between  $60-100^\circ\text{C}$ , and (c) between  $200-900^\circ\text{C}$ . Adapted from [92].

Oxidized porous silicon can be further modified by the same chemical protocols used to modify both silica and glass surfaces, because they present similar surface chemistry. In the case of biosensing, where the coupling of biological entities is interesting, one of the most popular reactions is the salinization with 3-aminopropyltriethoxysilane (APTES), resulting in reactive  $-\text{NH}_2$  groups on the porous silicon surface (figure 16) [117]:

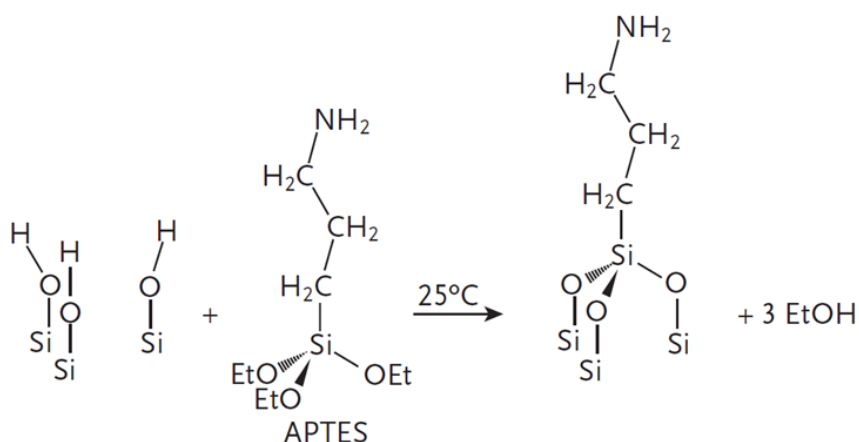


Figure 16 – Mechanism of the functionalization of oxidized porous silicon through the salinization with APTES. Adapted from [92].

For the modification of the interior of micropores, the use of n-propyldimethylethoxysilane (APDMES) (figure 17) is more effective, because the lack of additional Si-O bonds on the molecule eliminates the possibility of undesirable cross-linking reactions between other silanols. These cross-linking reactions can produce large oligomers that clog micropores, limiting the effective surface coverage [92]:

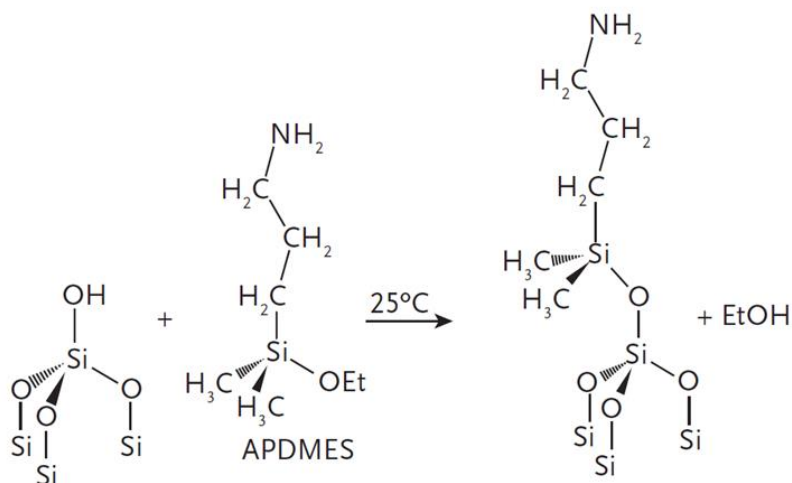


Figure 17 – Mechanism of the functionalization of oxidized porous silicon through the use of APDMES. Adapted from [92].

De Stefano et al. [117] measured the surface wettability, an important indication of the surface chemical composition, of oxidized porous silicon samples in three different configurations: just after oxidation (figure 18a), functionalized with APTES (figure 18b) and functionalized with APDMES (figure 18c).

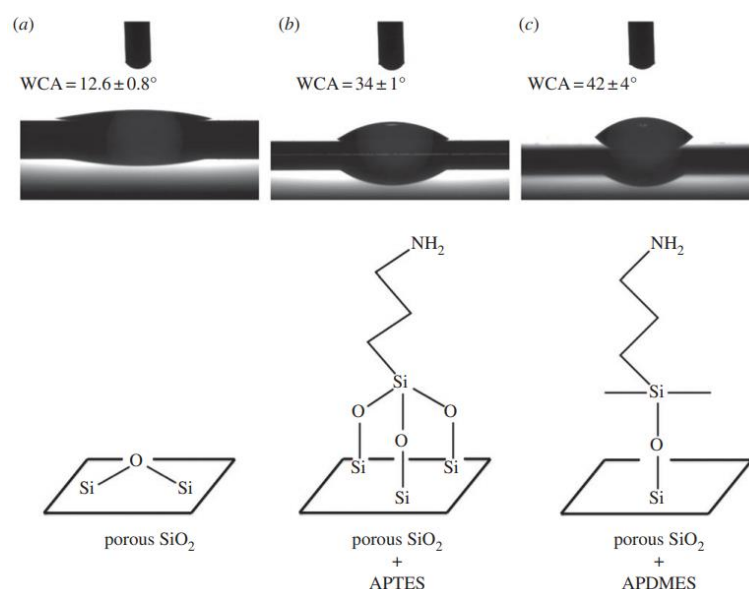


Figure 18 – Wettability study of porous silicon in three configurations: (a) oxidized porous silicon; (b) functionalized with APTES; (c) functionalized with APDMES [117].

Other less popular approaches use the reductive power of porous silicon to spontaneously reduce many metal salts to their element forms, forming porous silicon/metal composites that improve the luminescent property [118], magnetic property [119] and catalytic activity of porous silicon [120].

Thermal hydrosilylation is another interesting approach, as it forms silicon-carbon (Si-C) bonds [92], as seen in figure 19.

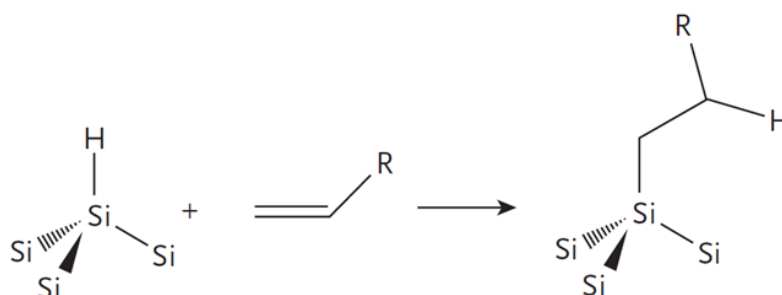


Figure 19 – Mechanism of thermal hydrosilylation of porous silicon. Adapted from [92].

Thermal hydrosilylation allows the placement of a wide variety of organic functional groups on a porous silicon surface, which includes carboxylic acid and ester groups that permits further chemical modifications [121]. For *in vivo* applications, such as drug delivery and imaging, hydrosilylation may not be an option because the Si-C chemistries on the porous silicon surface is too stable, making the material not dissolvable [92].

### 2.1.3. Biocompatibility and biodegradability

Biocompatibility is the ability of a material to perform with an appropriate host response in a specific situation [122]. The material can be considered biocompatible if inert, i.e. it does not induce any host immune response and have little or no toxic properties, or if bioactive, which means it initiates a controlled physiological response from the host [123]. Porous silicon has demonstrated bioactive properties in different examples in the literature. Canham [124] observed that hydroxyapatite (HA) crystals grow on microporous silicon films, having implications for bone tissue implants and bone tissue engineering, and that by applying cathodic current it is possible to further promote calcification on the surface [125]. Moxon et al. [126] used porous silicon to promote neuron viability when inserted into rat brains, making the material work as a potential neuronal biosensor.

Biodegradability is the capacity of a material to go through biological degradation, by the interactions with biological elements, down to the base substances such as water, carbon dioxide, methane, basic elements and biomass [127]. As previously mentioned, as-fabricated porous silicon is unstable in aqueous solutions due to oxidative hydrolysis [92], degrading into orthosilicic acid (Si(OH)<sub>4</sub>) [128], a nontoxic

acid that is the common form of bioavailable silicon in the human body [129]. The biodegradability of porous silicon is influenced by its porosity, as porous silicon with medium porosity (around 60%) shows slow degradation, while higher porosity porous silicon (over 80%) shows exponential release of silicic acid over time [130]. Surface modification can also be used to control the biodegradability. Depending on the modification, porous silicon degradation rates can be tuned anywhere from minutes to months [131], making porous silicon a strong material for both *in vitro* and *in vivo* applications.

#### **2.1.4. Optical and luminescence properties**

Porous silicon has shown several interesting optical properties over the years, with applications in different fields, ranging from micro- and optoelectronics to biosensing and biomedicine [132-134]. With pores size in the nanometer range well below the wavelengths of infrared and visible light, porous silicon can be considered as a homogeneous effective material, whose optical properties depend on its porosity, surface chemistry and pore-filling medium [135].

Being able to tune the porosity and pores size of porous silicon layers makes their optical properties, such as effective refractive index, also tunable for the needs of the applications. This change in refractive index can be detected by reflectance-based transducers, indicating which medium is filling the pores [135].

A common method of measuring the optical properties is by illuminating the sample with white light perpendicular to its surface, causing a reflection of the incident light at the top and at the bottom of the porous silicon layer, which result in an interference spectrum that is detected by a spectrometer. This interference spectrum is directly related to the refractive index of the sample through the effective optical thickness (EOT) [136]. This method has been broadly applied for the detection of enzyme activity [137], proteins [90,138], immunoglobulins [139], DNA [83,140] and bacteria [141].

Likewise, it is possible to fabricate porous silicon structures with predefined in-depth porosity profiles, having them work as dielectric multilayer stacks that show optical interference effects between layers of different porosity. With this approach, a wide variety of interference optical filters, such as double layer, Bragg mirror and micro-cavity, and rugate filters can be achieved with porous silicon layers (represented in figure 20) [92,135].

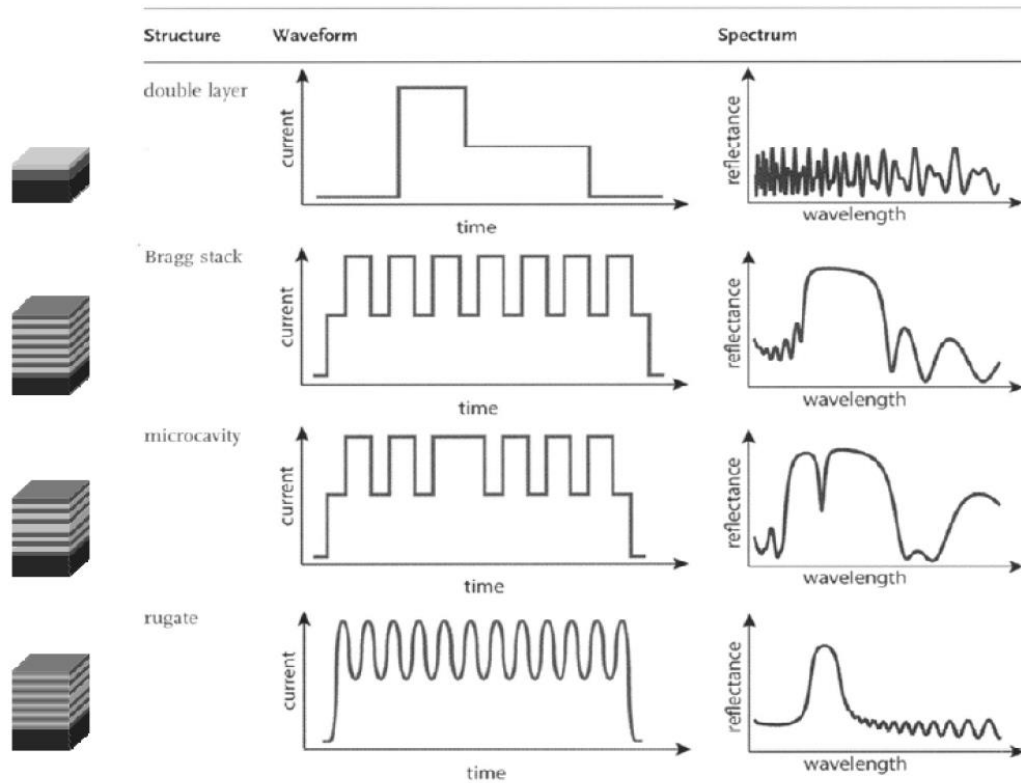


Figure 20 – Different porous silicon-based interference optical structures, with the waveforms of their current density used during fabrication and corresponding interference spectra [92].

Several methods have been proposed to model the optical properties of porous silicon (represented in figure 21), i.e. the Maxwell-Garnett model, the Bruggeman model, the Looyenga-Landau-Lifshitz model, and Bergman’s representation.

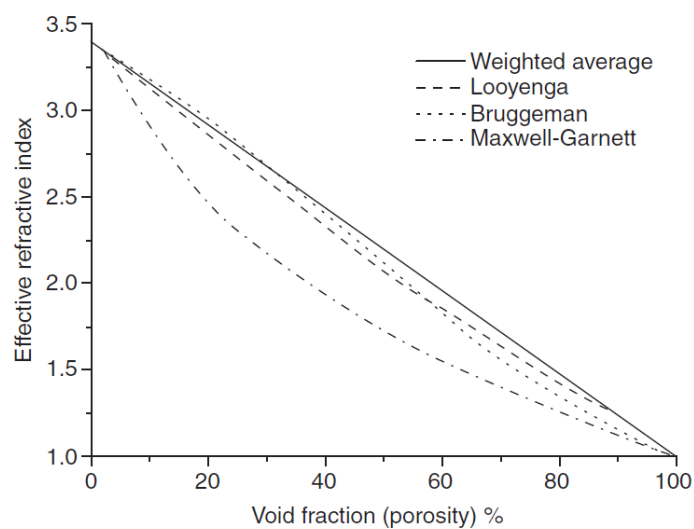


Figure 21 – Effective refractive index as a function of porosity using different effective medium models [135].

The Bruggeman model is the most frequently used model for medium porosities (between 33 and 66%) and it can be extended to effective medium formed of multiple components. For instance, Petrik et al. [142] have successfully modeled porous silicon as a material formed by three components: crystalline silicon, nanocrystalline silicon and air.

As mentioned earlier, porous silicon made its first big impact when it was discovered to have photoluminescence properties due to quantum confinement effects [93]. Over the following years of this discovery, it was learned that, depending on the degree of quantum confinement and on the chemical state of its surface, porous silicon could luminesce from the near infra-red (around 1.5  $\mu\text{m}$ ) to the near-ultraviolet, as a result of distinct emission bands having different origins [143,144].

The photoluminescence properties are being used for biosensing, by analyzing the changes in photoluminescence spectrum of the porous silicon caused by the presence of an analyte [145].

#### **2.1.5. Electrical properties**

The conductance and capacitance of a porous silicon layer depend on its morphology (i.e. pore size and porosity), set by the fabrication process (i.e. current density, reaction time, electrolyte's concentration), and also on the medium filling the pores [146-148]. Those properties have led to the development of conductance-based gas sensors [148,149] and capacitance-based vapor sensors [150,151].

Porous silicon has also demonstrated to have ion-selectivity properties [89]. Recently, this property has been taken advantage of for the use of porous silicon as a multi-ion selective electrode-based extended gate field transistor for the sensing of several cations [152]. Having ion-selectivity properties also makes porous silicon a strong candidate for doing sample concentration using ICP, which is an electrokinetic phenomenon based on the selective charge transport through an ion-selective nanojunction connecting two microfluidics compartments [61].

#### **2.2. Porous silicon membranes**

Throughout this chapter, several applications involving porous silicon and microfluidics have been presented. Some of those applications, i.e. electroosmotic pumps and size-based filtration, require the use of thin porous silicon membranes of some micrometers in thickness (figure 22).

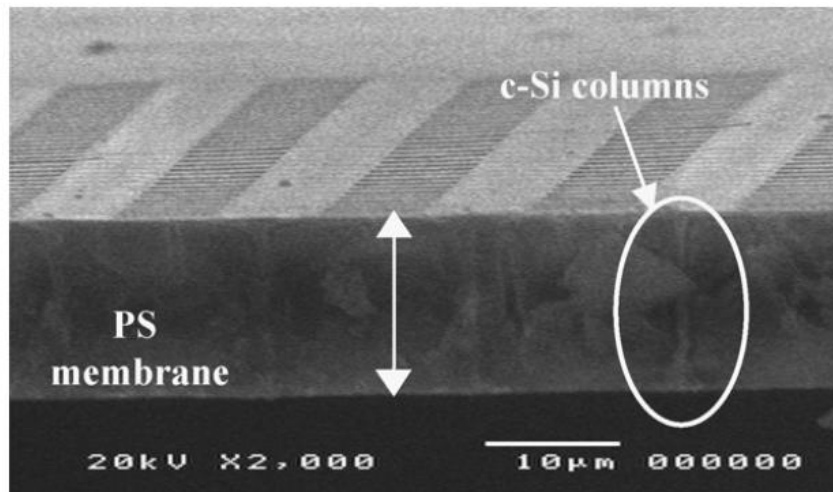


Figure 22 – Porous silicon membrane used for size-based filtration [103].

Besides the aforementioned electrochemical process, porous silicon can be fabricated by several other means [153], which we will describe in the next chapter. Whatever the fabrication technique, porous silicon elements are most commonly fabricated in a similar configuration of pore propagation direction, with the pores being formed in the direction perpendicular to the silicon wafer surface. In this configuration, flow-through membranes are usually obtained by backside etching the silicon wafer. The integration into microfluidic devices is then solved by sandwiching the membrane between two encapsulating layers that bear the microfluidic channels (figure 23a), requiring the use of three-dimensional (3D) microfluidic systems. Such systems have several disadvantages over planar (2D) devices:

- i) 3D microfluidic devices lack design flexibility and simplicity when it comes to fluidic operations, while 2D systems allow the possibility of easily integrate different designs with different functions and access for pressure and electrical control;
- ii) With the need of sandwiching the porous silicon layer, the integration adds the possibility of fluid leaks;
- iii) 3D devices make it difficult to do direct microscope observation, as the microchannels are not in the same observable plane.

### 2.2.1. Lateral porous silicon membranes

Our research team has recently proposed a novel approach for fabricating porous silicon membranes with the pores being formed in the direction parallel to the wafer surface (figure 23b) [154], called lateral porous silicon membranes, fully demonstrated in the PhD work of Yingning He [155]. With this approach, we are



able to monolithically integrate porous silicon membranes (with pores varying from ~5 to ~30 nm in size, and from ~15 to ~65% in porosity) into planar microfluidic devices (figure 24).

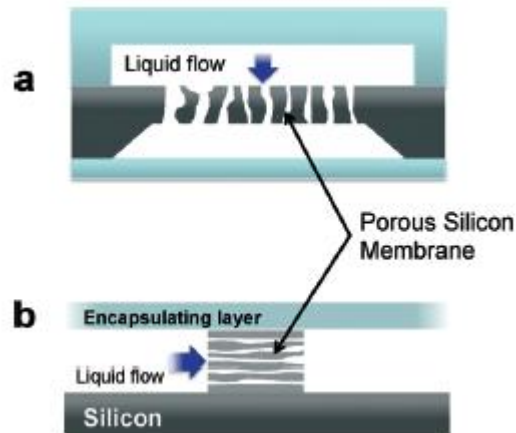


Figure 23 – Schematics of the integration of porous silicon membranes into microfluidic devices using (a) the classical vertical porous silicon approach, and (b) the novel lateral porous silicon approach [154].

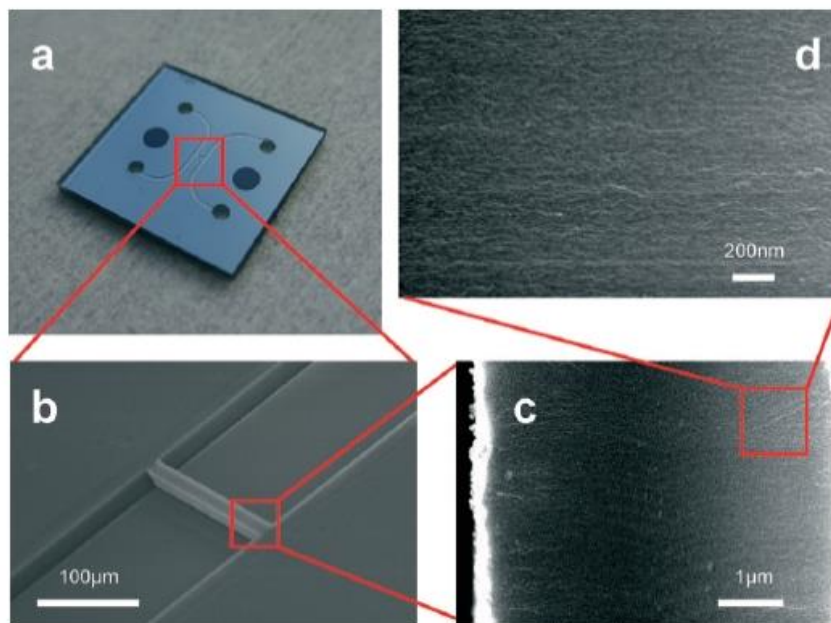


Figure 24 – Microscopic images of a 10 µm thick lateral porous silicon membrane integrated in between two microfluidic channels [154].

### 2.2.2. Use of lateral porous silicon membranes for bioanalysis applications

In past works, our research team has demonstrated the potential of lateral porous silicon membranes to carry out various tasks for bioanalysis. Size-based filtration was demonstrated with lateral porous silicon membranes [154-156] by forming a membrane in between two microchannels and applying pressure to flow solutions

with various-size objects: fluorescein (around 2 nm diameter), miRNA (around 10 nm diameter) and beads (around 300 nm diameter). For both fluorescein and miRNA, the molecules were able to flow back and forth through the porous silicon membrane (with mesopores of around 15 nm in diameter), while the beads were blocked, showing the filtering capabilities of the membrane (figure 25).

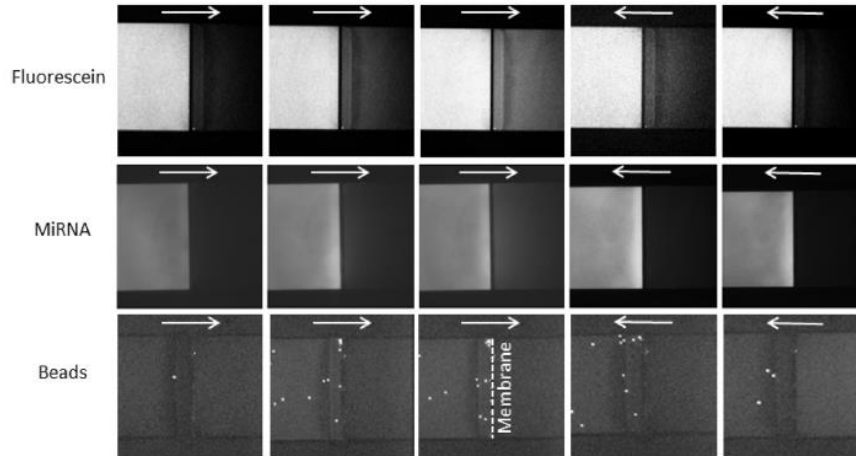


Figure 25 – Filtering experiments demonstrating the capabilities of the lateral porous silicon membrane [156].

By applying a voltage difference across the lateral porous silicon membrane, we were also able to show its capabilities for sample preconcentration through ICP. With 7V / 2V applied in the same microchannel, while the channel across the membrane was grounded, preconcentration factors of 100 for 100 nM of fluorescein in PBS 0.1x within 90s were achieved (the sequential recorded images of the process are seen in figure 26) [155]. However, a detected current leakage indicated that by amending the insulation of the membranes we should be able to improve its performance.

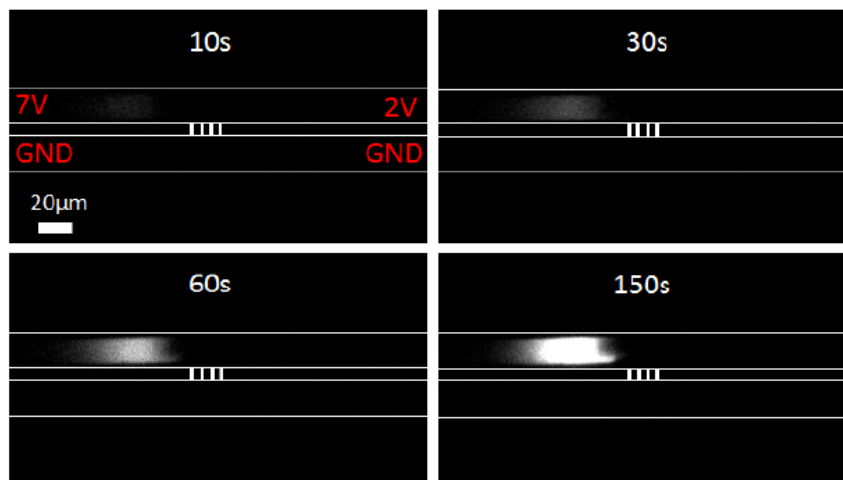


Figure 26 – Sequential images of fluorescein preconcentration by ICP using lateral porous silicon [155].

Finally, lateral porous silicon membranes were demonstrated to have transducing ability using optical interferometry, being a potential tool for optical biosensing. Because the refractive index of the membrane depends of the filling medium and it has a relation with the effective optical thickness of the reflected light (as described in section 2.1.4.), it was possible to identify the presence of three different solvents filling the pores (water, ethanol and acetone) through the red shift of the reflectance spectra caused by their presence when compared to empty and dry porous silicon (figure 27) [155,157]. However, to proper carry out biosensing we need to implement functionalization of the membranes in order to capture the targeted biomarkers (as explained in subsection 1.4.1.).

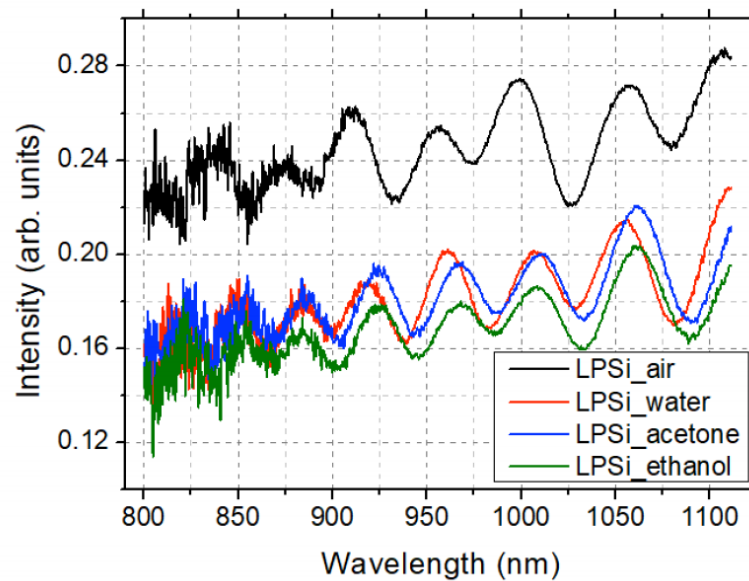


Figure 27 – Experimental reflectance spectra of the three tested solvents (water, acetone and ethanol) filling the lateral porous silicon membrane. The curved named air represents an empty and dry porous silicon [157].

By being suitable for monolithic integration into a planar microfluidic device, and capable of realizing the different stages required for sample analysis (namely filtering and sample concentration for sample preparation and possible biosensing), lateral porous silicon has the necessary attributes to enable the integration of these various analysis steps in a single microchip.

### 3. Challenges and motivations of this work: integration of multiple porous silicon elements of varying morphologies into a lab-on-a-chip

In the last section we presented preliminary studies that demonstrate lateral porous silicon membranes can be used for sample preparation steps (i.e. sample filtration and preconcentration), and has the potential to be used for biosensing if adequately biofunctionalized in order to capture specific biomarkers. Combining various porous silicon elements in a single chip monolithically, we could hope to create an

integrated LOC to be used for the complete sample analysis necessary for a point-of-care diagnosis tool. Accordingly, the goal of this work is to develop a fabrication process capable of monolithic fabricating a lab-on-a-chip device based on multiple porous silicon elements that would be capable of combining steps of sample preparation and biosensing (figure 28).

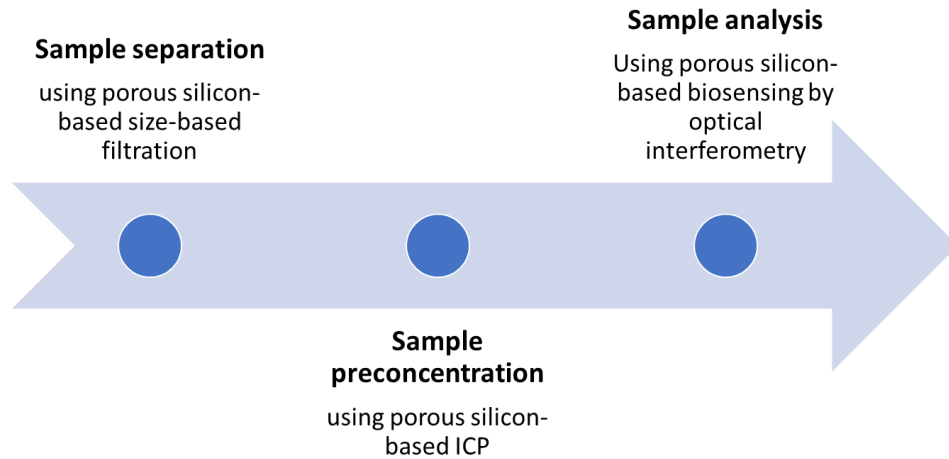


Figure 28 – Schematic diagram of the analysis process to be taken in the porous silicon-based LOC.

There are some obstacles that ought to be tackled for the development of such a LOC device. Due to the fabrication process previously developed for lateral porous silicon (which will be detailed in the chapter 2), we are limited in anodization time during the formation of porous silicon. This limits the pore size we are able to achieve to a range from 5 to 30 nm with the current anodization recipes. As mentioned beforehand, ICP performance has room for improvement by amending the membrane's electrical insulation, which can be tackled by thermal oxidation of the pores. Due to the limited size of our pores, both the thermal oxidation and the surface functionalization, required to carry out biosensing, are very difficult to be done without blocking the pores. As the various porous silicon elements are to be used for different tasks, we are also interested in having lateral porous silicon membranes of different morphologies, which could not be achievable with the current fabrication methods.

To put it briefly, the fabrication process developed in this thesis will have to succeed on the following challenges:

- i) Increase achievable pore size in lateral porous silicon membranes;
- ii) Form multiple porous silicon elements with different morphologies to monolithically integrate different functions.

After accomplishing those fabrication goals, we will also try and develop a selective surface modification process, which suits the materials and processes used for the encapsulation of our chips, to be selectively applied to the porous silicon element being used as an optical transducer.

#### **4. Conclusion**

In this chapter, we introduced the importance of developing point-of-care diagnosis devices built on microfluidic-based sample analysis. After presenting the different functions involved in the analysis of a biological sample (purification, preconcentration, biosensing) and briefly introducing examples of techniques and technologies that have been used to implement these tasks on chip, we have discussed the opportunity of using porous silicon membranes as a single technological brick capable of addressing these multiple functions for potentially reducing the complexity of their on-chip integration.

However, the integration of the classical porous silicon membranes in microfluidic devices is not trivial, because they require the use of 3D microfluidic systems, adding complexity and disadvantages over the 2D systems, and creating points of possible leakage. To tackle this, we proposed the use of lateral porous silicon membranes, which display pores along a direction parallel to the silicon wafer's surface, allowing their monolithic integration in 2D microfluidics systems.

We have presented lateral porous silicon membranes and their potential use for sample filtration, pre-concentration and biosensing, but this technology is still on its infancy and presents fabrication limitations. The goal of this thesis is to tackle said limitations, improving the performance of the technology, and to develop a porous silicon-based lab-on-a-chip able of performing the different functions involved in the bioanalysis process.

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## Chapter 2. Fabrication of multiple lateral porous silicon membranes onto a single chip

### 1. Porous silicon fabrication and characterization

After being accidentally produced through the electrochemical etching of silicon in the 1950s [1], over forty different ways to fabricate porous silicon of various forms and characteristics have been developed [2]. These techniques can be classified in two different categories: top-down and bottom-up approaches [3].

Top-down approach consists of forming the pores from solid silicon substrates. The most popular fabrication techniques, such as anodization and metal-assisted chemical etching, take this route.

Bottom-up methods are based on the use of silicon atoms and silicon-based molecules to build the porous geometry. Among the bottom-up techniques, deposition-based fabrication (fabrication of porous silicon by controlling silicon deposition [4]) and chemical conversion (based on the chemical reduction of silicon-based molecules to silicon [5]) are the most popular.

Choosing the fabrication route depends mostly on the requirements set by the application. The top-down methods are ideal for low-volume, high-value products, because they allow easier integration within chip-based products, but they can be too expensive for high volumes applications. For lower value, high-volume products, bottom-up techniques are more appropriate [2].

In our case, we aim at developing a lab-on-a-chip biosensor in the form of a microfluidic chip into which we want to integrate various porous silicon elements, therefore the top-down route is a clear choice. Among these techniques, three of them are interesting to discuss, due to their advanced development stage and their use in the fabrication of thin porous silicon membranes. Electrochemical anodization is the most popular technique, forming pores within bulk silicon through electrochemical etching, which consists of the silicon electrochemical oxidation followed by its etching by fluoric acid (HF) [6]. Metal-assisted chemical etching (MACE) follows a similar process, but it replaces the electrochemical reaction with the use of chemical oxidants to cause the oxidation, accompanied by noble metals used to increase the silicon's dissolution rate upon etching [7]. Finally, micromachining uses advanced machining techniques (i.e. dry etching) to form high aspect-ratio tubes in silicon [8].

Besides being the most popular, therefore the most developed technique, electrochemical anodization offers the additional advantage of controlling the direction the pores formed within the bulk silicon, since this direction follows the

current lines. This reason is the main motivation for its use in our project since it enables the fabrication of porous silicon elements with lateral pores, i.e. pores running parallel to the substrate's surface.

### 1.1. Electrochemical anodization

As mentioned previously, the mechanism behind the pores formation during the electrochemical anodization is divided in two general steps. First, the injected current (holes) causes the local electrochemical oxidation of silicon. The formed silicon oxide is instantaneously etched away due to the presence of HF in the electrolytic solution [6]. Figure 1 and figure 2 introduce the mechanism of pore formation.

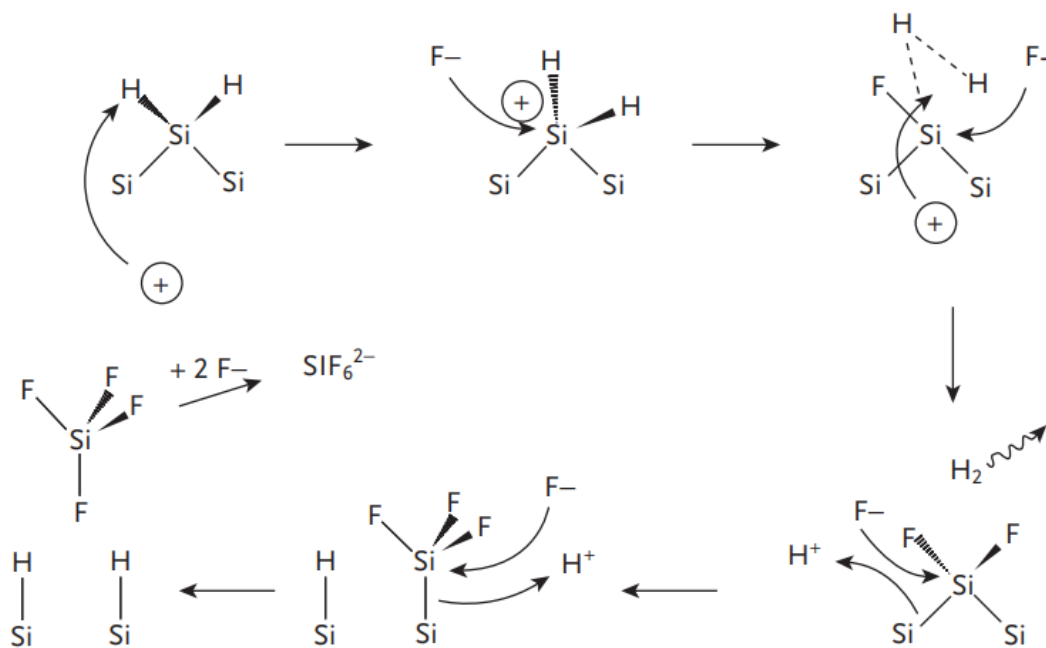


Figure 1 – Chemical reactions involved in porous silicon formation by electrochemical etching of silicon in fluoride-containing solution [6].

Anodization is done in a simple electrochemical etch cell. This cell is commonly formed by a silicon electrode (working electrode), where the porous silicon formation happens, and a platinum electrode (counter electrode).

As seen in figure 3, electrochemical reactions at the working electrode lead to pore formation by the anodic dissolution of silicon in fluoride-containing solution after the electrochemical oxidation of silicon. At the counter electrode, we observe the production of hydrogen gas.

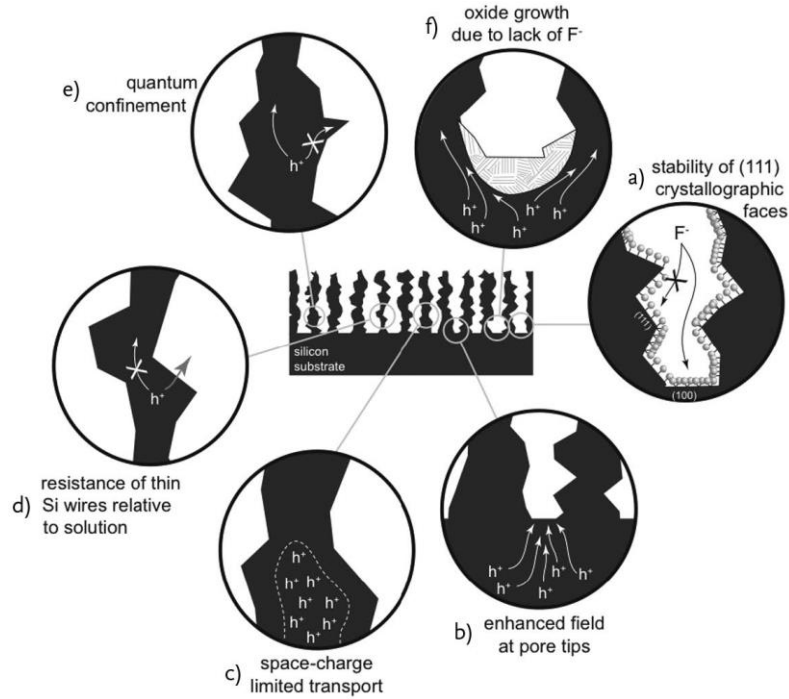


Figure 2 – Schematic representation of the various mechanisms involved in the electrochemical fabrication of porous silicon [6].

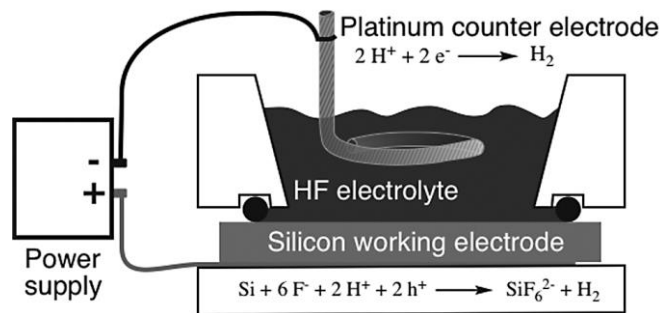


Figure 3 – Schematic representation of a classical electrochemical etch cell for the formation of porous silicon [6].

Pores are classically formed perpendicular to the wafer surface, because equipotential planes tend to be parallel to the surface, yielding a path of least resistance for valence band holes in the perpendicular direction [6].

Several parameters control the pores' morphology during the electrochemical anodization: doping type and level of the silicon wafer, crystallographic orientation of the substrate, current density, HF concentration and solvent utilized in the electrolyte.

### 1.1.1. Influence of doping type and level

Dopants are elements added to a semiconductor material to modify its conductivity. The element used as a dopant has one extra or one fewer valence electron than the semiconductor. In the case of silicon, phosphorous and boron are the most popular

dopants. Lying to the right column of silicon on the periodic table, phosphorous has one more valence electron than silicon. When phosphorus replaces a silicon atom in the crystal lattice (substitutional defect), the extra electron is donated to the conduction band, increasing the conductivity of the semiconductor (n-type doping). In the same way, sitting on the left column from silicon on the periodic table, boron increases the conductivity of the semiconductor by donating a hole to the valence band (p-type doping).

When a semi-conductor material is immersed in an electrolyte, the charge equilibration between the two phases leads to a barrier that either blocks or allows current to flow, depending on the direction of the current. In figure 4, which shows energy band diagrams, this barrier is represented by the bending of the conduction and valence bands in the vicinity of the interface. Since it is energetically favorable for the holes to move upwards along the band lines due to their positive charge, an upward bending represents a barrier for the holes, while a downward bend allows current to flow [6].

For the case of the use of p-type silicon, a downward bending is formed in the junction (figure 4b), favoring the hole current. In contrast, the bending formed on the n-type silicon creates a barrier (figure 4a), blocking hole current at the junction. On top of that, n-type silicon also lacks holes, as most of its carriers are electrons. To generate enough holes to cause the oxidation, light is used in a process called photoetching. Light generates electron-holes pairs near the semiconductor interface, and the built-in field sweeps the holes to the surface [6].

The doping level, which denotes the concentration of dopants on the substrate, have been found to have direct impact in the electrochemical etch rate of silicon. Eijkel et al. [9] demonstrate this impact in figure 5 below for applied voltage in the order of 10V.

In the matter of the formation of porous silicon, the etching speed has a direct influence on the morphology of the porous layer (pore size, porosity and thickness). Lehmann et al. [10] performed a study on how the morphology of the pores vary with different doping levels in the fabrication of mesopores with both p-type and n-type silicon. They observed that the density of pores would increase with the increase in doping level for both types of dopants (figure 6). Meanwhile, the pore size would increase for p-type silicon (figure 6a) and decrease for n-type silicon (figure 6b).

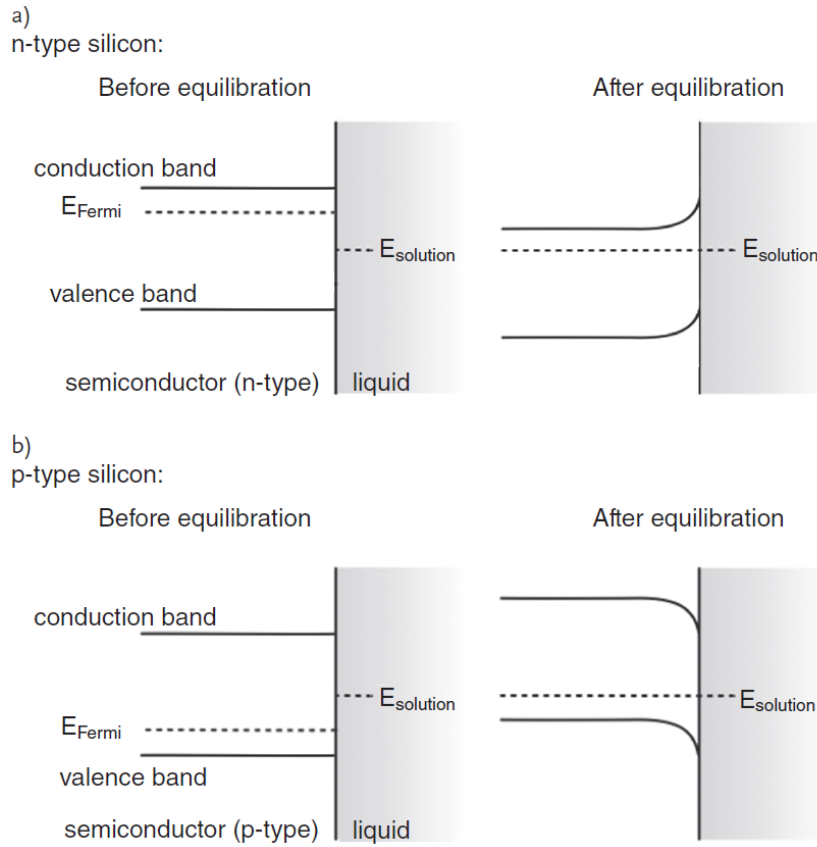


Figure 4 – Energy band diagrams of the equilibration between a solution and (a) n-type silicon and (b) p-type silicon [6].

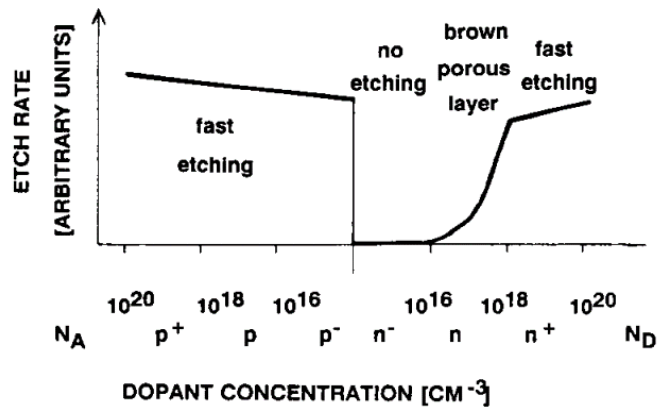


Figure 5 – Relation between etch rate of silicon during electrochemical etching and the doping level of the substrate for applied voltage in the order of 10V [9].



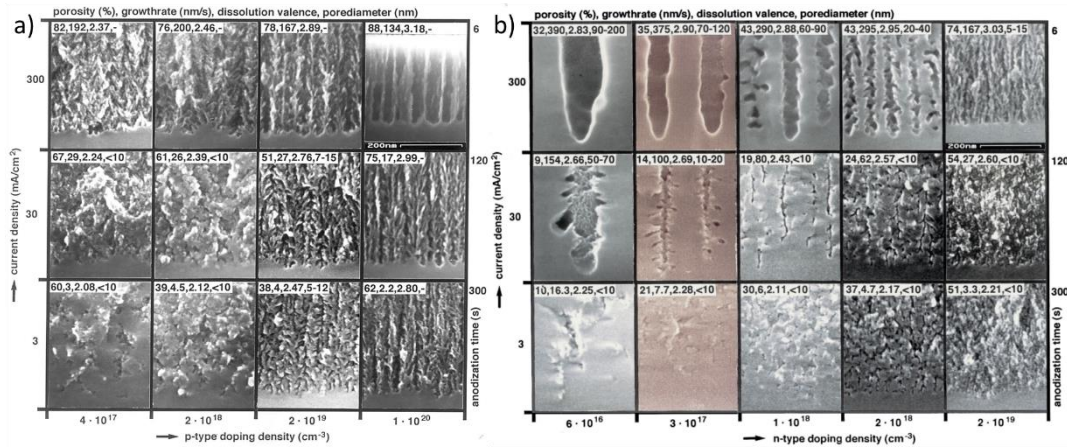


Figure 6 – Different morphologies of porous silicon fabricated with varying current density and doping levels for (a) p-type and (b) n-type silicon. Adapted from [10].

### 1.1.2. Influence of the crystallographic orientation

Silicon is an anisotropic material, and one of its characteristics is the different etching rates for the different crystallographic directions [11]. This is particularly well documented for KOH and TMAH etching of silicon, where the known (100)/(111) selectivity (figure 7a) can lead to proper etching masks in order to achieve the desired pattern (figure 7b).

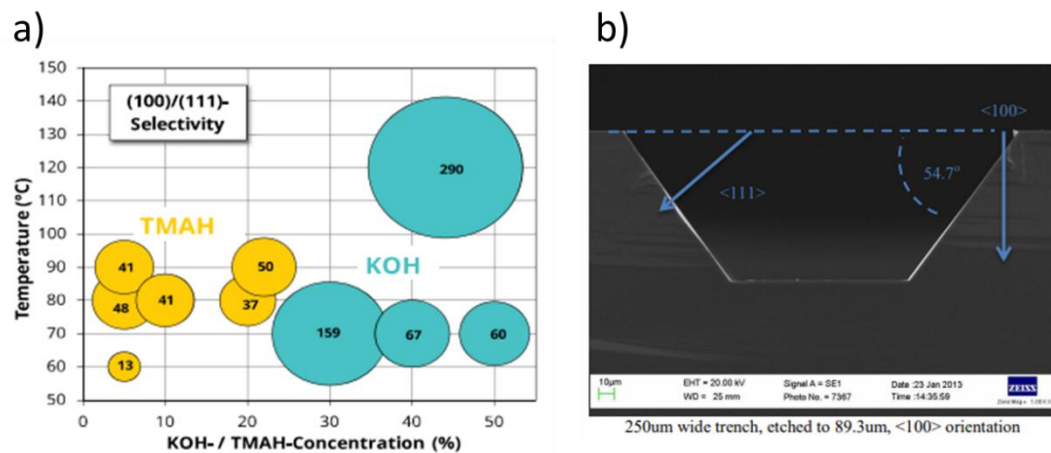


Figure 7 – (a) The ratio of etch rates of silicon in the <100> and <111> directions in TMAH (yellow) and KOH (green); (b) trench etched by KOH etch. Adapted from [12,13].

In the case of pores formation, (100) crystallographic faces contain strained Si-H bonds, making it more prone to dissolution compared to other faces. The (111) face is hydrogen-terminated, with the hydrogen atoms being more strongly bonded to the silicon atoms, making it more stable [6]. Because the “path of least resistance” can be sideways through the wall of a pore, due to the direction the pores are being formed on, branching can occur, hence the morphology of the pores also vary depending on the direction they are being formed. Figure 8 illustrates the porous

silicon growth with different orientations on n-type samples. In the different examples,  $\langle 100 \rangle$  is always the main growth direction.

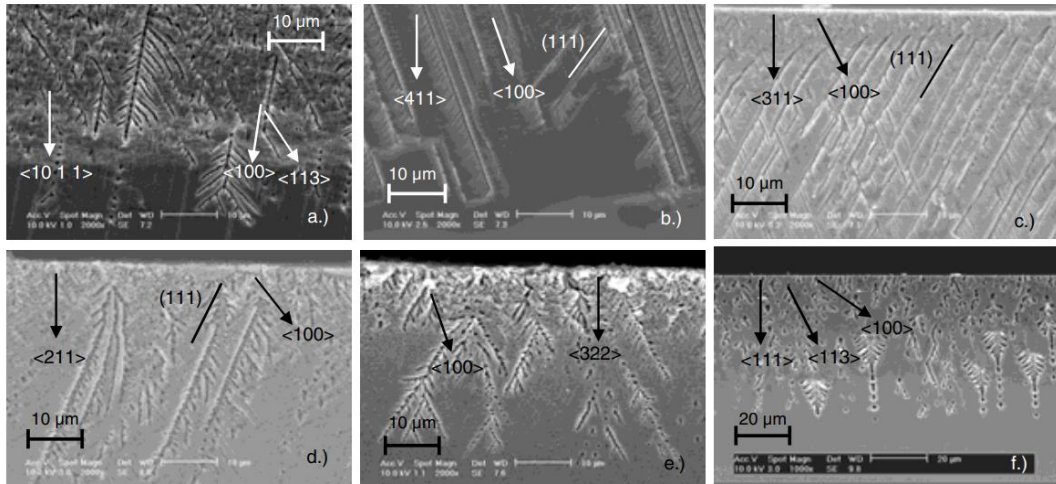


Figure 8 – Macropores silicon being formed in samples with (1,1,10), (114), (113), (112), (223) and (111) orientations, where the main growth direction is always  $\langle 100 \rangle$  [14].

### 1.1.3. Influence of the anodization parameters

Porous silicon formation upon anodization takes place in specific electrochemical conditions. Those conditions are better characterized by  $i$ - $V$  curves (figure 9): at small anodic overpotentials, the current increases exponentially with the electrode potential. As the potential is increased, the current exhibits a peak (point of critical current density), and then remains at a relatively constant value. At the region after said peak, the surface is completely covered with an oxide film, and the anodic reaction proceeds through the formation and dissolution of oxide, causing the electropolishing of silicon. Porous silicon forms mainly during the exponential region (it is also formed in the transition region, but with a decreased surface coverage). In the region where pores are being formed, the increase in current density results in more available holes, increasing the pore size and porosity [15].

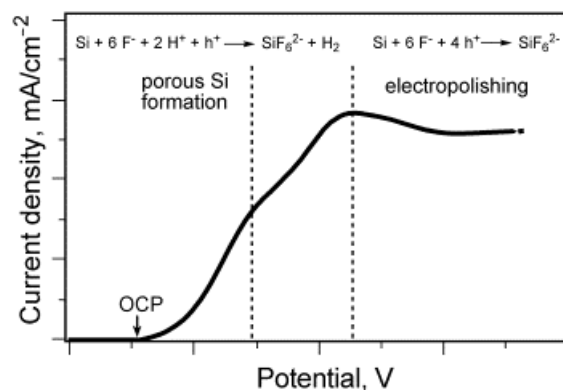


Figure 9 – Current-potential curve for p-type silicon in 1% HF solution. OCP indicates the open circuit potential of the silicon electrode [6,15].

Considering the same substrate, the characteristics of the different regions depend mainly on the HF concentration. The HF concentration plays a central role in anodization through the etching of oxidized silicon. On the one hand, when low concentration of HF is used, oxidized silicon atoms are generated at the surface too rapidly to be attacked by fluoride ions, allowing water molecules to take over the role of nucleophile, forming Si-O bonds (shown in figure 10). This lack of fluoride ions means that the oxide is not removed from the surface, terminating the propagation of pores. On the other hand, a high concentration of HF etches the formed oxide way too fast, leading to the formation of micropores. Furthermore, the maximum current density that can be used before electropolishing increases with increasing HF concentration. [16].

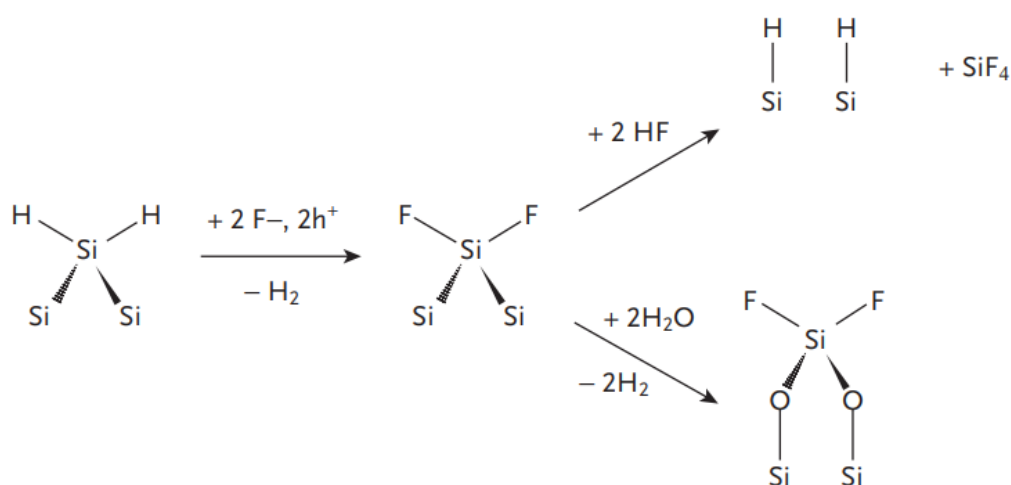


Figure 10 – Role of the HF concentration on the anodization process [6].

Alongside the aqueous HF, a surfactant (wetting agent) is also commonly added to the electrolyte, in order to help preventing evolving hydrogen bubbles from sticking to the porous silicon surface. Among different reagents that can play this part, alcohols and other organic solvents are the most used [17]. Despite the mentioned role, the organic solvent has also the function of retarding the dissolution of silicon by passivating its surface due to the low polarity of the Si-H and Si-C bonds [6]. The classical solvent used is ethanol, however tests with other alcohols of varying chain sizes have shown an increased stability in the pores formation while using higher current densities.

Urata et al. [18] studied the impact of electrolyte composition with low concentration of HF on the fabrication of macro porous silicon on <100> p-type boron-doped silicon wafers (resistivity of 10-20  $\Omega$ .cm). They tested various solvents: methanol (MeOH), ethanol (EtOH), 2-propanol (PrOH) and t-butanol (BuOH). The solutions used were mixtures of HF (47 wt.%), ultra-pure water and the cited alcohols, with compositions of 5:6:29 or 22:6:12 in volume. Whereas, the use of

methanol does not enable pore formation, the use of propanol and butanol leads to pores with morphologies that depend on the number of carbon atoms in the alcohol (figure 11).

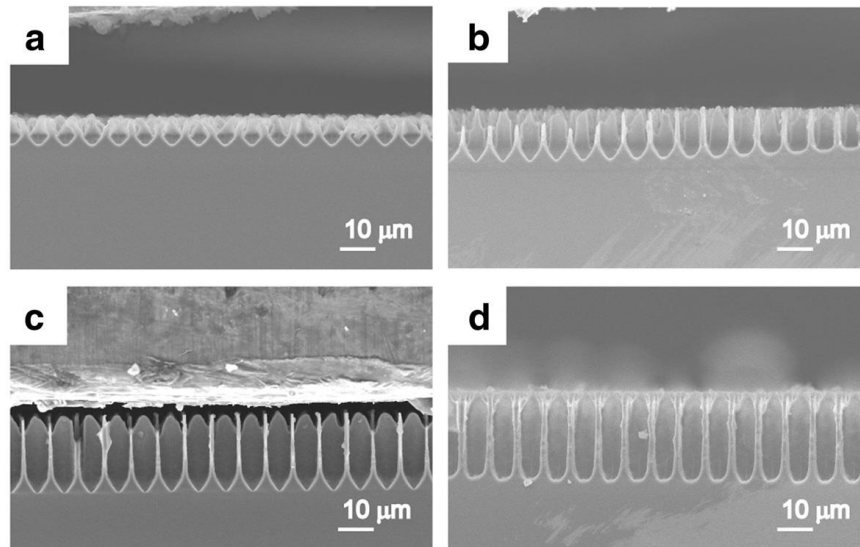


Figure 11 – SEM views of porous silicon formed by anodization using  $14 \text{ mA/cm}^2$  for 1 hour in HF solutions with (a) MeOH, (b) EtOH, (c) PrOH, and (d) BuOH [18].

## 1.2. Porous silicon characterization

### 1.2.1. Pore size

Due to the typical nanometric size of the pores, it is not trivial to properly characterize porous silicon. Several approaches that take advantage of the interesting physicochemical properties of the material have been performed by researchers. Among them, microscopy characterization techniques have been widely used because they are simple and they provide a direct characterization that, in many cases, is nondestructive [19]. Regarding the pore size, the use of a high-magnification scanning electron microscope (SEM) is the most common microscopy technique. It can be used for the characterization of lateral porous silicon. SEM can be used to view the pores from two positions. First a plan-view position (figure 12a), where we see the pores on the etching face (wafer's top face for standard vertical porous silicon and the step's front/back faces for lateral porous silicon samples shown in chapter 1). The disadvantage of this viewing angle is that a "crust" of pores smaller than the rest of the layer is often formed due to the segregation of dopants at the surface [6], so the measured pores can be smaller than they actually are within the layer.

The second position is the cross-section view (figure 12b) of the pores, which requires the cleavage of the chip, being a destructive but more precise and informative technique.

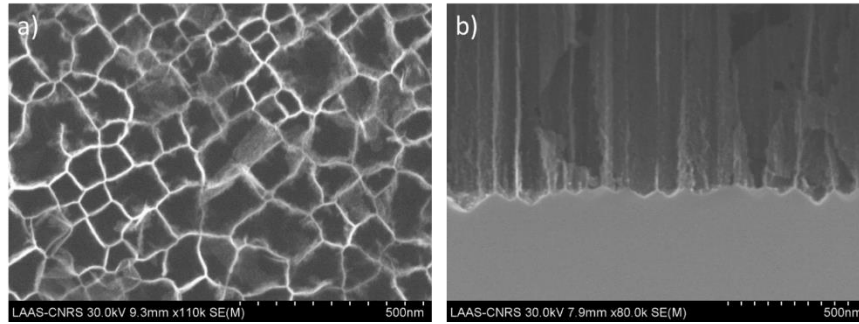


Figure 12 – SEM images of p+-type porous silicon fabricated with 1:1 HF:ethanol, 370 mA/cm<sup>2</sup> for 30s. (a) Shows the plan-view and (b) the cross-section view.

### 1.2.2. Porosity

The measurement of the porosity can be carried out in various ways. The simplest of them is to analyze the SEM images. However, this method lacks accuracy as it depends on human or software's interpretation of the images, making it an indirect method. From our experience of using this method compared to other techniques, we noticed that the lack of accuracy increases with the increase of porosity, and it is very inefficient for porosities above 60% (see example below).

Another very popular method found in the literature is the gravimetric analysis. Porosity is simply obtained by measuring the mass of the chip before and after the electrochemical anodization and, then, after etching away the porous layer. Despite being simple to implement, gravimetric analysis is destructive and limited to fairly large porous silicon samples. For example, in the case of a lateral porous silicon membrane of transversal dimensions 100x5  $\mu\text{m}^2$  and 10  $\mu\text{m}$  thick, with 40% of porosity, the removed mass is around 0.005  $\mu\text{g}$ , which is much lower than the resolution of standard analytical balances (0.001 mg). Other disadvantage of the gravimetric analysis is that the porous layer is considered uniform and that small variations in morphology due to current distribution are not taken into account, it provides an averaged value. Moreover, when porous silicon is etched, a very thin layer on the top can be dissolved in the electrolyte during its formation, resulting in a reduction of thickness of the porous silicon layer [6].

The third characterization technique, the Spectroscopic liquid infiltration method (SLIM), is based on the analysis of Fabry-Pérot thin-film interferences. A Fabry-Pérot interferometer is an optical cavity (here transparent porous silicon sandwiched between air and silicon) with two parallel reflecting surfaces. When a beam of light hits the interferometer, part of the light is reflected on the first reflecting surface, while some is transmitted and reflected on the second surface (figure 13) [20].

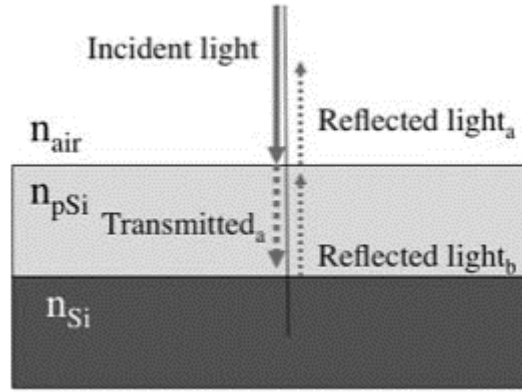


Figure 13 – Representation of porous silicon based Fabry-Pérot interferometer [6]

The reflectance spectrum of this structure displays a series of interference fringes that represents the constructive and destructive interferences of the beam reflected at each interface. The position of the fringe maximum can be interpreted as when both beams are in phase, resulting in the following equation [21,22]:

$$m\lambda_{max} = 2nL \quad (1)$$

Where  $m$  is an integer that corresponds to the spectral order of the fringe,  $\lambda_{max}$  is the wavelength of the fringe maxima,  $n$  and  $L$  are the refractive index and the thickness of the porous silicon layer. The term “ $2nL$ ” is referred as effective optical thickness (EOT). The EOT can be measured by applying the reflectometric interference Fourier transform spectroscopy (RIFTS) method on the reflectance spectrum, which computes the frequency spectrum of an input waveform, and, through a Fourier transform, yields a peak whose position along the x-axis corresponds to the EOT.

As explained in chapter 1, the refractive index of the porous silicon can be associated with the refractive index of silicon and the filling medium by the Bruggeman model with the following equation [6]:

$$P \frac{n_{fill}^2 - n^2}{n_{fill}^2 + 2n^2} + (1 - P) \frac{n_{skeleton}^2 - n^2}{n_{skeleton}^2 + 2n^2} = 0 \quad (2)$$

Where  $n_{fill}$  is the refractive index of the filling medium,  $n_{skeleton}$  the refractive index of silicon,  $n$  the refractive index of the porous silicon layer, and  $P$  the porosity.

SLIM consists of completing this analysis for two different filling media of known refractive indexes, such as air and ethanol, for example. With the EOT being measured for both, it is possible to solve equations 1 and 2 to find both the porosity and thickness of the porous silicon layers.

For the case of lateral porous silicon, SLIM is of special interest. The thickness of the lateral porous silicon membrane is well defined and constant throughout several samples, determined during the fabrication process (better presented in section 2 of this chapter), be it by the ion implantation profile, or by the device layer thickness of the silicon-on-insulator (SOI) wafer. With a known layer thickness, SLIM can be simplified and used with a single filling medium, such as air. However, when they are fabricated with the SOI method, we need to consider the arrangement of a double-layer structure composed by one layer of porous silicon and one layer of silicon dioxide.

SLIM can be much more precise than gravimetric analysis for being a more punctual solution due to the small observation windows that can be used (of a few thousands square micrometers in area). However, it does not take in consideration possible morphology variations along the thickness of the layer, which is particularly relevant for the case of lateral porous silicon fabricated by processes including implantation doping.

To exemplify each of those techniques we mentioned here, three vertical porous silicon samples were fabricated with three different recipes using the same p-type silicon wafer (<100> wafer,  $d = 100$  mm,  $t = 525$   $\mu\text{m}$ ,  $\rho = 3$   $\text{m}\Omega\cdot\text{cm}$ ): i) 3:1 HF:ethanol electrolyte, current density of  $160$   $\text{mA}/\text{cm}^2$  for  $60$  s (pores size  $\sim 15$  nm, thickness  $\sim 8.1$   $\mu\text{m}$ ); ii) 1:1 HF:ethanol electrolyte, current density of  $300$   $\text{mA}/\text{cm}^2$  for  $60$  s (pores size  $\sim 50$  nm, thickness  $\sim 10.0$   $\mu\text{m}$ ); and iii) 1:1 HF:1-butanol electrolyte, current density of  $400$   $\text{mA}/\text{cm}^2$  for  $60$  s (pores size  $\sim 70$  nm, thickness  $\sim 13.5$   $\mu\text{m}$ ). Using the image analysis software ImageJ, we measured the porosities of each chip based on their SEM images by counting the pixels based on the contrast of the images. The gravimetric analysis and SLIM (the interferometric spectra were processed with the software Wavemetrics Igor Pro, using the program Fringe\_24\_1.pxp written by M. J. Sailor, available at <http://sailorgroup.ucsd.edu/software>) were also applied to each of them, and the porosity for each chip can be seen in the table 1 below:

Table 1 – Porosities (%) measured for different chips using the three available techniques.

Chip	Porosity [%]		
	Image analysis	Gravimetric analysis	SLIM
i)	$54 \pm 1$	$57 \pm 6$	$52.1 \pm 0.1$
ii)	$67 \pm 1$	$88 \pm 6$	$77.9 \pm 0.1$
iii)	$55 \pm 1$	$90 \pm 4$	$86.3 \pm 0.1$

While the small increase in values when comparing gravimetric analysis to SLIM was expected due to the aforementioned morphology variation along the etched area (it is important to mention that for both image analysis and SLIM measurements were carried out at the center of the samples), the image analysis measurement

was not consistent as the porosities increased. This is due to a reduced contrast on the images at high porosity. By manually adjusting the contrast, it was possible to reach the expected porosity of sample iii ( $\sim 0.88$ ), for example (figure 14), however, human interpretation can make the adjustment arbitrary, thus this technique is highly unprecise for higher porosities.

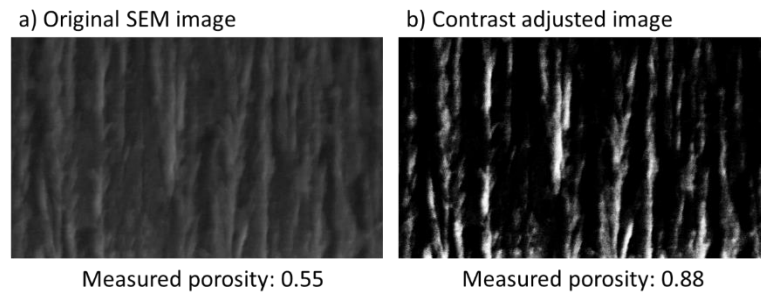


Figure 14 – a) Original SEM image of sample iii; b) contrast adjusted image of sample iii.

## 2. Lateral porous silicon fabrication

As discussed previously, the direction of the applied current influences the direction of pores propagation during the electrochemical anodization. In standard transverse porous silicon fabrication, the current is injected through the backside of the silicon substrate (figure 15a), flowing in the direction perpendicular to the wafer surface. For the fabrication of horizontal pores, we need to position the electrode in a way that the current is guided in a horizontal direction.

This is achieved by sandwiching a high conductivity silicon step between two insulating layers and molding a metal electrode in one side of the step (figure 15b). The top and bottom insulating layers are of primary importance to make sure the current flows solely in the horizontal direction, as it is the path of least electrical resistance.

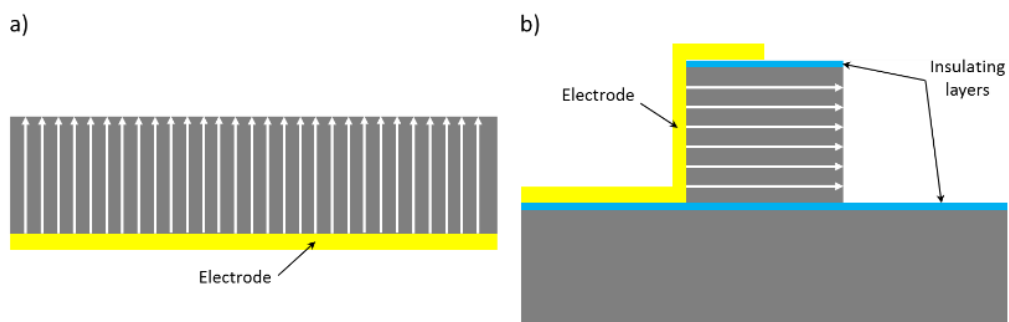


Figure 15 – Simplified schematics of the current flow for (a) transversal porous silicon and (b) lateral porous silicon fabrication.

To accomplish this concept, two different approaches were previously proposed by our research group (both are detailed in the thesis of Yingning He [23]). Each



approach has its own advantages and limitations. The first technique is the silicon-on-insulator (SOI) process, where we use the buried silicon dioxide layer of a SOI wafer as the bottom insulating layer during the anodization. The second technique is the implantation process, where we start from a lowly doped n-type silicon wafer, use boron implantation to form a thick highly doped p-type silicon layer, and then a phosphorous ion implantation to form a thin lowly doped n-type silicon layer on top of it. The n-type layers work, then, as insulating layers.

Our group used the software COMSOL Multiphysics 4.2a in order to do finite element analysis (FEA) to investigate the two techniques feasibility [23]. In COMSOL, three cases were simulated: the classical transversal pores, SOI lateral porous silicon process, and implantation lateral porous silicon process. Simplified 2D model of the electrochemical cell was made and the electric currents physics interface was used to compute the electrical currents and potentials.

The results of the simulations are seen in figure 16, where the electrical current flow is represented by the white arrows and the potential by the color scale. The horizontal current flow confirms the feasibility of both fabrication methods.

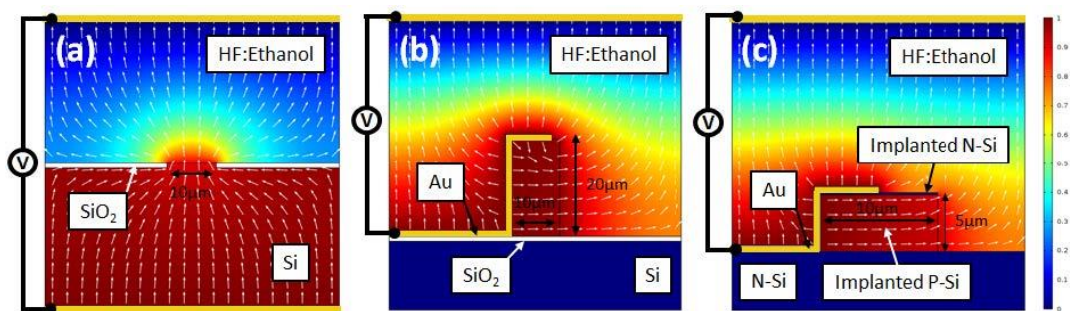


Figure 16 – COMSOL Multiphysics finite element analysis of a) classical transversal porous silicon, b) SOI lateral porous silicon and c) Implantation porous silicon fabrication techniques. The white arrows represent the electrical current flow while the color scale represents the potential [23].

Those approaches were used to fabricate lateral porous silicon membranes integrated within planar fluidics. The fabrication process of 10  $\mu\text{m}$  thick x 20  $\mu\text{m}$  high membranes onto SOI substrate was published in Lab-on-a-chip in 2015 and 10  $\mu\text{m}$  thick x 4  $\mu\text{m}$  high membranes fabricated onto implanted substrates were presented in a Sensors and Actuators B paper published in 2017 [24,25]. For information, details of the fabrication processes are shown in figures 17 and 18.

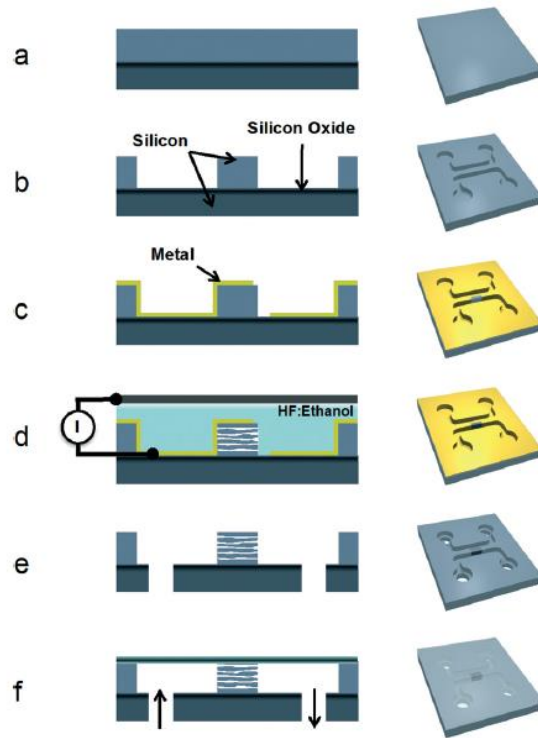


Figure 17 – Lateral porous silicon fabrication by the SOI process. (a) The process starts with a highly doped p-type SOI wafer; (b) reactive ion etching is used to form the microchannels; (c) a metal layer is deposited and then patterned to open the regions where porous silicon are to be formed; (d) after dicing the wafer into chips, they go through electrochemistry anodization in HF medium to form the pores; (e) the metal layer is etched away and the inlets/outlets are opened by sandblasting; (f) the silicon chip is encapsulated by anodic bonding to a glass chip of the same size [24].

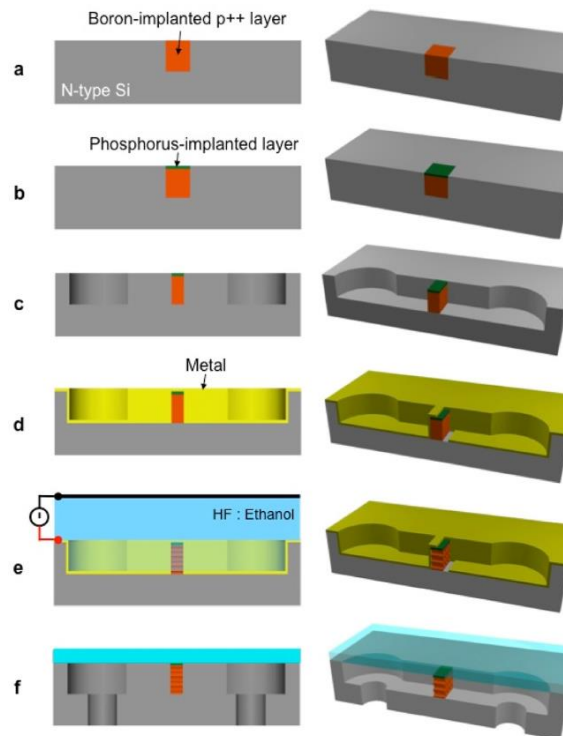


Figure 18 – Lateral porous silicon fabrication by the Implantation process. (a) The process starts by doing a boron implantation on a standard n-type silicon wafer to form a  $\sim 4 \mu\text{m}$  thick highly doped p-type layer; (b) it is followed by a phosphorous implantation to form a  $\sim 100 \text{ nm}$  thick n-type layer; (c) reactive ion etching is used to form the microchannels; (d) a metal layer is deposited and then patterned to open the regions where porous silicon are to be formed; (e) after dicing the wafer into chips, they go through electrochemistry anodization in HF medium to form the pores; (f) the metal is etched away, the inlets/outlets are opened by sandblasting and the silicon chip is encapsulated by anodic bonding to a glass chip of the same size [25].

### 3. Improvements and critical issues encountered in lateral porous silicon fabrication

Regarding the previously established lateral porous silicon fabrication techniques, some general fabrication adjustments had to be implemented before the development of the new fabrication processes.

Moreover, due to the complex nature of the fabrication process, a set of obstacles had to be overcome along the way. Those obstacles impacted the process in different forms, from the necessity to design a new electrochemical anodization cell to the modification of the sample drying steps.

#### 3.1. Fabrication issues to be solved

##### 3.1.1. Dark layer formation

During the fabrication process of lateral porous silicon chips, right after the metallization step, some regions of the metal layer presented a darker color

following the metal annealing. Those regions had random forms and were present on all the different areas of the wafer, no matter which material was at the surface (silicon, silicon dioxide or silicon nitride). Optical microscope images are shown in figure 19, where the contrast between the normal and the darker regions can be seen.

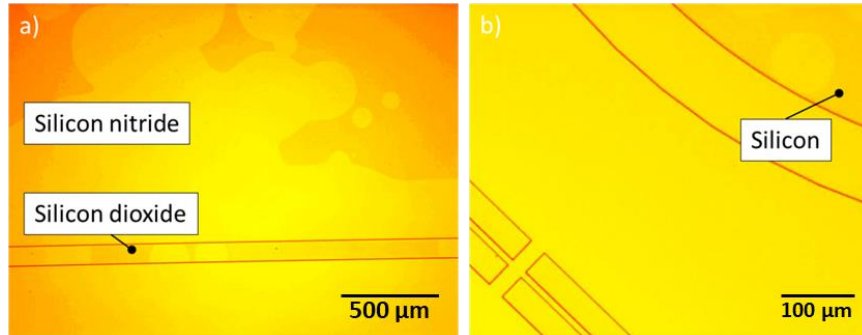


Figure 19 – Optical microscope images showing the dark layer formation over different surfaces: (a) silicon nitride and silicon dioxide; and (b) silicon.

Observing through the metal did not help clarifying if these areas were on the metal layer or on the wafer surface, so the metal layer was etched away on some selected areas. After removing the metal, it was possible to observe a dark layer on the surface of the wafer (figure 20).

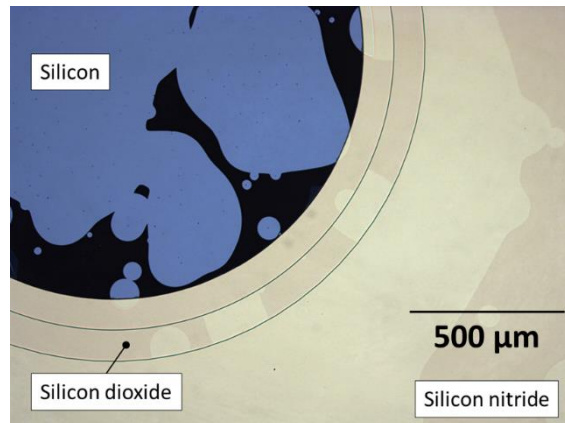


Figure 20 – Optical microscope image showing the dark layer that formed on the wafer surface after removing the metal.

The area covered by this layer varied from wafer to wafer, and in the worst case, the entire wafer surface was covered, as seen in figure 21. The dark layer was found to be easily removed with a piranha (1:1 H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>) bath (figure 22).

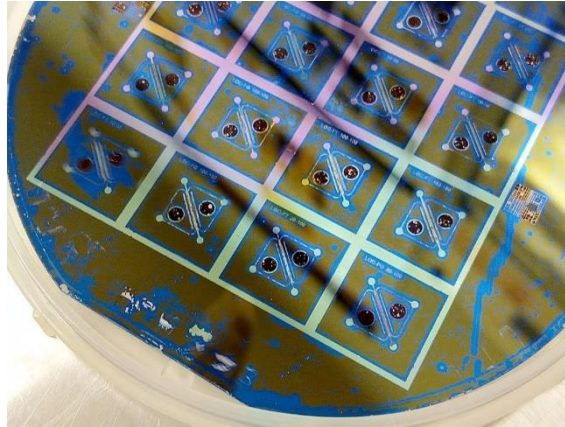


Figure 21 – Wafer affected by the dark layer on most of its surface.

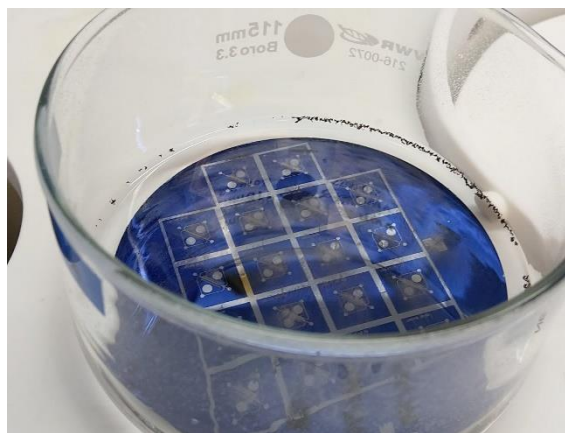


Figure 22 – Wafer affected by the dark layer formation being cleaned in piranha solution.

This led to the hypothesis that this dark layer was of organic nature, which pointed to the photoresist used to mask the wafer during the reactive ion etching processes, before metal deposition. The routine procedure used to remove the photoresist consists in rinsing the wafer with acetone and in carrying out a plasma O<sub>2</sub> cleaning step (800 W for 5 minutes). Visually, this process looked to be good enough. However, the RIE process is known to possibly damage the photoresist layer, making it harder to remove. In our case, we realized that a very thin residue of photoresist was still remaining on the wafer's surface. During the high temperature metal annealing step, this residue was carbonized, thus forming this dark layer.

The issue was solved by improving the cleaning process after the RIE processes. After acetone rinsing, the wafer now goes through a 5 minutes piranha bath, and then is put in plasma O<sub>2</sub> cleaning (800 W) for 15 minutes.

### 3.1.2. Porous metal layer

A second problem related to the metallization step was the quality of the sputtered layer. Indeed, the deposited metal layers displayed pores from 40 nm to over 500 nm in size on the silicon sidewalls, this effect being primarily observed on corners

(figure 23). This has been caused by the difficulty of depositing conformal metal layers on vertical walls of high topography wafers.

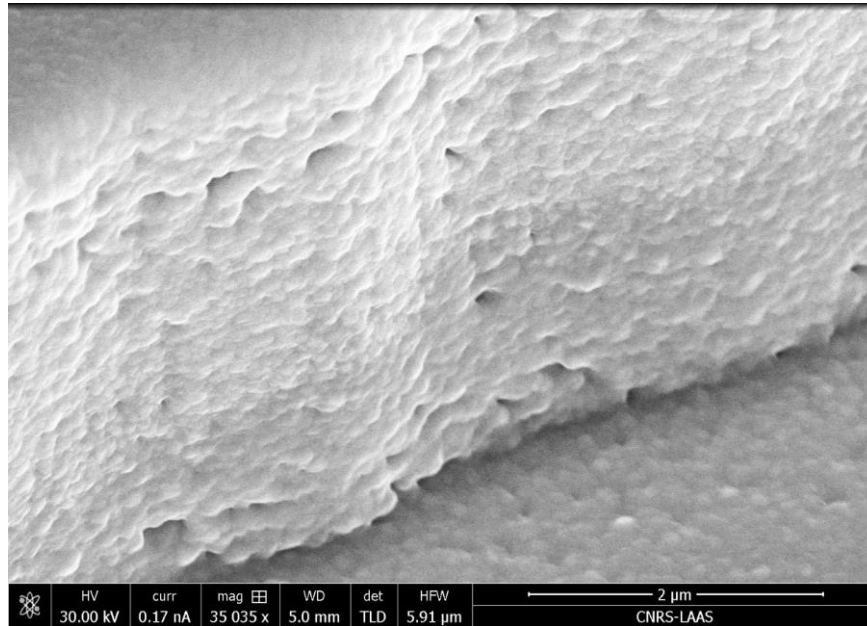


Figure 23 – SEM image of the microchannel wall covered with sputtered metal presenting pores.

Those pores were causing infiltration of the electrolyte during anodization, triggering porous silicon formation on both sides of the step (figure 24) and, also, on the microfluidic channel walls that were not supposed be porous (figure 25).

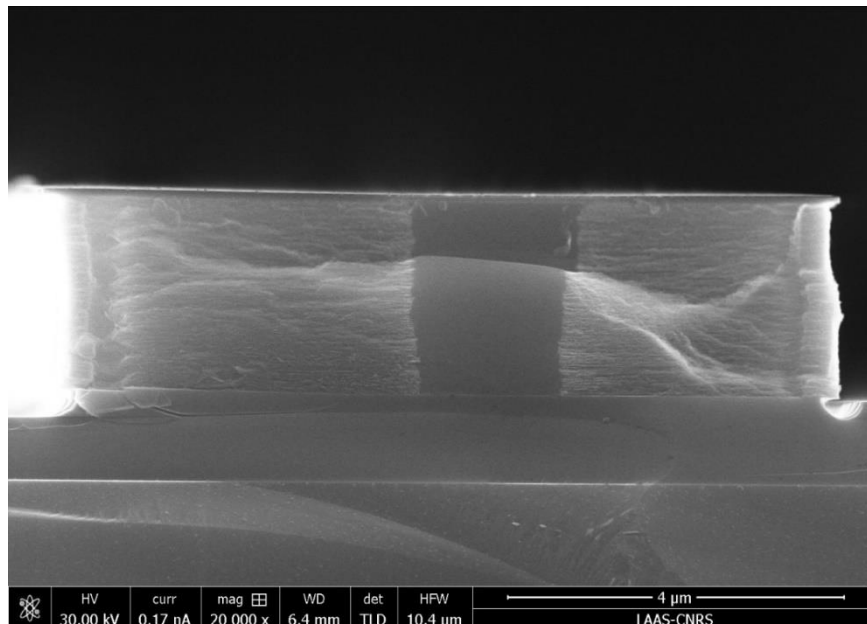


Figure 24 – SEM image of the transversal view of a step with lateral porous silicon formed from both sides on a 2 μm silicon step on a SOI wafer. The darker region observed in the middle is bulk silicon.

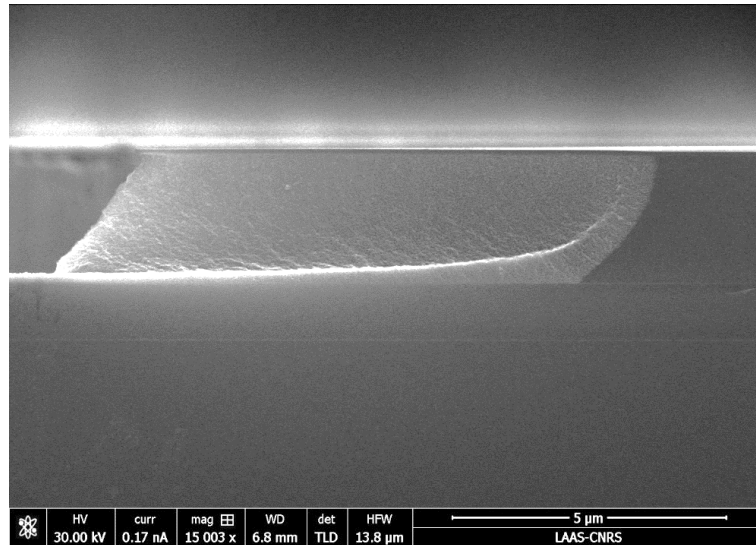


Figure 25 – SEM image showing lateral porous silicon being formed on a microchannel wall, which is supposed to be covered by metal during anodization.

We resolved this issue by using gold deposition through electroplating to thicken the layer by 1 μm, enough to completely fill the pores. As seen in figure 26, the pores were completely closed, while the regions that were supposed to be open, for the anodization to take place, remained open.

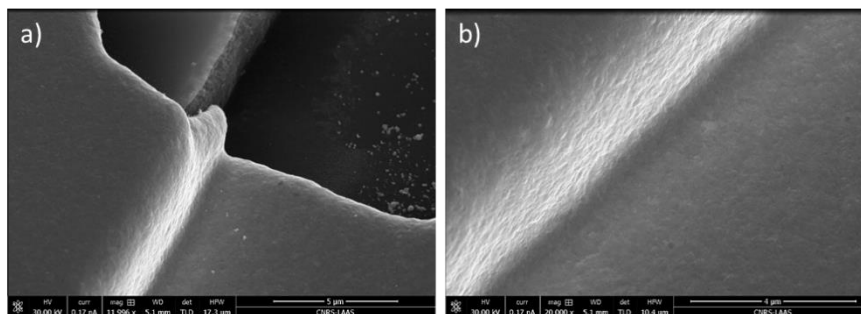


Figure 26 – SEM images showing the metal layer after being thickened by electroplating. In (a) we can see the open regions remain open; in (b) a higher magnification image is shown to better illustrate the uniformity of the metal layer.

### 3.1.3. Membranes damage while drying

In previous works, after performing anodization, we would rinse the chip with ethanol, followed by deionized water, then softly dry with nitrogen. However, due to the high surface tension of water ( $\gamma_{LV} = 72 \text{ mN/m}$ ), water drying could cause the pores to collapse. This issue happened mostly while fabricating membranes with bigger pores and higher porosity, as seen in figure 27.

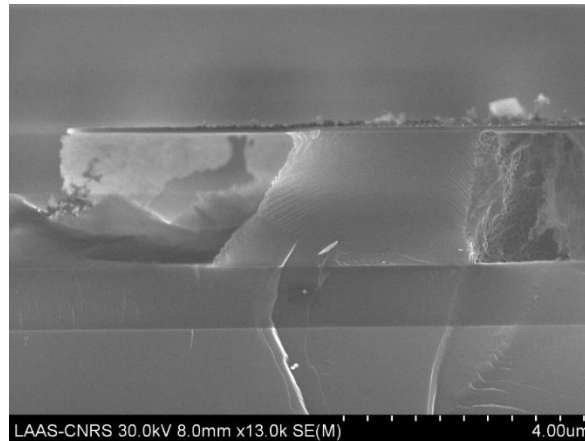


Figure 27 – 10  $\mu\text{m}$  thick lateral porous silicon membrane collapsed due to the cleaning process after anodization. Membrane fabricated using the SOI process, with 1:1 HF:1-butanol, and a current density of  $250 \text{ mA/cm}^2$  for 30 s.

There are different techniques that can be used to improve the drying process of the membranes, the simpler one being the replacement of water in the pores by a liquid with a lower surface tension [26-28]. To this aim, we dipped our samples into an isopropanol ( $\gamma_{\text{LV}} = 23 \text{ mN/m}$ ) bath during 30 minutes to completely replace the water inside the pores before the nitrogen dry. This process was also repeated to dry the porous silicon chips after the metal layer removal by wet etching.

### 3.2. Process improvements

#### 3.2.1. Redesign of the electrochemical anodization cell

The cell used for the electrochemical etching of silicon must fulfill specific requirements related to the use of HF electrolytes: it needs to be made of a material that is compatible with hydrofluoric acid; it has to present reliable electric connections; and it should prevent any leakage of the electrolyte. Previously, we used a cell made of two parts of polyurethane (PU) as seen in figure 28. To provide electric contact between the sample and the electric wires, stainless steel springs (RS Components) were used.

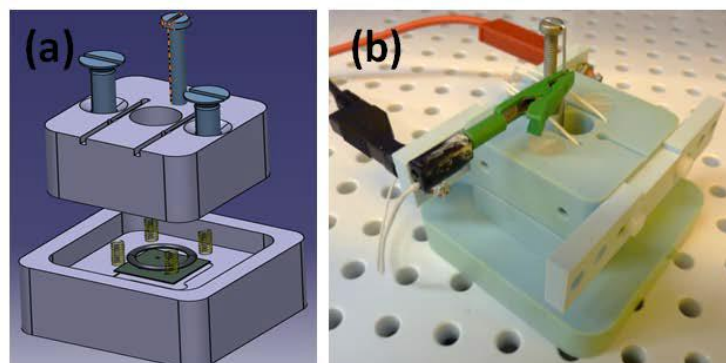


Figure 28 – (a) CAD model of the old cell; (b) photo of the old cell made of polyurethane [23].



However, we detected some issues with this cell. First, the connection between the springs and the electric wires was not reliable, because we could not properly solder the wires to the springs, since the filler metal (a tin alloy) does not attach to stainless steel.

The second concern was with the degradation of PU. After many uses of the same cell, the fit between the two parts was degrading because one of them has expanded. This was caused by the PU becoming porous after an extended exposure to HF. Also, while characterizing porous silicon nanoparticles fabricated with the same electrochemical anodization cell, we detected the presence of a PU layer covering the nanoparticles. This can be seen in the SEM picture below (figure 29).

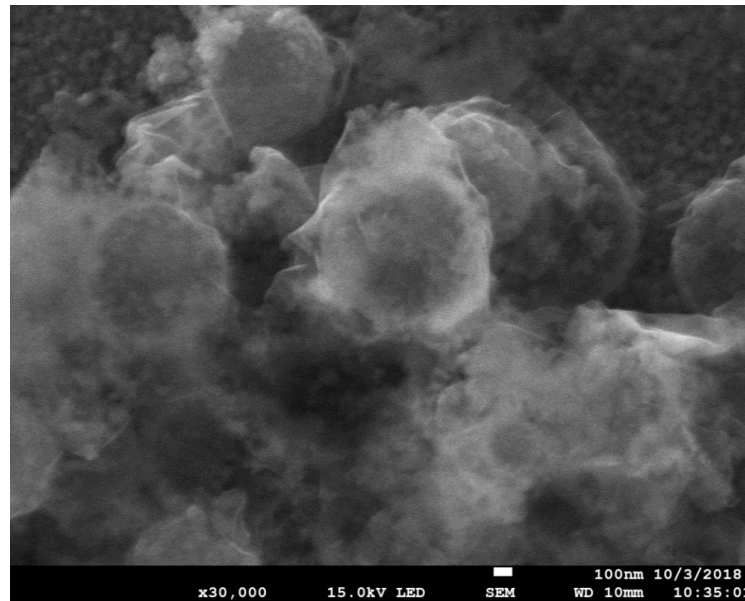


Figure 29 – Porous silicon nanoparticles fabricated with the PU cell covered by a PU layer.

To solve these problems, we designed a new cell with three main changes. First, the two parts that are in direct contact with HF were made with polyether ether ketone (PEEK) and polypropylene (PP), two materials that present better resistance than PU to HF exposition. Second, the springs were replaced with gold-plated discreet spring-loaded contacts (Mill-Max 0914 Spring-Loaded Pin), to allow easier soldering and a more stable connection. The last modification concerned the protection of the fragile wires to avoid breaking them during manipulation.

The new cell was made of four different parts (figure 30). Three of them were fabricated with micromachining: the bottom made of PP, used as the support of the device; the tube made of PEEK, used to get the solution on the top of the chip; and the top cover made of PP, to protect the outer body from drops of HF solution. The outer body was fabricated by 3D printing, using a DWS Precisa DL260 molding resin. The new cell can be seen in figure 31 below, where in (a) the 3D CAD model, and (b) the photo of the actual cell are shown.

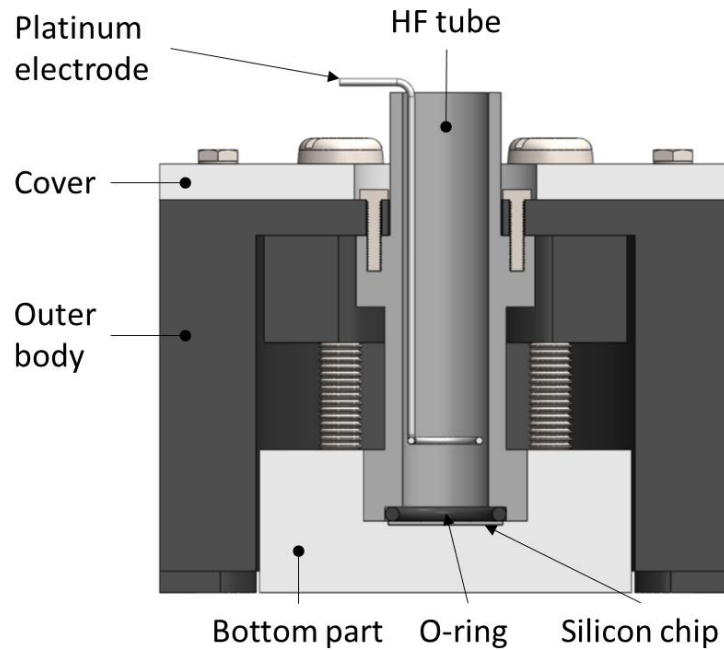


Figure 30 – Schematics of the new cell, with its different parts, the o-ring used to avoid solution leakage, the silicon chip and the platinum electrode.

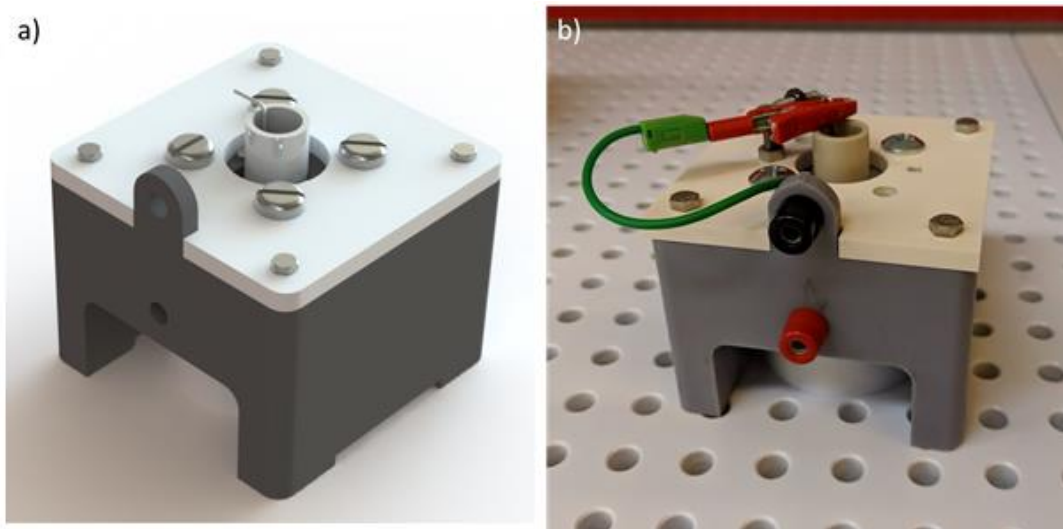


Figure 31 – (a) CAD model of the new cell; (b) photo of the new cell.

### 3.2.2. Silicon nitride used as the top insulating layer

As mentioned in section 2, the basis of lateral porous silicon fabrication consists in insulating the bottom and top of a conductive silicon step. While the bottom layer is more restricted and depends on the substrate and fabrication process, the choice of the top layer is more open.

Previously, our group has been doing phosphorous ion implantation to form a thin layer of n-type silicon to be used as the top insulating layer. However, we now propose the use of a thin silicon nitride layer instead, as its deposition is a cheaper

and faster, while working well as an insulating material (with resistivity over  $10^{15}$   $\Omega\cdot\text{cm}$ ), thus simplifying the overall fabrication process. An alternative to silicon nitride would be silicon dioxide, however, the high etching rate of silicon dioxide in HF medium would require a much thicker layer.

There are two classical methods to deposit silicon nitride. Low Pressure Chemical Vapor Deposition (LPCVD) is a high temperature technique (from 600 to 700°C) which relies upon thermally driven reactions using dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ). Meanwhile, Plasma Enhanced Chemical Vapor Deposition (PECVD) uses plasma with  $\text{SiH}_4$  to lower activation energies required for film formation, and can be done in temperatures under 400°C [29].

When comparing the two methods, the first obvious difference is the operating temperature. In our processes, the deposition of this insulating layer is carried out at the beginning of the fabrication process on a new wafer, so the temperature does not matter. Investigating further, we can also note that the PECVD silicon nitride is etched much faster in HF medium, with etch rates between 150 and 300 nm/min, against 8 nm/min for LPCVD nitride (in HF 49% solution) [30].

To validate the etch rate found in the literature, we did our own test by measuring how long it takes to etch 100 nm of LPCVD deposited silicon nitride in HF 50% solution, and we found a rate of around 10 nm/min. With this value in mind, we decided to use a silicon nitride layer of 80 nm since the electrochemical anodization time is typically kept under 5 minutes in our process.

### 3.2.3. Use of different electrolytes

As we discussed in chapter 1, being able to increase the pore size of the lateral porous silicon is of great importance to achieve better results for the proposed applications. The solvent used in the electrolyte during anodization has a significant impact in the pores morphology. To investigate the possibility of increasing the pore size of the lateral porous silicon membranes, we have fabricated standard vertical porous silicon using various solvents and using p-type silicon substrates with a resistivity similar to that of the substrates used in the fabrication of lateral porous membranes.

Tests were done with methanol, ethanol, isopropanol, and 1-butanol, in solution with HF (50%) at a 1:1 ratio. The reaction time was set to 60 s, while the current density was varied, starting from 200  $\text{mA}/\text{cm}^2$ . The substrates were made from highly doped p-type  $\langle 100 \rangle$  silicon wafers ( $d = 100$  mm,  $t = 525$   $\mu\text{m}$ ,  $\rho = 3$   $\text{m}\Omega\cdot\text{cm}$ ).

For methanol, at 300  $\text{mA}/\text{cm}^2$  the silicon surface was already getting electropolished, limiting the pore size fabricated at a lower current to around 50 nm. For ethanol and isopropanol, the electropolishing started at over 370  $\text{mA}/\text{cm}^2$ ,

and pore diameters reached 80 nm (figure 32a) and 50 nm, respectively. As in Urata's work [18], 1-butanol fabricated pores were more stable, allowing us to use up to 600 mA/cm<sup>2</sup> current density, with pore diameters reaching 110 nm (figure 32b). This result indicates that a higher range of pore diameters can be achieved using 1-butanol. In figure 33, a comparison of both pore size and porosity for ethanol and 1-butanol electrolytes is shown in graphic form.

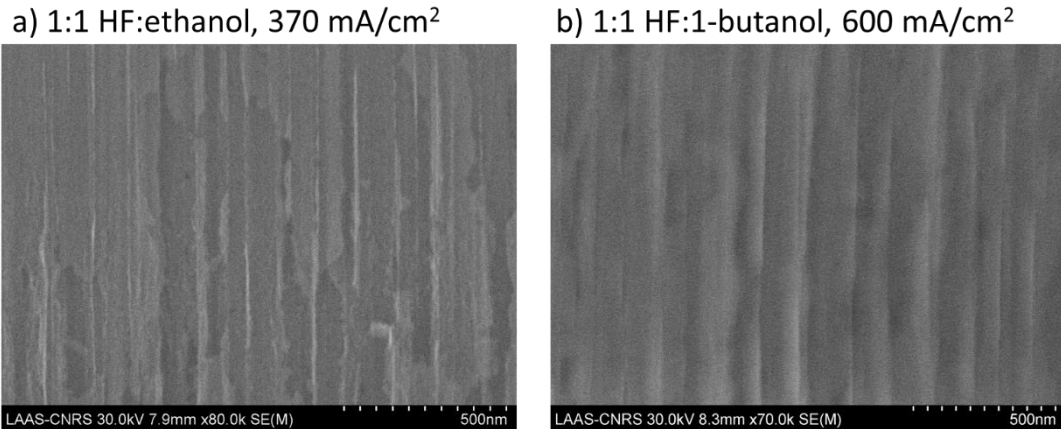


Figure 32 – SEM images of maximum pore sizes achieved using (a) 1:1 HF:ethanol at 370 mA/cm<sup>2</sup>; and (b) 1:1 HF:1-butanol at 600 mA/cm<sup>2</sup>.

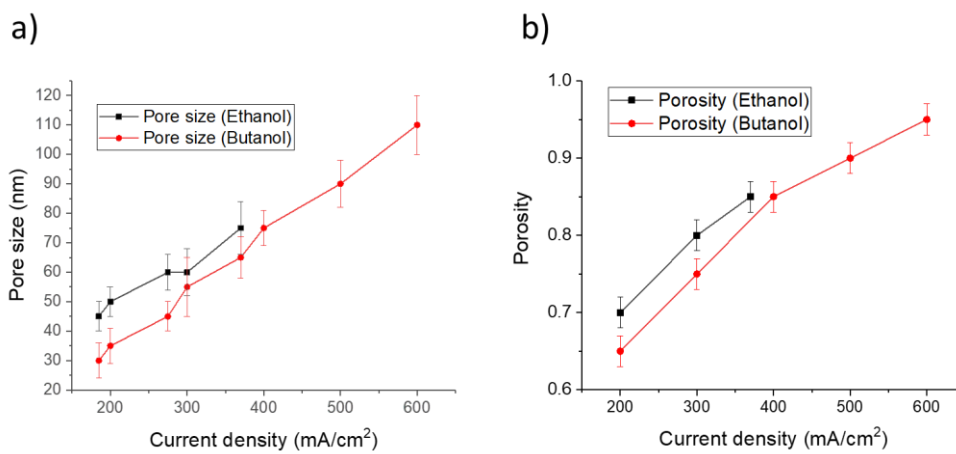


Figure 33 – Comparison of (a) pore size and (b) porosity between the porous silicon formation using ethanol (black) or 1-butanol (red) in its electrolyte.

#### 4. Fabrication of multiple porous silicon elements with controlled characteristics onto a single chip

In order to achieve the fabrication of a porous silicon-based lab-on-a-chip that displays different functions, we need to develop a process that results in porous silicon elements of different morphologies.

The parameters which control the porous silicon morphology can be divided in two categories: wafer-based parameters (doping type and level, crystallographic

orientation), and anodization-based parameters (current density, electrolyte used). To achieve the fabrication of different porous silicon elements in a single chip, we have to be able to change a parameter in one of those categories in selected regions of the chip.

Anodization-based parameters are easier to control, as they are set in one of the last steps of the fabrication process and they are the classical parameters used to control pore morphology during porous silicon fabrication. However, the fabrication of different porous silicon elements through the variation of anodization-based parameters requires the use of multiple anodization steps acting on different parts of the chip by isolating each specified part once at a time. Two approaches can be taken to achieve this. The first one consists in providing isolation through the anodization cell, where the electrolyte reaches only one specified region of the chip at a time. However, both the small size of the chip and the topography formed by the microchannels would most likely cause design and leakage problems, respectively. The second approach consists in providing isolation through protective layers on the chip. This approach adds more fabrication complexity, but it is interesting to be explored due to its likely feasibility through the use of multiple sequential anodization steps. This approach is presented in the next section 4.1.

Wafer-based parameters are not as straight forward to manipulate, and they add limitations as they are defined very early in the fabrication process. Still, we can envision producing membranes with various properties using a single anodization step by modifying the wafer-based parameters locally on the substrate. The parameters that can easily be locally controlled are the type and concentration of dopants. This option, that is explored and presented in section 4.2 can thus have the significant advantage of requiring less fabrication steps.

#### **4.1. Fabrication by sequential anodization steps**

Being able to use sequential anodization steps on a single chip is the easiest route to control the morphology of each porous silicon element we fabricate on different locations of the chip. We developed a method to test the feasibility of implementing multiple anodization steps. This method is based on repatterning a metal layer after the first anodization step, to protect the pores already created and to enable the anodization of another region on the wafer. This was tested on a SOI wafer, following the SOI process described in section 2 (figure 17), that ultimately enables the fabrication of lateral and vertical porous silicon elements on a single chip (see more details in section 4.2.1).

Up to the first anodization step (figure 34a to e), the fabrication process follows the same steps as the ones of the SOI process where the gold layer is only etched at the location of the first porous silicon elements (figure 34d). After the first anodization

(figure 34e), the metal layer is completely removed and a second analogous metal layer is deposited and patterned using a different photolithographic mask designed to open new regions on the wafer while keeping the previously fabricated membrane protected (figure 34f). The second anodization is then carried out (figure 34g), and the metal layer is removed.

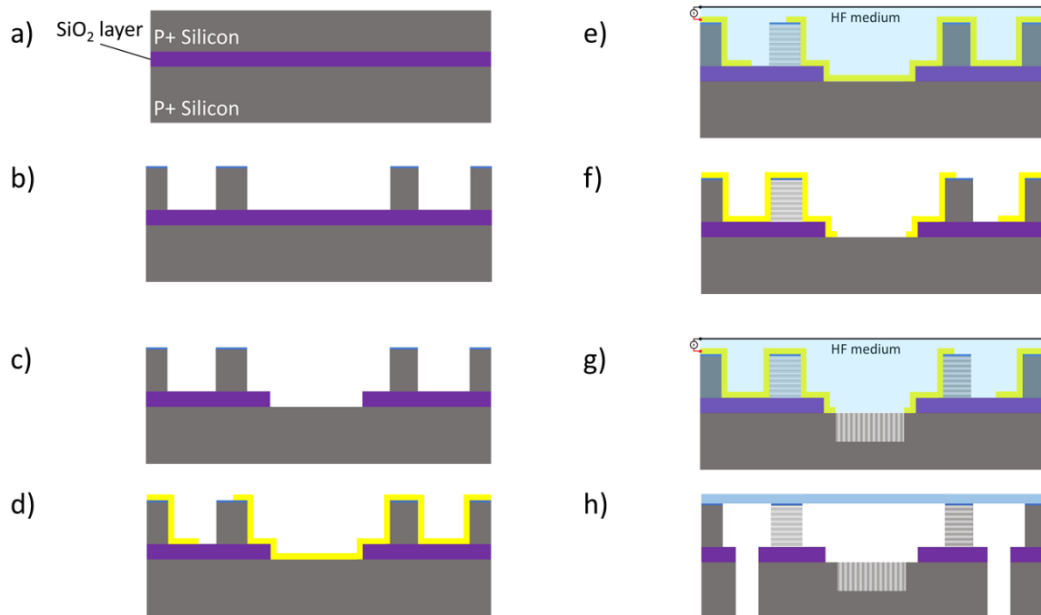


Figure 34 – Process flow for the fabrication of multiple membranes on a single chip using sequential anodization steps. (a) The process starts with a highly doped p-type SOI wafer; (b) a silicon nitride layer is deposited using LPCVD and reactive ion etching is used to form the microchannels; (c) the wafer goes through a second reactive ion etching step to open regions of the buried silicon oxide layer (for vertical porous silicon fabrication); (d) A metal layer is deposited and patterned to open the regions where porous silicon are to be formed during the first anodization step; (e) after dicing the wafers into individual chips, they go through electrochemical anodization; (f) the metal layer is removed, then a second layer is deposited and patterned, opening other regions for porous silicon fabrication; (g) the second anodization step is conducted to fabricate a second set of porous membranes with different characteristics than the previously fabricated ones; (h) the inlets/outlets are opened by sandblasting and the chip is encapsulated by anodic bonding to a glass cover chip.

Preliminary tests following this procedure raised important issues concerning the feasibility of this method. First of all, in addition to exhibiting many additional fabrication steps, because the anodization set-up cell can only host a single chip, the wafer has to be diced right before performing the first anodization step. This means that additional fabrication steps must be done at a single chip level, causing extra complications, especially for the photolithography steps. The second and more important issue we encountered was the damage of the first fabricated porous silicon membranes: indeed, the mechanical stress built during the second

metallization (Cr/Au 100/150 nm) process led to the destruction of the lateral porous silicon membrane (figure 35).

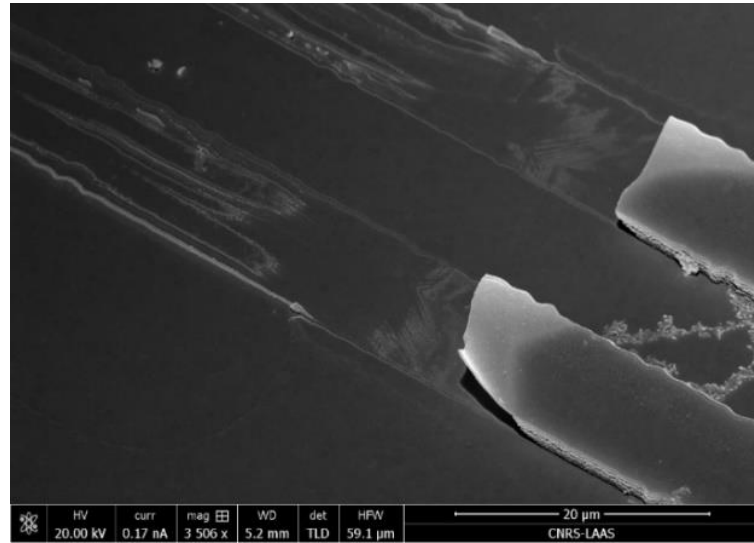


Figure 35 – SEM image of a chip after having a Cr/Au layer deposited on top of it, resulting in the destruction of the lateral porous silicon membranes.

To further investigate the cause of this damage, we deposited a metal layer on two other porous silicon membrane samples: a) 100 nm of Cr (figure 36a), and b) 150 nm of Au (figure 36b). We observe that the membranes were damaged upon deposition of the chromium layer.

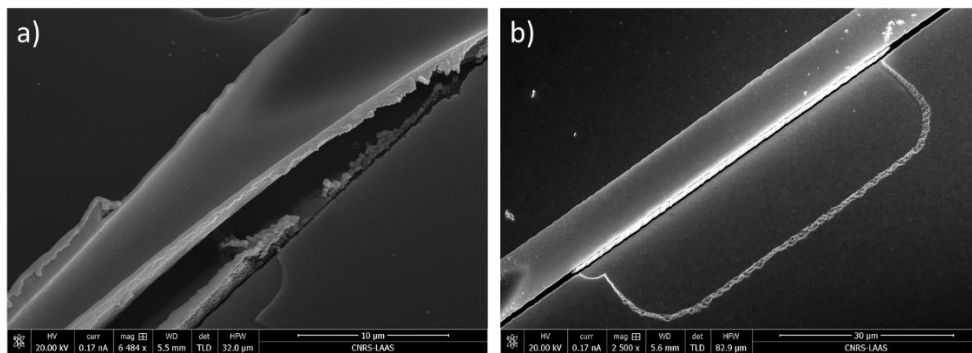


Figure 36 – SEM images of a porous silicon membrane covered with (a) 100 nm Cr (the lateral porous silicon membranes is broken), and (b) 150 nm Au (the membrane is preserved).

This result is not surprising, since high intrinsic stresses caused by the deposition of chromium, due to its low mobility, is a problem well known in the literature [31-33]. However, removing the chromium layer from the process is not trivial because it serves as a proper adhesion layer for gold on silicon.

Hence, further studies are necessary to assess the feasibility of the approach, where the chromium layer could be replaced by another metal (which is not

straightforward due to the process requirements of being HF resistant and of forming an ohmic contact with silicon), or where solutions to reduce the stress could be investigated [34].

Another approach would be to use a single metallization step but use patterned resin to locally protect some open areas in order to select the anodized region for each anodization step.

## **4.2. Fabrication by localized doping level manipulation**

The second approach for multiple membrane fabrication has the advantage of being easier to implement: it relies on manipulating the local dopant concentration and fabricating multiple membranes in a single anodization step. Following the two approaches for lateral membranes fabrication presented in section 2, we have developed two processes to fabricate multiple membranes on a single chip using one anodization step. The first method is called Implanted SOI, and, as the name suggests, it is based on the selective ion implantation of SOI wafers (see section 4.2.1). The second technique is the double Implantation process, and it is based on the ion implantation of standard n-type silicon wafers in order to create highly doped p-type layers with varying doses (see section 4.2.2). Implanted SOI presents the notable advantage of enabling to reach the p-type handle silicon layer at the bottom of the microchannels by etching the buried silicon oxide layer, thus allowing the fabrication of vertical silicon layers along with lateral porous silicon membranes.

### **4.2.1. Implanted SOI process**

The first method we developed allows us to fabricate both lateral porous silicon membranes and vertical porous silicon layers at the bottom of the microchannels. The process uses a highly doped p-type SOI wafer where the buried silicon oxide layer is used as the bottom insulating layer for the lateral porous silicon fabrication. It has been implemented on two different  $\langle 100 \rangle$  p-type SOI wafers: i)  $d = 100$  mm,  $t = 5/2/400$   $\mu\text{m}$ ,  $\rho = 10$  m $\Omega$ .cm at both device and handle layers; and ii)  $d = 100$  mm,  $t = 2/1/450$   $\mu\text{m}$ ,  $\rho = 15$  m $\Omega$ .cm at both device and handle layers.

The implanted SOI process, which is detailed in figure 37, starts by doing a thermal oxidation step to create a 40 nm oxide layer to prevent surface damage and channeling effects during the ion implantation. A photoresist layer (ECI 1.2  $\mu\text{m}$ ), patterned by photolithography, is used to protect the regions that are not supposed to be implanted. Boron implantation and thermal annealing (after photoresist removal) are performed with the aim to increase the dopant concentration of selected regions of the wafer (figure 37b).



After the implantation and the removal of the top oxide layer using buffered HF, an 80 nm silicon nitride layer is deposited on top of the wafer, through LPCVD technique (figure 37c).

The microchannels are created by patterning a photoresist layer (ECI 2.6  $\mu\text{m}$ ) using the microfluidic chip design, and then doing a reactive ion etching (RIE) of the layers of silicon nitride and silicon, stopping at the buried oxide layer, which then serves as the bottom insulating layer (figure 37d).

Another photoresist (ECI 2.6  $\mu\text{m}$ ) mask and a RIE step are used to open areas in the buried oxide where we want to fabricate vertical porous silicon layers in addition to large areas that are used for better controlling the current density during anodization (figure 37e).

A conformal metal layer of Cr/Au 100/500 nm is deposited by sputtering. A photoresist layer (AZ4562 5  $\mu\text{m}$ ) is coated and patterned, in a way that one side of the step where the lateral porous silicon membranes ought to be formed, and the areas where the vertical porous silicon layers will be created, are open. The wafer then goes through a wet etching process to remove the metal layer and the gold layer is thickened by gold plating (figure 37f). Since the anodization is done on each chip separately, the wafer is diced.

The chip is loaded in the anodization cell and current is provided by a Keithley 2450 sourcemeter to form porous silicon (figure 37g). After the anodization, the metal is removed by wet etching.

The next step consists in opening the inlets/outlets to allow the fluidic connections. A 40  $\mu\text{m}$  thick dry film of photoresist is laminated on the chip (64°C, 2 MPa, DYNACHEM, SA 3024 OC) to protect the porous membranes and the chip surface from physical damage and the inlets/outlets are opened by sandblasting. Finally, the silicon chip is encapsulated by anodic bonding (370°C,  $5 \times 10^{-5}$  mBar, 600 V for 10 min) to a 500  $\mu\text{m}$  thick borofloat 33 (Schott) glass chip of the same size (figure 37h).

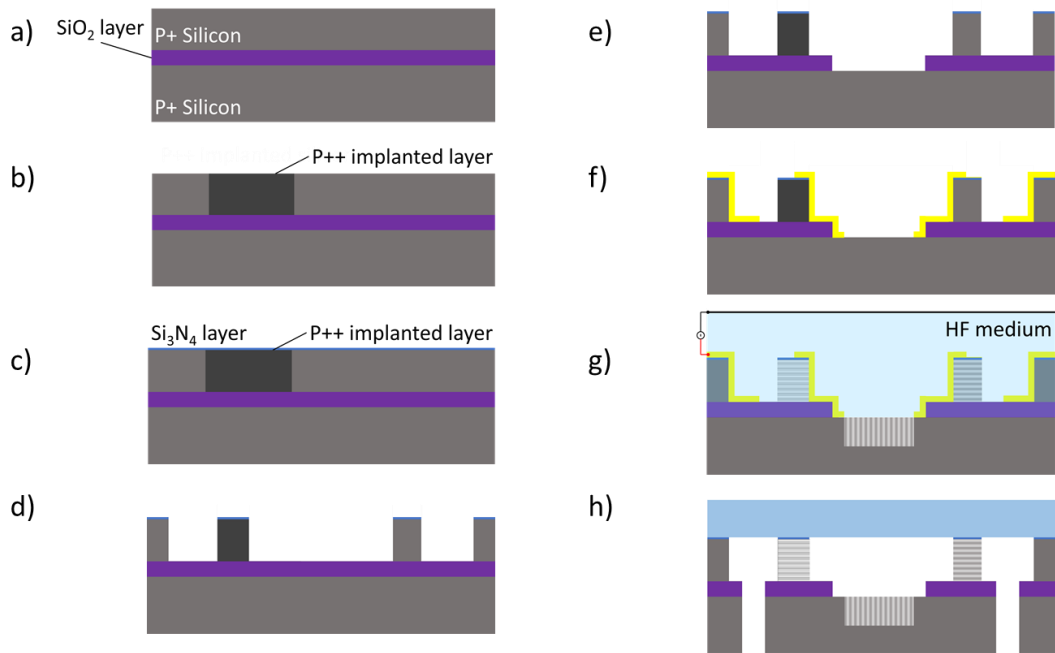


Figure 37 – Implanted SOI process flow. (a) The process starts with a highly doped p-type SOI wafer; (b) A selective boron implantation is done to form an even higher doped layer; (c) A silicon nitride layer is deposited using LPCVD; (d) Reactive ion etching is used to form the microchannels; (e) The wafer goes through a second reactive ion etching to open regions of the buried silicon oxide layer; (f) A metal layer is deposited and then patterned to open the regions where porous silicon is to be formed; (g) After dicing the wafers into chips, they go through electrochemical anodization in HF; (h) The inlets/outlets are opened by sandblasting and the chip is encapsulated by anodic bonding to a glass chip.

#### 4.2.2. Double Implantation process

A second process was developed based on the previously presented Implantation process for lateral porous silicon fabrication and the use of standard silicon wafers. This process starts by forming a top highly doped p-type layer using a strong boron implantation in a standard n-type silicon wafer. The n-type bulk silicon serves as an insulating layer under the step where the lateral porous silicon membrane is to be formed.

Unlike the implanted SOI method, the double implantation process has the disadvantage of not permitting the fabrication of vertical porous silicon in the bottom of the microchannels, thus restricting the porous silicon elements to lateral porous silicon membranes. Also, as low doped p-type silicon and n-type silicon can still be affected by the anodization, the porous silicon/silicon interface is not as clearly defined.

Starting with a n-type silicon wafer (<100>, d = 100 mm, t = 525  $\mu\text{m}$ ,  $\rho = 7 \Omega$ ), a thermal oxidation process is performed to form a 40 nm silicon oxide layer on the

surface of the wafer. A first boron implantation is done to form the p-type layer on the entire area of the wafer (figure 38a).

Before a second implantation step, a photoresist (ECI 2.6 $\mu$ m) is patterned so that regions where higher dopant concentration is desired, are open. The second boron implantation increases the boron concentration in the selected open region (figure 38b). After the resist is removed, the wafer goes through a long thermal annealing step to activate the implanted ions from both implantation steps, creating a layer of around 4  $\mu$ m of p-type silicon, with regions of different concentrations. Then, the oxide layer is etched away using HF 5%.

Following the implantation steps, an 80 nm silicon nitride layer is deposited using LPCVD to form the top insulating layer (figure 38c).

A mask with the microfluidic design is used to pattern photoresist (ECI 2.6  $\mu$ m), and the wafer goes through reactive ion etching to create 5  $\mu$ m deep microchannels (figure 38d).

A second reactive ion etching process is carried out to etch silicon nitride on large areas of the chip for better current density control during anodization.

From this point on, the process is similar to the implanted SOI process: a Cr/Au 100/500 nm layer is deposited, patterned and thickened (using AZ4562 5  $\mu$ m as the mask) and a 20 min thermal annealing at 250°C is carried out (figure 38e). The wafer is diced into chips and the chips are put through electrochemical anodization in HF medium (figure 38f). After protecting the chip with a 40  $\mu$ m thick dry film of photoresist (64°C, 2 MPa, DYNACHEM, SA 3024 OC), the inlets/outlets are drilled using sandblasting. Finally, the chip is encapsulated by anodic bonding (370°C, 5x10<sup>-5</sup> mBar, 600 V for 10 min) to a 500  $\mu$ m thick borofloat 33 (Schott) glass chip of the same size (figure 38g).

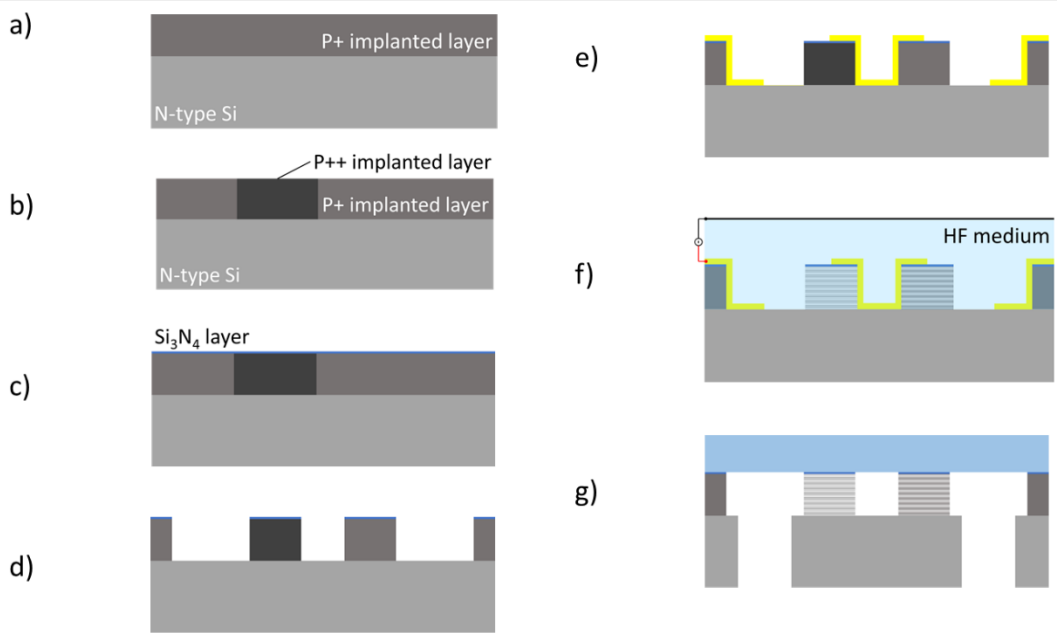


Figure 38 – Double Implantation process flow. (a) The process starts by doing a first boron implantation on a standard n-type silicon wafer; (b) A selective boron implantation is done to form an even higher doped layer in some regions of the wafer; (c) A silicon nitride layer is deposited using LPCVD; (d) Reactive ion etching is used to form the microchannels; (e) A metal layer is deposited and then patterned to open the regions where porous silicon are to be formed; (f) After dicing the wafers into chips, they go through electrochemical anodization in HF medium to form the pores; (g) The inlets/outlets are opened by sandblasting and the chip is encapsulated by anodic bonding to a glass chip of the same size.

#### 4.2.3. Manipulating the local dopant concentration by ion implantation: simulations and characterization

Using the mathematical simulation software Athena (Silvaco Int.), from which we are able to obtain two-dimensional dopant profiles, different doses of boron implantation were simulated for the selective implantation step in both fabrication processes.

For the implanted SOI technique, we start the simulation with the Fermi Compress model, simulating the 40 nm oxide layer formation on p-type silicon wafers with a boron concentration of  $9.72 \times 10^{18} \text{ cm}^{-3}$  (5  $\mu\text{m}$  SOI equivalent) and  $6.07 \times 10^{18} \text{ cm}^{-3}$  (2  $\mu\text{m}$  SOI equivalent). Aiming at reaching boron concentrations above  $1 \times 10^{19} \text{ cm}^{-3}$ , a value that is known to cause a relevant impact in the pores morphology (as shown in figure 6), we use the Dual Pearson Implant model to model the boron implantation, considering high ion energy of 150 KeV and doses of  $1 \times 10^{15}$ ,  $5 \times 10^{15}$  and  $1 \times 10^{16} \text{ cm}^{-2}$  (which is the limit of the machine we have in the laboratory). The Fermi Compress model is used again, this time to simulate the long thermal annealing process at a high temperature (8h, 1150°C), which is used to activate the

dopants and to repair the damages caused within the silicon crystal lattice, as well as to increase the doped layer depth through the dynamic diffusion of dopant atoms. It is important to note here that our model is overly simplified since we do not consider the presence of the buried oxide (BOX) layer.

The same was done for the double implantation process, but this time the Pearson Implant model was repeated to consider two boron implantations on a n-type silicon wafer with a phosphorous concentration of  $6.49 \times 10^{14} \text{ cm}^{-3}$ :

- i) First implantation: ion energy of 150 KeV and dose of  $2 \times 10^{15} \text{ cm}^{-2}$ ;
- ii) Second implantation: ion energy of 150 KeV and dose of  $1 \times 10^{15}$ ,  $5 \times 10^{15}$  and  $1 \times 10^{16} \text{ cm}^{-2}$ .

Figure 39 presents the resulting simulated profiles for each dose and for the three different wafers: 2  $\mu\text{m}$  SOI (figure 39a), 5  $\mu\text{m}$  SOI (figure 39b) and Double implantation (figure 39c).

For both types of SOI wafers, the simulations show that using a dose of  $1 \times 10^{16} \text{ cm}^{-2}$  we are able to keep the dopant concentration above  $1 \times 10^{19} \text{ cm}^{-3}$  on the entire height of the membranes: reaching up to  $3.1 \times 10^{19} \text{ cm}^{-3}$  for the 2  $\mu\text{m}$  SOI and  $3.4 \times 10^{19} \text{ cm}^{-3}$  for the 5  $\mu\text{m}$  SOI at the surface. Regarding the Double implantation process, the dopant concentration is  $3.1 \times 10^{19} \text{ cm}^{-3}$  at the surface, and is above  $8.0 \times 10^{18} \text{ cm}^{-3}$  (desirable limit for a highly doped p-type layer in a n-type substrate), up to 4.9  $\mu\text{m}$  deep.

Athena works with two different Dual Pearson models: SIMS-Verified Dual Pearson model (SVDP) and a standard Dual Pearson model. While SVDP is more precise and chosen as default when doses are under  $8 \times 10^{15} \text{ cm}^{-2}$ , the  $1 \times 10^{16} \text{ cm}^{-2}$  target dose requires simulations to be done with the standard Dual Pearson model. However, this model lacks accuracy [35]. Hence, to experimentally characterize the implanted layer is of extreme importance.

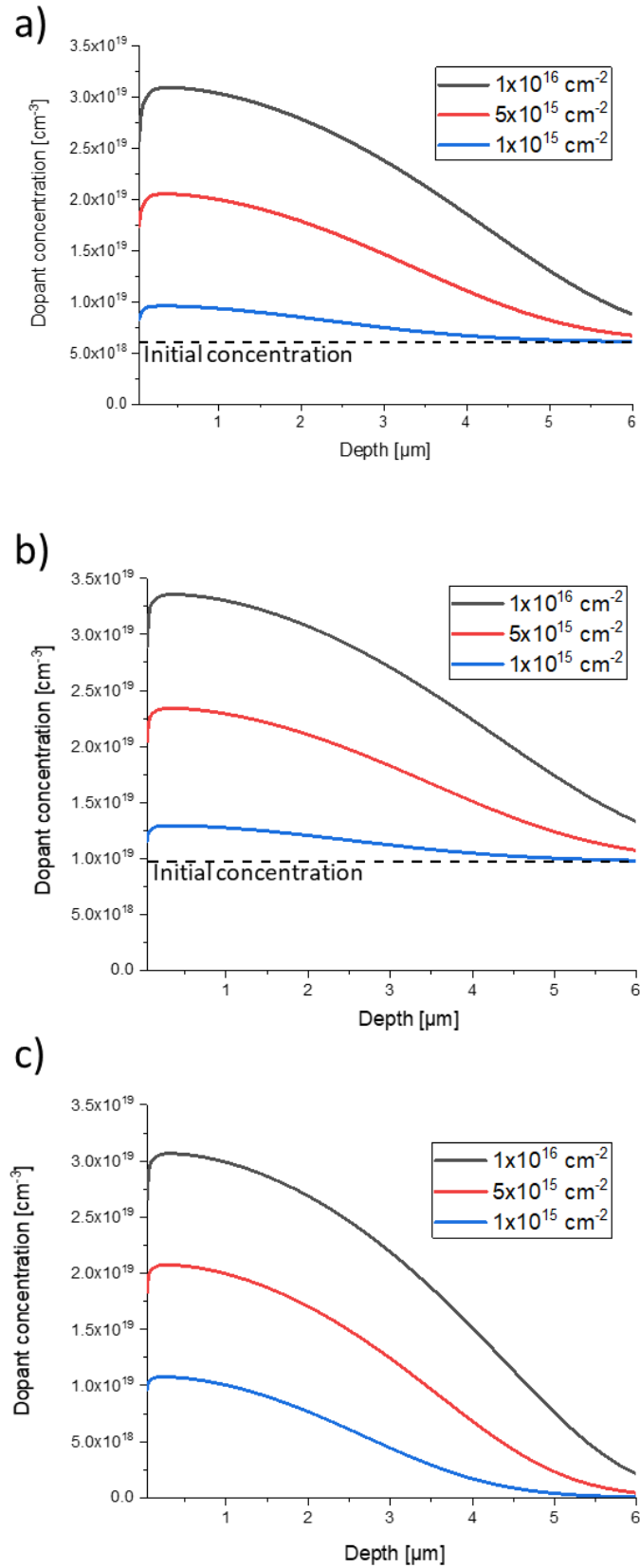


Figure 39 – Simulated boron implantation profiles, obtained from Athena (Silvaco Int.) for (a) 2  $\mu\text{m}$  SOI, (b) 5  $\mu\text{m}$  SOI and (c) Double implantation. Dashed lines in (a) and (b) represent the original dopant concentration of each wafer.

To validate the simulations, we have used two characterization means. The first approach is an electrical characterization of the surface of the wafer using the four-point probe method. This method consists in measuring the sheet resistance of a semi-conductor layer by applying current through four equally spaced probes. The sheet resistance is related to the implantation dose through the following equation [36]:

$$R_S = \frac{1}{qN\mu t} \quad (7)$$

Where  $R_S$  is the sheet resistance,  $q$  the carrier charge ( $1.6 \times 10^{-19}$  C),  $N$  the net impurity concentration,  $\mu$  the mobility of majority carrier, and  $t$  the thickness of the implanted layer. As an approximation, we consider the implanted layer to have a uniform dopant concentration, which equals to the surface value obtained from the curves in figure 39. By comparing the calculated sheet resistances with the ones measured with the four-probe method, we are able to confirm the dopant concentration we were able to reach at the surface of the wafers. We also measured the sheet resistance of each wafer before the selective implantation had taken place. Table 2 presents the calculated and measured sheet resistances for the three different wafers we have used.

Table 2 – Comparison between calculated and measured sheet resistance.

Fabrication technique	$N$ [ $\text{cm}^{-3}$ ]	Carrier mobility [ $\text{cm}^2/(\text{V.s})$ ] [37]	Calculated $R_S$ [ $\Omega/\text{sq}$ ]	Measured $R_S$ [ $\Omega/\text{sq}$ ]	Measured $R_S$ before imp. [ $\Omega/\text{sq}$ ]
Implanted SOI (2/1/450 $\mu\text{m}$ )	$3.1 \times 10^{19}$	56.8	17.7	12.7	89.3
Implanted SOI (5/2/400 $\mu\text{m}$ )	$3.4 \times 10^{19}$	56.1	6.6	8.3	21.1
Double implantation	$3.1 \times 10^{19}$	56.8	7.2	9.2	38.1

The measured sheet resistances are in good agreement with the calculated resistances, hence providing a good indication on the success of the implantation step. However, this method does not provide any details on the implantation profile, which is critical in the formation of the porous silicon membranes. For this, we characterized our samples using secondary ion mass spectroscopy (SIMS) analysis. The analysis was done, with the help of the CIMPACA association, on each implanted SOI sample (figure 40a and 40b) and twice (after each implantation step) on the double implantation sample (figure 40c).

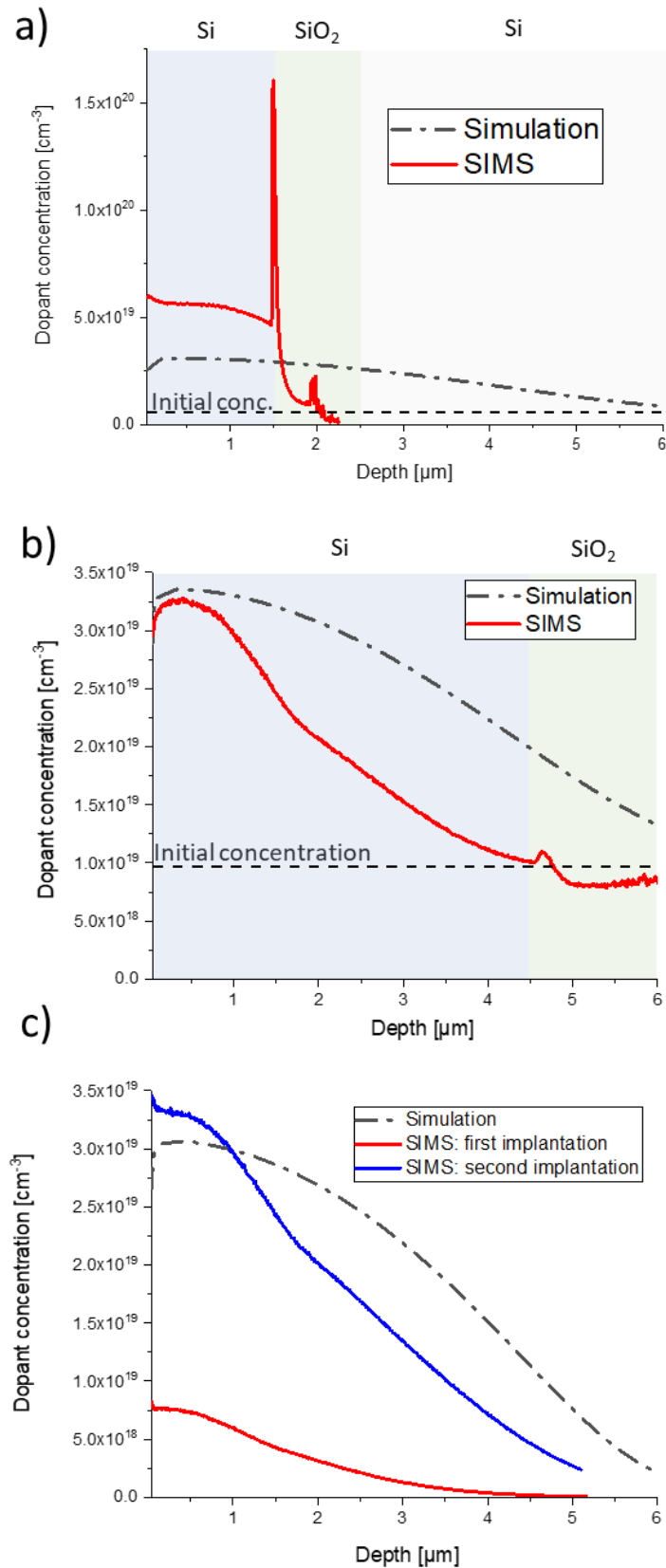


Figure 40 – Comparison of SIMS analysis and implantation simulations for (a) 2  $\mu\text{m}$  SOI, (b) 5  $\mu\text{m}$  SOI and (c) double implantation.



As mentioned before, in the simulations we did not consider the BOX layer. However, it is known that Si/SiO<sub>2</sub> interfaces play a very important role on dopants diffusion: boron tends to preferentially migrate to the Si/SiO<sub>2</sub> interface, causing a concentration peak at the interface and a ion depletion zone before that interface [38]. This is clearly seen in the SIMS profiles. Regarding the concentration levels, the 2 μm SOI shows variations from 5.8x10<sup>19</sup> cm<sup>-3</sup> on the wafer surface to 4.9x10<sup>19</sup> cm<sup>-3</sup> closer to the silicon/silicon dioxide interface. For the 5 μm SOI sample, the concentration at the surface (3.2x10<sup>19</sup> cm<sup>-3</sup>) is a bit lower than what the simulation predicted, and is as low as the initial concentration of 1.0x10<sup>19</sup> cm<sup>-3</sup> closer to the interface. This indicates that the 2 μm SOI sample is the most appropriate to implement the proposed fabrication process since 1) a bigger difference in pore morphology is expected from the larger dopant concentration difference between the implanted and non-implanted regions and 2) the implantation profile is more uniform through the thickness (this should lead to a porous membrane with better uniformity).

In the case of the double implanted layer, the SIMS profile is slightly different than the simulated one, where the surface concentration is higher (3.3x10<sup>19</sup> cm<sup>-3</sup>), and it reaches 8x10<sup>18</sup> cm<sup>-3</sup> at 3.8 μm deep.

#### **4.2.4. Characterization of diverse porous silicon elements on the same chip**

Following the parametric analysis of the implantation process through simulation and characterization, we have then fabricated porous silicon membranes using the two proposed fabrication processes with the highest implantation doses. The as-fabricated membranes were then fully characterized. The pores size was estimated using SEM images of the cross-section of porous silicon elements, and the porosity was obtained using the SLIM method, except for thin membranes where SEM image analysis was used (both techniques were previously detailed in section 1.2.).

##### **4.2.4.1. Implanted SOI process**

As expected from the SIMS characterization, the 2 μm SOI chips have shown more diversification in morphology in the porous silicon membranes than the 5 μm SOI chips. Figure 41 presents SEM images of membranes fabricated on the 2 μm SOI wafer with 1:1 HF:1-butanol electrolyte, applying a current density of 200 mA/cm<sup>2</sup> for 60 s. On this chip, we reached a pore size of around ~20 nm with a porosity of ~80% on the non-implanted membranes, and a pore size and a porosity of ~35 nm and ~85% on the implanted membranes, and we formed vertical porous silicon layers of ~7 μm with pore of ~25 nm in diameter and a porosity of ~60%.

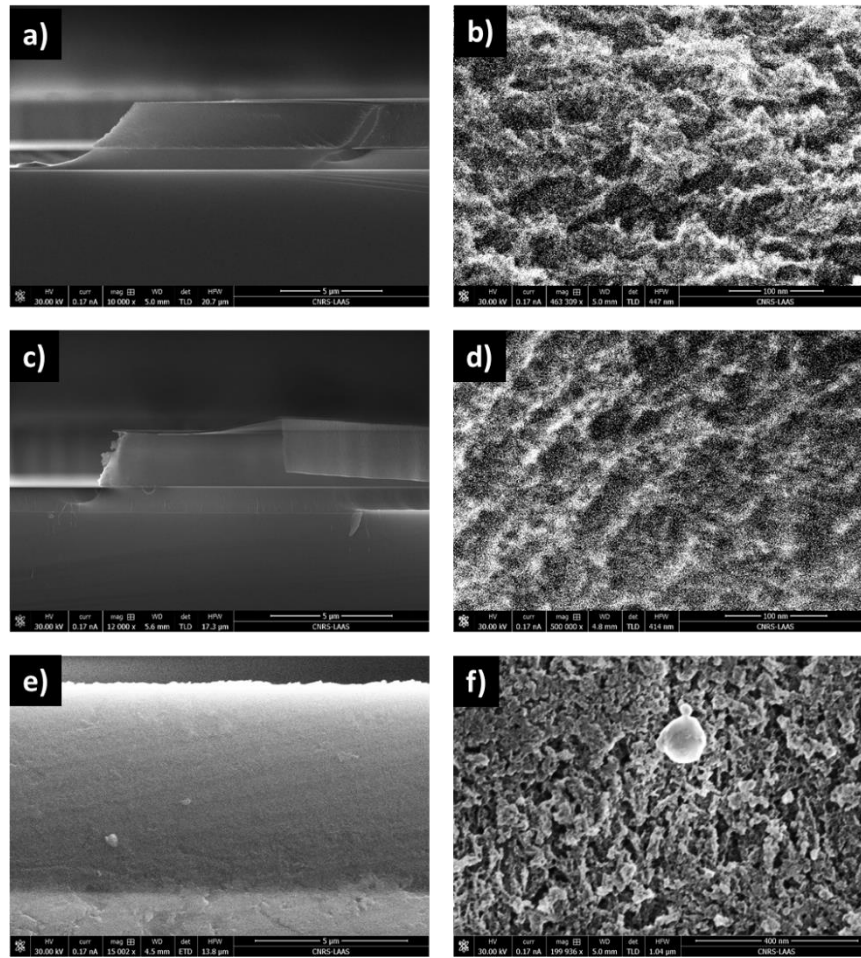


Figure 41 – SEM images of the cross-section of different porous silicon elements fabricated with a single anodization step (1:1 HF:1-butanol, 200 mA/cm<sup>2</sup>, 60 s) on a 2  $\mu$ m SOI chip. (a) and (b) show the non-implanted lateral porous silicon membrane, with pore size of  $\sim$ 20 nm and porosity  $\sim$ 75%; (c) and (d) show the implanted membrane, with pore size of  $\sim$ 35 nm and porosity  $\sim$ 85%; and (e) and (f) show the vertical porous silicon layer, with 7  $\mu$ m of depth, pore size of  $\sim$ 25 nm and porosity of  $\sim$ 60%.

Applying the same anodization recipe to a 5  $\mu$ m SOI chip (figure 42), led to  $\sim$ 30 nm pores with  $\sim$ 85% porosity on the non-implanted regions. As expected from the SIMS profile, the implanted regions display varying properties along the height of the membrane. While next to the surface, we observe  $\sim$ 45 nm pores (figure 43a), the size of the pores deeper in the membrane ( $\sim$ 35 nm), shown in figure 43b, is closer to the one of non-implanted regions (figure 42b). The average porosity of the implanted membrane is estimated to be around 90%. The formed vertical porous silicon layer is  $\sim$ 6.4  $\mu$ m thick with  $\sim$ 35 nm diameter pores and  $\sim$ 65% porosity.

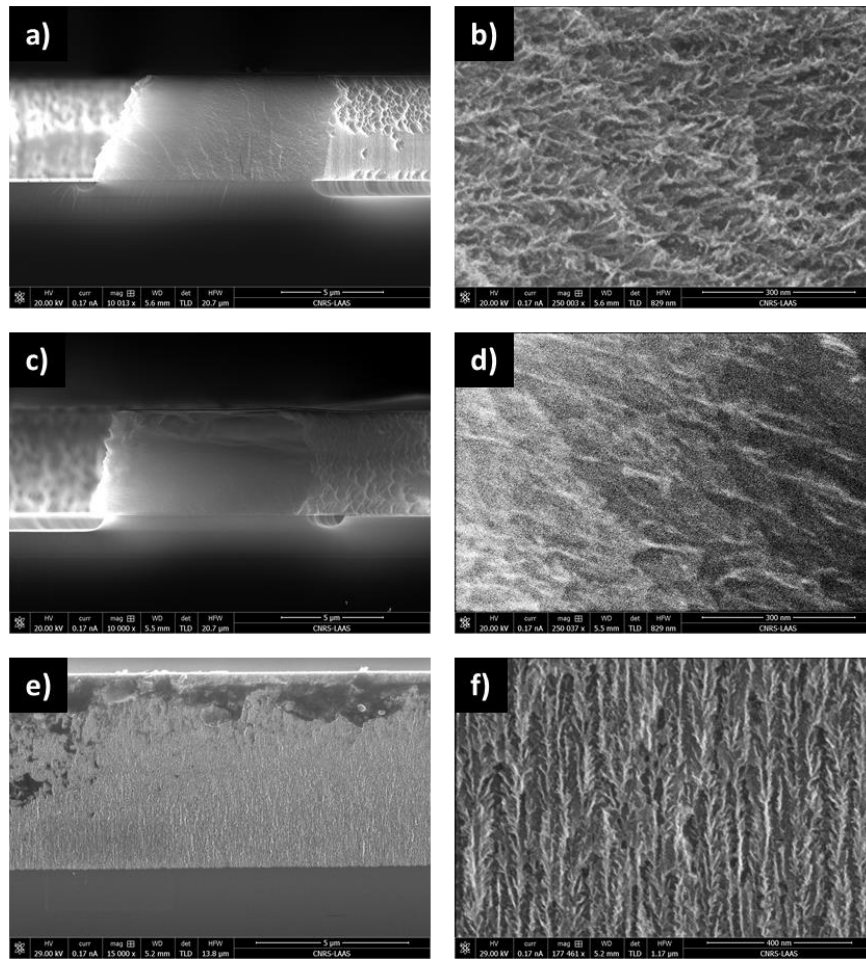


Figure 42 – SEM images of the cross-section of different porous silicon elements fabricated with a single anodization step on a 5 μm SOI chip following the implanted SOI fabrication process (1:1 HF:1-butanol, 200 mA/cm<sup>2</sup>, 60 s). (a) and (b) show the non-implanted lateral porous silicon membrane, with pore size of ~30 nm and porosity ~85%; (c) and (d) show the top region of the implanted membrane with slightly varying pore size and an average porosity of ~90%; and (e) and (f) show the vertical porous silicon layer, with 6.4 μm of depth, pore size of ~35 nm and porosity of ~65%.

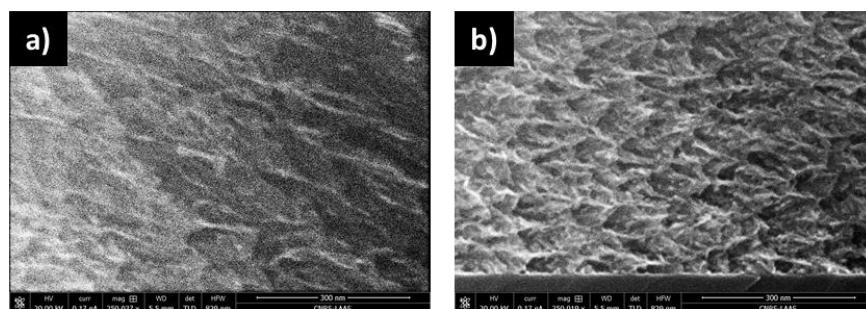


Figure 43 – SEM images of the cross-section of different regions of the same implanted lateral porous silicon membrane fabricated through the implanted SOI process using a 5 μm SOI chip (1:1 HF:1-butanol, 200 mA/cm<sup>2</sup>, 60 s). (a) is a region close to the wafer surface with pore size of ~45, while (b) is a region closer to the bottom of the membrane with pore size of ~35 nm.

Switching the electrolyte to 1:1 HF:ethanol, we were able to reach a two-fold increase in pore size (applying current density of 225 mA/cm<sup>2</sup> for 60 s) on 2 μm SOI chips (figure 44), forming ~25 nm pores with ~80% of porosity on non-implanted regions, and ~50 nm pores with ~90% of porosity on implanted regions. While 1-butanol based electrolytes have previously shown to be more interesting for reaching bigger pore size (refer to section 3.2.3), we are able to increase the variation in morphology between the membranes of different characteristics using ethanol. Also, on the same chip we formed 8.1 μm layers of vertical pore silicon with ~35 nm pore size and porosity of ~65%.

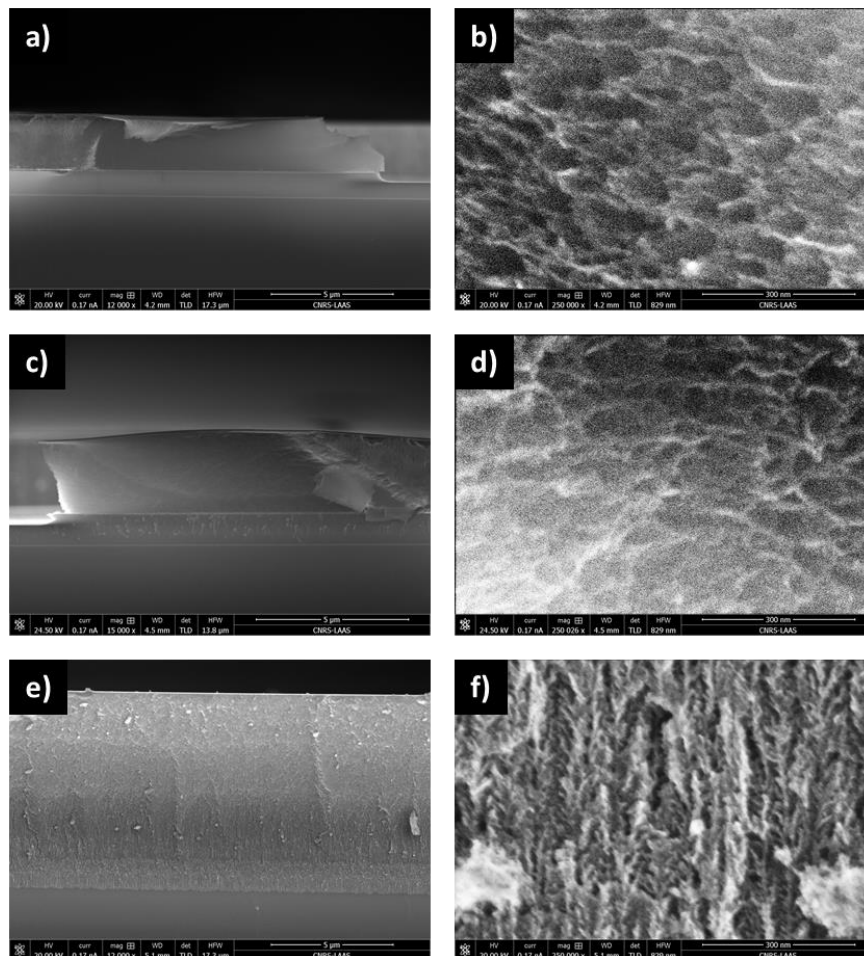


Figure 44 – SEM images of the cross-section of different porous silicon elements fabricated with a single anodization step on a 2 μm SOI chip following the implanted SOI fabrication process (1:1 HF:ethanol, 225 mA/cm<sup>2</sup>, 60 s). (a) and (b) show the non-implanted lateral porous silicon membrane, with pore size of ~25 nm and porosity of ~80%; (c) and (d) the top region of the implanted membrane, with pore size of ~50 nm and porosity of ~90%; and (e) and (f) the vertical porous silicon layer, with 8.1 μm of depth, pore size of ~35 nm and porosity of ~65%.

From this data, summarized in table 3, we have made a puzzling observation regarding the morphology of lateral porous silicon compared to standard vertical pores. Even being formed on equivalent <100> crystallographic directions, lateral

pores always present higher porosities, while keeping similar or even lower pore size, for the same parameters (it is important to remember that the vertical pores are grown on non-implanted regions). The reason behind this behavior is not yet clear, but the results shown here demonstrate the feasibility of multi-membrane fabrication with the implanted SOI process.

Table 3 – Summary of the measured pore size and porosity for both lateral porous silicon (LPSi) membranes and the vertical porous silicon (VPSi) layers for the samples fabricated using either 1-butanol (BuOH) or ethanol (EtOH) based electrolytes.

Sample	Non-implanted LPSi membrane		Implanted LPSi membrane		VPSi layer	
	Pore size [nm]	Porosity [%]	Pore size [nm]	Porosity [%]	Pore size [nm]	Porosity [%]
2 $\mu\text{m}$ SOI (BuOH)	20 $\pm$ 5	75 $\pm$ 5	35 $\pm$ 5	85 $\pm$ 5	25 $\pm$ 5	65 $\pm$ 5
5 $\mu\text{m}$ SOI (BuOH)	30 $\pm$ 5	85 $\pm$ 5	45 $\pm$ 6 35 $\pm$ 5	90 $\pm$ 5	35 $\pm$ 5	65 $\pm$ 5
2 $\mu\text{m}$ SOI (EtOH)	25 $\pm$ 6	80 $\pm$ 5	50 $\pm$ 6	90 $\pm$ 5	35 $\pm$ 6	65 $\pm$ 5

#### 4.2.4.2. Double Implantation process

Conclusions after fabricating and observing the devices using the double implantation are quite different and this process has shown significant limitations. In order to achieve more diversification in morphology between the regions of different doping levels, we have tried using various 1:1 HF:solvent recipes. However, we have been experiencing the electropolishing of regions at the base of the porous silicon membrane, mostly where the electrolyte can infiltrate under the metal layer. The outcomes are shown in figure 45, where a chip was fabricated using a 1:1 HF:ethanol electrolyte, applying 167 mA/cm<sup>2</sup> for 60 s. This resulted in very fragile membranes, and also introduced leaking points around the membrane.

Increasing the concentration of HF to 3:1 in the electrolyte reduced this effect, however, to completely avoid it we also needed to reduce the current density during anodization. Finally, using a 3:1 HF:ethanol electrolyte, and applying 133 mA/cm<sup>2</sup> of current density for 40 s, we were able to avoid electropolishing and fabricate lateral porous silicon membranes (figure 46). Nonetheless, achieving variation in pore size for this high concentration of HF is very difficult, and both implanted and non-implanted membranes displayed pore sizes and porosities of  $\sim$ 10 nm and  $\sim$ 50%, with no noticeable differences.

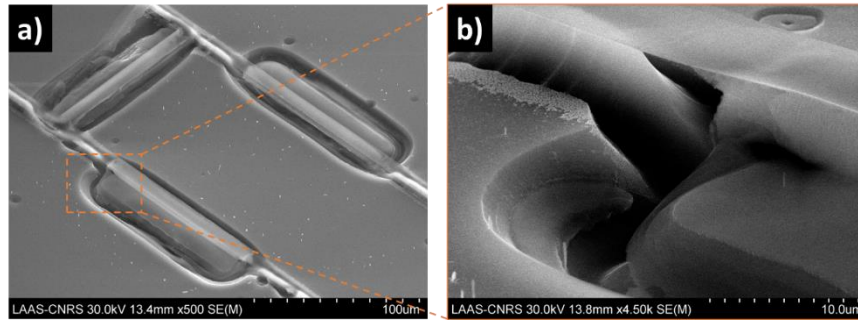


Figure 45 – SEM images of the tilted top view showing (a) a chip with 3 lateral porous silicon membranes fabricated following the double Implantation process (1:1 HF:ethanol,  $167 \text{ mA/cm}^2$ , 60 s). The two parallel membranes were implanted twice, while the third membrane was implanted only once. (b) shows the magnified view of the corners of one of the membranes, showing the region damaged by the electropolishing, with the silicon nitride layer becoming a bridge over a damaged area.

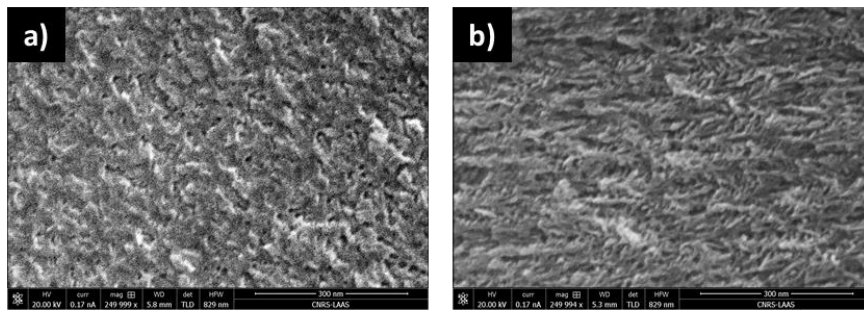


Figure 46 – SEM images of the cross-section view of different porous silicon elements fabricated with a single anodization step following the double Implantation fabrication process (3:1 HF:ethanol,  $133 \text{ mA/cm}^2$ , 40 s). (a) shows the pores on a single implanted lateral porous silicon membrane, and (b) shows the double implanted lateral porous silicon membranes with similar characteristics.

Due to the nature of the process, which is based on using the N-P junction as the etch-stop during the pores formation rather than the insulating silicon dioxide used in the SOI based process, another issue was observed in this process. Indeed, as we observed the pore orientation deeper in the substrate, we noticed that the pores would start tilting until they became vertically oriented at the bottom of the step. Figure 47 illustrates this effect. While this issue may not be a problem for filtration applications, this extra roughness under the membrane can be problematic for optical applications.

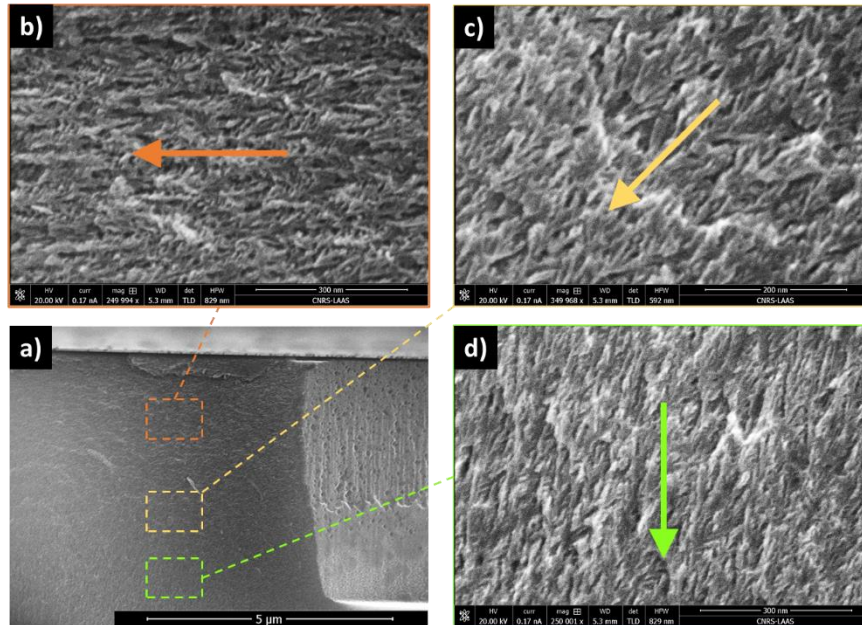


Figure 47 - SEM images of the cross-section view of different regions of the same double implanted lateral porous silicon membrane fabricated through the double implantation process (3:1 HF:1-butanol, 133 mA/cm<sup>2</sup>, 40 s). As indicated by the arrows, the magnified images (b, c and d) show how the pores propagation direction changes when we approach the bottom of the membrane.

Overall, the double implantation process raises fabrication issues not encountered in the Implanted SOI process. Besides, it is not obvious to imagine how multiple membranes with different morphologies could be fabricated through this route. Hence, the implanted SOI process, which is also much more efficient in achieving pore variation, is superior and considered to be the best option for multi-membranes lab-on-a-chip fabrication.

#### 4.2.5. Thin lateral porous silicon formation phenomenon

During the fabrication of implanted SOI chips, we observed an interesting phenomenon as high current densities were being used: this phenomenon could lead to the fabrication of very thin lateral porous silicon membranes that could be of great interest due to their reduced fluidic resistance.

A limitation of our lateral porous silicon fabrication technique is the thickness of the membranes that can be realized. While thick membrane fabrication is limited by the anodization time and the etching of the silicon dioxide layer in HF, the lower limit is set by the precision of the metal patterning step, including the photoresist application and development, and the chemical etching in aqueous baths. For this reason, it is practically difficult to envision making membranes thinner than 10  $\mu\text{m}$ .

For lateral porous silicon fabrication with the implanted SOI process, we achieve high porosities ( $\sim 90\%$ ) and  $\sim 50$  nm pore size. This means the silicon walls of the

pores are  $\sim 6$  nm thick. When increasing the current density, we can expect to decrease this thickness even more, making the material very fragile and prone to collapsing. However, we have noticed that both extremities of the step show different morphology than its middle, as if the current density was different, and two thin membranes are left standing connected by a “silicon nitride bridge” after the collapse of the middle portion.

This effect was first observed while anodizing a  $5\ \mu\text{m}$  SOI using  $400\ \text{mA}/\text{cm}^2$  for 60 s in 1:1 HF:1-butanol electrolyte. As seen in figure 48a, looking at the membrane from the top, the membrane can be divided in three parts. Using focused ion beam (FIB) etching, we were able to carve the membrane from one of its faces (figure 48b), realizing the entire middle of the membrane was gone, and the region identified by the number 2 in the figure below was actually empty: we were looking directly at the buried silicon dioxide layer through the thin silicon nitride layer. The two thin membranes had pores of  $\sim 30$  nm in size and  $\sim 60\%$  in porosity (figure 48c), with the membranes measuring  $\sim 2\ \mu\text{m}$  in thickness (figure 48d).

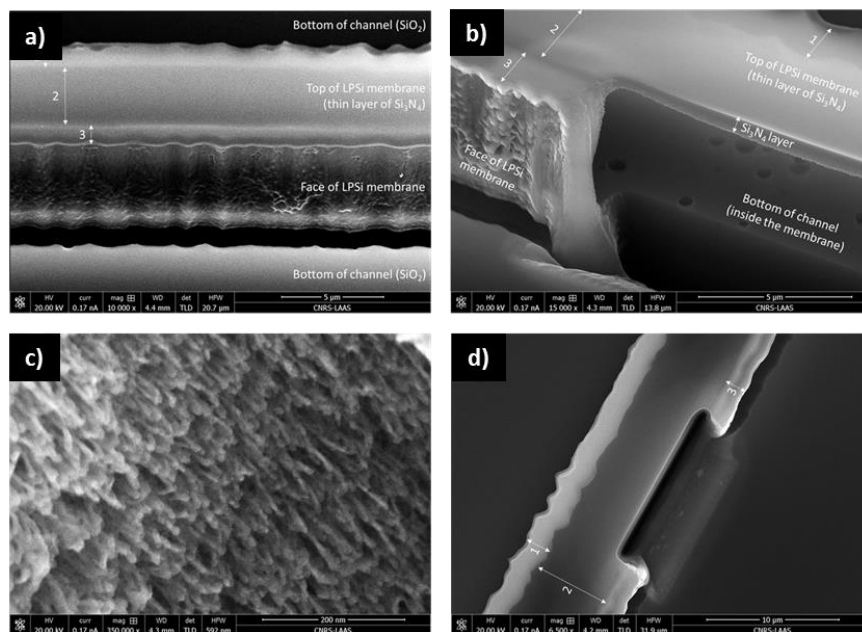


Figure 48 – SEM images of a step anodized with high current density, on a  $5\ \mu\text{m}$  SOI chip following the implanted SOI fabrication process, where the thin membranes phenomenon happened. (a) Is a general inclined top view of the step, showing the different layers; (b) shows a closer view of the step after part of it was FIB etched, revealing that the inside of the membrane is empty; (c) shows the  $\sim 30$  nm pores on the thin membranes; and (d) is a general top view of the step where the two  $2\ \mu\text{m}$  thin lateral porous silicon membranes are well defined.

Reducing the current density allowed us to fabricate those thin membranes on the implanted step whilst we fabricated a standard  $10\ \mu\text{m}$  thick porous silicon membrane on the non-implanted step. In figure 49, another  $5\ \mu\text{m}$  SOI chip is shown,



anodized with the same recipe as before, but with a current density of  $350 \text{ mA/cm}^2$ . The non-implanted membrane (figure 49a and b) had  $\sim 30 \text{ nm}$  pores with  $\sim 60\%$  in porosity formed all over the  $10 \mu\text{m}$  thickness of the step. The implanted step (figure 49c and d) was divided in two  $< 2 \mu\text{m}$  thick thin membranes, with pores of around  $\sim 15 \text{ nm}$  and  $\sim 40\%$  in porosity. A standard vertical porous silicon layer with  $6.7 \mu\text{m}$  in depth, pores of  $\sim 40 \text{ nm}$  and porosity of  $\sim 60\%$  was also fabricated on the same chip (figure 49e and f).

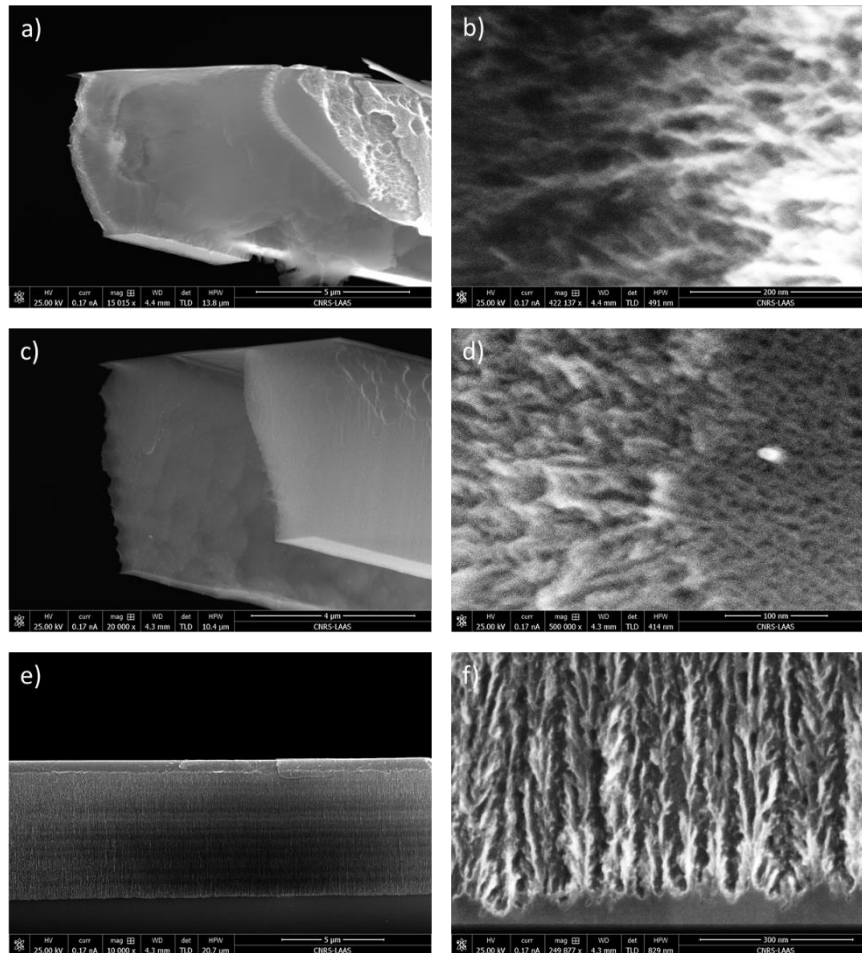


Figure 49 – SEM images of  $5 \mu\text{m}$  chip anodized with  $350 \text{ mA/cm}^2$  of current density, following the implanted SOI fabrication process, where the thin membranes phenomenon happened only on the implanted region. (a) Cross-section view of the non-implanted step; (b) closer cross-section view of the non-implanted step showing the  $\sim 30 \text{ nm}$  pores with  $\sim 60\%$  of porosity; (c) cross-section view of the implanted step, where the thin membranes formation phenomenon happened, creating two membranes of under  $2 \mu\text{m}$  in thickness; (d) closer view of the  $\sim 15 \text{ nm}$  pores and  $\sim 40\%$  of porosity formed on the thin membranes; (e) cross-section view of the  $6.7 \mu\text{m}$  depth vertical pores silicon layer formed in the same chip; and (f) the closer view of the vertical pores with  $\sim 40 \text{ nm}$  in size and  $\sim 60\%$  in porosity.

#### 4.3. Proposed alternative for the fabrication of membranes with macropores and low porosity

The last section demonstrates that despite the study conducted onto vertical porous silicon membranes to increase the pore size, useful for biosensing applications, we could not simply apply the same recipe to our process because it resulted in membrane collapsing. Here, we propose a new approach that is in its early stages of development but that could possibly address this limitation, even if it would probably increase the fabrication complexity of the final device.

This work was conducted in collaboration with Dr. David Cardador Maza from the group of Prof. Angel Rodriguez at the Polytechnic University of Catalonia (UPC). Our proposed method consists in fabricating multi-directional connected pores in silicon through anodization, thermal oxidation and silicon dioxide etching. This method is based on the process for fabricating modulated macropores (figure 50) developed at UPC [39,40], which function as photonic crystals [41].

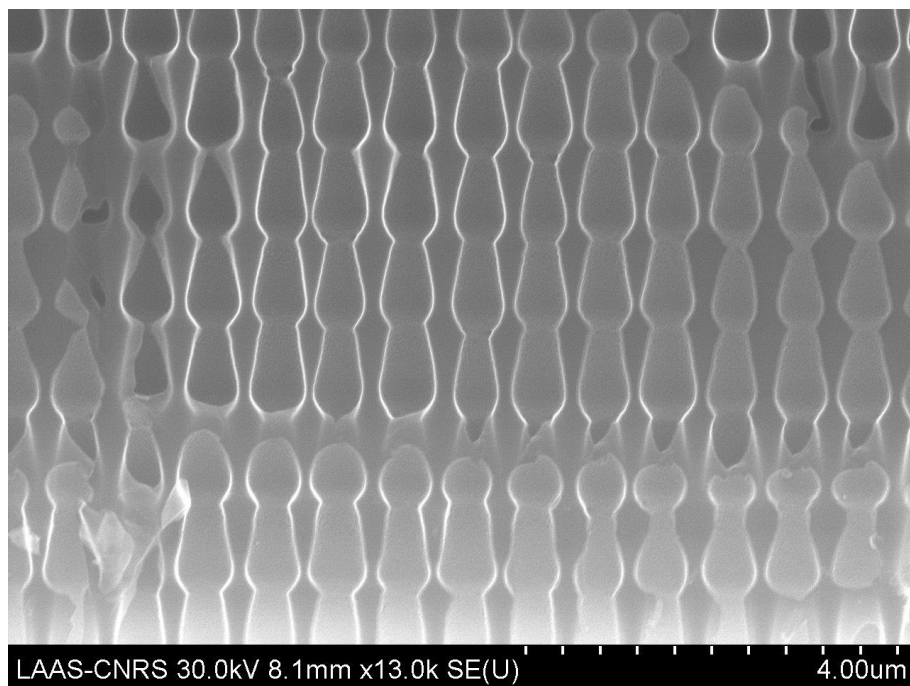


Figure 50 – SEM image of porous silicon-based photonic crystals developed at UPC.

By applying a multi-step thermal oxidation process followed by the silicon oxide etching in HF, we were able to break the walls separating the pores selectively where pores are thicker (and pore walls thinner). This resulted in holes connecting the pores in the horizontal direction. We managed to fabricate a network of macropores with average size between 200 and 300 nm, depending on the oxidation process, connected both vertically and horizontally (figure 51).

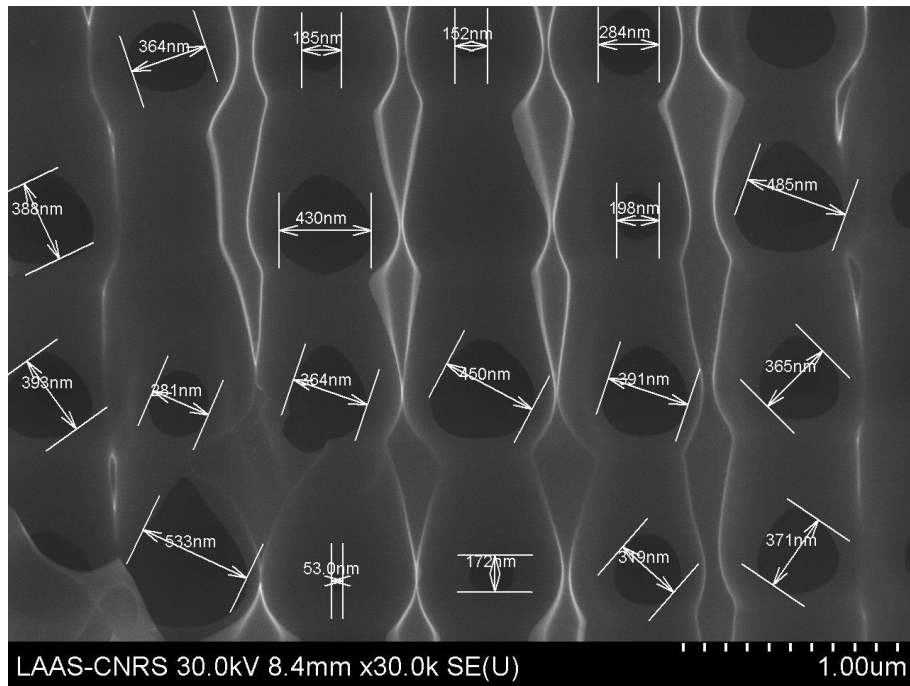


Figure 51 – SEM image of the network of pores connected both vertically and horizontally. Formed after 50 minutes in oxidation at 900°C in the presence of air.

The complex nature of the fabrication of the modulated pores is the notable drawback of this technique, because it is not trivial to fabricate them in selected zones of a microfluidic chip, which means that it is hard to envision the monolithic integration of membranes with various characteristics. Still, this technique could also be interesting for other microfluidic application e.g. efficient passive pumps, but it needs further development.

## 5. Conclusion

In this chapter, we went through the mechanics behind the fabrication of porous silicon, for both lateral and vertical pores. We have investigated different approaches to achieve the fabrication of an integrated chip with different porous silicon elements: either the use of sequential anodization steps or through the manipulation of the local dopant concentration by ion implantation to create membranes of various morphology in a single anodization step (with two processes envisioned: one relying on the use of a SOI substrate, the other one calling for two implantation steps performed on a conventional wafer).

While the process based on sequential anodization steps showed complications that would require further addressing to become viable, we were able to achieve the fabrication of diverse porous silicon elements through the use of the implanted SOI technique. The double Implantation process was shown to impose limitations to the anodization step, considerably reducing the variation in morphology of the diverse lateral porous silicon membranes fabricated.

With the goal of fabricating bigger pores on lateral porous silicon membranes, by increasing current density and changing the solvent for anodization, we have observed that our processes were limited due to the collapse of membranes with high porosity. Surprisingly, this resulted in the fabrication of two thin lateral porous silicon membranes that could be useful to decrease the fluidic resistance of such membranes. On the other hand, we have also imagined an alternative process that could tackle the issue of the need of membranes with bigger pore size (macropores) for biosensing: this alternative technique, which is still in its early development stage, is based on the fabrication of multi-directional connected macropores.

The next step of this work, which will be presented in the following chapter, is to design and use the fabrication techniques presented here to fabricate a porous silicon-based lab-on-a-chip for bioanalysis and to discuss the implementation of the various steps involved in the analysis of biological samples.

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## **Chapter 3. Microfluidic chip integrating multiple porous silicon membranes: preliminary results**

### **1. Introduction**

In the first chapter of this manuscript, we have presented the two tasks involved in the biosensing process for the detection of biomarkers: namely sample preparation (separation, preconcentration) and sample analysis. We have argued that implementing both stages on a single lab-on-a-chip is a difficult task and we have also inferred that porous silicon membranes are excellent candidates to this aim.

In the second chapter, we have presented various fabrication approaches for the integration of multiple membranes on a same chip, with the implanted SOI technique succeeding in demonstrating the possibility to tune the membrane characteristics, a requirement for implementing the various steps involved in analytical processes, i.e. filtration, separation and biosensing.

The aim of this chapter is to develop and fabricate, through the implanted SOI technique, a monolithic integrated lab-on-a-chip with multiple porous silicon membranes designed to carry out sample preparation and biosensing. Following the device conception, we will present preliminary experimental results and studies to validate and further advance its use for the target applications.

### **2. Implementing analytical processes onto a single chip**

As strongly emphasized along this work, the on-chip integration of sample preparation (i.e. sample separation and sample preconcentration) and biosensing steps is crucial as we target point-of-care applications. We showed in chapter 1 that lateral porous silicon membranes can be used for these different steps: i) it can be used as a filter membrane for size-based separation; ii) it is capable of doing sample preconcentration through ion concentration polarization (ICP), due to its ion-selectivity properties which allows selective charge transport-based techniques; and iii) it has tunable optical characteristics, which allows its use as an optical transducer and as a potential tool for optical biosensing. The steps a lateral porous silicon-based lab-on-a-chip would require to achieve is, then, represented bellow in figure 1.

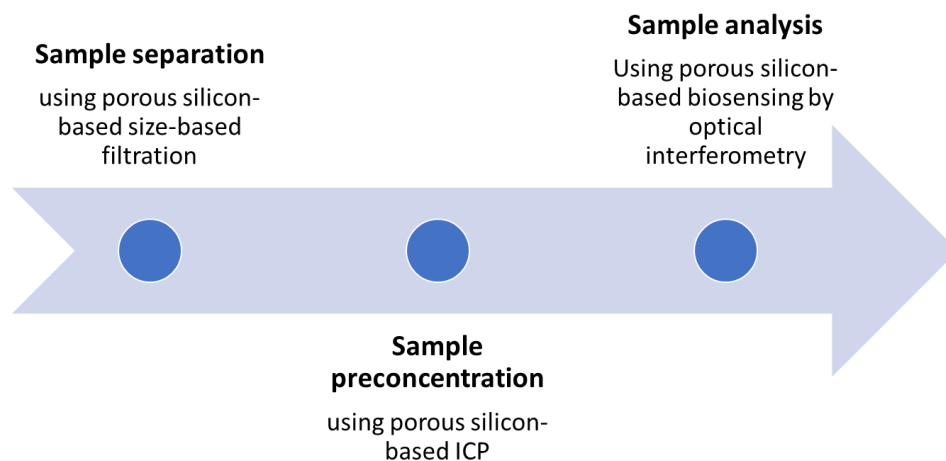


Figure 1 – Schematic diagram of the analysis process to be taken in the porous silicon-based LOC.

As a proof-of-concept to demonstrate the use of our fabrication techniques to fabricate a monolithically integrated lab-on-a-chip, we have designed a chip that can do both sample preconcentration through ICP and optical interferometry.

Before getting into the lab-on-a-chip design, we have to first better understand the mechanics of the target applications of each porous silicon element, in order to properly implement them into the chip design.

### 2.1. Ion concentration polarization for sample concentration

Concentration polarization is the increase or decrease of a specific component at the boundary layer close to a membrane surface due to the selective transport through said membrane [1]. As briefly explained in chapter 1, in the particular case of ICP, the selective transport through an ion-selective nanoporous membrane or nanochannel connecting two microfluidics compartments is charge-based. This generates an electrokinetic phenomenon that results in the accumulation of charged species in one compartment (ion enrichment) and ion depletion in the other [2].

To accomplish the electrokinetic effects on an ICP device, a voltage is applied across a perm-selective nanojunction, the counterions pass through the membrane, while the co-ions are driven away, decreasing the concentration of both near the nanojunction on one side of the junction (ion depletion zone), while increasing the concentration of counterions on the other side (ion enrichment zone).

In regard to the design of the preconcentrator, three configurations have been considered in the literature, and are to be preferred depending on the microfluidic application, microfluidic chip design, and fabrication limitations. The single-channel

configuration (SC, figure 2a) presents a microchannel incorporating a flow-through single nanojunction. Dual and triple-channel configurations (DC, TC, figure 2b and 2c) are based on applying a voltage difference across a primary microchannel filled with the sample solution; and grounded (GND) secondary channels, filled with a buffer solution, connected by a nanojunction to the sample channel. While the DC configuration uses one secondary microchannel and one nanojunction, the TC configuration consists of two secondary microchannels and two nanojunctions.

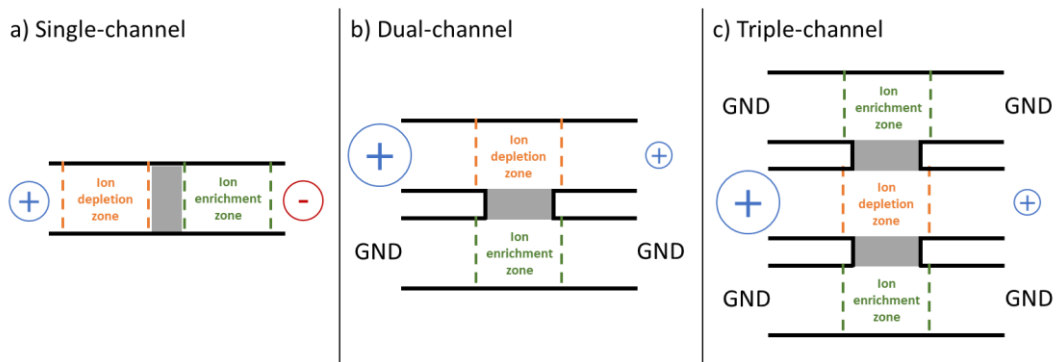


Figure 2 – Schematic representation of cation perm-selectivity based ICP designs based on number of microchannels and nanojunctions. Negative signal indicates the cathodic compartment, positive signal the anodic compartment, and GND the grounded channels. (a) Single-channel: one primary channel divided by a nanojunction; (b) dual-channel: one primary and one secondary channels, connected by a nanojunction; and (c) triple-channel: one primary channel connected to two secondary channels.

The voltage difference applied in the primary channel in DC and TC preconcentrators creates a tangential electric field, generating an electroosmosis flow through the microchannel to transport the sample molecules into the ion depletion zone, where they are trapped by the counter-flow focusing mechanism. As the electroosmosis flow is not applied through the nanojunction, when compared to SC, both DC and TC enables higher flow for faster preconcentration. TC preconcentrators provide an even more stable and consistent performance due to the generated symmetric and enhanced depletion zone [3,4].

## 2.2. Optical interferometry for biosensing

As introduced in the previous chapters, biosensing through optical interferometry is based on the analysis of the interference spectra of a biofunctionalized multi thin-layer structure. The transducers can present two configurations: flow-over and flow-through. As the names suggest, in the flow-over configuration (figure 3a), the fluid flows over the surface of the transducer, while in the flow-through configuration (figure 3b), the fluid goes through the transducer.

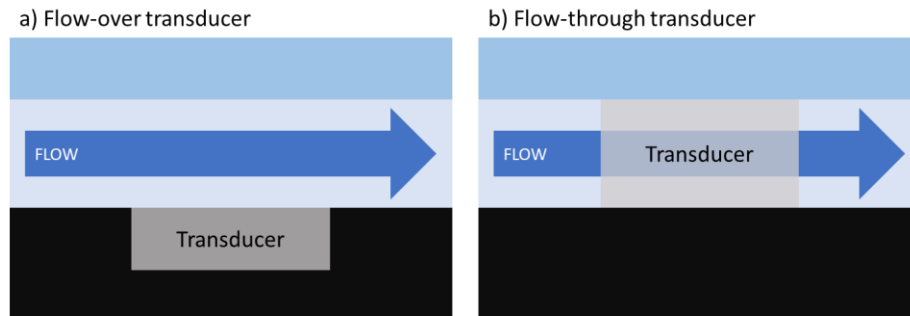


Figure 3 – Schematic representation of a (a) flow-over transducer fabricated on the bottom of a planar microfluidic device, and a (b) flow-through transducer fabricated inside the microchannel.

While the flow-over configuration for porous silicon-based transducer is by far the most popular approach for biosensing [5], both theoretical [6] and experimental [7,8] studies have shown a considerable improvement in device sensitivity due to a more efficient convective transport in the porous membrane. However, porous silicon-based flow-through transducers have not been adapted to planar microfluidic devices yet, a limitation that our lateral porous silicon membranes allow us to easily tackle.

### 2.3. Device design

With monolithic integrated fabrication processes, we have few microfluidic design limitations for our device, one of which is still the membrane dimensions: we can thus properly position the elements that compose each analytical stage.

We have designed each chip with four inlets/outlets (with 1 mm in diameter) located in a way to form a square shape with 7 mm long edges, in order to fit in our already produced sample holders for microfluidic experiments (shown in figure 8c and 8d). There are also two circles (2 mm in diameter) in which we etch the top layers of the SOI wafers until we reach the bottom silicon layer. Those circles are used to better control the current density during anodization by offering a relatively large area ( $\sim 0.06 \text{ cm}^2$ ) when compared to the membrane areas where the lateral porous silicon is to be formed ( $\sim 10^{-6} \text{ cm}^2$ ), allowing us to apply higher absolute current values (in the order of 10 mA) to reach the desired current densities (between 100 and 400 mA/cm<sup>2</sup>).

Among the 18 chips fabricated on a single 100 mm wafer, we present various microfluidic configurations to evaluate and test the influence of different design choices in the performance of the different functions for the lab-on-a-chip applications. The different designs contain three parallel microchannels that form a 45° angle with the (100) wafer flat so the lateral pores are formed in the <100> crystallographic direction. These three channels form a triple channel preconcentrator. Each secondary channel has only one inlet, since they do not

require any fluid flow for operation, allowing us to keep the chips compatible with our 4 entries sample holders (figure 4b). Both secondary microchannels are connected to the primary microchannel by 10  $\mu\text{m}$  thick lateral porous silicon membranes, located few micrometers before the porous silicon element to be used for molecular analysis (figure 4c and 4d).

The width of the main microchannel and the length of the membranes to be used for ICP can have direct impact on the preconcentration performance. For this reason, we have designed four configurations to be able to study this impact in the future: i) 20  $\mu\text{m}$  wide channel with 20  $\mu\text{m}$  long membranes; ii) 20  $\mu\text{m}$  channel with 100  $\mu\text{m}$  long membranes; iii) 50  $\mu\text{m}$  channel with 50  $\mu\text{m}$  long membranes; and iv) 100  $\mu\text{m}$  channel with 100  $\mu\text{m}$  long membranes. A chip with a single membrane was also designed (20  $\mu\text{m}$  channel with 20  $\mu\text{m}$  long membrane) in order to study the improvement of TC ICP over DC ICP. These different configurations are also compatible with the analysis of typical finger-pricked volumes ( $\sim 10 \mu\text{l}$ ).

As discussed in the previous chapter, our implanted SOI fabrication technique allows us to form both lateral porous silicon membranes and vertical porous silicon layers (on the bottom of the microfluidic channel). In order to test both flow-over and flow-through configurations during the analysis step, we designed chips with both forms of porous silicon interferometers (figure 4c and 4d).

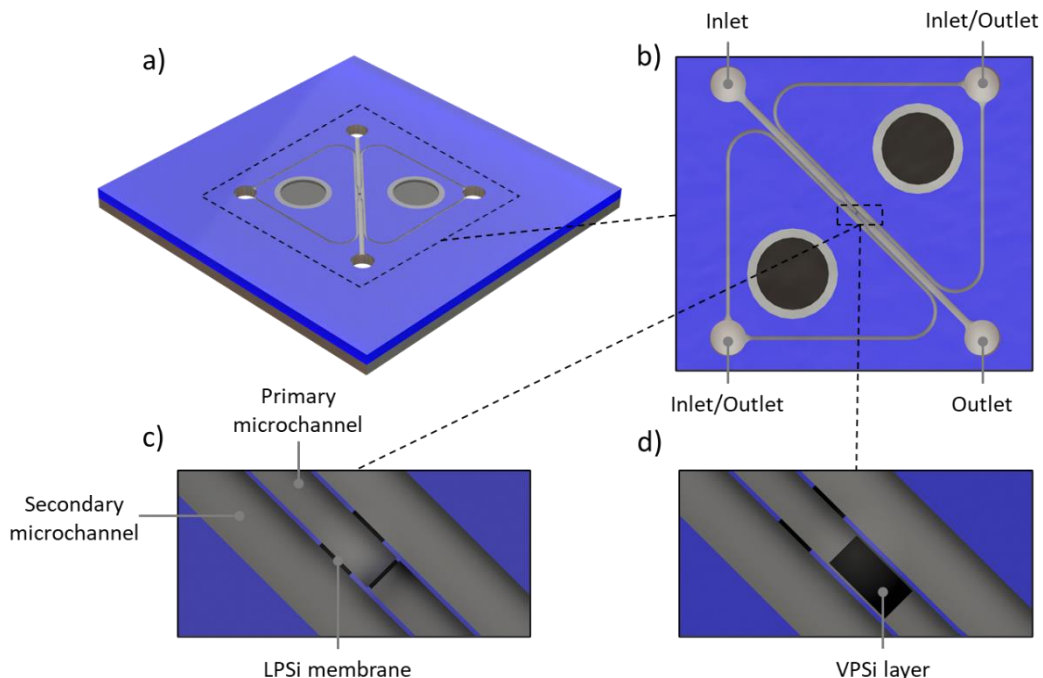


Figure 4 – CAD images showing the (a) isometric view of the microchip, (b) top view of the complete microfluidic design, (c) zoomed in top view of the design using of three lateral porous silicon membranes (in black), and (d) zoomed in top view of the design replacing the third lateral porous silicon membranes with a vertical porous silicon layer.

Regarding the dimensions of the transducer element, they are mostly limited by the width of the main microchannel. To work with the dimensions presented previously, we designed lateral porous silicon transducers of 15, 45 and 95  $\mu\text{m}$  in length, and vertical porous silicon layers of  $90 \times 10$ ,  $90 \times 40$  and  $90 \times 90 \mu\text{m}^2$  in area.

#### 2.4. Device fabrication

We designed a set of photolithography masks to implement the implanted SOI process on a 4" SOI wafer and fabricate 18 square chips of  $16 \times 16 \text{ mm}^2$  integrating an ICP-based sample concentration stage and an interferometer-based biosensor (figure 5 and 6 show the masks designed in the software CleWin 4.0).

In the implantation step, we only exposed the membranes to be used for ICP and not the one used for transduction, in order to guarantee the uniformity in pore morphology through the thickness of the transducing membrane and avoid affecting the optical results (figure 7).

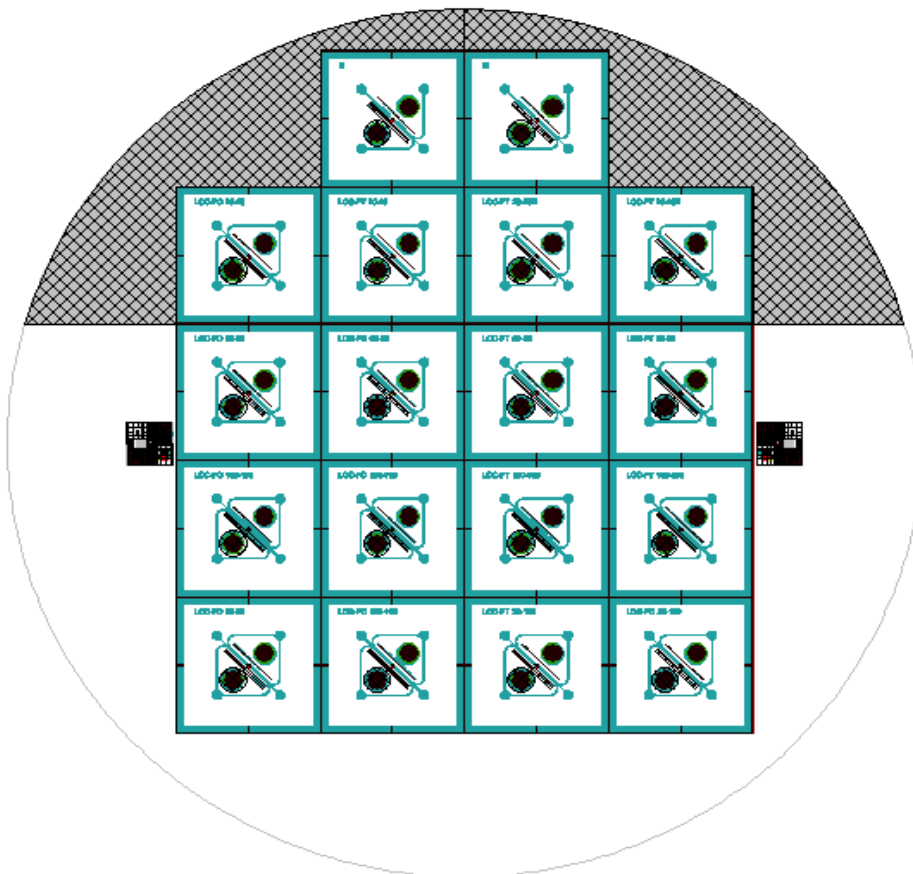


Figure 5 – Masks designed to fabricate 18  $16 \times 16 \text{ mm}^2$  square chips using the implanted SOI fabrication process on 4" SOI wafers

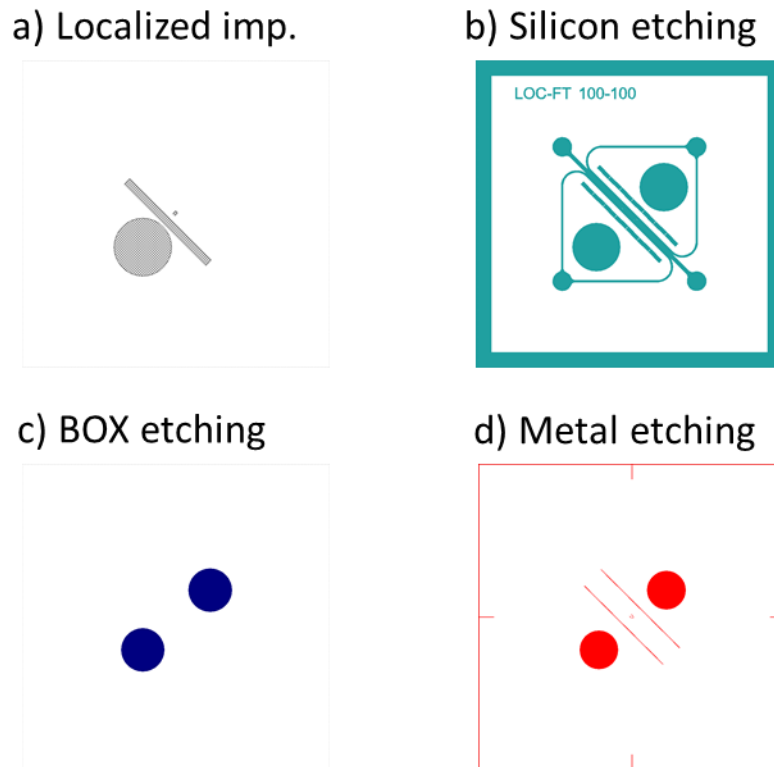


Figure 6 – Zoom on a single chip of all 4 masks layers used for localized implantation (a), for silicon etching to form the microchannels (b), for buried silicon oxide etching to reach the bottom silicon layer (c), and for patterning the metal layer (d).

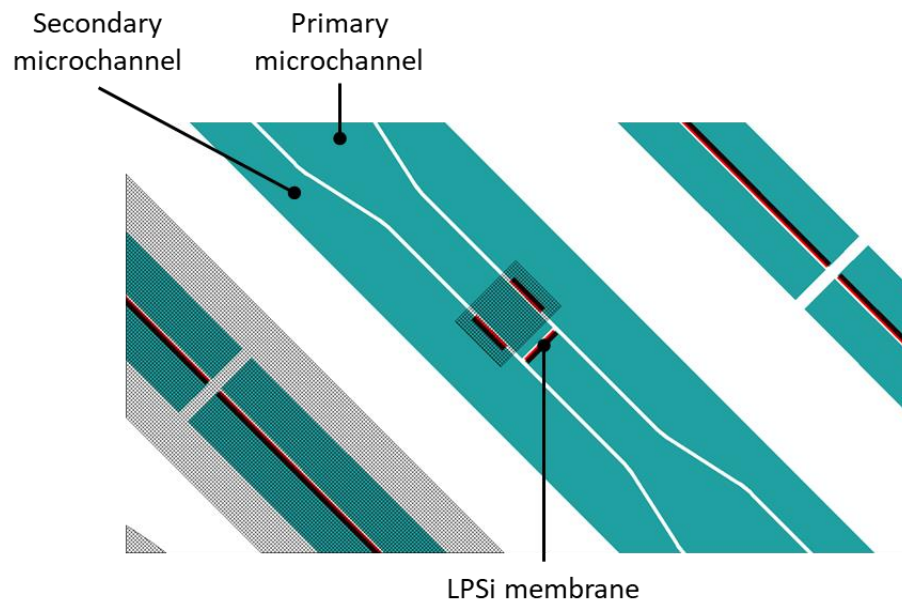


Figure 7 – Zoomed in picture on the masks showing the region that received implantation (in black grid). The long porous silicon membranes fabricated on the sides, outside the microfluidic system, are to be used for characterization.

We successfully fabricated samples on 2  $\mu\text{m}$  SOI wafers following the implanted SOI fabrication process (as seen in figure 8, where we present the wafer before and



after the metallization step). We have implanted selected regions to enable different levels of doping that would lead to membranes with different morphologies.

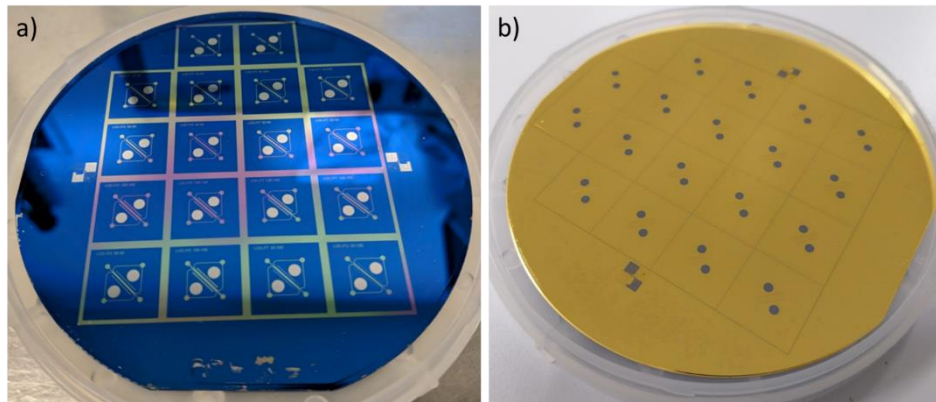


Figure 8 – Wafer in process during two different steps. (a) Before the metallization step, and (b) after the selective wet etching of the metallization layer.

After dicing the wafers and anodizing the chips, we produced several chips (figure 9, and figure 10a and 10b), compatible with the sample holder used for microfluidic experiments (figure 10c and 10d).

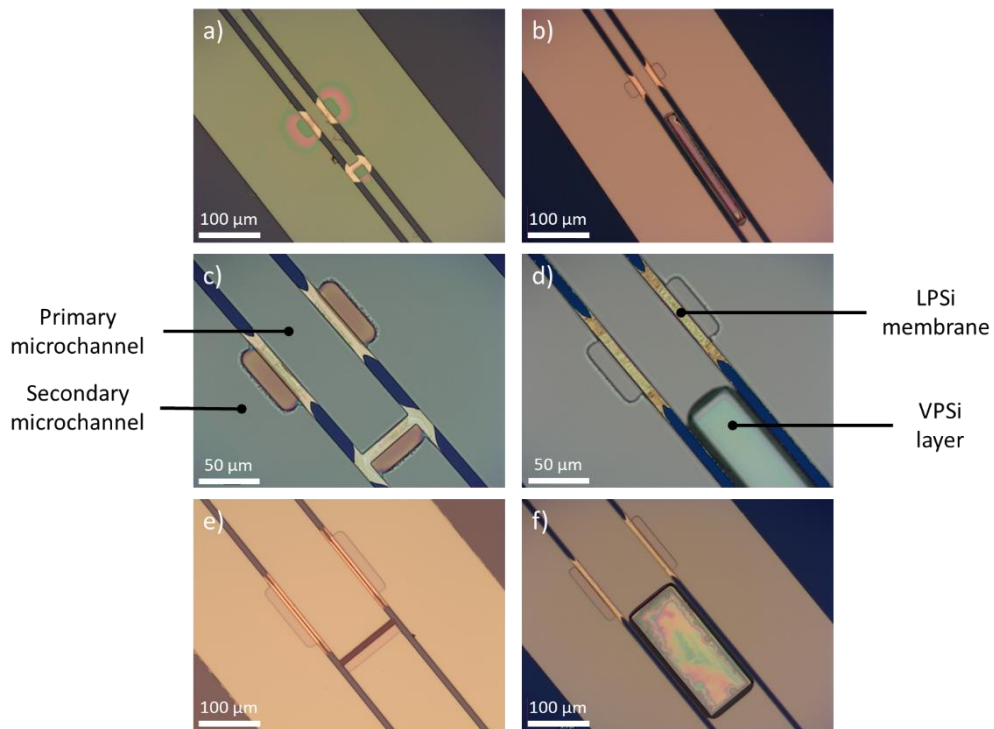


Figure 9 – Optical microscopy pictures of the different device designs fabricated on SOI chips with different primary channel widths: (a) and (b) 20  $\mu\text{m}$ , (c) and (d) 50  $\mu\text{m}$ , (e) and (f) 100  $\mu\text{m}$ . The pictures on the left show devices with flow-through interferometers, the one on the left present devices with flow-over interferometers.

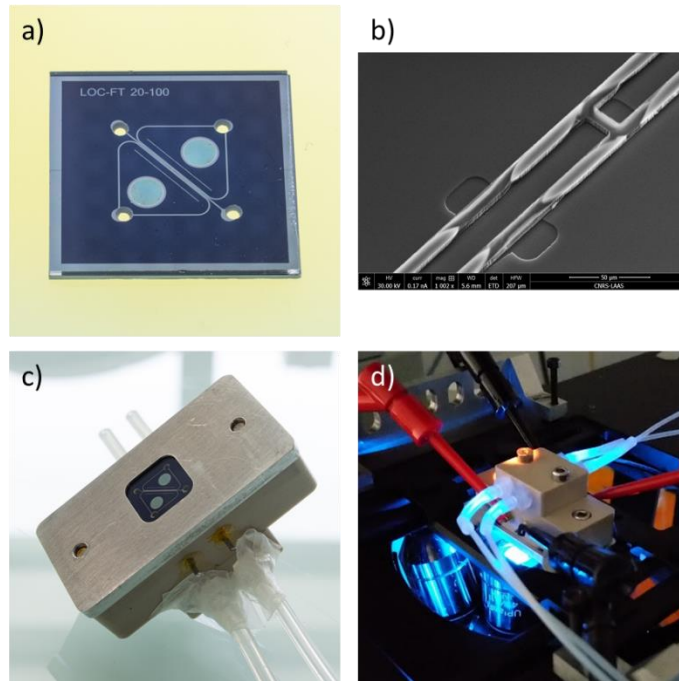


Figure 10 – (a) Photo of a fabricated device; (b) SEM image of the microchannels and the multiple lateral porous silicon membranes; (c) photo of the device in the microfluidic sample holder; and (d) sample holder on the fluorescence microscope during an ICP experiment.

With the intention of testing the chips for microfluidic applications, we filled the microchannels with a solution of  $10 \mu\text{M}$  of fluorescein (hydrodynamic radius of  $\sim 1 \text{ nm}$ , Sigma Aldrich) in PBS 1X buffer ( $\sim 150 \text{ mM}$ , pH 7.4, Sigma Aldrich), after exposing each chip to oxygen plasma to increase its wettability. To flow the solution in the microchannels, we applied  $\sim 0.2 \text{ Bar}$  at the sample's inlets using a pressure controller (MFCS-8C, Fluigent). Then, we observed the samples by means of an IX70 Olympus inverted epifluorescence microscope equipped with an EMCCD camera (Andor) and a light source (Lumencore).

The resulting pictures in figure 11 show that both samples with flow-through and flow-over interferometers were completely filled by the fluorescent solution. We can see some micro air bubbles stuck in the vicinity of the membranes, but this should not be an issue since such bubbles should dissolved upon proper degassing the solution before the injection.

Those results validate the use of the implanted SOI fabrication method to fabricate lab-on-chips integrating multiple porous silicon membranes to be used for the various steps of sample analysis. In the following sections of this chapter, we will present studies and preliminary experiments we have carried out to show how the on-chip biosensing function can be implemented.

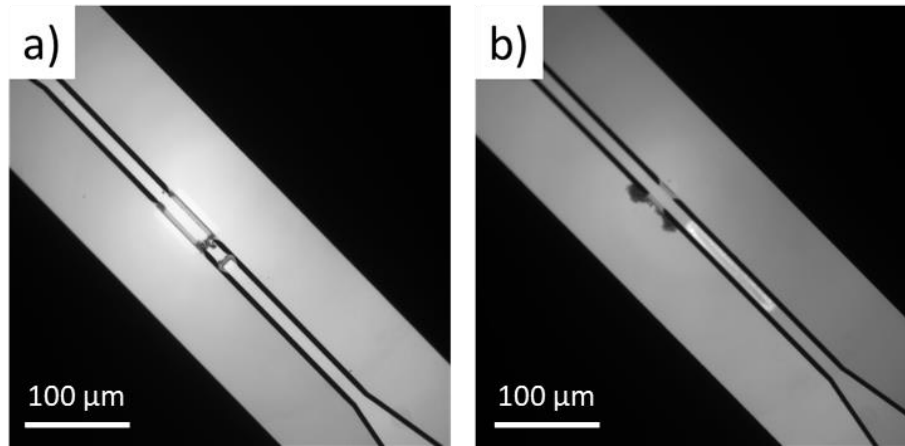


Figure 11 – Fluorescence microscope images of a (a) flow-through and a (b) flow-over design filled with 10  $\mu\text{M}$  of fluorescein in PBS 1X buffer.

### 3. Preliminary results and studies on lateral porous silicon optical interferometry

#### 3.1. Lateral porous silicon interferometry: proof-of-concept

In his thesis work, defended in 2016, Yingning He already demonstrated the feasibility of using lateral porous silicon as an interferometer [9]. To this aim, he carried out optical measurements on lateral porous silicon membrane fabricated with the implantation technique (porosity of  $\sim 40\%$ ,  $\sim 4 \mu\text{m}$  in thickness) filled with different solvents (water, acetone and ethanol). The resulting reflectance spectra are presented in figure 12a.

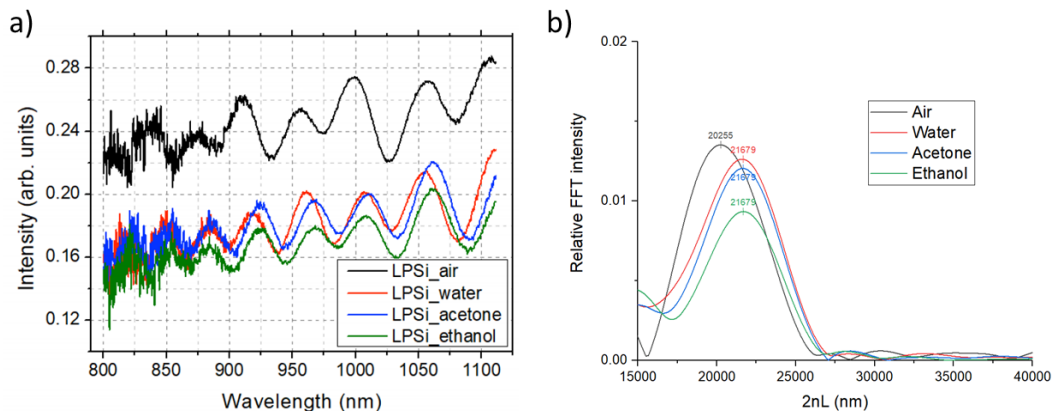


Figure 12 – (a) Experimental reflectance spectra of the three tested solvents (water, acetone and ethanol) filling the lateral porous silicon membrane. The plot named air represents an empty and dry porous silicon. (b) RIFTS analysis of the spectra. Adapted from [10].

We estimated the sensitivity of the implanted lateral porous silicon interferometer from the experimental shift of the maximum peak at 910.1 nm. We observed a 51.3 nm shift of the interference spectrum after filling the chip with water ( $n_{\text{water}} = 1.328$ , compared to  $n_{\text{air}} = 1$ ). This shift corresponds to a sensitivity of  $\Delta\lambda/\Delta n_{\text{fill}} \approx 156$

nm/RIU (refractive index unit), which is in the same range as the sensitivity of other vertical porous silicon interferometers reported in the literature, *e.g.* 78 nm/RIU [11], 140 nm/RIU [12] and up to 425 nm/RIU [13]. Since the spectral resolution of our apparatus ( $4 \text{ cm}^{-1}$ ) translates into a 0.3 nm wavelength resolution at 900 nm, the corresponding limit of detection is estimated to be  $2 \times 10^{-3}$  RIU. This limit of detection could be lowered to  $6 \times 10^{-4}$  RIU using an improved set-up with 0.1 nm resolution [14]. Although this value is significantly lower than for surface plasmon resonance sensors, porous silicon sensors display high surface area that could offer other advantages for biosensing [15].

Next, reflectometric interference Fourier transform spectroscopy (RIFTS, a technique described in chapter 2) analysis was performed since it is usually used to obtain the effective optical thickness (EOT) and estimate the refractive index of the pore filling. However, as can be seen on the plot in figure 12b, RIFTS did not prove to be very sensitive in the measurement of the EOT, and it was not possible to differentiate the refractive index of each solvent with this method ( $n_{\text{water}} = 1.328$ ,  $n_{\text{acetone}} = 1.354$ , and  $n_{\text{ethanol}} = 1.357$ ). This low resolution of the RIFTS analysis is due to the wavelength range the technique was applied to (over 800 nm), as well as to the overwhelming noise that already starts at under 900 nm and gets even worse under 800 nm. Applying RIFTS to the  $>800$  nm data results in a resolution of 158 nm in EOT, which is equivalent to a variation of  $\sim 0.05$  of refractive index of the filling, explaining why we cannot differentiate the various solvents. Applying FFT to a segmented signal has a direct impact to its spectral resolution: as we reduce the number of data samples in a segment, averaging between data points is required, resulting in a higher distance between the created frequency bins, decreasing the spectral resolution [16]. Being able to increase the length of the segment would result in higher FFT resolution.

Following the fabrication of lateral porous silicon membranes via different routes, we are now aiming to compare how these configurations perform from an interferometer point of view.

### **3.2. Comparison between different configurations of porous silicon interferometers**

As described in chapter 2, we have fabricated samples following the implanted SOI technique with lateral porous silicon thickness of 2  $\mu\text{m}$  (the samples analyzed were fabricated with 1:1 HF:1-butanol electrolyte, applying 200  $\text{mA}/\text{cm}^2$  for 60 s, and the membranes observed were non-implanted, meaning the pores are  $\sim 25$  nm in size, with porosity around  $\sim 80\%$ ). We also measured the reflectance of the in-channel vertical porous silicon layer (as shown in figure 4d). Finally, we fabricated a standard vertical porous silicon layer (3:1 HF:ethanol, 160  $\text{mA}/\text{cm}^2$ , 40 s, achieving  $\sim 15$  nm pores,  $\sim 55\%$  porosity and  $\sim 6$   $\mu\text{m}$  thickness) to be used as a reference.

All the optical experiments were carried on a VERTEX 70 FTIR (Bruker Optics), equipped with a tungsten light source, a quartz beam splitter and a Si-diode detector (SiD 510), able to cover the spectral range between 500 and 1100 nm. The spectrometer was connected to a HYPERION microscope equipped with a 36x objective (with incident angle of around 8°) and an adjustable rectangular observation window (maximum size of 277x277 μm<sup>2</sup>). The spectroscopy software OPUS (Bruker Optics) was used to control the equipment and acquire the data.

The spectra for all samples (using the same observation window of 90x10 μm<sup>2</sup>), including the lateral porous silicon membrane fabricated by the implantation technique (mentioned in the previous section), can be seen in figure 13.

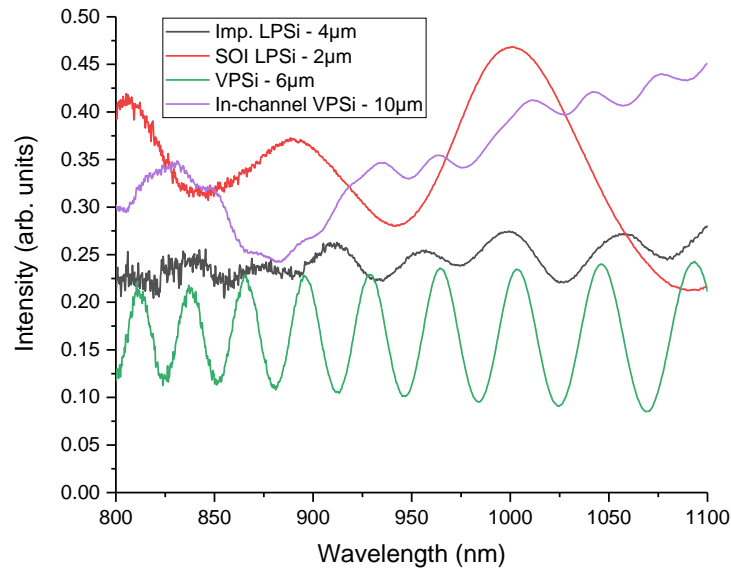


Figure 13 – Reflectance spectra of the different configurations of porous silicon analyzed.

With the aim to compare the different spectra, we have estimated the signal-to-noise ratio (SNR) of each plot. To calculate the SNR, signal and noise powers were calculated from:

$$P = \int I d\lambda \cdot A \quad (1)$$

Where  $I$  is the optical intensity of the signal ( $I_S$ ) or noise ( $I_N$ ) spectrum at a specific wavelength and  $A$  is the cross-section area of the incident beam. Thus, the signal-to-noise ratio (SNR) is:

$$\text{SNR} = \frac{\int I_S d\lambda}{\int I_N d\lambda} \quad (2)$$

Figure 14 illustrates the process followed to estimate the signal level, noise level, and signal-to-noise ratio. The spectral signal was obtained by first performing a smoothing process using the “FFT filter” in Origin 2017 with points of window set at 20 (cutoff frequency=0.26), applying the absolute value function and integrating the resulting spectrum in the wavelength range. The apparent noise level of each reflectance spectrum was estimated by comparing the original data to the filtered ones by subtraction, applying absolute value function, and integrating the resulting spectra.

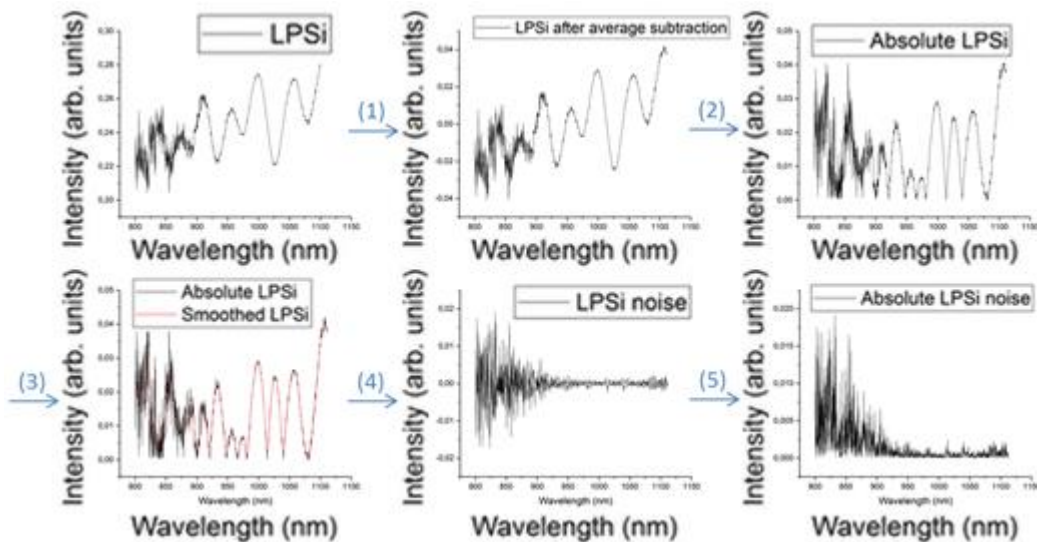


Figure 14 – Steps for extracting the relative noise. (1) The average value is subtracted from the reflectance spectrum; (2) We plot the absolute values; (3) The curve is smoothed by the “FFT filter” with points of window set at 20 (cutoff frequency=0.26); (4) The smoothed curve is subtracted from the original curve to isolate the noise; (5) We use the absolute values.

Among the lateral porous silicon membranes, the 2  $\mu\text{m}$  SOI showed a considerable ten-fold increase in SNR over the chip fabricated by the implantation technique (achieving values of  $\sim 70$  for 2  $\mu\text{m}$  SOI and  $\sim 7$  for the chip fabricated through implantation). This improvement is believed to be, in part, a consequence of the smooth porous silicon/oxide interface of the implanted SOI membrane compared to the probably rougher interface of the implanted chip (as we mentioned in chapter 2). While the improvement in SNR performance does not necessarily translates into direct improved sensitivity, it allows to exploit the data on a larger range of wavelength: thus, we can increase the measured range for the 2  $\mu\text{m}$  SOI chips to over 600 nm (figure 15), and the SNR is still  $\sim 25$ , resulting in an increased RIFTS resolution of 40 nm (compared to 140 nm using a 800 – 1100 nm range on this same sample), translating into a resolution of  $\sim 0.01$  RIU, five times higher than what it has been achieved using lateral porous silicon fabricated through the implantation technique.

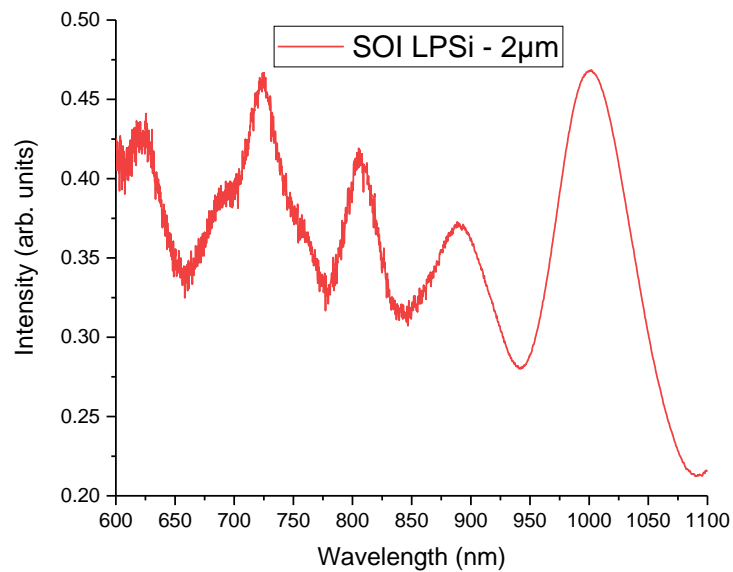


Figure 15 – Reflectance spectra in the 600 – 1100 nm range of a 2 μm SOI lateral porous silicon sample.

The corresponding RIFTS curves can be seen in figure 16, it is remarkable to note that only one peak can be seen when considering data >800 nm due to the loss of resolution, while three peaks appear when considering data >600 nm. These multiple peaks are expected for multilayer interferometers (silicon/BOX/porous silicon in our case) [17]: the first peak (3006 nm) corresponds to the EOT of the BOX layer (theoretically around 2954 nm for a 1 μm silicon dioxide layer, confirmed by the experimental result in figure 16, with the peak for BOX at 2953 nm), the second peak (5274 nm) is the porous silicon layer, and the third peak (8228 nm) roughly matches the sum of the first two.

Meanwhile, in-channel vertical porous silicon demonstrated very similar results to the lateral porous silicon membrane fabricated by implantation. This can be explained by the small area of anodization (90x80 μm<sup>2</sup>). Due to corner effects, the current density during anodization is much higher closer to the corners (as seen in figure 17), meaning that small in-channel vertical porous silicon layers are much more irregular when it comes to layer thickness, affecting the uniformity of the measured area.

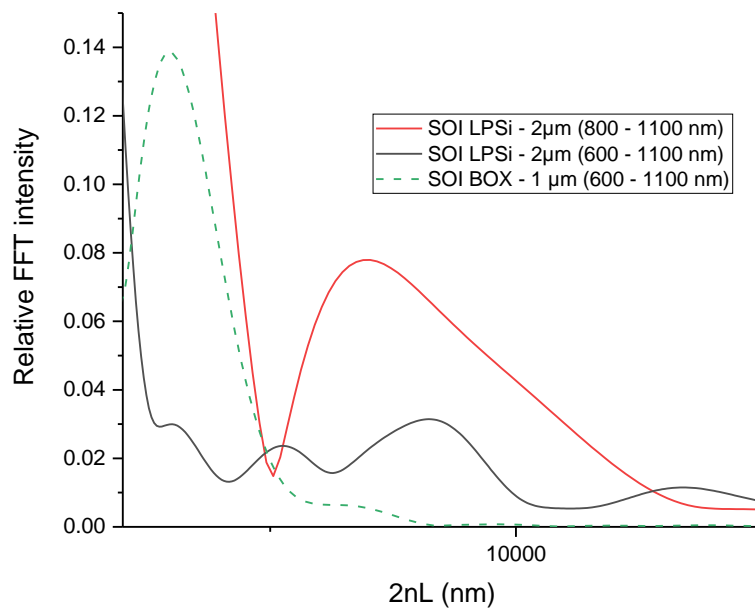


Figure 16 – RIFTS analysis of the spectra for 2 µm SOI lateral porous silicon membranes taking into account two wavelength ranges: 600 – 1100 nm (black) and 800 – 1100 nm (red). In dashed green, the RIFTS analysis was made directly on the BOX layer.

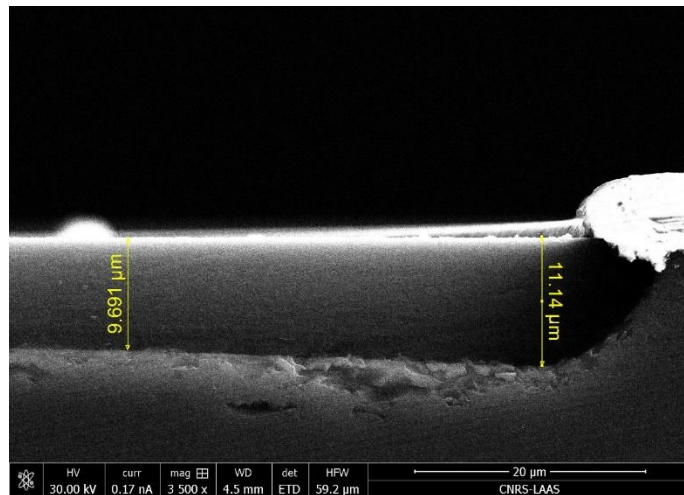


Figure 17 – SEM image showing the cross-section view of the corner of a vertical silicon layer fabricated in our device.

From these analyses, we can conclude that 2 µm SOI lateral porous silicon is the most promising configuration to be used for the transducer. As expected, the SNR also reduces considerably when we reduce the observation window to  $45 \times 10 \mu\text{m}^2$  (as seen in figure 18) going from  $\sim 25$  to  $\sim 8$  at the 600 – 1100 nm range, making the chip configuration with 95 µm long lateral porous silicon membranes the most ideal among the proposed designs.



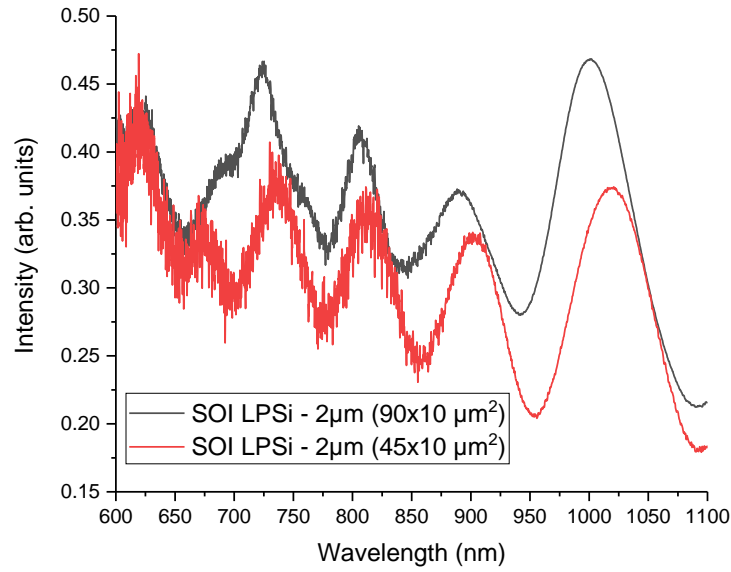


Figure 18 – Reflectance spectra of 2 μm SOI lateral porous silicon membranes measured with different observation window sizes.

### 3.3. Simulation studies on lateral porous silicon interferometry

To better understand how different characteristics of the transducer's configuration impact the optical analysis, we have carried out optical simulations on thin film coatings with the help of Dr. Véronique Bardinal from LAAS-CNRS using the software Essential Macleod (Thin Film Center Inc.), which outputs a reflectance spectrum (with resolution of 0.5 nm) based on the Fabry-Pérot interferometer with specific characteristics: i) refractive and extinction indexes of each material; ii) the layers' thickness; iii) the medium above the interferometer (air for open samples and glass for closed samples); iv) the incident angle of the light.

While the refractive and extinction indexes for the classical materials (glass, air, silicon, silicon dioxide and silicon nitride) were already provided in the software's database, we had to input the values for porous silicon. These values were estimated based on the Bruggeman model mentioned in chapter 1. The refractive and extinction indexes were calculated by the symmetric and nonsymmetric Bruggeman approximations using equation 3 and 4 below [17,18]:

$$n = \frac{1}{2} \sqrt{ \frac{2n_{skeleton}^2 - n_{fill}^2 - 3Pn_{skeleton}^2 + 3Pn_{fill}^2}{\sqrt{8n_{skeleton}^2 n_{fill}^2 + (n_{fill}^2 - 2n_{skeleton}^2 + 3Pn_{skeleton}^2 - 3Pn_{fill}^2)^2}} } \quad (3)$$

$$\frac{k^2}{k_{skeleton}^2} - \frac{k_{fill}^2}{k_{skeleton}^2} = (1 - P) \left[ \left( 1 - \frac{k_{fill}^2}{k_{skeleton}^2} \right) \left( \frac{k^2}{k_{skeleton}^2} \right)^{\frac{1}{3}} \right] \quad (4)$$

Where  $n$ ,  $n_{skeleton}$  and  $n_{fill}$  are the refractive indexes for the porous silicon layer, its silicon skeleton and its medium filling, respectively; and  $k$ ,  $k_{skeleton}$  and  $k_{fill}$  their respective extinction indexes.  $P$  is the porosity.

As the refractive index of silicon varies according to the wavelength [19], we applied the model throughout the range studied.

### 3.3.1. Simulation validation: comparison with experimental results

To validate the simulations, we modelled a single homogeneous 4  $\mu\text{m}$  porous silicon layer with 40% of porosity covered by a glass slide, for various refractive index filling media (figure 19), and compared the output spectra with the experimental spectra of the implanted lateral porous silicon sample (of figure 12).

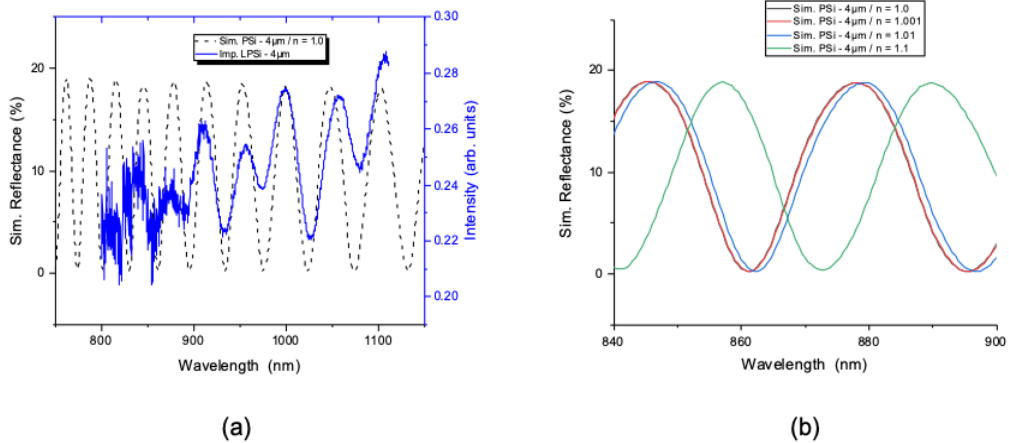


Figure 19 – (a) Comparison of experimental (solid blue) and simulated (dashed black) reflectance spectra of the implanted porous silicon sample. (b) Simulated spectra for various refractive index filling media.

The simulation adequately predicts peaks at the same position of the fringe maxima observed in the experimental spectra for the same filling media ( $n = 1.0$ ). Furthermore, by varying the refractive index filling media, we have estimated the theoretical sensitivity of our device. The simulated spectra shift at 845 nm is 44 nm when  $n_{fill}$  changes from 1 to 1.1, leading to a theoretical sensitivity of 440 nm/RIU. This is almost a threefold increase compared to the experimental sensitivity ( $\sim 156$  nm/RIU). We suggest that this discrepancy could originate from the lack of homogeneity of the porous layer in terms of thickness, porosity, and pore size, confirming what we have discussed over the SNR analysis.

### 3.3.2. Impact of various experimental parameters

For the purpose of understanding the impact of several parameters involved in the experimental setup or the transducer architecture, we carried out RIFTS analysis of simulated spectra for 2  $\mu\text{m}$  SOI and: i) a change in light incidence angle ( $8^\circ$  vs.  $0^\circ$ ); ii) the presence of the glass cover; iii) the presence of the thin silicon nitride layer on top of the porous silicon; iv) with and without the bottom silicon dioxide layer. All the comparison can be seen in figure 20.

First, the change of light incidence angle has shown virtually no impact in the analysis, peaks are positioned at  $8701 \pm 60$  nm and  $8751 \pm 59$  nm, for  $8^\circ$  and  $0^\circ$  incident angles, respectively. Due to how small the incident angle derived from the microscope's objective ( $8^\circ$ ), we can confirm that we can consider a normal incidence light beam.

Second, as expected because the equivalent added EOT is much larger than that of the porous silicon layer and the BOX layer, the presence of glass cover has also virtually no incidence on the peak position.

Third, we studied the influence of the 80 nm thick silicon nitride layer added on top of the porous silicon membrane to force the current to flow in a lateral fashion during anodization. Because the thickness of that layer is much lower than the 2  $\mu\text{m}$  porous silicon and 1  $\mu\text{m}$  silicon dioxide layers, we confirm through the simulation that its presence is negligible as well.

Lastly, the conclusion regarding the presence of the BOX layer is similar, even if the resulting FFT plot looks different because of the additional peak due to the oxide interferometer.

From these four analyses, we can conclude that the configuration resulted from our fabrication technique (BOX/porous silicon/silicon nitride/glass) bare no impact in the transducer's spectra, confirming that the technique causes no limitations when it comes to lateral porous silicon-based interferometry.

However, there is still room for improvement. In the next section, we will go through our investigation of the possibility of improving the transducer's performance with the use of advanced optical structures.

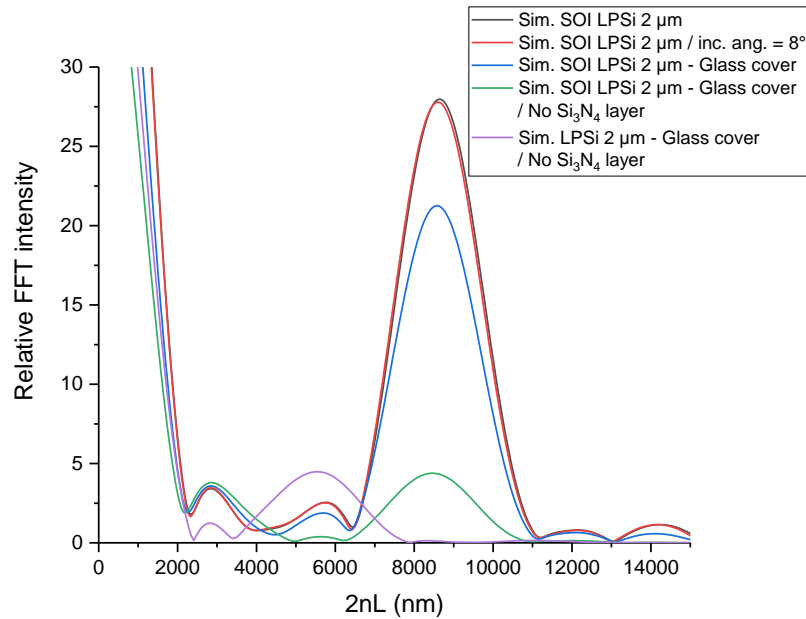


Figure 20 – RFTS analysis of the simulated spectra of different configurations. Si/BOX/PSi/Si<sub>3</sub>N<sub>4</sub>/Air (black), Si/BOX/PSi/Si<sub>3</sub>N<sub>4</sub>/Air with an incidence angle = 8° (red), Si/BOX/PSi/Si<sub>3</sub>N<sub>4</sub>/Glass (blue), Si/BOX/PSi/Glass (green), and Si/PSi/Glass (purple).

### 3.3.3. Study on the use of advanced optical structures

Rather than simple porous layers, microcavities and rugate filters are known to provide sharp spectral features and sensors with high quality (Q) factors [20]. Even if the device sensitivity is independent of the Q factor, a better Q improves the confidence and reliability in resolving smaller resonance shifts [13]. Such advanced architectures that rely on the integration of dielectric layers are fairly easy to fabricate with vertical porous silicon layers since they can be made up with alternating layers of different porosities to modulate the refractive indexes [15]. This can simply be achieved by modulating the current density during porous silicon anodization through the thickness of the silicon wafer.

In our case, because we are creating the porous silicon in a lateral fashion, we cannot use this simple trick. However, we can easily pattern thin films with various refractive indexes, e.g. silicon dioxide and silicon nitride, on top of the porous silicon membrane to create a dielectric mirror. As a matter of fact, we could also imagine, after encapsulating the microchannels and membranes with the glass cover, etching the handle wafer to release the structure and report it onto a substrate hosting another dielectric mirror, thus sandwiching the lateral porous silicon membrane between 2 mirrors. We acknowledge that it surely would be much more complicated to implement, and it would cancel the monolithic integration advantage of our process. Still, we have used simulation to study the impact of the integration of 3.5 pairs of alternating 105 nm silicon nitride and 146 nm silicon

dioxide layers. The corresponding spectra are shown in figure 21 and, as expected display narrower fringes that would enable to create lateral porous silicon interferometers with improved performances.

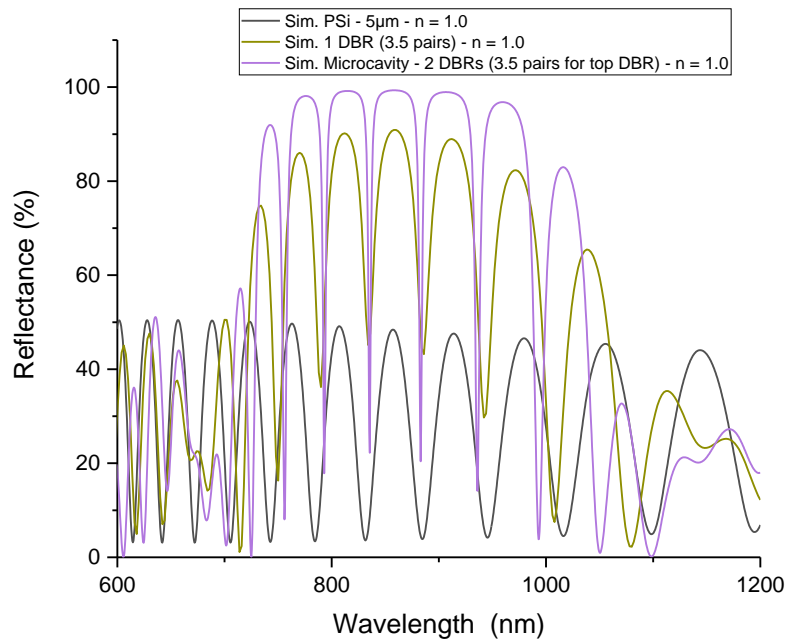


Figure 21 – Simulated reflectance spectrum of a 4  $\mu\text{m}$  thick implanted lateral porous silicon layer (black curve). Similar spectra when a dielectric mirror is added on top of the porous layer (yellow curve) and when two mirrors are added on top and bottom of the lateral porous silicon membrane (purple curve).

#### 4. Preliminary results on porous silicon functionalization

In chapter 1, we discussed the importance of surface functionalization to use porous silicon as a biosensor. This need is caused first by the instability of the material in aqueous solutions, due to dominance of Si-H and Si-O bonds; and second it is mandatory to be able to selectively trap the biomolecular targets for biosensing.

In the case of our integrated chip, a considerable level of complexity is introduced due to the need of the functionalization process to be localized, as the target molecules need to be trapped only on the porous silicon element to be used as a transducer.

There are several means that we could consider to achieve localized functionalization of the lateral porous silicon membranes. First, silanization of oxidized silicon is a very commonly used method to attach proteins, DNA, and many other molecules to the silicon surface, and it can be coupled with a spotting system to enable local patterning. Secondly, and for porous silicon more specifically, a functionalization method was developed by M. J. Sailor's group in which a selective modification of the outside/inside of the pores is done by liquid masking [21].

Finally, hydrosilylation provides the formation of Si-C bonds on silicon surfaces by the insertion of an unsaturated bond into a silicon-hydride group, and when it is promoted by ultra-violet (UV) light induced photochemistry, it enables the localized chemical binding of unsaturated compounds on the porous silicon surface with high resolution and accuracy by means of a protective mask.

Because it offers a real option for local functionalization with micrometer precision by using a dedicated a hard mask [22], making it easily adapted to the functionalization of lateral porous silicon-based devices, we have conducted preliminary tests of UV-induced photochemical hydrosilylation.

#### 4.1. Introduction to UV-induced photochemical hydrosilylation

Hydrosilylation is a common surface functionalization technique based on the covalent binding of alkenes and alkynes to hydrogen-terminated silicon surfaces. Its primary mechanism is a radical chain reaction initiated by abstraction of hydrogen from the surface via thermal, catalytic or photochemical activation to form a highly reactive surface dangling bond [23]. UV irradiation cause the hydrosilylation by promoting the homolytic cleavage of Si-H bonds, resulting in surface radicals that allow the binding of alkenes and alkynes [22] (the mechanism is shown in figure 22).

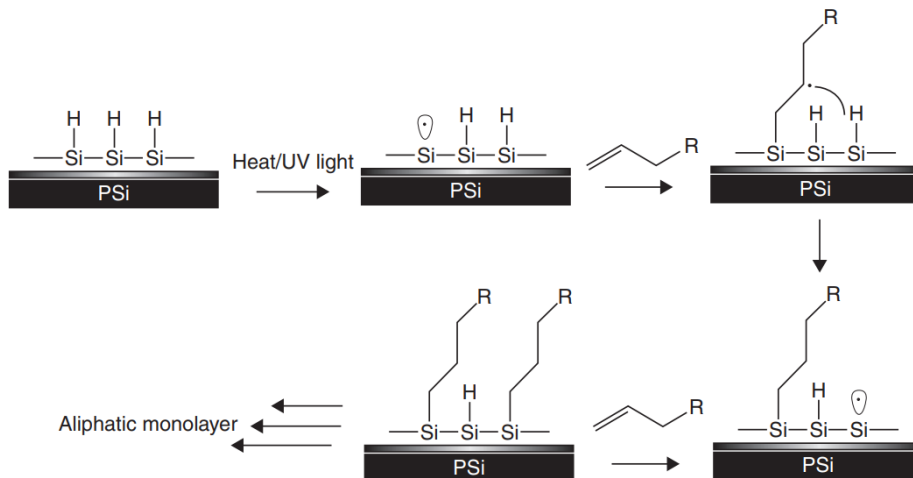


Figure 22 – Schematics of the mechanism of UV-induced photochemical hydrosilylation of porous silicon for 1-alkenes reacting with silyl radical [22].

Since this technique relies on UV irradiation for local activation, there are two ways to apply it to the functionalization of our samples:

- i) We can carry out surface functionalization before closing the microfluidic chip, and thus apply this technique directly to the sample before encapsulation. However, this means that encapsulation through anodic bonding is not possible anymore because this high temperature process would damage the grafted molecules. A way to counter this obstacle would

be to replace the anodic bonding technique with the use of an adhesive, e.g. polydimethylsiloxane (PDMS) bonding. A thin layer of PDMS ( $\sim 40 \mu\text{m}$ , so it is not an issue for optical measurements) can be easily spin-coated on a glass slide, and upon plasma  $\text{O}_2$  activation, it can form an irreversible bond with silicon dioxide at room temperature when the surfaces are brought together [24];

- ii) Since we can flow the allylamine solution through the microchannels, we could imagine carrying out the functionalization process after chip encapsulation, in that case we could still use the anodic process.

#### **4.2. Procedure for UV-induced photochemical hydrosilylation**

The work presented here was conducted mainly by Dr. Kata Hajdu, a postdoctoral researcher in our team, in collaboration with the team of Dr. Frédérique Cunin from the Institut Charles Gerhardt Montpellier (ICGM). The UV-induced photochemical hydrosilylation was tested on porous silicon samples fabricated from  $\langle 100 \rangle$  p-type wafers ( $d = 100 \text{ mm}$ ,  $t = 525 \mu\text{m}$ ,  $\rho = 3 \text{ m}\Omega\cdot\text{cm}$ ) upon anodization in 1:1 HF:1-butanol electrolyte, by applying a current density of  $500 \text{ mA/cm}^2$  for 30 s, forming  $\sim 80 \text{ nm}$  diameter pores with  $\sim 90\%$  porosity.

Allylamine (purchased from Merck) was used as a simple unsaturated organic molecule with an accessible amine-group. We dissolved it in dimethoxyethane (DME) with different concentrations: i) pure allylamine, ii) 2 times dilution, iii) 10 times dilution, and iv) 100 times dilution. The covalent attachment of allylamine took place at room temperature by UV irradiation (wavelength 365 nm) on freshly etched porous silicon samples for 2 hours. After the hydrosilylation procedure, the samples were intensively washed with chloroform, ethanol, and water, ensuring the removal of unspecific binding molecules.

#### **4.3. Characterization of functionalized samples**

The samples were characterized by SEM. We have observed that using pure allylamine (figure 23) or 2 times dilution, the pores were completely filled, and a thick layer was formed on the surface. The 10 times diluted allylamine solution (figure 24), on another hand, covered the pores walls without clogging them, allowing a uniform layer on the porous silicon surface. Finally, samples treated with 100 times diluted solution did not display a continuous and homogenous layer.

With the formation of a homogenous allylamine coating, amine groups are available at the silicon surface. The grafting of probe biomolecules can then be accomplished by using different amine-targeted crosslinker molecules, e.g. glutaraldehyde (GTA), which is a homobifunctional crosslinker, enabling the connection of the allylamine's amine group with that of the desired biomolecule (antibodies, DNA, enzymes).

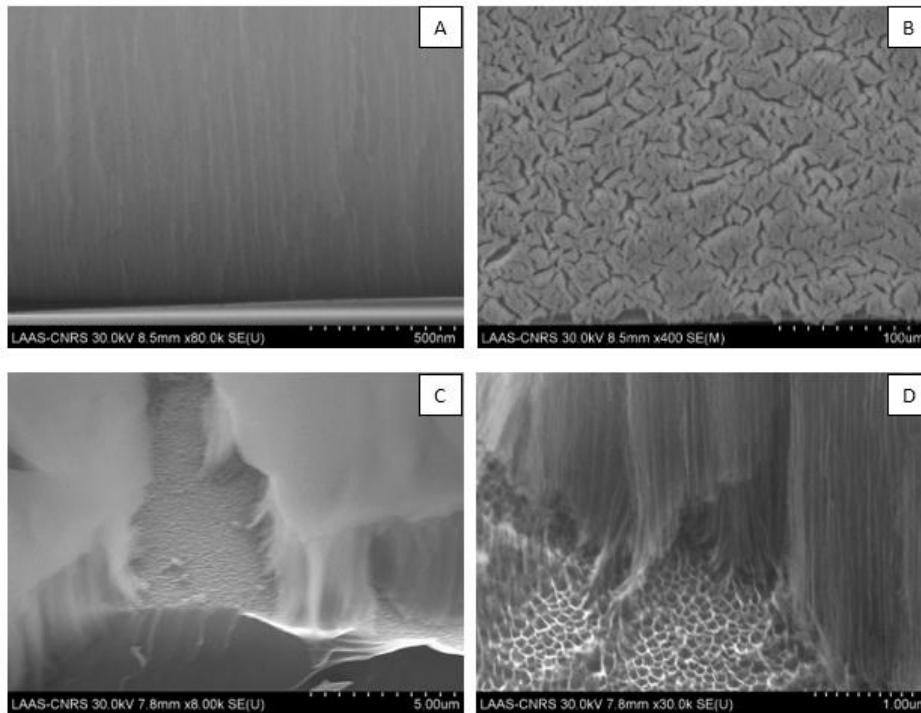


Figure 23 – SEM images of vertical porous silicon samples after incubation with non-diluted allylamine for 2h under UV radiation (365 nm). (a) Cross-section, (b) top view, (c, d) cross section at 45°.

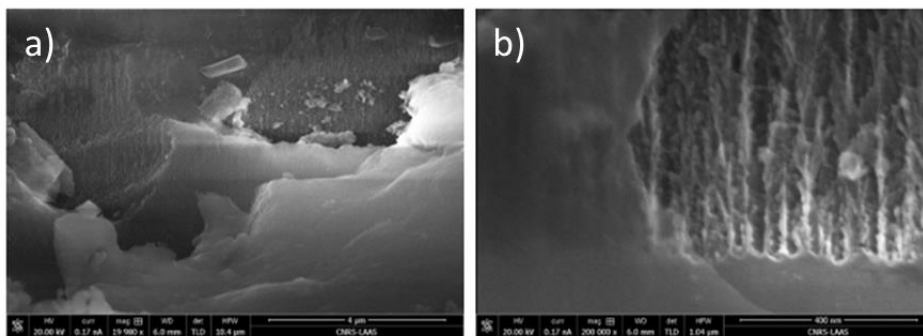


Figure 24 – SEM cross-section images of vertical porous silicon samples after incubation with 10 times diluted allylamine for 2h under UV radiation (365 nm).

## 5. Conclusion and perspectives

In this chapter, we have presented the design and fabrication of microfluidic chips using various porous silicon membranes to achieve the different functions involved in sample preparation and analysis.

We have proposed several designs with both lateral porous silicon and in-channel vertical porous silicon of various sizes as candidates for interferometry transducers. We then conducted several experiments and simulation analysis to study the influence of key parameters in the imaging set up and porous silicon chip onto the



interferometer performance: this preliminary work confirmed that the lateral porous silicon interferometer based on SOI is best suited for on-chip sensing.

Lastly, in order to turn the lateral porous silicon interferometer into a biosensor, we have presented various routes for porous silicon biofunctionalization. Out of the different approaches that could enable localized molecular grafting onto the porous silicon sensing elements, we have investigated the use of UV-induced photochemical hydrosilylation: this functionalization method could be integrated in the fabrication process of the lab-on-a-chip, but more work is needed to confirm this claim and deliver a proof-of-concept.

Still, despite the lack of demonstration of adequate on-chip working functionalities, we have shown here that lateral porous silicon elements can be integrated into a lab-on-a-chip to perform the sample preparation and analysis steps: if the remaining challenges can be overcome, our solutions could deliver a monolithic point-of-care device. The last questions to answer are, then: for what application? To detect what kind of biomarkers? Hints that could help us answering these questions are to be found within the characteristics of the porous silicon lab-on-a-chip:

- From a sensitivity point of view, despite the fact that we unfortunately did not provide experimental data on biosensing in this PhD work, given the fact that our interferometer displays optical sensitivities in the range of values that can be found in the literature, we can speculate that we could reach at least the nM concentration sensitivity [25].
- The previous works of Yingning He on ion concentration polarization with lateral porous silicon in a dual-channel configuration have shown achievable concentration factors up to 5000, using very low voltages when compared to the literature [9]. By solving electrical leakage issues on the chip that should allow us working with higher voltages, and by using the triple-channel configuration proposed in this work, we believe that we can achieve a concentration factor of  $10^6$ , which has been obtained with nanofluidic junctions [26]. Such a concentration factor would allow us to lower the sensitivity of the lateral porous silicon interferometric sensor to the fM range.
- From a throughput point of view, we know we will be limited by the fluidic resistance of the membranes: hence, in order to keep the assay time short enough to make sense from a point-of-care point of view (e.g. <2h), the application should concern samples of very small volumes. For instance, membranes with the largest pore diameter achieved in this work display 50 nm pore diameter and a porosity close to 90%: from an estimated fluidic resistance

in the range of few tenths of  $\text{Pa s } \mu\text{m}^{-3}$  allows to process roughly  $1 \mu\text{l/h}$ , which is thus suitable for the analysis of finger prick blood for instance.

Assuming we could process blood samples, which is the aim to integrate a filtering module to the chip, then, we could for instance target the detection of Troponin I, a biomarker for myocardial infection in blood, for which the availability of an early diagnostic test would have a huge impact. Indeed, cardiovascular disease is one of the greatest causes of adult mortality, which accounts for nearly half of all the deaths in the western world [27]. Electrocardiogram is currently the major methodology for diagnosis of cardiovascular diseases; however, up to 50-70% of hospital admission related to acute coronary syndromes, among which, myocardial infections, shows either normal or ambiguous electrocardiogram result. Therefore, the assessment of cardiac biomarker becomes an important diagnostic methodology to truly make a reliable medical decision and treatment.

Troponin I is considered the gold standard biomarker of myocardial infection diagnosis, because it is present only from the damage of the myocardium. Typical commercially available biosensors for detection of biomarkers require 20 minutes to 1 hour of assay time, but have a limit of detection at  $1 \text{ ng/mL}$  level for Troponin I, whereas the clinical cut-off levels are around  $0.01\text{-}0.1 \text{ ng/mL}$  ( $\approx 0.4\text{-}4 \text{ fM}$ ). As a result, sensitive immunoassay-based biosensors, processing crude samples, are thus required for early detection of cardiovascular biomarkers [28]. Given its previously discussed characteristics, we believe that the lateral porous silicon platform can provide an all integrated and simple-to-implement solution to this challenge.

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## Conclusion

The goal of this work was to develop a monolithic integrated device for point-of-care applications. The foundation of this work was the lateral porous silicon membranes, previously proposed by the MEMS team at LAAS, that can be integrated into planar fluidics and can function as a filtering, a preconcentration or a biosensing module. Hence, we proposed here to integrate multiple membranes with controlled and varying morphologies on the same chip to implement sample preparation and analysis tasks.

The parameters that control the porous silicon morphology can be divided in two categories: wafer-based parameters (doping type and level, crystallographic orientation), and anodization-based parameters (current density, electrolyte used). To achieve the fabrication of different porous silicon elements in a single chip, we can tune one of these parameters in selected regions of the chip.

Anodization-based parameters are easier to control, since they are set in one of the last steps of the fabrication process and they are the usual parameters used to control pore morphology. Hence, we have implemented a process based on sequential anodization steps in order to fabricate multiple membranes with modified anodization-based parameters. To this aim, we have proposed to protect previously fabricated lateral porous silicon membranes with a metal layer (Cr/Au) to avoid further exposition to HF solution. However, because the intrinsic stress caused by chromium deposition results in the damage of the porous silicon membranes, this process was not successful. Hence, further developments are needed where we should investigate the replacement of the chromium layer or means to reduce the mechanical stress induced during the metal deposition.

Wafer-based parameters are not as straight forward to manipulate, and they add limitations since they are set early on in the fabrication process. However, being able to perform only a single anodization step adds a considerable simplicity to the process. Since the doping parameters are the wafer-based parameters that mostly contributes to the morphology of the pores, we have developed two fabrication processes based on the local ion implantation of silicon. We have first investigated the possibility to carry out a double implantation on a standard silicon wafer: the first one being conducted on the entire wafer and the second one being localized to create zones of higher doping levels. This technique has shown to have strong limitations: indeed, the use of higher current densities and lower concentration of HF required to achieve larger pore sizes, result in electropolishing regions around the membranes. Finally, by performing a single localized ion implantation on an already highly doped SOI wafer, we have shown that this implanted SOI process is less complex and most reliable. We were able to achieve a two-fold pore size increase in different regions of the chip with a single anodization step, fabricating 10  $\mu\text{m}$  thick lateral porous silicon membranes with pores size ranging from

~25 nm to ~50 nm on a single 2  $\mu\text{m}$  SOI chip, while the porosities varied from ~80% to ~90%. By etching the BOX layer on the bottom of the microchannels, we were also able to form vertical porous silicon layers during the same anodization step, reaching ~35 nm of pore size and ~65% of porosity on the same sample.

After developing the process to fabricate multimembranes with tunable properties, we have designed and fabricated a lab-on-a-chip to be used for sample preparation through ion concentration polarization, and sample analysis through interferometric-based biosensing. Fabricated chips were filled with liquid solution, proving the adequate fluidic function of the porous membranes. We carried out preliminary experimental tests and simulation studies on the porous silicon interferometer module, confirming that the SOI configuration was best suited for sensing. The measured sensitivity of the fabricated interferometer was  $\Delta\lambda/\Delta n_{fill} \approx 156 \text{ nm/RIU}$ , which is in the same range as the sensitivity of other vertical porous silicon interferometers reported in the literature, and the corresponding limit of detection was  $6 \times 10^{-4} \text{ RIU}$ . Although, it is a typical value for single layer porous silicon interferometers, it is high compared to e.g. surface plasmon resonance platforms. For this reason, we proposed to implement advanced optical structures by integrating dielectric layers on top of the porous membranes. Simulation studies that we conducted have shown that such structures would provide sharp spectral features and sensors with high quality factors that improve the confidence and reliability in resolving smaller resonance shifts. However, the integration of said structures is far from simple for our devices, requiring further development.

In order to turn our interferometric sensor into a biosensor, the porous silicon must be adequately functionalized. Additionally, the functionalization only concerns the porous membrane to be used for sensing. Hence, we have proposed various means to achieve the localized molecular grafting onto porous silicon and we have tested the most promising route, that is optically-induced and offers micrometer precision by using a dedicated a mask. We have shown that UV-induced photochemical hydrosilylation can achieve selective pore functionalization without obstruction after properly diluting the active chemicals. Remaining work consists in demonstrating that this functionalization protocol is adapted to lateral porous silicon-based chips and is compatible with the entire fabrication process.

In conclusion, we have developed a fabrication technique that allows the monolithic integration of porous silicon membranes with tunable characteristics into planar lab-on-a-chips for microfluidic applications. Still, more work is necessary to fully develop the bioanalytical device: implementation of the functionalization strategy on the lateral porous silicon membranes, assessment of the biosensor and ICP modules, and probably most importantly, find a killer application and test the device in real conditions.