Development of an innovative 77 GHz radar receiver architecture and demonstration in 28 nm FDSOI CMOS

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THÈSE

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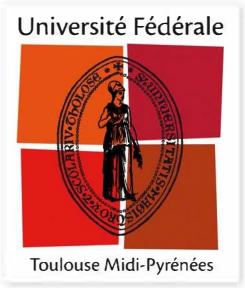

A DISSERTATION

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Alexandre FLETE

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Design of an innovative 77 GHz radar receiver architecture in 28-nm FDSOI CMOS

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Department: **Electromagnétisme et Systèmes Haute Fréquence**

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Mr. Sylvain BOURDEL, Referee
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Mr. Philippe CATHELIN, PhD Co-supervisor from the socio-economic world
Mr. Jean GAUBERT, President

Résumé :

Grâce à sa capacité à détecter des cibles éloignées malgré une mauvaise visibilité, le radar automobile à 77 GHz joue un rôle important dans l'aide à la conduite. L'utilisation des fréquences millimétriques offre une bonne résolution et une importante capacité d'intégration des circuits. C'est aussi un défi car il faut satisfaire un cahier des charges exigeant sur le bruit et la linéarité du récepteur.

Les technologies SiGe BiCMOS ont été les premières utilisées pour la conception de récepteurs radar à 77 GHz. De bons résultats ont été obtenus en se basant sur des architectures utilisant des mélangeurs actifs. Cependant l'utilisation des technologies BiCMOS se traduisait par une consommation élevée, une faible capacité d'intégration et des couts de production importants. Récemment, l'intégration des procédés CMOS menant à l'augmentation des fréquences de transition rend ces technologies plus attractives pour les applications nécessitant un faible coût et la cointégration de plusieurs fonctions au sein d'une même puce.

La littérature sur les récepteurs radars en technologie CMOS à 77 GHz montre que les architectures inspirées par les technologies BiCMOS ne sont pas pertinentes pour cette application. Le but de cette thèse est de montrer que l'utilisation de techniques propres aux technologie CMOS comme l'échantillonnage et l'utilisation de portes logiques permet d'obtenir de très bonnes performances.

Dans ce travail, deux nouvelles architectures de récepteur radar basées sur le principe d'échantillonnage sont proposées. La première architecture est basée sur un mélangeur passif échantillonné qui permet d'obtenir un très bon compromis bruit/linéarité. La seconde exploite les propriétés des mélangeurs sous-échantillonnés afin utiliser une fréquence d'OL trois fois inferieure à la fréquence RF offrant ainsi de très intéressantes simplifications au niveau de la chaine de distribution du signal d'OL du récepteur.

Le contexte de cette étude est expliqué dans le 1er chapitre qui présente les exigences de conception liées à l'application radar et fourni une analyse de l'état de l'art des récepteurs à 77 GHZ. Le chapitre suivant décrit le principe de fonctionnement et l'implémentation d'un mélangeur échantillonné à 77 GHz en technologie CMOS 28-nm FDSOI. Une topologie de mélangeur sous-échantillonné utilisant une fréquence d'OL de 26 GHz pour convertir des signaux RF autour de 77 GHz est ensuite détaillée dans le chapitre 3. Le chapitre 4 conclut cette étude en détaillant l'intégration des mélangeurs étudiés dans les chapitres précédents avec un amplificateur faible bruit dans différents récepteurs radars. Ces architectures de récepteurs basées sur l'échantillonnage sont ensuite comparées entre elles et avec l'état de l'art montrant ainsi leurs avantages et inconvénients. Les résultats de cette comparaison confirment l'intérêt des techniques d'échantillonnage pour la conversion de fréquence dans le cadre de l'application radar.

Summary:

With its ability to detect distant targets under harsh visibility conditions, the 77 GHz automotive radar plays a key role in driving safety. Using mm-wave frequencies allow a good range resolution, a better circuit integration and a wide modulation bandwidth. This is also a challenge for circuit designers who must fulfill stringent requirements especially on the receiver front-end.

First 77 GHz radar receivers were manufactured with SiGe BiCMOS processes benefiting from the high transition frequency and high breakdown voltage of Hetero-junction Bipolar Transistors (HBT). Good results have been achieved with active-mixer-based architectures, but these technologies suffer from high power consumptions, limited integration capacity and large production cost.

More recently, the scaling down of CMOS processes (coming together with the increase of the transition frequency of the transistors) makes CMOS a good candidate for 77 GHz circuit design, especially when cost target requires single chip solutions.

The literature related to CMOS radar receivers highlights that receivers based on BiCMOS architectures generally show poor performances. The aim of this work is to demonstrate that using CMOS specific technics such as sampling and the use of high-speed digital gates should enhance the performance of the receivers.

In this work, two innovative radar receiver architectures based on the sampling principle are proposed. The first one shows that this principle can be extended to millimeter wave frequencies to benefit from a very good noise/linearity trade-off. While the second one uses this principle to converts a 77 GHz RF signal by using a 26 GHz LO frequency thus simplifying the LO distribution chain of the receiver.

The background of this study is introduced in the chapter 1 presenting the design trade-off related to the 77 GHz radar receiver and provides a review of the existing solutions. The following chapter describes the sampling mixer principle and the implementation of a 77 GHz sampling mixer in 28-nm FDSOI CMOS technology. Then, a sub-sampling mixer topology allowing to convert an RF signal around 77 GHz using a 26 GHz LO frequency is detailed in the chapter 3. The chapter 4 draws the conclusion of this study by showing the implementation of the two proposed sampling-based mixers with a low noise amplifier in 77 GHz front ends. These receiver architectures are compared with the state of the art highlighting the strengths and weaknesses of the proposed solutions. The results of this study demonstrates that using sampling for down conversion can be convenient to address millimeter-wave frequency applications.

Table of Contents

Acknowledgments

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First of all, I would like to thank my advisors Christophe Viallon, Thierry Parra and Philippe Cathelin, for making these 3 years a very nice experience. I really appreciated their amazing support and their huge involvement. By showing a lot of interest and proposing very interesting ideas they made me really enjoy this project and learn a lot.

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General introduction

From the first generation of vehicles, including a few comfort driving assistance options, to semi-automated driving features like automatic emergency braking or lane keep assistance, the driving assistance products have been continuously improved in the past few decades. Nowadays, the brand-new vehicles include ultrasonic sensors, camera, Radar and Lidar to ensure object detection all around the car under any conditions, paving the way for a full autonomous driving. To detect potential threat, the automotive radar emits a high-frequency electromagnetic wave which is reflected on the surrounding objects. Then, the radar sensor receives and analyses the reflected signals to calculate the speed, range and direction of the obstacles. With its ability to detect distant targets under harsh visibility conditions, the 77 GHz automotive radar plays a key role in driving safety.

Millimeter-wave frequencies enable a better circuit integration and good radar resolution on the target speed and range. This is also a challenge for circuit designers who must deal with stringent requirements especially on the receiver front-end. The main challenge is the trade-off between noise and linearity. An automotive radar must cope with multiple signal reflections that desensitize the receiver if its linearity is not high enough. At the same time, a too high noise level limits the receiver distant targets detection. These requirements are not easily compatible because a high-gain low noise amplifier will improve noise performances but will degrade linearity, as the mixer that follows will be saturated earlier. Consequently, the mixer design is important to find a good trade-off between noise and linearity.

First 77 GHz radar receivers were manufactured with SiGe BiCMOS processes benefiting from the high transition frequency and high breakdown voltage of Hetero-junction Bipolar Transistors. Good results have been achieved with active-mixer-based architectures, but these technologies suffer from high power consumptions, limited integration capacity and large production cost. More recently, the scaling down of CMOS processes makes CMOS a good candidate for 77 GHz circuit design, especially when cost target requires single chip solutions. The literature related to CMOS radar receivers highlights that receivers based on BiCMOS architectures show poor performances. The aim of this work is to demonstrate that

performances of 77 GHz CMOS receivers can be enhanced using CMOS specific technics, such as sampling and the use of high-speed digital gates. In this work, two innovative radar receiver architectures based on the sampling mixer principle are proposed. The first one shows that this principle can be extended to millimeter-wave frequencies to benefit from a very good noise/linearity trade-off. The second architecture uses this principle to convert a 77 GHz RF signal by using a 26 GHz LO frequency thus simplifying the LO distribution chain of the receiver.

The background of this study is presented in the chapter 1. First, the automotive radar application is introduced by explaining the 77 GHz radar operating principle and design specificities. Then the 28-nm FD-SOI CMOS technology used for the integrated RF circuit design in this work is presented. Finally, the different existing CMOS radar receiver design solutions will be presented and discussed to highlight the more appropriate architecture for the integration of a 77 GHz radar receiver in a 28-nm FD-SOI CMOS technology. The chapter 2 describes the sampling mixer principle and the implementation of a 77 GHz sampling mixer based on a new 77 GHz LO pulse shaper. The measurement setup and associated measured performances are reported at the end of this chapter and validate the interest of this new mixer topology. Then, a sub-sampling mixer topology allowing to down-convert an RF signal around 77 GHz using a 26 GHz LO frequency is detailed in the chapter 3. Measured performances confirm the good capabilities of the sub-sampling principle. The chapter 4 draws the conclusion of this study by showing the implementation of the proposed sampling-based mixers with a low noise amplifier in 77 GHz front-ends. These receiver architectures are compared with the state of the art highlighting the strengths and weaknesses of the proposed solutions. All the results of this study demonstrate that using sampling down-conversion can be the good choice to address millimeter-wave frequency applications.

Chapter 1 The 77 GHz radar for automotive applications

1.1 Introduction

The acronym RADAR stands for “RAdio Detection And Ranging”. In a radar sensor, an electromagnetic wave is generated and emitted by an antenna. Then, this signal is reflected by the surrounding objects and received by the radar sensor. Analysing the properties of the reflected signals allow to detect surrounding objects and calculate their speed, range and direction.

In the past few decades, the growing concern about driving safety is challenging the automotive industry with the need of very efficient driving assistance products. Therefore, Automotive manufacturers started to include radar sensors into their vehicles. The first generation of cars integrating radar sensors only benefited from a few comfort options as adaptive cruise control and parking assist [1, p. 17]. From the first cars including these features, the driving assistance has been continuously evolving to reach different level of automation. Nowadays, new cars benefit from a lot of new features as for example self-parking, blind spot detection or emergency braking [2],[3]. This partial driving automation paves the way for a full autonomous driving in the coming years. To reach this level of automation, a full coverage detection around the car is required [3] as described in Figure 1-1. To cover every angle around the car more radar sensors will be required in the next car generations. Furthermore, as each kind of sensor has its strengths and weaknesses, the automotive radar must be combined with other driving safety sensors to be able to prevent crashes under any conditions.

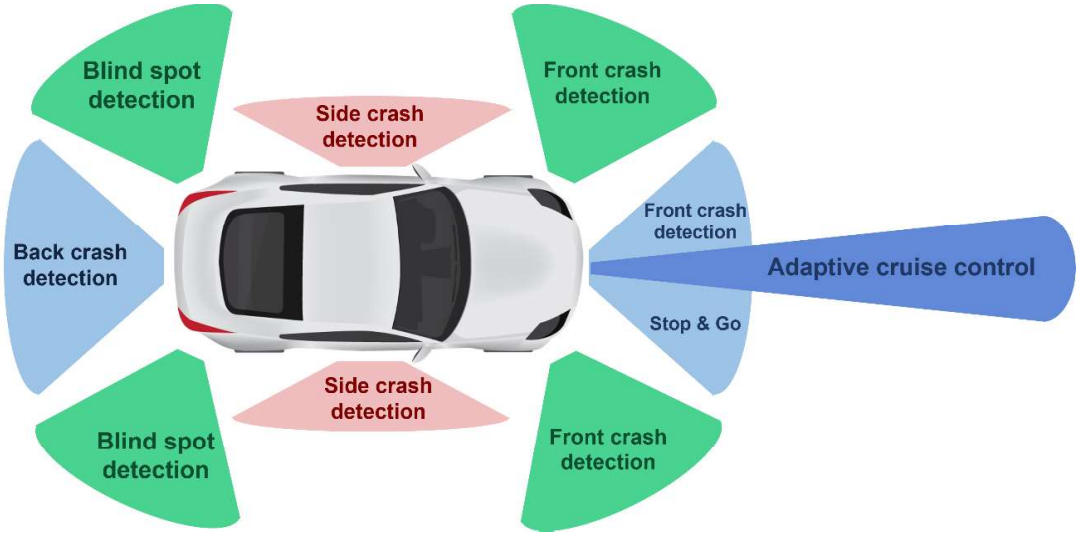

Figure 1-1: Detection coverage in the next generation of cars.

1.2 The radar among the driving assistance sensors

The object detection for driving safety generally relies on four different detection principles: Ultrasound, radar, camera and lidar [4]. The advantages and drawback of each kind of sensor ([3], [5]) are summarized in the Table 1-1.

Table 1-1:Comparison of automotive detection sensors.

	Ultrasound	**Camera**	**Radar**	**LiDAR**
Strengths	• Range detection	• Object recognition	• Range/speed detection • Weather immunity	• Range/speed detection • Accuracy
Weaknesses	• Limited range • No speed detection	• Limited range/ no speed detection • Weather	• Ghosts target	• Weather
Cost	Low	low	moderate	High

Ultrasonic sensors are the best solution for close objects detection as they are well mastered and low cost, but they are too sensitive to weather and have a too limited range to address other applications. Nowadays, the use of camera for automotive application is widespread as they

are low cost, easy to implement and can recognize colours and objects. Nevertheless, cameras are very sensitive to weather and cannot efficiently assess the speed and range of a target. With its ability to detect the range, speed and direction of a distant target under any weather condition, the radar sensor plays a key role in driving safety. The weaknesses of radar sensors are the potential wrong detection caused by ghost targets [6] and cost which remains significantly higher than ultrasound sensors or cameras. Finally, Lidar sensors based on the laser detection are also able to detect the range, speed and direction of a target and have the best accuracy among automotive sensors. Lidar sensors are not currently widespread because of production cost. To reach the next level of driving automation, a combination of these detection principles will be used. With its substantial benefits, the radar sensors will play a key role in driving safety in the upcoming years.

1.3 Basics of the automotive radar

To assess the distance to surrounding objects, the radar sensor must be able to generate and transmit a high frequency signal, and then must be able to receive the reflected signal and to perform its analysis. The Figure 1-2 is a simplified block diagram of an automotive radar transceiver showing the required functions.

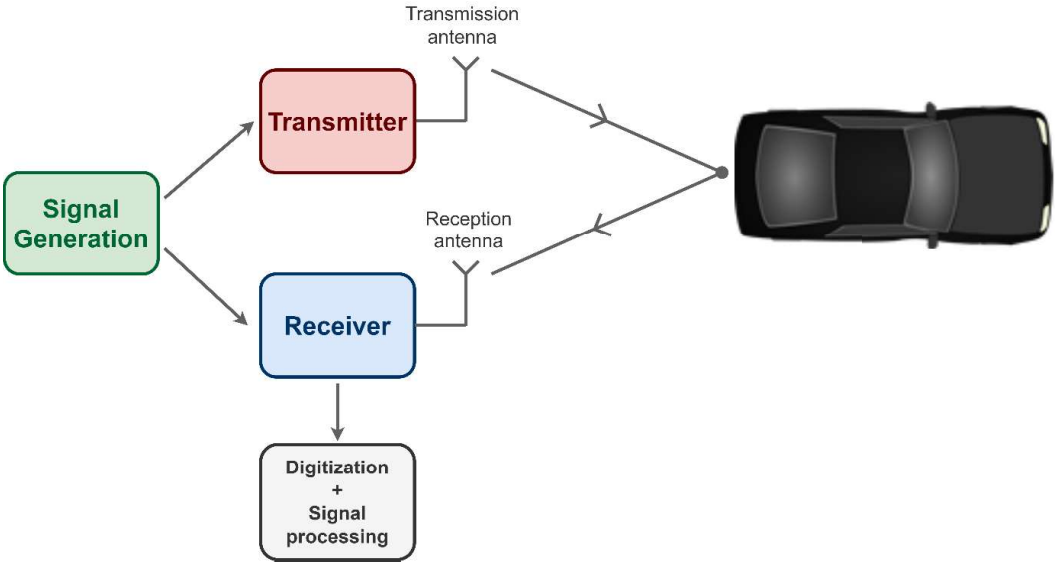

Figure 1-2: Simplified block diagram of an automotive radar transceiver.

A radar transceiver includes an oscillator to generate a high-frequency signal which is amplified by the transmitter and emitted by an antenna. Then the reflected signal is received by the reception antenna. The receiver down-converts the frequency of the received signal from millimeter-wave frequencies to a few MHz to be able to digitize this signal. The signal generated by the oscillator is also used in the receiver to perform the frequency translation. Finally, the received signal is converted into a digital information by the Analog-to-Digital Converter (ADC). The signal processing on the digital side allows the extraction of all the information required for the driving assistance.

The radar emitter also modulates the emitted signal. As a result, a radar sensor can emit different kinds of signal. The simplest signal waveforms used for radar detections are the pulsed and the continuous waveforms. The first one allows to easily calculate the target range by analysing the time of flight while the second one is suited to detect the target speed by analysing the doppler frequency shift. However, range detection using a continuous wave and speed detection using a pulsed waveform are difficult [1, p. 10 to 15]. To be able to compute the target speed and range at the same time, more elaborate modulations are needed.

1.4 The FMCW modulation

The most popular frequency modulation in automotive radars is the Frequency Modulated Continuous Wave (FMCW). This modulation based on a sine wave with a linear frequency variation versus time is described in Figure 1-3. Different patterns of frequency variation versus time can be used for FMCW, but the saw-tooth shape depicted in Figure 1-3 is the more used for automotive application [7], [8]. This figure shows the time-domain transient waveform of the modulated carrier as well as the frequency shift over time. The FMCW modulation is very simple compared to the modulation used in communication systems and allows to easily compute the target speed and range at the same time. Figure 1-3 (b) shows the frequency variation versus time for both emitted and received modulated signals.

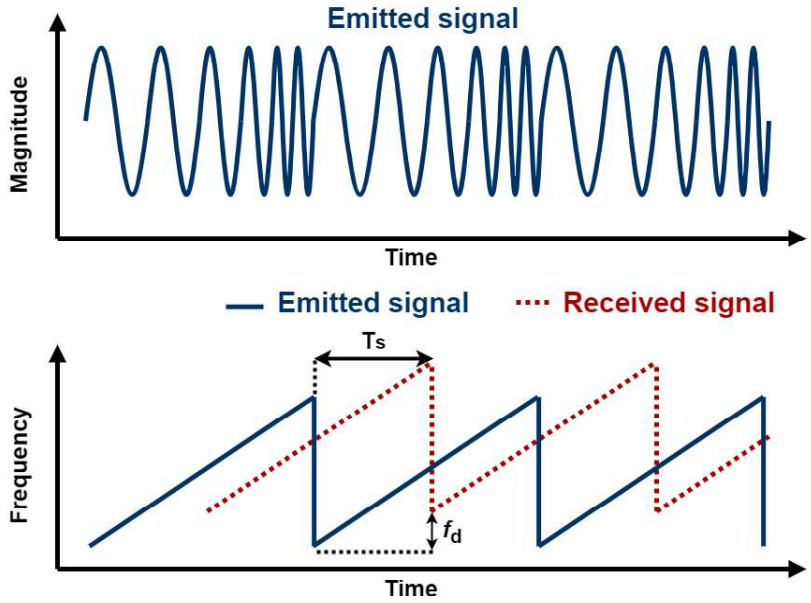

Figure 1-3: Magnitude and frequency variations over time of sawtooth shaped FMCW signal

The comparison of the two signals gives access to the time between the emitted and received modulation patterns T_s and to the Doppler frequency shift f_d. The information on T_s allows to compute the target distance while the f_d gives access to the target speed [1, p. 14]. When several receivers are implemented in a radar module, comparing the phase shift between the signal received by each receiver allows to compute the direction of the target [9].

Considering a FMCW modulation with a linear frequency variation between f_1 and f_2, the modulation bandwidth (B) is f_1 - f_2 and the modulated carrier (f_c) is (f_1 - f_2)/2. In a FMCW modulation the range resolution is proportional to $1/B$ while the speed resolution is proportional to $1/f_c$ [1, p. 14],[7], [8]. As a result, a high frequency carrier associated to a wide modulation bandwidth is required to provide an accurate radar detection.

1.5 Frequency band allocation

As previously stated, the FMCW modulation principle requires a high modulation carrier frequency and a large bandwidth to benefit from a high accuracy. Furthermore, the radar transceivers must emit in unlicensed frequency bands to avoid interferences with communication devices. The organizations in charge of the frequency allocation in Europe and USA respectively the European Telecommunications Standards Institute (ETSI) and the

Federal Communications Commission (FCC), have dedicated a specific band for automotive radar application. This frequency band is located between 76 GHz and 81 GHz [10]. As efficient and cost-effective integrated circuits design was difficult to achieve at such high frequencies until recently, the FCC and ETSI had allocated temporary frequency bands around 24 GHz to let enough time to manufacturers to get proper 77 GHz radar transceivers. Nowadays, the development of 77 GHz radar products is well mastered and the 24 GHz frequency band will not be available after the first quarter of 2022. The definitive spectrum allocated to automotive radars is depicted in Figure 1-4.

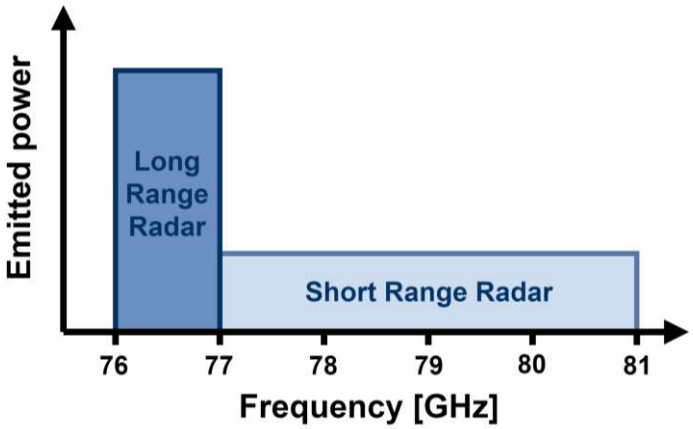

Figure 1-4: Allocated frequency spectrum for automotive radar.

The 76-81 GHz automotive radar frequency band is divided in two parts with different specifications. The first one between 76 GHz and 77 GHz is dedicated to the long-range radar which is in front of the car for adaptive cruise control. In this frequency band an important emitted power is allowed to be able to reach distant targets thus providing a high detection range (up to 250m) [1, p. 18]. The band between 77 GHz and 81 GHz is dedicated to the short-range radar which does not need high power to cover a short range (<30m) but requires a large bandwidth to reach a fine range resolution.

As a conclusion, the unlicensed band around 77 GHz allocated to automotive radar application appears as an ideal choice providing a fine accuracy detection thanks to an high frequency carrier and a large modulation bandwidth. Nevertheless, using a such high frequency is also a challenge for circuit designers who must face stringent requirements especially on the receiver front-end (LNA+mixer). The next sections will describe the 77 GHz radar receiver architecture and the associated design constraints.

1.6 Automotive radar receiver architecture

As previously stated, the role of the radar receiver is to convert an RF frequency received by the antenna around 77 GHz to a low enough Intermediate Frequency (IF) (a few MHz) to enable the signal digitization by an ADC. The different functions needed in a conventional radar receiver architecture serving this purpose are described in the Figure 1-5.

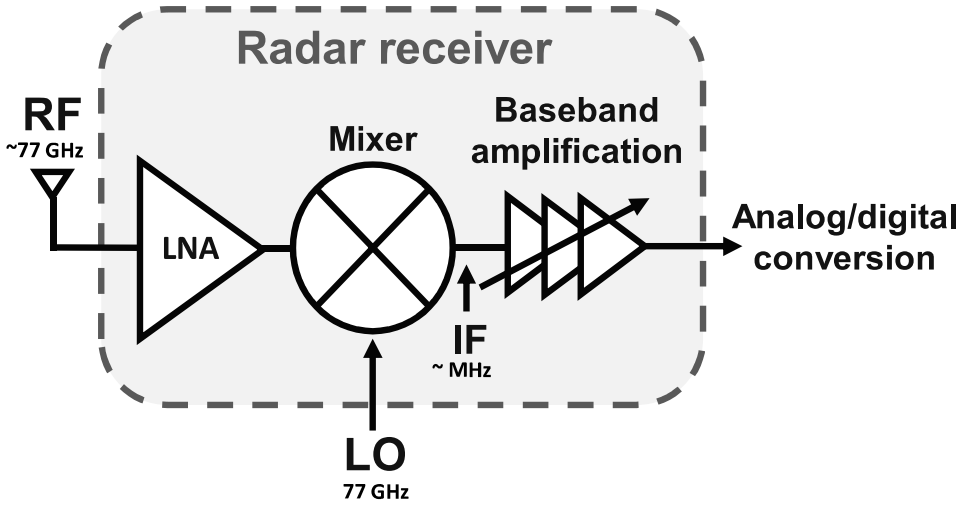

Figure 1-5: Conventional Radar receiver architecture.

The first stage of a radar receiver is generally a Low Noise Amplifier (LNA) which amplifies the weak received signal without degrading too much the Signal to Noise Ratio (SNR). Then the mixer down-converts the received RF signal around 77 GHz to a few MHz one by using the 77 GHz signal from the Local Oscillator (LO). After the frequency conversion, the signal centered at the IF frequency is amplified by Variable Gain Amplifiers (VGA) to ensure a voltage swing of constant magnitude at the input to the ADC.

1.7 Requirements on the receiver design

To ensure driving safety, 77 GHz radar receivers must be able to detect distant targets without being too sensitive to multiple signal reflections. Origins of the performance requirements for the radar receiver noise and linearity are illustrated in Figure 1-6.

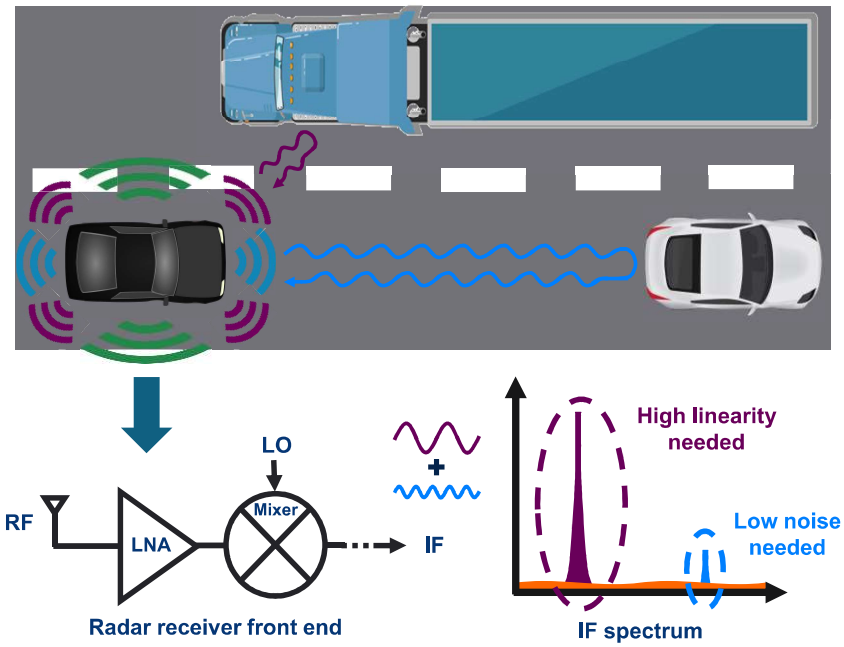

Figure 1-6: Illustration of performance requirements for automotive radar receivers.

The power reflected by a distant target (the car in Figure 1-6) is generally very weak and can be too close to the receiver noise floor to be properly detected. As a result, a too high Noise Figure (NF) in a radar receiver will limit its ability to detect distant targets.

On the other hand, a signal reflected by a close target or a large vehicle (a truck in Figure 1-6) is resulting in an important power level at the receiver input. If the receiver is not linear enough, harmonics due to the distortion or intermodulation products with other reflected signals can be generated. Because the differentiation between these parasitic spurious and signals related with distant targets (the car in Figure 1-6), can be difficult, the non-linearity of the receiver can lead to wrong detections.

Thus, the most important metrics in a radar receiver are the NF representing the receiver ability to keep a good SNR and the 1-dB Input Compression Power (ICP1dB) traducing the receiver linearity. Nevertheless, a good NF is not easily compatible with a high ICP1dB. The mixer, with its highly non-linear behavior, is the main limiting stage regarding the receiver linearity. As a result, a high-gain LNA improves noise performances but also degrades linearity, as the mixer is exposed to higher voltage swing for the same power received by the antenna. On the other hand, limiting the LNA gain enhances the linearity, but in agreement

with the Friis theorem, noise contributions of the blocks following the mixer (VGA, Filter, ADC) are increased.

As a conclusion, the balance in gain repartition in the different stages is the key to find the best trade-off between noise and linearity, while preserving cost (area) and power consumption. The analysis of existing CMOS radar receivers coming later in this chapter will give a detailed illustration of this aspect. The mixer linearity, which can force to limit the LNA gain, is essential in the overall chain performance. Consequently, it is the main topic addressed in this manuscript.

1.8 Evolution in automotive radar

First works on 77 GHz automotive radars were reported between 1995 and 2000. At that time, only III-V technologies were efficient enough to address such high frequencies. Consequently, the first reported integrated transceivers for 77 GHz radar applications were manufactured using Ga-As processes [11].

Some years later, the increase in the performances of SiGe processes became good candidates to design millimeter-wave integrated circuits. With lower production costs, silicon processes were more appropriate than III-V processes for consumer applications. First SiGe BiCMOS circuits for automotive radar have been published around 2005 [12]–[14]. Then, these processes were selected to manufacture the first 77 GHz radar products.

As already stated, the first generation of cars integrating 77 GHz radar only included a few radar sensors. More radar sensors and a more advanced signal processing will be required in the upcoming years to cover every angle around the car and enable a semi-automated driving. The analysis performed in [15] shows that CMOS technologies, while offering too poor millimeter-wave performances in the early 2000s, have been continuously scaled down to finally reach high enough transition frequencies (f_t) to allow 77 GHz circuits design. With a better circuit integration and lower production costs, CMOS processes seem now far more appropriated than BiCMOS technologies to design the next generation of 77 GHz radar transceivers. CMOS processes will enable the Radar sensor multiplication in a car without

leading to prohibitive costs. It will also make easier the signal processing co-integration with the transceiver.

1.9 28-nm FD-SOI CMOS technology description

The 28-nm FD-SOI technology developed by STMicroelectronics has been selected for this work. This process offers Fully Depleted Silicon On Insulator (FD-SOI) CMOS transistors with a 28-nm minimum transistor gate length. With nm-scaled CMOS transistors benefiting from f_t and f_{max} higher than 300 GHz this technology is well suited for low power millimeter-wave frequencies integrated circuits design [16].

1.9.1 FD-SOI CMOS transistor

The main specificity of this technology is the FD-SOI CMOS transistor. A cross section of a FD-SOI CMOS transistors is described in Figure 1-7.

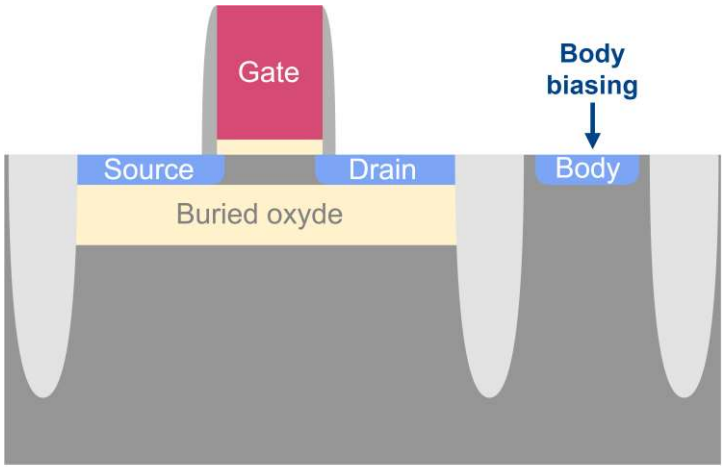

Figure 1-7: FD-SOI CMOS transistor cross section.

In FD-SOI technologies, the ultra-thin buried oxide layer (25-nm) present under the CMOS transistor channel offers many benefits. The manufacturing process is simpler than a conventional bulk process as fewer masks are required [16]. The electrical performances are also improved. As the transistor channel is insulated with this buried oxide, current leakages are reduced and the electrostatic channel control becomes easier.

An important feature resulting from the channel insulation by the buried oxide is the body biasing. In a conventional bulk process, there is not much flexibility to set the transistors body voltage. For a PMOS on a bulk substrate, V_{body} must remain above Drain and Source voltages, to keep Drain-to-body diode reverse-biased. This is generally achieved by either connecting body to V_{DD} or to Source. For the NMOS, unless the transistor is insulated by a triple well, the body is tied to bulk and thus to ground. In FD-SOI technologies, a voltage can be applied under the transistor channel (Figure 1-7) to provide an additional channel control. This way, the body access acts as a second gate at the back of the transistor channel. As a result, applying a voltage to the transistor body allows to change the transistor threshold voltage (V_{th}). The insulation of the conducting channel also makes possible to use N or P type doping below the transistor leading to different nominal V_{th} values. This principle is used in the 28FDSOI technology to propose 4 different CMOS transistor "flavours" [16] as described in Figure 1-8.

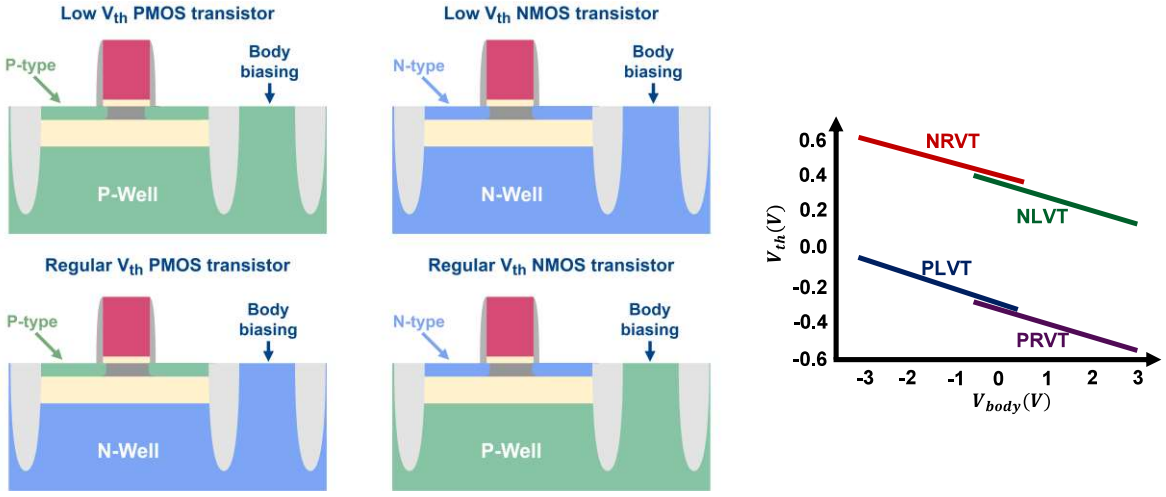

Figure 1-8: different transistor flavours proposed in 28FDSOI and their Body-bias characteristic.

As described Figure 1-8 using the same type of doping for the conducting channel and under the box offers CMOS transistors with low nominal V_{th} value (NLVT and PLVT). Moreover, using the opposite doping leads to CMOS transistors with regular V_{th} nominal value (NRVT and PRVT). These different configurations offer four transistor flavours. For each transistor type, the V_{th} value can be tuned around the nominal value with the body biasing by setting the voltage applied to the hybrid zone (V_{body}). This technology exhibits a quite high body factor (~85 mV/V) enabling a large V_{th} tuning range. This body biasing capability in FD-SOI technologies provides new design opportunities by controlling the CMOS transistors V_{th}.

The high-speed CMOS transistors have a thin gate oxide and operate under a nominal V_{DD} value around 1V. The 28FDSOI process also offer LVT and RVT CMOS transistors with a thick gate oxide able to operate under 1.5 V or 1.8 V nominal V_{DD} value. Nevertheless, thick gate oxide transistors exhibit lower f_t and f_{max}.

1.9.2 Metal stack

The 28FDSOI technology provides different metal stack configurations. The selected configuration is described in Figure 1-9.

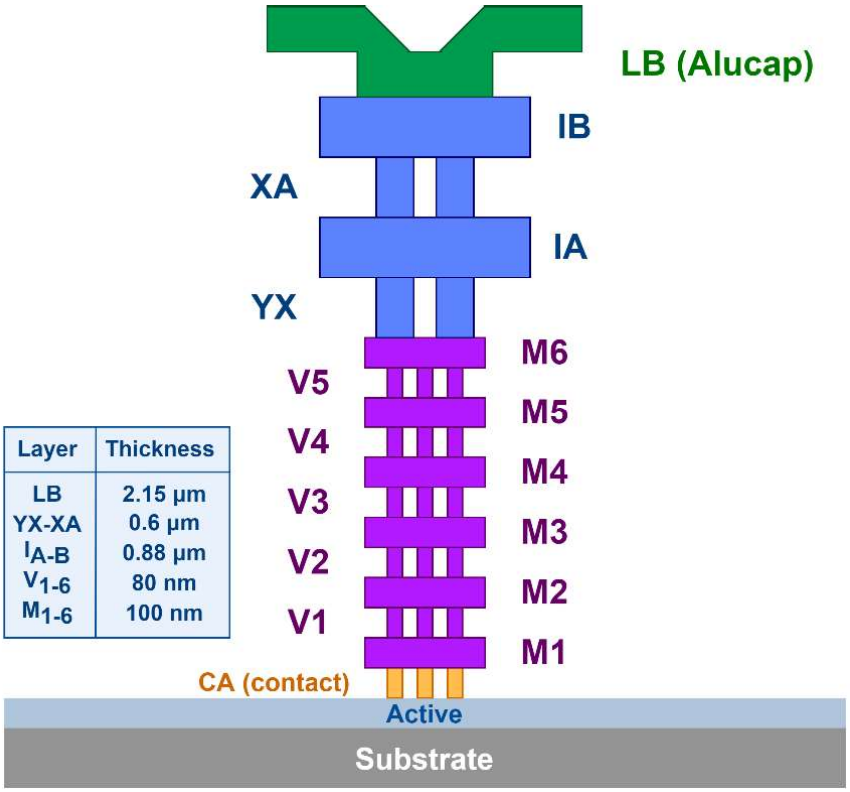

Figure 1-9: 28FDSOI 8 metal levels stack.

The metal stack includes 8 metal layers and an "Alucap" top level. The metal layers M_1 to M_6 are quite thin (100 nm) and are often used for active components routing. Thicker metallization are available from the top metal layers (IA and IB) with the alucap LB. They are used for passive structures such as inductances or transmission lines as they are less resistive than underneath layers. These higher levels are also less sensitive to parasitic coupling to the ground plane or substrate.

1.9.3 Passive components

MIM and MOM capacitors are available for RF designs with the 28FDSOI technology. The MIM capacitors are located between the two thick metal layer (IA and IB) and show a capacitance density around 20 fF/µm². The MOM capacitors are implemented from metal layers M_1 to M_6 and offer a capacitance density around 6 fF/µm². As the MIM capacitors option requires additional masks, MOM capacitors with an RF compliant layout should be preferred for low-cost RF design.

The 28FDSOI also provides different kinds of resistors. A P+ doping poly-silicon resistor with a 439 Ω/square density is preferred for RF design as it lead to the best RF performances.

1.10 77 GHz radar receiver architectures

Many different architectures of millimeter-wave receiver front-ends related to 77 GHz CMOS radar receivers have been published so far in the literature. The main differences between existing solutions come from the mixer topology used to down-convert the 77 GHz RF signal. Since the choice made in the mixer topology have a strong impact on the overall receiver design, the main existing configurations are discussed and compared in this section. The goal is to find the more suitable architecture to design a 77 GHz radar receiver in a 28-nm FD-SOI CMOS technology.

1.10.1 Radar receivers based on active mixers

First silicon 77 GHz radar receivers were manufactured with SiGe BiCMOS processes benefiting from the high transition frequency and high breakdown voltage of Hetero-junction Bipolar Transistors (HBT). The more spread 77 GHz BiCMOS receiver architecture is based on the Gilbert Cell [17] described in Figure 1-10.

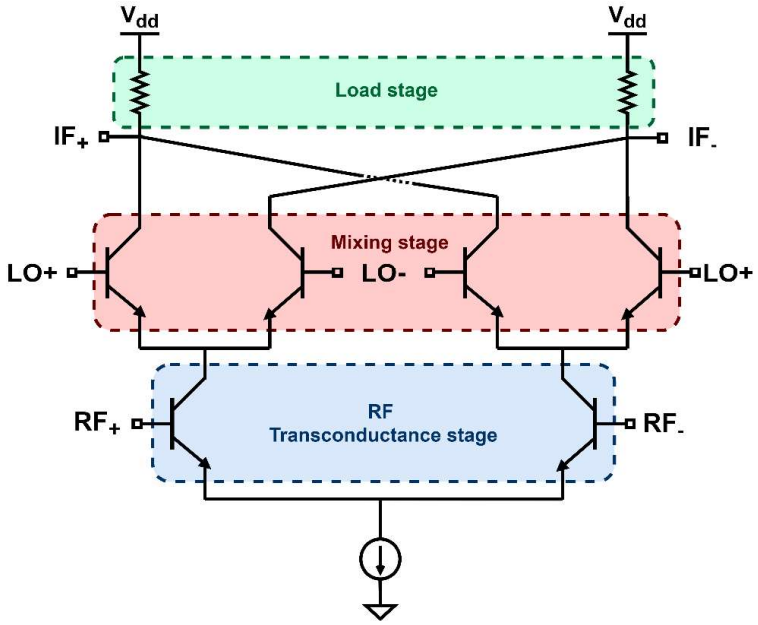

Figure 1-10: Conventional double-balanced Gilbert cell.

The gilbert cell is an active mixer topology stacking a differential RF transconductance amplifier and a double-balanced mixing stage loaded by resistors thus allowing to design extremely compact mixers. In the Gilbert cell, some conversion gain is provided by the RF transconductance and resistors. Therefore, this kind of mixer does not always require a LNA. The main drawback of the gilbert cell is the linearity which remains limited by two factors. The first contributor to the linearity degradation in Gilbert cells is the RF transconductance stage as the HBT differential pair can handle a very limited input voltage swing (a few U_t) without saturating. Furthermore, using three vertical stages (transconductance, mixing cell and loads) results in a low voltage headroom for each stage thus restraining the output voltage swing.

The conventional Gilbert cells is implemented in the first generation of BiCMOS 77 GHz receiver demonstrator as in [18]. In this work, the proposed mixer operates under a 2.5 V supply showing a good trade-off between noise and linearity. Nevertheless, the work in [19]–[21] demonstrates a better linearity by using a folded topology or removing the RF transconductance of the Gilbert cell. This approach seems to be the most suitable for the design of BiCMOS 77 GHz radar receivers and lead to very high performances on the noise/linearity trade-off in [19]–[21].

As architectures based on active mixers translates into high performances with BiCMOS processes, active topologies have been firstly implemented in 77 GHz CMOS receiver test chips. The Table 1-2 summarizes the performances of the existing CMOS radar receivers relying on active mixers ([22]–[26]) and compares them to their BiCMOS counterpart.

Table 1-2: performances of Gilbert-cell-based 77 GHz receiver front-ends in silicon technologies.

Ref	**Tech**	**Topology**	**Gain [dB]**	**ICP1dB [dBm]**	NF_{SSB} **[dB]**	V_{DD} **[V]**	P_{dc} **[mW]**
[18]	130-nm BiCMOS	Gilbert cell	15	-13	13.8	2.5	335
[19]	130-nm BiCMOS	Gilbert cell mixing stage only	16	-2	11-12	3.3	200
[21]	180-nm BiCMOS	Folded Gilbert cell	21.5	-5	10.8	3.3	70
[22]	65-nm CMOS	Gilbert cell	11.8	-18*	12.9	1.2	8
[23]	28-nm CMOS	2-stage LNA + Gilbert cell mixing stage	18 (LNA) 2 (mixer)	-30*	12	NA	68
[24]	65-nm CMOS	3-stage LNA + folded Gilbert cell	31.6 (Rx) 5 (mixer)	-37 (Rx) -20* (mixer)	8.8	1	61
[25]	65-nm CMOS	3-stage LNA + folded Gilbert cell	11	-15	8	1	22
[26]	65-nm CMOS	3-stage LNA (Tunable gain) + Gilbert cell mixing stage	18/66 (Rx) 4 (Mixer)	-7/-31	26/11	1	31

*estimated

Compared to the HBT of the SiGe processes the CMOS transistors have a lower voltage handling capabilities and lower g_m at high frequencies. Therefore, the comparison between the work in [22]–[26] and 77 GHz BiCMOS Gilbert cells highlights that a satisfying trade-off between noise and linearity cannot be reached with CMOS receivers based on active mixers. As a result, CMOS active mixers do not appear as the right choice for 77 GHz radar receiver.

1.10.2 Radar receivers based on passive mixers

Even if CMOS transistors are not as efficient as HBT for active mixer topologies, they perform very well as switches. As a result, double-balanced passive mixers using four cold-biased CMOS transistors operating as switches are widespread in CMOS receiver design. Furthermore, CMOS processes scaling down drastically improves the performances of the CMOS switches. As the channel ON-state resistor r_{on} of the transistor is proportional to the W/L ratio while the gate capacitance is proportional to W×L, decreasing L while keeping the same r_{on} results in a significantly lower gate capacitance. Reducing the gate capacitance improves the CMOS switches performance by allowing the transistors to quickly switch between ON and OFF states.

Passive mixers are chosen for their good linearity and zero DC power consumption. Since the passive mixers high linearity allows to implement more gain on the LNA while keeping a suitable ICP1dB for the radar application, they appear as a good alternative to active mixers regarding noise performances of the receiver. Furthermore, as no DC current passes through the mixing transistors, passive mixers are also less sensitive to the $1/f$ noise than active mixers. On the other hand, passive mixers bring significant conversion losses thus requiring a LNA at the receiver input to avoid a receiver NF degradation.

Passive mixers can be used in voltage or current mode depending on LNA and baseband amplifier topologies. Both operating modes are presented here below. When the passive mixer is implemented in a receiver between a low noise RF amplifier and an IF amplifier (IFA) showing respectively a low output impedance and a high input impedance (Voltage amplifier), the mixer operates in voltage mode (Figure 1-11).

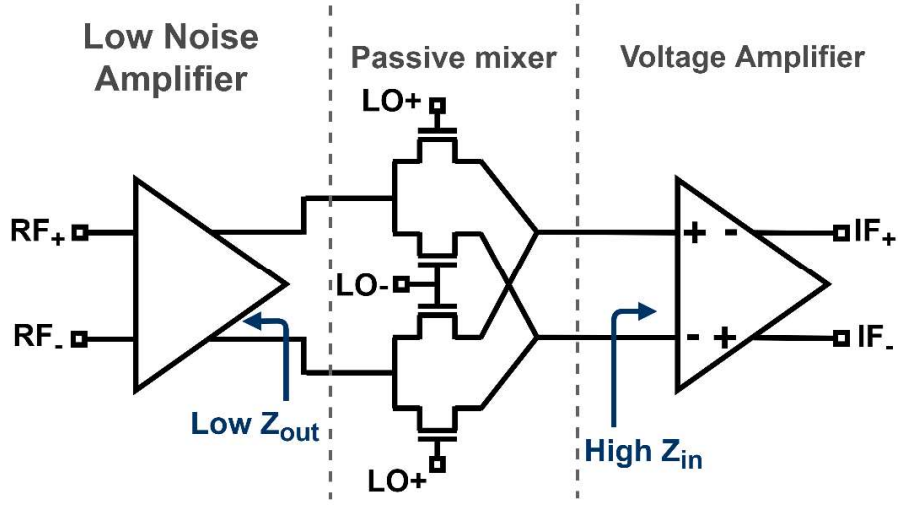

Figure 1-11: Receiver architecture based on a voltage mode passive mixer.

When the same passive mixer is implemented between a RF low noise transconductance amplifier (LNTA) and an IF transimpedance amplifier (TIA) the input RF voltage is turned into a current by the first stage, passes through the mixer and is converted back to a voltage by the IF TIA. This operating principle is described in Figure 1-12 and is called current mode. A proper current transfer in the mixer requires a high output impedance for the RF LNTA while the IF TIA must present a low input impedance.

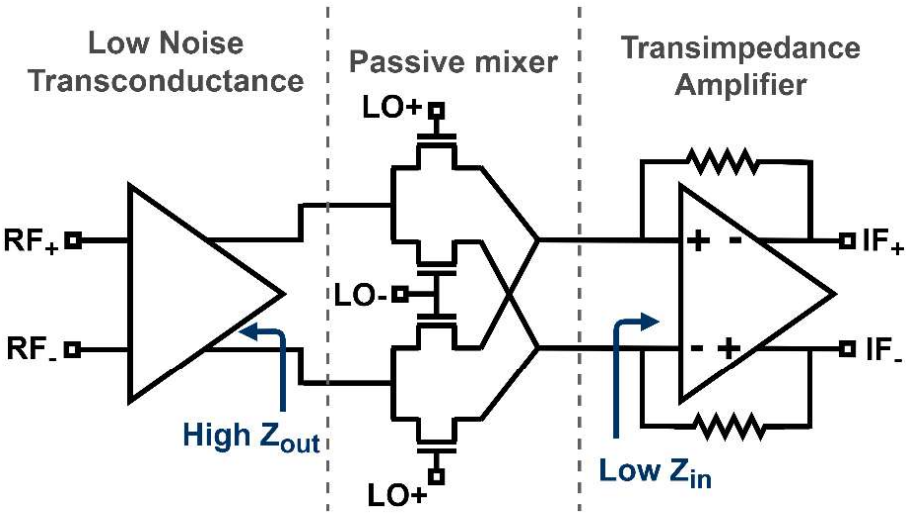

Figure 1-12: Receiver architecture based on a current mode passive mixer.

Both operating modes have strengths and weaknesses. In the voltage mode mixer, the condition for maximizing the voltage transfer and thus the conversion gain is:

$$|Z_{out_{LNA}}| + r_{on} \ll Z_{in_{IFA}} \quad (1\text{-}1)$$

This requirement is quite easy to fulfil as the IFA input impedance is in the range of tens of kΩ. For the current mode mixer, the condition to ensure a good current transfer through the mixer is:

$$|Z_{out_{LNTA}}| \gg r_{on} + |Z_{in_{TIA}}| \quad (1\text{-}2)$$

This requirement is harder to fulfil because a low r_{on} requires a large mixing transistor which can be hard to drive. In addition, a low TIA input impedance is hard to reach above a few MHz. Not meeting this requirement would results in extra conversion losses. On the other hand, using current rather than voltage in a millimeter-wave receiver can be very helpful to deal with the low supply voltage of the nm-scaled CMOS process. As using a current mode mixer results in a low voltage swing at the input of the mixer, the RF transconductance is less sensitive to voltage saturation coming with the low voltage supply. The low voltage swing at the input and output of the mixer also keeps the mixing transistor V_{DS} close to 0 V increasing the mixer linearity.

Both operating modes are present in the literature related to 77 GHz radar receivers. Receivers in [27], [28] rely on current mode passive mixers an exhibit excellent trade-offs between noise and linearity. In [27] a 1-stage LNA is used rather than a 2-stage LNA (as done in [28]) leading to a lower front-end gain. The reduced front-end gain is compensated by the higher gain of the IF TIA operating under a high voltage supply (1.8V vs 0.8V for RF blocks) to preserve the overall linearity. This strategy allows to reach a better ICP1dB at the cost of a higher NF. Voltage mode passive mixers are developed in [8] and [29] also showing a high linearity and a good NF. The work in [29] push the strategy used in [27] further by removing the LNA to propose a passive mixer first receiver showing an excellent linearity with a low NF. References [8], [27]–[29] present the best published 77 GHz CMOS radar receivers when considering the trade-off between noise and linearity. The performances of the receiver front-ends presented in this section are summarized in the following table:

Table 1-3: performances of passive mixer-based 77 GHz CMOS receiver front-ends.

Ref	Tech	Topology	Gain [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	V_{DD} [V]	P_{dc} [mW]
[28]	40-nm CMOS	LNTA + current mode passive mixer + TIA	17	-7.4	8.7	1.8	NA
[8]	65-nm CMOS	LNA + voltage mode passive mixer + IFA	26.2	-8.5	15.3	1	78
[27]	22-nm FD-SOI	Common gate LNA + current mode passive mixer + TIA	16	-3.5	12.8	0.8/1.8 (RF/Baseband)	NA
[29]	28-nm CMOS	Voltage mode passive mixer first + IFA	15	-5	9	1.8	100

As passive mixers exhibit conversion losses, they are generally implemented with a LNA and/or an IFA in a whole front-end, whereas the Gilbert cell can be used in a standalone configuration. Therefore, standalone passive mixers are not represented in the publications related to the 77 GHz radar application making their performances hard to assess. Nevertheless, the performances of the 77GHz CMOS receivers reported in Table 1-3 demonstrate that using a passive mixer to design a 77 GHz radar receiver with nm-scaled CMOS processes appears as the right choice. As passive mixers rely on the CMOS transistor switching behaviour, which is the strength of nm-scaled CMOS processes, this approach allows to take the best from those technologies. It can be noticed that using a low front-end gain is the key to get a good linearity. If this gain is not high enough to prevent a too high noise contribution from the baseband VGA, an IF amplifier with a moderate NF can be used to compensate the low front-end gain. As CMOS processes generally offer thick gate oxide CMOS transistors with a higher breakdown voltage than RF transistors at the cost of a lower f_t the IF amplifier can operate on a higher voltage supply than for RF blocks as in [27]. This way, more gain can be introduced before the VGA without degrading the ICP1dB. This approach combined with the use of passive mixers seems to be the best way to design a high performances CMOS radar receiver.

1.10.3 Radar receivers based on sub-harmonic mixers

All receiver architectures presented in previous sections are using a 77 GHz LO signal to drive the mixer. Implementing a 77 GHz Voltage Controlled Oscillator (VCO) is not the preferred solution for radar systems, because of the difficulties to design the VCO itself. Conventional radar architectures use a 38.5 GHz VCO followed by a frequency doubler and high consumption 77 GHz drivers ([26], [28]). Sometimes higher frequency multiplication factors as a tripler in [27] or a sextupler in [24] are implemented to relax the design complexity of the VCO and LO distribution chain. At the scale of a full radar chip including several receivers, this approach is a bit complex and results in extra power consumption and circuit area, as frequency multipliers rely on active blocks (push-push structures or equivalent) followed by LC tanks. The use of sub-harmonic mixers, using a LO frequency submultiple of the RF frequency ($f_{LO} \approx f_{RF}/n$, with n a natural integer), opens the way to get rid of multipliers. This solution has already been considered for the first generations of 77 GHz CMOS radar receivers ([30], [31]). The performances of the sub-harmonic receivers in [30], [31] are summarized in the following table:

Table 1-4: performances of sub-harmonic mixer-based 77 GHz CMOS receiver.

Ref	Tech	f_{RF}/f_{LO} [GHz]	Topology	Gain [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	V_{DD} [V]	P_{dc} [mW]
[30]	65 nm CMOS	78 / 39	5-stage LNA + ×2 sub-harmonic Gilbert cell mixing stage	16 (Rx) 6.2 (Mixer)	-20 (Rx) -10.2*(mixer)	13	1.2	28.5
[31]	65 nm CMOS	78 / 39	2-stage LNA + ×2 sub-harmonic folded Gilbert cell	14.5 (Rx) 2 (Mixer)	-16.2 (Mixer) -28 (Rx)	10.5	1.5	57

*estimated

[30], [31] are the only existing works on 77 GHz CMOS sub-harmonic receivers. They are both based on ×2 CMOS sub-harmonic Gilbert cells which show limited performances compared to conventional solutions. However, the prospect of a simpler LO chain for 77 GHz radar transceiver let this approach appear as promising. Therefore, 77 GHz sub-harmonic receiver architectures will be considered in the chapter 3.

1.11 Conclusion

The main existing solutions for a 77 GHz radar receiver architecture have been discussed in this section. This discussion highlights that even if receivers based on active Gilbert cells show very good performances with BiCMOS technologies, active mixers are not suited for advanced CMOS technologies. On the other hands, CMOS passive mixers take advantages of the strength of CMOS processes leading to far better performances. Therefore, using passive mixer topologies appears as the best solution to design a 77 GHz radar receiver in 28-nm FD-SOI CMOS technology. The literature related to 77 GHz radar receivers also puts forward that a sub-harmonic mixer-based architecture is a solution to reduce the burden of the LO distribution chain in term of area and consumption. This solution thus proposes a better Noise/Linearity/Consumption/Area trade-off. This promising approach has not demonstrated state of the art performances yet but we strongly believed that, associated to an optimal mixer design, it can be the right choice for radar architectures. The purpose of this thesis is to demonstrate this statement.

Chapter 2 Design of a 77 GHz sampling passive mixer in 28-nm FD-SOI CMOS technology

2.1 Introduction

The state of the art presented in the previous chapter highlights that high performances are reached with passive mixers that provide high linearity and zero DC consumption [8], [27], [28]. The discussion on the noise/linearity trade-off in radar receivers (chapter 1) also puts forward that, as their high linearity allows to implement more gain on the LNA while keeping a good ICP1dB, they are also a good alternative to active mixers from the noise point of view. As these topologies rely on cold CMOS transistors used as switches, they allow to take the best from the recent nm-scaled CMOS processes. Thus, using passive mixers in a 28FDSOI radar receiver at 77 GHz appears as the best solution. First, this chapter presents the conventional CMOS voltage passive mixers operating principle highlighting their benefits and drawbacks. Then a new 77 GHz sampling mixer topology showing better performances is proposed. The aim of this chapter is to present a new solution enabling the use of sampling mixers at millimeter-wave frequencies. This solution is integrated in a 28FDSOI technology for an experimental validation of reachable performances.

2.2 Conventional CMOS passive mixers

As previously stated, CMOS passive mixers are well suited to design highly linear receivers with low power consumption. As, they use cold CMOS transistors, they are also particularly appropriated to nm-scaled CMOS processes, like 28FDSOI, because transistors of these technologies can behave as very good switches. The following section will introduce the operating principle of the conventional CMOS passive mixer and put forward its strengths and weaknesses.

2.2.1 Operating principle

As discussed in the chapter 1, the conventional CMOS passive mixer can operate in current mode [27], [28] or voltage mode [8] depending on the impedance presented by the previous and following stages. This thesis focuses on sampling passive mixers relying a hold capacitor to store a sampled voltage value at the output of a voltage mode mixer. Therefore, the current mode passive mixer operating principle will not be detailed here-after.

The principle of a conventional double-balanced voltage mode CMOS passive mixer is depicted in Figure 2-1. When compared to its single ended counterpart, it can be noticed that the double-balanced topology provides a good harmonic rejection and translates into a better conversion gain [32], [33, Ch. 6].

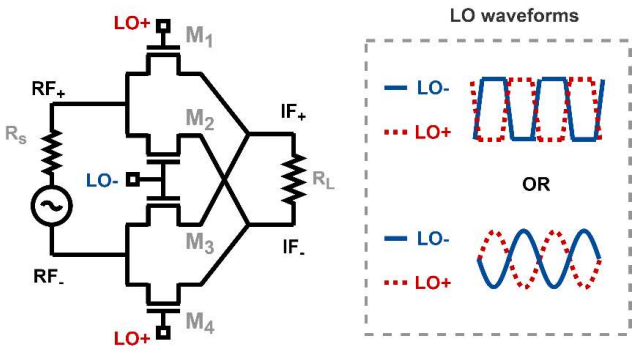

Figure 2-1: Conventional voltage double-balanced passive mixer.

As the high load impedance R_L results into a high mixer input impedance ($\approx R_L$) the voltage transfer from an input voltage source with R_S far lower than Z_{in} is maximised. The mixer is acting as a proper voltage conveyor. The conventional voltage passive mixer is usually driven by a sinusoidal local oscillator waveform or a 50% duty cycle square wave [32], as described in Figure 2-1. The shape of the LO signal is depending on frequencies. It can be square when LO frequency is low enough, whereas it can be only sinusoidal at high LO frequency. In these conditions, the mixer output voltage is V_{RF} (RF_+ - RF_-) in the first half of the LO period and -V_{RF} in the other half. The result is the conversion of the input signal at RF frequency to the output one at the Intermediate Frequency. The voltage conversion Gain (G_{cv}), linearity and noise figure NF of a conventional passive mixer will be discussed in the following sections.

2.2.2 Passive mixer conversion gain

Considering all mixing CMOS transistors $M_{1,2,3,4}$ as voltage-controlled switches, with a r_{on} ON-state resistance, the voltage conversion gain of the passive mixer of Figure 2-1 is [32]:

$$G_{Cv} = \frac{2}{\pi}.\frac{R_L}{R_L + r_{on} + R_s} \tag{2-1}$$

The theorical maximum value of this conversion gain G_{cv} is reached for an ideal voltage matching (R_s far lower than Z_{in} and r_{on} far lower than R_L) and is equal to $2/\pi$ (≈ -4 dB).

2.2.3 Noise in passive mixer

The main noise contributor in CMOS passive mixer is the thermal noise in the channel of the mixing transistors. The r_{on} ON-state resistance produces thermal noise which is converted to the mixer output. For this kind of mixer, the output voltage noise spectral density is [34]:

$$V_{n_{th}}^2 = 8KTr_{on} \tag{2-2}$$

In (2-2) K is the Boltzmann constant and T the ambient temperature. This result is easily understandable because a conventional CMOS passive mixer is driven by a 50% duty cycle LO waveform, and there is always a conductive path with two series r_{on} between the input and the output.

The second important noise contribution is inherent to mixer principle. As the mixer converts RF signals from $f_{LO} \pm f_{IF}$ to f_{IF}, the noise in both RF frequency bands is added a f_{IF}.

If we consider that the conversion gain is the same for both bands, the input noise is doubled when only one input frequency band is used.

Taking into account these contributions, the voltage passive mixer Single Side-Band Noise Figure (NF_{SSB}) is:

$$NF_{SSB} = \frac{{V_{nmix}}^2}{4KTR_s.G_{Cv}^2.\alpha^2} \qquad with\ \alpha = \left|\frac{Z_{in}}{Z_{in} + R_s}\right| \tag{2-3}$$

$$NF_{SSB} = \frac{8KTr_{on} + 2.(4KTR_s.G_{Cv}^2.\alpha^2)}{4KTR_s.G_{Cv}^2.\alpha^2} = 2 + \frac{8KTr_{on}}{4KTR_s.G_{Cv}^2.\alpha^2} \tag{2-4}$$

In (2-4), G_{cv}, Z_{in} and V_{nmix} are respectively the voltage conversion gain, the input impedance and the output noise voltage of the mixer, and R_s is the series impedance of the input RF source. Expression (2-4) shows that the minimum value of NF_{SSB} is 3 dB, when the mixer is noiseless. The additional noise resulting from the mixer depends on the r_{on} resistance and the conversion gain: NF_{SSB} increases with the r_{on} and decreased with G_{cv}.

2.2.4 Passive mixer linearity

The linearity of a passive mixer depends on the switching time of mixing transistors. Fast switching from the OFF-state to the ON-state provides a good linearity [35]. As presented before (Figure 2-1), passive mixer can operate either with square or sinusoidal LO waveforms. The conversion gain stays the same for both situations. However, square LO waveforms with sharp rising and falling edges allow a faster switching, which translate into a better linearity.

2.2.5 Conventional CMOS passive mixer for millimeter-wave receivers

As discussed in chapter 1, with its 0 DC power consumption in the mixer core and high linearity, the conventional CMOS passive mixer is a good candidate to comply with the strong linearity requirement on radar receivers. Nevertheless, the low conversion gain of passive mixer is a main drawback regarding noise performances of the overall receiver. As already stated, the inherent upper limit of a passive mixer conversion gain is -4 dB, when the mixer is driven with a 50% duty cycle LO signal. Since the LNA gain is limited for receiver linearity purpose, the implementation of a passive mixer can lead to a low gain front-end. Finally, as the baseband variable gain amplifier exhibits a quite high input voltage noise [36], this low front-end gain has a strong impact on the NF of the receiver.

This issue is addressed in the next section showing how the conversion gain of the passive mixer can be improved while its good linearity is kept, by using a sampling passive mixer.

2.3 Sampling passive mixer principle

Passive mixer topologies based on the sampling principle can be considered to benefit from the advantages of passive mixer while enhancing the value of conversion gain. This section

presents the sampling down-conversion principle and its comparison with conventional passive mixer principle detailed earlier.

2.3.1 Using sampling for down-conversion

At low frequencies, the use of sampling for frequency down-conversion as in [37] is wide spread. The sample and hold circuit performing the frequency conversion relies on a switch and a capacitor as described in Figure 2-2. The switch is closed for a very short time for sampling the input voltage. Then the hold capacitor stores the sampled value while the switch is open. In an ideal sampling operation, every RF signal close to a sampling frequency harmonic ($n.f_{LO}$) is translated at an f_{IF} of $|f_{RF}-n.f_{LO}|$ by the sampling aliasing. This frequency translation is illustrated in Figure 2-2 for n = 1.

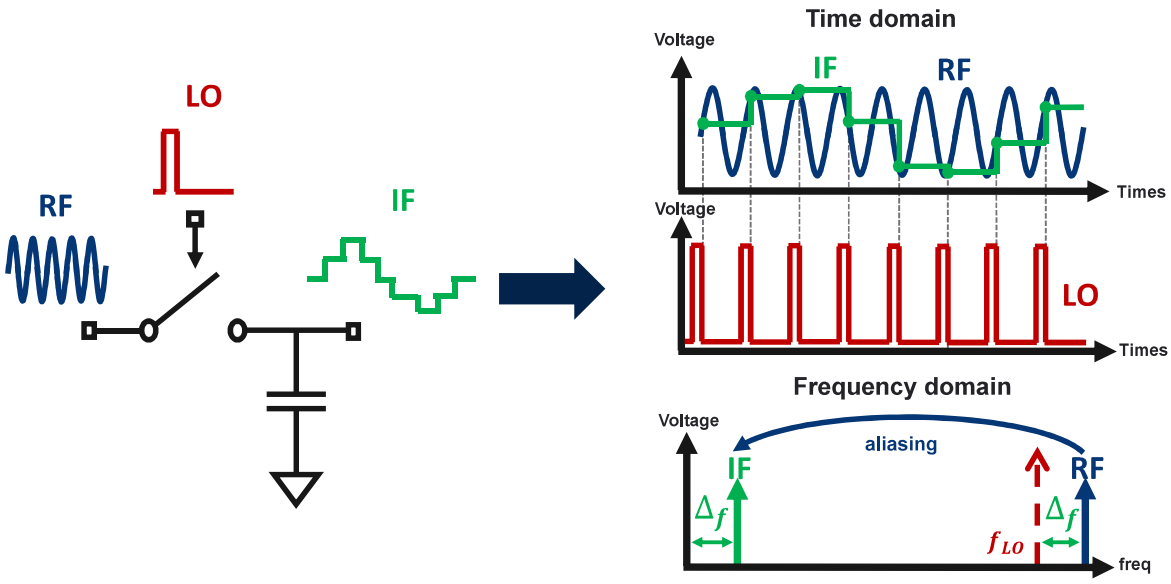

Figure 2-2: Sampling down-conversion principle.

The sampling can be interesting for down-conversion, because it allows a theoretically lossless frequency down-conversion with a LO frequency equal to f_{RF}/n close to the RF frequency (n=1) or close to an harmonic sub-multiple of the RF frequency. In this last situation, the only limitation to the frequency conversion results from the low pass filtering which is induced by the ON-state switch resistance and the hold capacitor.

2.3.2 Sampling passive mixer operating principle

The conventional passive mixer operating principle described earlier can be improved by introducing the sampling operation. This way, the conversion gain is enhanced and a sub-harmonic conversion is possible as well. In order to turn the mixer into a voltage sampler, a low duty cycle square wave must be applied as the LO signal and the IF outputs must be loaded with a capacitance. This principle is developed in a double-balanced configuration in Figure 2-3. As in a sample and hold circuit, transistors are used as switches that are closed for a very short time for sampling the input voltage. The hold capacitors C_H store the sampled values when all switches are open.

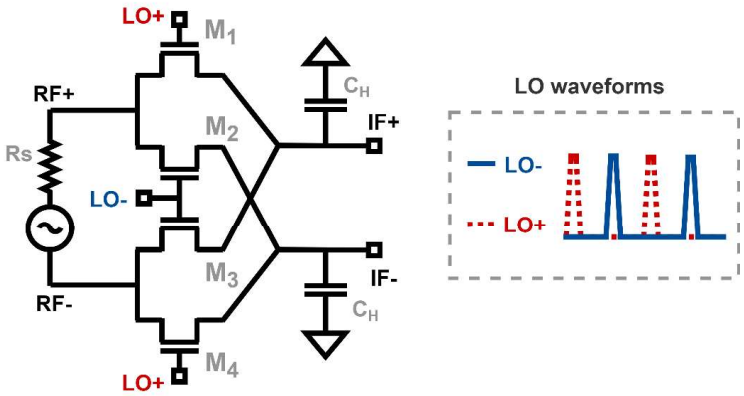

Figure 2-3: Double-balanced sampling mixer.

At IF frequencies, the mixer acts as a low-pass C_H/g_c network where g_c is the mean channel conductance of transistors $M_{1,2,3,4}$ over the LO period. Because of the passive mixer transparency regarding impedances, this network results in a high RF input impedance ([38], [39]) around each odd LO harmonics. A proper voltage conversion is enabled as soon as source impedance R_s is low enough (<< $|Z_{in}|$).

2.3.3 Sampling mixer conversion gain

With a proper input voltage source and considering that $M_{1,2,3,4}$ are conducting for a time τ_{on} equal to $D.T_{LO}$, the voltage conversion gain of a sampling mixer is calculated as:

$$G_{cv} = \frac{1}{2} sinc\left(\frac{f_{RF}}{f_{LO}}.D\right)\left(1 - e^{-j\pi\frac{f_{RF}}{f_{LO}}}\right) \quad where\ sinc(x) = \frac{sin(\pi x)}{\pi x} \qquad (2\text{-}5)$$

The gain calculation method is similar as in [40]. According to (2-5), G_{cv} increases when the duty cycle D gets lower and tends toward 1 as D tends to 0. This formula also illustrates that with double-balanced structure, only RF signals around odd LO harmonics are down converted.

The conversion gain of a fundamental sampling mixer ($n = f_{RF}/f_{LO} = 1$) for different duty cycles is illustrated in Figure 2-4. This figure shows that the $2/\pi$ conversion gain limitation of a conventional CMOS voltage passive mixer can be broken with a sampling mixer, which conversion gain can ideally reach the value of 1 for very small LO duty cycles.

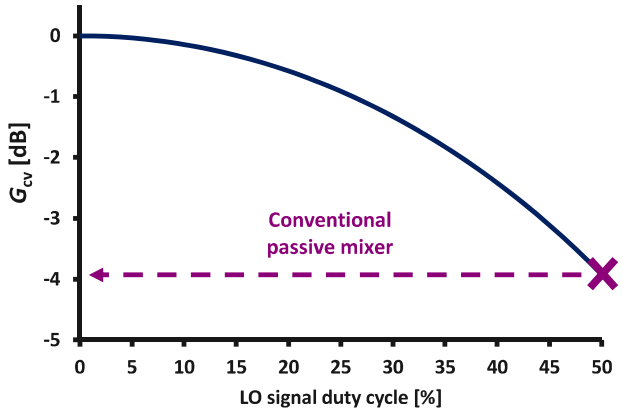

Figure 2-4: Conversion gain of a fundamental sampling mixer vs the LO signal duty cycle.

2.3.4 Noise in sampling mixer

The conversion gain around each odd LO harmonic coming with the sampling behavior has an impact on the sampling mixer noise. The main noise contributors in sampling mixers are similar as in conventional passive mixers. The input noise aliasing described in [37] and the r_{on} thermal noise of the mixing transistors converted around f_{LO} and its harmonics remain the two main noise contributions to the mixer output noise. However, as sampling mixer presents a higher conversion gain than conventional passive mixer, the output voltage noise spectral densities are different. The output voltage noise spectral density due to the input noise conversion around LO harmonics can be calculated as [41]:

$$N_{alias} = 2.\sum_{n} N_{in}(n.f_{LO}).G_{cv}^2(n.f_{LO}).\alpha^2\,(n.f_{LO}) \;\; with \;\; \alpha(n.f_{LO}) = \left|\frac{Z_{in}(n.f_{LO})}{Z_{in}(n.f_{LO}) + R_s}\right| \quad (2\text{-}6)$$

In (2-6) $N_{in}(n.f_{LO})$ represents the voltage noise spectral density at the mixer input around each LO harmonic. Each LO harmonics output noise contribution is multiplied by 2 because of the image frequency band.

To compute the output voltage noise spectral density added by the mixer, all r_{on} thermal noise conversions around LO harmonics must be added [42]:

$$N_{th_{out}} = 2.N_R.\sum_{-\infty}^{\infty} G_{cv}^2(n.f_{LO}) \quad with\ N_R = 2KTr_{on} \tag{2-7}$$

N_R is the two-sided noise spectral density of the mixing transistor r_{on} resistance. A factor 2 is added in (2-7) as the r_{on} resistance of each differential path (RF_+ and RF_-) of the double-balanced mixer must be considered. Including the G_{cv} expression of (2-5) in the calculation of the sum in (2-7) gives the following one-sided thermal noise spectral density:

$$N_{th_{out}} = \frac{4KTr_{on}}{D} \tag{2-8}$$

The calculation steps leading to this result are similar as in [42] and are given in annex. The equation (2-8) shows that the mixer thermal noise increases when the duty cycle D is decreased. This result is consistent with the increase of the conversion gain around f_{LO} and its harmonics.

If the mixer added thermal noise and the input noise conversion are only considered, the sampling mixer NF_{SSB} is:

$$NF_{SSB} = \frac{{V_{nmix}}^2}{N_{in}(f_{RF}).G_{c_v}^2(f_{RF}).\alpha(f_{RF})^2} \qquad with\ \alpha(f) = \left|\frac{Z_{in}(f)}{Z_{in}(f)+R_s}\right| \tag{2-9}$$

$$= \frac{N_{th_{out}} + N_{alias}}{N_{in}(f_{RF}).G_{c_v}^2(f_{RF}).\alpha(f_{RF})^2} \tag{2-10}$$

In (2-9) and (2-10), $N_{in}(f_{RF}).G_{cv}^2(f_{RF}).\alpha^2(f_{RF})$ is the input RF frequency band converted noise. Except for the wideband applications, the input noise outside the f_{RF} band is filtered by a narrow band matching network or LNA. Consequently, the input noise conversion for RF bands corresponding to LO harmonics becomes negligible. In this case, N_{alias} become equal to $2.N_{in}(f_{RF}).G_{cv}^2(f_{RF}).\alpha^2(f_{RF})$ and the overall NF can be written as:

$$NF_{SSB} = 2 + \frac{\frac{4KTr_{on}}{D}}{N_{in}(f_{RF}).G_{c_v}^2(f_{RF}).\alpha(f_{RF})^2} \tag{2-11}$$

Since the converted thermal noise has a 1/D variation while G_{cv} has a sinc($n.D$) variation (2-5), (2-11) shows that NF_{SSB} reach his lower value for the minimum of:

$$f(D) = \frac{1}{D.sinc^2(n.D)} \tag{2-12}$$

The function in (2-12) is plotted for n ratio of 1 and 3 in the Figure 2-5.

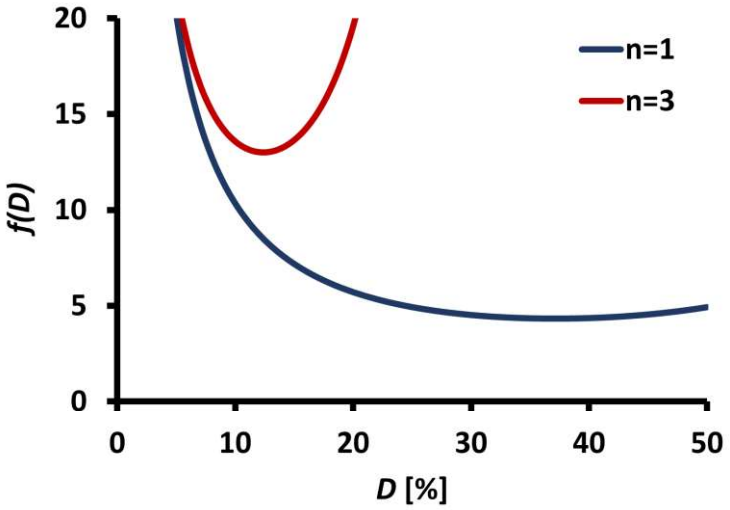

Figure 2-5 :plot of the *f*(D*)* function.

It can be noticed that the minimum NF_{SSB} value depends on the ratio between f_{RF} and f_{LO}. For example, when f_{RF} is close to f_{LO} (n=1), the lower is reached when D is around 35%. When f_{RF} is close to $3f_{LO}$ (n=3), the optimal NF_{SSB} value is reached with D around 12%. When D is set to this optimal value, the sampling mixer provides better NF_{SSB} than a conventional passive mixer (which is the case where D=50%). In addition, using a sampling mixer increases the conversion gain of the front-end before the baseband amplification. As a result, the baseband amplification noise contribution is lowered, thus improving the overall NF_{SSB} of the receiver.

2.3.5 Sampling mixer linearity

Like in a conventional CMOS passive mixer, the sampling mixer linearity is a strength. As this kind of mixer is intended to be driven by a low duty cycle LO signal, sharp rising and falling edges are needed. Hence, sampling passive mixer is highly linear thanks to fast transitions from OFF-state to ON-state [35].

2.3.6 Previous works on high frequency sampling passive mixers

To sum up, the sampling principle allows the design of highly linear passive mixer while the conventional passive mixer conversion gain limitation is overcome. Benefits of this mixing operation have already been demonstrated at lower frequencies. In [43], a sampling mixer in the IMS band at 2.4 GHz is implemented to take advantage of low consumption and good conversion gain. In addition, [43] shows that sampling mixer can also be used to benefit from a good I/Q isolation, since low duty cycle LO prevents overlapping between I/Q paths.

This principle is extended at higher frequencies in [44]. In this work, a sampling mixer has been implemented around 20 GHz with a 130 nm CMOS technology, demonstrating the interest of this principle for millimeter-wave receiver.

The good performances of nm-scaled CMOS processes, as the 28 nm FD-SOI, let the sampling passive mixer appear as a possible option for the conversion of a 77 GHz RF signal. However, the 77 GHz pulsed LO signal generation is critical. Therefore, next section deals with a new 77 GHz pulse shaper and its implementation into a sampling passive mixer.

2.4 Low duty cycle LO signal and frequency limitations

As previously stated, passive mixer driven into a sampling operation by a low duty cycle LO signal can reach high performances in terms of consumption, gain, noise figure and linearity. Nevertheless, the generation of such an LO signal is a challenge at high frequency.

2.4.1 High frequency low duty cycle LO signal

The generation of a proper low duty cycle square wave is quite difficult at high frequencies because it requires many harmonics that cannot be generated or managed. Main frequency limitations come from too low transistor f_t and parasitic elements. For example, the Figure 2-6 shows an ideal 77 GHz 25% duty cycle LO square signal and its resulting spectrum. Figure 2-6 puts forward that generating a LO signal with sharp falling and rising edges requires a significant voltage magnitude around many harmonics. Therefore, such a LO waveform is difficult to create with CMOS transistors f_t around 300 GHz.

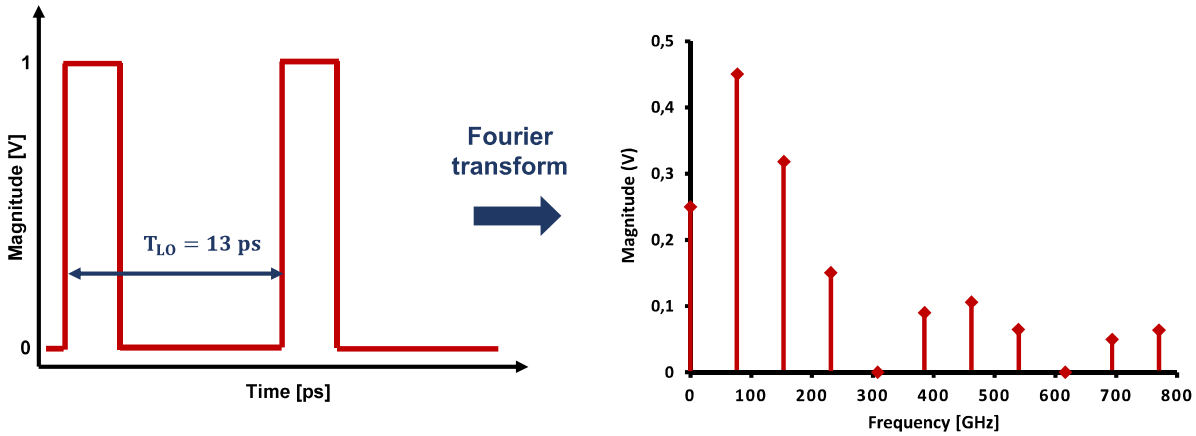

Figure 2-6: 77 GHz 25% duty cycle square signal in time and frequency domains.

2.4.2 CMOS low duty cycle signal generation at millimeter-wave frequencies

The more spread solution to generate low duty cycle signals is based on logic gates. At low frequency, the generation of non-overlapping low duty cycle clock for interleaved track and hold or N path mixer or filter is well mastered. Thanks to nm-scaled CMOS processes, these approaches based on logic gates have been extended to high frequencies.

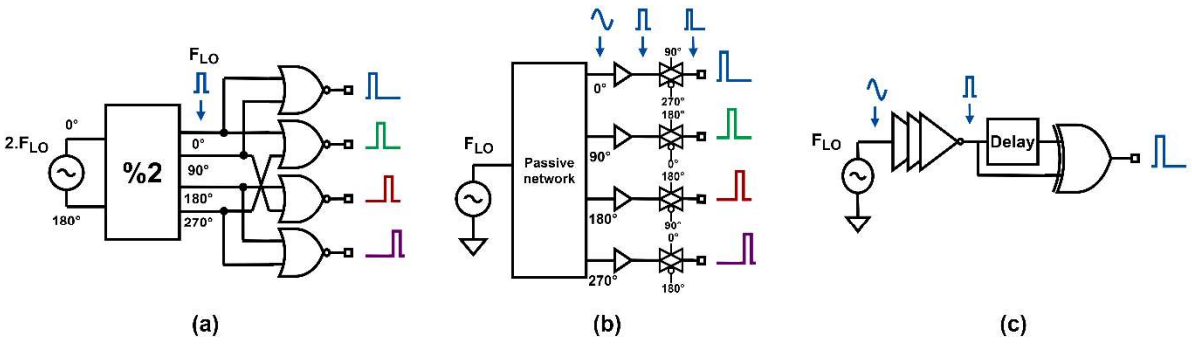

Figure 2-7: (a) Four non-overlapping clock generator based on D-latch divider (b) Four non-overlapping clock generator based on a passive network (c) Variable low duty cycle signal generator.

Different ways to generate a low duty cycle signal from a few GHz to 30 GHz are depicted in Figure 2-7. Circuits of Figure 2-7.a and Figure 2-7.b generate four 25% non-overlapping clocks often required for N path or I/Q mixers. Figure 2-7.a describes a quite conventional method to generate 25% duty cycle clock used in [43] at 2.45 GHz. In this circuit a D-latch divider by 2 generates four 50% duty cycle square waves with 0°, 90°, 180°, 270° phase shifts. These signals are then combined with XOR gates to generate low duty cycle signals.

Figure 2-7.b is used in [45] and presents a quite similar operating principle. However, this circuit operates up to 30 GHz. As a 60 GHz D-latch divider design would be critical or would result in a very high DC power consumption, this divider is replaced by a passive network. This network generates 4 phase shifted sinusoidal signals which are turned into square wave by buffers. Finally, the four non-overlapping clocks are generated by four transmission gates.

Finally, a simple approach to generate low variable duty cycle signal is depicted in Figure 2-7.c. With this method a sinusoidal signal is turned into a square signal with inverters. Then two time-delayed square signals are created and combined by an AND gate.

Even if all these low duty cycle LO signal generators, based on CMOS logic gates, are reported up to 30 GHz, it seems difficult to extend their operation up to 77 GHz with the available nm-scaled CMOS processes. The logical gates exhibit a too poor gain value in the millimeter-wave range to reach all required harmonic amplitudes for the LO voltage on a capacitive load (mixing transistor gate). As a result, another solution must be found for the generation of a low duty cycle LO signal in the range of 77 GHz.

2.5 Non-Linear Transmission Lines for millimeter-wave pulse shaping

An interesting solution to overcome active device frequency limitations is to use passive non-linear devices with very high cut-off frequencies to create the harmonics required for a pulsed signal. This idea is illustrated by a Non-Linear Transmission Line (NLTL) based on varactors [46], which turns a sine wave into a pulsed periodic signal (Figure 2-8).

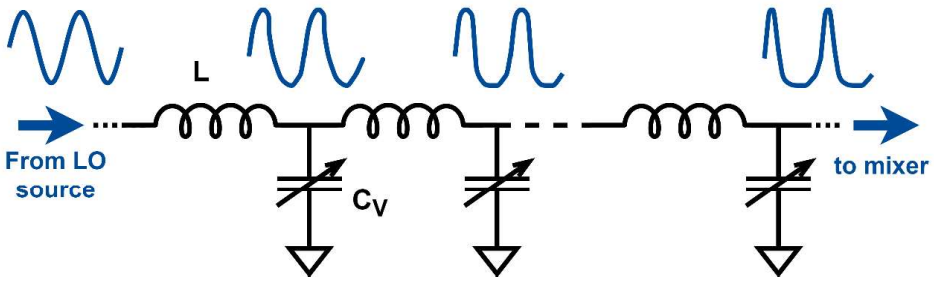

Figure 2-8: NLTL operating principle.

The pulse shaping comes from the varactor non-linearities. The NLTL characteristic impedance and the propagation constant of the signal in a NLTL are:

$$Z_{NLTL} = \sqrt{\frac{L}{C_{vmean}}} \; and \; \gamma_{NLTL} = \; \mathrm{j}.\omega\sqrt{L.C_v(V)} \tag{2-13}$$

In (2-13), C_{vmean} is the average capacitance of varactors. As the sinusoidal propagation constant is different for the lower and the upper part of the sine, the outgoing signal is distorted, and the sine is finally turned into a pulsed waveform.

For a proper 77 GHz LO pulse shaping, the NLTL exhibits quite large length ([46]) and an input impedance lower than 50 Ω. As the required varactor capacitance tends to decrease the NLTL characteristic impedance, the NLTL brings a lower input impedance than mixing transistor gates. As providing a high voltage swing on a low input impedance requires a significant power, the LO voltage swing amplitude is a bit limited and an additional driving stage is necessary resulting in an extra consumption. At the scale of a whole radar transceiver chip with multiple Rx and Tx, NLTL extra consumption and size make its implementation quite difficult. To overcome these limitations, a new pulse shaper architecture inspired from NLTL has been designed and it is presented in the following sections.

2.6 A new 77 GHz pulse shaper architecture

A new pulse shaper architecture is presented in Figure 2-9, which is convenient for millimeter-wave application. This architecture is inspired from the NLTL operating principle. From this circuit the input sine is amplified and turned into a pulsed waveform at the same time. The common-source transistor (M_{amp}) brings the linear amplification of the LO input signal while the pulse shaping comes from the LC_v resonator. The M_{amp} transistor sizing is W/L = 36 µm/30 nm. A NMOs transistor (M_{var}) with a W/L of 25µm/1µm is chosen to implement the varactor C_{v}. This choice is explained later.

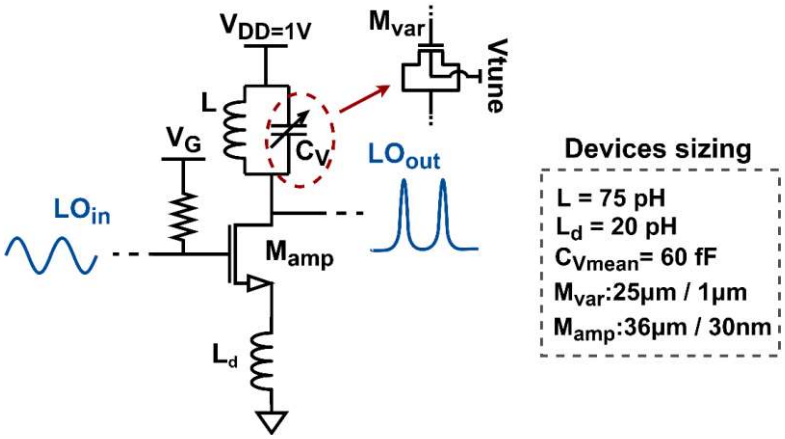

Figure 2-9: Pulse shaper topology.

The impedance of the resonator is varying in time as C_v capacitance value depends on the LO_{out} voltage. These impedance changes make LO_{out} phase and magnitude alternatively increase and decrease over the LO period to create this pulsed waveform. The varactor $C_v(V)$ characteristic must be as abrupt as possible to reach sharp rising and falling edges [47] and thus getting a low pulsed signal duty cycle. L and $C_v(V)$ values are chosen to get a mean resonance frequency as:

$$f_{0_{LC}} = \frac{1}{2\pi\sqrt{L.C_{v_{mean}}}} \approx 77\ GHz \qquad (2\text{-}14)$$

As the pulse shaper output is directly connected to the mixing transistor gates it is thus charged by a quite high impedance. A proper LO voltage swing can be delivered without a prohibiting DC power consumption. This structure is also very compact. Therefore, this topology is well suited to nm-scaled CMOS designs.

2.7 Pulse shaper implementation

2.7.1 NMOS Varactor implementation

In the pulse shaper, a NMOS transistor is used as varactor because of its abrupt $C_v(V)$ curve. The layout of this NMOS varactor is described in Figure 2-10. The chosen sizing leads to a varactor capacitance ranging between 20 fF and 90 fF.

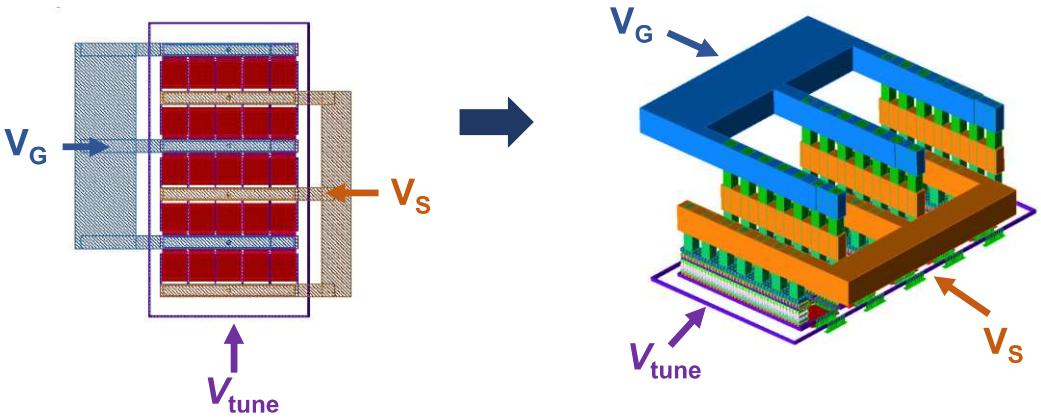

Figure 2-10: Layout of the NMOS varactor.

In FD-SOI technologies, the body effect is high (~ 85mV/V) making possible to tune the V_{th} by changing the body voltage V_{tune}. As shown in Figure 2-11, this property can be used to shift the varactor C_v(V) characteristic. This feature is used to tune LO waveform and to find the best trade-off between LO peak magnitude and duty cycle

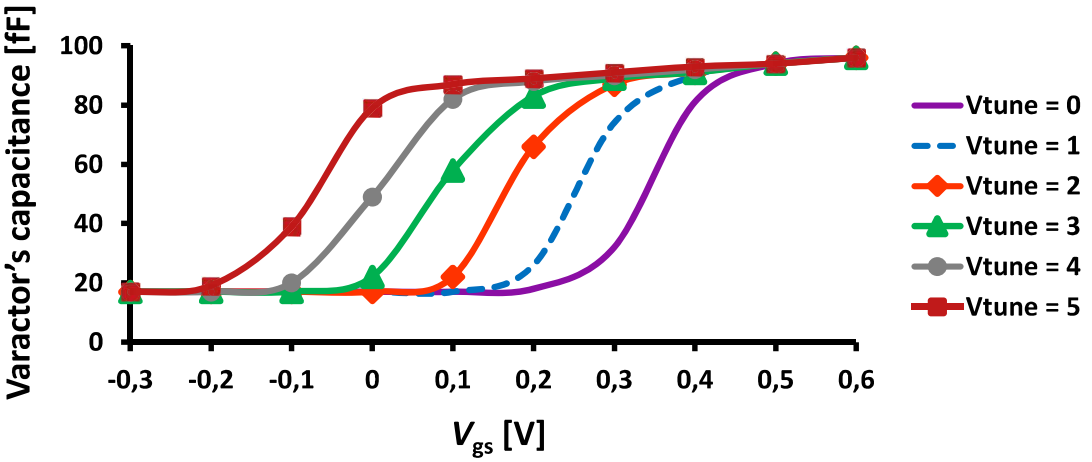

Figure 2-11: Cv(V) of the varactor for different body voltages.

2.7.2 Stability

As the varactor capacitance C_v(V) is driven by the output voltage swing of the pulse shaper, only using a small signal S-parameter analysis to simulate the input reflection coefficient of the pulse shaper is not sufficient. A large signal S-parameter simulation combining an harmonic balance simulation to consider the output voltage swing and a small signal S-parameter simulation computing the S_{11} is performed. Small and large signal S-parameter analysis results

reported in Figure 2-12 show that an inductive degeneration helps keeping the pulse shaper S_{11} below 1 by neutralizing the output signal feedback coming from the parasitic capacitances of the transistor M_{amp}. Therefore, this inductive degeneration is necessary to ensure the pulse shaper stability. A 20-pH inductance is implemented on the source of each transistor in common source configuration of the pulse shaper (M_{amp} in Figure 2-9) to guaranty the pulse shaper stability.

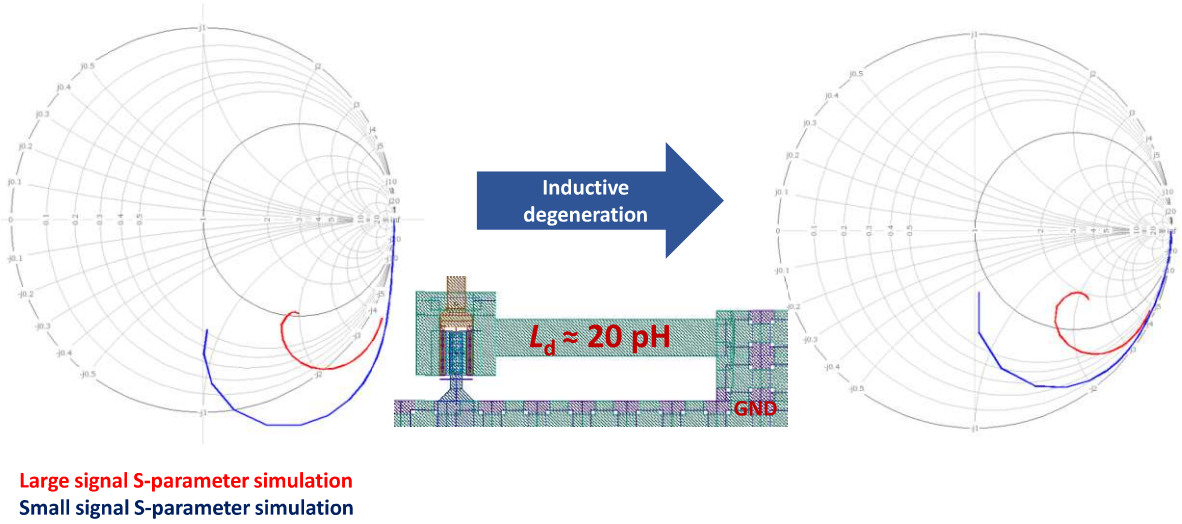

Figure 2-12: Pulse shaper input impedance with and without inductive degeneration.

Finally, the stability of this circuit is checked by applying current pulses on the input and DC supply ports and simulating the pulse shaper transient response.

2.7.3 LO input matching

An LO input balun is used to provide a differential 77 GHz LO signal to the pulse shaper and for the 50 Ω matching of the LO port. Each output of the LO balun are connected to a single-ended pulse shaper (Figure 2-9). The implemented balun has a 75 µm external diameter and both primary and secondary coils have a 4 µm metal strip width. The upper thick metal levels (alucap and IB) are used to avoid losses coming with series resistances. Matching capacitances C_1 of 40 fF and C_2 of 15 fF are set for enabling a proper 50 Ω matching. The whole matching network of the LO port is depicted in Figure 2-13.a

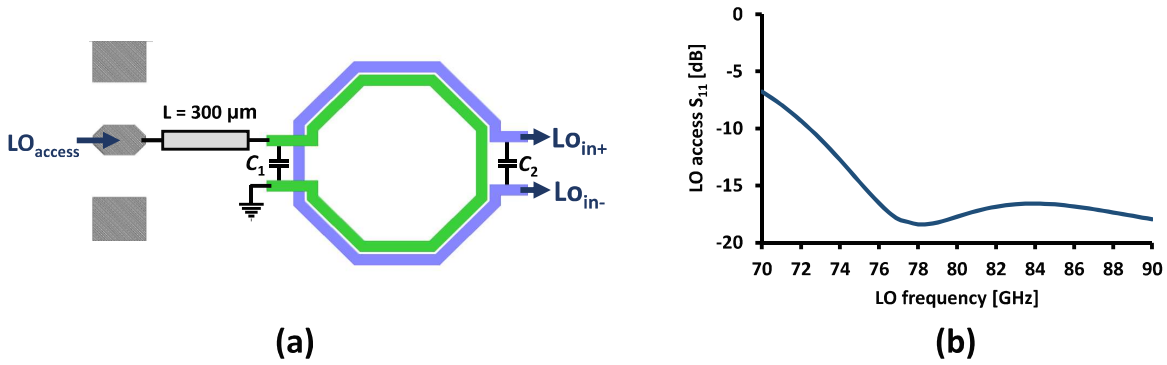

Figure 2-13: (a) LO input network (b) magnitude of LO port reflection coefficient.

A large signal S-parameter simulation is performed to extract the LO port reflection coefficient (Figure 2-13.a). The result of this simulation is reported in Figure 2-13.b showing a S_{11} lower than -16 dB over the 76-81 GHz frequency band.

2.8 Generated LO pulsed waveform

A transient simulation of the standalone pulse shaper is performed after the modelling of all layout parasites with momentum or Post Layout Simulation (PLS) extracts. Output voltage waveforms are depicted in Figure 2-14 for an input LO power of 0 dBm and different varactor tuning voltages (V_{tune}). Using this tuning voltage allows to find the best trade-off between the mixer linearity and conversion gain. A V_{tune} of 1V leads to the sharpest rising and falling edges and will provide the best mixer linearity. Nevertheless, this waveform shows the higher LO duty cycle. On the contrary a V_{tune} of 5V will give the lower LO duty cycle to benefit from the best conversion gain but the rising and falling edges are significantly softened. The best trade-off on mixer performances will be reached with a V_{tune} of 3V. In this configuration, the power consumption of the 77 GHz LO pulse shaper is 10 mW under a 1V supply.

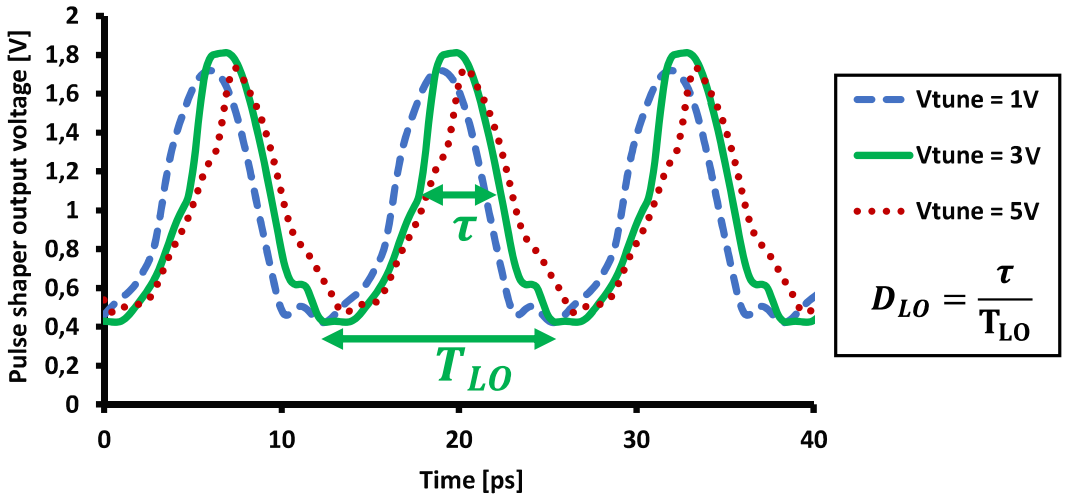

Figure 2-14: Pulse shaper output waveforms for different V_{tune}.

With dimensions of devices presented in Figure 2-9 and a V_{tune} of 3V, the pulse shaper generates a 1.4 $V_{\text{p-p}}$ pulsed LO waveform with a duty cycle D_{LO} of 33%. This value of D_{LO} appears to be the best performance that can be reached, because of limitations introduced by the non-negligible layout parasite influence at 77 GHz. Nevertheless, this LO pulsed waveform still improves mixer performances compared to a sinusoidal LO drive.

To check the reliability of the transistors of the pulse shaper under voltage conditions of Figure 2-14, the V_{DS} and V_{GS} have been monitored. Because V_{GS} is low (no current) when V_{DS} is high, transistors do not enter into high Hot Carrier Injection and stay in a safe operating area.

All in all, this new pulse shaper topology appears quite promising to generate low duty cycle LO signals at millimeter-wave frequencies. The next sections present the implementation of this circuit into a 77 GHz sampling mixer prototype in 28FDSOI technology.

2.8.1 Layout description

The Figure 2-15 shows the layout of the balanced pulse shaper implemented on the 77 GHz sampling mixer test chip in 28FDSOI.

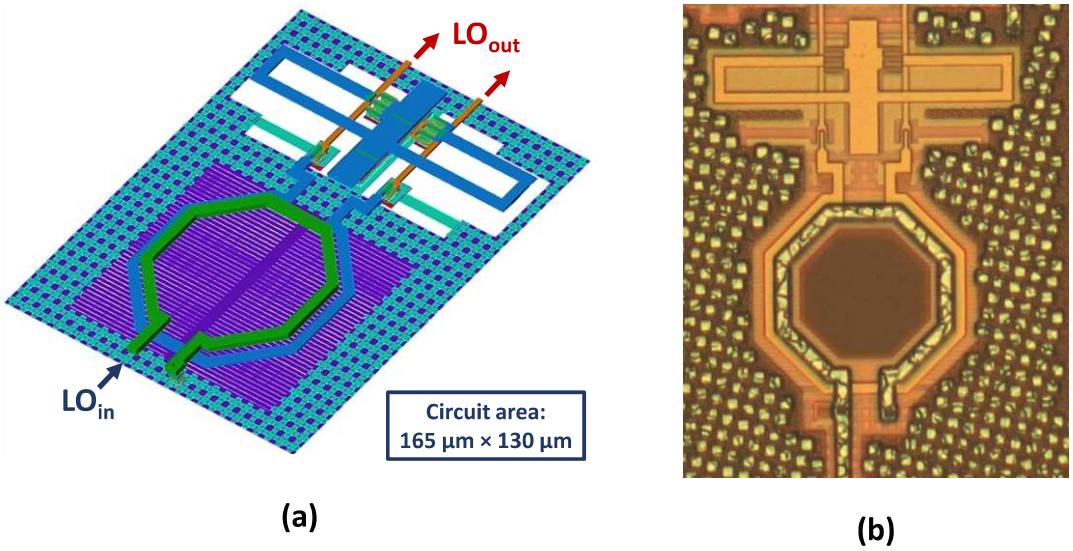

Figure 2-15: (a) 3D view of the pulse shaper layout (b) Pulse shaper implemented in the 28FDSOI test chip.

An input passive balun is used to feed the balanced LO pulse shaper where the single-ended pulse shaper of Figure 2-9 is duplicated to address both LO phases.

The LC resonator 75-pH inductor of both pulse shapers is tied to a common V_{DD} supply. Figure 2-16 describes the V_{DD} supply decoupling strategy for the pulse shaper.

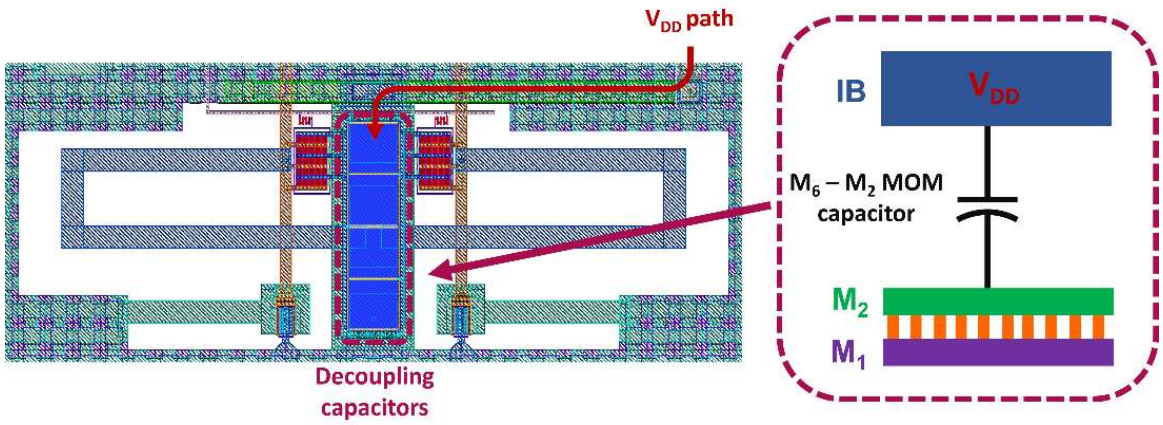

Figure 2-16: Decoupling strategy for the pulse shaper.

As the inductive parasitic elements of the V_{DD} supply path can lead to a degradation of the LO waveform or potential oscillations, a proper decoupling must be implemented as close as possible to the pulse shaper. Four 150-fF MOM capacitors using M_2 to M_6 metal levels are used to connect the V_{DD} access to the ground plane. This decoupling ensures a low impedance of the V_{DD} supply bus at millimeter-wave frequencies. Extra decoupling capacitors are

implemented between the pulse shaper and the V_{DD} supply pad to get an efficient decoupling at lower frequencies.

2.9 Sampling mixer core implementation

2.9.1 Mixing transistor and hold capacitor sizing

The mixing transistor sizing is essential to get a good noise/linearity trade-off. As already stated, sharp LO pulse rising and falling edges are needed to get the best linearity from the sampling mixer. However, mixing transistors present a capacitive load to the output of the pulse shaper, which tends toward a low impedance at high frequencies. Consequently, the LO pulse edges can be softened, and the linearity decreased. Lowering the width of mixing transistors helps keeping sharp LO edges. On the other hand, increasing the width helps to reach a low NF by lowering the ON-state resistor r_{on} of transistors. A trade-off must be found as illustrated in Figure 2-17.

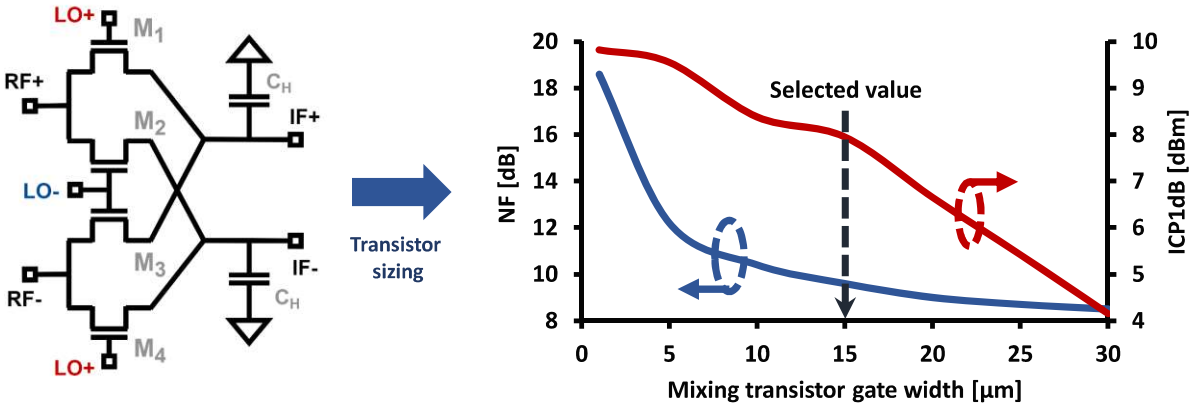

Figure 2-17: Noise and linearity performances vs mixing transistors gate width.

Figure 2-17 shows the noise/linearity variations versus transistor width when conversion gain is kept constant. It can be noticed that widths between 10 µm et 20 µm give the best trade-off. The mixing transistor sizing of 15 µm / 30 nm has been selected.

Finally, to ensure a good sampling, each IF amplifier input provides a high resistive impedance (10 kΩ) in parallel with the C_H/g_c lowpass network (g_c is the mean channel conductance of $M_{1,2,3,4}$). The C_H value is set to 300 fF to have a discharge time constant $R_{IF}.C_H$ far higher than $1/f_{LO}$ to properly store sampled value. With a C_H of 300 fF, the $g_c/(2\pi C_H)$ cut-

off frequency is higher than the IF amplifier bandwidth so C_H does not limit the bandwidth of the circuit.

2.9.1.1 Layout of the sampling mixer core

Figure 2-18 depicts the layout of the sampling mixer core, including mixing transistors, the 300-fF hold capacitors and DC supplies. The Thick metal levels IA and IB are used for RF and LO signals to limit losses, while the thin metal level M_6 is used for IF frequencies around 20 MHz. Source and gate DC voltages applied on the mixing transistors (respectively V_{Smix}/V_{Gmix}) are provided by way of 10 kΩ resistors.

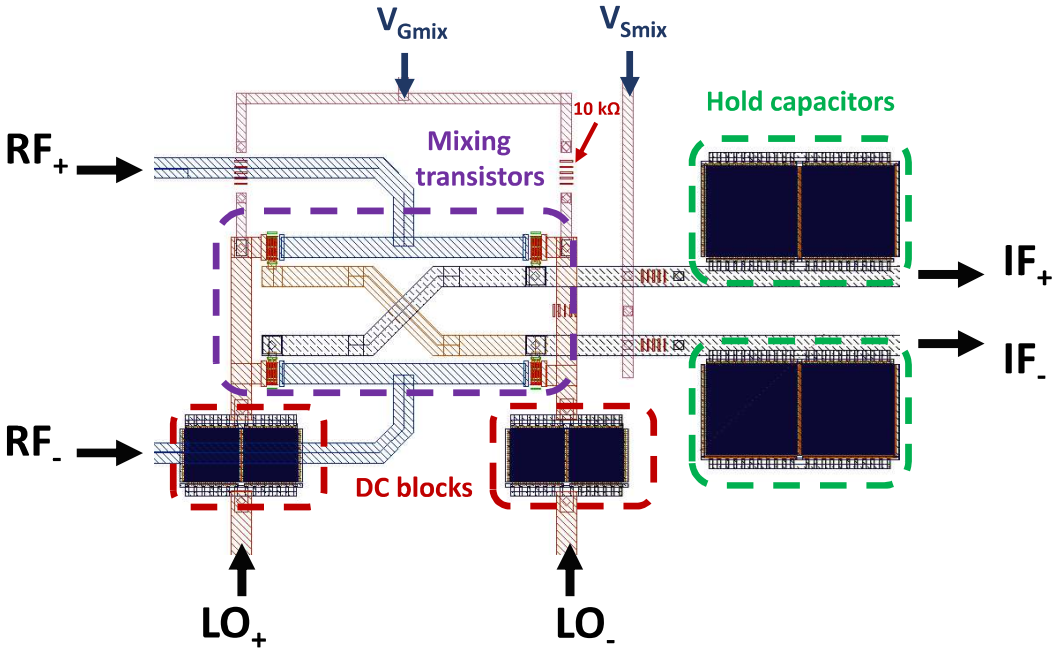

Figure 2-18: Sampling mixer core layout.

The V_{Smix} DC value is set to 0.6 V to properly bias the IF OP-amp followers. To have a sharp ON/OFF transition, the LO signal has to make V_{GS} crossing V_{th} when LO signal slope is maximum. The DC value of pulse shaper output (1V) is too high to comply with this condition. DC blocking capacitors have been added so that LO DC voltage can be adjusted using V_{Gmix}. The choice of V_{Gmix} is illustrated on Figure 2-19.

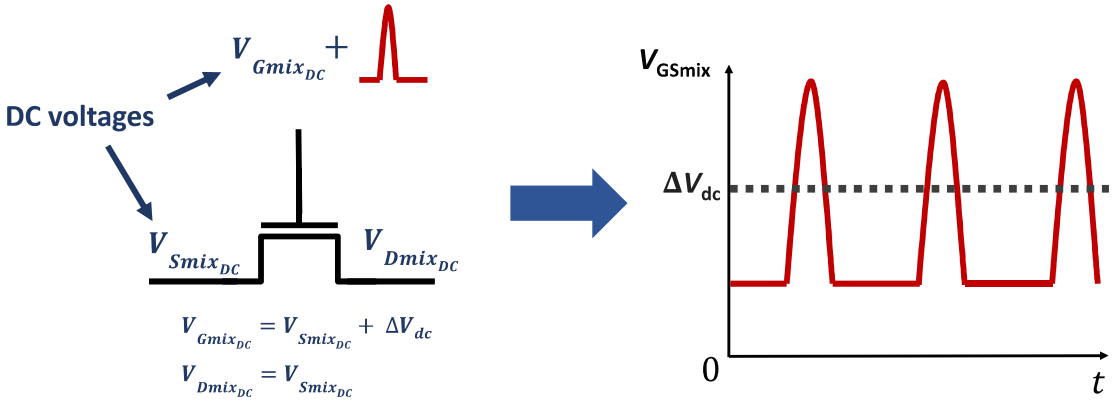

Figure 2-19: Mixing transistor biasing.

After the DC block, the LO waveform is centered on V_{Gdc} which is equal to $V_{Sdc} + \Delta V_{dc}$. Setting the half magnitude of pulses close to the mixing transistor V_{th} requires a V_{Gdc} around 0.75V for the gate bias voltage.

2.9.2 RF input matching

As the sampling mixer exhibits a quite high input impedance, a RF balun with a 1:2 turns ratio is necessary to present a 50 Ω impedance at the RF port. The external diameter of this RF input balun (Figure 2-20) is around 50 µm. Like for the LO balun, upper metal levels are used. The primary and secondary metal strip widths are respectively 4 µm and 2 µm. Two parallel 10-fF matching capacitors are implemented at the output of the RF balun. The 25-fF capacitance of the signal pad, which is part of the GSG pattern integrated for RF probing, is used as input matching capacitance. In this way, no de-embedding of RF pads will be required when characterizing this circuit.

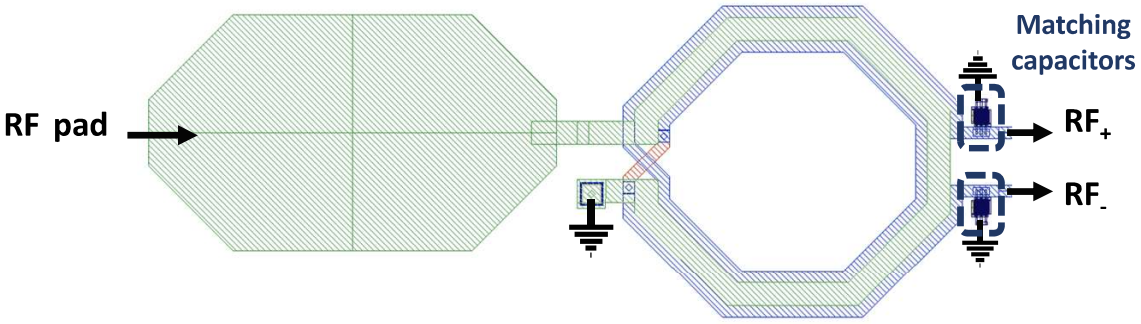

Figure 2-20: RF port matching network.

As the mixer is a non-linear device, the LO signal cannot be considered as a small signal to compute the mixer S_{11}. Consequently, a large signal S-parameter simulation is performed. The simulated RF input reflection coefficient for different f_{LO} is reported in Figure 2-21. The simulation shows a good RF matching for f_{LO} in the range of 76-81 GHz.

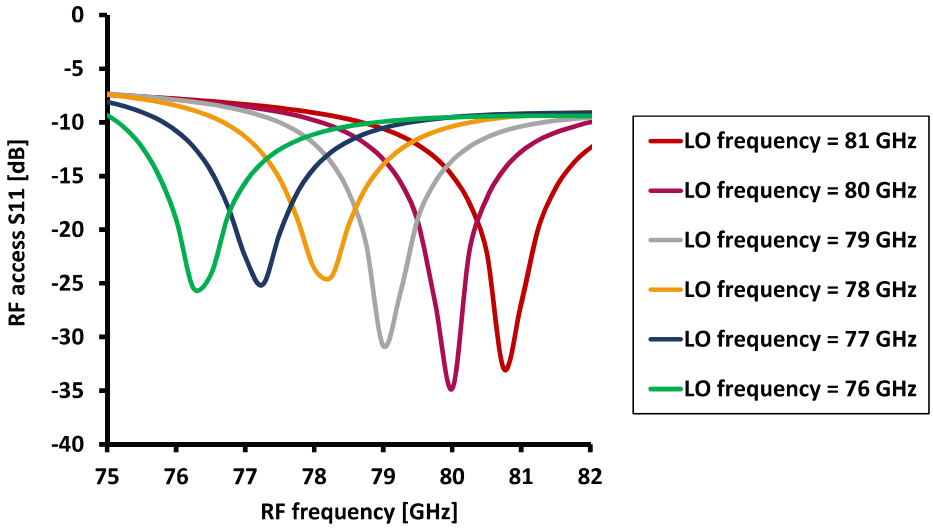

Figure 2-21: RF input reflection coefficient.

2.10 Standalone mixer simulated performances

All simulation results presented in this section involve a global layout modelling using momentum and a PLS extract. Moreover, in order to assess the benefits of sampling, a sinusoidal and a pulsed LO waveform of same magnitude are used to drive the mixer. The pulsed 77 GHz LO waveform is generated by the LO pulse shaper presented earlier, with a 0-dBm input power.

2.10.1 Gain and linearity

The harmonic balance simulation results, with RF and LO frequencies respectively set to 77.02 GHz and 77 GHz are reported in Figure 2-22. Simulated voltage conversion gain compressions are reported for both LO waveforms.

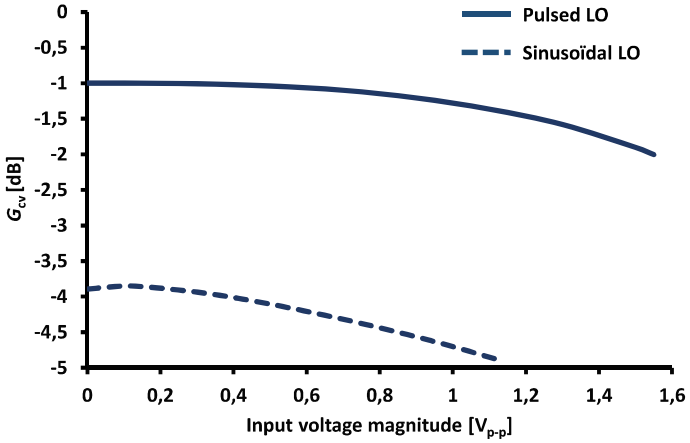

Figure 2-22: Voltage conversion gain compression curves.

When the mixer is driven by a sinusoidal waveform, the conversion gain is around $2/\pi$ (-4 dB), which corresponds to the theorical gain of a conventional voltage passive mixer. For the sampling mixer driven by the pulsed LO waveform, the conversion gain is now -1 dB. In good agreement with the sampling mixer principle, this simulation shows that the low duty cycle pulsed LO waveform significantly improves the conversion gain.

This pulsed LO waveform also presents sharper falling and rising edges than a sine, which leads to a better linearity. This improvement is validated by simulations, since the input -1 dB compression voltage $V_{\text{-1}dB}$ is 1.55 $V_{p\text{-}p}$ for the pulsed waveform and 1.1 $V_{p\text{-}p}$ for the sine wave. This compression point is expressed as a voltage because the use of power is not relevant here, considering the high Z_{in} of the mixer. However, an equivalent power compression point in a 50 Ω system can be derived considering that $V_{\text{-1}dB}$ voltage is delivered to a 50 Ω load. For pulsed and sinusoidal LO waveforms, these equivalent ICP1dB are +7.8 dBm and +5.2 dBm, respectively. This result proves that turning a sine into a pulsed waveform improves the linearity when the LO voltage amplitude is kept constant. It is welcomed since the linearity of mixers is decreasing with the scaling down of CMOS processes as the transistor breakdown voltage reduction is limiting the maximum LO voltage amplitude that can be applied.

2.10.2 Noise

A harmonic balance-based non-linear noise simulation has been performed as well. The NF_{SSB} when using a 50 Ω RF source is plotted in Figure 2-23, and an enhancement of 1.3 dB

can be noticed for a pulsed LO signal. Once again, the sampling mixer appears as a favourable alternative to the sine driven passive mixer.

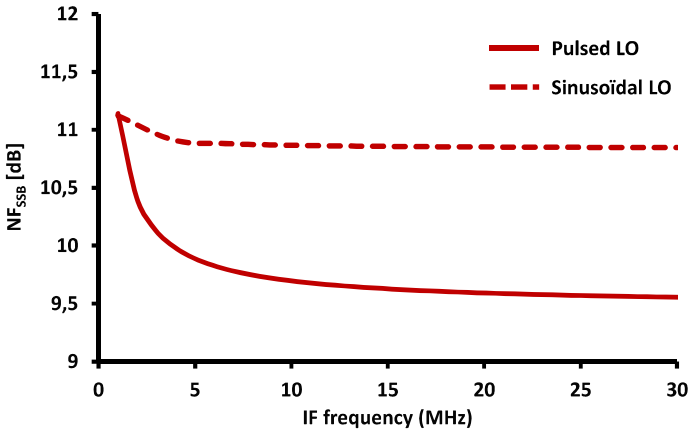

Figure 2-23: Simulation results for mixer NF_{SSB}.

In addition, it must be reminded that another positive sampling mixer contribution on noise is resulting from a higher front-end gain which limits the important baseband noise contribution into the receiver noise budget.

As a summary, these simulations show that sampling mixer exhibits better performances than conventional sine driven passive mixers, thanks to the LO pulse shaping. The voltage conversion gain is increased by 3 dB, the ICP1dB by 2.6 dB and the NF_{SSB} is reduced by 1.3 dB.

2.11 IF Operational amplifier followers

An operational amplifier (OP-amp) in a follower configuration is implemented on both outputs of the mixer. These output buffers are isolating the mixer from the measurement setup with a unitary gain while providing a high input impedance in parallel with the hold capacitor of the mixer core. Using an output stage with a unitary gain prevents any de-embedding of measurements to reach the mixer gain. The linearity of this output stage must be also higher than the mixer linearity not to impact measurements.

2.11.1 Operational amplifier design

The schematic of the IF OP-amp is given in Figure 2-24. This amplifier is based on a conventional topology with a PMOS common source output stage, for increasing the open loop gain. The OP-amps are used as followers (OUT connected to IN_- and IN_+ to one mixer output).

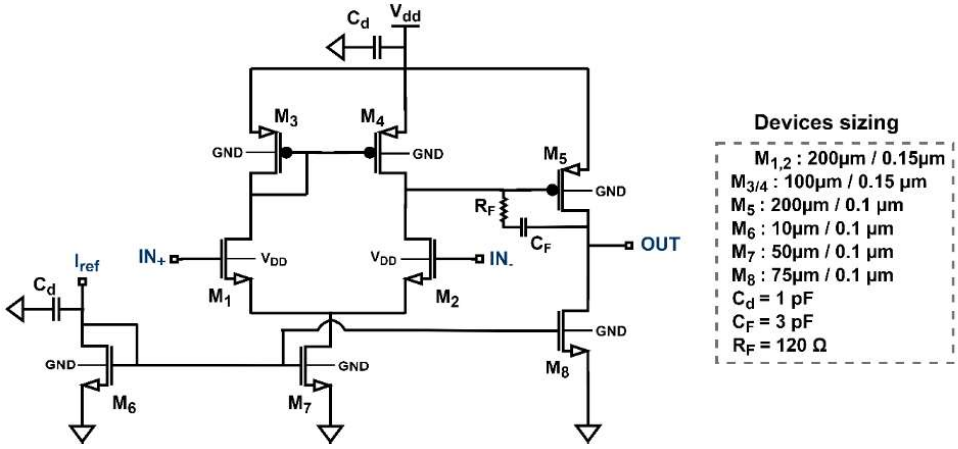

Figure 2-24: OP-amp schematic.

Gate length of 100-nm and 150-nm are used for lowering the *1/f* noise. Amplifying stages are biased by way of a current mirror. $R_F C_F$ feedback is implemented on the output stage to provide at least 50° of phase margin. The aim is to ensure a good stability whatever process variations are. Finally, decoupling capacitors C_d are implemented on the V_{DD} and I_{ref} DC supplies.

These OP-amp output buffers are biased under a 1.5 V V_{DD} to get the required linearity. Reliability issues are prevented using thick gate oxide transistors with higher breakdown voltages. The V_{th} of transistors is adjusted from the body voltage set to V_{DD} or to GND. The layout of one OP-amp in a follower configuration is depicted in Figure 2-25. The represented circuit area is 105µm×100µm.

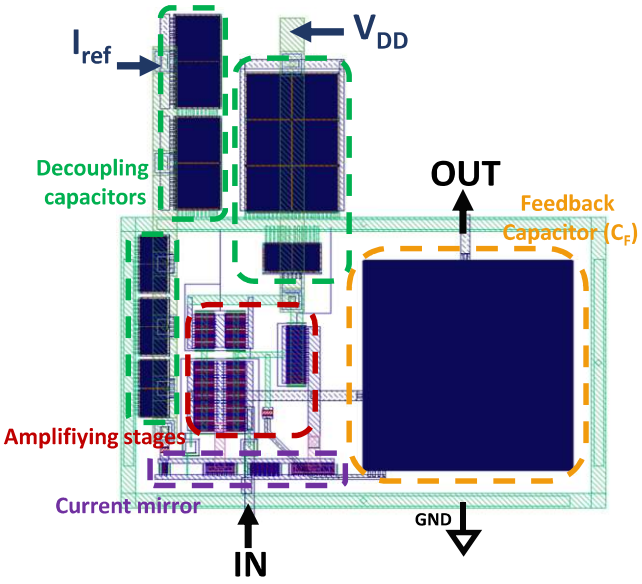

Figure 2-25: OP-amp follower layout.

2.11.2 Open loop analysis

The stability of OP-amps designed for the output stage is checked from simulation of the open loop configuration (no feedback on the inverting input IN-). A small signal simulation taking into account all parasitic elements of the layout is performed to compute the open loop gain and the input/output phase shift. Results of this simulation are reported in Figure 2-26.

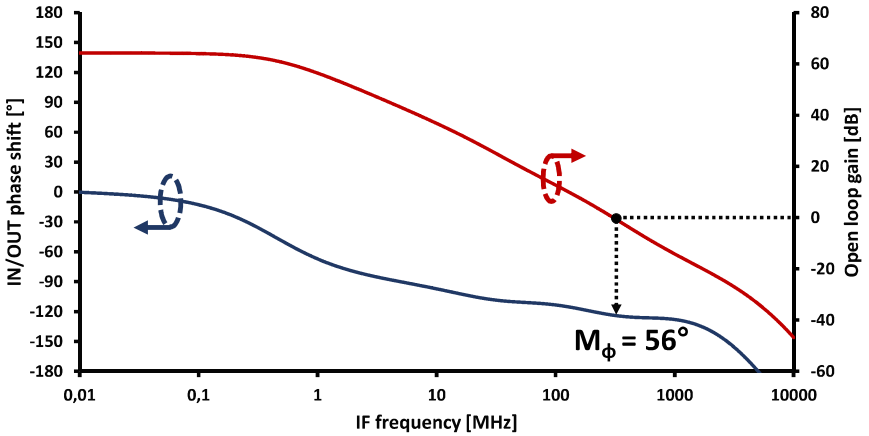

Figure 2-26: OP-amp open loop performances.

Capacitive loads tend to degrade the OP-amp stability by lowering the frequency where the phase shift between the OP-amp input and output reach 180°. As a result, the phase margin decreases when the load capacitance increases. The OP-amp is simulated with a 20-pF

capacitive load representing an oscilloscope probe input capacitance. Under these conditions, this circuit exhibits an open loop gain of 64 dB with a 56° phase margin.

2.11.3 Closed loop performances

The OP-amp is implemented and simulated in the follower configuration (The OP-amp inverting input IN- tied to the output). The harmonic balance and noise simulation results are reported in Figure 2-27.

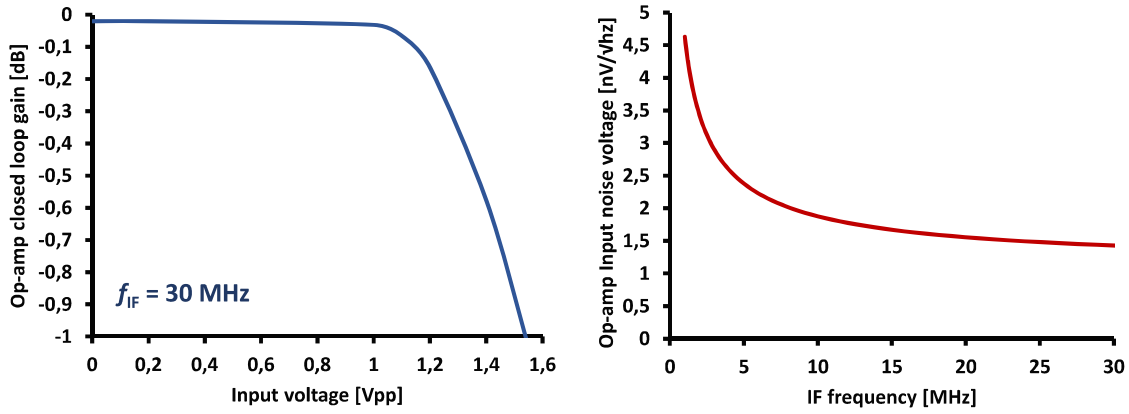

Figure 2-27: OP-amp closed loop performances.

Each IF output stage exhibits a 0 dB gain and a 1.5 nV/√hz input-referred noise voltage at 30 MHz. The gain compression occurs for input voltages beyond 1.2 $V_{p\text{-}p}$. Since the voltage on each mixer IF output is around 0.6 $V_{p\text{-}p}$ at the mixer 1 dB compression point, these buffers appear linear enough to keep the whole circuit linearity. Power consumption of each OP-amp is 7.5 mA on the 1.5 V voltage supply.

2.12 77 GHz sampling mixer test chip

The architecture of the test chip for the standalone 28FDSOI 77 GHz sampling mixer is depicted in Figure 2-28.a. A picture of the manufactured chip is given in Figure 2-28.b. The circuit area is 0.83 mm × 0.68 mm.

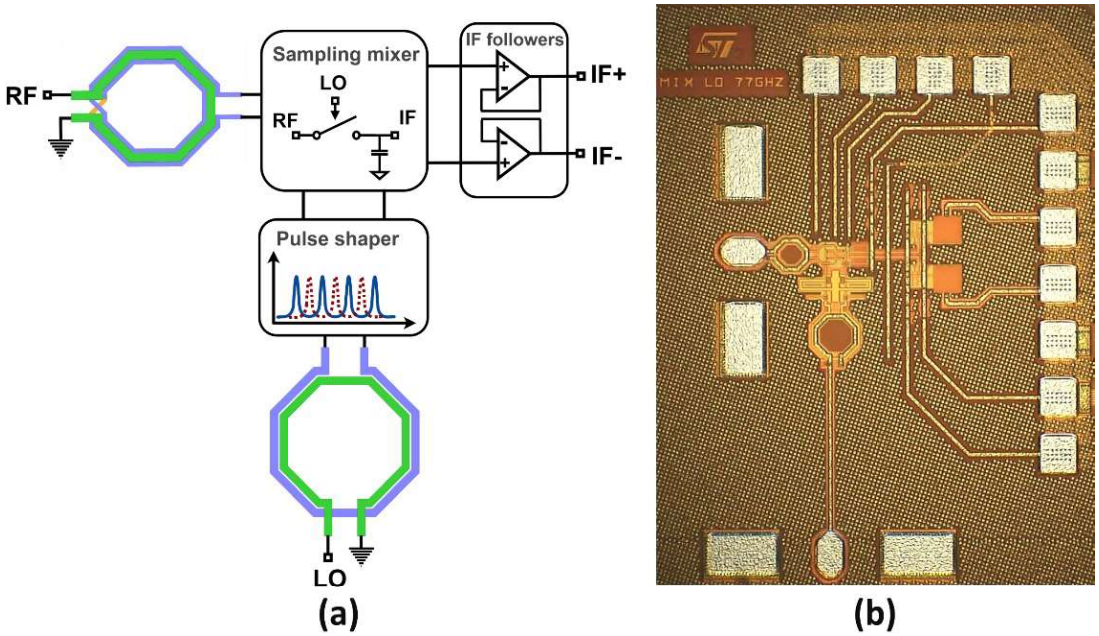

Figure 2-28: (a) RF mixer block diagram (b) manufactured chip.

Differential 77 GHz signal synthesizers are not available. Consequently, as for the LO signal, an input passive balun providing differential RF signals and performing a 50Ω matching is implemented on the RF port. This balun exhibits a 8.2 dB voltage gain corresponding to the voltage transformation ratio. To be able to measure the 77 GHz mixer with perpendicular RF probes, a 300µm line must be inserted between the LO balun and the LO GSG pads to separate both RF probes.

Following sections are dealing with the measurement setup used for the characterization of this 77 GHz sampling mixer demonstrator and with the presentation of measurement results.

2.13 Millimeter-wave measurement setup

2.13.1 Measurement bench description

The 77 GHz prototypes have been measured at the LAAS-CNRS laboratory. The available millimeter-wave RF-probe measurement bench is based on commercial WR-12 waveguide components operating in the 60-90 GHz frequency band. The LO and RF chain are set up around a Süss Microtech PM8 probe station. Figure 2-29 is a picture of the whole millimeter-wave measurement bench.

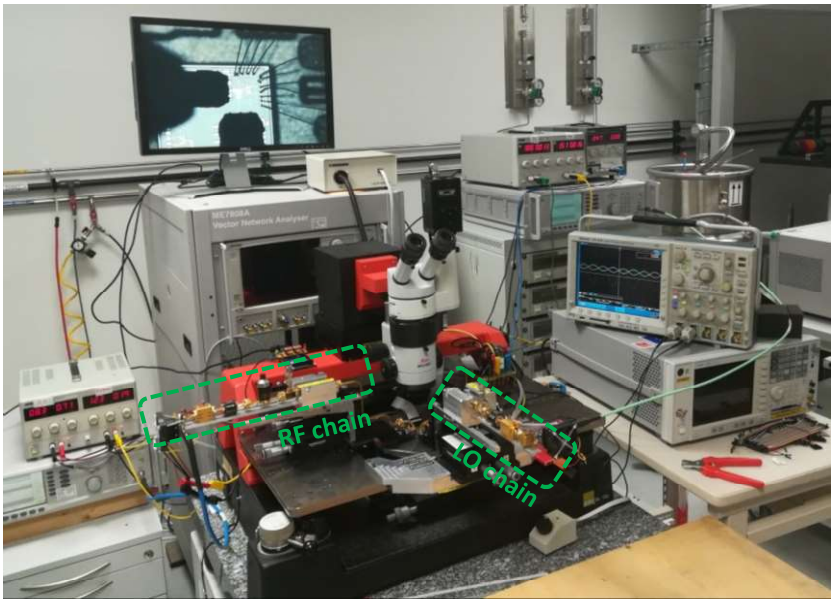

Figure 2-29: 60-90 GHz RF-probe measurement bench.

The RF and LO signal chains rely on dedicated mechanical supports manufactured at the laboratory to adapt the PM8 station to the mixer measurement specific configuration. These mechanical supports and the micro-positioners are moving simultaneously to avoid constraint on motions of the RF probes.

2.13.2 Gain and linearity measurement setup

2.13.2.1 RF and LO chain description

The Figure 2-30 presents the photograph of the 60-90 GHz RF or LO chain based on WR-12 waveguide components.

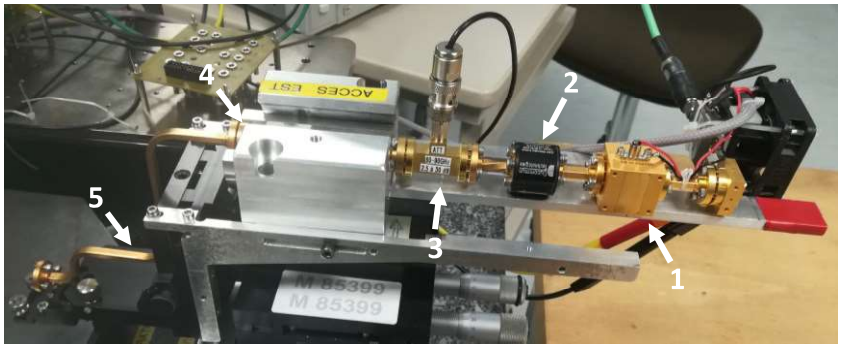

Figure 2-30: 60-90 GHz RF/LO chain.

RF or LO signal generation chain is fed by a RF signal synthesizer operating up to 15 GHz. These chains include a x6 multiplier to generate 60-90 GHz signals, an isolator ensuring a 50 Ω matching and a voltage-controlled attenuator providing an accurate control of the RF chain output power. Straight and "S" WR-12 are used to connect RF and LO chains to 150 µm GSG probes. In this configuration each chain can deliver a RF power up to 2 dBm at the plane of the RF probe tips.

2.13.2.2 Conversion gain and linearity measurement

The setup for conversion gain and linearity measurements is described in Figure 2-31. RF and LO signals around 77 GHz are applied by GSG RF probes laid down on the RF and LO ports of the die. IF output signals around 20 MHz are then measured with an oscilloscope and the mixer voltage conversion gain is calculated considering RF signal chain power calibration. IF output signals are measured for several positions of the RF chain attenuator, and the mixer ICP1dB is computed from this set of measures.

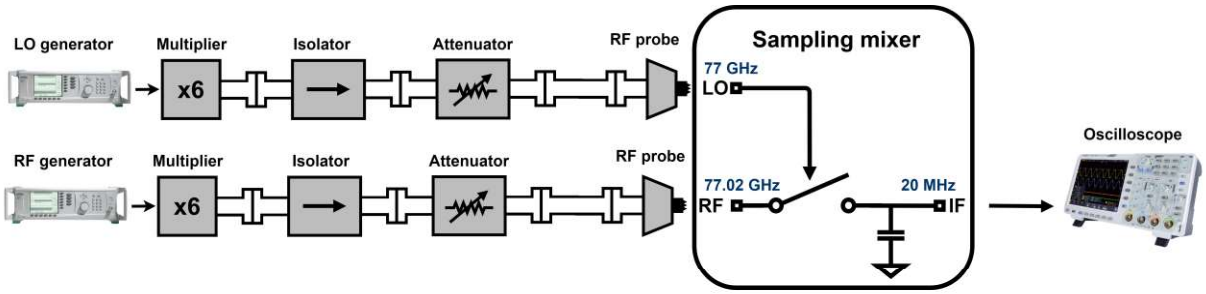

Figure 2-31: Conversion gain and linearity measurement setup.

2.13.2.3 Calibration of the RF and LO chains

The knowledge of the RF and LO chain output power for each attenuator position is required to perform an accurate conversion gain measurement. However, directly measuring the delivered power at the output of the RF probes is impossible. Thus, the calibration method described in Figure 2-32 is used.

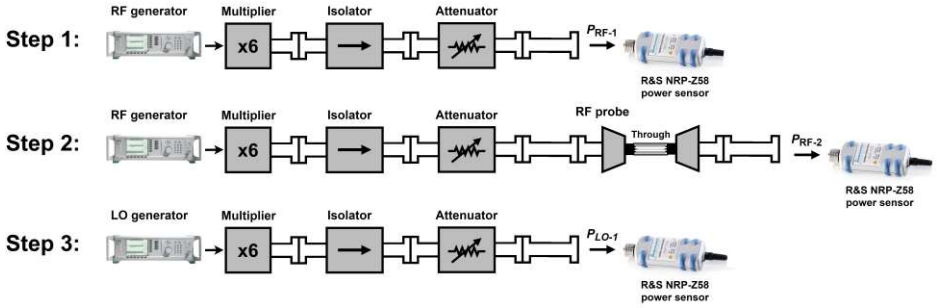

Figure 2-32: RF and LO chains calibration method.

The first calibration step consists in measuring the available power ($P_{\text{RF-1}}$) at the attenuator output with a R&S NRP-Z58 thermal power sensor for all attenuator positions. Then, both RF and LO probes are placed on a calibration standard "through" corresponding to a short 50 Ω line between both probes and the power at the 2nd probe output $P_{\text{RF-2}}$ is measured (Step 2). By neglecting the losses of the through-standard, the losses of a single RF probe can be calculated as:

$$L_{probes} = \frac{P_{RF-1} - P_{RF-2}}{2} \tag{2-15}$$

Finally, the step 3 is similar to step 1 and provides the available power ($P_{\text{LO-1}}$) at the attenuator output for the LO chain. The RF and LO power delivered to the Device Under Test (DUT) is calculate as:

$$P_{RF} = P_{RF-1} - L_{probes} \text{ and } P_{LO} = P_{LO-1} - L_{probes} \tag{2-16}$$

2.13.3 Noise measurement setup

For the noise measurement setup, the LO power is provided by the same LO chain as in the previous configuration while an ELVA-1 WR-12 RF noise source is directly connected to the RF port. This configuration is detailed in Figure 2-33.

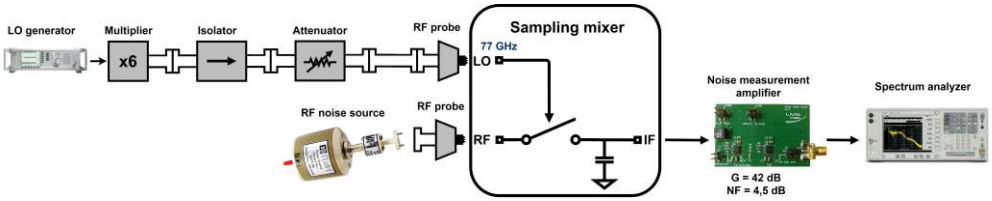

Figure 2-33: Noise measurement setup.

The IF output noise power is measured using an Agilent E4440A spectrum analyzer. As the measured circuits do not have enough gain, a Printed Circuit Board (PCB) noise measurement amplifier must be added before the spectrum analyzer to increase the measured noise floor. Otherwise, the measured noise level may be too close to the analyzer noise floor to be accurately measured. This amplifier is also used to recombine the IF output differential signals thus avoiding difficulties coming from differential NF measurements. This noise measurement amplifier is described in Figure 2-34.

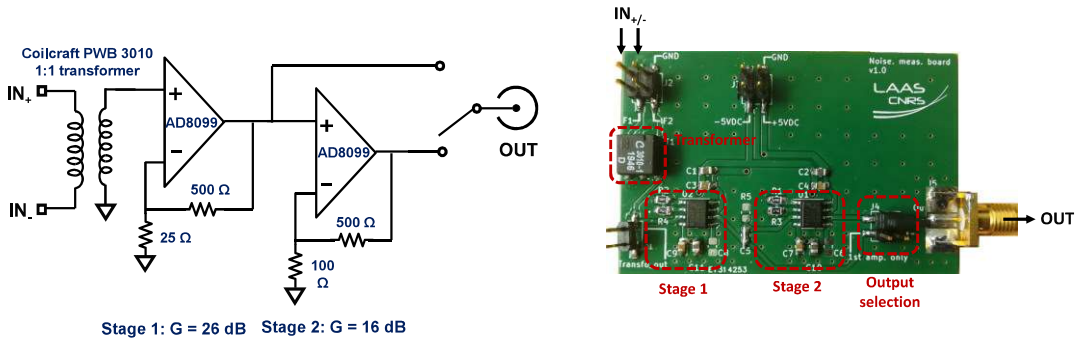

Figure 2-34: Noise measurement amplifier.

The designed noise measurement board includes a Coilcraft PWB-3010 transformer for differential to single-ended conversion and two AD8099 OP-amp amplifying stages. When both stages are used, this amplifier provides around 42 dB of voltage gain associated with a 4.5 dB NF over a 50 MHz frequency range.

2.13.4 PCB test board and chip mounting

For its characterization, the chip is reported and wire-bonded on a PCB test board supporting DC supplies and IF outputs. RF and LO signals are applied by way of 60-90 GHz GSG RF probes. The designed PCB test board and the chip integration are shown in Figure 2-35. The sampling mixer circuit presented in this chapter is implemented with other circuits designed for this PhD work in a 28FDSOI test chip. As circuits smaller than 1mm×1mm cannot be sawed from the wafer to be reported on the PCB, implementing several circuits on a test chip is necessary. Distributed in the four quarters of the test chip, each circuit has the same DC pad and IF output pattern. Consequently, a single PCB design can be used to measure all the prototypes. When reported on the PCB, test chips only need to be rotated by 90° to choose the circuit to be under test.

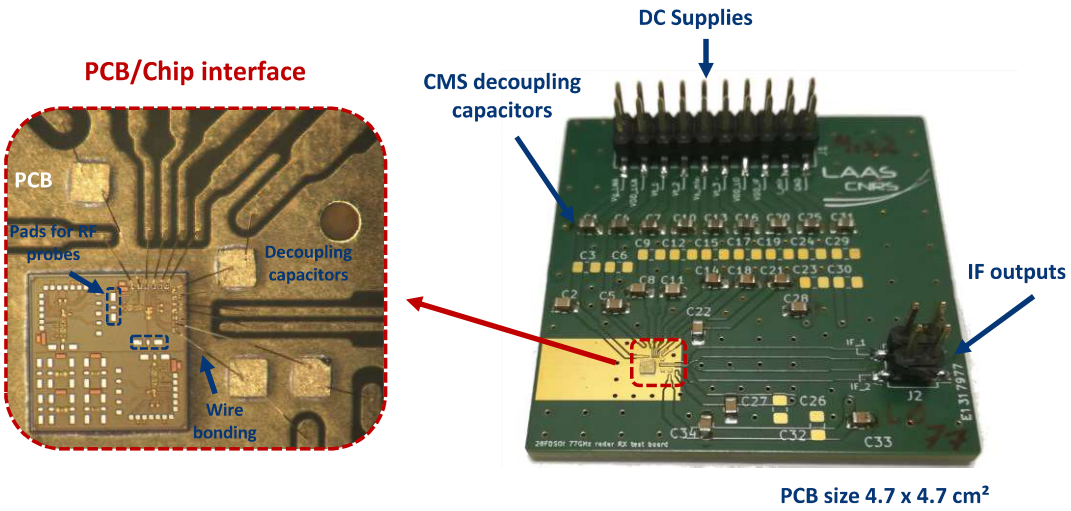

Figure 2-35: PCB test board and chip mounting.

2.14 77 GHz sampling mixer measurement results

2.14.1 Conversion gain and linearity

The voltage conversion gain of the sampling mixer is reported in Figure 2-36, for an RF frequency between 76 and 81 GHz and compared with simulated data. The pulse shaper varactors body voltage V_{tune} leading to the best simulated performances was selected for the measurements. RF and LO frequencies are both set from 76 GHz to 81 GHz in order to keep f_{IF} constant at 20 MHz. These measurements are performed with a 0-dBm LO input power and include the RF input balun performances. The measured G_{cv} varies between 7 dB and 8.5 dB in the f_{RF} range 76-81 GHz showing a good agreement with simulations.

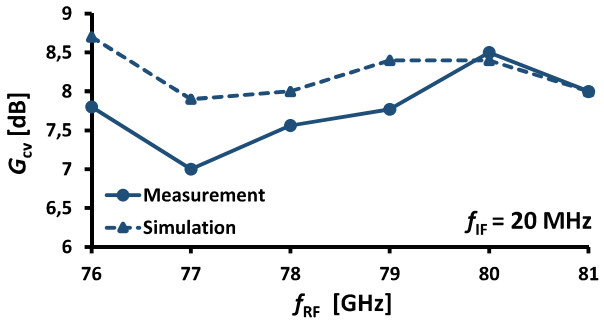

Figure 2-36: measured G_{cv} variations vs f_{RF}.

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 2-37. RF and LO frequencies are respectively set to 78.02 GHz and 78 GHz. The extracted G_{cv} and ICP1dB are respectively 7.5 dB and -1.5 dBm.

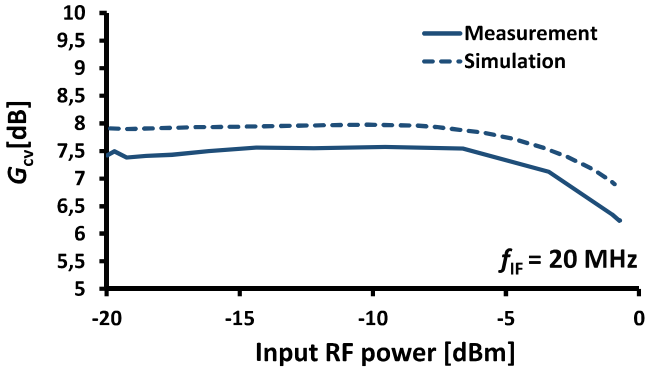

Figure 2-37: G_{cv} vs the input RF power at 78 GHz.

The simulated voltage transformation ratio of the RF input balun is considered to extract its contribution from the measured G_{cv} and ICP1dB. In these conditions, the G_{c_v} becomes -0.7 dB and an input -1 dB compression voltage (V_{1dB}) is 1.37 $V_{p\text{-}p}$. Voltage is used here to express the mixer compression point as it is more relevant for a high Z_{in} block. This voltage is equivalent to an ICP1dB of + 6.7 dBm in a 50 Ω system.

2.14.2 Noise figure

2.14.2.1 IF output follower stage noise measurement

The Noise Figure is measured using the cold source method [48]. The RF noise source in OFF mode is used as a 50 Ω resistance at room temperature T_R (≈ 297 °K). The noise power at the circuit output (N_{out}) is amplified by the noise measurement amplifier (2.12.3) and measured with a spectrum analyzer. Finally, the NF is calculated as:

$$NF = \frac{N_{out}}{k.T_R.G_{c_v}^2} \quad (2\text{-}17)$$

The OP-amp follower output buffer is only used to isolate the mixer from the measurement setup and must not be considered in the mixer performance. Consequently, it has been characterized in a standalone configuration to extract its noise contribution from the mixer NF

measurement. Its measured input-referred noise ($V_{n\,in}$) in the f_{IF} range 1-30 MHz is reported in Figure 2-38.

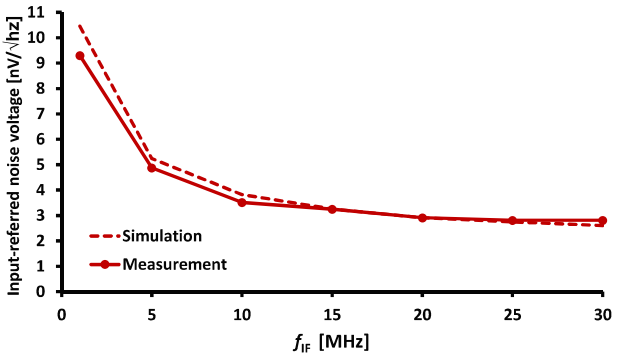

Figure 2-38: *IF* output stage input-referred noise versus f_{IF}.

The measured value at an IF frequency of 20 MHz is 2.9 nV/√Hz. This noise contribution can be extracted from overall NF_{SSB} measurements. Removing this noise contribution gives:

$$NF_{SSB\,mix} = NF_{SSB\,meas} - \frac{v_{n_{in}}^{2}}{k.T_r.\mathrm{R_s}.G_{c_v}^{2}} \tag{2-18}$$

2.14.2.2 Mixer noise measurement

The Measurements of the NF_{SSB} of the sampling mixer in the f_{RF} range 76-81 GHz with an IF frequency of 20 MHz are reported in Figure 2-39. These measurements were also performed using the cold source method and include the noise of the IF buffer which will be extracted later. The NF_{SSB} is measured between 10.5 dB and 13 dB a in the f_{RF} range 76-81 GHz in good agreement with simulations.

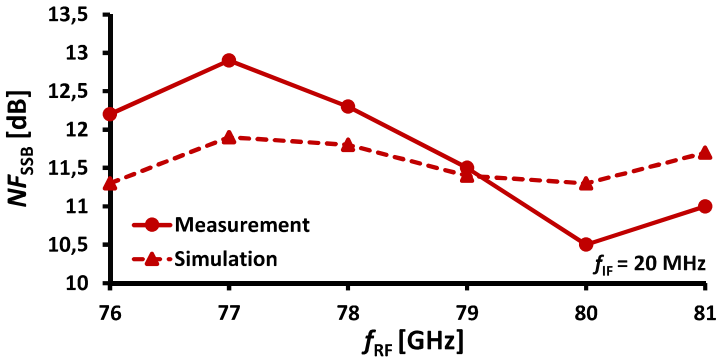

Figure 2-39: sampling mixer NF_{SSB} versus f_{RF}.

Finally, Figure 2-40 shows the NF_{SSB} with a LO frequency of 78 GHz and an IF frequency range up to 30 MHz. An increase of the NF_{SSB} for f_{IF} below 20 MHz can be noticed, due to the IF OP-amp *1/f* noise. The measured value of NF_{SSB} is 12.3 dB at 20 MHz. The measured NF_{SSB} of the sampling mixer at 20 MHz becomes equal to 9.1 dB after removing the noise contribution of the OP-amp follower.

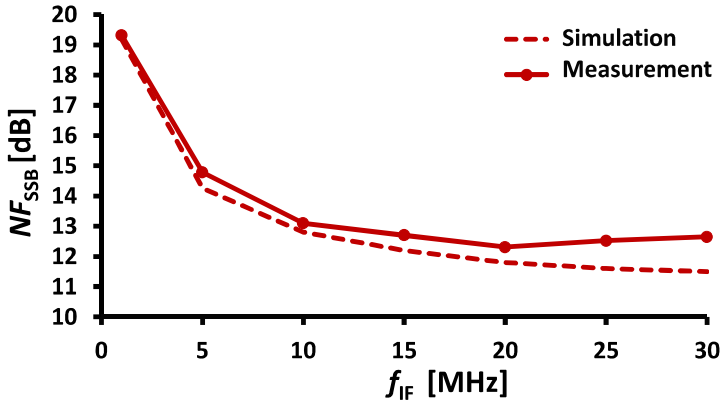

Figure 2-40: sampling mixer NF_{SSB} at an f_{RF} of 78 GHz.

2.15 Performance summary and conclusion

Sampling mixer measured performances after the RF balun and IF output buffer de-embedding are summarized on Table 2-1. Because of time constraints, only one sample of this circuit was measured.

Table 2-1: Sampling mixer measured performances.

f_{LO} [GHz]	f_{IF} [MHz]	G_c [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{LO} [dBm]	P_{dc} [mW]
78	20	-0.7	+6.7	9.1	0	10 + 23*

* IF output follower consumption

These measurements demonstrate that the implementation of the proposed LO pulse shaper results into a sampling mixer which exhibits a good conversion gain associated with a high linearity. Moreover, these results highlight that sampling mixers allow to break the voltage conversion gain limitation of 2/π which applies for conventional sine driven passive mixers.

To conclude, in this chapter, a new sampling mixer, operating at millimeter-wave frequencies, is proposed. The discussion puts forward that driving the mixer with a low duty

cycle LO signal, in association to a capacitive load, creates a sampling behaviour improving the conversion gain and the linearity, when compared with sine driven mixer. Nevertheless, the generation of a low duty cycle signal at 77 GHz is a critical point. As a solution, an innovative 77 GHz pulse shaper able to turn the LO signal into a pulsed waveform is introduced. The implementation of the LO pulse shaper within a double-balanced passive mixer in a 28-nm FD-SOI CMOS technology validates this new sampling mixer topology. According to these results, this sampling mixer appears as a good candidate to satisfy automotive radars stringent requirements.

As standalone passive mixers are not presented in the literature related to CMOS 77 GHz radar receivers, a meaningful comparison between this sampling mixer and other solutions is a bit difficult. However, this sampling mixer topology implementation with a LNA in a 77 GHz front-end will be presented in chapter 4. The performances of the full radar front-end will help to provides a proper comparison with others 77 GHz radar receivers.

Chapter 3 Design of a 77 GHz passive sub-sampling mixer in 28-nm FD-SOI CMOS technology

3.1 Introduction

The 77 GHz sampling mixer presented in the chapter 2 proves that the sampling principle can be efficiently extended to millimeter-waves. Nevertheless, implementing a 77 GHz LO chain to drive the mixer is not straightforward as it generally requires a 38.5 GHz VCO, frequency doublers and highly consuming 77 GHz amplifying stages.

To avoid this complexity, a solution could be found by replacing fundamental mixers with sub-harmonic mixers that use a LO frequency sub-multiple of the RF frequency (f_{RF}/n with n a natural integer). This solution has already been considered for the first generations of 77 GHz radar receivers [30], [49]. However, as sub-harmonic passive mixers often result in prohibitive conversion losses, high-frequency architectures mostly rely on sub-harmonic active mixers. At lower frequencies, passive sub-sampling mixers as in [37] are widespread and are characterized by low conversion losses and good linearity. The aim of this chapter is then to evaluate the feasibility of this concept at millimeter frequencies on a recent CMOS FDSOI technology node through the design of a ×3 sub-sampling passive mixer operating at 77 GHz.

First, this chapter introduces the sub-sampling mixer principle, which is a particular case of the sampling mixer principle presented in the chapter 2. Then, the proposed topology is detailed with a focus on the 26 GHz LO signal shaping method. Finally, the implementation of this mixer with the 28-nm FD-SOI CMOS technology is described and measurement results validating this work are given.

3.2 Existing topologies of millimeter-wave sub-harmonic mixers

Sub-harmonic mixers are generally used to avoid difficulties due to the high frequency LO generation or to address frequency bands above transistors limits (f_t). This section describes the main sub-harmonic mixer topologies found in the literature within millimeter-wave CMOS receivers.

3.2.1 Active Gilbert cell-based sub-harmonic mixers.

Most of active sub-harmonic mixers encountered at millimeter-wave frequencies are based on the widespread Gilbert mixer topology [30], [49]. The operation of the sub-harmonic Gilbert cell is depicted in Figure 3-1. Each mixing transistor used in a conventional Gilbert cell is replaced by two paralleled transistors as in Figure 3-1.a (M_1 and M_2). These two paralleled transistors act as a frequency doubler embedded in the Gilbert cell mixing core. M_1 and M_2 need to be driven by two LO voltages featuring the same frequency f_{LO} and magnitude but with opposite phases. By setting the transistors gate voltage as described in Figure 3-1.b (respectively in blue and red), M_1 and M_2 are alternatively conducting at $2f_{LO}$ frequency. This way M_1 and M_2 act as a single mixing transistor operating with an equivalent $2f_{LO}$ drive, as illustrated in Figure 3-1.b (grey waveform).

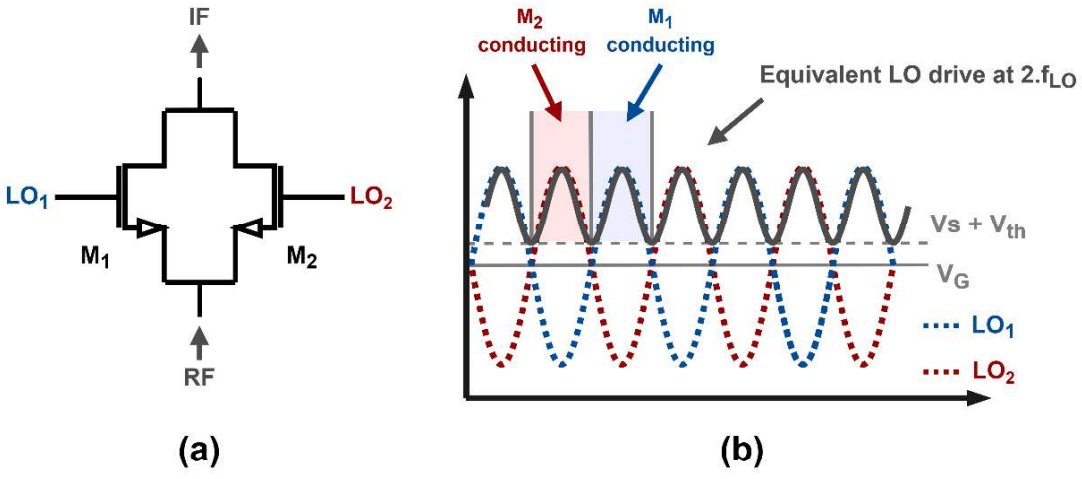

Figure 3-1: (a) Sub-harmonic Gilbert cell operating principle (b) LO waveforms.

An example of double-balanced ×2 sub-harmonic Gilbert cell employing this principle is drawn in Figure 3-2. [50] demonstrates that this principle can be extended to a ratio n (f_{RF}/f_{LO}) higher than 2 by paralleling n transistors. In this case, n LO phases will be required to drive a single balanced mixer and $2n$ for a double-balanced mixer.

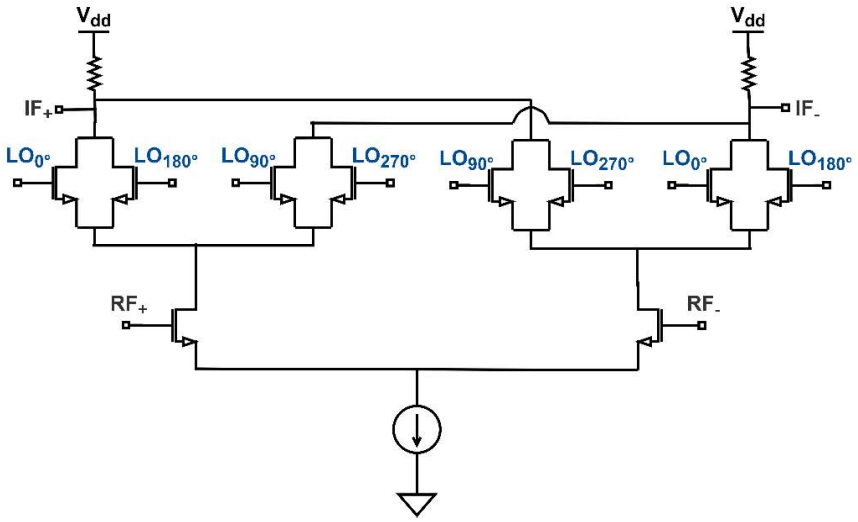

Figure 3-2: Example of conventional x2 Sub-harmonic Gilbert cell.

The advantage of these actives topologies is their ability to provide a conversion gain which can be helpful to keep a good NF at receiver level. However, Figure 3-1.b shows that the magnitude of the equivalent $2f_{LO}$ drive is significantly lower that the magnitude of the signals $LO_{1/2}$. It often results into a poor linearity degrading the overall receiver performances. The extension of this principle to n values higher than 2 is also difficult as a circuit generating the $2n$ LO phases is required.

3.2.2 Passive subharmonic mixers

Only a few passive subharmonic mixers are represented among the published millimeter-wave CMOS receivers. The more spread approach to design sub-harmonic passive mixers is to use cascaded passive mixers core driven by time delayed LO signals. In [51] and [52], this approach is used to convert a RF frequency of 24 GHz by using a 12 GHz LO signal as depicted in Figure 3-3.

The Figure 3-3 shows that when two cascaded double-balanced CMOS passive mixers are driven by LO signals with a 90° phase shift, the whole operates exactly as a double-balanced CMOS passive mixer driven by a fictive $2f_{LO}$ LO signal. The LO waveforms represented in

Figure 3-3.b illustrate the behaviour of the whole mixer. The main advantage of this topology is that the conversion gain remains equal to - 4 dB regardless of the *n* ratio between RF and LO frequencies. This solution also benefits from a better linearity than active subharmonic Gilbert cells. As the conventional passive mixer described in chapter 2, this kind of mixer can operate in a current or a voltage mode depending on the load impedance value defined between IF ends.

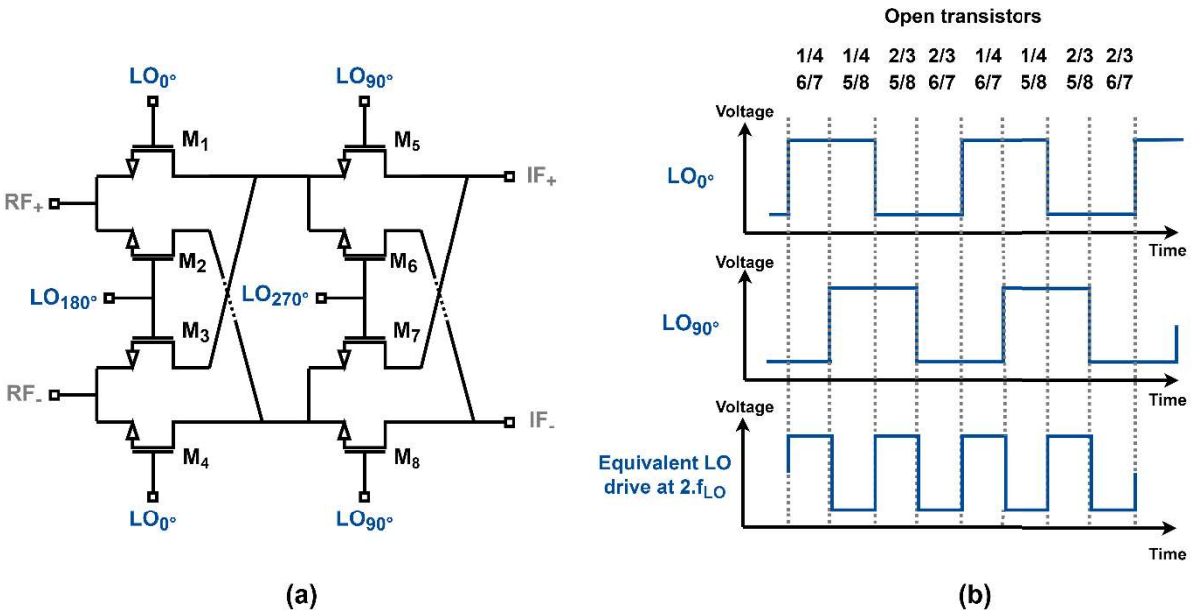

Figure 3-3: (a) Sub-harmonic passive mixer (b) LO waveforms.

In [53] this principle is extended to four cascaded mixers to reach frequencies around 80 GHz. However, passive subharmonic mixers also require 2*n* LO phases. In addition, the conversion gain degradation due to the error between the LO phases and the transistors ON-time increases with *n*. Using more cascaded mixers will also lead to higher r_{on} on the signal path bringing more converted thermal noise at the mixer output.

3.2.3 Low-frequency sub-sampling mixers

As previously discussed in chapter 2, at lower frequencies, the use of sub-sampling mixers with important *n* ratio as in [37] is well mastered. This principle translates into low conversion losses and good linearity without requiring a growing number of LO phases when the *n* ratio increases, its implementation towards millimeter frequencies is tempting. The following section demonstrates its feasibility to down-convert a 77 GHz signal using a LO signal *n* time lower than $f_{RF,}$ thus relaxing the constraints on the LO distribution chain.

3.3 Sub-sampling mixer operating principle

The sub-sampling mixer is based on the operating principle of the sampling mixer presented in chapter 2, with a ratio *n* greater than 1. As a result, sub-sampling can be used to design a sub-harmonic passive mixer exhibiting a high linearity, a low conversion loss and requiring less LO phases than the topologies previously described.

However, using sub-sampling mixers to lower the LO frequency increases the constraints on the LO pulse shape compared to a fundamental sampling mixer (*n*=1). This difficulty is illustrated in Figure 3-4 which shows the sub-sampling mixer conversion gain for different odd *n* ratios. Even *n* ratios are not represented as the double-balanced configuration of this topology rejects RF signals around even LO harmonics resulting in a zero conversion gain. The more *n* increases the more *D* must be kept low to keep a decent conversion gain. As low duty cycle LO signals are hard to generate at high frequencies, the possible choices for the ratio *n* are limited.

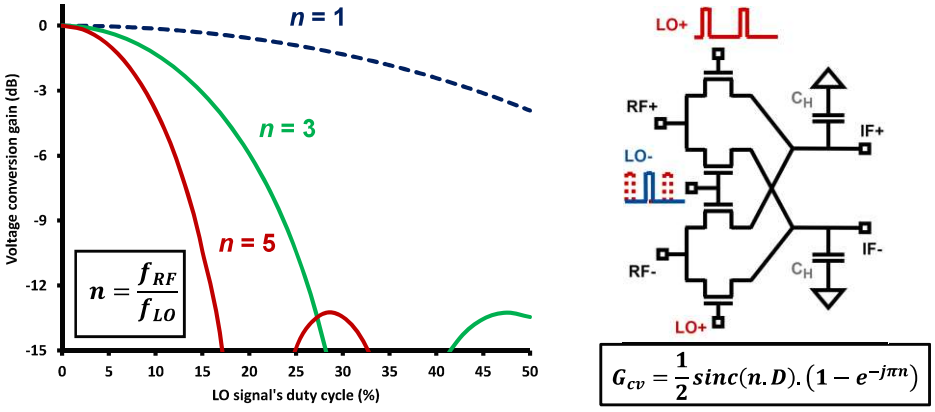

Figure 3-4: Conversion gain of the sub-sampling mixer on the right calculated for perfect switches.

Using a low duty cycle also affects the noise conversion. As described in chapter 2, such a mixer converts the noise present around each odd LO harmonic and the overall thermal noise added by the mixer follows a 1/*D* trend. Consequently, lowering *D* to get a decent conversion gain in sub-sampling mode results in a higher NF than for *n* = 1. Nevertheless, the input noise around the odd LO harmonics is generally filtered by the previous stages so only the input noise around 77 GHz and the thermal noise added by the mixer must be considered.

The most reasonable ratio *n* appears to be 3 to design a sub-sampling mixer operating at 77 GHz. This configuration corresponds to a LO frequency of 26 GHz and a duty cycle that

should be less than 20 %. These characteristics appear to be accessible to advanced nm-scale CMOS processes such as the 28-nm FD-SOI. The following section discusses the design of a 26 GHz LO pulse shaper based on logic gates.

3.4 26 GHz LO pulse shaper based on logic gates

3.4.1 Pulse shaper architecture

The architecture of the proposed differential pulse shaper is summarized in Figure 3-5. The differential driving of the mixer requires the generation of two pulse trains shifted by 180° with respect to each other. In each pulse shaper, two inverter chains A/C and B/D integrating a different number of stages are used to create square waveforms with the required time delay. This time delayed square signals are then turned into a pulsed signal by the AND gate. This solution provides a high LO voltage swing from 0 V to V_{DD} to the mixer. High driving voltages maximizes mixer linearity.

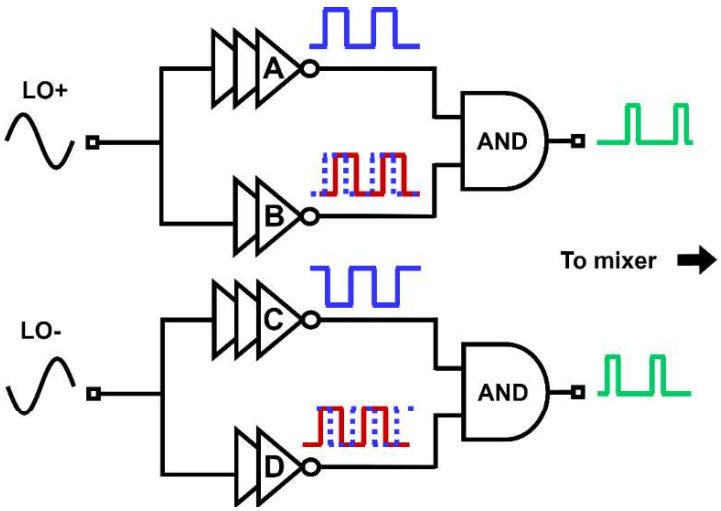

Figure 3-5: 26 GHz logic gates differential pulse shaper architecture.

This approach leads to quite low duty cycles but appears sensitive to process variations. Figure 3-4 shows that the conversion gain of a sub-sampling mixer with $n = 3$ quickly changes with the duty cycle. Process variations can significantly change the propagation delay of logic gates. As it turns into duty cycle fluctuations, it can lead to an important degradation of the conversion gain. As a solution, a LO duty cycle tuning capability is provided by the circuit. In FD-SOI technologies the body voltage can be used to tune the threshold voltage V_{th} of the

transistors. In each inverter, applying a tuning voltage V_{tune} at the NMOS transistor body and -V_{tune} at the PMOS transistor body creates a V_{th} shift resulting in a different inverter time delay. Finally, changing the delay between the square signals before the AND gate directly changes the LO signal duty cycle. Opposite values of tuning voltages are chosen for the inverter chains A and B to increase the duty cycle tuning range.

3.4.2 Pulse shaper implementation

The logic gates used in this 26 GHz pulse shaper are described in Figure 3-6. The layout of the whole differential pulse shaper is shown in Figure 3-7.

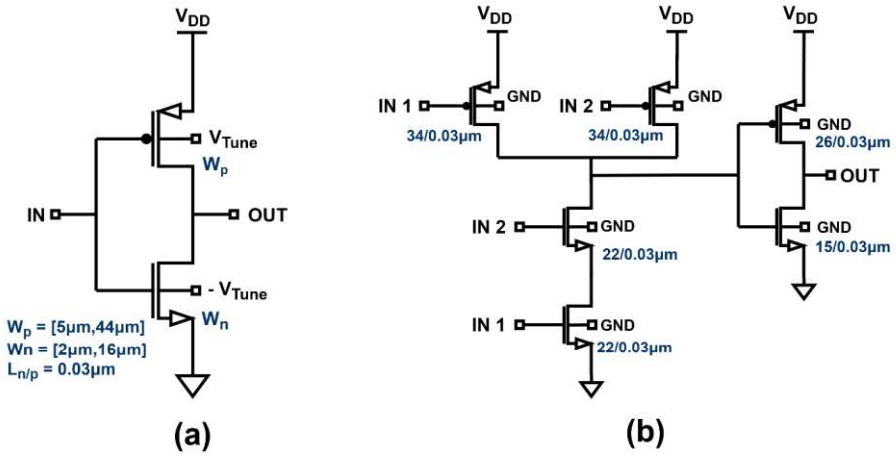

Figure 3-6: (a) Tunable delay inverter, (b) AND gate.

As the transistor gate capacitances limit the high-frequency gain of complex logic gates, gate length is set to the minimum value (30 nm) in the inverter chains. However, the width W_p and W_n of the transistors are not constant. The LO pulse shaper layout in Figure 3-7 shows that the transistor size is progressively increased along the inverter chains. This way, current capability of each inverter is progressively increased to ensure a proper driving of the loading stage gate capacitance.

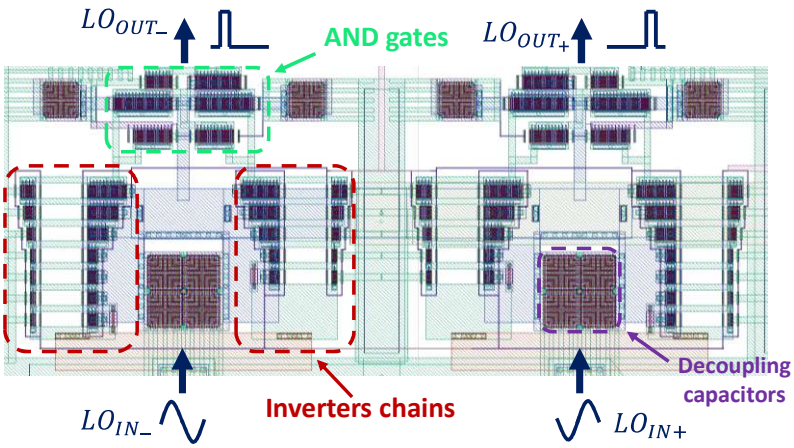

Figure 3-7: 26 GHz LO pulse shaper Layout.

To provide similar V_{th} in the inverters, PMOS gate width W_p is chosen between 2 W_n and 3 W_n. As in the 77 GHz pulse shaper presented in the chapter 2, decoupling capacitors connected between V_{DD} and ground are implemented as close as possible to the logic gates. Finally, a 10 kΩ resistor is implemented between the input and the output of the first inverter of each chain. The resistive feedback on this stage set the DC voltage of the inverters input to $V_{DD}/2$ without needing an additional DC voltage reference.

The inverter chains are connected to a NAND gate followed by an inverter to create the required AND gate (Figure 3-6.b). As for the previous stages, transistors sizes are adjusted to deliver enough current to the mixing transistors gate capacitances without presenting a too low capacitive impedance to the inverter chains. As PMOS transistors V_{th} are higher than NMOS ones, each body access is tied to the ground. Thus, PMOS V_{th} decreases to reduce the gap between both V_{th} values.

3.4.3 Generated LO waveforms

The pulse shaper DC power consumption is 36 mW under a 1.2V V_{DD}. The value chosen for this voltage is the result of a trade-off between the LO swing required to optimize the linearity of the mixer, the circuit power consumption and transistors reliability. In an inverter the transistors never experience high V_{GS} and high V_{DS} at the same time making it less sensitive to Hot Carrier Injection, even with 1.2V supply voltage. Figure 3-8 shows the output voltages of the A and B inverter chains (Figure 3-5).

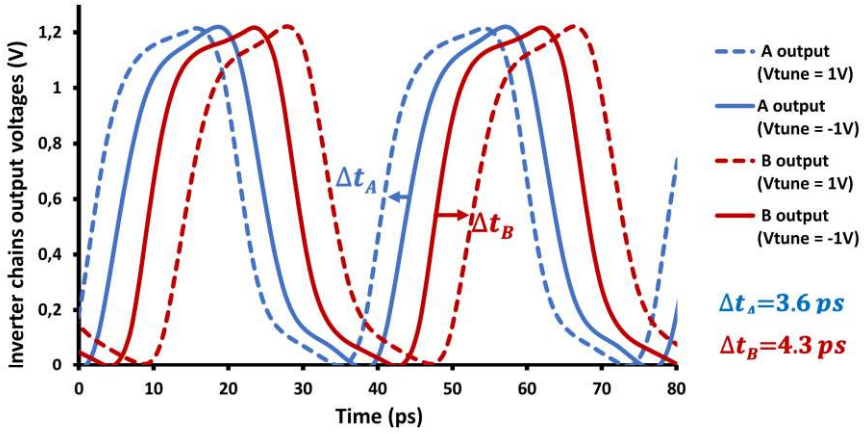

Figure 3-8: Inverter chains output for different V_{tune}.

Transient simulation results of the 26 GHz LO pulse shaper are reported in Figure 3-8 and Figure 3-9. This simulation takes into account the parasitic effects due to the layout. Layout modelling includes momentum and a PLS extractions. In Figure 3-8, solid line and dot line waveforms correspond respectively to the minimum and the maximum time delay between A and B output signals. The maximum achievable time delay variation Δt_{max} ($\Delta t_a + \Delta t_b$) is equal to 7.9 ps ($0.2f_{LO}$) and is obtained with V_{tune} varying in the range of -1V to +1V.

The AND gate output voltage of one side of the pulse shaper for a LO frequency of 26 GHz is given for different values of V_{tune} in Figure 3-9. The tunable delay observed between the inverter chain output voltages results into a 19%-33% duty cycle tuning range without decreasing the LO voltage swing under 1.1V. When duty cycles are set under 19%, the LO swing becomes limited by the logic gates rise and fall times.

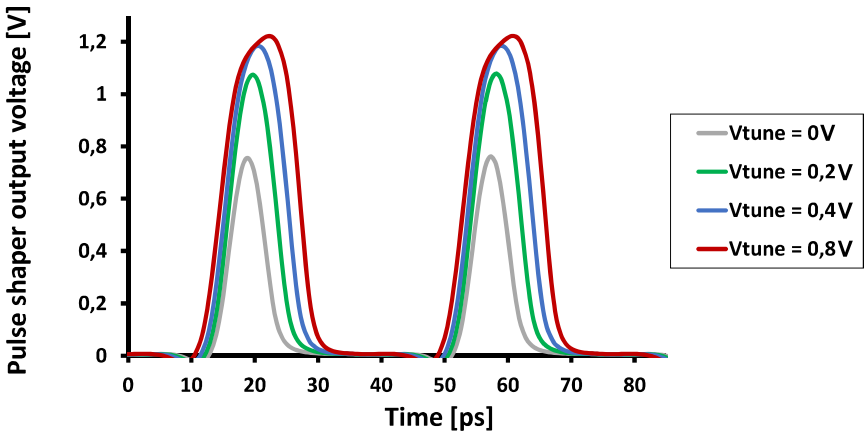

Figure 3-9: AND gates output for different V_{tune}.

This duty cycle is computed as $D_{LO} = \tau_{half}/T_{LO}$ with τ_{half} the pulse width at half magnitude. The duty cycle can be different depending on the pulse magnitude level considered to compute the pulse width τ. As a result, fixed V_{tune} the duty cycle of the mixer conductance can be adjusted by changing the pulse level relatively to the mixing transistors V_{th}. This strategy can be used to adjust the mixer conversion gain with a fixed LO signal.

3.5 Sub-sampling mixer core implementation

3.5.1.1 Mixer core implementation

The sizing of the mixing transistors and its hold capacitors being very similar to the circuit described in chapter 2, it will not be detailed here. As for the sampling mixer, the mixing transistors geometry is 15 µm / 30 nm and the value of the hold capacitors is 300 fF.

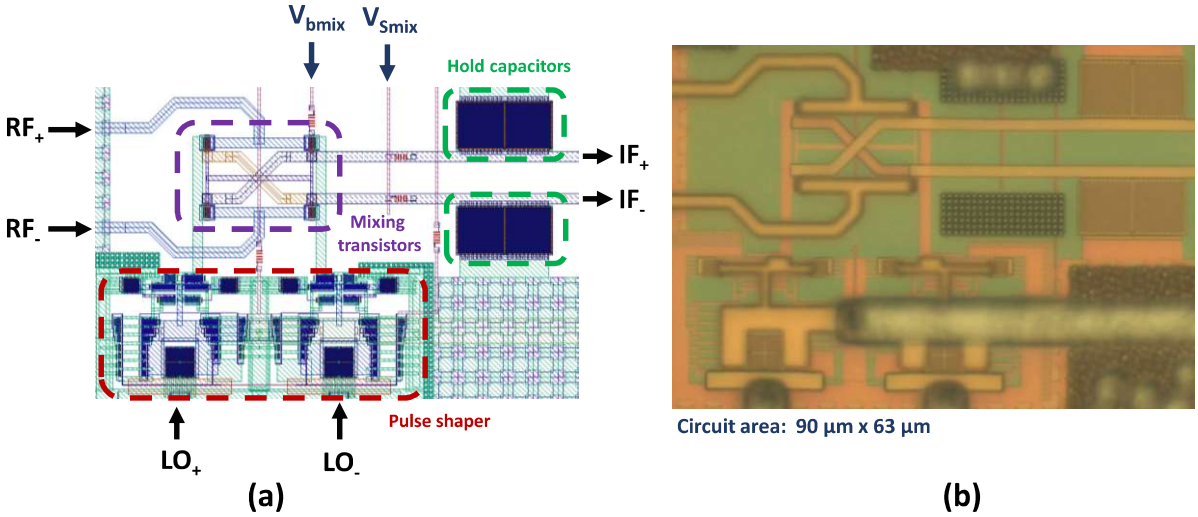

Figure 3-10: (a) Sampling mixer core layout, (b) detail of the manufactured chip.

Figure 3-10.a depicts the layout of the sub-sampling mixer core including the mixing transistors, the 300 fF hold capacitors and the DC supplies. The logic gates are also represented. This architecture allows to implement the pulse shaper very close to the mixer core avoiding LO signal degradation and leading to a very compact sub-sampling mixer.

As in chapter 2, the DC voltage on the source/drain of the mixing transistors (V_{Smix}) is set close to 0.6V to bias the IF stage while the LO waveform is centered on 0.6V ($V_{DD}/2$). The biasing strategy of the mixing transistors is described in Figure 3-11.

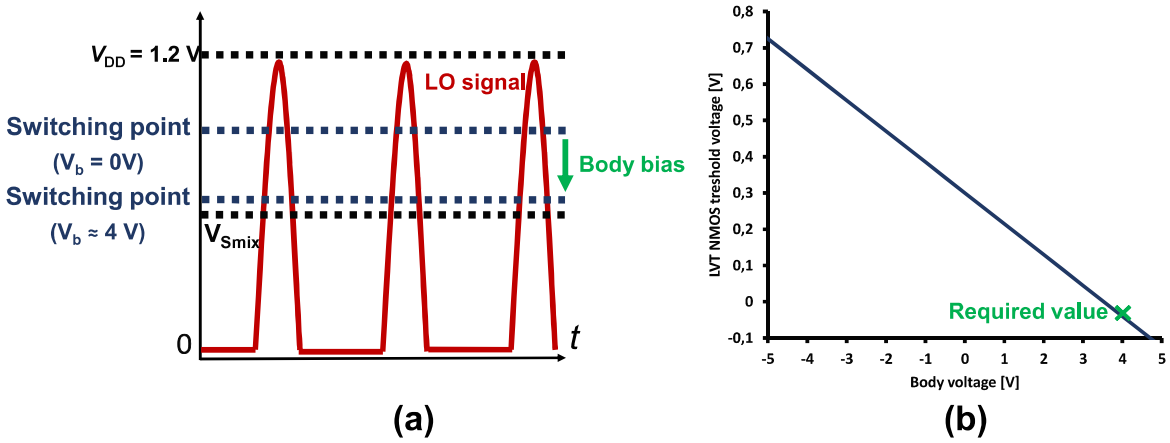

Figure 3-11: (a) Mixing transistor biasing (b) Body bias voltage setting.

To avoid losses, no coupling capacitance has been inserted in the LO path. This mean that transistor switching voltage must be close to $V_{DD}/2$. Actually, the switching point is close to 0.9V ($V_{Smix} + V_{th}$). Hence, body bias is used to bring this value as close as possible to 0.6V as illustrated on Figure 3-11.

3.5.2 RF and LO input matching

The RF input balun for the sub-sampling mixer has a 1:2 turns ratio and has a quite similar sizing as the RF input balun of the sampling mixer seen in chapter 2. Therefore, it will not be detailed here. The simulated RF input reflection coefficient is reported in Figure 3-12.

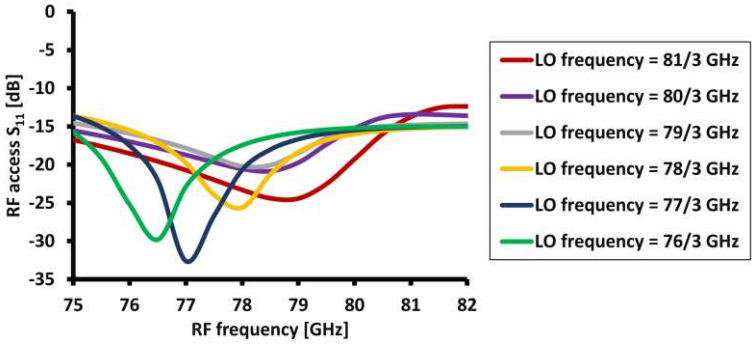

Figure 3-12: RF input reflection coefficient for several LO frequencies.

The large signal harmonic balance simulation shows the RF matching for f_{LO} in the range of 76-81 GHz. This mixer has a good RF matching between 76 and 78 GHz but its input impedance makes it difficult to match over the whole band. Nevertheless, the S_{11} remains lower than -14 dB between 76 and 81 GHz.

The input impedance of the 26 GHz LO pulse shaper is high because of the very small gate capacitances brought by the first inverter stages. A parallel 50 Ω resistor is attached to the ground plane on each input of the balanced LO pulse shaper to provide impedance matching. A 0.9 pF capacitor is implemented as DC block between the 50 Ω resistors and the ground plane. This matching network is described in Figure 3-13.a. This configuration was preferred to a single 100 Ω resistors between both inputs of the pulse shaper to set the differential and common mode impedance at the same time. Only setting the differential mode would provide a proper LO matching but would results into a high common mode impedance. This uncontrolled common mode impedance could lead to oscillations in the pulse shaper.

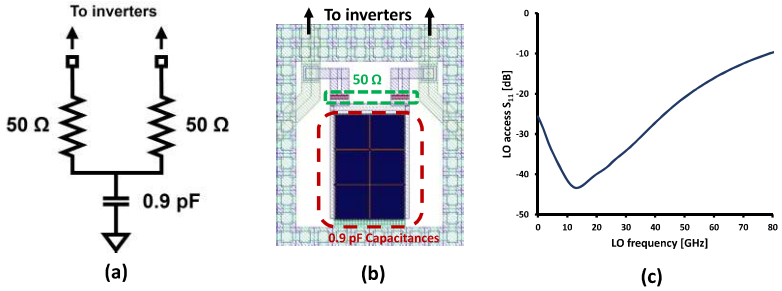

Figure 3-13: LO access matching (a) schematic (b) layout (c) LO access input reflection coefficient.

Figure 3-13.b shows the simulated LO input reflection coefficient. This broadband matching network leads to a proper RF matching up to 50 GHz thus covering the required 25 – 27 GHz frequency band for LO signal.

3.5.3 Standalone mixer simulated performances

3.5.3.1 Gain and linearity

Harmonic balance simulations including global layout modelling using momentum and PLS extractions have been carried out using an RF frequency of 78.02 GHz, a LO signal of 26 GHz and an IF frequency of 20 MHz to extract the performances of the mixer. The simulated voltage conversion gain of the circuit as a function of RF input level is plotted in Figure 3-14. The duty cycle of the pulse shaper and the body voltage of the mixing transistors was tuned to find the best trade-off between conversion gain and linearity. Under these conditions, the sub-sampling mixer shows a simulated conversion gain of -3.5 dB. The input-referred 1 dB compression voltage is 0.9 $V_{p\text{-}p}$. As in chapter 2, voltage is preferred to express the input compression point considering the high Z_{in} of the mixer. An equivalent ICP1dB of +3 dBm is derived.

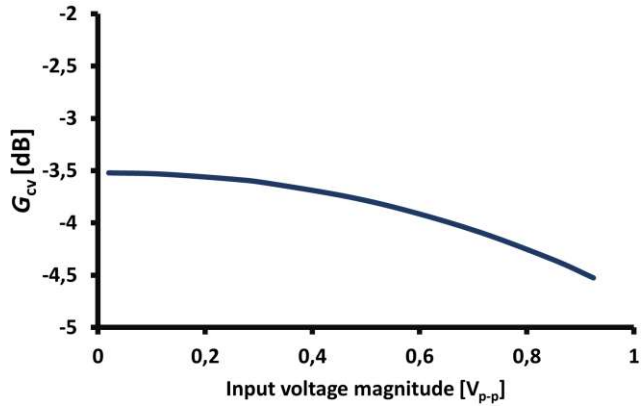

Figure 3-14: Voltage conversion gain compression curve.

This result shows that the sub-sampling principle can be used effectively used at millimeter-wave frequencies to design passive mixers using a LO frequency tree times lower than the RF frequency while benefiting from good linearity and an attractive conversion gain. Even if these performances are lower than the ones obtained with the sampling mixer in chapter 2, the chapter 4 will demonstrate that they remain suitable for the radar application. They also appear as very attractive when compared with other 77 GHz sub-harmonic mixers.

3.5.3.2 Noise

A non-linear noise simulation has been performed as well. The NF_{SSB} involving a 50 Ω RF source is plotted in Figure 3-15 with a LO frequency of 26 GHz and an IF frequency swept from 1 MHz to 25 MHz.

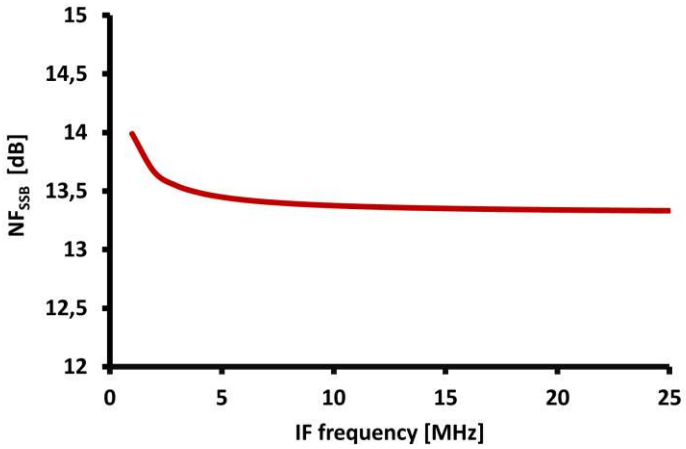

Figure 3-15: Sub-sampling mixer NF_{SSB}.

At an IF frequency of 20 MHz, the NF_{SSB} is 13.3 dB. As expected, the sub-sampling mixer exhibits a lower conversion gain compared to the sampling mixer in chapter 2 due to the

frequency translation of noise around the odd LO harmonics. Nevertheless, when compared to others sub-harmonic mixers, this solution exhibits a good compromise between conversion gain, linearity, noise and the *n* ratio.

3.5.4 77 GHz sub-sampling mixer test chip

The architecture of the test chip for the standalone 28FDSOI 77 GHz sub-sampling mixer is depicted in Figure 3-16.a. A microphotograph of the manufactured chip is given in Figure 3-16.b. The whole circuit area represented in Figure 3-16.a is 0.81 mm × 0.54 mm.

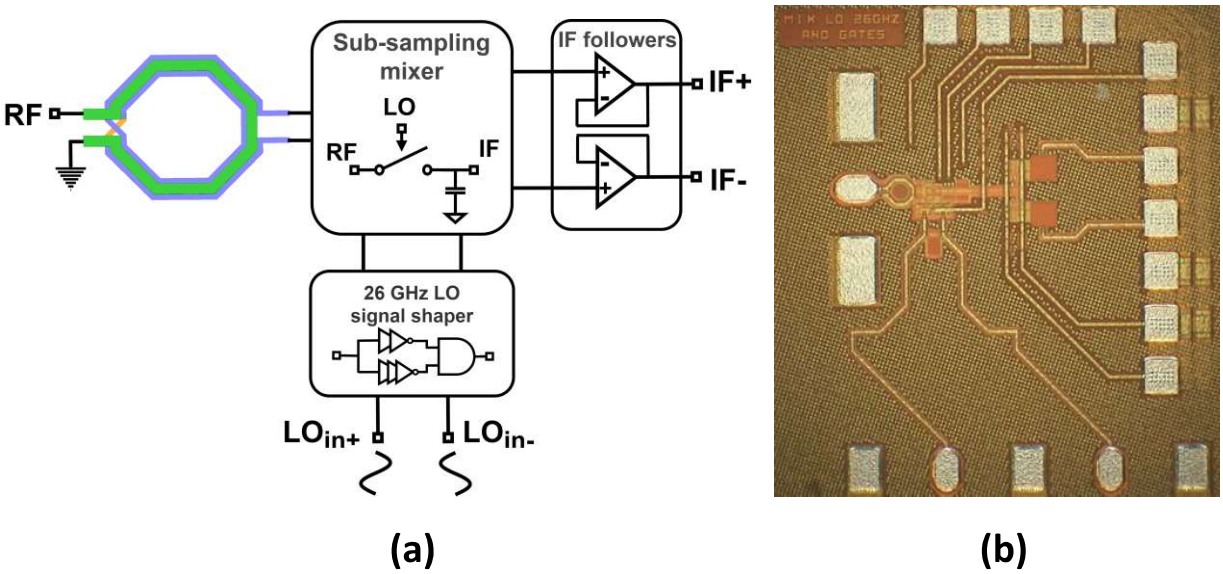

Figure 3-16: (a) mixer block diagram, (b) manufactured chip microphotograph.

As for the sampling mixer described in the chapter 2, a passive balun is added to provide a differential excitation of the mixer from the single-ended RF port and to improve its impedance matching. The balun exhibits a voltage gain of 8.1 dB at 78 GHz corresponding to the voltage transformation ratio. In this configuration, the required 26 GHz differential LO signal will be created externally using a 4-port PNA-X network analyzer source.

3.6 Sub-sampling mixer topology with co-integrated AND gates

3.6.1 Overcoming the frequency limitation of the LO pulse shaper

The 77 GHz sub-sampling mixer presented in the previous sections exhibits good performances thanks to the pretty low LO signal duty cycles reached with the logic gate pulse shaper. However, these duty cycles are a bit limited by the AND gate that represents the main limiting element. Because of its complexity, it limits the rise and fall times of the entire pulse shaper. This frequency limitation can be noticed on the LO voltage waveforms of Figure 3-9 when the duty cycle gets lower than 20%. To overcome this limitation, the AND function has been merged with the mixer core. This solution is presented in Figure 3-17 and the sub-sampling mixer core based on this idea is drawn in Figure 3-18. It will be referred as version 2 in the following.

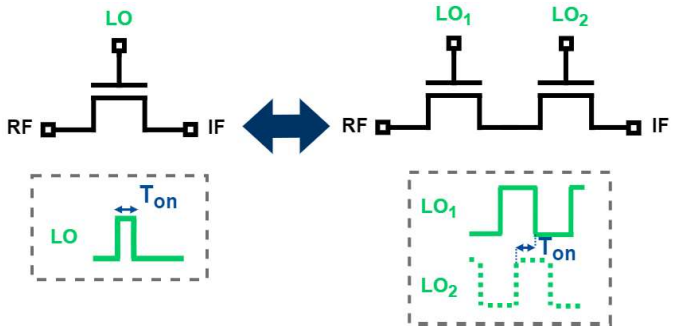

Figure 3-17: Co-integration of the AND function to the mixer core.

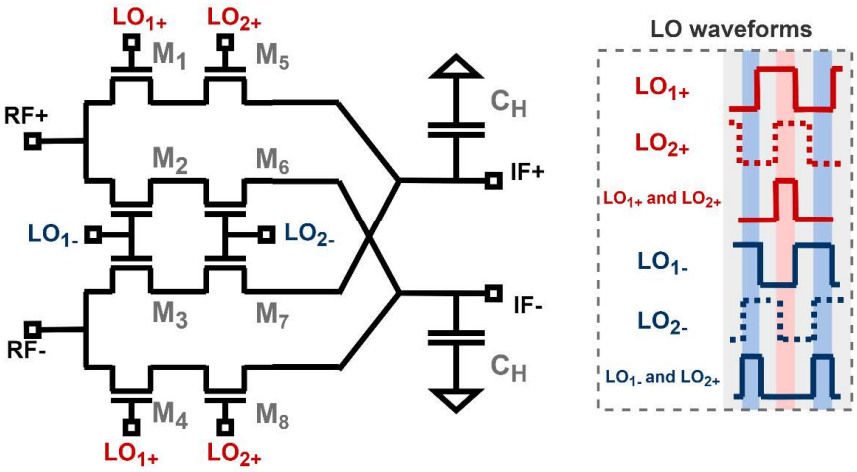

Figure 3-18: double-balanced sub-sampling mixer embedding the AND function within the mixer core.

The main behaviour of this second version does not change compared to the previously described circuit. Here, LO_2 is a new LO signal and represents the delayed version of LO_1. As an example (Figure 3-18), transistors M_1 and M_5 are both open only when LO_{1+} and LO_{2+} are simultaneously at the high state. This operation is equivalent to a single transistor driven with a pulsed LO signal with a duty cycle D of $T_{LO1+} \cap T_{LO2}/T_{LO}$ where $T_{LO1+} \cap T_{LO2}$ is the intersection time of LO_{1+} and LO_{2+}. This innovative approach suppresses the AND gate and its transition times to reach lower duty cycles. As a result, only inverter chains are needed to generate the required LO waveforms. Nevertheless, since two series transistors are involved in each branch of the mixer, this topology presents a higher r_{on} increasing the thermal noise.

Figure 3-19 shows the single-ended version of the LO signal shaper associated with this sub-sampling mixer. The sizing of the inverters is similar to the previous version and the AND gates have been removed. In this configuration, the time delayed square signals at the output of the inverter chains (Figure 3-8) are directly applied to the gates of the mixing transistors.

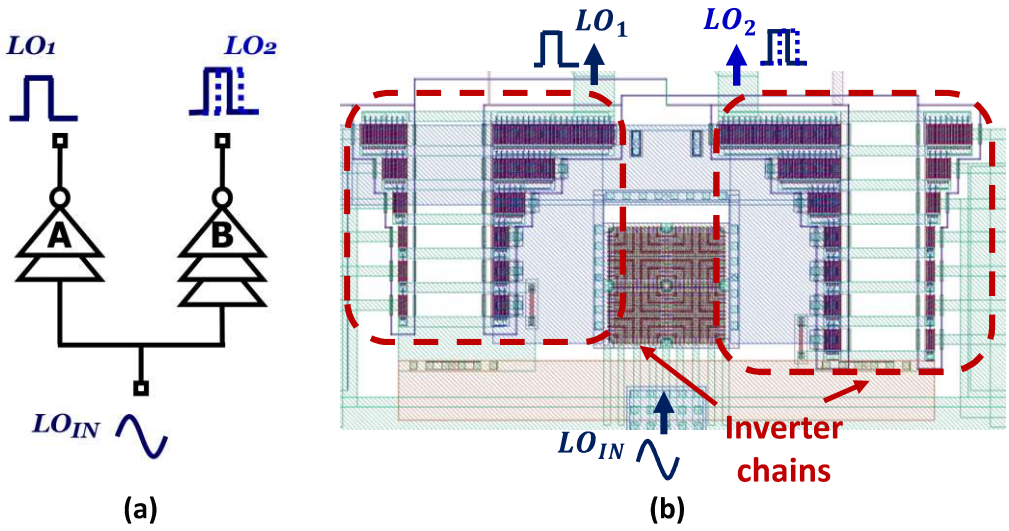

Figure 3-19:(a) single ended LO signal shaper (b) Signal shaper layout.

3.6.2 Mixer core implementation

Figure 3-20.a shows the layout of the sub-sampling mixer while Figure 3-20.b is a picture of the sub-sampling mixer with the RF input balun and the GSG pad. The mixer core layout and area are similar as for the version 1. The only difference is the two additional connections between the LO signal shaper and the mixer core with the embedded AND gates.

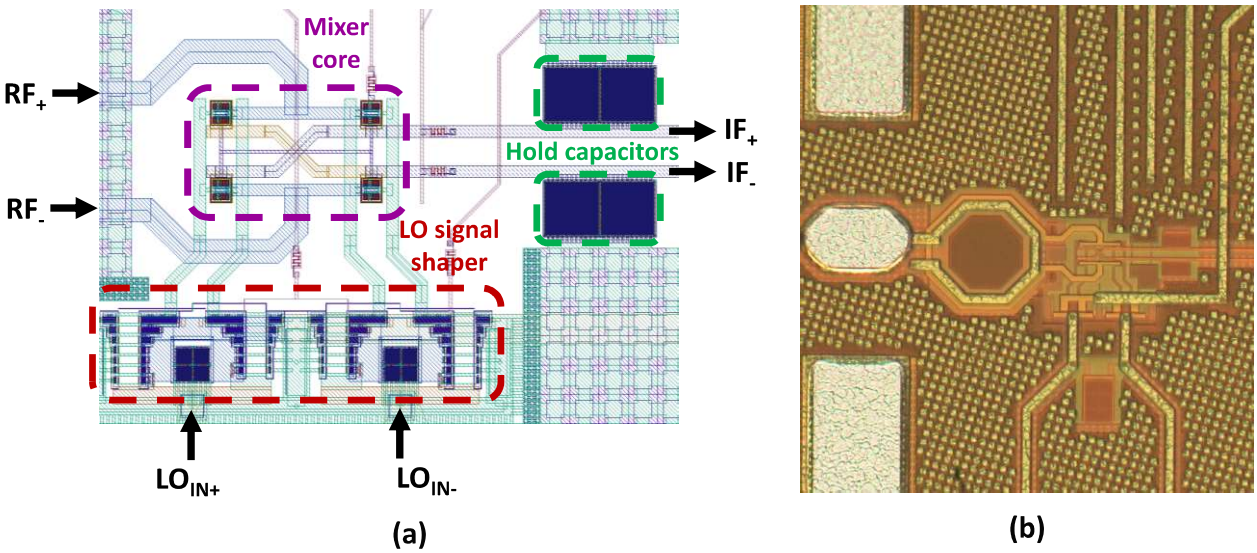

Figure 3-20: (a) Sub-sampling mixer core layout with LO signal shaper (b) Manufactured chip.

The sizing of the mixing transistors follows the same approach as for the other mixers studied. However, getting rid of the AND gates allow to increase the size of the transistors in the last inverters of the chains while exhibiting the same DC current consumption as for the pulse shaper in the version 1. As a result, the last inverter stages of this signal shaper provide square LO signals with sharper rising and falling edges than with the AND gates. We can now afford to use larger mixing transistors, which consequently have higher gates capacitances without detrimental effects on the linearity of the mixer. Larger transistors also mean lower r_{on} and thermal noise. The optimal geometry was found with a W/L ratio of 20µm/30nm.

The two mixing transistors connected in series finally benefit from a specific arrangement described in Figure 3-21. The interleaved layout of Figure 3-21.b is preferred over the conventional approach of Figure 3-21.a The interleaved layout merges the drain of the transistor T_1 with the source of T_2 to remove the parasitic capacitors and resistances associated with the connection to the first metal level (M_1) between T_1 and T_2. The layout of the interleaved mixing transistors implemented in the sub-sampling mixer is depicted in Figure 3-22 with the whole metal stack.

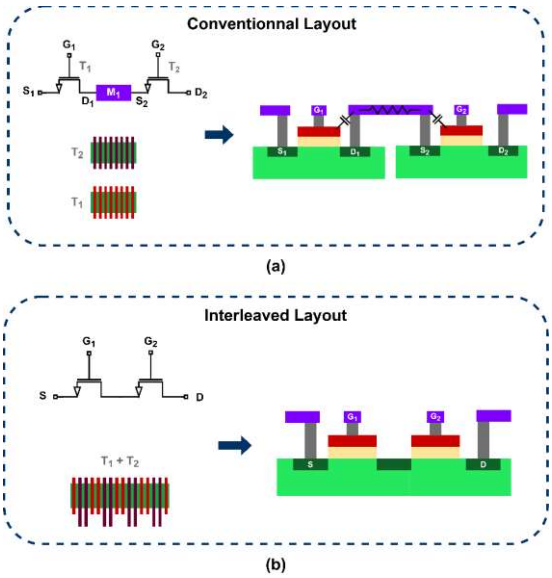

Figure 3-21: (a) Conventional layout for series transistors (b) Interleaved layout.

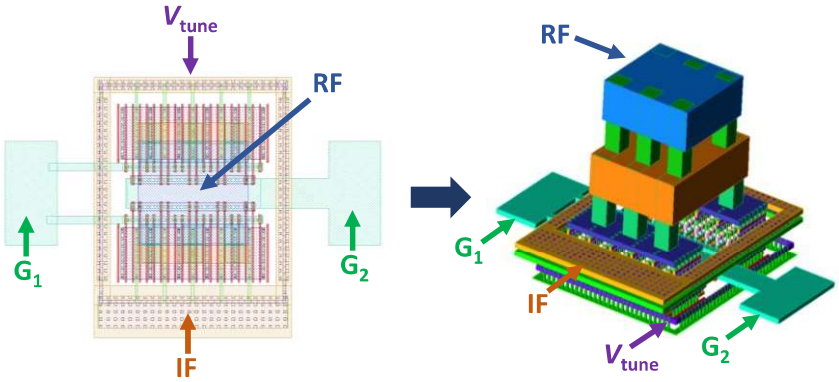

Figure 3-22: mixing transistor layout and 3D view.

3.6.3 RF input matching

The balun used to match the RF input is a bit different from those implemented in the previous mixers. Using two series mixing transistors rather than one increases the parasitic capacitances lowering the mixer RF input impedance. A balun with a 1:1 turns ratio was found to optimize the impedance matching.

The layout of the RF input of the mixer and its associated balun is drawn in Figure 3-23. The external diameter of the balun is around 70 µm. The width of the primary and secondary inductors are set to 4 µm. An input matching capacitance of 35 fF built using a MOM capacitor along with the GSG pad capacitance is employed. Two output matching capacitances of 40 fF are used.

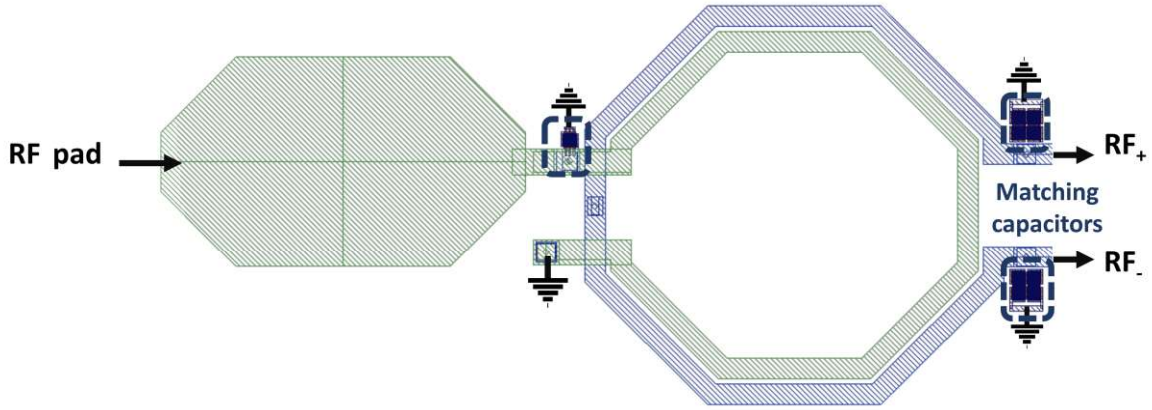

Figure 3-23: layout of the RF access matching network.

The large-signal harmonic balance simulation has been performed on the sub-sampling mixer to compute the RF matching for LO frequencies in the range of 76-81 GHz. These results are reported in Figure 3-24. The implemented RF balun provides a 4.8 dB voltage gain due to its voltage transformation ratio and a S_{11} lower than -15 dB is observed all over the 76-81 GHz frequency band. The LO matching is unchanged compared to the previous version.

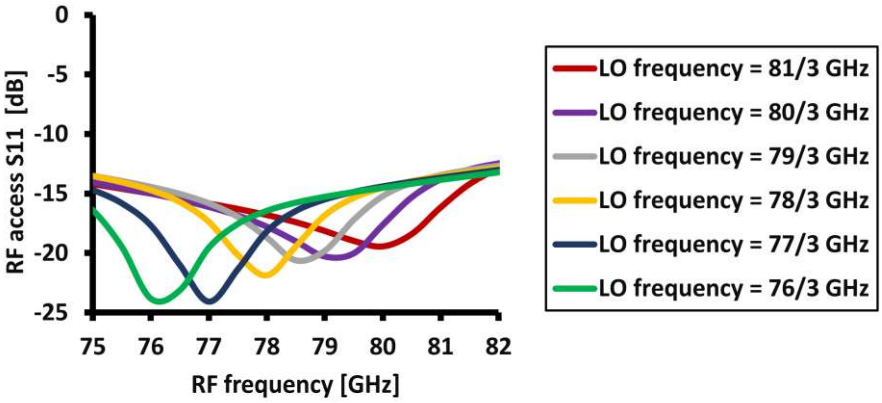

Figure 3-24: RF return losses plotted for several LO frequencies comprised between 25.33 and 27 GHz.

3.6.4 Standalone mixer simulated performances

3.6.4.1 Gain and linearity

The harmonic balance simulation results, with RF and LO frequencies respectively set to 78.02 GHz and 26 GHz are reported in Figure 3-25. This mixer and the previous version of sub-sampling mixer are simulated in the same configuration.

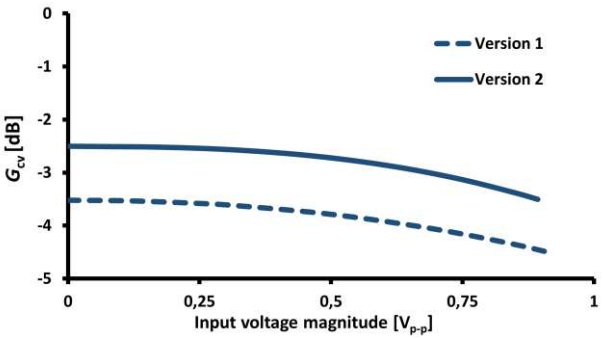

Figure 3-25: voltage conversion gain compression curves for version 1 and 2.

The simulated voltage conversion gain of the standalone sub-sampling mixer is depicted in Figure 3-25 and compared with the first version of the sub-sampling mixer. Under these conditions, the sub-sampling mixer with the AND gates embedded within the mixer core presents a conversion gain of -2.5 dB which is 1 dB higher than in the version 1. Its input-referred 1 dB compression voltage $V_{\text{-}1dB}$ is of 0.9 $V_{p\text{-}p}$ for an equivalent ICP1dB of +3 dBm. This value is identical to the previous version.

3.6.4.2 Noise

A harmonic balance-based non-linear noise simulation has been performed as well. The NF_{SSB} extracted form a 50 Ω RF source is plotted in Figure 3-26 for both versions of the mixer.

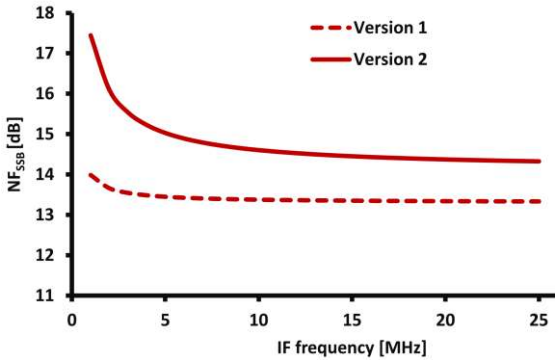

Figure 3-26: Sub-sampling mixer NF_{SSB} and comparison to version 1

The second version of sub-sampling mixer exhibits a NF_{SSB} of 14.4 dB at a 20 MHz IF frequency. As expected, the higher r_{on} resistance due to the cascade of the two mixing transistors increases the amount of thermal transposed in frequency. This increase is translated into a NF_{SSB} 1.1 dB higher than in the version 1. The performances of both versions of the 77 GHz sub-sampling mixer are summarized in Table 3-1.

Table 3-1: Simulated performances of the sub-sampling mixers.

Version	f_{RF} [GHz]	f_{LO} [GHz]	G_c [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{DC} [mw]
1	78	26	-3.5	+3	13.3	36
2	78	26	-2.5	+3	14.4	36

The better conversion gain of the version 2 of the mixer confirms that the AND gates in the mixer core turn into a lower LO duty cycle. On the other hand, this approach requires more mixing transistors leading to a higher NF_{SSB}.

3.7 Mm-wave measurement setup

The measurement setup is quite similar to the one introduced in chapter 2. The Figure 3-27 and Figure 3-28 shows the two setups, respectively for conversion gain and linearity measurements and for noise measurements.

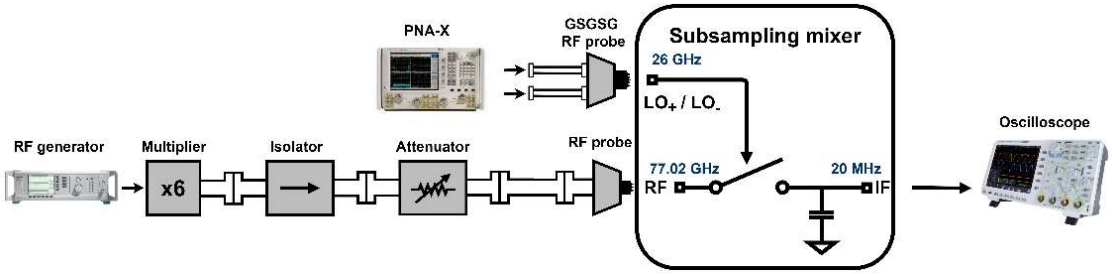

Figure 3-27: Sub-sampling mixer test setup for gain and linearity measurements.

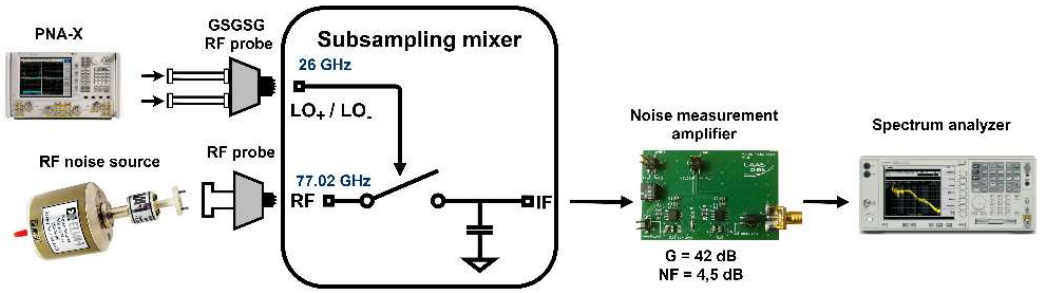

Figure 3-28: Sub-sampling mixer test setup for noise measurement.

WR-12 waveguide components are still used at 77 GHz on the RF access but the 26 GHz differential LO signal is provided by a 4-port 67 GHz PNA-X. This vector network analyzer includes two internal sources with relative phase and magnitude control capabilities used to directly apply a differential LO signal to the sub-sampling mixer test chip.

3.8 Measurement results of the 77 GHz sub-sampling mixers

3.8.1 Conversion gain and linearity

3.8.1.1 Sub-sampling mixer version 1

The voltage conversion gain of the first version is reported in Figure 3-29 for an RF frequency between 76 and 81 GHz and compared with simulated data. The RF and LO frequencies are swept from 76 GHz to 81 GHz and 25.33 GHz to 27 GHz respectively with a constant IF frequency of 20 MHz. The measurements are performed at a 0 dBm LO input power and plotted data include the contribution of the RF balun. Under these conditions, the inverter chains consume 32 mW at a 1.2 V supply.

As explained previously, the delay defined between chains of LO inverters, and therefore the duty cycle with which the mixer operates, can be adjusted. The data displayed comes from the setting which maximizes the conversion gain at 78GHz. Changing this setting to get the best performance for each frequency would have taken too much time.

The measured G_{cv} varies between 3.7 dB and 6.8 dB in the f_{RF} range 76-81 GHz showing a good agreement with simulations. The variations observed on G_{cv} are mainly due to a fluctuating voltage transformation ratio in the input balun.

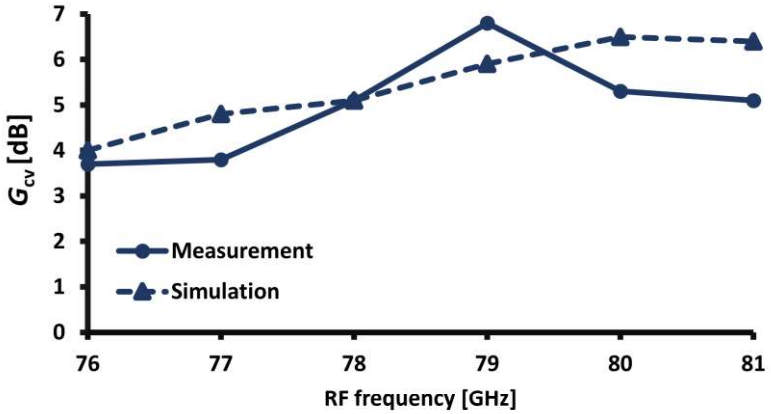

Figure 3-29: G_{cv} vs f_{RF} of the sub-sampling mixer version 1.

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 3-30. RF and LO frequencies are respectively set to 78.02 GHz and 26 GHz. The extracted G_{cv} and ICP1dB are respectively 5.1 dB and -5.3 dBm. The sub-sampling mixer core performances are extracted by de-embedding the input RF balun from measurements. In these conditions, the G_{cv} becomes equal to -3 dB with an ICP1dB of + 2.8 dBm.

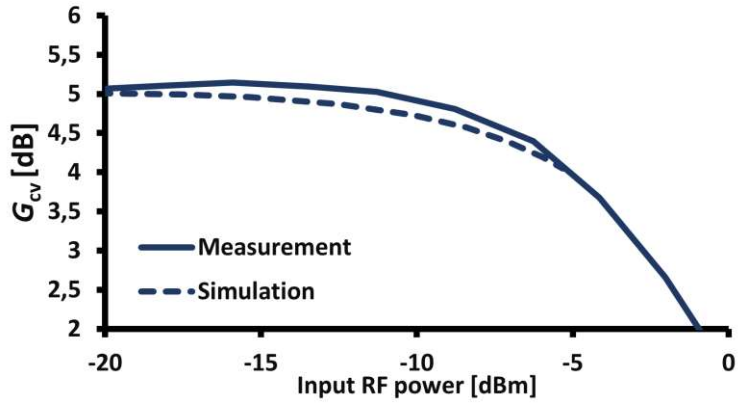

Figure 3-30: G_{cv} vs the input RF power at 78 GHz (sub-sampling mixer version 1).

3.8.1.2 Sub-sampling mixer version 2

The measurements of the second version of the sub-sampling mixer were performed using the same approach as for the first version. The results are reported in Figure 3-31. The G_{cv} is measured between 2.7 dB and 3.5 dB a in the f_{RF} range 76-81 GHz and shows a good agreement with simulations.

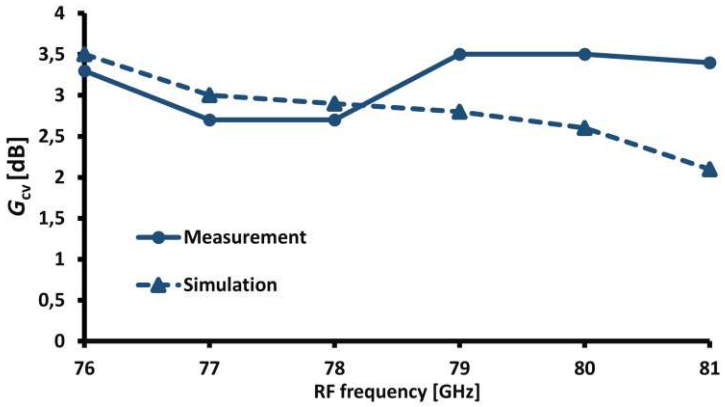

Figure 3-31: G_{cv} vs f_{RF} (sub-sampling mixer version 2).

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 3-32. RF and LO frequencies are respectively set to 78.02 GHz and 26 GHz. The extracted G_{cv} and ICP1dB are respectively 2.7 dB and -1.5 dBm. The mixer core performances are extracted by de-embedding the input RF balun from measurements. In these conditions, the G_{cv} becomes equal to -2.1 dB with an ICP1dB of + 3.3 dBm.

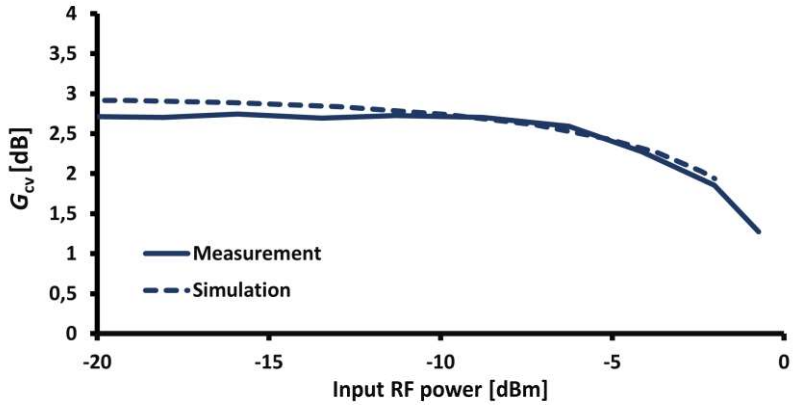

Figure 3-32 G_{cv} vs the input RF power at 78 GHz (sub-sampling mixer version 2).

3.8.2 Noise figure

3.8.2.1 Sub-sampling mixer version 1

As for the sampling mixer presented in chapter 2, the NF_{SSB} is measured using the cold source method. In both sub-sampling mixers exhibit a higher $1/f$ noise than expected. To remove the contribution of the $1/f$ noise to the NF_{SSB}, the measurements have been carried out in the range 76-81 GHz with an IF frequency of 30 MHz rather than 20 MHz as in the chapter 2.

The results are reported in Figure 3-33. These measurements include the noise contribution of the input balun and the IF output stage. The NF_{SSB} is measured between 17.9 dB and 23 dB a in the f_{RF} range 76-81 GHz. and appears always higher than the simulated values.

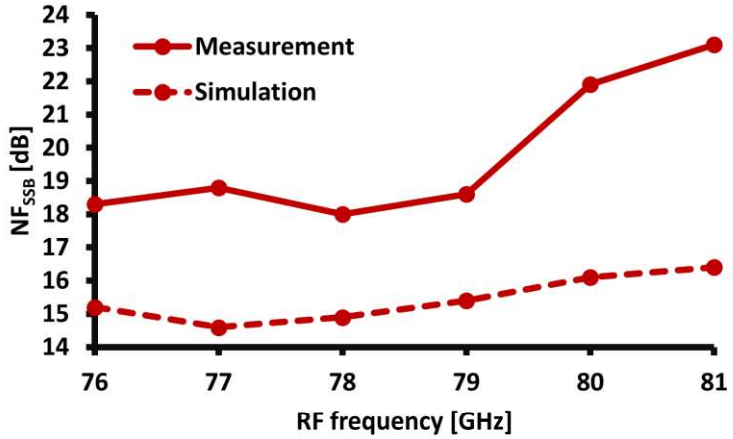

Figure 3-33: NF_{SSB} vs f_{RF} (sub-sampling mixer version 1).

Finally, Figure 3-34 shows the NF_{SSB} with a LO frequency of 26 GHz and an IF frequency range up to 30 MHz. The measured values of NF_{SSB} are far higher than the simulated values at low frequencies highlighting an important 1/*f* noise. The discrepancies between the measured and simulated NF values will be discussed in a dedicated section at the end of this chapter.

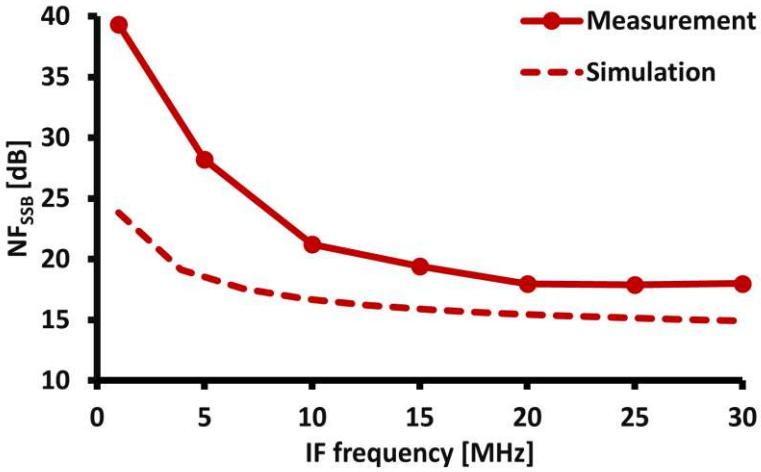

Figure 3-34: NF_{SSB} at a f_{RF} of 78 GHz (sub-sampling mixer version 1).

The measured value of NF_{SSB} at an IF frequency of 30 MHz is 17.9 dB. When the noise contribution of the output stage is removed from this measurement, the NF_{SSB} of the mixer considering input balun losses becomes equal to 16.9 dB.

3.8.2.2 Sub-sampling mixer version 2

The measurements of the NF_{SSB} of the second sub-sampling mixer version versus the RF frequency are reported in Figure 3-35. The NF_{SSB} is measured between 18.1 dB and 18.8 dB a in the f_{RF} range 76-81 GHz in good agreement with simulations.

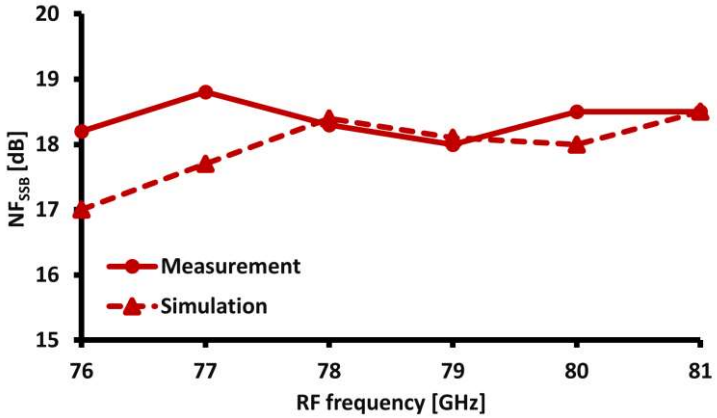

Figure 3-35: NF_{SSB} vs f_{RF} (sub-sampling mixer version 2).

Finally, Figure 3-36 shows the NF_{SSB} with a LO frequency of 26 GHz and an IF frequency range up to 30 MHz. The difference between measured and simulated values in the flicker noise is still present with this version. Nevertheless, the measured values are getting close to the simulated ones starting from 20 MHz. The measured NF_{SSB} value at an IF frequency of 30 MHz is 18.4 dB. After removing the noise contribution of the output stage, the NF_{SSB} of the mixer with the input balun is 16.8 dB.

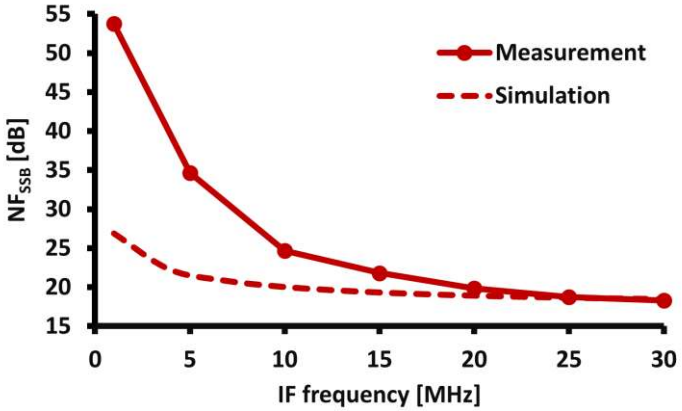

Figure 3-36: NF_{SSB} at a f_{RF} of 78 GHz (sub-sampling mixer version 2).

3.8.3 Performance summary and conclusion

The Table 3-2 sums up the measured performances for both versions of the sub-sampling mixers.

Table 3-2: Measured performances of the sub-sampling mixers.

Version	f_{RF}/f_{LO} **[GHz]**	G_c **[dB]**	**ICP1dB [dBm]**	NF_{SSB} **[dB]**	P_{dc} **[mW]**
1	78/26	-3	+2.8	16.9	32 + 23*
2	78/26	-2.1	+3.3	16.8	32 + 23*

* IF output follower consumption

These measurements demonstrate the interest of the sub-sampling mixer topology to efficiently convert a millimeter-wave RF signal while involving a LO frequency approximately three times lower than the RF one. Both versions show very low conversion losses for passive mixers and a high linearity. The obtained NF_{SSB} are higher than in the sampling mixer presented in the chapter 2 ($f_{RF} \approx f_{LO}$) due to the noise aliasing effects present around the LO harmonics where a frequency conversion path exists. This noise aliasing effect remains the main drawback of sub-sampling and conventional sub-harmonic mixers.

The second version embedding the AND function inside the mixer core to remove the external AND gates show the best performances as the lower achievable duty cycles allow better conversion gains with a similar linearity.

As standalone sub-harmonic mixers are not widespread in the literature related to CMOS 77 GHz radar receivers, a meaningful comparison between this sub-sampling mixer and other solutions is difficult. However, both versions of this mixer topology were also co-integrated with a LNA to build front-ends that will be presented in chapter 4. The full radar front-end performances will help to provide a proper comparison with others 77 GHz radar receivers.

3.8.4 Discrepancies between simulated and measured NF for sub-sampling mixers

The NF measurements of both versions of the sub-sampling mixer in the previous sections show some differences with simulated values. Two distinct kinds of discrepancies can be noticed.

3.8.4.1 Differences between measured and simulated NF at low IF frequencies

The first discrepancy is common to both versions of the mixer and is related to low frequency noise. In Figure 3-34 and Figure 3-36 showing the mixer NF_{SSB} at a fixed f_{LO} of 26 GHz and a f_{IF} range up to 30 MHz, the measured NF is far higher than the simulated values at low frequencies highlighting an extra $1/f$ noise.

As this issue is common to both sub-sampling mixers and did not occur with the sampling mixer in chapter 2, the differences between de measured and simulated values can be explained by a high phase noise of the LO signal introduced by the logic gates. When converted by the mixer, this LO signal phase noise will result in a high low frequency noise. In [54], the influence of various noise sources on a CMOS inverter is discussed showing that the noise coming from the inverter input, voltage supply and ground access is significantly amplified resulting in an important output jitter. As at least five inverters are included in each inverter chain of the proposed LO signal shaper, the amplification of the noise coming from the LO source, voltage supply and ground can explain the high low frequency noise reported in Figure 3-34 and Figure 3-36. The simulation results compared with measurements do not consider the noise of the LO input source and potential noise coming from the DC power supply or the ground access of the 26 GHz LO signal shaper. Therefore, the simulated low frequency noise could have been underestimated.

3.8.4.2 Differences between measured and simulated NF at 30 MHz

The second main difference with simulation is only related to the version 1 of the sub-sampling mixer. In Figure 3-33 the measured values of the NF_{SSB} for a f_{IF} of 30 MHz and

different f_{LO} are higher than the simulated values in the 76-81 GHz f_{RF} frequency range. This difference is not correlated with the low frequency noise discrepancy discussed earlier as the IF frequency of 30 MHz is high enough to avoid the influence of the low frequency noise.

As previously stated, the duty cycle tunning setting was performed to maximize the conversion gain at f_{RF} of 78 GHz. The measured conversion gain of the version 1 of the sub-sampling mixer reported in Figure 3-29 shows a good agreement with simulation. Nevertheless, the LO pulsed signal generated in the version 1 of the mixer cannot be monitored when measuring the circuit, the good agreement between the measured and simulated conversion gain only ensures that the LO duty cycle is close to the expected value.

The LO pulse shaper simulated output waveforms for different duty cycle tunning setting (Figure 3-9) highlights that the AND gates frequency limitation leads to a decrease of the LO swing for duty cycle lower than 20%. A LO pulsed signal with a similar duty cycle than the simulated waveform and a lower voltage swing would results in a higher mixing transistor r_{on} resistance of the mixing transistors with the same measured and simulated conversion gain. As the load impedance of the mixer is far higher than the mixing transistors r_{on} an increase of the r_{on} will not significantly degrades the conversion gain. As a result, a lower LO voltage swing at the AND gates output resulting in a higher r_{on} value would increase the NF_{SSB} of the mixer without a significant difference between the measured and simulated conversion gain explaining the differences between measured and simulated values.

In the version 2 of the mixer, removing the AND gates avoid the decrease of the LO signal swing for the low duty cycle. This characteristic can explain why these discrepancies between measured and simulated NF_{SSB} values at a f_{IF} of 30 MHz only occur for the version 1 of the sub-sampling mixer.

Chapter 4 Sampling-based 77 GHz radar receivers in 28-nm FD-SOI CMOS technology

4.1 Design of a 77 GHz automotive radar receiver

4.1.1 Introduction

Two mixer topologies based on the sampling principle were introduced in the previous chapters. The chapter 2 demonstrates that sampling generally used in RF architectures can be extended to millimeter-wave frequencies to design passive mixers benefiting from a high linearity associated to very low conversion losses. Then, the chapter 3 demonstrates that using careful design, especially for the LO circuitry to convert a 77 GHz RF signal by using a 26 GHz LO frequency, simplifies the LO distribution chain.

To assess the benefits of both sampling-based solutions in a 77 GHz automotive radar receiver, the proposed mixers have been implemented together with a LNA in a 77 GHz receiver front-ends. On top of that, CMOS 77 GHz radar receivers are widely present in the literature allowing to compare this implementation with other solutions.

In this chapter, the selection of a LNA suitable for the front-ends and its implementation with the mixers are detailed. Then measurement results of the different receivers are described. Finally, the proposed architectures will be compared with the state of the arts of 77 GHz radar receivers highlighting their strengths and weaknesses.

4.1.2 Noise and linearity of a RF receiver

To get the best overall receiver performance from the proposed mixers, the LNA must be sized properly. As discussed in chapter 1, the choice of the LNA gain is essential get a good noise/linearity trade-off. To choose the right LNA gain the overall receiver NF and ICP1dB must be calculated from the specifications of the different receiver stages. The following

section deals with the receiver ICP1dB and NF calculation and the choice of the LNA implemented in the 77 GHz receiver front-ends.

4.1.2.1 Overall receiver NF calculation

The Friis formula [55] allows to express the NF of a receiver as a function of the gain and NF of the different stages. The conventional version of the Friis formula is:

$$NF_{RX} = NF_1 + \frac{NF_2 - 1}{G_{P1}} + \cdots + \frac{NF_n - 1}{G_{P1} \times G_{P2} \times \ldots \times G_{Pn}} \quad (4\text{-}1)$$

This equation considers n 50 Ω matched stages where NF_n and G_{Pn} are the NF and the power gain of the n^{th} stage. As the proposed sampling mixers does not have a 50 Ω input impedance, a version of the FRIIS formula using the voltage gain, the input and output impedance and the noise voltage spectral density is preferred. Furthermore, as the 2nd receiver stage is a mixer, the noise conversion around each LO harmonics and in the image bands must be considered. The Friis formula considering n stages without assuming a 50 Ω matching between the stages is given in [33]. Using this formula while taking into account the multiple noise conversions in the sampling mixer leads to the NF_{SSB} described in Figure 4-1.

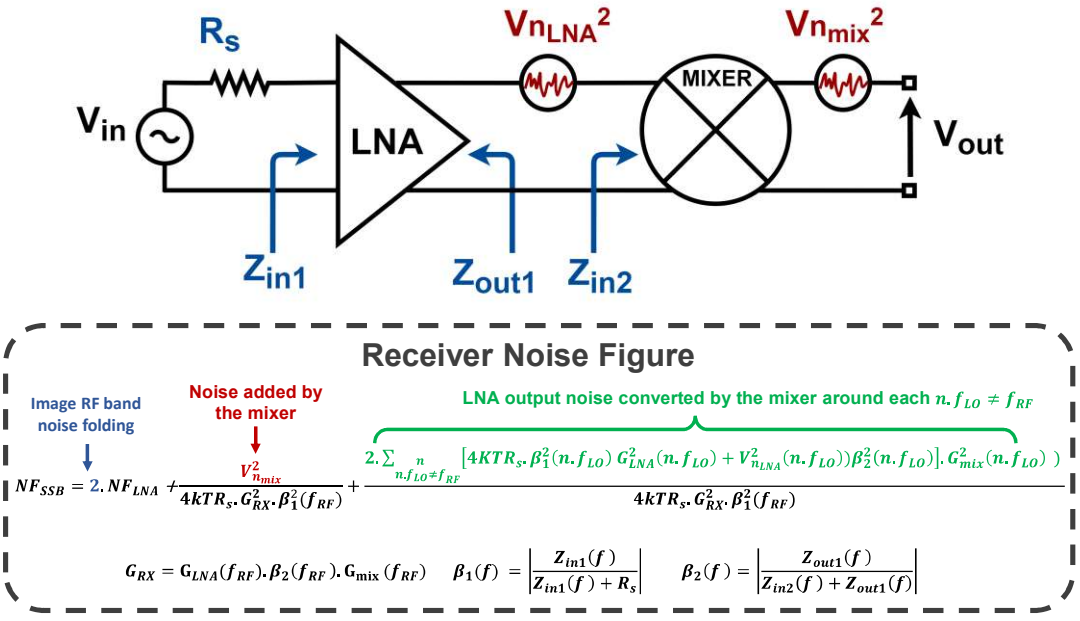

Figure 4-1: NF_{SSB} of the receiver.

The NF_{SSB} expressed in Figure 4-1 considers the resistive noise added by the mixer and every noise conversion around the LO harmonics. As the LNA implemented in the 77 GHz receivers is narrow band, the LNA output noise around other LO harmonics than 77 GHz is filtered. As a result, the LNA output noise converted by the mixer around each $n.f_{LO} \neq f_{RF}$ is negligible compared to the noise in the RF frequency band. In addition, as the receiver input is matched to 50 Ω and as the mixers tend to present a quite high input impedance at f_{RF}, $\beta_1(f_{RF}) \approx 0.5$ and $\beta_2(f_{RF}) \approx 1$. Hence, the formula in Figure 4-1 can be simplified as follow:

$$NF_{SSB} = 2.NF_{LNA} + \frac{V_{n_{mix}}^2}{\frac{1}{4}.4kTR_s.G_{LNA}^2.G_{mix}^2} \tag{4-2}$$

This equation will be used to choose the right LNA gain to satisfy the noise/linearity trade-off on the receiver considering the LNA NF and performances of the mixers.

4.1.2.2 Overall receiver ICP1dB calculation

The output and input 1-dB compression points of the receiver can be calculated from the LNA and mixer compression points and gains with a similar approach as for the NF. In [56], an equation close to the FRIIS formula is used to calculate the receiver OCP1dB:

$$\frac{1}{OCP1dB} = \frac{1}{OCP1dB_{mix}} + \frac{1}{OCP1d_{LNA}.G_{p_{mix}}} \tag{4-3}$$

In this formula, the OCP1dB are power value expressed in watts. When powers are expressed in dBm and gains in dB the ICP1dB can easily be obtained with the relation:

$$OCP1dB = ICP1dB + (G_{LNA} + G_{mix} - 1) \tag{4-4}$$

These relations will be used with the FRIIS formula for NF to choose LNA gain knowing the LNA OCP1dB and the mixers performances.

4.1.3 Description of the 77 GHz LNA

For time constraints, and because it was not the focus of this PhD work, it has been decided to use an existing LNA. Obviously having a specific LNA designed to match the sampling

mixers performances would allow to have a better noise/linearity trade-off. Using an already existing and measured LNA was also a way to secure the overall front-end performances.

The LNA presented in [57] was designed by STMicroelectronics with the 28-nm FD-SOI technology and exhibits at the same time low noise and high linearity. So, a version of this LNA with minor modifications was chosen for the receiver implementation.

4.1.3.1 LNA architecture

In the LNA presented in [57] each stages is based on the architecture presented in Figure 4-2. A balanced topology is used to improve the linearity and meet the radar stringent requirements. Transformers are used at the input and output of each stage to provide at the same time a good matching and DC isolation between stages. Gate-source capacitors are combined to degeneration inductors to find the best compromise between matching, noise optimum impedance and stability.

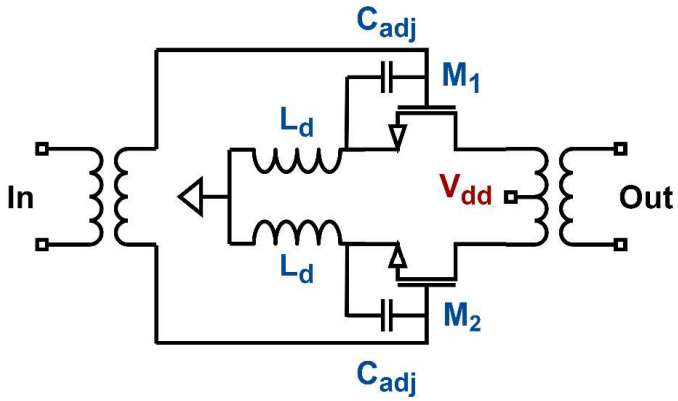

Figure 4-2: LNA stage architecture.

Each stage has around 4-dB of voltage gain when both input and output are 50 Ω matched. As multiple identical stages can be stacked to get the required gain, the Friis formula on NF and ICP1dB will be used to find the right number of stages to implement in the 77 GHz receivers.

4.1.3.2 LNA performances

In [57] 2 stages and 6 stages versions of this LNA are described. The simulation and measurement results are described in the Table 4-1.

Table 4-1: LNA measured and simulated performances in [57].

Number of stages	Gain [dB]	*NF* [dB]	ICP1dB [dBm]	BW [GHz]	P_{dc} [mw]
2	7.3*/6.5	5.1*/4.6	-2.4*/-3	20*/17	8.7*/8.7
6	23.1*/21.5	5.7*/5.5	-22*/-18.8	6.5*/6.5	25*/25

* Simulated performances

4.1.3.3 Layout of a LNA stage

The Figure 4-3 shows the layout of one stage of the LNA. The different elements of the schematic in Figure 4-2 are clearly visible in the layout. The thickest metal levels (Alucap, IA, IB) are used to design the transformers. Multiple similar stages can be stacked by using the output transformer for the interstage. The area of a LNA stage is approximatively 210µm ×125µm.

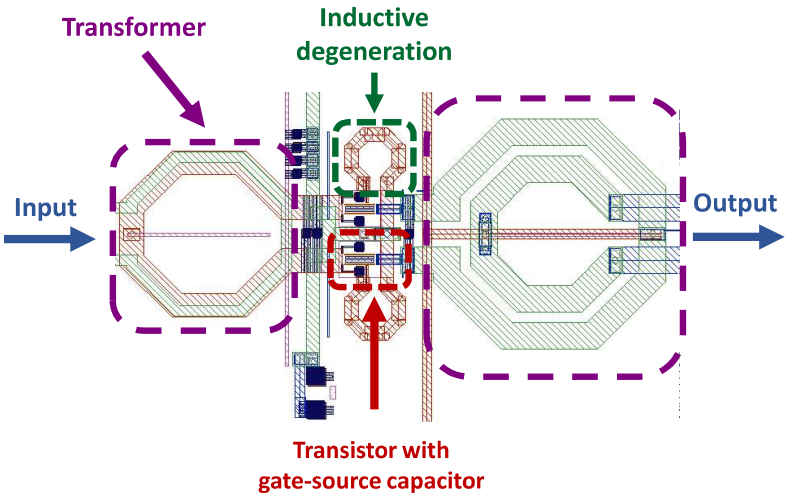

Figure 4-3: Layout of one stage of the LNA.

4.1.4 Choice of the number of LNA stages

The formulas on NF and ICP1dB presented earlier will be used in this section to calculate the receiver noise and linearity performances for different LNA gains. This approach allows to quickly assess the performances of the receivers knowing the LNA performances and the

simulated performances of the three different mixers. As simplifications are made to keep this calculation simple, these results will only be used to get approximative value of the receiver ICP1dB and NF to find the optimal number of LNA stages. The receiver front-ends will then be implemented and simulated for more accurate results.

There is no voltage drop at LNA output because the mixer Z_{in} is far higher than the 50 Ω Z_{out} of the LNA. Therefore, the LNA voltage gain is 6 dB higher than with a 50 Ω load. Considering that each LNA stage has 4 dB of voltage gain, the LNA voltage gain in this configuration will be:

$$G_{v_{LNA}} = number\ of\ stages\ \times 4\ dB + 6\ dB \tag{4-5}$$

The approximate values of the receiver performances calculated from the simulated values of the mixers for different number of LNA stages are plotted in Figure 4-4.

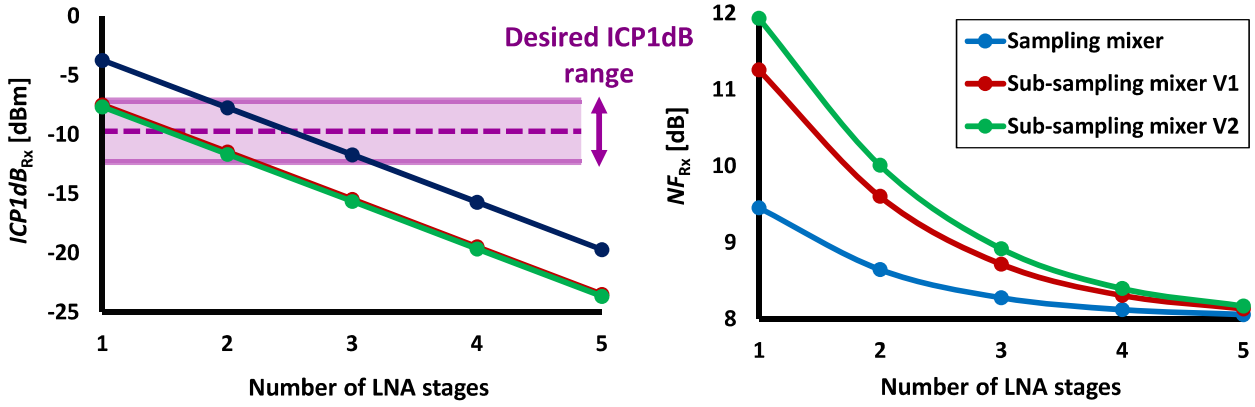

Figure 4-4: Choice of the LNA number of stages based on the Friis formula.

As the automotive radar application requires a highly linear front-end, the chosen ICP1dB target on the receiver is around -10 dBm. The NF should be kept as low as possible while satisfying the linearity constraint. Relying on the performance estimation of the receivers in Figure 4-4, using a 2-stages LNA with a 14 dB gain seems to be the best compromise. It enables to get a good noise/linearity trade-off with the three designed mixers with the same LNA. The performances estimated with this approach are summed up in Table 4-2.

Table 4-2: Receivers estimated performances.

Mixer implemented with the LNA	Gain [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	DC Power [mW]
Sampling mixer	13	-7.7	8.6	19
Sub-sampling mixer V1	10.5	-11.6	9.6	45
Sub-sampling mixer V2	11.5	-11.6	10	45

4.2 77 GHz receiver based on a sampling mixer

4.2.1 Receiver architecture

The architecture of the test chip including the low noise amplifier presented earlier and the 77 GHz sampling mixer described in chapter 2 is depicted in Figure 4-5.a. A picture of the manufactured chip is given in Figure 4-5.b.

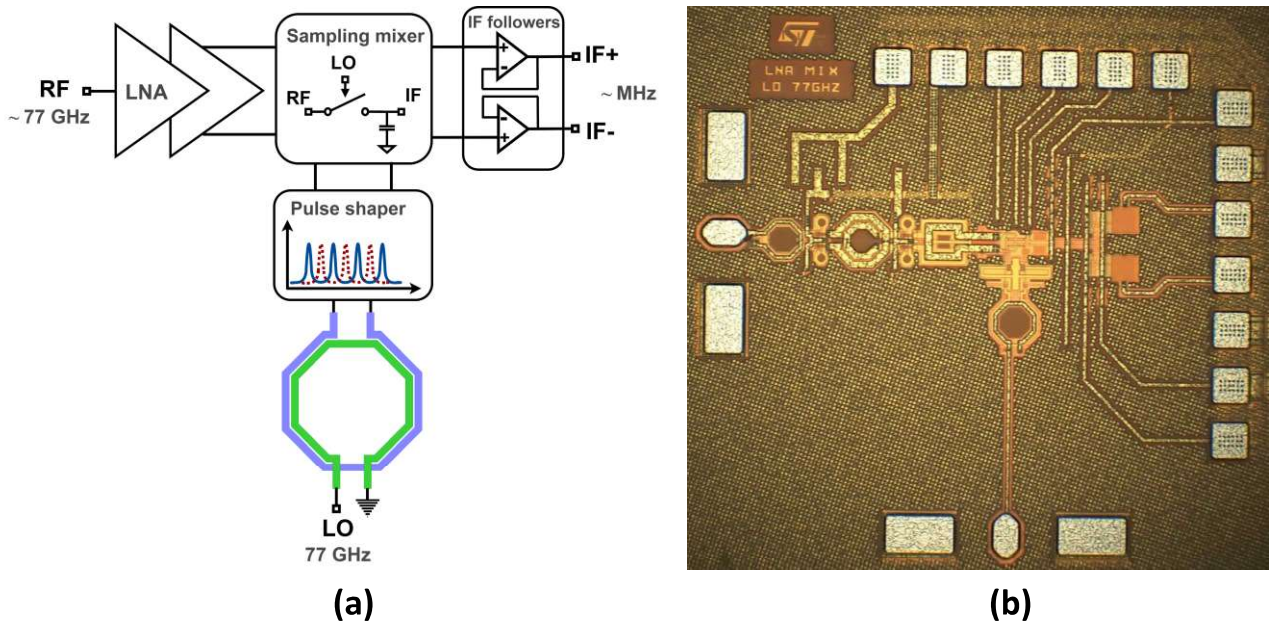

Figure 4-5: (a) Receiver block diagram (b) manufactured chip.

In this receiver the input balun of the LNA converts the single-ended RF input signal into a differential signal. As in the previous design the RF GSG pad capacitance is used for the

matching of the RF access to avoid pad de-embedding. The Figure 4-6 is a focus on the receiver layout highlighting the different receiver blocks.

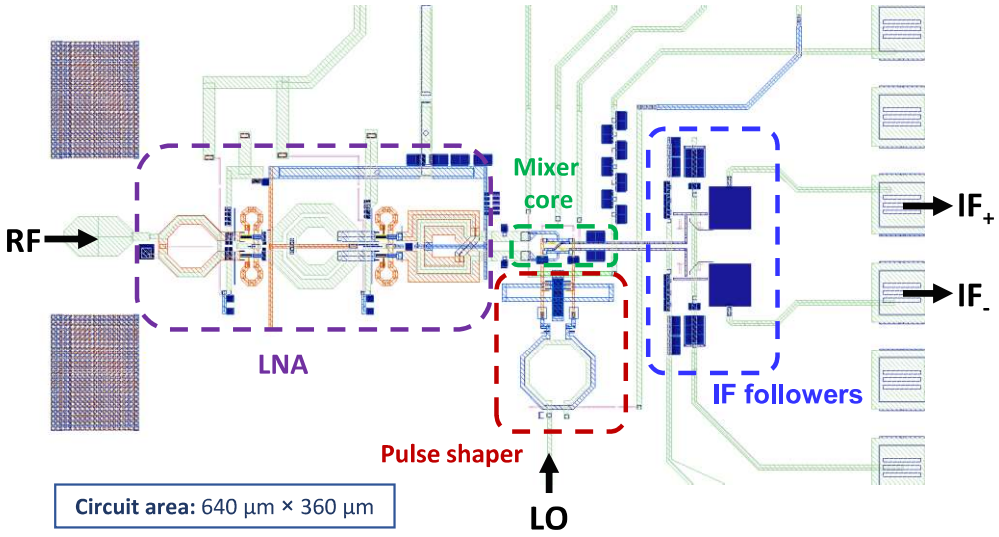

Figure 4-6: Focus on the receiver layout.

4.2.2 Receiver measurement results

4.2.2.1 Conversion gain and linearity

The simulated gain repartition in the receiver with the RF and LO frequencies respectively set to 77.02 GHz and 77 GHz is reported in the following table:

Table 4-3: Simulated gain repartition in the receiver.

Receiver gain [dB]	Input matching gain [dB]	LNA gain [dB]	Mixer gain [dB]
11.5	-0.9	13.9	-1.5

The LNA gain is close to the expected value and the mixer conversion gain is quite similar as in chapter 1. As the output stage relies on two OP-amp followers with a 0 dB gain. Thus, this stage is not considered in the gain repartition of the receiver. The input of the LNA presents a resistive input impedance around 40 Ω. Therefore, the input 50 Ω RF source delivers less voltage than expected at the input of the LNA leading to the following matching network gain:

$$G_M = 2.\frac{Z_{in_{LNA}}}{50+Z_{in_{LNA}}} \approx -1\ dB \qquad (4\text{-}6)$$

In the (4-6) the factor 2 is explained by the fact that 50 Ω voltage sources use a $2V_{in}$ input voltage swing to actually deliver a V_{in} voltage swing at the input of the LNA because of the voltage drop due to the 50 Ω source impedance.

Measurements of the RF voltage conversion gain G_{cv} of the receiver based on the sampling mixer presented in the chapter 2 in the f_{RF} range 76-81 GHz are reported in Figure 4-7. The receiver was measured under the same conditions as the sampling mixer in chapter 2. The LNA consumes 10 mW on a 1V supply. The G_{cv} is measured between 9.5 dB and 11.5 dB in the f_{RF} range 76-81 GHz.

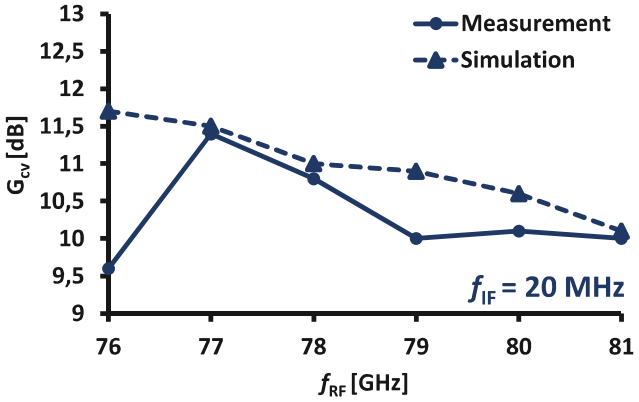

Figure 4-7: G_{cv} vs f_{RF}

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 4-8. RF and LO frequencies are respectively set to 77.02 GHz and 77 GHz. The extracted G_{c_v} and ICP1dB are respectively 11.4 dB and -7.4 dBm. Figure 4-8 shows a good agreement between the measured and simulated conversion gain at 77 GHz.

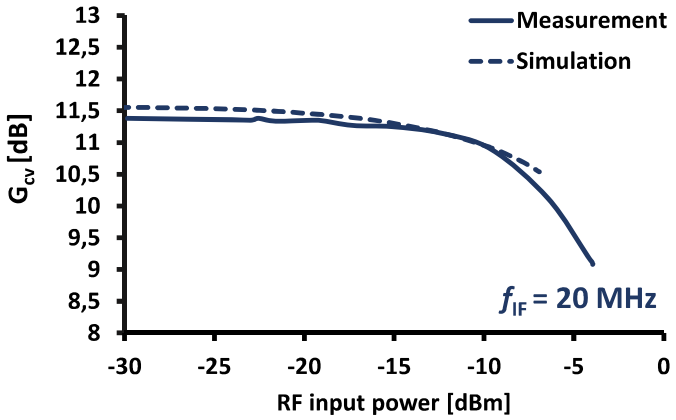

Figure 4-8: G_{cv} vs the input RF power at 77 GHz.

4.2.2.2 Noise Figure

Measurements of the NF_{SSB} of the receiver in the f_{RF} range 76-81 GHz are reported in Figure 4-9. The NF_{SSB} is measured between 10.3 dB and 12.2 dB in the f_{RF} range 76-81 GHz.

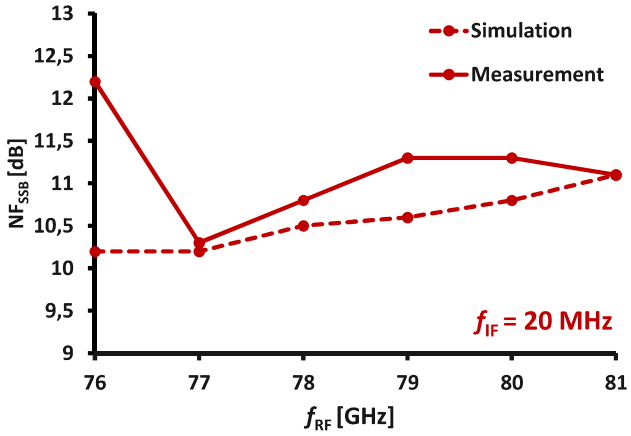

Figure 4-9: NF_{SSB} versus f_{RF}

Finally, Figure 4-10 shows the NF_{SSB} with a LO frequency of 77 GHz and an IF frequency range up to 30 MHz. The measured value at 20 MHz of NF_{SSB} is 10.3 dB in good agreement with simulation. When the noise contribution of the output stage (IF followers) is removed from this measurement, the NF_{SSB} of the receiver is 8.9 dB.

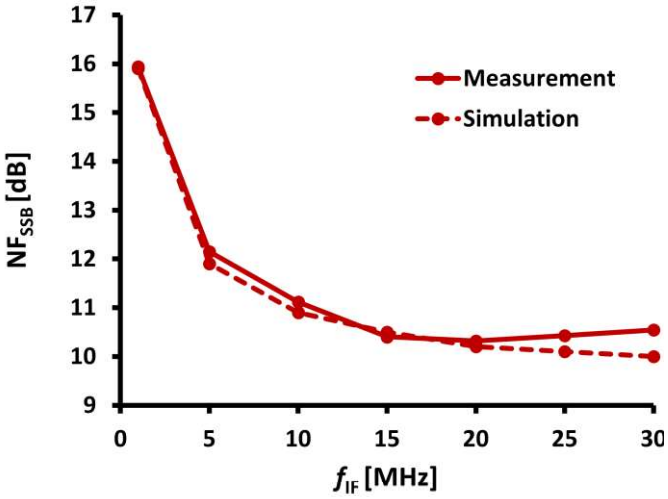

Figure 4-10: NF_{SSB} at $f_{RF} = 77\ GHz$

4.2.2.3 Performance summary and conclusion

The Table 4-4 sums up the measured performances of the receiver based on the sampling mixer (chapter 2). In the following sections, this receiver will be called receiver 1.

Table 4-4: Receiver measured performance.

f_{LO} [GHz]	f_{IF} [MHz]	G_{Rx} [dB]	ICP1dB [dBm]	NF [dB]	P_{dc} [mW]
77	20	11.4	-7.4	8.9	10 (LNA) + 10 (LO shaping)

The implementation of the sampling mixer with a LNA in a 77 GHz front-end results into a good trade-off between noise and linearity associated to a low power consumption. A detailed comparison between this solution and other radar receivers will be provided later in this chapter.

4.3 77 GHz receivers based on sub-sampling mixers

4.3.1 Receiver architecture

The architecture of the test chip including the low noise amplifier with the 77 GHz sub-sampling mixers described in chapter 3 is depicted in Figure 4-11.a. A picture of the manufactured chip is given in Figure 4-11.b.

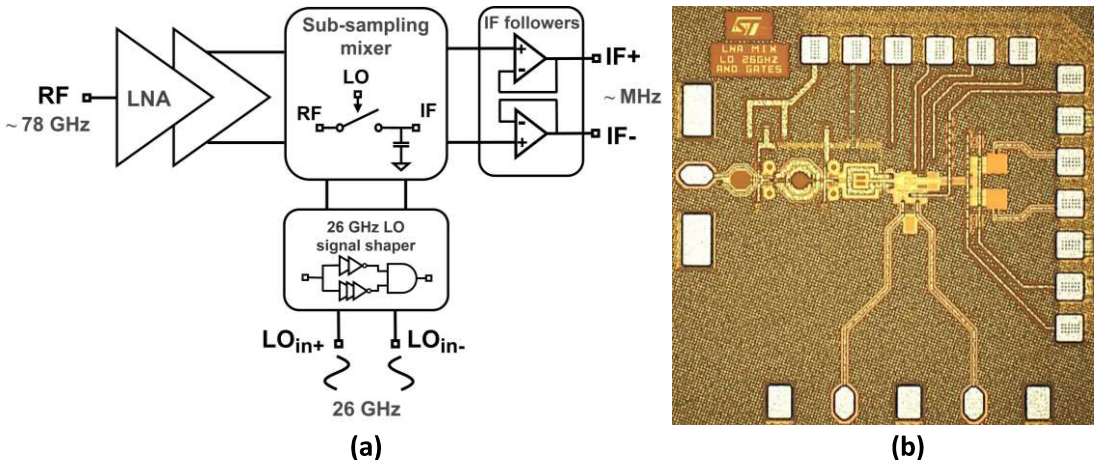

Figure 4-11: (a) Receiver block diagram (b) manufactured chip.

The RF access matching is the same as in the previous receiver and the 26 GHz differential LO signal is directly applied to the GSGSG pads with RF probes. The Figure 4-12 is a focus on the receiver layout highlighting the different receiver blocks. It can be noticed that the logic gate LO shaper is more compact than the 77 GHz LO shaper in the previous receiver.

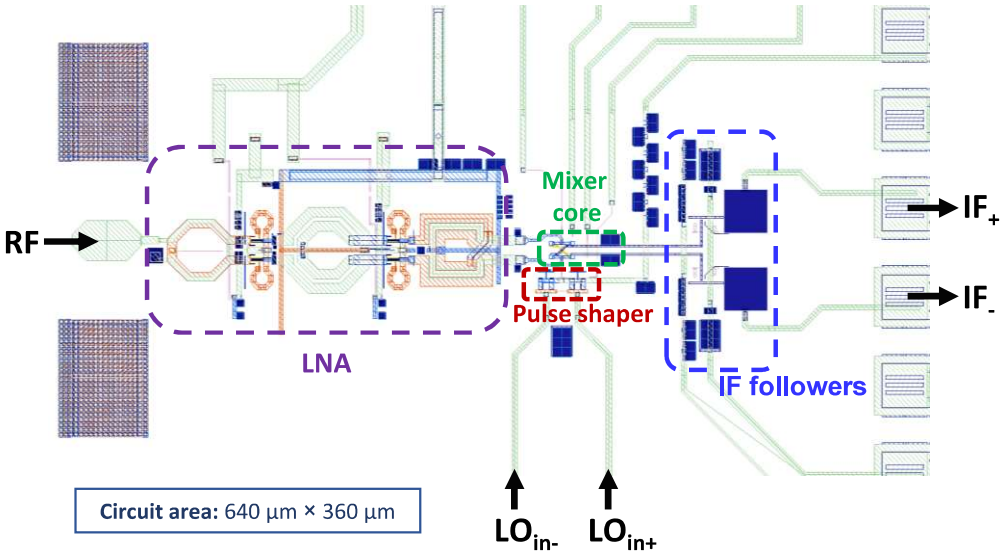

Figure 4-12: Focus on the receiver layout.

4.3.2 Measurement results of the receivers

4.3.2.1 Conversion gain and linearity

4.3.2.1.1 Receiver based on the sub-sampling mixer with AND gates

The simulated gain repartition in the receiver based on the sub-sampling mixer using AND gates for the LO signal shaping (version 1 in chapter 3) with the RF and LO frequencies respectively set to 77.02 GHz and 25.66 GHz is reported in the following table:

Table 4-5: Simulated gain repartition in the receiver.

Receiver gain [dB]	Input matching gain [dB]	LNA gain [dB]	Mixer gain [dB]
8.7	-0.8	13.5	-4

Measurements of the G_{cv} of this receiver are reported in Figure 4-13. The receiver was measured under the same conditions as the sub-sampling mixer in chapter 3. The G_{cv} is measured between 6 dB and 9.4 dB a in the f_{RF} range 76-81 GHz. As previously stated in the chapter 3, the duty cycle setting was performed for a RF frequency of 78 GHz and kept unchanged for the other RF frequencies.

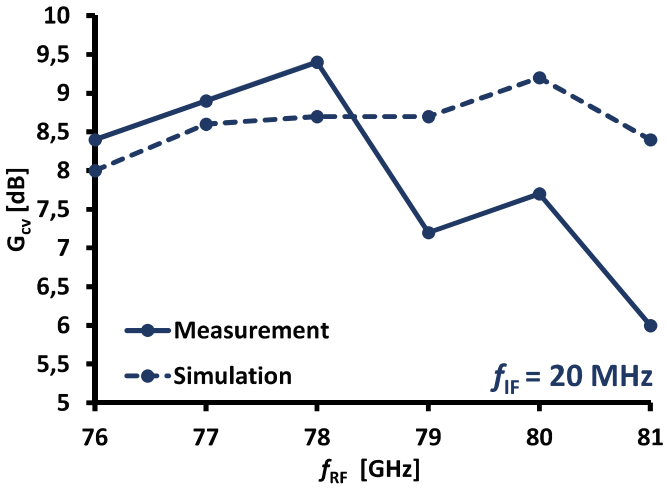

Figure 4-13: G_{cv} vs f_{RF}.

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 4-14. RF and LO frequencies are respectively set to 77.02 GHz and 25.66 GHz. The extracted G_{cv} and ICP1dB are respectively 8.9 dB and -11 dBm.

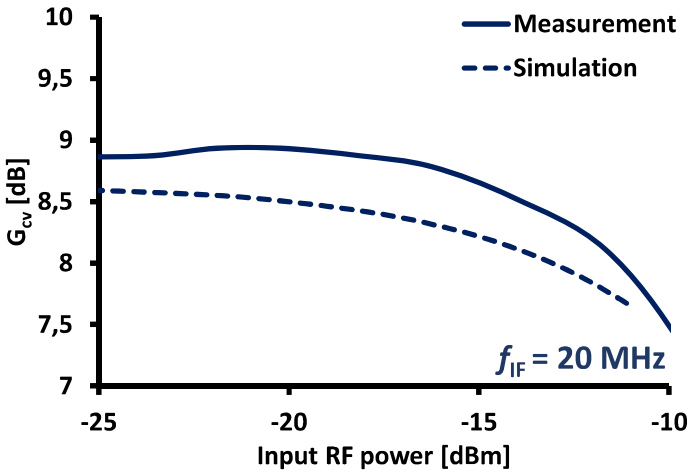

Figure 4-14: G_{cv} vs the input RF power at 77 GHz.

4.3.2.1.2 Receiver based on the sub-sampling mixer with co-integrated AND gates

The simulated gain repartition in the receiver based on the sub-sampling mixer co-integrating the AND gates to the mixer core (version 2 in chapter 3) with the RF and LO frequencies respectively set to 77.02 GHz and 25.66 GHz is reported in the following table:

Table 4-6: Simulated gain repartition in the receiver.

Receiver gain [dB]	Input matching gain [dB]	LNA gain [dB]	Mixer gain [dB]
9.7	-0.6	13.3	-3

Measurements of the G_{cv} of this receiver are reported in Figure 4-15. The G_{cv} is measured between 7.9 dB and 9.5 dB in the f_{RF} range 76-81 GHz.

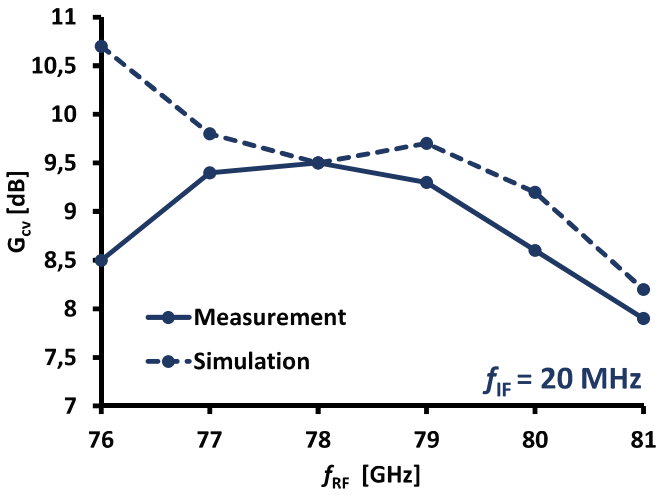

Figure 4-15: G_{cv} vs f_{RF}.

The voltage conversion gain compression obtained from a varying RF input power is plotted in Figure 4-16. RF and LO frequencies are respectively set to 77.02 GHz and 25.66 GHz.

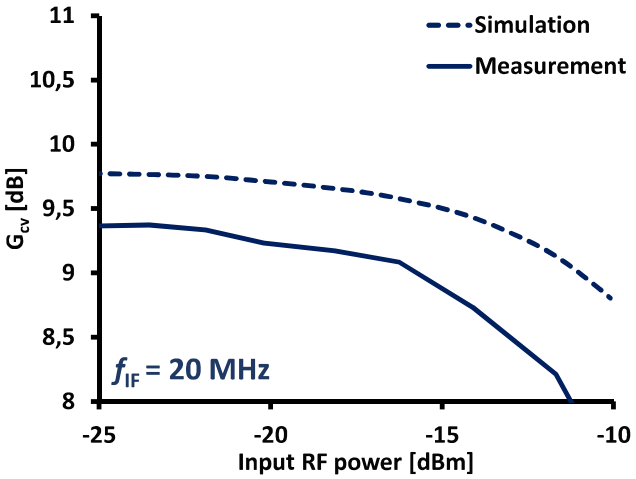

Figure 4-16: G_{cv} vs the input RF power at 77 GHz.

4.3.2.2 Noise Figure

4.3.2.2.1 Receiver based on the sub-sampling mixer with AND gates

Measurements of the NF_{SSB} of the receiver based on the sub-sampling mixer using AND gates for the LO signal shaping in the f_{RF} range 76-81 GHz are reported in Figure 4-17. The NF_{SSB} is measured between 12.6 dB and 13.1 dB below 78 GHz and increases up to 23 dB for a f_{RF} of 81 GHz. This discrepancy has already been noticed and discussed for this mixer in a standalone configuration in the chapter 3.

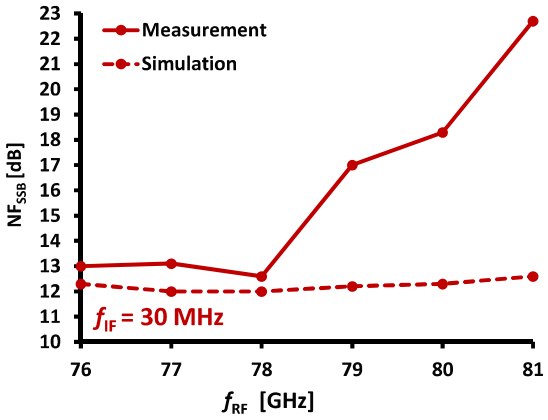

Figure 4-17 : NF_{SSB} versus f_{RF}.

Finally, Figure 4-18 shows the NFSSB with LO frequency of 25.66 GHz and an IF frequency range up to 30 MHz. The measured value of NFSSB at a fIF of 30 MHz is 13.2 dB.

When the noise contribution of the output stage is removed from this measurement, the NF_{SSB} of the receiver is 11.9 dB.

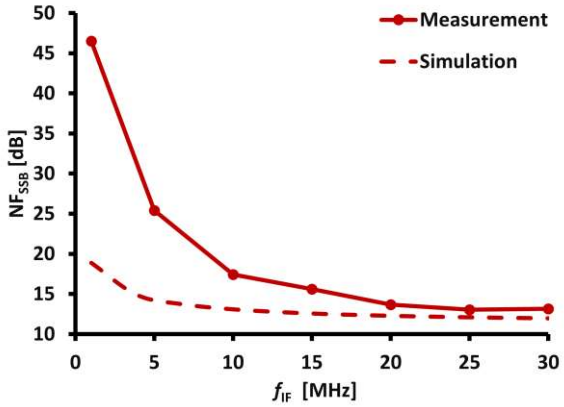

Figure 4-18: NF_{SSB} at a f_{RF} of 77 GHz.

4.3.2.2.2 Receiver based on the sub-sampling mixer with co-integrated AND gates

Measurements of the NF_{SSB} of the receiver based on the sub-sampling mixer co-integrating the AND gates to the mixer core in the f_{RF} range 76-81 GHz are reported in Figure 4-19. The NF_{SSB} is measured between 12.6 dB and 15.6 dB in the f_{RF} range 76-81 GHz.

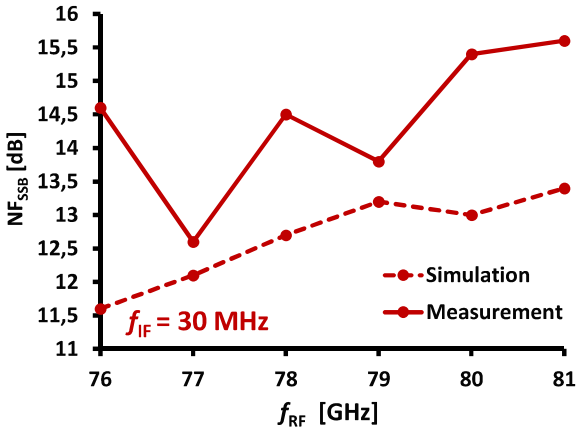

Figure 4-19 NF_{SSB} versus f_{RF}.

Finally, Figure 4-20 shows the NF_{SSB} with a LO frequency of 25.66 GHz and an IF frequency range up to 30 MHz. The measured value of NF_{SSB} at an IF frequency of 30 MHz is 12.6 dB. When the noise contribution of the output stage is removed from this measurement, the NF_{SSB} of the receiver is 11.5 dB.

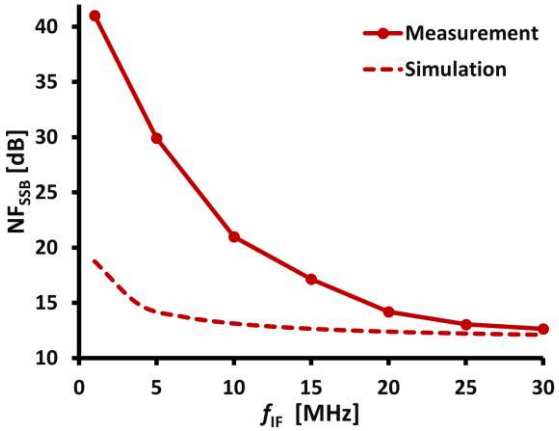

Figure 4-20: NF_{SSB} at a f_{RF} of 78 GHz.

4.3.2.3 Performance summary and conclusion

The Table 4-7 sums up the measured performances of both receivers including the 77 GHz sub-sampling mixers described in chapter 3. The receiver based on the sub-sampling mixer using the AND gates for the LO shaping is referred as receiver 2 while the second version relying on co-integrated AND gates is called receiver 3.

Table 4-7: Receivers measured performance.

	f_{RF} / f_{LO} [GHz]	f_{IF} [MHz]	G_{Rx} [dB]	ICP1dB [dBm]	NF [dB]	P_{dc} [mW]
Receiver 2	78 / 26	30	8.9	-11	11.9	10 (LNA) + 32 (LO shaping)
Receiver 3	78 / 26	30	9.4	-12.1	11.5	10 (LNA) + 32 (LO shaping)

The implementation of both sub-sampling mixers in 77 GHz front-ends demonstrates that sub-sampling principle allows to use a 26 GHz LO frequency to converts a 77 GHz RF signal with a very decent noise/linearity trade-off when compared to the receivers 1 (Table 4-4). As already discussed in the chapter 3, the measurement of the receivers confirms that the co-integration of the AND gates to the mixer core allows to overcome their frequency limitation thus leading to a better front-end gain. A detailed comparison between this solution and other radar receivers will be provided later in this chapter. The opportunity to simplify the radar receiver architecture regarding to the 26 GHz LO frequency will be discussed in this comparison.

4.4 Comparison between the proposed sampling-based receivers and the state of the art

The performances of the sampling-based receivers described in this chapter are summarized and compared with the state of the art of 77 GHz radar receivers in the Table 4-8. The receiver including the sampling mixer presented in chapter 2 is referred as receiver 1 (Rx 1). The receivers based on the version 1 of the sub-sampling mixer (chapter 3) using true AND gates for the LO pulse shaping is called receiver 2 (Rx 2). Finally, the receiver relying on the 2nd version of the sub-sampling mixer co-integrating the AND function to the mixer core is called receiver 3 (Rx 3). This table compares this work with 77 GHz radar receivers based on active, passive and sub-harmonic active mixers covering the existing solutions. As explained in chapter 1, the key performances in a radar front-end are noise and linearity. Therefore, Figure 4-21 highlights the trade-off between ICP1dB and NF_{SSB} for this work and all references in Table 4-8. The specifications on ICP1dB and NF for a radar receiver are discussed in [21], [28]. According to [21], [28], an ICP1dB target around -10 dBm is high enough to cope with multiple signal reflections faced by radar sensors. In [5], the maximum receiver NF to ensure a 250m detection range is estimated as 14 dB. Therefore, the nominal NF values targeted in [21], [28] are around 10 dB. The green, orange and red areas in Figure 4-21 represents these specifications on the noise and linearity of the radar receivers.

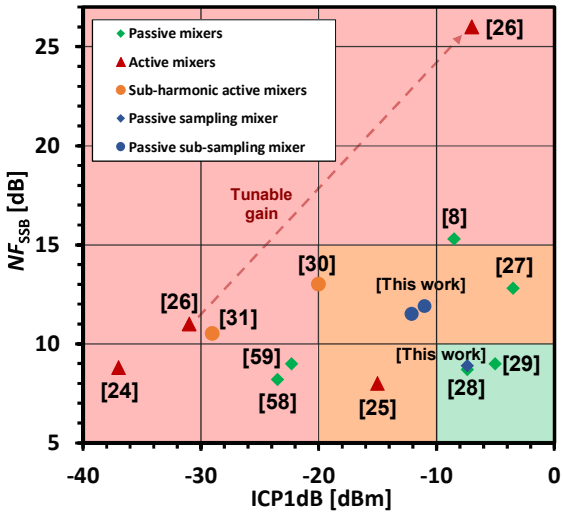

Figure 4-21: Trade-off between ICP1dB and NF_{SSB} in 77 GHz receivers.

Table 4-8: Comparison with the state of the art.

	Ref	CMOS node	f_{RF}/f_{LO} [GHz]	G_{Rx} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	Area [mm²]	V_{DD} [V]	P_{dc} [mW]
Passive sampling mixer (This work)	**Rx 1**	28-nm FD-SOI CMOS	78 / 78	11.4	-7.4	8.9	Rx 0.23	1	20$
Passive sub-sampling mixer (This work)	**Rx 2**		78 / 26	8.9	-11	11.9	Rx 0.23	1 /1.2 (LNA/LO)	42
	Rx 3		78 / 26	9.4	-12.1	11.5	Rx 0.23	1 /1.2 (LNA/LO)	42
Passive mixer	[28]	40-nm CMOS	78 / 78	17	-7.4	8.7	Rx 1.67* LO 0.81*	1.8	NA
	[8]	65-nm CMOS	78 / 78	26.2	-8.5	15.3	Rx 0.15* LO 0.36*	1	Rx 78 LO 49
	[27]	22-nm FD-SOI	78 / 78	16	-3.5	12.8	NA	0.8/1.8 (RF/Baseband)	NA
	[58]	28-nm FD-SOI CMOS	78 / 78	33	-23.5	8.2	0.96	1	Rx 27 LO 11$
	[59]	40-nm CMOS	78 / 78	30.8	-22.3	9	Rx 0.4*	1.1/1.8 (RF/Baseband)	42$
	[29]	28-nm CMOS	78 / 78	15	-5	9	Rx 0.1	1.8	100$
Active mixer	[24]	65-nm CMOS	78 / 78	31.6	-37	8.8	Rx 0.88* LO 0.13*	1	Rx 61 LO 22
	[25]	65-nm CMOS	78 / 78	11	-15	8	Rx 0.23	1	22$
	[26]	65-nm CMOS	78 / 78	18/66	-7/-31	26/11	Rx 0.3* LO 0.4*	1	Rx 31 LO 58
Sub-harmonic active mixer	[31]	65 nm CMOS	78 / 39	14.5	-16.2 (Mixer) -28(Rx)	10.5	0.58	1.5	57
	[30]	65 nm CMOS	78 / 39	16	-20	13	2.33	1.2	28.5
Notes		* Estimated area for 1 Rx and the associated LO path (If the LO path is common for several Tx/Rx the LO area is divided by the number of Tx/Rx) $ additional LO blocks required (multipliers or/and LO drivers) The NF are supposed SSB if not specified in the paper							

The state of the art described in Figure 4-21 and Table 4-8 put forwards that best noise/linearity trade-off are obtained with receivers based on passive mixers. The receivers in [27], [28] and [29] show at the same time a high linearity and low $NF_{SSB.}$ As the receiver linearity strongly depends on the LO voltage amplitude the receiver in [28] and [29] relies on an higher supply voltageto benefit from a high linearity. Another strategy is used in [27] where the single stage LNA results in a low front-end gain ensuring a high linearity on a 0.8 V supply voltage. The low front-end gain is compensated by the IF TIA gain without degrading the linearity by taking advantage of the high baseband voltage supply (1.8V vs 0.8V for RF blocks). This strategy allows to reach the best ICP1dB of this comparison by degrading a little bit the $NF_{SSB.}$ In [29] this concept is pushed further by removing the LNA to implement a passive mixer first receiver where all the gain comes from an IF LNA showing one of the best performances of this comparison. As in [28] and [27] this receiver operates under a 1.8V supply to implement a high linearity IF amplifier and provides a high LO voltage swing resulting into a quite high DC consumption.

The solution proposed in this work with the receiver 1 relies on a sampling mixer showing at the same time a high linearity with low conversion losses on a 1V voltage supply. Using a pulsed LO waveform keeps the transistors in a safe area without sacrificing the linearity, which is a major challenge considering the low breakdown voltages of nm-scaled CMOS processes. As a result, the receiver 1 benefits from similar performances as in [28] under a lower voltage supply. Compared to [27], using a 2 stages LNA with a higher front-end gain results in a better NF_{SSB} and a lower ICP1dB. The measurements results of the standalone sampling mixer (chapter 2) with the RF input balun allows to estimate the performances which could be reached with a passive sampling mixer first approach as in [29]. By using a low noise IF voltage amplifier to compensate for the limited gain of the sampling mixer with the RF input balun (~8 dB) a similar gain as in [29] could be achieved with a ICP1dB of -1.5 dBm and a NF_{SSB} of 9.5 dB (estimated for a IFA input noise voltage of 1 nV/√hz). As in [28], [27] and [29] the IF LNA should use a 1.5V or 1.8V baseband voltage supply to amplify the mixer output signal without degrading the receiver linearity. Even if this approach appears as a good solution, the input impedance of the sampling mixer or voltage mode passive mixer as in [29] is quite high and depends on the LO signal magnitude and shape. Consequently, ensuring a good 50 Ω matching at the receiver input over the 76-81 GHz frequency band under any conditions is difficult.

Using at least a single stage LNA as in [27] to ensure a less sensitive wideband matching of the receiver input seems to be more appropriate to design a reliable receiver than a mixer first approach. This comparison demonstrates that thanks to the high performances of the proposed sampling mixer, the receiver 1 represents with [27], [28] and [29] the best trade-offs between noise and linearity of the state of the arts. By operating under a 1V supply this front-end also exhibits a low power consumption.

In this work the IF amplifier is only used as a buffer to isolates the circuit from the measurement setup and was not optimized to enhance the receiver performances. The previous discussion on a potential sampling mixer first approach show that a good prospect for this work would be to implement a low noise IF amplifier with a high linearity providing more gain before the rest of the baseband amplification as in [27], [28] and [29]. As the sampling mixer operates in voltage mode, implementing an IF LNA which does not degrade the linearity would require a higher voltage supply than for the RF block (1.5V or 1.8V). Using a current mode mixer can be a good solution to avoid high voltage swing at the IF amplifier input and enhance the receiver linearity while providing a high gain with an IF TIA. Nevertheless, the sampling principle is inherent to voltage mode mixer which use a hold capacitor to store the sampled voltage value. A current mode approach would not allow to benefit from the sampling behaviour. Another prospect for this work could be to find a solution to enable current mode sampling mixer by using an inductor to store the sampled current value.

The comparison of the receivers in Table 4-8 shows that CMOS radar receiver front-ends have a low power consumption compared to 77 GHz SiGe front-ends as in [20]. Nevertheless, in the receiver 1 and [58], [59], [29], [59] an additional frequency multiplier and/or LO driver are required. The receivers in [8], [24] and [26] include the LO frequency multiplier and LO drivers with the RF front-end giving access to the consumption and the silicon area dedicated to the LO distribution chain. Comparing the works in [8], [24] and [26] allow to estimate that a conventional 77 GHz LO distribution chain consumes around 40 mW and represents a 0.3 mm^2 silicon area which is comparable to the consumption and area of the associated receiver. Hence, using a conventional LO distribution chain can sometime double or triple the receiver consumption and area leading to a significant impact at the scale of a full radar transceiver chip including several receivers.

As a solution, the receivers 2 and 3 (this work) and the receivers in [31] and [30] are respectively based on sub-sampling and sub-harmonic mixers which uses a LO frequency sub-multiple of the RF frequency ($f_{LO} \approx f_{RF}/n$ with n a natural integer). The receivers based on this principle do not require an additional LO distribution chain which drastically simplifies the picture. The receivers 2 and 3 can use a 26 GHz VCO without requiring a frequency tripler and 77 GHz LO drivers. The sub-sampling mixers are also very compact as they do not require inductors. Consequently, the proposed receivers based on sub-sampling mixers save DC power and silicon area while keeping decent performances when compared to conventional radar receivers. The comparison between the receivers 2 and 3 and radar receivers based on sub-harmonic Gilbert cells in [31] and [30] highlights that using sub-sampling mixers lead to better overall performances with a higher ratio between f_{RF}/f_{LO}.

4.5 Conclusion

This chapter presents the implementation of the proposed sampling and sub-sampling mixers with a LNA to create 77 GHz radar receiver front-ends with the 28-nm FD-SOI CMOS technology. The receiver 1 exhibits noise and linearity performances aligned with best published results while bringing significant power consumption reduction. The implementation of sub-sampling mixers in the receivers 2 and 3 demonstrates that the sub-sampling allows to use a 26 GHz LO frequency to converts a 77 GHz RF signal with a penalty (3 dB for the NF and 3-4 dB for the compression point). As a result, this approach significantly simplifies the LO distribution chain of the receivers, saving area and reducing power consumption. To conclude, this chapter highlights that using the sampling principle results in high performances or allows to drastically simplify the architecture of 77 GHz radar receivers. Therefore, using sampling-based receivers appears as a solution to get the best from nm-scaled CMOS processes at millimeter-wave frequencies.

General conclusions

In the last decade, driving assistance products have continuously been improved to reach a high level of automation in recent vehicles. The next generation of cars will ensure driving safety by providing a full detection coverage around the car. The 77 GHz automotive radar is the only one able to assess the range, speed and direction of a target under bad weather conditions. Consequently, it will be essential to enhance driving assistance products. As more radar sensors associated to an advanced signal processing will be necessary to reach the next steps of driving automation, the CMOS technologies are preferred for the design of the next generation of integrated radar transceiver. CMOS technologies benefit from a lower production cost and a better circuit integration allowing to integrate a part of the signal processing in the transceiver chip. Nevertheless, the design technics used for the first transceiver chips in BiCMOS technologies are no longer relevant to design millimeter-wave CMOS receivers. The aim of this work is to demonstrate that using the sampling principle which is an approach inherent to CMOS processes will lead to high performance 77 GHz radar receivers.

In the chapter 1, the 77 GHz automotive radar and the associated design requirements are presented. The main existing solutions to design a 77 GHz radar receiver are then discussed highlighting that even if receivers based on active Gilbert cells showed very good performances with BiCMOS technologies, active mixers are not very appropriates to CMOS radar receiver design. Analysing the trends in the literature related to 77 GHz CMOS receiver design shows that using passive mixer topologies appears as the best solution to design a 77 GHz radar receiver in 28-nm FD-SOI CMOS technology. Some works on sub-harmonic mixers also put forwards that this approach can be promising to propose simpler 77 GHz radar receiver architectures by reducing the complexity of a 77 GHz LO distribution chain.

The chapter 2 introduces the sampling mixer principle and a new sampling mixer, operating at mm-wave frequencies, is proposed. The discussion puts forward that driving the mixer with a low duty cycle LO signal, in addition to a capacitive load, creates a sampling behaviour improving the conversion gain and linearity when compared with a 50% duty cycle driven mixer. Nevertheless, the generation of a low duty cycle signal at 77 GHz is a critical point. As

a solution an innovative 77 GHz pulse shaper able to turn the LO signal into a pulsed waveform is proposed. The implementation of the LO pulse shaper and a double-balanced passive mixer in a 28-nm FD-SOI CMOS technology validates this new sampling mixer topology combining a good conversion gain with a high linearity. According to these results, using sampling for down-conversion seems to be the right approach to take the best from nm-scaled CMOS processes. The proposed principle will still be valid for next CMOS nodes, with a preference of FD-SOI which enable some adjustments. This work has been accepted for the IMS 2022 conference.

The chapter 3 investigate the opportunity to use the sub-sampling principle to convert a RF signal around 77 GHz by using three times lower LO frequency thus simplifying the 77 GHz receiver LO distribution chain. A 3x sub-sampling mixer topology relying on digital gates for the LO pulse shaping is proposed. Two versions of this topology are presented and implemented in 28-nm FD-SOI CMOS. An innovative solution consisting in the co-integration of the AND function with the mixer core is used in the second version to overcome the frequency limitation due to the complexity of the AND gates. The measurement results prove that using sub-sampling allows to convert a 77 GHz by using a 3x lower LO frequency while keeping decent performances when compared to the sampling mixer designed in the chapter 2. Digital pulse shaping technics will take advantage of CMOS gate scaling and, once again FD-SOI will allow fine performance tuning. This implementation has been presented to SiRF 2022 and has been submitted for ESSCIRC 2022.

The chapter 4 draws the conclusion of this work by presenting the implementation of the proposed sampling and sub-sampling mixers with a LNA in 77 GHz radar receiver front-ends with the 28-nm FD-SOI CMOS technology. The receiver based on the sampling mixer proposed in the chapter 2 exhibits a very good trade-off between noise and linearity with a low power consumption. The implementation of sub-sampling mixers presented in the chapter 3 in receiver front-ends demonstrates that the sub-sampling allows to use a 26 GHz LO frequency to converts a 77 GHz RF signal while keeping a decent noise/linearity trade-off when compared to other solutions. As a result, this approach significantly simplifies the LO distribution chain of the receivers, saving area and reducing power consumption.

To conclude, this works highlights that using the sampling principle results in high performances or allows to drastically simplify the architecture of 77 GHz radar receivers. Consequently, using sampling-based receivers is a good approach to take advantage from the strengths of nm-scaled CMOS processes at millimeter-wave frequencies. This thesis work shows some important prospects. In a first step, to master the sub-sampling design technic, analysis of the $1/f$ noise simulation vs measurement discrepancies is needed. In a second step, working on calibration is important. On each implementation, body biasing capability has been used to fine tune performances (mainly DC). Dedicated procedure and hardware are needed to bring this demonstrator to a product maturity.

Publications

International conferences

- A. Flete, C. Viallon, P. Cathelin and T. Parra, "A ×3 Sub-Sampling Mixer for a 77 GHz Automotive Radar Receiver in 28 nm FD-SOI CMOS Technology," *2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2022, pp. 52-54, doi: 10.1109/SiRF53094.2022.9720061.

- A. Flete, C. Viallon, P. Cathelin and T. Parra, " New 77 GHz Sampling Mixer in 28-nm FD-SOI CMOS Technology for Automotive Radar application," *IEEE MTT-S International Microwave Symposium (IMS).*

- A. Flete, C. Viallon, P. Cathelin and T. Parra, " A Low-Loss 77 GHz Sub-Sampling Passive Mixer Integrated in a 28-nm CMOS Radar Receiver" *IEEE European Solid State Circuits Conference (ESSCIRC)*. (Accepted)

National conference

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Annex: Sampling mixer thermal noise calculation

To compute the output voltage noise spectral density added by the sampling mixer, all r_{on} thermal noise conversions around LO harmonics must be added:

$$N_{th_{out}} = 2.N_R.\sum_{-\infty}^{\infty} G_c^2(n.f_{LO}) \quad with\ N_R = 2KTr_{on} \tag{A-1}$$

The calculation of the summation of the sampling mixer conversion gain around each LO harmonic is detailed here below:

$$\sum_{-\infty<i<\infty} G_{c_i}^2 = \sum_{-\infty<i<\infty} \frac{1}{2}.sinc^2(iD)\left(1-e^{-j.\pi.i}\right) = \sum_{\substack{-\infty<i<\infty \\ i\neq pair}} sinc^2(iD) \tag{A-2}$$

$$= 2.\sum_{\substack{1<i<\infty \\ i\neq pair}} sinc^2(iD) = 2.\frac{1}{2}\left[\sum_{i=1}^{\infty} sinc^2(iD) + \sum_{i=1}^{\infty}(-1)^{i+1}sinc^2(iD)\right] \tag{A-3}$$

Both sum of the decomposition proposed in (A-3) will be calculated separately:

$$\sum_{i=1}^{\infty} sinc^2(iD) = \frac{1}{(\pi D)^2}\sum_{1}^{\infty}\frac{1-\cos(2\pi Di)}{2i^2} = \frac{1}{2(\pi D)^2}\left[\sum_{1}^{\infty}\frac{1}{i^2} - \sum_{-\infty}^{\infty}\frac{\cos(2\pi Di)}{i^2}\right] \tag{A-4}$$

The calculation of both sum in (A-4) is provided in [60]:

$$\sum_{1}^{\infty}\frac{1}{i^2} = \frac{\pi^2}{6} \tag{A-5}$$

$$\sum_{-\infty}^{\infty}\frac{\cos(2\pi Di)}{i^2} = \frac{\pi^2}{6} - \frac{2\pi^2 D}{2} + \frac{(2\pi D)^2}{4} \tag{A-6}$$

Using these results in (A-4) gives:

$$\sum_{1}^{\infty} sinc^2(iD) = \frac{1}{2(\pi D)^2}\left[\frac{\pi^2}{6} - \left(\frac{\pi^2}{6} - \frac{2\pi^2 D}{2} + \frac{(2\pi D)^2}{4}\right)\right] = \frac{1}{2}.\left(\frac{1}{D} - 1\right) \quad \text{(A-7)}$$

The second sum in (A-3) is calculated as:

$$\sum_{i=1}^{\infty}(-1)^{i+1} sinc^2(iD) = \sum_{1}^{\infty}(-1)^{i+1}\frac{\sin^2(\pi Di)}{(\pi Di)^2} = \frac{1}{(\pi D)^2}\sum_{1}^{\infty}(-1)^{i+1}\frac{1-\cos(2\pi Di)}{2i^2} \quad \text{(A-8)}$$

$$= \frac{1}{2(\pi D)^2}\left[\sum_{1}^{\infty}(-1)^{i+1}\frac{1}{i^2} - \sum_{-\infty}^{\infty}(-1)^{i+1}\frac{\cos(2\pi Di)}{i^2}\right] \quad \text{(A-9)}$$

According to [60]:

$$\sum_{1}^{\infty}(-1)^{i+1}\frac{1}{i^2} = \frac{\pi^2}{12} \quad \text{(A-10)}$$

$$\sum_{-\infty}^{\infty}(-1)^{i+1}\frac{\cos(2\pi Di)}{i^2} = \frac{\pi^2}{12} - (\pi D)^2 \quad \text{(A-11)}$$

Finally:

$$\sum_{i=1}^{\infty}(-1)^{i+1} sinc^2(iD) = \frac{1}{2(\pi D)^2}\left[\sum_{1}^{\infty}(-1)^{i+1}\frac{1}{i^2} - \sum_{-\infty}^{\infty}(-1)^{i+1}\frac{\cos(2\pi Di)}{i^2}\right] \quad \text{(A-12)}$$

$$= \frac{1}{2(\pi D)^2}\left[\frac{\pi^2}{12} - \left(\frac{\pi^2}{12} - (\pi D)^2\right)\right] = \frac{1}{2} \quad \text{(A-13)}$$

When combining (A-7) and (A-13) the sum in (A-3) can be calculated:

$$\sum_{\substack{-\infty<i<\infty \\ i\neq pair}} sinc^2(iD) = 2.\frac{1}{2}\left[\sum_{i=1}^{\infty} sinc^2(iD) + \sum_{i=1}^{\infty}(-1)^{i+1} sinc^2(iD)\right] \quad \text{(A-14)}$$

$$= \left[\frac{1}{2D} - \frac{1}{2} + \frac{1}{2}\right] = \frac{1}{2D} \quad \text{(A-15)}$$

As a conclusion:

$$N_{th_{out}} = 2.N_R.\sum_{-\infty}^{\infty} G_c^2(n.f_{LO}) = 2.2KTr_{on}.\frac{1}{2D} = \frac{2KTr_{on}}{2D} \quad \text{(A-16)}$$

To calculate the one-sided noise spectral density, (A-16) is multiplied by a factor 2 giving:

$$N_{th_{out}} = \frac{4KTr_{on}}{D} \quad \text{(A-17)}$$

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