

# Hybrid Limit Cycles: from theory to practice in resonant converters

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# Doctorat de l'Université de Toulouse

préparé à l'Université Toulouse III - Paul Sabatier

# Hybrid Limit Cycles:

# from theory to practice in resonant converters

Cycles Limites Hybrides : de la théorie à la pratique dans les convertisseurs résonants

Thèse présentée et soutenue, le 25 octobre 2024 par

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# Abstract

#### "Hybrid Limit Cycles: from theory to practice in resonant converters"

This dissertation addresses the stabilization of periodic trajectories in hybrid dynamical systems, focusing on resonant power converters from both theoretical and practical perspectives. The focus is twofold: on one side there are the theoretical analyses and simulations that show specific behaviors; on the other side there is the "on-the-field" work involving hardware and software development and coding to create a functioning controller that confirms the validity of the theory. The aim of this dissertation is to integrate the theoretical control aspects with the practical power electronics aspects, starting from the analysis of different control laws that ensure an oscillating behavior, and ending with a current regulation problem on a power converter prototype.

Initially, we build the theoretical framework for the formal analysis of systems exhibiting both continuous and discrete behavior, the so-called hybrid dynamical systems. We focus particularly on second-order resonant converters, which are relatively easy to represent but present some challenges. In this initial part we overview control laws that ensure a desired self-oscillating behavior with different properties in terms of switching and design efficiency, with the focus on the Zero-Voltage Switching (ZVS) behavior. After focusing on the second-order resonant converter, we extend the control algorithm to the third-order LLC resonant converter. In other words, we apply the same controller used for second-order systems to a more complex converter with richer behavior and observe what is the outcome. This extension anticipates the eventual validation of our controller on a battery charger, which uses the LLC topology. Indeed, the latter part of the manuscript is dedicated to the realization and testing of an LLC prototype, with the objective of validating the theoretical results and the formulated conjectures. The prototype includes all power stages, from the resonant tank to the rectifier, as well as the necessary sensing. The control law is implemented in a Field-Programmable Gate Array (FPGA). The final step is the regulation of the output current of the converter while ensuring ZVS of the transistors.

# Résumé

#### "Cycles Limites Hybrides : de la théorie à la pratique dans les convertisseurs résonants"

Cette thèse traite de la stabilisation des trajectoires périodiques dans les systèmes dynamiques hybrides, en se concentrant sur les convertisseurs résonants de puissance, à la fois d'un point de vue théorique et pratique. L'objectif est double : d'un côté, des analyses théoriques et des simulations permettent de démontrer et mettre en évidence certains comportements ; de l'autre, une mise en œuvre expérimentale impliquant le développement de l'électronique et le codage pour créer un contrôleur fonctionnel illustre le bien-fondé des approches proposées d'un point de vue théorique. Le but de ce travail est d'intégrer les aspects théoriques du contrôle avec les aspects pratiques de l'électronique de puissance, en commençant par l'analyse de différentes lois de contrôle qui assurent un comportement oscillant, et en terminant par un problème de régulation de courant sur un proto-type de convertisseur.

Dans un premier temps, nous construisons le cadre théorique pour l'analyse formelle des systèmes présentant un comportement à la fois continu et discret, également appelés systèmes dynamiques hybrides. Nous nous concentrons particulièrement sur les convertisseurs résonants du second ordre, qui sont relativement faciles à représenter, mais qui présentent certains défis. Dans cette première partie, nous reproduisons et proposons des lois de contrôle qui garantissent un comportement auto-oscillant souhaité avec différentes propriétés en termes de commutation et d'efficacité de conception, en mettant l'accent sur le comportement de commutation à tension nulle (Zero-Voltage Switching – ZVS). Après nous être concentrés sur le convertisseur résonant de second ordre, nous étendons le contrôle au convertisseur résonant LLC de troisième ordre. En d'autres termes, nous appliquons le même contrôleur que celui utilisé pour les systèmes de second ordre à un convertisseur plus complexe au comportement plus riche, et nous observons le résultat. Cette extension anticipe la validation de notre contrôleur sur un chargeur de batterie, qui utilise la topologie LLC. Par conséquent, la dernière partie du manuscrit est consacrée à la réalisation et à l'essai d'un prototype LLC, dans le but de tester les résultats théoriques et les conjectures formulées. Le prototype comprend tous les étages de puissance, du réservoir résonant au redresseur et tous les capteurs nécessaires. La commande est mise en œuvre dans un circuit logique programmable (Field-Programmable Gate Array – FPGA). L'étape finale est la régulation du courant de sortie du convertisseur tout en garantissant le ZVS des transistors.

# Sommario

#### "Cicli Limite Ibridi: dalla teoria alla pratica nei convertitori risonanti"

Questa tesi affronta il problema la stabilizzazione di traiettorie periodiche in sistemi dinamici ibridi, concentrandosi sui convertitori di potenza risonanti da una prospettiva sia teorica che pratica. L'attenzione è duplice: da un lato le analisi teoriche e le simulazioni mostrano determinati comportamenti, dall'altro lato il lavoro in laboratorio che comprende lo sviluppo dell'elettronica e del codice. L'obiettivo di questo lavoro è integrare gli aspetti teorici del controllo con quelli pratici dell'elettronica di potenza, partendo dall'analisi di diverse leggi di controllo che assicurano un comportamento oscillante e terminando con un problema di regolazione della corrente su un prototipo di convertitore.

Inizialmente costruiamo il quadro teorico per l'analisi formale di sistemi che presentano un comportamento sia continuo che discreto, i cosiddetti sistemi dinamici ibridi. I convertitori risonanti del secondo ordine sono al centro della discussione dato che sono relativamente facili da rappresentare ma che al contempo presentano delle sfide. La strada naturale per l'analisi e la progettazione del controllo è quella dei sistemi ibridi che combina strumenti della teoria dei sistemi dinamici continui e discreti. Nella parte iniziale replichiamo e proponiamo leggi di controllo che assicurano il comportamento auto-oscillante desiderato con diverse proprietà in termini di commutazione ed efficienza, con particolare attenzione al comportamento di commutazione a zero tensione (Zero-Voltage Switching – ZVS). In seguito, questi risultati sono euristicamente estesi al controllo del convertitore risonante LLC del terzo ordine. In altre parole, applichiamo lo stesso controllore utilizzato per i sistemi del secondo ordine a un convertitore più complesso con un comportamento più ricco e ne osserviamo il risultato. Questa estensione anticipa la successiva validazione del nostro controllore su un caricabatterie basato sulla topologia LLC. L'ultima parte del manoscritto è dedicata alla realizzazione e al collaudo di un prototipo di un convertitore risonante LLC, con l'obiettivo di verificare i risultati teorici e le congetture formulate. Il prototipo comprende tutti gli stadi di potenza, dalla parte risonante al raddrizzatore, e tutti i sensori necessari. Il controllo è implementato in un Field-Programmable Gate Array (FPGA). Il passo finale è la regolazione della corrente di uscita del convertitore, garantendo al contempo l'efficienza dalla commutazione grazie allo ZVS.

# Abstracte

#### "Cicles Límits Híbrids: de la teoria a la pràctica en convertidors ressonants"

Aquesta tesi tracta el problema de l'estabilització de trajectòries periòdiques en sistemes dinàmics híbrids, centrant-se en els convertidors de potència ressonants des d'una perspectiva tant teòrica com pràctica. El tractament és doble: d'una banda, les anàlisis teòriques i les simulacions mostren determinats comportaments; d'altra banda, el treball al laboratori que inclou el desenvolupament de l'electrònica i del codi. L'objectiu d'aquest treball és integrar els aspectes teòrics del control amb els pràctics de l'electrònica de potència, començant per l'anàlisi de diverses lleis de control que asseguren un comportament oscil·lant i acabant amb un problema de regulació del corrent en un prototip de convertidor.

Inicialment, construïm el marc teòric per a l'anàlisi formal de sistemes que presenten un comportament tant continu com discret, els anomenats sistemes dinàmics híbrids. La discussió es centra en els convertidors ressonants de segon ordre, ja que són relativament fàcils de representar, però al mateix temps presenten alguns reptes. El camí natural per a l'anàlisi i el disseny del control és el dels sistemes híbrids, que combina eines de la teoria de sistemes continus i discrets. A la part inicial, repliquem i proposem lleis de control que asseguren un comportament auto-oscil·lant desitjat amb diferents propietats en termes de commutació i eficiència, amb especial atenció al comportament de commutació a tensió zero (Zero-Voltage Switching - ZVS). Després, aquests resultats s'estenen de manera heurística al control del convertidor ressonant LLC de tercer ordre. En altres paraules, apliquem el mateix controlador utilitzat per als sistemes de segon ordre a un convertidor més complex amb un comportament més ric i n'observem el resultat. Aquesta extensió anticipa la posterior validació del nostre controlador en un carregador de bateries basat en la topologia LLC. L'última part del manuscrit està dedicada a la realització i prova d'un prototip d'LLC, amb l'objectiu de verificar els resultats teòrics i les conjectures formulades. El prototip inclou totes les etapes de potència, des de la part ressonant fins al rectificador, i tots els sensors necessaris. El control està implementat en una Field-Programmable Gate Array (FPGA). El pas final és la regulació del corrent de sortida del convertidor, garantint al mateix temps l'eficiència de la commutació gràcies al ZVS.

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We are in a world where technology is moving faster and faster. The rapid development of new tools and the high demand for novel solutions is increasing. A direction where the global community is pushing is electrification, with the hope of decreasing the production of greenhouse gases and fight climate change. The necessity of electrification stimulates many fields: power electronics for the development of new power conversion techniques, power systems to improve how the electricity is distributed in the grid, materials science to reduce the impact of new technologies or to unleash new routes, power generation from photovoltaic to nuclear, and many other related sectors.

This dissertation has its foundations in a practical question: "*How can we improve the control of resonant power converters?*". This query highlights the two research fields underpinning this work: control theory, and power electronics. *Control* is the field that analyzes, observes, and controls systems by developing mathematical theories and applying them to real-world problems. *Power electronics* focuses on the design, construction, and applications of power converters, whose objective is to transform electrical quantities from sources to loads, with the minimum power loss. This dissertation demonstrates how these two fields – which sporadically speak to each other – can collaborate and share knowledge.

In our everyday lives, we are surrounded by examples of control and power electronics. Control systems are ubiquitous, from the thermoregulation in our body to the operations of a washing machine. Power converters are in any electronic device that requires power level adjustments, such as battery chargers or DC-links in transmission stations. Both fields have been studied extensively for many years, with different solutions and novel techniques being proposed and tested. Power converters are electrical systems that leverage electronic semiconductor devices – such as MOSFETs, diodes, IGBTs, among many – which act as switches to open or close connections within a converter circuit, thereby changing its behavior. This on-and-off switching capability, achieved through relatively simple circuits, has revolutionized the field of energy conversion. For example, it is now possible to build much more compact and efficient voltage regulation circuits compared to earlier designs, which required significantly more space. From a control perspective, power converters are classical examples of *hybrid dynamical systems* – i.e., systems that present both a continuous and a discrete behavior – where the discrete behavior is represented by the switching actions of the semiconductor devices.

## **Objective and Context**

In this dissertation, the focus revolves around a particular type of power converters, the *resonant power converters*, known for the high power density and efficient conversion capabilities [Salem et al., 2018]. The objective is to propose different control laws that enable different behaviors in terms of waveforms and efficiency. These control laws are formulated and analyzed within the robust theoretical framework of hybrid dynamical systems, allowing us to draw conclusion about the stability and robustness. These control laws can then be employed in a dc-dc converter application that uses a resonant converter as its modulation stage. Hence, this manuscript encompasses the control theoretical problems with the experimental work in the laboratory for the validation, creating a connection between the mathematical formulation and the practical experience.

The key aspect of resonant converters is the capability to take advantage of the natural oscillation phenomenon – present when there is a network of capacitors and inductors called resonant tank – to generate a sinusoidal signal with high efficiency [Erickson and Maksimović, 2020]. In simple words, the resonant converter transforms a DC voltage into a sinusoidal one, that is why it is also referred to as *inverter* (Figure 1).



Figure 1: Basic representation of a resonant inverter with input and output signals.

In the context of resonant converters, numerous approaches have been proposed to ensure the oscillatory behavior [Youssef and Jain, 2004]. Among the various control strategies, we focus on the techniques that enable self-oscillating behavior, where the oscillating frequency is inherently determined by the internal operating conditions rather than being externally imposed. To model, analyze, and design control laws for resonant converters, we utilize hybrid dynamical systems theory as developed in [Goebel et al., 2012]. In particular, for the theoretical part of this manuscript, we keep the focus on second-order resonant converters, which can be represented in a plane. However, we will see how links can be drawn for third-order resonant converters, which can be generally found in applications due to their richer behavior. Anyway, since they cannot be fully represented in a plane, we will consider a projection on a plane to formulate the control law.

In the context of hybrid systems control theory, stabilizing limit cycles is a nontrivial problem that has been addressed in various works [Grizzle et al., 2001; Simic et al., 2002; Bisoffi et al., 2018; Lou et al., 2023]. A commonly adopted solution involves identifying a Poincaré map, a tool that describes the dynamics of a system in a discrete manner by examining the starting and the arriving points of a trajectory on the same surface. Using this discrete description, it is usually possible to identify a fixed point – if it exists – and demonstrate whether it is Globally Asymptotically Stable (GAS).

One important part that needs to be considered when designing a power converter is efficiency. The losses occur in different parts of a converter: switching losses that occur during the on-off transition and vice versa of the devices; conduction losses due to current flowing in dissipative elements; core and copper losses that occur in the passive components due to magnetic effects and Joule heating. In resonant converters, a significant portion of losses is concentrated in the switching losses, which are proportional to the high switching frequency typically in the order of hundreds of kHz for these converters. Therefore, one objective that the control should guarantee is to reduce the switching losses, and this is possible by ensuring Zero-Voltage Switching (ZVS) in the case of a resonant converter. ZVS means that the switch occurs when the voltage through the device (switch) is approximately zero, i.e., the commutation is happening in soft-switching conditions. Otherwise, if the voltage is not zero, the commutation occurs in hard-switching conditions. These two different commutation situations are represented in Figure 2, where the dotted area is related to the losses during hard-switching.



Figure 2: Comparison of the signals in the case of hard and soft switching.

In the final stage of this manuscript, we consider the application of resonant converters in battery chargers, focusing specifically on regulating the output current that charges the battery. To achieve this, we employ a simple closed-loop control scheme: the Proportional-Integral (PI) controller. The choice is motivated by the need for an implementation that is both straightforward and effective, capable of easily adapting to changing conditions. For the experimental part on the battery charger we are inspired by the work done in [Deng et al., 2014]. We develop a system that contains all the necessary stages from the resonant inverter to the rectifier, so that a resonant dc-dc converter is obtained as shown in Figure 3. Considering a battery charger presents an extra challenge: the resonant tank is a third-order one and its load is nonlinear. Moreover, from the implementation perspective, implementing the hybrid control laws relies on the continuous knowledge of the signals, which is challenging when the controller is implemented digitally.



Figure 3: Representation of a resonant converter with the DC-AC stage and the AC-DC stage.

## **Organization and Contributions**

The organization of the manuscript mirrors the workflow that guided our research, beginning with theoretical analysis and finishing with the experimental implementation. The manuscript is structured in two parts. The first part, comprising the chapters, presents the essential results developed during the thesis, highlighting the contributions from a research perspective. The second part consists of the appendices, providing the necessary tools for comprehending the work: methodological aspects in the first two appendices, and practical aspects in the latter ones. The contributions in Appendices C and D stem from the "know-how" of the author and common knowledge in the field, rather than representing pure research work. Nonetheless, the implementation of the results in an experimental prototype required significant effort and time, including: designing the electronic circuit; designing, building and testing the Printed Circuit Boards (PCBs); and writing and debugging the code.

**Chapter 1** introduces resonant power converters giving an overview on the state of the art. It continues with the detailed description of second-order topologies introducing a novel change of coordinates – initially introduced in [Zaupa et al., 2021] – that allows unifying the description for the two possible topologies, the parallel and the series. The chapter ends with the description of third-order LLC, which is the topology used at the end of the thesis for the battery charger.

**Chapter 2** contains general notions about hybrid dynamical systems, with a focus on power converters. Soft switching conditions are discussed, with a particular regard towards Zero-Voltage Switching (ZVS) in an H-bridge configuration.

**Chapter 3** discusses a frequency modulation control law presented in [Zaupa et al., 2023a]. Hybrid dynamical system theory is used to model the system and the proof of stability and uniqueness for the hybrid periodic orbit is provided. Frequency modulation control law is shown to be effective on an experimental series resonant converter prototype, whose design is reported in the chapter.

**Chapter** 4 discusses a phase-shift modulation control law presented in [Zaupa et al., 2023b]. Hybrid dynamical system theory is used to model the system and the proof of stability and uniqueness for the hybrid periodic orbit is provided. Phase-shift modulation control law is shown to be effective on an experimental series resonant converter prototype.

Chapter 5 tackles the design and control of a dc-dc converter, with particular attention to the battery charger application. A novel mixed modulation control law that combines frequency and

phase-shift modulation is proposed, ensuring ZVS and reduced frequency range. Considering a dcdc converter, the resonant tank becomes a third-order one, and the analysis and approximations of the additional stages for the rectifier are included in order to give a global overview. The objective of the dc-dc converter is to regulate the output current. To this end a control loop with a Proportional-Integral (PI) controller and anti-windup feedback is introduced, together with a Linear Matrix Inequality (LMI) based technique. In the end, the experimental prototype design is discussed in a brief way to complete the description and prepare the terrain for the following chapter.

**Chapter 6** contains the experimental results obtained on the dc-dc converter prototype for battery charging applications. Various test conditions are considered, by initially validating the mixed modulation control law and then the closed-loop behavior when ensuring constant current to a constant voltage load (e.g., a battery). The frequency and phase-shift modulation control laws are also validated on the LLC resonant converter experimental prototype in order to show that the modulation control laws developed for second-order converters can be employed in third order LLC converters.

Five appendices are included to complete the manuscript with complementary material.

Appendix A reports the proofs of two lemmas useful in Chapters 3 and 4.

Appendix B reports on general knowledge about electronic circuit design and components.

Appendix C discusses the prototype design considering all the stages and related problems.

Appendix D reports the code used for the implementation of all the control loops in a FPGA.

## **Publications**

Several publications are linked to this work. A conference paper [N1] was initially produced during my master internship in the group of automatic control and industrial electronics (GAEI) of Universitat Rovira i Virgili (Spain), with which I kept the collaboration during the PhD. [N1] presents the hybrid model for second-order resonant converters, which served as ground for the future work, and proposes a frequency modulation control strategy. During the PhD, these ideas were further developed and shown to be effective in two journal publications. In [N2], the frequency modulation control law is demonstrated to be stable, and it is experimentally validated on a series resonant converter. In [N3], a phase-shift modulation control law is proposed, its stability is proven, and it is experimentally validated. A final side project [N4] addressing the RMS current regulation problem in a series resonant converter was conducted in collaboration with a PhD colleague. This publication has received the *Young Author Award* of the MICNON conference. This work includes an analytical study of the closed-loop model, including saturation, and proposes a hybrid dynamical system to estimate the RMS value of the output current. Contributions in [N1,N2,N3] are described in Chapters 1, 3 and 4.

[N1] Zaupa Nicola, Martínez-Salamero Luis, Olalla Carlos, and Zaccarian Luca. (2021). Results on hybrid control of self-oscillating resonant converters. *IFAC-PapersOnLine*, 54(5):211–216.

[N2] Zaupa Nicola, Martínez-Salamero Luis, Olalla Carlos, and Zaccarian Luca. (2023). Hybrid Control of Self-Oscillating Resonant Converters. *IEEE Transactions on Control Systems Technology*, 31(2):881–888.

**[N3]** Zaupa Nicola, Olalla Carlos, Queinnec Isabelle, Martínez-Salamero Luis, and Zaccarian Luca. (2023). Hybrid Control of Self-Oscillating Resonant Converters With Three-Level Input. *IEEE Control Systems Letters*, 7:1375–1380.

[N4] Doré Manon and Zaupa Nicola. (2024). Control of the RMS Output Current in Series Resonant Converters. In IFAC-PapersOnLine, volume 58 of 4th IFAC Conference on Modelling, Identification and Control of Nonlinear Systems MICNON 2024, pages 132–137.

Two papers are ongoing works. One is related to the continuity of Poincaré maps in hybrid dynamical systems following a visit of Rafal Goebel at INSA Toulouse. Another is related to the experimental part of this manuscript contained in Chapters 5 and 6, showing the capability of the proposed controller on a battery charger.

[N-] Goebel Rafal, Queinnec Isabelle, Zaccarian Luca, and Zaupa Nicola. (2024). Outer-semicontinuity of Poincaré set-valued mappings in Hybrid Dynamical Systems. *Ongoing work*.

[N-] Zaupa Nicola, Olalla Carlos, Queinnec Isabelle, Martínez-Salamero Luis, and Zaccarian Luca. (2024). Hybrid Control of Self-Oscillating Resonant Converters for Battery Charging. *Ongoing work*.

During the course of my thesis, I also had the opportunity to explore the problem of synchronization in multi-agent systems from a theoretical perspective. Although this work falls outside the primary scope of this manuscript and it is not reported here, it led to two contributions: one published in the proceedings of a conference and another one in a journal. Nevertheless, the stability conditions developed in **[N6]** could be applied to the synchronization of a network of converters.

**[N5]** Zaupa Nicola, Zaccarian Luca, Tarbouriech Sophie, Queinnec Isabelle, and Giordano Giulia. (2023). Controlling Identical Linear Multi-Agent Systems Over Directed Graphs. *In 2023 62nd IEEE Conference on Decision and Control (CDC)*, pages 7395–7400.

**[N6]** Zaupa Nicola, Giordano Giulia, Queinnec Isabelle, Tarbouriech Sophie, and Zaccarian Luca. (2024). Equivalent Conditions for the Synchronization of Identical Linear Systems over Arbitrary Interconnections. *European Journal of Control*, Volume 80, Part B, 2024, 101099, ISSN 0947-3580.

# 1

# **About Resonant Converters**

In this chapter we will start by discussing – in general terms – what are resonant converters and where they are employed. Since the modeling part is interlaced with the control one, we will also go through several control techniques that have been employed over time. Afterwards, we will go more into the details of the modeling, mostly for second-order resonant converters, but we will also discuss a third-order topology, which will be useful when considering the battery charger application in Chapter 5. We will finish with an overview on dc-dc converters for battery charging.

The second-order resonant converters analysis and modeling is useful since it is relatively simple and allows extending the same properties and intuitions to higher order converters. Let us remark that the word *converter* may not be the most appropriate word to use as compared to *inverter*, since we initially consider systems whose output is an Alternating Current (AC). Second-order converters mainly have a theoretical interest for their *easy* tractability. From an application point of view, thirdorder (or higher) resonant converters are indeed more common. For example, having a transformer to isolate the output of the resonant tank introduces an inductor (corresponding to the magnetizing inductance of the transformer) in parallel to the output, implying that a third-order model might be more suitable under some conditions.



Figure 1.1: General scheme of a resonant converter (inverter) that we are considering.

## 1.1 Introduction to Resonant Power Converters

A resonant power converter contains a resonant tank, in which current and voltage are high-frequency AC signals. The output of the converter may be rectified and filtered for a Direct Current (DC) output, or directly used in AC loads, functioning as an *inverter*. The resonant frequency is usually in the order of the tens or hundreds of kHz. Figure 1.1 illustrates a generic resonant converter (inverter). The core is the resonant tank that comprises an L-C network – which define the order of the converter – characterized by sinusoidal time-varying waveforms of current and voltage, driven by a switch network – which define the input waveform type – supplied by an external DC power supply. Consequently, the topology is relatively straightforward and practical to implement.

The resonant converter takes advantage of the resonance phenomenon to reduce losses and achieve high efficiency in generating a sinusoidal signal [Erickson and Maksimović, 2020]. Under certain conditions, the resonant tank is characterized by an oscillatory behavior, which we want to take ad-



Figure 1.2: Examples of topologies for the resonant tank networks.

vantage of. Since the range of variation of voltage and current is usually large, small signal approximations are not applied but rather a first harmonic approximation (FHA) is used for the analysis. This approximation is generally valid when the resonant tank is acting as a filter removing highorder harmonics. To be more precise, the operating conditions depend on the oscillating frequency (i.e., how far it is from the resonant one) and from the load (i.e., the quality factor). The first harmonic approximation is accurate as far as the converter has a high quality factor, and is operating in continuous conduction mode, hence when the signals in the resonant tank are mostly sinusoidal.

Resonant converters are well-known in the power electronics industry due to numerous advantages, including soft-switching, reduced switching losses, and high power densities (high power factor), if they operate near the resonant frequency. Thanks to these features, during the years many strategies – more or less sophisticated depending on the application – have been considered to model and control resonant converters. These converters find application in fields like: inductive heating where the output is a 20-100 kHz current [Lucia et al., 2009], wireless power transfer [Bojarski et al., 2014], battery charging where the output is a DC current [Park and Choi, 2014; Deng et al., 2014], electronic ballast that needs frequency control [Yin et al., 2003], medical application [Cavalcante, 2006], renewable energy systems [Krishnaswami and Mohan, 2009; Suryawanshi et al., 2018], systems with piezoelectric transducers, among many others.

#### 1.1.1 Types of resonant tanks

The resonant tank is the L-C network constituting the core of the converter, providing the ability to generate an oscillatory behavior. Hence, the resonant tank has to be composed of at least a capacitor and an inductor. Figure 1.2 depicts some possible topologies that can be found when working with resonant converters. The simplest topology that we can think of is a combination of one inductor and one capacitor, where we have the inductors in series with the input and the capacitor either in series or in parallel with the load forming a Series Resonant Converter (SRC) or a Parallel Resonant Converter (PRC), respectively. These two topologies are of second-order since they are composed of two independent components; equivalently, the circuit of the resonant tank can be described by a second-order differential equation. Then, other components can be added in order to enrich the possible behaviors and properties, notably of the frequency response. Higher order topologies arise also when there is the need to interface the converter with other components. A typical case is when a transformer is used to isolate the output voltage from the downstream, resulting in the addition of an inductor (the magnetizing inductance of the transformer) in parallel to the output, which also enables boost operation (namely, the output voltage can be higher than the input). Regarding thirdorder resonant converters, there are two classical topologies. Both are characterized by an inductor and capacitor in series with the input. Then, we can have either a capacitor or an inductor in parallel with the output, which is the case of the LCC or LLC converter, respectively.

#### 1.1.2 Analysis techniques

Several approaches have been used for the analysis of resonant converters, from the simplest ones, where only a specific topology is considered, like the second-order converter in [Vorperian, 1989], to more generalized formulations where different topologies are analyzed with the same high-order model using first-harmonic approaches or linearization [Bhat, 1991; Cutrona and Di Miceli, 1992]. Then, considerations for a specific configuration can be done by fixing some values of the parameters either to zero or infinity.

Here, we will focus our attention on the modeling using the theory of hybrid dynamical systems developed in [Goebel et al., 2012]. We can see it as a generalization of the affine models used in [Molla-Ahmadian et al., 2012]. The advantage is that we have powerful analysis tools for stability and robustness analysis coming from a solid theoretical framework. Within this framework is easy to cast both continuous and discrete states, as well as differential and difference equations – more in general also set-valued mapping.

Since resonant converters are characterized by oscillations, it is natural to reason in terms of period behavior and cycles. This is the reason why we are interested in the so-called *stability* of *limit cycles*; in other words, we are interested in the stability of a periodic behavior. First approaches in the case of resonant converters appear in [Hernandez et al., 2003] where the stability of the induced limit cycle with the switching mechanism for the start-up is analyzed with a Poincaré map. Further developments in that direction include [Molla-Ahmadian et al., 2012; Molla-Ahmadian et al., 2015; Afshang et al., 2017] that analyze series resonant converters with switched affine models, followed by [Bonache-Samaniego, 2017; El Aroudi et al., 2019] who demonstrate that state-plane based methods can outperform the dynamics of conventional approaches, but with limited stability guarantees.

#### 1.1.3 Control techniques

Control of resonant converters is a well-known problem in power electronics associated with several solutions [Erickson and Maksimović, 2020; Oruganti and Lee, 1985b; Youssef and Jain, 2004]. Essentially, the magnitudes of the currents and voltages in the resonant tank can be modified by acting on the frequency or the amplitude of the input voltage. Two main categories can be identified looking at the operating frequency, with it either being kept constant or variable. There are advantages and disadvantages in both: for a resonant converter it is detrimental to change the frequency from the nominal one but, at the same time, changing the frequency allows increasing the output range of the converter. Changing the frequency impacts the efficiency of the magnetic components (inductors and transformers) since they are designed to operate in a specific and restricted range of frequencies. Another notable distinction lies between converters where the frequency is externally imposed and others where the operating frequency emerges from the operating conditions, which is the case of the *self-oscillating* resonant converters.

**Variable-frequency.** Frequency modulation techniques are common in applications where there is the need for a wide range of output amplitudes. The switching frequency is the control input, with the input voltage being either positive or negative. Usually, this kind of control offers good softswitching properties and induces the desirable ZVS behavior; on the downside, the regulation of the operating point may require a wide frequency range. One way to exploit it is through a Voltage-Controlled Oscillator (VCO): the switching frequency is externally imposed by the VCO and the implementation is straightforward [Yin et al., 2003]. On the same idea, self-sustained oscillation techniques have been proposed: the converter sets its operating frequency at the resonant frequency (or nearby it) without being externally imposed [Pinheiro et al., 1999; Bonache-Samaniego et al., 2016]. As said, the counterpart of these *frequency modulation* techniques is the wide range of frequencies that on one side complicates the control implementation and on the other side makes it hard to optimize the design of the circuit. On the other hand, these techniques are suitable when the converter needs to work in some specific narrow range. **Constant-frequency.** The advantage of keeping the oscillating frequency constant stands in the opportunity to simplify the design of the converter: it is possible to optimize the choice of the components and therefore to minimize the losses. In order to modulate the amplitude of the signals in the resonant tank other parameters of the input need to be changed. One possibility is to have a period of time at which the input voltage of the resonant tank is zero, allowing one to modulate the amplitude of the first harmonic of the input voltage. Another option is to change the duty-cycle with the consequence that the average value is not zero. This can be achieved with different techniques that have different properties summarized in [Burdio et al., 2001]. Among them, we can recognize: *phase-shift* or *clamped mode* where the input is symmetric with a period of time at zero; *asymmetrical duty-cycle* in which the duty cycle is changed; and *asymmetrical clamped-mode* that combines the two previous techniques. In these techniques the control input is either the phase-shift between the two legs of the switches or the duty-cycle. Figure 1.3 represents the different waveforms for the amplitude modulation laws cited above.



Figure 1.3: Different waveforms for the input voltage for constant-frequency control laws.

**Remark 1.1** In the literature, we can find the generic denomination amplitude modulation, which stands for the generic techniques that act on the amplitude of the first harmonic of the input voltage. In our case, we will focus on the phase-shift modulation case. This name comes from the technique originally used to implement it: in the case of an H-bridge, the command signals of the two legs are shifted with respect to each other, generating a combination that implies a period in which the output of the H-bridge is shorted.

**Other techniques.** Additional techniques that merge the useful aspects of constant and variable frequency have been proposed. The core idea behind them is to operate in a limited range of frequencies, allowing ZVS, and to compensate for the consequent limited output range by modulating the amplitude. The combination of self-oscillating behavior with phase-shift modulation is used in [Youssef et al., 2006]. A two-mode operation, variable frequency and phase-shifted Pulse-Width Modulation (PWM), is presented in [Lo et al., 2011]. Other propositions consider multilevel converters at the expense of increasing the number of required switches [Bojarski et al., 2015; Peter and Mathew, 2021]. A multiphase solution is presented in [Bojarski et al., 2014].

#### Self-oscillating behavior

The techniques discussed so far encompass various methods for controlling a resonant converter. When the oscillating frequency is externally imposed (like the VCO case) the controller may not be robust to parameter variations, which determine variations in the resonant frequency. This is not the case for *self-oscillating* resonant converters, also known as *self-sustained* oscillating resonant converters, which inherently determine their oscillating frequency based on internal operating conditions. One of the inherent advantages of self-oscillation is that the converter can be operated at the resonant frequency with no compensation for changes in the parameters of the resonant tank. Self-oscillating techniques have been used and proposed extensively along the years, like in [Pinheiro et al., 1999; Sira-ramírez and Silva-Ortigoza, 2002; Bonache-Samaniego, 2017].

#### State-plane techniques

The state-plane representation of a resonant converter can give useful insights into the behavior [Oruganti and Lee, 1985a]. In state-plane control approaches, the dynamics can be simpler, streamlining the design of controllers, which can show improved regulation performance and a more immediate hardware realization. Moreover, using state-plane approaches allows us to forget about the time dependence when applying the control since it is implicitly embedded in the two states. Stateplane-based approaches have been proposed, where the input switching is derived from current and voltage measurements in the converter. The ones that turn to self-oscillating schemes have been proposed, either ensuring the oscillations regardless of the load condition [Pinheiro et al., 1999; Youssef et al., 2006], or proposing state-plane-induced input selection [Bonache-Samaniego et al., 2016; Bonache-Samaniego et al., 2017].

#### 1.1.4 Resonant converters for battery chargers

Most of the control techniques in the literature that ensure the oscillating behavior of the tank have been previously introduced in Section 1.1.3. These techniques can be combined with another control loop for the regulation of a desired quantity, in general the output current for battery chargers. For the battery charging application, the most common resonant topology is the LLC, which allows boost operation. Several works have their focus on the circuit/components design and a few of them tackle the control problem in a clear way. The simplest control technique that we can implement is a PI controller in combination with a Voltage-Controlled Oscillator (VCO), so that the converter is operating with frequency modulation behavior. Some recent works that use this technique are: [Qin et al., 2022] that proposes a higher order resonant tank that induces better properties than standard LLC; [Cittanti et al., 2022] where the LLC is used for fast charging and the control is done with two cascade control loops; [Saadati et al., 2022] that proposes a novel analog controller design procedure for LLC resonant converters for battery charging. Then, there are other techniques similar to the one that we are going to propose. In [Youssef et al., 2006] they combine self-sustained oscillations with phase-shift modulation. Their objective is to reduce the frequency range while maintaining ZVS. The controller is composed of two loops: the inner one adjusts the phase-shift to ensure ZVS, and the outer one adjusts the output voltage. Differently from us, they follow a time-domain approach: they look at the time domain waveforms and act on the angles and the switching frequency. Instead, our control is based on the state-plane where time does not matter directly. More recent works are [Bojarski et al., 2014; Bojarski et al., 2015; Bojarski et al., 2016] which propose a so called "phasefrequency control" for the wireless battery charging case (the topology is similar to the On-Board Charger (OBC) for Electric Vehicle (EV) batteries). Essentially, the control tries to keep the frequency near the resonant one while maintaining ZVS, the output being regulated by changing the phaseshift. More in detail, [Bojarski et al., 2014] discusses a multiphase resonant inverter for wireless power transfer; [Bojarski et al., 2015] proposes a multi-level topology with 12 switches; and [Bojarski et al., 2016] presents a 25 kW prototype of wireless EV charger where the control is implemented in an FPGA. In [Peter and Mathew, 2021], a three-level single stage LLC converter is proposed. The control scheme is dual: frequency modulation is used to regulate the output voltage and PWM is used to control the DC-bus voltage. A complete and complex analysis of the design and modeling for an LLC resonant converter for electric vehicle battery charging is given in [Deng et al., 2014]. The worst-case operating point is identified and used for the design with the aim to globally ensure ZVS. First Harmonic Approximation (FHA) is used in above-resonance region, while for the belowresonance region a specific mode analysis is employed.

When proposing new techniques for resonant converters, there are two main approaches: change the *control technique* of the full-/half- bridge configuration, or change the *topology* of the converter, potentially providing a richer behavior with more degrees of freedom. With this philosophy, in [Liu et al., 2017] a three-phase three-level converter is presented. The improvement stands in the fact that switches are subject to half the input voltage and the ripple at the output is reduced due to the

3-phase signals. In [Ta et al., 2020], a new slightly different topology that keeps the LLC properties is proposed, allowing different modes of operation by having a full-bridge configuration for the switches and a transformer with a central point. ZVS is guaranteed in all modes. In [Li et al., 2020], a bidirectional LLC charger is proposed. The topology is similar to a dual-active-bridge since the rectification is active. In [Li et al., 2023], a slightly different topology is presented. The resonant tank is on the secondary side of the transformer and the resonant elements' connection is different. The resonant tank has a T shape and the battery is modeled as a resistor (its value is determined by the charging curve). The converter can behave either as an LCL or an LC tank, depending on the charging mode, constant-current (CC) and constant-voltage (CV) respectively. In [Wu et al., 2023] different topologies for high-frequency ac-dc converters are discussed. They include Dual Active Bridge (DAB) and resonant LLC.

In this manuscript, for the battery charger application we propose two control loops: an inner one that enables a self-oscillating behavior while ensuring ZVS, similar to [Youssef et al., 2006]; and an outer loop consisting in a PI controller for output current regulation. Therefore, our contribution is in a novel control technique rather than a topology change.

#### 1.1.5 Basic modeling



Figure 1.4: Simple scheme of a resonant converter with the symbols.

For the rest of the manuscript, the general scheme in Figure 1.4 is considered as reference for what we are going to discuss. The switch network (an H-bridge in our case) is supplied by an external DC supply  $V_g > 0$ , and it can deliver either positive ( $v_s = +V_g$ ), negative ( $v_s = -V_g$ ), or zero ( $v_s = 0$ ) voltage to the resonant tank. The output voltage  $v_s$  is modeled by a discrete variable  $\sigma$  that represents the configuration of the switch network so that  $v_s = \sigma V_g$  with  $\sigma \in \{-1, 0, 1\}$ . The load of the resonant tank can be generic, in what we are going to consider it is going to be either a resistor or something whose behavior can be approximated by a resistor, thanks to the first order approximation. For the modeling, any variation of  $\sigma$  is considered instantaneous as we consider it to be a purely discrete state, so that  $\dot{\sigma} = 0$ .

#### 1.2 Second-order topologies

The two possible second-order topologies are the series and the parallel ones. The difference in the circuit stands in the capacitor location: either in series or in parallel with the load. The Series Resonant Converter (SRC) delivers a voltage below the first harmonic of  $v_s$  – it is a buck converter. The Parallel Resonant Converter (PRC) can deliver a voltage above the first harmonic of  $v_s$  – it is typically used as a boost converter.

#### 1.2.1 Dynamical equations

For the series configuration (Figure 1.5a), from the Kirchhoff's laws, the following equations hold

$$\sigma V_g - L \frac{\mathrm{d}i_s}{\mathrm{d}t} - v_C - Ri_s = 0, \quad i_s = i_C.$$
(1.1)



Figure 1.5: Second order topologies.

Similarly, the linear equations governing the parallel configuration (Figure 1.5b) correspond to

$$\sigma V_g - L \frac{\mathrm{d}i_s}{\mathrm{d}t} - v_C = 0, \quad i_s = i_C + \frac{v_C}{R}.$$
 (1.2)

Knowing that the relationship of current and voltage on the capacitor is  $i_C = C \frac{dv_C}{dt}$ , both circuit dynamics can be expressed in terms of the voltage  $v_C$  through a second order differential equation:

SRC: 
$$\frac{\mathrm{d}^2 v_C}{\mathrm{d}t^2} + \frac{R}{L} \frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{1}{LC} v_C = \frac{V_g}{LC} \sigma \tag{1.3}$$

PRC: 
$$\frac{\mathrm{d}^2 v_C}{\mathrm{d}t^2} + \frac{1}{RC} \frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{1}{LC} v_C = \frac{V_g}{LC} \sigma \tag{1.4}$$

We can notice that the equations are similar, the only difference stands in the factor in front of the voltage derivative, which is related to the dissipation.

**Normalized coordinates.** Now, we want to express (1.3), (1.4) in normalized coordinates. To this end, the following quantities are introduced:

$$\omega_0:=\frac{1}{\sqrt{LC}},\quad Z_0:=\sqrt{\frac{L}{C}},\quad \beta_{\mathrm{PRC}}:=\frac{1}{RC},\quad \beta_{\mathrm{SRC}}:=\frac{R}{L};$$

with  $\omega_0$  the natural frequency,  $Z_0$  the characteristic impedance, and  $\beta$  the damping factor – different for the two linear circuits. We define the new set of dimensionless coordinates  $(x_1, x_2)$  where the voltage is scaled by  $1/V_g$  and the current by  $Z_0/V_g$ :

$$x_1 := \frac{1}{V_g} v_C, \qquad x_2 := \frac{Z_0}{V_g} i_C.$$
 (1.5)

Therefore, we can express (1.3) and (1.4) as

$$\ddot{x}_1 + \beta \dot{x}_1 + \omega_0^2 x_1 = \omega_0^2 \sigma, \tag{1.6}$$

with the relationship between  $v_C$  and  $i_C$  becoming  $\dot{x}_1 = \omega_0 x_2$ . The corresponding state-space representation is

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & -\beta \end{bmatrix}}_{A} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ \omega_0 \end{bmatrix}}_{B} \sigma, \qquad (1.7)$$

whose compact reads as  $\dot{x} = Ax + B\sigma$ . In this form, we can clearly recognize the structure of a harmonic oscillator with the resonant frequency  $\omega_0$  in the off diagonal elements (nondissipative part), and the damping factor  $\beta$  in the diagonal (dissipative part). Remarkably, we have the same differential equation (1.6) describing both the SRC and the PRC.

**Input-dependent normalized coordinates.** We can go a bit further and introduce the  $(z_1, z_2)$  set of coordinates where the input  $\sigma$  is included within the state  $z_1$ :

$$z_1 := x_1 - \sigma = \frac{1}{V_g} v_C - \sigma, \qquad z_2 := x_2 = \frac{Z_0}{V_g} i_C.$$
 (1.8)

As we will see later, this is useful since we can express the dynamics (1.7) as an autonomous system

$$\begin{bmatrix} \dot{z}_1\\ \dot{z}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \omega_0\\ -\omega_0 & -\beta \end{bmatrix}}_{A} \begin{bmatrix} z_1\\ z_2 \end{bmatrix}.$$
(1.9)

**Remark 1.2** In the following we will reason either in the  $(x_1, x_2)$  or  $(z_1, z_2)$  coordinates, while "forgetting" about the physical quantity of current and voltage. Here stands the power of having unified the description of second-order resonant converters, since we can reason in these new coordinates and then retrieve the results either for the SRC or the PRC, without losing information. Moreover, we will see that sometimes it is more intuitive to describe the control laws in the x-coordinates. While, for the mathematical proofs, the z-coordinates simplify the analysis.

#### Quality factor

At this stage, we introduce the concept of quality factor Q, which is a measure of the dissipation in a system. From [Erickson and Maksimović, 2020], a general definition – for a sinusoidal excitation of a passive element or network – is

$$Q := 2\pi \frac{(\text{peak stored energy})}{(\text{energy dissipated per cycle})}.$$

For a second-order system, as the case of SRC and PRC described by the dynamical equation (1.6), the explicit expression for the quality factor is

$$Q = \frac{\omega_0}{\beta}.\tag{1.10}$$

To make a connection with frequency domain analysis, let us consider the prototypical second-order transfer function

$$\frac{\omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2},$$

where  $\xi$  is the *damping ratio* and the scalar  $2\xi\omega_0$  has been previously denoted as  $\beta$ . From standard second-order systems analysis, we can identify three cases:

- $\xi > 1$ : overdamped system;
- $\xi = 1$ : critically damped system;
- $\xi < 1$ : underdamped;
- $\xi = 0$ : undamped.

In this work, we focus one the case with  $\xi < 1$ , which implies that the step response is characterized by an oscillating behavior before reaching the steady-state value. From (1.10), condition  $\xi < 1$ is equivalent to  $Q > \frac{1}{2}$ , which is the condition to ensure self-oscillating behavior in second-order resonant converters as we will see later. An informal way to express this concept is *"How likely is the oscillation in a system?"*, in other words *"Does the system have a natural oscillatory behavior?"*. The bigger Q (i.e., the smaller  $\xi$ ), the more pronounced are the oscillation. From a practical perspective, if the resonant tank is excited by a step input and  $Q > \frac{1}{2}$ , it is going to stabilize to the equilibrium point while oscillating, which can be observed in the state-plane as a spiraling trajectory around the equilibrium point, the origin.

#### Matrix Exponential

The solution to the autonomous dynamics (1.9) can be obtained as

$$z(t) = e^{At} z(0),$$

where  $e^{At}$  is the matrix exponential of matrix A, which has the following expression

$$e^{At} = e^{-\frac{\beta}{2}t} \begin{bmatrix} \cos\left(\frac{\Delta}{2}t\right) + \frac{\beta}{\Delta}\sin\left(\frac{\Delta}{2}t\right) & \frac{2\omega_0}{\Delta}\sin\left(\frac{\Delta}{2}t\right) \\ & & \\ -\frac{2\omega_0}{\Delta}\sin\left(\frac{\Delta}{2}t\right) & \cos\left(\frac{\Delta}{2}t\right) - \frac{\beta}{\Delta}\sin\left(\frac{\Delta}{2}t\right) \end{bmatrix},$$
(1.11)

where  $\Delta^2 = \omega_0^2 - 4\beta^2 > 0$  under the assumption that  $Q > \frac{1}{2}$ . The matrix exponential (1.11) shows us that with the underdamped assumption  $Q > \frac{1}{2}$ , the states  $z_1$  and  $z_2$  are oscillating (sine and cosine functions) with an exponential decay factor  $-\frac{\beta}{2}$ .

#### Polar coordinates

Let us consider the following change of coordinates

$$z_1 = \rho \cos \phi, \qquad z_2 = \rho \sin \phi. \tag{1.12}$$

In polar coordinates  $(\rho, \phi)$ , dynamics (1.9) reads as

$$\dot{\rho} = -\beta\rho\sin^2\phi, \qquad \dot{\phi} = -\omega_0\left(1 + \frac{\beta}{2\omega}\sin(2\phi)\right),$$
(1.13)

where we can see that the decay factor  $\beta$  control the decay rate of  $\rho$ , i.e., how fast is the trajectory approaching the origin.

#### 1.2.2 Transfer functions

From the analysis and design point of view, the use of Transfer Functions (TFs) is useful. As a convention, we will refer to the Laplace transform of a variable with the corresponding capital letters when possible: e.g.  $V_C(s) := \mathcal{L}\{v_C(t)\}$ . We are interested in the input ( $\sigma$ ) to output (voltage or current on the load) characteristic. In particular, we can notice that the voltage and current on the capacitor are linked to the output for both converters: in the SRC,  $i_C$  corresponds to the output current; in the PRC,  $v_C$  corresponds to the output voltage. Then, output voltage and current are proportional since we considered that the load is resistive. Therefore, we can focus on the TFs between  $v_s$  and  $i_C$ ,  $v_C$ . For the capacitor voltage we have

$$H_{v_C}(s) := \frac{V_C(s)}{V_s(s)} = \frac{\omega_0^2}{s^2 + \beta s + \omega_0^2},$$
(1.14)

while for the capacitor current we have

$$H_{i_C}(s) := \frac{I_C(s)}{V_s(s)} = \frac{1}{Z_0} \frac{\omega_0 s}{s^2 + \beta s + \omega_0^2}.$$
(1.15)

Notice that at the resonant frequency  $\omega_0$  the gain for the voltage  $|H_{v_C}(j\omega_0)| = Q$  corresponds to the quality factor Q, and the gain for the current corresponds to  $|H_{i_C}(j\omega_0)| = \frac{Q}{Z_0}$ . In particular, the input to output voltage gain at the resonant frequency is unitary for the SRC, and Q for the PRC.

To remain in a dimensionless framework, we can express the TFs for  $x_1$  and  $x_2$ , which are directly related to (1.14) and (1.15). In particular

$$H_{x_1}(s) := \frac{X_1(s)}{\Sigma(s)} = \frac{\omega_0^2}{s^2 + \beta s + \omega_0^2},$$
(1.16)

$$H_{x_2}(s) := \frac{X_2(s)}{\Sigma(s)} = \frac{\omega_0 s}{s^2 + \beta s + \omega_0^2},$$
(1.17)



Figure 1.6: Bode plots for the transfer functions (1.16) and (1.17) for various values of Q in (1.10).

where  $\Sigma(s) := \mathcal{L}{\sigma(t)}$ . The Bode plots are depicted in Figure 1.6 for different values of the quality factor. Let us remark that, by normalizing the frequency  $\omega$ , the quality factor Q (i.e. the damping ratio) is enough to describe the behavior in the frequency domain. For example, the peak amplitude of the magnitude for both TFs corresponds to the quality factor, and the peak width is related to Q.

## 1.3 Third-order LLC

We switch our focus to the third-order topologies, in particular the to LLC one. Let us mention that there is also the LCC topology as shown in Figure 1.2, but we focus only on the LLC since it is the one employed in the battery charger application that is going to be considered in Chapter 5. To make a link with the second-order topologies, the LLC corresponds to an SRC with an inductor in parallel with the output (the load). The corresponding circuit is shown in Figure 1.7.



Figure 1.7: Electrical circuit of the LLC resonant converter.

#### 1.3.1 Dynamical Equations

For the LLC, from the Kirchhoff's laws, we can write the following equations:

$$v_s = L \frac{\mathrm{d}i_s}{\mathrm{d}t} + v_C + v_o, \quad i_s = i_o + i_{L_m}, \quad v_o = L_m \frac{\mathrm{d}i_{L_m}}{\mathrm{d}t};$$

from which we can derive the following system of linear differential equations

$$\begin{cases} \frac{\mathrm{d}i_s}{\mathrm{d}t} = \frac{1}{L}(v_s - v_C - v_o),\\ \frac{\mathrm{d}v_C}{\mathrm{d}t} = \frac{1}{C}i_s,\\ \frac{\mathrm{d}i_{L_m}}{\mathrm{d}t} = \frac{1}{L_m}v_o. \end{cases}$$
(1.18)

Now, let us consider a change of coordinates similar to (1.5)

$$x_1 := \frac{v_C}{V_g}, \qquad x_2 := \frac{Z_0}{V_g} i_s, \qquad x_3 := \frac{v_o}{V_g},$$
 (1.19)

with the following parameter definitions

$$\omega_0 := \frac{1}{\sqrt{LC}}, \qquad \beta := \frac{R}{L}, \qquad Z_0 := \sqrt{\frac{L}{C}}, \qquad Q := \frac{\omega_0}{\beta}, \qquad l := \frac{L}{L_m}. \tag{1.20}$$

For the LLC behavior an important parameter is the ratio between the inductances L and  $L_m$ , which gives a measure of the influence of the magnetizing inductance  $L_m$  on the dynamics: the higher  $L_m$ , the closer the LLC behaves to the SRC (l = 0 corresponds to the SRC case). Let us remark that the quality factor definition is inherited by the SRC, but it does not reflect the definition in Section 1.2. Therefore, the meaning is not the same, and we can observe this from the fact that there is similar behavior for low and high Q (Figure 1.8). Using (1.19), (1.20), and knowing that  $v_o = Ri_o = R(i_s - i_{L_m})$ , dynamics (1.18) can be written in the following state-space form

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & \omega_0 & 0 \\ -\omega_0 & 0 & -\omega_0 \\ -\beta & 0 & -\beta(1+l) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_0 \\ \beta \end{bmatrix} \sigma.$$
(1.21)

For the LLC, two characteristic frequencies can be identified, one related to the open-circuit behavior  $(R \rightarrow \infty)$ , and one related to the short-circuit behavior (R = 0). For the short-circuit case, the frequency corresponds to  $\omega_0$  as in the SRC, while in the open-circuit case the frequency is

$$\omega_1 := \frac{1}{\sqrt{(L+L_m)C}} = \omega_0 \sqrt{\frac{l}{l+1}}.$$
(1.22)

Let us remark a difference from the SRC. LLC and SRC have the same behavior for short-circuit conditions, while it is different for open-circuit conditions. Let us reason in a case with very high-load, which corresponds to low quality factor (Q < 0.5): in the SRC there are no oscillations since they are overdamped; in the LLC this corresponds to underdamped conditions with the resonant frequency being determined by  $L + L_m$  and not only L. Therefore, in an LLC converter, the quality factor does not indicate low or high load as it does in an SRC, where the quality factor determines whether oscillating behavior occurs. Instead, in an LLC converter, the quality factor provides information about the peak location of the TF, as shown in Figure 1.8.

#### 1.3.2 Transfer functions

Considering the circuit in Figure 1.7, the impedance of the resonant tank is given by

$$Z_{tank} := sL + \frac{1}{sC} + \frac{sL_mR}{sL_m + R} = L \frac{s^3 + \beta(1+l)s^2 + \omega_0^2 s + l\beta\omega_0^2}{s(s+l\beta)},$$
(1.23)

which can tell us when the tank has an inductive or capacitive behavior. The TFs between the input  $\sigma$  and normalized states are:

$$H_{x_1}(s) = \frac{\omega_0^2(s+l\beta)}{s^3 + \beta(1+l)s^2 + \omega_0^2 s + l\beta\omega_0^2},$$
(1.24)

$$H_{x_2}(s) = \frac{s\omega_0(s+l\beta)}{s^3 + \beta(1+l)s^2 + \omega_0^2 s + l\beta\omega_0^2},$$
(1.25)

$$H_{x_3}(s) = \frac{s^2 \beta}{s^3 + \beta (1+l)s^2 + \omega_0^2 s + l\beta \omega_0^2}.$$
(1.26)

Using normalized coordinates lets us abstract from the values of the real components and do a more generic analysis. The TFs are represented in Figure 1.8 for different value of Q and l in (1.20). We can see that with small l we can recognize the two characteristic frequencies, while they tend to overlap with higher l. The effect of Q is in the peak prominence and location.



Figure 1.8: Transfer functions for the LLC converter. The vertical dotted lines correspond to  $\omega_1/\omega_0$ .

# 1.4 Final consideration

In this chapter we have seen the basics about resonant power converters. In particular, we provided a modeling framework mostly for second-order topologies, which is going to be used in Chapters 3 and 4 to develop some control laws that ensure the self-oscillating behavior in the resonant converter. Nevertheless, from a practical point of view, we are more interested in the LLC topology, which can be found in different applications. This is why we described the third-order LLC, which is going to be used in Chapter 5 to construct the framework for the analysis of a dc-dc resonant converter.

# 2

# **Background material**

#### 2.1 Hybrid dynamical systems

Hybrid dynamical systems are a class of dynamical systems that present both the characteristics of continuous-time and discrete-time dynamical systems. Continuous-time dynamical systems are represented by differential equations or inclusions, whose solutions are parameterized by continuous (also called ordinary) time  $t \in \mathbb{R}_{\geq 0}$ . Discrete-time dynamical systems are represented by difference equations or inclusions, whose solutions are parameterized by an integer number  $k \in \mathbb{N}$ . A good reference for the theoretical analysis of hybrid dynamical systems is the book [Goebel et al., 2012].

Several examples fit the hybrid formulation, one may even argue that most real systems are characterized by a hybrid behavior. Some examples are: digitally-controlled mechanical systems, electronic circuits with digital logic as power converters, event-triggered systems, and systems with impacts among many others. If we consider the example of power converters, the dynamical state involves both physical quantities (e.g. voltages, currents) taking values in the reals, and logical quantities (e.g. position of switches) taking values in the integers. Other times, a same state variable may present both continuous and discrete behavior, like in the classical bouncing ball example where the speed of the ball has an instantaneous change at the impact.

In the setting of differential and difference equations, a hybrid dynamical system can be formally written as

$$\mathcal{H}\begin{cases} \dot{x} = f(x), & x \in \mathcal{C}, \\ x^+ = g(x), & x \in \mathcal{D}. \end{cases}$$
(2.1)

The solutions of (2.1) can evolve according to continuous dynamics  $\dot{x} = f(x)$  while in set C or to discrete dynamics  $x^+ = g(x)$  while in set D. We refer to the data of H as follows: C is the flow set and f the flow map while D is the jump set and g the jump map. Furthermore, the description could be even more generalized using differential and difference inclusions where f and g become set-valued maps.

For a hybrid dynamical system, we can give a proper description for solutions  $\phi$ . An important feature of hybrid solution is that classical solutions to continuous-time and discrete-time systems are special cases of the hybrid solution concept, whenever the set C or D is the empty, i.e., when the system has purely discrete or purely continuous dynamics, respectively. Each hybrid solution  $\phi$  is characterized by its own time domain dom  $\phi$  constructed to match the jumping and flowing properties of that solution, depending on its evolution. Since hybrid solutions evolve both in continuous-time t and in discrete-time k, solutions exist on a *hybrid time domain* parameterized by  $(t, k) \in \mathbb{R}_{\geq 0} \times \mathbb{N}$ .

#### 2.1.1 Hybrid dynamics of powers converters

To provide rigorous guarantees, a full nonlinear dynamics perspective on these on-off type of feedbacks requires the use of a hybrid dynamical systems formalism: an area where powerful stability
analysis tools, such as the Lyapunov approach, have been developed in [Goebel et al., 2012]. Power converters naturally call for a hybrid description due to the discrete behavior of the switches, while the dynamics when the switches' positions are fixed is described by a continuous behavior through differential equations. Hybrid dynamical systems theory can be seen as extension of specific theories; for instance, power converters can be described by switched affine systems, a particular case of hybrid dynamical systems. Switched affine systems are characterized by having a switching rule that selects, at each time instant, a dynamic subsystem from a set of available ones [Liberzon, 2003]. Consider an example with power converter: each subsystem is defined by a different combination of on-off switches and the role of the control law is to select the proper configuration, i.e., subsystem, at the right moment [Deaecto et al., 2010]. Formally, the linear case formulation is as follows

$$\dot{x} = A_q x + B_q u, \quad q = 1, \dots, n,$$

where q is the index of a specific subsystem and the control law acts on q, e.g,  $q^+ = h(x, u, q)$ . Thus, switched affine systems are frequently encountered in the literature when discussing power converters. However, the use of hybrid dynamical systems theory enables stronger tools for stability and robustness analysis, as well as control design techniques. Several relevant power electronics challenges have been addressed using hybrid dynamical systems tools, such as hybrid control of inverters in [Chai and Sanfelice, 2014; Torquati et al., 2017] and dc-dc converters in [Theunisse et al., 2015; Sanchez et al., 2019; Sferlazza et al., 2020a; Sferlazza et al., 2020b]. The advantage offered by hybrid dynamical systems is the possibility to consider several aspects of power converters that are generally relegated to robustness assumptions or simplifications. For example, limit the switching frequency is an important aspect, and this can be easily considered through a dwell-time condition [Sanchez et al., 2019], which can be translated to a timer in a hybrid dynamical system (e.g.  $\dot{\tau} = 1$  and  $\tau^+ = 0$ ). On the other side, the practical implementation of these type of control laws is not always straightforward and could present some difficulties. Nonetheless, the approaches cited so far for dc-dc converters are not applicable to resonant conversion, where the switching frequency does not correspond to a small ripple, but to the main AC component of the power transfer. Moreover, in the considered case of self-sustained oscillations, there is no external reference for the sinusoidal signals as in [Chai and Sanfelice, 2014]. Therefore, the stabilization in our case is not done with respect to a given reference, but with respect to unknown internal operating conditions.

#### 2.1.2 Hybrid dynamical systems for resonant converters

In the following chapters, we will often refer to the state-plane. To be rigorous, keep in mind that this is a projection on it, since the hybrid system includes (at least) also the state  $\sigma$ .

#### Hybrid setting

In general, the hybrid dynamical system for a resonant converter is as follows

$$\begin{cases} \dot{x} = f(x,\sigma) \\ \dot{\sigma} = 0 \end{cases}, \quad (x,\sigma) \in \mathcal{C}, \qquad \begin{cases} x^+ = g(x,\sigma) \\ \sigma^+ = h(x,\sigma) \end{cases}, \quad (x,\sigma) \in \mathcal{D}. \end{cases}$$
(2.2)

Where  $f(x, \sigma)$  incorporates the dynamics of the resonant tank, for example corresponding either to (1.7) or to (1.9). While, the discrete part amounts for the update law that we have at each switch. Essentially, function *h* is in charge of ensuring the appropriate sequence of values for  $\sigma$ . The function  $g(x, \sigma)$  depends on the definition of the coordinates *x*, while  $h(x, \sigma)$  describes the update law – i.e., the sequence – for the input  $\sigma$ . At this point, the core of the work stands in the design of:

- the jump set D, i.e., when the switching occurs;
- the update function  $h(x, \sigma)$ , i.e., what is the sequence of values for  $\sigma$ .

In general, the sets C and D are suitable subsets of  $\mathbb{R}^n \times \{-1, 0, 1\}$  to be designed, where n is the order of the converter. Their intuitive meaning is that whenever  $(x, \sigma)$  belongs to D, it is time to change the switch position in the H-bridge driving the converter, whereas as long as  $(x, \sigma) \in C$ , one may let the converter evolve continuously without changing the switch position. As a consequence, the selection of C and D implicitly defines a feedback controller because it characterizes under what conditions the switches should be toggled (or left unchanged).

**Remark 2.1** In the following chapters, the flow and jump sets are going to be selected as closed sets, and the flow and jump maps are continuous functions. Therefore, the hybrid system  $\mathcal{H} = (\mathcal{C}, f, \mathcal{D}, g)$  enjoys the so-called hybrid basic conditions of [Goebel et al., 2012, Assumption 6.5]. This, among other things, implies robustness of asymptotic stability of compact attractors, as characterized in [Goebel et al., 2012, Chapter 7]. A consequence of robustness is that one expects a graceful degradation of the closed-loop stability properties (the so-called semiglobal practical robustness): an important feature for the experimental results.

Since in this manuscript period trajectories, e.g., oscillations, are considered, it is useful to recall the concept of periodicity for a hybrid trajectory. According to [Bisoffi et al., 2018], and alternatively in [Lou et al., 2018], the notion of periodicity for a hybrid trajectory is reported below, which is a straightforward extension of the usual notion of periodicity.

**Definition 2.1** Given a hybrid system, a nontrivial hybrid periodic trajectory  $\zeta$  is a complete solution (namely, a solution that evolves forever) that is not identically zero and for which there exists a pair  $(T, J) \in \mathbb{R}_{\geq 0} \times \mathbb{Z}_{\geq 0}$  satisfying T + J > 0, such that  $(t, j) \in \text{dom}(\zeta)$  implies  $(t + T, j + J) \in \text{dom}(\zeta)$  and, moreover,

$$\zeta(t,j) = \zeta(t+T,j+J). \tag{2.3}$$

*The image of*  $\zeta$  *is a nontrivial* hybrid periodic orbit.

Analysis and stabilization of hybrid period trajectories is a known problem. Several works have considered it in different fields: gene network [Lou et al., 2018], spiking systems [Izhikevich, 2003], bipedal walking [Grizzle et al., 2001], mass spring systems [Bisoffi et al., 2018], and in general impulsive systems. For planar systems, the Poincaré–Bendixson theorem is usually employed to show properties about limit cycles. We find an extension of the classical Poincaré–Bendixson theorem to the planar hybrid case in [Simic et al., 2002]. On the same line, [Grizzle et al., 2001] analyses biped robots, which are characterized by impact and the walking behavior can be modeled as a periodic behavior. [Wendel and Ames, 2010] shows that the properties of the Poincaré maps for hybrid systems are different compared to the one of smooth systems. Nevertheless, many of these works consider some specific case and do not provide a general theory. Recently, [Lou et al., 2018] considers robust stability in systems characterized by multiple jumps, and [Lou et al., 2023] discusses stability, existence and robustness of limit cycles in hybrid dynamical systems with only one jump per period.

#### Conditions for self-oscillation in second-order resonant converters

In Chapters 3 and 4, we consider the following assumption on second-order resonant converters dynamics (1.7) and (1.9), which is necessary in showing that there exists a nontrivial hybrid periodic trajectory.

**Assumption 2.2** For dynamics (1.7) and (1.9), the relation  $2\omega_0 > \beta > 0$  is satisfied, namely the resonant tank is underdamped. Equivalently: the roots of  $s^2 + \beta s + \omega_0^2 = 0$  are complex conjugate, or the quality factor in (1.10) satisfies  $Q > \frac{1}{2}$ .

The intuition behind Assumption 2.2 is that it is reasonable to ask for a natural oscillatory behavior in a system where we want closed-loop oscillations that arise spontaneously. A practical way to see this condition is: if the system is excited with nonzero initial conditions and/or constant input, it reaches the equilibrium point while having an oscillatory behavior (typical of second-order systems with damping ratio less than one).

**Remark 2.3** Assumption 2.2 imposes constraints on the physical components to ensure that a natural oscillatory motion occurs. For the two circuit configurations of Figure 1.5, the constraint  $\beta < 2\omega_0$  corresponds to:

$$SRC: R < 2\sqrt{\frac{L}{C}} = 2Z_0; \qquad PRC: R > \frac{1}{2}\sqrt{\frac{L}{C}} = \frac{1}{2}Z_0.$$
 (2.4)

These requirements are reasonable since the effect of the load R must be sufficiently small to not destroy the natural oscillatory behavior of the LC resonant network. Ideally one would want,  $R \to \infty$  (open circuit) for the PRC and  $R \to 0$  (short circuit) for the SRC.

### 2.2 Soft switching

When designing a power converter, efficiency is an important aspect to consider. Therefore, we are interested in reducing the losses, which can be identified in two main categories: conduction losses and switching losses.

**Conduction losses** are related to the reactive power in the circuit. Namely, if there is a shift in phase between the input current and voltage it means that there is a circulating current in the circuit which is not providing actual power to the load. Hence, this unnecessary circulating current generates Joule losses in the circuit and in the switches (ON resistance).

**Switching losses** are related to the switches used in the circuit, e.g.: MOSFET, BJT, IGBT, SRC, and GTO, among others. There is a loss when the current and voltage across the switch during the switching instant are not zero. Usually, during the turn-on and turn-off phases, there is a transition moment when the current increases and voltage decreases or vice versa. A solution to this problem, known as *soft switching*, is to switch when the current or voltage across the component is zero. Namely, we can have Zero-Current Switching (ZCS) or Zero-Voltage Switching (ZVS).

Having a soft switching behavior allows reducing the Electromagnetic Interference (EMI), which are disturbances that can interfere with the normal operation of the system or of the surroundings electronics. ZVS is a way to reduce EMI linked to the parasitic capacitors of the device. As we will see, when the switches are commuting without ZVS there is the emergence of high-frequency ringing, which is generated by the rapid charge/discharge of the capacitors of the semiconductor device [Chen et al., 2010].

The bigger picture is that typical resonant converters employ "majority carrier" devices, such as MOSFETs, GaN or SiC FETs [Erickson and Maksimović, 2020, Chapter 4]. The majority carrier devices cause power loss every time they are switched ON with some charge stored in the drain-tosource capacitance  $C_{ds}$ , represented in Figure 2.1. The higher the input voltage of the converter (and battery charger may work with 400 V, 800 V) the higher the charge in  $C_{ds}$ , hence the loss. In ZVS, we discharge  $C_{ds}$  before turning on the device, so that voltage  $v_{ds}$  is reduced. When  $v_{ds}$  is zero, i.e., when the anti-parallel diode conducts, the transistor is turned ON.



Figure 2.1: Equivalent representation of the MOSFET with the body diode and terminal capacitors.

#### 2.2.1 Zero-Voltage Switching

Zero-Voltage Switching (ZVS) is specific for the turn-on of majority carrier devices, like MOSFETs. The idea behind ZVS is to turn-on the device when the voltage across it is zero, in order to limit the switching losses. This condition is not straightforward, usually the voltage across a OFF switch is non-zero, for example in a full-bridge configuration it corresponds to the input voltage  $V_g$ . In practice, the voltage across a switch is equal to the voltage across the parasitic capacitor  $C_{ds}$  between the drain and the source, as shown in Figure 2.1. In order to obtain ZVS, the capacitor should be discharged before turning on the switch. The capacitor is discharged when the freewheeling diode, which can be the body diode or a dedicated diode device, starts to conduct. Hence, the best moment to turn-on a majority carrier switch is when its antiparallel diode (e.g., the body diode) starts to conduct. The higher the flowing current the faster the capacitor is discharged.

We can take advantage of ZVS when the load is dominated by the inductive component since the current lags the voltage. Otherwise, we would not be able to ensure it. This usually corresponds to the case of a resonant converter working at a frequency higher than the resonant one. The important parameter that regulates the ZVS behavior is the dead-time, which allows for a period where the following switch is not turned-on so that the flowing current can discharge the parasitic capacitance.



Figure 2.2: Representation of the stages in a full-bridge acting in ZVS condition.

**ZVS on two-level full-bridge.** On a full-bridge configuration, in order to provide two output levels  $v_s = \{-V_g, V_g\}$ , the switches are activated in pairs, M1 with M4 and M2 with M3. Let us consider the case when we want to switch from positive to negative voltage. Figure 2.2 shows the principle functioning stages. The switch sequence is the following:

- (i) M1 and M4 are ON providing positive output voltage  $v_s = V_g$ .
- (ii) M1 and M4 are turned OFF, and the current continues to flow through C2 and C3 discharging them during a period corresponding to the dead-time.
- (iii) M2 and M3 are turned ON in ZVS conditions reducing the losses, and  $v_s$  is negative.
- (iv) M2 and M3 are turned OFF, and the current continues to flow through C1 and C4.

The duration by which the capacitors are discharging is determined by the dead-time. Therefore, the dead-time should be chosen long enough to ensure the discharge of the parasitic capacitors, but not too long to reverse current. The effects of the dead-time can be appreciated in Figure 2.3, where we can see that for a dead-time of 100 ns the ringing is clearly visible. If we increase the dead-time, we



Figure 2.3: Oscilloscope screenshots that show the dependency of ZVS with the dead-time in a twolevel full-bridge. On the top of each screenshot we can observe the output voltage  $v_s$  (square) and current  $i_s$  (pseudo-sinusoidal) of the H-bridge; on the bottom there are the voltage drain-to-source ( $v_{ds}$ ) of MOSFETs M3 and M4.

can observe how the ringing amplitude is reduced until becoming negligible for a 600 ns dead-time. In Figure 2.3d, we can observe clearly the effect of the dead-time as the fact that the voltage  $v_s$  is initially decreasing linearly, due to the discharge of the parasitic capacitors.

**ZVS on three-level full-bridge**. On a full-bridge configuration, in order to provide three output levels  $v_s = \{-V_g, 0, V_g\}$ , the switches are activated in a specific sequence. The operating stages of a full-bridge with MOSFETs for half-cycle are represented in Figure 2.4. The switches sequence is the following:

- (i) M1 and M4 are conducting providing positive output voltage  $v_s = V_g$ .
- (ii) M1 is turned OFF and, to ensure the current flow, C3 starts to discharge during the dead-time.
- (iii) M3 is turned ON to allow bidirectional flow of the current<sup>1</sup>,  $v_s = 0$ .
- (iv) M4 is turned OFF and C2 starts to discharge. After this phase, the current changes direction.
- (v) M2 is turned ON before the zero-crossing of the current,  $v_s = -V_g$ .

<sup>&</sup>lt;sup>1</sup>If the flowing current will be only positive, it is not necessary to turn-on M3, although this increase losses since a diode is worse than a MOSFET.



Figure 2.4: Representation of the stages of a half-cycle in a full-bridge with intermediate stage where  $v_s = 0$ .

Then, the sequence continues similarly to complete a cycle. We cannot obtain ZVS when in stage (iii) the current changes direction. If this is the case, D2 won't start to conduct and therefore M2 will be turned ON without ZVS. This is the case of the phase-modulation control law, described in Chapter 4, where the switch from zero to  $-V_g$  happens with negative current. The effect of the current level at the switching instant can be observed in the oscilloscope screenshots in Figure 2.5. With higher current the ringing is lower.

#### 2.2.2 Zero-Current Switching (ZCS)

The Zero-Current Switching (ZCS) happens when a device changes its state while the current flowing through it is zero. ZCS is typical for minority carrier devices as diodes and IGBTs. In our case are the diodes of the rectifier that might benefit from ZCS. This is typical of converter working in Discontinuous Conduction Mode (DCM)<sup>2</sup>. In our case, we have the output current of the transformer that is going to zero, which implies that the diodes do not deal with reverse recovery current and they do turn on and off with zero current. This behavior usually occurs when the switching frequency is lower than the resonant one. An example of the waveforms involved in ZCS is shown in Figure 2.6.

# 2.3 Final considerations

In this chapter, we have reviewed some concepts related to hybrid dynamical systems as applied to resonant converters. These concepts will be useful in Chapters 3 and 4 and in Section 5.1, where the hybrid formalism is used to describe the dynamics and the control laws embedded in the jump set definitions. Secondly, we have revisited the concept of soft-switching, with particular attention to ZVS. We will see that ZVS is a desired property for a resonant converter, which we will enforce through the control laws when possible. Nevertheless, at the beginning it might be not straight forward to understand when there is ZVS from theoretical analysis or simulation, while it is really intuitive and direct to deduce it from experimental results, as shown in Figure 2.3, due to the presence of the ringing.

<sup>&</sup>lt;sup>2</sup>DCM is identified by the fact that the inductor current remains at zero for a portion of the switching time.



Figure 2.5: Oscilloscope screenshots that show the dependency of ZVS on the current level and sign at the switching instants. On the top of each screenshot we can observe the output voltage  $v_s$  (square) and current  $i_s$  (pseudo-sinusoidal) of the H-bridge; on the bottom there are the voltage drain-to-source ( $v_{ds}$ ) of MOSFETs M3 and M4.



(a) Case with output current equal to 1 A.

(b) Case with output current equal to 5 A.

Figure 2.6: Oscilloscope screenshots display the waveforms involved when there is ZCS in the rectifier. The waveforms at the top are the input current  $i_s$  and voltage  $v_s$ . At the bottom, the magenta waveform is the input current of the rectifier  $i_T$ , where we can observe that  $i_T$  remains at zero for an interval of time, during which ZCS occurs.

# 3

# **Frequency modulation**

This chapter contains the main contribution about the control of series and parallel converters with frequency modulation techniques. The idea is to cast different (known and novel) control techniques on the state-plane. In this direction, with the work presented in [Zaupa et al., 2021; Zaupa et al., 2023a], we propose a different approach with respect to [Bonache-Samaniego, 2017]. The strong contribution is to prove the stability for second-order tanks with Q > 0.5. Moreover, PRC and SRC topologies are studied with the same normalized coordinates allowing us to study a single system, whose results can then be read in terms of the series or parallel topology.

For the frequency modulation control, the objective is to modulate the output by changing the frequency of the input  $\sigma$ , without modulating its amplitude (the one of the first harmonic). Therefore, the input voltage is constrained to be either positive or negative:  $\sigma \in \{-1, 1\}$ . From this simple consideration, we can already state that the update law for  $\sigma$  will be:  $\sigma^+ = -\sigma$ ; since we want to enforce a toggling sequence. Therefore, the problem boils down to designing the jump set in the state-plane. The jump set is modeled as two half-lines, symmetric with respect to each other's in the state-plane. The symmetry comes from the fact that the input voltage should have an average value of zero. Otherwise, this would correspond to having a constant bias supplying the resonant tank, which is usually not desired. Finally, Theorem 3.3 provides the proof of stability for the hybrid periodic orbit and the control law is shown to be effective on an experimental SRC prototype.

The proposed frequency modulation control law is formulated in *z*-coordinates. This allows us to exploit some properties of the autonomous dynamic (1.9) in the stability proof. Moreover, we compare the proposed control law with a similar one formulated in the *x*-coordinates. Let us remark that we will express the results of the simulation always in terms of the state *x* since it is proportional to the current and voltage in the circuit, i.e., it has a direct physical meaning.

Let us remark that, in this chapter, the control has the objective to ensure the oscillations, while having some desired properties. The output regulation problem will not be considered as the interest is on the qualitative behavior of the oscillations, i.e. we fix the parameter of the control law, and we look at the output properties. The only used feedback is the one to locate the trajectory in the stateplane to enable the modulation control laws.

#### 3.1 Hybrid dynamics definition

This control law has been initially proposed in [Zaupa et al., 2021], then extended in [Zaupa et al., 2023a] with the stability proof and the experimental results. Essentially, the jump set corresponds to a line passing through the origin in the state-plane  $(z_1, z_2)$ . The idea is inspired by the work done in [Bonache-Samaniego et al., 2017], where a similar control law is proposed in the state-plane  $(x_1, x_2)$ .

The sets C and D are designed based on a reference input  $\theta \in (0, \pi]$  capable of inducing different output amplitudes and frequencies in the self-oscillating behavior. Using (1.8) and (1.9), the

dynamics equations in the z-coordinates are

$$\begin{bmatrix} \dot{z}_1\\ \dot{z}_2\\ \dot{\sigma} \end{bmatrix} = f_{\theta}(z,\sigma) := \begin{bmatrix} \omega_0 z_2\\ \omega_0 z_1 - \beta z_2\\ 0 \end{bmatrix} \qquad (z,\sigma) \in \mathcal{C}(\theta), \qquad (3.1a)$$

$$\begin{bmatrix} z_1^+\\ z_2^+\\ z_2^+\\ \sigma^+ \end{bmatrix} = g_{\theta}(z,\sigma) := \begin{bmatrix} z_1 + 2\sigma\\ z_2\\ \sigma \end{bmatrix} \qquad (z,\sigma) \in \mathcal{D}(\theta). \qquad (3.1b)$$

We select the jump and flow sets as:

$$\mathcal{C}(\theta) := \mathcal{C}_1(\theta) \cup \mathcal{C}_{-1}(\theta), \qquad \mathcal{D}(\theta) := \mathcal{D}_1(\theta) \cup \mathcal{D}_{-1}(\theta), \qquad (3.2a)$$

where each set  $C_1$  and  $C_{-1}$  denotes a half-plane and  $D_1$  and  $D_{-1}$  are two half-lines delimiting C

$$\mathcal{C}_q(\theta) := \{ (z, \sigma) : \ \sigma = q, \sigma(z_1 \sin \theta + z_2 \cos \theta) \le 0 \}, \tag{3.2b}$$

$$\mathcal{D}_q(\theta) := \{ (z, \sigma) : \sigma = q, \sigma z_2 \ge 0, z_1 \sin \theta + z_2 \cos \theta = 0 \},$$
(3.2c)

for each  $q \in \{1, -1\}$ . These sets are depicted in Figure 3.1 for a constant value of  $\theta$ .



Figure 3.1: Projections of the flow and jump sets for the frequency modulation case and for a fixed  $\theta$ . Intuitively, other values of  $\theta$  correspond to rotated version of these sets.

Remark 3.1 An equivalent control law that enforces the same behavior as (3.1), (3.2) is

$$\sigma = -\operatorname{sign}\left(z_1\sin\theta + z_2\cos\theta\right). \tag{3.3}$$

But, control law (3.3) alone is not robust with respect to noise. In (3.1), (3.2), once a solution has jumped, it needs to wait to reach the other jump set, which is "far". Instead, with update law (3.3),  $\sigma$  could change rapidly between 1 and -1 due to the noise, inducing an unwanted irregular behavior, because no hysteresis mechanism is implemented.

A possible closed-loop solution induced by (3.2) is illustrated in Figure 3.1, where it evolves in the three-dimensional state-space  $(z_1, z_2, \sigma)$ . During flows (in  $C(\theta)$ ), the continuous evolution revolves in the clockwise direction. Switching always occurs when the continuous motion hits the tilted solid line, because from that line solutions cannot flow in  $C(\theta)$ , unless the state  $\sigma$  is toggled. When a switch occurs, the state variable  $z_1$  is shifted horizontally by two units (see (3.1b)), and the specific choice of  $C(\theta)$  and  $\mathcal{D}(\theta)$  ensures that those shifts always map to the interior of  $C(\theta)$ , from where flowing



Figure 3.2: Comparison of the state-plane representations for the frequency modulation control laws in the z and x coordinates.

should occur. The choice to split  $\mathcal{D}$  in two half lines regularizes the domain avoiding Zeno solutions with  $\theta = \pi$ . The angle  $\theta$  controls the tilting of the solid line, namely the subspace where the switch takes place. It is apparent that with small values of  $\theta$  solutions flow only in a small portion of the state-plane while for larger values of  $\theta$  flowing is allowed in a larger range of phases, up to the limit case  $\theta = \pi$ , where the solution spans all the possible phases while flowing.

**Remark 3.2** The control law proposed in [Bonache-Samaniego, 2017] has the same idea with the difference that the jump set (3.2c) (switching line) is defined in the x-plane, inducing the same self-oscillating behavior but with different properties. To identify the differences, let us consider Figure 3.2. In the left, with the jump set described by (3.2c) in the z-plane, the trajectory jumps every time it hits the switching line. In the right, with the jump set defined in the x-plane, the jump does not influence the  $(x_1, x_2)$  states (i.e.,  $x_1^+ = x_1$  and  $x_2^+ = x_2$ ). Another difference is the way the line is defined, in our case the line is described by the angle  $\theta$ , while in [Bonache-Samaniego et al., 2017] the line is described by its slope k or equivalently by the angle  $\alpha$ 

$$\sigma = \operatorname{sign}(x_2 - kx_1) = \operatorname{sign}(-x_1 \sin \alpha + x_2 \cos \alpha). \tag{3.4}$$

In the following we are also using  $\theta$  for (3.4) as follows

$$\sigma = \operatorname{sign}(x_1 \sin \theta + x_2 \cos \theta), \tag{3.5}$$

where we can observe that the only difference with (3.3) is the coordinates that are used to define the switching line. Both control approaches lead to a self-oscillating behavior where the output frequency depends on the slope of the line. In the x-plane, the control law has the remarkable property that the slope is approximately directly related to the phase-shift between the input current and the input voltage, i.e., to the frequency. As said, the input-output relationship is not the same, in the z-plane the amplitude tends to zero as  $\theta \to 0$ , while in the x-plane the amplitudes tends to zero as  $\theta \to \frac{\pi}{2}$ , which is a singularity for [Bonache-Samaniego et al., 2017] since  $k \to \infty$ .

The main difference with respect to [Bonache-Samaniego, 2017] is on the conditions under which we can ensure the existence of a limit cycle. Our constraint on the quality factor from Assumption 2.2, namely  $Q > \frac{1}{2}$ , shows the advantage of the proposed switching law, as compared to the alternative solutions of [Bonache-Samaniego, 2017]. Indeed, a nontrivial discussion is present in [Bonache-Samaniego et al., 2016] showing for the PRC case that with Q < 3.15 there is no guarantee of a self-oscillating behavior (the controller in [Bonache-Samaniego et al., 2016] may reach an equilibrium). Whereas, we are able to guarantee that there exists a limit cycle for all the cases with a quality factor greater than  $\frac{1}{2}$ .



Figure 3.3: Simulation results of the frequency-modulation control law (3.2). At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes normalized by Q.



Figure 3.4: Simulation results of the frequency-modulation control law (3.5). At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes normalized by Q. The control parameter k from (3.4) is substituted by  $\theta = \pi - \arctan(k)$  in this case as in (3.5).

#### 3.2 Input-output characteristic

The most important part of a control law is the relationship between the control parameter and the quantities in the system. In this case, we are interested in the relationship between  $\theta$  and the frequency and amplitude of the state x (even if we presented the system in the z-coordinates, x is directly related to the physical quantities, hence it is more informative for us from a practical point of view). The first factor of impact on the amplitude of states  $x_1$  and  $x_2$  is the quality factor Q, as can be understood by the transfer functions in Figure 1.6. Therefore, the amplitudes of  $x_1$  and  $x_2$  are scaled by Q in order to highlight the effect of Q on the shape of the function.

Figure 3.3 shows at the left that the frequency drastically increases in order to ensure low amplitudes, which is known and expected since the frequency increase is one of the major drawbacks in frequency modulation techniques, i.e., the necessity of a large frequency range in order to modulate the amplitude from zero to the maximum. The scaled amplitudes of states  $x_1$  and  $x_2$  reported at the right of Figure 3.3 show that the relationship between  $\theta$  and the amplitude is nonlinear, and it is highly influenced by the quality factor.

On the other side, if we consider the results in Figure 3.4 – obtained by simulating the control law (3.5) in [Bonache-Samaniego, 2017] – we can see at the left that the frequency always tends to increase, but the range is limited compared to the control law (3.2) in the *z*-plane. In Figure 3.3 the frequency goes up to 6 times the resonant one, while in Figure 3.4 it goes up to 3.2 times. Moreover, the relationship  $\theta$ -frequency is heavily influenced by the quality factor in Figure 3.4, while the effect of the quality factor on the curves of the amplitude is lower (right of Figure 3.4) compared to control (3.2) in Figure 3.3. Let us remark that for (3.2) the angle is limited in the range ( $\frac{\pi}{2}$ ,  $\pi$ ].

# 3.3 Stability result

In this section, we state the stability result for the control law in the *z*-plane (3.1), (3.2) for any value of the input control parameter  $\theta$ , and we provide a proof for it.

**Theorem 3.3** Under Assumption 2.2, for each selection of  $\theta \in (0, \pi]$ , the closed loop (3.1), (3.2) has a unique nontrivial hybrid periodic orbit  $\mathcal{O}_{\theta}$  that is stable and almost globally attractive (its basin of attraction includes all points such that  $z \neq 0$ ). Moreover, the nontrivial hybrid periodic trajectories of (3.1), (3.2) are characterized by J = 2 and  $T(\theta) > 0$ , and exhibit periodic jumps interlaced by flowing intervals of length  $T(\theta)/2$ .

#### 3.3.1 Hybrid Lyapunov function and proof of Theorem 3.3

In this section we provide the proof to Theorem 3.3, based on hybrid Lyapunov theory [Goebel et al., 2012]. Our proof shares interesting similarities with the approach reported in [Bisoffi et al., 2016] (see also [Bisoffi et al., 2018]), which addresses relay-based control of mechanical systems.

Before proving Theorem 3.3, let us recall from Definition A.2 that a function  $\psi : \mathbb{R} \to \mathbb{R}$  is  $\alpha$ -strongly convex if and only if there exists  $\alpha > 0$  such that for each  $a, b \in \mathbb{R}$  it holds that

$$\psi(a) - \psi(b) \ge \sigma(a-b) + \frac{\alpha}{2}|a-b|^2, \ \forall \sigma \in \partial \psi(b),$$
(3.6)

where  $\partial \psi(b) \subset \mathbb{R}$  is the subdifferential of  $\psi$  at *b*. Based on (3.6) we use the following lemma, which is instrumental for the proof of Theorem 3.3. Proof of Lemma 3.4 in given in Appendix A.1.

**Lemma 3.4** Consider two continuous functions of the scalar variable  $\xi \in \mathbb{R}_{\geq 0}$ , a linear function  $\xi \mapsto \psi_1(\xi) = \psi_0 + \gamma \xi$ , with  $\psi_0, \gamma \in \mathbb{R}$ , and a strongly convex function  $\psi_2$  with  $\psi_2(0) < \psi_0$ . Function  $\xi \mapsto \psi_2(\xi) - \psi_1(\xi)$  grows unbounded as  $\xi \to +\infty$  and has exactly one zero for  $\xi \geq 0$ .

For proving Theorem 3.3, we formulate the following corollary of [Bisoffi et al., 2018, Lemma 1], relating the dissipated energy along a flowing solution of (3.1), (3.2) to the hatched area in Figure 3.5 (right). The proof of Lemma 3.5 is given in Appendix A.2.

**Lemma 3.5** Consider any solution z from (1.9) flowing between two points from ordinary time  $t_1$  to ordinary time  $t_2 > t_1$  and define the energy-like function  $E(z) = \frac{1}{2}z_1^2 + \frac{1}{2}z_2^2 = \frac{1}{2}|z|^2$ . The dissipated energy  $E(z(t_2)) - E(z(t_1))$  is equal to  $\frac{\beta}{\omega_0}\Pi(z)$ , where  $\Pi(z)$  is the (unsigned) area hatched between the graph of the trajectory z(t),  $t \in [t_1, t_2]$  and the coordinate axis  $z_2 = 0$ .

To construct a Lyapunov function proving Theorem 3.3, let us only consider the half-space  $C_1$ , which also contains  $\mathcal{D}_1$  (parallel definitions apply to  $C_{-1}$ ) and introduce the set

$$\mathcal{G}_{1} := \{ z \in \mathcal{C}_{1} : z_{2} \leq 0, (z_{1}+2) \sin \theta + z_{2} \cos \theta = 0 \} \cup \{ z \in \mathcal{C}_{1} : z_{1} \in [-2, 0], z_{2} = 0 \},$$

$$(3.7)$$



Figure 3.5: Evolution of solutions and sets  $G_1$  (in green) and  $D_1$  (in red) discussed in the proof of Theorem 3.3.

which corresponds to the green-colored half line parallel to  $\mathcal{D}_{-1}$  in Figure 3.5. Then, for each point  $z \in \mathcal{C}_1 \setminus \{0\}$ , denote the compact time interval associated with the unique backward and forward flowing solutions of (3.1), flowing in  $\mathcal{C}_1$ , as

$$\mathcal{T}_1(z) := \{ \tau \in \mathbb{R} : e^{As} z \in \mathcal{C}_1, \ \forall s \in [\tau, 0] \cup [0, \tau] \},$$

$$(3.8)$$

where  $e^{As}$  is the matrix exponential of (1.11), and  $[t_2, t_1]$  should be understood as the empty set when  $t_2 > t_1$ , so that  $[\tau, 0] \cup [0, \tau]$  always describes an interval containing zero, whether  $\tau$  is positive or negative. Clearly,  $0 \in \mathcal{T}_1(z)$  for all  $z \in \mathcal{C}_1 \setminus \{0\}$ . Based on  $\mathcal{T}_1(z)$ , define the following two times, which exist and are unique for each  $z \in \mathcal{C}_1 \setminus \{0\}$  due to the revolving nature of solutions, as per Assumption 2.2:

$$\tau_G(z) := \{ \tau \in \mathcal{T}_1(z) : e^{A\tau} z \in \mathcal{G}_1 \},$$
(3.9)

$$\tau_D(z) := \{ \tau \in \mathcal{T}_1(z) : e^{A\tau} z \in \mathcal{D}_1 \}.$$
(3.10)

The Lyapunov function proposed in this proof, which is represented in Figure 3.6 for the special case  $\theta = 3\pi/4$ , is based on (3.9), (3.10) and corresponds to

$$V(z) := \max\{\tau_G(z), 0\} + \frac{\left(\delta_V(z) - \frac{\beta}{\omega_0}\Pi(z)\right)^2}{([1\ 0\ ]e^{A\tau_G(z)}z)^2},$$
(3.11)

$$\delta_V(z) := 2\left(1 + \sigma \left[1 \ 0\right] e^{A\tau_D(z)} z\right),\tag{3.12}$$

where  $\Pi(z)$  is the (unsigned) area hatched between the graph of the trajectory z(t),  $t \in [t_1, t_2]$  and the coordinate axis  $z_2 = 0$  (as defined in Lemma 3.5).

The first term of V(z) in (3.11) is positive when z lies in the stripe between the set  $\mathcal{D}_{-1}$  and  $\mathcal{G}_1$ of Figure 3.5, wherein  $\tau_G(z) > 0$ , but it is zero in the remaining points of  $\mathcal{C}_1$ , wherein  $\tau_G(z) \leq 0$ . The second term of V(z) is inspired by [Bisoffi et al., 2016]. Referring to the energy E defined in Lemma 3.5, its numerator corresponds to the difference between the dissipated energy  $\frac{\beta}{\omega_0} \Pi(z)$ (sampled in a Poincaré fashion) along the flow from  $\mathcal{G}_1$  to  $\mathcal{D}_1$  with the increase of energy across the jump from  $z_{1,D} = [1 \ 0] e^{A\tau_D(z)} z$ , which belongs to  $\mathcal{D}_1$ , namely

$$\delta_V(z) = \frac{1}{2} \left( (z_{1,D}^+)^2 - z_{1,D}^2 \right) = 2 \left( 1 + \sigma z_{1,D} \right), \tag{3.13}$$

as defined in (3.12). Note that by construction  $\Pi$  and  $\delta_V$  are constant along flowing solutions, therefore, whenever  $\tau_G(z) \leq 0$ , V remains constant along flowing solutions. Comparing  $\delta_V(z)$  with  $\frac{\beta}{\omega_0}\Pi(z)$ , an energy balance between flows and jumps emerges when  $\delta_V(z) - \frac{\beta}{\omega_0}\Pi(z) = 0$ , that is when V(z) = 0. The denominator of the right term in (3.11) simply ensures that, close to the origin, V blows up to infinity, as it should because the origin is a weak equilibrium (it admits a constant flowing solution not converging to the hybrid periodic orbit) and cannot belong to the basin of attraction.

Defining V(z) in a parallel way for  $z \in \mathcal{C}_{-1}$ , we prove below the zero level set of V

$$\mathcal{A} := \{ (z, \sigma) : \delta_V(z) = \frac{\beta}{\omega_0} \Pi(z), \text{ and } \tau_G(z) \le 0 \},$$
(3.14)

with  $\delta_V$  defined in (3.12), corresponds to the set  $\mathcal{O}_{\theta}$  characterized in Theorem 3.3. We are now ready to prove Theorem 3.3.

**Proof of Theorem 3.3.** Let us first characterize function  $\Pi$ , which is constant by construction along flowing solutions. Due to this fact we can parametrize all values of  $\Pi(z)$ ,  $z \in C \cup D$ , following a Poincaré approach for each  $z \in D_1$ , via  $\Pi(z) = \psi_2(|z|)$ , where  $\psi_2(|z|)$  is the sum of the upper area  $\psi_2^{up}(|z|) = \alpha^{up}|z|^2$ , which is homogeneous of degree two by construction, and the lower area  $\psi_2^{lw}(|z|) = \alpha^{lw} \max\{|z| - |z_0|, 0\}^2$ , with  $z_0 \in D$  being the unique point such that  $e^{A\tau_G(z_0)}z_0 = \begin{bmatrix} -2\\ 0 \end{bmatrix}$ , namely the point where  $\mathcal{G}_1$  has a kink, in Figure 3.5. Due to homogeneity of the linear solutions (larger solutions are scaled versions of the smallest ones), it is immediate to see that  $\psi_2^{lw}(|z|)$  is (nonstrictly) convex and  $\psi_2^{up}(|z|)$  is strongly convex. Therefore, their sum is strongly convex. Let us continue by observing that for each  $z \in D_1$ , we can express the injected energy as

$$\psi_1(|z|) := |z^+|^2 - |z|^2 = 2(1 - |z|\cos\theta) = \delta_V(z).$$
(3.15)

Then, from Lemma 3.4, there exists only one positive value  $\xi^* = |z^*|$  of |z| leading to the energy balance  $\psi_2(|z^*|) = \psi_1(|z^*|)$ . In particular, the hybrid periodic orbit  $\mathcal{O}_{\theta}$  corresponds to the image of the hybrid periodic trajectory starting at the unique point  $z^* \in \mathcal{D}_1$ . By uniqueness of  $z^*$ , the nontrivial hybrid periodic orbit  $\mathcal{O}_{\theta}$  is unique and coincides with set  $\mathcal{A}$  in (3.14).

Let us now prove the asymptotic stability of  $\mathcal{A}$  with basin of attraction  $\mathcal{B}_{\mathcal{A}} = (\mathbb{R}^2 \setminus \{0\}) \times \{-1, 1\}$ . To this end, let us first note that V is zero in  $\mathcal{A}$ , positive in  $\mathcal{B}_{\mathcal{A}}$  and, from Lemma 3.4, radially unbounded, relative to the open set  $\mathcal{B}_{\mathcal{A}}$ , with respect to  $\mathcal{A}$ . Moreover, since the points  $e^{A\tau_D(z)}z$ and  $e^{A\tau_G(z)}z$  remain constant along flowing solutions and  $\tau_G(z)$  is a decreasing function of time (due to the revolving nature of the solutions stemming from Assumption 2.2), then V in (3.11) is nonincreasing when flowing in  $\mathcal{C}$ . Finally, from Lemma 3.4, and using similar arguments to those of [Bisoffi et al., 2016, Lemma 2], the Lyapunov function decreases across jumps. More specifically,



Figure 3.6: Logarithmic representation of the Lyapunov function V in (3.11), for the value  $\theta = \frac{3}{4}\pi$ .

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the following weak Lyapunov properties hold

$$\begin{split} \dot{V} &:= \langle \nabla V(z), f(z,\sigma) \rangle \leq 0, \ \forall (z,\sigma) \in \mathcal{C} \setminus (\{0\} \times \{-1,1\}), \\ \Delta V &:= V(g(z,\sigma)) - V(z) < 0, \ \forall (z,\sigma) \in \mathcal{D} \setminus \mathcal{A}. \end{split}$$

As in [Bisoffi et al., 2016], the asymptotic stability of  $\mathcal{A}$  with basin of attraction  $\mathcal{B}_{\mathcal{A}}$  then follows from the nonsmooth hybrid invariance principle of [Seuret et al., 2019, Theorem 1].

The proof is completed by noting that, except for the trivial flowing solution at zero, the hybrid limit cycle, whose orbit is  $\mathcal{A}$ , is globally attractive, and therefore it is the only possible one. Moreover, due to the symmetry of the flow/jump sets and maps, this cycle is associated with periodic jumps, where the period  $T(\theta)$  of the jumps is given by the time it takes for a solution to reach  $\mathcal{D}_1$  from  $\mathcal{G}_1$ , along the periodic orbit. The period of the limit cycle is  $(2T(\theta), 2)$  because, by construction, it takes two half revolutions for the periodic trajectory starting from  $\mathcal{G}_1$  to revisit the same point in  $\mathcal{G}_1$ .  $\Box$ 

#### 3.4 Experimental validation

An experimental prototype of an SRC is developed to validate our modulation control law (3.2). First we discuss how the control law embedded in the jump set (3.2c) can be cast in a digital controller. Eventually, we are briefly considering the design of the prototype, and we end by showing the comparison between experimental and simulation results.

#### 3.4.1 Controller Implementation

This section discusses the practical implementation of the hybrid switching law, which has been verified with high fidelity simulations in PSIM software.

Implementing the hybrid feedback requires making a decision about whether a switch should be performed or not, based on the jump/flow sets. An analog-based solution could check the flow/jump conditions in the continuous time domain, as in [Sferlazza et al., 2020b], such that there is no information loss, at the expense of a relatively complex tuning and a rigid design reuse. On the other hand, a digital alternative would facilitate complex calculations and reprogramming capability, at the expense of some information loss due to the Analog-to-Digital Converters (ADCs) and the presence of a time-delay in the control loop. Information loss in digitally controlled power converters is caused by the digital PWM and the quantization error of the ADC, which may generate undesired oscillations [Peterchev and Sanders, 2003]. In turn, time-delay negative effects can be mitigated by performing the sampling/conversion process at a fast sampling rate, up to more than 30 times the switching frequency [Costabeber et al., 2008]. In this work, the hybrid control is digitally implemented because the two above-mentioned drawbacks are minimized. Namely, no numerically-induced oscillations emerge because the control strategy does not require a PWM element, and no undesirable delay effects emerge because of the low latency of the Field-Programmable Gate Array (FPGA) and the high sampling frequency of the ADCs.

This last statement is confirmed by the simulation results reported in Figure 3.7, where a delay in the order of 2% (200 ns) of the half period (10 µs) is acceptable and does not affect significantly the closed-loop response. Figure 3.7 reports simulation results for trajectories in the phase-plane ( $z_1$ ,  $z_2$ ) when a delay is introduced in the acquisition chain, namely this delay can account for: acquisition time, latency, internal ADC timing. Our discussed theoretical framework actually justifies these robustness features in a rigorous way, thanks to the properties discussed in Remark 2.1. The results of Figure 3.7 confirm that the asymptotic stability is preserved despite the introduction of these perturbations in the feedback loop.

For the measurements of the state  $z = (z_1, z_2)$ , needed by the feedback controller, it is enough to measure a scaled version of the current and the voltage on the capacitor,.

The core task of the controller is evaluating the jump condition, to decide whether to switch or not. The introduced jump set formulation (3.2c) requires checking zero crossing conditions that can



Figure 3.7: Comparison between the simulated response with an analog implementation (top-left) with the sampled-data implementation, with different delays  $t_D$  and using a constant switching angle  $\theta = 3\pi/4$ .

be conveniently extended to a half plane. Moreover, in order to cope with the disturbances arising at the switching instant (which could generate multiple consecutive jumps), time regularization is introduced, which inhibits jumps for  $t_R$  seconds, so that the trajectory moves away from the jump set border. We can model this behavior by introducing a timer variable  $\lambda > 0$  that is reset to 0 at every jump and linearly increases during flow. Then a jump is allowed only if  $\lambda \ge t_R$ . The dynamics for  $\lambda$ , which can be added to (3.1), is

$$\dot{\lambda} = 1$$
  $(z, \sigma, \lambda) \in \mathcal{C}_{\mathbf{R}}(\theta),$  (3.16a)

$$\lambda^{+} = 0 \qquad (z, \sigma, \lambda) \in \mathcal{D}_{\mathbf{R}}(\theta), \qquad (3.16b)$$

where the time-regularized flow/jump sets are  $C_{R}(\theta) = C(\theta) \cup \mathbb{R}_{\geq 0}$  and  $\mathcal{D}_{R}(\theta) = \mathcal{D}(\theta) \cup [t_{R}, +\infty)$ .

A graphical representation of the time-regularized sets is reported in Figure 3.8, where the gray area represents the area spanned by the solution while jumps are inhibited. The angular aperture can be approximated as  $\omega_0 t_{\rm R}$ . As long as  $t_{\rm R}$  is sufficiently small, the results of Theorem 3.3 also apply with the regularized sets.



Figure 3.8: Representation of the jump sets. The theoretical formulation (left) and the experimental one (right) corresponding to half-plane with time regularization. The shaded areas show the effects of time regularization.



Figure 3.9: Schematic of the electronics involved in the SRC prototype including: H-bridge, resonant tank, sensing, controller and drivers.

#### 3.4.2 Prototype design

An experimental prototype of an SRC has been developed with target parameters:  $f_0 = \frac{\omega_0}{2\pi} = 50 \text{ kHz}$ ,  $V_g = 24 \text{ V}$ , and operating power of 100 W. The prototype schematic is shown in Figure 3.9 and the physical realization in Figure 3.10, the list of components is given in Table 3.1. Frequency is limited to reduce the effect of the sampling-induced delay, even though also industrial prototypes work in this range up to a few hundreds of kHz.

The power stage consists of an H-bridge and a resonant tank. The H-bridge comprises two MOS-FET power modules (APTC60AM242G) driven by the driver IR2110. The resonant tank employs a multi-layer ceramic (X7R) 100 nF capacitor and a 94.3 µH inductor. The sensing is performed with a Hall-effect sensor (CQ-3200) for the current measurements and a differential operational amplifier (NCS2007) for the voltage measurements. Both sensing stages have a low-pass filter to reduce the noise, additionally the current sensing has a high-pass filter to remove the DC component introduced by the current sensor, which would hinder the operation of the ADC stage.

The controller is implemented in the Stratix IV GX (EP4SGX230KF40C2) FPGA, part of the DE4 board from Terasic extended with the daughter board (AD/DA Data Conversion Card) equipped with the AD9254 ADCs operating at 100 Msps. The high sampling frequency reduces the delay to a negligible value estimated in 200 ns, which is in accordance with the simulation results of Figure 3.7.

The converter has been tested with two different loads:  $10.1 \Omega$  and  $22 \Omega$ , corresponding to quality factors of Q = 3 and Q = 1.4, respectively.

#### 3.4.3 Experimental results

The steady-state input-output waveforms are reported in Figure 3.11, showing a desirable output oscillation for various values of  $\theta$ , thus confirming the result of Theorem 3.3. Figure 3.12 illustrates several simulation (top row) and experimental (bottom row) responses, represented in the ( $z_1$ ,  $z_2$ ) phase-plane. In the phase-plane representations, the dotted horizontal segments (yellow and purple) represent the jumps in the trajectories.

Additionally, the converter behavior has been experimentally characterized with respect to the input signal  $\theta$ . Figure 3.13 reports the experimental results compared with the simulation for the



Figure 3.10: Picture of the SRC experimental prototype.

two loads. The results show a good match for large values of  $\theta$ , near the resonance. This is expected because this type of converter typically operates around that region. Figure 3.13 reports the peak of the normalized voltage and the current measured on the capacitor  $x_1$  and  $x_2$ , respectively, which have a more meaningful physical interpretation. The reported resonant frequencies  $\hat{\omega}_0$  are evaluated based on a characterization of the inductance value of the prototype's resonant tank for the two different load conditions,  $R = 10.1 \Omega$  and  $R = 21.8 \Omega$ . The different values are due to the nonlinear effects of frequency, current and circuit layout on the value of the inductance.

The experiments show good matching with the simulation results for large values of  $\theta$ , while the discrepancy increases as  $\theta$  decreases. Experiments with small  $\theta$  have not been performed due to the high frequency shown by the converter, which makes the self-oscillation harder to sustain with this controller. Moreover, for small values of  $\theta$ , the acquired amplitudes were too low with respect to the ADCs input range. These issues reduced the set of angles tested in the prototype, but practically this is not problematic since the converter is supposed to work not far from the resonant frequency.

# 3.5 Final considerations

In this chapter, we have seen how a frequency modulation control law can be described with hybrid dynamical systems. We have proposed a slightly different formulation by changing the coordinates with respect to the work in [Bonache-Samaniego, 2017], whose results have been reported, too. In both cases, by operating above the resonant frequency, we are able to ensure ZVS for all the commutations. On the other hand, to ensure a wide range of output amplitudes, the resulting frequency range is large. We have provided formal guarantees for stability and attractivity of the limit cycle for every input parameter  $\theta$  in the range  $(0, \pi]$  if the underdamped condition  $Q > \frac{1}{2}$  is satisfied. The proposed frequency modulation control law (3.2) has been validated in an experimental prototype of a second-order series resonant convert. In Chapter 6, we will see how the same control law works also for a third-order LLC resonant converter prototype.



Figure 3.11: States  $\sigma$  (red) and  $x_2$  (light blue) from the SRC experimental prototype with  $R = 10.1 \Omega$ , for values of  $\theta$  shown in Figure 3.12.



Figure 3.12: Phase portraits in the  $(z_1, z_2)$  coordinates with different values of  $\theta$ . Simulation results (top row) and experimental results (bottom row). The  $\theta$ -tilted dotted violet line represents the jumps set. The load used is  $R = 10.1 \Omega$ .



Figure 3.13: Comparison between the experiments and the simulations for the frequency modulation control law (3.2) with  $R = 10.1 \Omega$  at the left and  $R = 21.8 \Omega$  at the right. The frequencies are rescaled by the estimated resonant frequency  $\hat{\omega}_0 = 2\pi \hat{f}_0$ :  $\hat{f}_0 = 50 \text{ kHz}$  for  $R = 10.1 \Omega$  and  $\hat{f}_0 = 45.8 \text{ kHz}$  for  $R = 21.8 \Omega$ .

Parameter	Component	Value
$V_{ m g}$	_	$24\mathrm{V}$
$C_{ m in}$	X7R	$1\mu\mathrm{F}$
$M_{1-2}$	APTC60AM242G	_
L	AGP4233	$100\mu H$
C	X7R	$100\mathrm{nF}$
$C_{ m LPF}$	poly	$10\mathrm{nF}$
$C_{\mathrm{HPF}}$	poly	$100\mathrm{nF}$
$R_{ m LPF}$	trough-hole resistor	$50\Omega$
$R_{ m HPF}$	trough-hole resistor	$1\mathrm{k}\Omega$
$R_1$	trough-hole resistor	$270\mathrm{k}\Omega$
$R_2$	trough-hole resistor	$1.2\mathrm{k}\Omega$
Driver	IR2110	_
OPAMP	NCS2007	_
Current Sensor	CQ-3200	_
ADC	AD9254	_
FPGA	EP4SGX230KF40C2	_

Table 3.1: SRC prototype parameters.

# 4

# Phase-shift modulation

This chapter contains the main contribution about the control of series and parallel converters with phase-shift modulation published in [Zaupa et al., 2023b]. This technique is the complementary direction of frequency modulation where we look at the hybrid dynamical systems formulation and the representation in the state-plane. The proposed modulation law relies on a simplified framework allowing to analyze some properties and prove the stability with a different technique.

Given the limitations of using wide frequency ranges in resonant conversion like for the frequency modulation in Chapter 3, the objective of this section is to propose a hybrid controller that allows modulating the amplitude of the first harmonic of the input  $\sigma$  while keeping the frequency constant. In a way, the hybrid controller produces a *self-oscillating phase-shift modulation* behavior. In this setting,  $\sigma$  can take values in  $\{-1, 0, 1\}$ . The zero level allows operating at the resonant frequency of the tank across a range of output amplitudes by modulating the amplitude of the first harmonic, i.e., by changing the time when  $\sigma = 0$ . The hybrid dynamical system that embeds the control law is presented, Theorem 4.2 provides the proof of stability for the hybrid periodic orbit and the control law is shown to be effective on an experimental SRC prototype.

Let us remark that, in this chapter, the control has the objective to ensure the oscillations, while having some desired properties. The output regulation problem will not be considered as the interest is on the qualitative behavior of the oscillations, i.e. we fix the parameter(s) of the control law, and we look at the output properties. The only used feedback is the one to locate the trajectory in the state-plane to enable the modulation control laws.

# 4.1 Hybrid dynamics definition

The phase-shift modulation extends the possibility to apply a zero input voltage,  $\sigma = 0$ . While this extra value does not change coordinates (1.8) nor their continuous dynamics (1.9) (equivalently (1.5) nor (1.7), respectively), it radically changes the switching possibilities, which are here described by a hybrid model enforcing a precise periodic sequence for  $\sigma$ : 1, 0, -1, 0, ... (in practice  $\sigma$  is a three-level square waveform):



Figure 4.1: Jump sets (solid lines) and flow sets (sectors) for each selection of ( $\sigma$ , d). A sample trajectory is represented in black. Coordinate  $\lambda$  will be introduced and used in the proof.

In our new model (4.1),  $\xi := (z_1, z_2, \sigma, d)$  collects the four states: two physical and two logical ones. The new logical state  $d \in \{-1, 1\}$  plays an important role when  $\sigma = 0$  as it stores the past value of  $\sigma$ , so that the next value will be assigned as the opposite one (i.e. -d), in order to generate the correct switching pattern. Clearly, any variation of  $\sigma$  and d must be instantaneous, so that  $\dot{\sigma} = 0$  and  $\dot{d} = 0$ . Another way to see the extra state d is as part of a state machine where the state is identified by  $(\sigma, d)$ . The angle  $\varphi \in [0, \frac{\pi}{2})$  is a reference input affecting the steady-state output voltage (minimum for  $\varphi = \frac{\pi}{2}$  and maximum for  $\varphi = 0$ ). Based on  $\varphi$ , we select the jump and flow sets as

$$\begin{aligned}
\mathcal{C}(\varphi) &:= \mathcal{C}_1(\varphi) \cup \mathcal{C}_{10}(\varphi) \cup \mathcal{C}_{-1}(\varphi) \cup \mathcal{C}_{-10}(\varphi), \\
\mathcal{D}(\varphi) &:= \mathcal{D}_1(\varphi) \cup \mathcal{D}_{10}(\varphi) \cup \mathcal{D}_{-1}(\varphi) \cup \mathcal{D}_{-10}(\varphi),
\end{aligned} \tag{4.2a}$$

which correspond to the union of four jump and flow sets graphically illustrated in Figure 4.1. Selection (4.2a) intuitively leads to a reduced phase mismatch between  $\sigma$  and  $z_2$  (equivalently, between  $v_s$  and  $i_c$ ), as shown by the sample solution of (4.1), (4.2) represented in black in Figure 4.1. More precisely, for each  $q \in \{-1, 1\}$ , define

$$\mathcal{C}_q(\varphi) := \{ (z, \sigma, d) : \ \sigma = q, d = q, d ((z_1 + \sigma) \sin \varphi - z_2 \cos \varphi) \le 0 \},$$

$$(4.2b)$$

$$\mathcal{C}_{q0}(\varphi) := \{ (z, \sigma, d) : \ \sigma = 0, d = q, (d (z_1 \sin \varphi - z_2 \cos \varphi) \ge 0) \lor (dz_2 \ge 0) \},$$
(4.2c)

$$\mathcal{D}_q(\varphi) := \{ (z, \sigma, d) : \sigma = q, d = q, dz_2 \ge 0, (z_1 + \sigma) \sin \varphi - z_2 \cos \varphi = 0 \},$$

$$(4.2d)$$

$$\mathcal{D}_{q0}(\varphi) := \{ (z, \sigma, d) : \ \sigma = 0, d = q, dz_2 \le 0, z_1 \sin \varphi + z_2 \cos \varphi = 0 \}.$$
(4.2e)

Note that  $\mathcal{D}_1(\varphi)$  and  $\mathcal{D}_{-1}(\varphi)$  are horizontally translated with respect to the origin. Therefore, when  $\sigma = 0$ , solutions flow by spanning a constant cone centered at the origin, so that the flowing interval is constant regardless of the amplitude of z. Secondly, the zero crossing of the current  $i_C$  (proportional to  $z_2$ ) happens approximately at the middle of that flowing interval (the lower  $\beta$  is, the better this approximation becomes, due to the higher quality factor). For the SRC configuration, having  $v_s$  and  $i_C$  mostly in phase ensures that the input voltage and the current of the resonant tank are almost in-phase. However, having  $v_s$  and  $i_C$  almost in-phase prevents ZVS in half of the commutations because the jumps when  $\sigma = 0$  happen when the current is already inverted. Not having ZVS is the most important drawback of the phase-shift modulation control law. Moreover, at this stage, not having ZVS can only be identified by looking at how the control is formulated, this is going to be clear with the experimental results in Figure 4.7, where the induced ringing is clearly visible in the input voltage  $v_s$ .

Remark 4.1 An equivalent control law that avoids using the state d and enforces the same behavior is

$$\sigma = \begin{cases} 0, & \text{if } x_1^2 \sin^2 \varphi - x_2^2 \cos^2 \varphi \ge 0, \\ \text{sign}(x_2), & \text{otherwise.} \end{cases}$$
(4.3)

However, having the couple  $(\sigma, d)$  allows implementing the control (4.1), (4.2) like a state-machine, which is a robust solution due to the presence of a hysteresis. While, control law (4.3) alone is subject to noise.



Figure 4.2: Simulation results of the phase-shift modulation control law (4.2). At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes normalized by Q.

### 4.2 Input-output characteristic

With the phase-shift modulation control, the desired property that the system oscillates near the resonant frequency is achieved for all the values of  $\varphi$ . Figure 4.2 confirms that the oscillating frequency is near the resonant one if Q is high enough. The frequency with respect to  $\varphi$  is no more constant when Q is low, specifically when Q is almost at the limit of  $\frac{1}{2}$  considered by the underdamped condition in Assumption 2.2. A highly nonlinear behavior can be observed in the same low Q condition for the amplitude at the right of Figure 4.2. The amplitude reaches zero for  $\varphi = \frac{\pi}{2}$ . As for the frequency modulation analysis, we reason in terms of the peak amplitudes of  $x_1$  and  $x_2$ , which are proportionally related to voltage and current. If the quality factor is not near the  $\frac{1}{2}$  limit, the static relationship between  $\varphi$  and the peak amplitude of  $x_1$ , and therefore also  $x_2$ , is approximately described by a cosine function.

The cosine relationship can be explained if we analyze the system considering the harmonic content, in particular the one of the fundamental harmonic. The parameter  $\varphi$  acts on the harmonics of  $\sigma$ , as it corresponds to the phase-shift, namely it is proportional to the time during which  $\sigma = 0$ . From [Pitel, 1986],  $\sigma$  can be expressed by the Fourier expansion

$$\sigma = \frac{4}{\pi} \sum_{n=1,3,\cdots}^{\infty} \cos \varphi \frac{\sin \frac{n\pi}{2}}{n} \sin(n\omega t), \tag{4.4}$$

where we can remark that the amplitude of the first harmonic corresponds to  $\frac{4}{\pi}\cos\varphi$ , and  $\omega$  is a generic oscillating frequency. Moreover, assuming that the oscillating frequency is almost constant and near  $\omega_0$ , we know that the static gain between the first harmonic of  $\sigma$  and the amplitude of  $x_2$  corresponds to the quality factor Q. This let us conclude, considering only the first harmonic and using (4.4), that an approximated expression between  $\varphi$  and the amplitude of  $x_2$  is

$$x_{2\text{peak}} \simeq \frac{4}{\pi} Q \cos \varphi.$$
 (4.5)

For a visual confirmation of (4.5), see Figure 4.3 showing simulation results (orange stars) vs the graph of the function  $\frac{4}{\pi}Q\cos\varphi$  for the selected values of Q = 1.14 and Q = 3.43. For a lower value of Q we can see that the relationship is not perfect but yet acceptable, while for higher Q it is almost exact. The discrepancy for the lower Q case comes from the fact that the signals are not fully sinusoidal, hence the first harmonic description is limited.



Figure 4.3: Peak value of  $x_2$  with respect to  $\varphi \in [0, \frac{\pi}{2})$  for Q = 1.14 and Q = 3.4. The interpolating cosine function in (4.5) (solid violet) vs simulations results (orange star).

# 4.3 Stability result

For the stability result we require the mild underdamped Assumption 2.2 for the oscillating behavior, requiring that flowing solutions revolve in the state-plane of Figure 4.1, which ensures existence of a nontrivial asymptotically stable hybrid limit cycle for any reference input  $\varphi \in [0, \frac{\pi}{2})$ . The theorem states the asymptotic stability of a nontrivial hybrid periodic orbit with basin of attraction corresponding to the whole space except for the four points (see the green dots projection in Figure 4.4) in the set

$$\mathcal{K} := \{(0,0,0,-1), (0,0,0,1), (-1,0,1,1), (1,0,-1,-1)\}.$$

These points comprise weak equilibria<sup>1</sup> and they do not belong to the basin of attraction: for example, solutions starting from (0, 0, 0, -1) and (0, 0, 0, 1) can flow forever staying there or may jump to (-1, 0, 1, 1) or (1, 0, -1, -1) and then: either flow and converge to the hybrid limit cycle, or continue to jump among the points in  $\mathcal{K}$ .

**Theorem 4.2** Under Assumption 2.2, for each selection of  $\varphi \in [0, \frac{\pi}{2})$ , the closed loop (4.1), (4.2) has a unique nontrivial hybrid periodic orbit  $\mathcal{O}_{\varphi}$  that is stable and almost globally attractive with basin of attraction  $\Xi = (\mathbb{R}^2 \times \{-1, 0, 1\} \times \{-1, 1\}) \setminus \mathcal{K}$ .

#### 4.3.1 Preliminary observations to prove Theorem 4.2

Let us define the set  $\Omega = \Omega_1 + \Omega_{-1} + \Omega_{10} + \Omega_{-10}$  as the set of points visited by any solution flowing in C from g(D). More rigorously, denoting  $t \mapsto \psi_{\xi_0}(t, 0)$  any flowing solution of (4.1) from  $\xi_0$ , for each  $i \in \{1, -1, 10, -10\}$ , we define

$$\Omega_i = \{\xi \in \mathcal{C} : \xi = \psi_{g(\xi_0)}(t, 0) \text{ for some } \xi \in \mathcal{D}_i, t \ge 0\}.$$

Sets  $\Omega_1$  and  $\Omega_{-1}$  correspond to two cones centered at the origin. Set  $\Omega_{10}$  (respectively  $\Omega_{-10}$ ) corresponds to a cone minus an area limited by what we may call *boundary solution*, which flows from the cone vertex  $z_v = (1,0)$  (respectively  $z_v = (-1,0)$ ). About this *boundary solution*, it is well-defined for any  $\varphi \in [0, \frac{\pi}{2})$  since the vector field at the vertex is vertical, therefore the solution is forced to initially flow inside the cone and then, due to Assumption 2.2, it revolves clockwise while flowing, until it reaches  $\mathcal{D}_{-1}$  (respectively  $\mathcal{D}_1$ ). We define the scalar  $\lambda_m > 0$  as the distance between the vertex (1,0) (respectively (-1,0)) and the point where the *boundary solution* intersects  $\mathcal{D}_{-1}$  (respectively  $\mathcal{D}_1$ ) after flowing in the cone.

<sup>&</sup>lt;sup>1</sup>A weak equilibrium is a point from which there exist constant solutions but also non-constant ones.



Figure 4.4: Projection on the z-plane of the sets:  $\Omega$  (shaded areas),  $\mathcal{P}$  (solid red lines),  $\mathcal{K}$  (green dots) and representation of the *boundary solutions* defining  $\lambda_m$  (black dotted arcs). The dashed-dotted lines represent sample solutions used in the proof.

Figure 4.4 depicts  $\lambda_m$ , the set  $\Omega$ , the set  $\mathcal{P} := (\mathcal{D}_1 \cup \mathcal{D}_{-1}) \cap \Omega$ , and the coordinate  $\lambda \in [\lambda_m, +\infty)$  defined as

$$\lambda = \Lambda(\xi) := \left| \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} g(\xi) \right|, \quad \forall \xi \in \mathcal{P},$$
(4.6)

i.e., the distance from the origin in the state-plane projection. See also the first and third diagram in Figure 4.1.

The following lemma is an immediate property of solutions.

**Lemma 4.3** Set  $\Omega$  is forward invariant and all solutions from  $\Omega$  are unique. Moreover, all solutions from  $(\mathcal{C} \cup \mathcal{D}) \setminus \mathcal{K}$  converge to  $\Omega$  in uniform finite time.

Introduce now the function  $\phi_{\mathcal{P}}(\xi_0) : \Omega \to \mathcal{P}$  returning the value  $\psi_{\xi_0}(t_{\mathcal{P}}, j_{\mathcal{P}}) \in \mathcal{P}$ , where  $\psi_{\xi_0}$  is the solution to (4.1) starting at  $\xi_0$  (unique by Lemma 4.3), and  $(t_{\mathcal{P}}, j_{\mathcal{P}})$  is

$$(t_{\mathcal{P}}, j_{\mathcal{P}}) = \operatorname*{argmin}_{(t,j)\in \operatorname{dom}\psi_{\xi_0}}(t+j) \quad \text{s.t. } \psi_{\xi_0}(t,j)\in\mathcal{P}.$$
(4.7)

Intuitively speaking, for any  $\xi_0 \in \Omega$ ,  $\phi_{\mathcal{P}}(\xi_0)$  denotes the value of the unique solution starting at  $\xi_0$  the first time that it belongs to  $\mathcal{P}$ .

#### 4.3.2 **Proof of Theorem 4.2**

We first prove existence and global asymptotic stability (GAS) from  $\Omega$  of a hybrid periodic orbit  $\mathcal{O}_{\varphi}$  contained in the interior of  $\Omega$ , based on a Poincaré analysis. Then by the uniform convergence established in Lemma 4.3, the result follows.

After the first jump, all solutions must transit through set  $\mathcal{P}$ . Therefore, we may define a Poincaré map characterizing a solution half-cycle as  $\xi^+ = \phi_{\mathcal{P}}(g(\xi)) \in \mathcal{P}$  for any  $\xi \in \mathcal{P}$ . Due to the central symmetry of the dynamics, we can also parameterize the Poincaré map in terms of  $\lambda$ , as defined in (4.6), through description

$$\lambda^{+} = \Phi(\lambda), \quad \lambda \in [\lambda_m, +\infty), \tag{4.8}$$

with  $\Phi(\lambda) := \Lambda(\phi_{\mathcal{P}}(\xi_{\lambda}))$ , and  $\Lambda^{-1}(\lambda)$  denoting a selection of  $\xi_{\lambda} \in \mathcal{P}$  ensuring  $\Lambda(\xi_{\lambda}) = \lambda$ . The discrete dynamics (4.8) plays the role of a Poincaré map for (4.1) restricted to  $\Omega$ . We show below that there exists a unique globally asymptotically stable equilibrium  $\lambda^* = \Phi(\lambda^*)$  for (4.8).

**Energy function.** Due to Lemma 4.3, we consider next only points  $\xi \in \mathcal{P}$ . Then, the proof of existence and uniqueness focuses on the behavior of the *z* components of the unique solution to (4.1) inducing  $\Phi$ , in terms of the energy function

$$E(z) := \frac{1}{2}|z|^2.$$
(4.9)

Due to this fact, to simplify our notation, in the sequel, we use  $\overline{g}$  to denote the *z* component of the jump map *g*. Also, we will employ overlines on the jump and flow sets, to denote their projection on the *z* plane. With a slight abuse of notation, we will only refer to the *z* component of the solutions, whenever the  $\sigma$  and *d* components are clear from the (flow or jump) set under consideration.

Let  $\varphi \in [0, \frac{\pi}{2})$  be fixed and, for each  $\lambda \geq \lambda_m$ , consider any pair of points  $z_F(\lambda) \in \overline{g}(\mathcal{D}_1)$  and  $z_B(\lambda) \in \overline{g}(\mathcal{D}_{-1})$  both of them at the same distance  $\lambda$  from the origin, where "F" stands for "Forward" and "B" stands for "Backwards". A pictorial representation of these points and related solutions is shown in Figure 4.4. Due to the symmetry of the jump sets, we have  $E(z_F(\lambda)) = E(z_B(\lambda)) = \frac{1}{2}\lambda^2$ . Consider the points  $\zeta_F(\lambda) \in \overline{g}(\mathcal{D}_{10})$  and  $\zeta_B(\lambda) \in \overline{g}(\mathcal{D}_{10})$  obtained, respectively, from the forward flowing solution (unique from Lemma 4.3) starting at  $z_F(\lambda)$  and the backward solution starting at  $z_B(\lambda)$ , jumping back to the unique point  $z_B(\lambda)^- \in \mathcal{D}_{-1}$  and then (uniquely) flowing backwards in time in  $\mathcal{C}_{-1}$  until they both reach  $\overline{g}(\mathcal{D}_{10})$ .

Forward solution. About  $z_F(\lambda)$  and  $\zeta_F(\lambda)$ , the forward solution flows in  $C_{10}$  and then jumps after it reaches  $\mathcal{D}_{10}$  (which necessarily happens after a finite time, due to the revolving nature of flowing solutions, as induced by Assumption 2.2). In particular, since  $C_{10}$  is a cone, regardless of  $\lambda$ , the solution flows for a fixed time T and the energy dissipation during such a flowing interval corresponds to  $\Sigma_F(\lambda) = \frac{1}{2}\lambda^2(1-\mu(\varphi)^2)$ , where  $\mu(\varphi)$  (the dependence on  $\varphi$  is dropped in the following) is a constant that can be easily computed from the flowing solution of  $\dot{z} = Az$ , by solving the equality  $e^{AT} \lambda \begin{bmatrix} \cos \varphi \\ \sin \varphi \end{bmatrix} = \lambda \mu \begin{bmatrix} \cos \varphi \\ -\sin \varphi \end{bmatrix}$ , resulting in  $\mu = \begin{bmatrix} \cos \varphi \\ -\sin \varphi \end{bmatrix}^{\top} e^{AT} \begin{bmatrix} \cos \varphi \\ \sin \varphi \end{bmatrix} \in (0, 1]$ . After this flowing interval, the solution belongs to  $\mathcal{D}_{10}$  and must jump (from  $e^{AT} z_F(\lambda) = \lambda \mu \begin{bmatrix} \cos \varphi \\ -\sin \varphi \end{bmatrix}$  to  $\zeta_F(\lambda)$ ). This jump is associated with an increase  $\delta_F$  of the energy E, amounting to

$$\delta_F(\lambda) = \frac{1}{2} \left( |(e^{AT} z_F)^+|^2 - |e^{AT} z_F|^2 \right) = \frac{1}{2} + \lambda \mu \cos \varphi.$$
(4.10)

Overall, we may characterize the energy at point  $\zeta_F(\lambda)$  as

$$E_F(\lambda) := E(\zeta_F(\lambda)) = \frac{1}{2}\lambda^2 - \Sigma_F(\lambda) + \delta_F(\lambda).$$
(4.11)

**Backward solution.** Consider now  $z_B(\lambda)$  and  $\zeta_B(\lambda)$ , and also here notice that the backward solution of interest jumps backwards to a point in  $\mathcal{D}_{-1}$  denoted as  $z_B(\lambda)^- = \lambda \begin{bmatrix} -\cos\varphi \\ -\sin\varphi \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1-\lambda\cos\varphi \\ -\lambda\sin\varphi \end{bmatrix}$ . The variation of energy across this backward time jump corresponds to

$$\delta_B(\lambda) = \frac{1}{2} \left( |z_B(\lambda)^-|^2 - |z_B(\lambda)|^2 \right) = \frac{1}{2} - \lambda \cos \varphi.$$
(4.12)

Continuing in the backward motion of this solution, for any  $\lambda \ge \lambda_m$ , we see a flowing interval in the set  $C_{-1}$  where the solution reaches (in finite backward time) the set  $\overline{g}(\mathcal{D}_{10})$ , due to the revolving properties induced by Assumption 2.2.

Applying Lemma 3.5 such a flowing interval is associated with an energy increase (in backwards time) corresponding to  $\Sigma_B(\lambda) := \frac{\beta}{\omega_0} \Pi(z_B(\lambda)^-)$ , where  $\Pi(z_B(\lambda)^-)$  is the (unsigned) area hatched between the graph of the backwards trajectory and the axis  $z_2 = 0$ . Note that  $\Sigma_B$  is a positive and quadratically increasing function of  $\lambda$ .

Overall, we may characterize the energy at point  $\zeta_B(\lambda)$  as

$$E_B(\lambda) := E(\zeta_B(\lambda)) = \frac{1}{2}\lambda^2 + \Sigma_B(\lambda) + \delta_B(\lambda).$$
(4.13)

Energy balance. Consider the mismatch function

$$\widetilde{E}(\lambda) := E_F(\lambda) - E_B(\lambda) = \delta(\lambda) - \Sigma(\lambda), \qquad (4.14)$$

where  $\Sigma$  is a quadratically increasing function of  $\lambda$  (it is strongly convex):

$$\Sigma(\lambda) := \Sigma_B(\lambda) + \Sigma_F(\lambda) = \Sigma_B(\lambda) + \frac{1}{2}\lambda^2(1-\mu^2), \qquad (4.15)$$

and  $\delta$  is a linearly increasing function of  $\lambda$ :

$$\delta(\lambda) := \delta_F(\lambda) - \delta_B(\lambda) = \lambda(1+\mu)\cos\varphi.$$
(4.16)

**Lemma 4.4** There exist a unique value  $\lambda^* > \lambda_m$  such that  $\widetilde{E}(\lambda^*) = 0$ . Moreover,  $\lambda^*$  is a fixed point for  $\Phi$  in (4.8).

**Proof.** Let us show that  $\widetilde{E}(\lambda_m) = \delta(\lambda_m) - \Sigma(\lambda_m) > 0$ , which from (4.14) is equivalent to showing that  $E_F(\lambda_m) - E_B(\lambda_m) > 0$ . For  $\lambda = \lambda_m$ , a) the forward solution reaches  $\zeta_F(\lambda_m)$  with energy  $E_F(\lambda_m) = \frac{1}{2} + \frac{1}{2}\lambda_m^2\mu^2 + \lambda_m\mu\cos\varphi$ ; b) by definition of  $\lambda_m$ , the backward solution reaches the vertex  $\zeta_B = (1, 0)$  with energy  $E_B(\lambda_m) = \frac{1}{2}$ . Therefore,  $E_F(\lambda_m) - E_B(\lambda_m) = \frac{1}{2}\lambda_m^2\mu^2 + \lambda_m\mu\cos\varphi$ , which is the sum of two positive scalars. Since function  $\lambda \mapsto \widetilde{\psi}(\lambda) := -\widetilde{E}(\lambda)$  is negative at  $\lambda_m$  and strongly convex, then, from Lemma 3.4, there exists a unique positive value  $\lambda^* > \lambda_m$  such that  $\widetilde{E}(\lambda^*) = 0$ . Finally, we can express the energy difference, in terms of  $\lambda$ , between the final and initial points  $\Phi(\lambda)$  and  $\lambda$ , as  $\widetilde{E}(\lambda) = \frac{1}{2}(\Phi(\lambda)^2 - \lambda^2)$ . From which we conclude that  $\lambda^*$  is a fixed point for (4.8).

The corresponding points  $\xi^* \in \mathcal{P}$  that satisfy  $\Lambda(\xi^*) = \lambda^*$ , and the image of the unique solution originating from those points is a unique nontrivial hybrid periodic orbit in the interior of  $\Omega$  (because  $\lambda^* > \lambda_m$ ), characterized as

$$\mathcal{O}_{\varphi} = \{\xi \in \Omega : \Lambda(\phi_{\mathcal{P}}(\xi)) = \lambda^{\star}\}.$$
(4.17)

**Lyapunov function.** In order to prove GAS of the hybrid periodic orbit we reduce the stability analysis to the Poincaré map (4.8). We have already shown that there exists a unique equilibrium point  $\lambda^* = \Phi(\lambda^*)$ . Then, we introduce the quadratic Poincaré-like Lyapunov function,

$$V(\lambda) := (\lambda - \lambda^*)^2, \tag{4.18}$$

which is shown in Figure 4.5 for the special case  $\varphi = \pi/4$ . Similar to the final part of the proof of [Bisoffi et al., 2018, Lemma 2], to prove global asymptotic stability, we show that:

$$V(\Phi(\lambda)) - V(\lambda) < 0 \quad \forall \lambda \ge \lambda_m, \ \lambda \ne \lambda^{\star},$$

or, equivalently,

$$(\Phi(\lambda) - \lambda)(\Phi(\lambda) + \lambda - 2\lambda^*) < 0 \quad \forall \lambda \ge \lambda_m, \ \lambda \ne \lambda^*.$$
(4.19)

To show this, let us divide the study for  $\lambda > \lambda^*$  and  $\lambda < \lambda^*$ . From the proof of Lemma 4.4, for  $\lambda > \lambda^*$ , we have that  $\tilde{E}(\lambda) < 0$ , which implies  $\Phi(\lambda) - \lambda < 0$ , in other terms  $\lambda > \Phi(\lambda) > \lambda^*$  where  $\Phi(\lambda) > \lambda^*$  comes from the uniqueness of flowing solutions so that they cannot cross. Next, we assess the positivity of the second term in (4.19) as  $\Phi(\lambda) + \lambda - 2\lambda^* > 2(\Phi(\lambda) - \lambda^*) > 0$ . For the case  $\lambda < \lambda^*$ , similar considerations hold, leading to (4.19). Finally, continuity of  $\Phi$  following from similar reasoning to [Bisoffi et al., 2018, Lemma 2] and the stability of  $\lambda^*$  for (4.8) proved above, imply global asymptotic stability of  $\mathcal{O}_{\varphi}$  in (4.17) from  $\Omega$ , following the steps in [Bisoffi et al., 2018, Proposition 1]. Finally, GAS of  $\mathcal{O}_{\varphi}$  from  $\Xi$  follows from the uniform convergence established in Lemma 4.3.



Figure 4.5: Logarithmic representation of the Lyapunov function V in (4.18), for the value  $\varphi = \frac{\pi}{4}$ .

# 4.4 Experimental validation

The results of Theorem 4.2 are validated on an experimental SRC prototype and via simulations. The experimental setup consists of an SRC designed for a 50 kHz resonant frequency. The DC power supply is  $V_g = 24$  V, the resonant tank components are  $L = 94.5 \,\mu\text{H}$  and C = 100 nF. The control law is implemented in an FPGA where we use ADCs to sense the current and the voltage on the capacitor. The adaptation with respect to Section 3.4 is in the control law implemented in the FPGA, which is clearly different, whereas the hardware is described in Section 3.4.

The control law is implemented in the FPGA as an automaton with four states, correspond-



Figure 4.6: Phase portraits in the  $(z_1, z_2)$  coordinates: simulations on the top and experiments on the bottom with different values of  $\varphi$ . The  $\varphi$ -tilted dashed violet lines represents the jumps sets. The load is  $R = 10.1 \Omega$ .



Figure 4.7: States  $\sigma$  (red) and  $x_2$  (light blue) from the SRC experimental prototype with  $R = 10.1 \Omega$ , for values of  $\varphi$  shown in Figure 4.6.

ing to the four parts in which one period can be decomposed, based on the variables  $\sigma$  and d:  $(\sigma, d) \in \{(1, 1), (0, 1), (-1, -1), (0, -1)\}$ . (see Figure 4.1). The jump sets are modeled as half-planes to ensure robustness and simplicity in the implementation. The automaton is allowed to go to the next sequential state whenever 1) jump signal is active and 2) the automaton is in the preceding state (e.g  $(\sigma, d) = (1, 1)$  and  $\mathcal{D}_1$  active:  $x_1 \sin \varphi - x_2 \cos \varphi \ge 0$ ).

As in Section 3.4, we need to deal with noise injected by the switching, but in the current case it is not possible to use time regularization on the signal corresponding to  $\sigma$ , since consecutive changes in  $\sigma$  can be infinitely fast (e.g. for  $\varphi = 0$  or  $\varphi = \pi/2$  there are two consecutive jumps). Therefore, the implemented solution is to regularize the signals of the jump sets because they have a regular behavior since they are active approximately for half-cycle. The regularization of the jump signals solved the main problems related to the switching, making the jump detection robust.

Multiple experiments have been run for two load selections:  $R = 10.1 \Omega$  and  $R = 21.8 \Omega$ . Figure 4.6 compares the simulated and experimental steady-state responses for different values of  $\varphi$ . We emphasize that no startup controller is needed due to the (almost) global attractivity established in Theorem 4.2, thus the device starting at rest effectively spirals out to reach the prescribed oscillating behavior. The corresponding experimental time waveforms are reported in Figure 4.7. Note that, the input current (i.e. the capacitor current, due to the SRC configuration) is approximately in phase with the input voltage. Having the first harmonics aligned implies improved performance in terms of efficiency, since more power is transmitted to the load and less power is dissipated in the resonant tank. Finally, Figure 4.8 compares the simulated and experimental frequencies and amplitudes. The black horizontal dotted lines show the resonant frequencies evaluated by characterizing the resonant tank, with the load, at low power. The physical controller presents some limits for low amplitudes (large  $\varphi$ ) due to the resolution of the ADCs and the amplitude of the noise. Therefore, only a subset of values for  $\varphi$  has been validated experimentally.

The experiments confirm the simulation results. The frequency mismatch visible in both figures amounts to an acceptable 4%. Minor amplitude discrepancies are also visible, probably due to model uncertainties (e.g. nonlinear dependence of the inductor on the current, parasitic effect on the PCB, sampling effects) but the reliable closed-loop behavior illustrates the robustness of the proposed control.



Figure 4.8: Comparison between experiments and simulations for the phase-shift modulation (4.2) with  $R = 10.1 \Omega$  at the left and  $R = 21.8 \Omega$  at the right. The frequencies are rescaled by the estimated resonant frequency  $\hat{\omega}_0 = 2\pi \hat{f}_0$ :  $\hat{f}_0 = 50$  kHz for  $R = 10.1 \Omega$  and  $\hat{f}_0 = 45.8$  kHz for  $R = 21.8 \Omega$ .

# 4.5 Final considerations

In this chapter, we have seen how a phase-shift modulation control law can be described with hybrid dynamical systems. The proposed control law results in a self-oscillating behavior that allows us to modulate the amplitudes while keeping the frequency constant. The counterpart is that by keeping the frequency constant at the resonant one, ZVS is not enabled for all the commutations. In particular, ZVS is achieved only for half of the commutations in a cycle. We will see in Chapter 5 how this control law can be modified in order to ensure ZVS. For the phase-shift modulation, we have provided formal guarantees for stability and attractivity of the limit cycle for every input parameter  $\varphi$  in the range  $[0, \frac{\pi}{2})$  if the underdamped condition  $Q > \frac{1}{2}$  is satisfied. The proposed phase-shift modulation control law (4.2) has been validated in an experimental prototype of a second-order series resonant convert. In Chapter 6, we will see how the same control law works also for a third-order LLC resonant converter prototype.

# 5

# Mixed modulation for dc-dc converters

The objective of this chapter is to propose a control methodology for resonant converters, which is then applied to a dc-dc converter. We first propose a novel self-oscillating control law for the resonant tank, referred to as *mixed modulation*, which incorporates the benefits of the frequency and phase-modulation control laws, discussed in Chapters 3 and 4, respectively. The mixed modulation control will be developed for second-order resonant converters as an extension of frequency and phase-shift modulation.

Eventually, we chose to focus on a battery charger application as a dc-dc converter application. Nevertheless, similar considerations to what we are going to discuss can be applied for a more generic dc-dc converter. We opted for a battery charger due to it being a hot-topic with the fast increase of electro-mobility nowadays. There are several topologies that can be selected for a battery charger. Both resonant converters, like the LLC or LCCL, and non-resonant, like the DAB, are used, the specific choice depends on the specific requirements of the application. Some requirements can be: galvanic isolation (with a high-frequency transformer), low output ripple to avoid heating the battery, low EMI, high efficiency, bidirectional operation are usually required). For example, wall chargers require a bi-directional current flow, making DAB a viable option, whereas the latest trend in OBCs is towards unidirectional current flow. Low EMI and high efficiency can be enabled thanks to ZVS, which can be achieved with resonant converters. Therefore, generally there is not a unique answer, in our case we are going to consider an On-Board Charger (OBC) for Electric Vehicles (EVs) with an LLC resonant topology.

The basic scheme of the converter is shown in Figure 5.1, it contains one dc-ac stage and one ac-dc stage. The H-bridge together and the resonant tank form the dc-ac stage: the input DC voltage  $V_g$  is modulated by the H-bridge inducing an oscillating behavior in the resonant tank. The ac-dc stage includes the rectifier with an output filter, which then delivers a DC current to the load. This application introduces some challenges with respect to what has been seen so far:

- the resonant tank is a third-order LLC due to the magnetizing inductance of the transformer;
- the load is generally nonlinear;



Figure 5.1: Representation of the stages in a dc-dc converter.

• the output filter introduces additional unmodeled dynamics to the converter.

Our solution stands out for the following reasons:

- the capability to ensure Zero-Voltage Switching (ZVS) for all switching conditions, implying reduced EMI and high efficiency;
- the oscillations in the resonant tank are self-sustained and not externally imposed;
- there is no direct time dependency in the control law thanks to the state-plane approach;
- a wide range of conversion ratios is possible with a narrow range of operating frequencies;
- galvanic isolation thanks to the transformer, which also enables the boost operation of the converter.

In this chapter, we also focus on the analysis of the complete system – LLC and rectifier – in order to additionally propose a control scheme for output current regulation. Usually, considering battery chargers, they do not have hard constraints on the dynamics, since the dynamics of the charging process is relatively slow, but rather they have constraints on the maximum amplitude of the output current ripple, which depends on the output filter. The interconnection of different circuits makes the control challenging and more interesting since new behaviors emerge. In particular, we will see how the battery enables the equivalent resistor model, and the LLC allows ZCS in the rectifier.

#### Contribution

The contribution of this chapter is threefold. First, we propose a novel self-oscillating control law, denoted as *inner loop* in Figure 5.2, which is in charge of ensuring the oscillations through a *mixed modulation* control law (block  $\mathcal{H}_{MM}$  in Figure 5.2). This mixed modulation takes as input parameters  $\delta$ , which is fixed, and  $\varphi$  as described in Section 5.1. The novel control law is analyzed for second-order resonant converters, as in Chapters 3 and 4. Even though, it is employed in the third-order LLC resonant converter as denoted in the *inner loop* in Figure 5.2. related to this, we will see in Chapter 6 the different modulation control laws applied to the third-order LLC resonant converter prototype developed by us. Second, the modeling of the electronic parts in Figure 5.1 is discussed in Section 5.2, with emphasis on a simplified model that can be adopted in an initial analysis. Third, in Section 5.3 we propose a control strategy for the output current regulation, denoted as *outer loop* in Figure 5.2. The outer loop is composed of a Proportional-Integral (PI) controller with anti-windup (AW) feedback. The PI is designed using an LMI based procedure for an initial estimation of the gains.



Figure 5.2: Overview of the inner and outer control loops in the dc-dc converter.



Figure 5.3: Representation of the zones used for the mixed modulation control law.

# 5.1 Inner loop: mixed modulation

So far we have seen two state-plane-based control techniques that ensure either frequency modulation or phase-shift modulation. The downsides are that frequency modulation requires a large range of frequencies resulting in low efficiency, whereas phase-shift modulation cannot ensure ZVS during all commutations for all input reference values. Starting from these considerations, we propose another technique that combines frequency and phase-shift modulation from Chapters 3 and 4, respectively, while mitigating the downsides. The idea is to have a dominant phase-shift modulation behavior – i.e., we change the amplitude of the harmonic content of the input voltage  $v_s$ , in order to modulate the amplitude – while letting the frequency adapt in order to ensure ZVS.

Casting this idea in the state-plane is easier than expected. First, reasoning on the  $(x_1, x_2)$  stateplane, we modulate the output by acting on the aperture of the zones where  $\sigma = 0$ , which corresponds to the previous phase-shift control. What is different in this control law is the location of these zones. Let us notice that there is ZVS if the input current is positive (respectively negative) when the turn-on of the switches occurs from positive input voltage to negative input voltage (respectively from negative input voltage to positive input voltage). Therefore, it is enough to keep the zones where  $\sigma = 0$  in the upper plane ( $x_2 > 0$ ) when switching from +1 to -1, and in the lower plane ( $x_2 < 0$ ) in the opposite case.

This can be easily understood by looking at Figure 5.3, where we can draw some links with the frequency and phase-shift modulation control strategies of Chapters 3 and 4. As before, the aperture of the zone  $\sigma = 0$  is  $2\varphi$ . Therefore, the maximum amplitude is obtained with  $\varphi = 0$ . The opposite happens with  $\varphi = \frac{\pi}{2}$ , since  $\sigma$  is always zero and the converter is off. To ensure ZVS it is enough to keep these zones far enough from the horizontal axis where  $x_2 = 0$ , i.e. the input current for an SRC. To this end, we introduce the new parameter  $\delta$  that describes the angular distance between axis  $x_1$  and the line marking the switch condition from  $\sigma = 0$ . The parameter  $\delta$  is a positive angle that should be sufficiently large as to ensure enough current for the soft-switching. Here, a link can be drawn with the frequency modulation control where the parameter  $\theta$  would correspond to  $\theta = \pi - \delta - \varphi$  ( $\theta$  describes the angular position of the line dividing in two halves the zero-sets). Therefore, by acting on  $\delta$  with fixed  $\varphi$ , the behavior is similar to that of frequency modulation. While, by acting on  $\varphi$  a phase-shift modulation like behavior is induced. To fix the notation, the control law that we propose has  $\varphi$  as control parameter, while  $\delta$  is a constant parameter that ensures ZVS.

**Remark 5.1** The consideration above about ZVS only holds for a series resonant converter and not for a parallel one. The reason is that in the SRC, as in the LLC, the current on the capacitor  $i_C$  (proportional to  $x_2$ ) corresponds to the input current, which is the one that has to be considered for ZVS, whereas this is not the case for the PRC. Generally speaking, in order to have ZVS with state-plane-based control laws, the input current should always be represented in one of the axes.

#### 5.1.1 Hybrid dynamics definition

The hybrid dynamical system describing the mixed modulation is similar to the one defined in Chapter 4. What changes is the definition of the jump and flow sets. For the rest, the dynamics remains the same and also the periodic sequence for  $\sigma$ . For completeness, we report here the dynamics (in *x*-coordinates)

$$\begin{vmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{\sigma} \\ \dot{d} \end{vmatrix} = f_{\delta}(\xi) := \begin{vmatrix} \omega_0 x_2 \\ -\omega_0 x_1 - \beta x_2 + \omega_0 \sigma \\ 0 \\ 0 \end{vmatrix}$$

$$\xi \in \mathcal{C}(\varphi, \delta), \qquad (5.1a)$$

$$\begin{cases} x_1^+ \\ x_2^+ \\ \sigma^+ \\ d^+ \end{cases} = g_{\delta}(\xi) := \begin{bmatrix} x_1 \\ x_2 \\ -d + \sigma \\ -d + 2\sigma \end{bmatrix}$$

$$\xi \in \mathcal{D}(\varphi, \delta). \qquad (5.1b)$$

The angle  $\varphi \in [0, \frac{\pi}{2})$  is the reference input affecting the steady-state output voltage (minimum for  $\varphi = \frac{\pi}{2}$  and maximum for  $\varphi = 0$ ). Moreover, the angle  $\delta$  intuitively represents a margin that ensures ZVS. Ideally, we would like  $\delta$  to be the smallest possible, implying that the oscillating frequency is closer to the resonant one. On the other side, to ensure ZVS we need a certain margin of time, to ensure the discharging of the parasitic capacitors of the switches through the flowing current. Practically,  $\delta$  is a trade-off parameter that depends on the switches properties, and it needs to be tuned on the considered system.

Based on  $\varphi$  and  $\delta$ , we select the jump and flow sets as

$$\begin{aligned}
\mathcal{C}(\varphi,\delta) &:= \mathcal{C}_1(\varphi,\delta) \cup \mathcal{C}_{10}(\varphi,\delta) \cup \mathcal{C}_{-1}(\varphi,\delta) \cup \mathcal{C}_{-10}(\varphi,\delta), \\
\mathcal{D}(\varphi,\delta) &:= \mathcal{D}_1(\varphi,\delta) \cup \mathcal{D}_{10}(\varphi,\delta) \cup \mathcal{D}_{-1}(\varphi,\delta) \cup \mathcal{D}_{-10}(\varphi,\delta),
\end{aligned}$$
(5.2a)

which correspond to the union of four jump and flow sets graphically illustrated in Figure 5.3. More precisely, for each  $q \in \{-1, 1\}$ , define

$$\mathcal{C}_q(\varphi,\delta) := \{ (x,\sigma,d) : \sigma = q, \ d = q, \ d(x_1\sin(2\varphi+\delta) - x_2\cos(2\varphi+\delta)) \le 0 \},$$
(5.2b)

 $\mathcal{C}_{q0}(\varphi, \delta) := \{ (x, \sigma, d) : \ \sigma = 0, \ d = q, \ d \left( x_1 \sin \delta - x_2 \cos \delta \right) \ge 0 \},$ (5.2c)

$$\mathcal{D}_{q}(\varphi,\delta) := \{ (x,\sigma,d) : \ \sigma = q, \ d = q, \ dx_{2} \ge 0, \\ x_{1}\sin(2\varphi+\delta) - x_{2}\cos(2\varphi+\delta) = 0 \},$$
(5.2d)

 $\mathcal{D}_{q0}(\varphi, \delta) := \{ (x, \sigma, d) : \ \sigma = 0, \ d = q, \ dx_2 \ge 0, x_1 \sin \delta - x_2 \cos \delta = 0 \}.$ (5.2e)

Remark 5.2 An equivalent update law that enforces the same behavior as (5.1b) is

$$\sigma^+ = -(1 - |\sigma|)\operatorname{sign}(x_2), \tag{5.3}$$

if  $\delta > 0$ . Using (5.3), the behavior is theoretically the same as (5.1b) since the half-plane where the jump is going to occur is known. However, solution (5.3) would not be robust in situations with noise and when the switch happens in the proximity of  $x_2 = 0$ , which is the case for a small  $\delta$ . Once again, the hybrid formulation introduces an important hysteresis mechanism.



(c) Simulation with  $\delta=20\deg$  for different values of  $\varphi.$ 

Figure 5.4: Simulation results of the mixed modulation control law (5.2). In the rows, different values of  $\delta$  have been considered. For each row, at the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes normalized by Q.
### 5.1.2 Input-output characteristic

Figure 5.4 reports simulation results for the mixed control law for different values of  $\delta$  (in different rows) and for different values of the quality factor Q in (1.10) (inside each row). We can observe that the behavior is actually a mix between frequency and phase-shift modulation. First, the frequency range is narrower compared to the frequency modulation case in Figures 3.3 and 3.4. The frequency range becomes larger as Q decreases. At the right of Figure 5.4, we can notice that the amplitudes have a pseudo "cosine" behavior for larger amplitudes, which is lost as  $\delta$  increases. This reflects the fact that for larger amplitudes the converter is operating closer to the phase-modulation conditions; while, in order to reach smaller amplitudes and maintain ZVS, the frequency needs to be increased resulting in a behavior more similar to the frequency modulation. The effect of increasing  $\delta$  is that the range of the frequencies becomes larger, which is expected since increasing  $\delta$  corresponds, more or less, to decrease  $\theta$  in the frequency modulation control laws. Moreover, over certain value of  $\varphi$ , the amplitudes drops (the converter is off) since the controller is not able to ensure the oscillations.

### 5.1.3 Comparison with other modulation control laws

In this section we have seen another modulation control law that can be applied to second-order resonant converters by means of a state-plane representation. Figure 5.5 wraps up the different representations in the state-plane, together with a sketch of the related waveforms of input current and voltage, of the different modulation control laws that have been discussed so far. What we have seen is:

- 1. Frequency modulation: it ensures ZVS at the cost of increasing the frequency.
- 2. Phase-shift modulation: it ensures an almost constant frequency at the cost of losing ZVS.
- 3. Mixed modulation: it ensures ZVS and keeps the frequency variation limited.

Summarizing, we have gone through frequency and phase-shift modulation in order to introduce our *final* control law that is capable of overcoming the disadvantages of the other two. Mixed modulation is a compromise hoping to obtain higher efficiency: from one side by having ZVS and therefore small switching losses; and from another side by reducing the frequency range and therefore improving the efficiency of the magnetic components.

As a final remark, for the modulation control laws, we have kept the focus only on second-order converters. We will see in Chapter 6 that these control laws are also effective on a third-order LLC resonant converter. This is expected when considering the LLC as a perturbed version of the SRC, suggesting that the controller should function similarly.

# 5.2 Modeling

In this section we analyze from an electronic point of view the modeling of the dc-dc converter in Figure 5.1, whose electric schematic is reported in Figure 5.6. The dc-dc converter is composed of four main electronic stages:

- the H-bridge (left block of Figure 5.1);
- the LLC resonant tank (left block of Figure 5.6);
- the rectifier (center block of Figure 5.6);
- the filter (right block of Figure 5.6).

In this section we focus on the latter three stages, whereas the H-bridge, which modulates the voltage  $V_g$  into  $v_s$ , is modeled by the algebraic relationship  $v_s = \sigma V_g$ . Hence, we consider the behavior of the H-bridge to be ideal. The LLC resonant tank has been modeled in Section 1.3, but in this



Figure 5.5: Comparison of the different control laws in the state-plane (left) with a sample of the waveforms of  $\sigma$  and  $x_2$  (right), which are important from an electronic point-of-view. From top to the bottom: frequency modulation, phase-shift modulation, and mixed modulation. From the waveform side to the state-plane we can observe when ZVS is achieved, i.e. when the current at the commutation has the proper sign.



Figure 5.6: Simplified electric schematic of an OBC based on an LLC resonant converter.

case the load of the tank is a full-wave rectifier with an output low-pass filter. Nevertheless, the control design model will use an approximate model of the downstream of the LLC resonant tank in Figure 5.6, which comprises the rectifier with the filter and the battery, as a resistor. Then, the dynamic behavior of the filter is modeled in order to obtain a simplified version, which is tractable in the design of the current regulation control loop, i.e., the outer loop.

### 5.2.1 Equivalent model of a rectifier

The objective of this section is to find a relationship between the transformer output voltage and current  $v_T$  and  $i_T$ , as represented in Figure 5.6, in order to simplify the analysis of the electrical schematic of Figure 5.6. An interesting discussion can be found in [Steigerwald, 1988], where the same expression that we are going to derive is given. These expressions are approximations since the real behavior of the electronic components is not considered (e.g., the threshold voltage of the diodes). The objective is not to find an exact model, but rather an approximation that predicts the range of operation of the circuit.

Let us consider the circuit in Figure 5.6 and start by assuming that the battery voltage  $V_{bat}$  is constant. This implies that also the voltage  $v_r$  – at the output of the rectifier – can be assumed to be constant. Therefore, the voltage  $v_T$  can be represented by a square wave with the same polarity as  $i_T$ , as represented in Figure 5.7, due to the rectifier; i.e., if the current  $i_T$  is positive, so has to be the voltage  $v_T$ , and vice versa, otherwise the diodes would not be conducting as expected.



Figure 5.7: Simplified representation of the input and output waveform of the rectifier.

In summary, what we have is a pseudo-sinusoidal current  $i_T$  and a square wave voltage  $v_T$  in phase with  $i_T$ . If we consider a first harmonic approximation, having voltage and current fundamental harmonics in phase implies that we can consider as if there is a resistor at the secondary side of the transformer. We may therefore represent the circuit of Figure 5.6 by an equivalent system as the one represented in Figure 5.8.

The value of this *equivalent resistor*  $R_{eq}$  in Figure 5.8 is not constant, but it depends on the battery voltage and current  $V_{bat}$  and  $i_{bat}$  shown in Figure 5.6. The expression of  $R_{eq}$  can be retrieved by



Figure 5.8: Simplified equivalent circuit for the OBC.

relying on the amplitudes  $(v_T^{(1)}, i_T^{(1)})$  of the first harmonics of the transformer voltage and current  $(v_T, i_T)$  as follows

$$R_{eq} := \frac{1}{n^2} \frac{v_T^{(1)}}{i_T^{(1)}},\tag{5.4}$$

where the transformation ratio n of the transformer is already included following (B.1) described in Appendix B, so that the circuit is reduced to an LLC, like the one studied in Section 1.3. For the voltage, since  $v_T$  is a square wave with amplitude  $V_{bat}$ , we have that the first harmonic amplitude is  $v_T^{(1)} = \frac{4}{\pi}V_{bat}$  from the Fourier analysis. Similarly, if we assume that the sinusoidal  $i_T$  is rectified and filtered into a constant current of amplitude  $I_{bat}$ , we get that its amplitude is equal to  $i_T^{(1)} = \frac{\pi}{2}I_{bat}$ in order to have the corresponding average value  $I_{bat}$  from the Fourier analysis. Hence, from (5.4) with the above defined first harmonic amplitudes, the expression of  $R_{eq}$  can be written as

$$R_{eq} = \frac{1}{n^2} \frac{\frac{4}{\pi} V_{bat}}{\frac{7}{2} I_{bat}} = \frac{1}{n^2} \frac{8}{\pi^2} \frac{V_{bat}}{I_{bat}}.$$
(5.5)

### 5.2.2 Output filter

The selection of the output filter in Figure 5.6 is an important choice because it affects the output ripple and the converter efficiency. The role of this stage is to filter the *output current* of the rectifier  $i_r$  so that only the dc component reaches and charges the battery. We assume that the input waveform is a rectified sinusoidal current  $i_r = |I_r \sin(\omega t)|$  with average value  $\frac{2}{\pi}I_r$  and harmonics located at  $2n\omega$ . In practice, we will see later that this is not always the case when the rectifier is operating in ZCS condition.

A first simple solution for the output filter design might be to use a first order RC Low-Pass Filter (LPF) consisting of a capacitor  $C_f$  in parallel with the input and a resistor  $R_f$  in series with the battery (namely, circuit in Figure 5.9 without inductors). The advantage of the RC LPF solution is that the dynamics is first-order (no overshoot); on the other hand, the resistor  $R_f$  is subject to the full current going to the battery, which implies high losses. In practice, this solution is implemented with just the capacitor  $C_f$  since  $R_f$  is considered to be the resistance of the battery. A second possibility for the filter design, which is the adopted one, is to use a combination of two inductors  $L_{f1}$  and  $L_{f2}$  and a damping resistor  $R_f$  in series with the battery, instead of only one resistor [Erickson and Maksimović, 2020, Chapter 4]. The electronics schematic is reported in Figure 5.9. As we will see from the transfer function in Figure 5.10, the filter has a low-pass behavior and the resistor  $R_f$  is useful to reduce the peak of the frequency response.

For the filter in Figure 5.9, we can write the following relationship between the input current  $i_r(t)$  and output current  $i_{bat}(t)$  in the frequency domain:

$$I_{bat}(s) = H_i(s)I_r(s) - H_v(s)V_{bat}(s),$$

where the transfer functions are

$$H_i(s) = \frac{R_f \left(1 + s \frac{L_{f1}}{R_f}\right)}{s^3 C_f L_{f1} L_{f2} + s^2 R_f C_f (L_{f1} + L_{f2}) + s L_{f1} + R_f},$$
(5.6)

$$H_{v}(s) = \frac{sR_{f}C_{f}\left(1 + s\frac{L_{f1}}{R_{f}}\right)}{s^{3}C_{f}L_{f1}L_{f2} + s^{2}R_{f}C_{f}\left(L_{f1} + L_{f2}\right) + sL_{f1} + R_{f}},$$
(5.7)



Figure 5.9: Scheme of the output stage filter for the circuit in Figure 5.6.

with the DC gains being  $H_i(0) = 1$  and  $H_v(0) = 0$ . Since we can consider the battery voltage  $V_{bat}$  as almost constant, its value has no influence on the output current  $i_{bat}$ , which in this case only depends on the rectified current  $i_r(t)$ . The transfer function  $H_i(s)$  is represented in Figure 5.10, where we can observe that  $R_f$  plays the role of reducing the peak gain and moving the peak between two characteristic frequencies

$$f_A = \frac{1}{2\pi\sqrt{C_f(L_{f1} + L_{f2})}}, \qquad f_B = \frac{1}{2\pi\sqrt{C_f L_{f2}}}.$$
(5.8)

The two frequencies in (5.8) correspond to the extreme cases where  $R_f \rightarrow \infty$  and  $R_f \rightarrow 0$ , respectively, in equation (5.6).



Figure 5.10: Bode plot of the transfer function  $H_i$  in (5.6) associated with the output stage low pass filter of Figure 5.9, for different values of the resistor  $R_f$ , with  $C_f = 22 \,\mu\text{F}$  and  $L_{f1} = L_{f2} = 2.2 \,\mu\text{H}$ .



Figure 5.11: Proposed control scheme for the output current regulation (outer loop).

### 5.3 Outer loop: output regulation

In this section the outer loop (at the left of Figure 5.2) is analyzed, whose scope is to regulate the output current  $i_{bat}$  to a desired reference  $i_{ref}$  by selecting the proper value of  $\varphi$ . The value  $\varphi$  is determined through a PI controller with anti-windup (AW) feedback (block PI+AW in Figure 5.2).

The reasons behind the choice of the PI are: robustness, adaptability, and easy implementation in a prototype both for an analog or a digital solution since the operations that it requires are simple one: summation, multiplication and integration. The anti-windup should be considered when there is a saturation behavior. In our case, the control parameter  $\varphi$  is constrained to the set  $[0, \frac{\pi}{2}]$  from the control definition in Section 5.1. The limited range of  $\varphi$  can be modeled with the following saturation function

$$\operatorname{sat}(\varphi), \operatorname{dz}(\varphi) \xrightarrow{\frac{\pi}{2}} \varphi \qquad \operatorname{sat}(\varphi) := \begin{cases} \frac{\pi}{2}, & \text{if } \varphi \geq \frac{\pi}{2}, \\ \varphi, & \text{if } 0 \leq \varphi \leq \frac{\pi}{2}, \\ 0, & \text{if } \varphi \leq 0. \end{cases}$$
(5.9)

Saturation (5.9) can be integrated in the control loop by using the dead-zone function dz(u) := u - sat(u) in the anti-windup feedback [Tarbouriech et al., 2011]. The proposed PI+AW control scheme is presented in Figure 5.11, and its dynamical model is

$$\begin{cases} \varepsilon = i_{bat} - i_{ref}, \\ \dot{x}_c = \varepsilon - k_{aw} \, dz(\varphi), \\ \varphi = k_P \varepsilon + k_I x_c + \varphi_0, \end{cases}$$
(5.10)

where there are three gains to tune:  $k_P$ ,  $k_I$ , and  $k_{aw}$ . In brief,  $k_P$  controls the reactivity,  $k_I$  eliminates the static error and compensates for nonlinearities, and  $k_{aw}$  avoids the integral state  $x_c$  to explode when the computed control input is not applicable due to constraints on  $\varphi$ , which usually implies that it is not possible for the output current to reach the provided current reference.

Basically, the anti-windup function counters the increase of the integral term when the saturation element is active. Hence, if the saturation is not active, the controller acts as a standard PI. While, if it is active, the feedback signal coming from the saturation element acts on the integral part reducing its absolute value. In our case the proportional part speeds up the response to changes, the integral part compensates for the nonlinearity and cancels the static error, and  $\varphi_0$  provides an initial reference corresponding to low-amplitude-output to avoid starting the converter abruptly. The anti-windup feedback provides an improved behavior when the computed control  $\varphi$  exceeds its allowed range  $[0, \frac{\pi}{2}]$ . The anti-windup is also important for the implementation in a digital controller since it can avoid digital overflow of the register keeping track of the integral of the error  $x_c$  in (5.10).

Finding the proper set of gains  $(k_P, k_I, k_{aw})$  is not always an easy task. One thing that we can do is to try different combinations and observe the relative behavior, and adjust them until the desired

behavior is obtained. However, starting from scratch with no idea might be a time consuming task. Therefore, it might be good to have an initial guess from which the gains can be adapted in order to find the desired behavior. One possibility is to use LMIs to formulate a problem capable of considering the stability conditions and the fact that there is a saturation. In a general way, LMIs let us formulate a control analysis or design problem in a convex way, which can be resolved rapidly and efficiently [Boyd et al., 1994]. A similar procedure is what is proposed in [Doré and Zaupa, 2024] for the control of the RMS current in a SRC. In our case, the LMI formulation requires the dynamical model of the plant, i.e., the converter in Figure 5.6. We are going to see in the next section how we can obtain such a formulation.

### 5.3.1 Closed-loop description

At this stage, we would like to have a method to obtain a first guess of the gains  $(k_P, k_I, k_{aw})$ . To this end, we need a dynamic model for the plant, i.e., for what is between  $\operatorname{sat}(\varphi)$  and  $i_{bat}$ , which in our case, from Figure 5.6, is the resonant tank and the filter. Once we have a bare model of the plant, we can set up an LMI design procedure to have a first guess of the values of  $(k_P, k_I, k_{aw})$ . Let us consider some raw assumptions about the relationship  $\varphi \to i_{bat}$  in order to simplify it. The steady-state relationship can be approximated by a linear function of the form

$$i_{bat,ss} = i_{bat,max} - \nu\varphi, \tag{5.11}$$

where  $\nu = i_{bat,max} \frac{2}{\pi}$ , so that the amplitude is the maximum when  $\varphi = 0$ , and it is zero when  $\varphi = \frac{\pi}{2}$ . From the perspective of the dynamics, we consider that the dominant dynamics is the one of the filter in Figure 5.9, and that it can be described with a first order LPF with cut-off frequency  $f_B$  in (5.8):

$$\dot{i}_{bat} = -\frac{1}{\tau}(i_{bat} - i_{bat,ss}),$$
(5.12)

where  $\tau := \frac{1}{2\pi f_B}$ . Now, using the plant model in (5.11), (5.12) and the PI+AW dynamics (5.10), we can write the following approximated equation to describe the overall dynamics of the control scheme in Figure 5.2

$$\begin{cases} \dot{i}_{bat} = -\frac{1}{\tau} i_{bat} + \frac{1}{\tau} i_{bat,max} - \frac{\nu}{\tau} \operatorname{sat}(\varphi), \\ \dot{x}_c = \varepsilon - k_{aw} \operatorname{dz}(\varphi), \\ \varphi = k_P \varepsilon + k_I x_c + \varphi_0, \end{cases}$$
(5.13)

with  $\varepsilon = i_{bat} - i_{ref}$ . Moreover, let use consider that the value  $\varphi_0$  corresponds to the "ideal" reference  $\varphi_{ref}$  such that  $i_{ref} = i_{bat,max} - \nu \varphi_{ref}$ . Thereafter, we rewrite dynamics (5.13) in error coordinates considering  $\Delta_{\varphi} := \varphi - \varphi_{ref}$  and  $\dot{\varepsilon} = \dot{i}_{bat}$  assuming that  $i_{ref}$  is constant. With this change of coordinates, dynamics (5.13) can be written as

$$\begin{cases} \dot{\varepsilon} = -\frac{1}{\tau}\varepsilon - \frac{\nu}{\tau} \left(\Delta_{\varphi} - \mathrm{dz}(\varphi)\right), \\ \dot{x}_{c} = \varepsilon - k_{aw} \,\mathrm{dz}(\varphi), \\ \Delta_{\varphi} = k_{P}\varepsilon + k_{I}x_{c}. \end{cases}$$
(5.14)

To simplify notations, let us define  $q := dz(\varphi)$  and  $\zeta := \begin{bmatrix} \varepsilon & x_c \end{bmatrix}^\top$ , so that dynamics (5.14) can be expressed in the compact form

$$\dot{\zeta} = \underbrace{\begin{bmatrix} -1/\tau & 0\\ 1 & 0 \end{bmatrix}}_{A_{PI}} \zeta - \underbrace{\begin{bmatrix} \nu/\tau\\ 0 \end{bmatrix}}_{B_{PI}} \underbrace{\begin{bmatrix} k_P & k_I \end{bmatrix}}_{K} \zeta + \underbrace{\begin{bmatrix} \nu/\tau\\ 0 \end{bmatrix}}_{B_q} q - \underbrace{\begin{bmatrix} 0\\ 1 \end{bmatrix}}_{B_{aw}} k_{aw} q. \tag{5.15}$$

### 5.3.2 LMI-based design

Now, we want to build an LMI formulation that can consider all the constraints in order to design the gains  $(k_I, k_P, k_{aw})$  of the controller. The main objective is to ensure the stability of the closed-loop dynamics (5.15) with a given decay rate  $\alpha > 0$ . To this end, let us consider the nonnegative quadratic Lyapunov function  $V(\zeta) = \zeta^{\top} P \zeta$ , with  $P = P^{\top} \succ 0$ . Then, the stability and the decay rate are ensured if

$$\dot{V}(\zeta) = 2\zeta^{\top} P \dot{\zeta} < -2\alpha V(\zeta).$$
(5.16)

Since q is the deadzone nonlinearities, the scalar sector condition  $qw(\Delta_{\varphi} - q) \ge 0$  holds for every w > 0. Therefore, following the procedure in [Zaccarian and Teel, 2011, Sec 3.4.3], in order to guarantee the previous conditions, it is enough to check

$$2\zeta^{\top} P\dot{\zeta} + 2qw(\Delta_{\varphi} - q) + 2\alpha V(\zeta) < 0,$$

where  $\Delta_{\varphi} = K\zeta$ . This expression can be developed in an equivalent matrix form

$$2\begin{bmatrix}z\\q\end{bmatrix}^{\top}\underbrace{\begin{bmatrix}P(A_{PI}-B_{PI}K+\alpha I) & P(B_{q}+B_{aw}k_{aw})\\ wK & -w\end{bmatrix}}_{M}\begin{bmatrix}z\\q\end{bmatrix}<0,$$
(5.17)

which is equivalent to the bilinear matrix inequality  $\text{He}(M) \prec 0$  in the unknowns  $P \in \mathbb{S}^2$ ,  $K \in \mathbb{R}^{1 \times 2}$ ,  $k_{aw} > 0$ , and w > 0. Then, by multiplying it left and right by

$$\begin{bmatrix} S & 0 \\ 0 & v \end{bmatrix} = \begin{bmatrix} P^{-1} & 0 \\ 0 & w^{-1} \end{bmatrix},$$

and applying a change of variable, we obtain

$$\operatorname{He}\left(\begin{bmatrix} (A_{PI} + \alpha I)S - B_{PI}Y & B_qv + B_{aw}r\\ Y & -v \end{bmatrix}\right) \prec 0,$$
(5.18)

which is an LMI in the unknowns  $S \in \mathbb{S}^2$ ,  $Y := KS \in \mathbb{R}^{1 \times 2}$ , v > 0, and  $r := vk_{aw} > 0$ . Therefore, if LMI (5.18) is feasible, the linearized closed-loop system is stable. However, LMI (5.18) alone might lead to badly conditioned optimized selections of K, due to the fact that the spectral abscissa of  $A_{PI} - B_{PI}K$  may potentially grow unbounded for arbitrarily large values of K. Thus, we fix a maximum desired norm  $\bar{\kappa}$  for K and enforce the constraint  $||K|| \leq \bar{\kappa}$  through the following LMI formulation:

$$\begin{bmatrix} S + S^{\top} - I & Y^{\top} \\ Y & \bar{\kappa}^2 I \end{bmatrix} \succ 0,$$
(5.19)

stemming from the expression  $K^{\top}K \preceq \bar{\kappa}^2 I$  after applying a Schur complement and exploiting  $(S - I)(S^{\top} - I) \succeq 0$ . Additionally, we consider a constraint on the pole placement of the closed-loop, namely the eigenvalues of  $A_{PI} - B_{PI}K$  must lie in the circle centered in c with radius  $\rho$  in the complex plane. From [Tarbouriech et al., 2011, Section B.5.2], this constraint can be formulated with the following LMI:

$$\begin{bmatrix} -\rho S & (A_{PI} - cI)S - B_{PI}Y \\ S(A_{PI}^{\top} - cI) - Y^{\top}B_{PI}^{\top} & -\rho S \end{bmatrix} \prec 0.$$
(5.20)

To summarize, we have that the eigenvalues of the closed loop must lie in the left of the complex plane, LMI (5.18), and they must be inside a circle with radius  $\rho$  and center in *c*, LMI (5.20), as represented by the gray area in Figure 5.12.

To make our design robust, we consider that the parameters  $\tau$  and  $\nu$ , related to the maximum output current and cut-off frequency  $f_B$  of the filter in Figure 5.9, can vary in a range:  $\tau \in [\tau_{min}, \tau_{max}]$ 



Figure 5.12: Representation of the constraints imposed on the eigenvalues by the LMIs (5.18) and (5.20) in the complex plane. The eigenvalues should lie in the gray area.

and  $\nu \in [\nu_{min}, \nu_{max}]$ . These uncertainties on  $\tau$  and  $\nu$  can be easily taken into account by imposing LMI (5.18) four times, with the matrices  $A_{PI}$ ,  $B_{PI}$ , and  $B_q$  evaluated at the four corner of the polytope

$$\left(\frac{1}{\tau}, \frac{\nu}{\tau}\right) \in \left[\frac{1}{\tau_{max}}, \frac{1}{\tau_{min}}\right] \times \left[\frac{\nu_{min}}{\tau_{max}}, \frac{\nu_{max}}{\tau_{min}}\right].$$
(5.21)

Then, the gains can be found by solving the following feasibility problem with an LMI solver for a selected decay rate  $\alpha$ :

$$\begin{split} S \succ 0, \\ v > 0, \\ \mathrm{He} \left( \begin{bmatrix} (A_{PI,i} + \alpha I)S - B_{PI,i}Y & B_{q_i}v + B_{aw}r \\ Y & -v \end{bmatrix} \right) \prec 0, \\ \begin{bmatrix} X + X^\top - I & Y^\top \\ Y & \bar{\kappa}^2 I \end{bmatrix} \succ 0, \\ \begin{bmatrix} -\rho S & (A_{PI,i} - cI)S - B_{PI,i}Y \\ S(A_{PI,i}^\top - cI) - Y^\top B_{PI,i}^\top & -\rho S \end{bmatrix} \prec 0, \end{split}$$
(5.22)  
for all  $i = 1, 2, 3, 4,$ 

where  $A_{PI,i}$ ,  $B_{PI,i}$  and  $B_{q_i}$  are the matrices on the vertices of the polytope (5.21). The controller gains are then derived by

$$K = \begin{bmatrix} k_P & k_I \end{bmatrix} = YS^{-1} \quad \text{and} \quad k_{aw} = r/v.$$
(5.23)

The feasibility problem (5.22) can be transformed into an optimization problem if needed. For instance, we may want to minimize the norm of K, namely minimize  $\bar{\kappa}$ . Additionally, thanks to the LMI formulation, other conditions can be easily incorporated if necessary.

### 5.4 Final considerations

In this chapter we have discussed the key aspects in designing a dc-dc converter with a focus on a battery charger. Initially, we discussed how to simplify the analysis by modeling the LLC load as an equivalent resistor. Then we proposed and analyzed the low-pass output filter in charge of reducing

the ripple affecting the battery. Eventually, we moved to the control loops involved in the converter: an inner one ensuring the oscillation, and an outer one ensuring the output current regulation. The inner control loop is a novel self-oscillating control law, called mixed modulation, that overcomes the limitations of frequency and phase-shift modulation, by ensuring ZVS and a reduced frequency range in order to modulate the signal in the converter. The outer loop is eventually discussed, which consists of a PI with anti-windup feedback. An LMI-based technique is proposed as first step to choose the gains (proportional, integral, and anti-windup) of the outer controller. This chapter serves as an introduction to Chapter 6, where we delve into the experimental validation of our theory.

# 6

# Experiments with 3rd order LLC

In this chapter we present the experimental results related to the discussion in Chapter 5. Initially, the dc-dc converter prototype used for the validation is introduced in Section 6.1. Then we test the dc-dc converter experimental prototype in different conditions. First, we test the modulation control laws (frequency (3.2) and (3.5), phase-shift (4.2), and mixed (5.2)) alone in Section 6.2, i.e., the LLC resonant tank in Figure 5.6 is directly connected to a resistor. These tests let us have a validation of the behavior of the different modulation control laws in a third-order LLC resonant converter, whereas they have been introduced for second-order resonant converters.

Secondly, we test the whole dc-dc converter. Initially, we execute PSIM simulations to have a reference for the experimental results in Section 6.3. Then, we test the outer loop for current regulation described in Section 5.3 where the inner loop is running on the mixed modulation control law of Section 5.1. These test are carried out both on an electronic load in constant voltage mode and for a 48V battery, connected at the output.

The electronic load used for the measurements is the EA-EL 3400-25 from Elektro-Automatik, which can operate in four different modes: constant current (CC), constant voltage (CV), constant power (CP), and constant resistor (CR). The 48 V battery is composed of a series of 20 cells. Each cell is the EX-T30K from ELERIX, which is a Lithium Titanate Oxide cell with: capacity 30 Ah, nominal voltage 2.3 V, and voltage range 1.5 V to 2.9 V.

In the early stages of the testing phase, we preferred to work with the electronic load because we can impose limits on the current, voltage and power. Therefore, it is generally safer to operate with it rather than with a real battery. With the battery, there is the risk to overheat the cells or to go beyond the cell's voltage limits, which could result in failures or explosions. Moreover, the electronic load let us change easily the voltage, while it is harder in a battery that needs to be charged and discharged. However, the battery can be considered as a true constant voltage load, while the electronic load might have some interactions with the converter that could generate instability (the electronic load is a power converter itself).

The two objectives of this chapter are:

- Showing that modulation control laws for second-order resonant converters can be applied to third-order LLC resonant converter. At the same time, we can see the advantage of the mixed modulation control law with respect to frequency modulation, where both ensure ZVS but with a different frequency range.
- Showing that the output current can be regulated with a simple control scheme when using the mixed modulation to ensure the oscillating behavior.



Figure 6.1: Photo of the experimental prototype showing: the power stage with the resonant tank at the left, the rectifier at the right, and the FPGA at the top.

# 6.1 OBC Prototype design

The aim of the prototype realization is to test the different results that has been obtained in simulation. The design and the characterization of the complete prototype are detailed in Appendix C. Here, we report a condensed version with the main information useful for the simulation. With the reference to Figure 5.6, the requirements for the design are:

- Input voltage  $V_g$  equal to 48 V.
- Nominal output voltage  $V_{bat}$  equal to 48 V, in the range 40 V to 58 V.
- Frequency  $f_0 = \frac{1}{2\pi\sqrt{LC}}$  of the resonant tank 60 kHz.
- Maximum output current  $i_{bat}$  equal to 10 A.
- Maximum resonant voltage  $v_C$  equal to 100 V.
- Maximum output power  $W_{bat} = i_{bat}V_{bat} = 500$  W.

### 6.1.1 Electronic design

Recalling the scheme in Figure 5.1, there are three main circuits that need to be designed: the Hbridge, the resonant tank, and the rectifier. The H-bridge design was previously developed by us, and it is discussed in Appendix C, Section C.1. The remaining two stages that need to be designed from scratch are the resonant tank and the rectifier. In the following we give some basic details on their design focusing more on the overview avoiding discussing the details of the sensing circuits. The photo of the final setup that is used for the validation is shown in Figure 6.1 where we can see that there are three main boards: the H-bridge with the resonant tank, the rectifier, and the FPGA for the controller. More details are given in Section C.2 for the resonant tank and in Section C.3 for the rectifier. **Resonant tank.** For the resonant tank the electronic schematics is given in the left block of Figure 5.6. The resonant components are selected as

$$L = 10 \,\mu\text{H}, \quad C = 850 \,\text{nF}, \quad L_m = 35 \,\mu\text{H}.$$
 (6.1)

The inductor  $L_m$  corresponds to the magnetizing inductance of the transformer with transformation ratio 1:0.919. Therefore, we have a resonant frequency of  $f_0 = \frac{1}{2\pi\sqrt{LC}} = 54.6$  kHz (equivalently  $\omega_0 = 2\pi f_0 = 343 \cdot 10^3$  rad/s). The choice in (6.1) is partially constrained by the availability of the components. The inductor L is selected based on the commercial availability, therefore the capacitor C is selected to obtain the desired resonant frequency:  $C = (L\omega_0^2)^{-1}$ . The inductances ratio is  $l = \frac{L}{L_m} = 0.28$ , which implies that the open-load resonant frequency is  $f_1 = \sqrt{\frac{l}{1+l}}f_0 = 25.7$  kHz according to (1.22). In the resonant tank we need to sense  $i_C$  and  $v_C$  in order to implement the modulation control laws of Chapter 5. The sensing is done using two signal transformers – which reduce the amplitudes to a measurable range – and a passive circuit for the interface with the ADC on the FPGA as detailed in Section C.2.2.

**Rectifier and filter.** The rectifier board is composed of a full-wave rectifier with 4 Schottky diodes. The components in the output filter (Figure 5.9) have the following values:

$$C_f = 22 \,\mu\text{F}, \quad L_{f1} = 2.2 \,\mu\text{H}, \quad L_{f2} = 2.2 \,\mu\text{H}, \quad R_f = 0.33 \,\Omega$$

The two characteristic frequencies are  $f_A = 16.2 \text{ kHz}$  and  $f_B = 22.9 \text{ kHz}$  from (5.8), which are far enough from the frequency of the first harmonic of  $i_r(t)$ , which is around  $\approx 2f_0 = 109.2 \text{ kHz}$ . The rectifier board is equipped with two ADCs to sense the output current and voltage. At this stage we are mainly interested in the current, the voltage is sensed mostly for safety reasons. The detail design of the sensing circuit is discussed in Section C.3.3.

### 6.1.2 Control

The control-related part of the prototype is managed by the FPGA integrated in the development board *DE4 Stratix IV Development Board* from Terasic Inc. The details regarding the board and an extensive explanation of the code can be found in Appendix D. Here, we discuss the most important parts and aspects. The FPGA manages the two control loops operating in parallel:

- a. a first one that ensures the oscillation (inner loop in Figure 5.2) through the mixed modulation described in Section 5.1;
- b. a second one in charge of the output current regulation law (outer loop in Figure 5.2) described in Section 5.3.

Regarding the mixed modulation control, the current and voltage on the resonant capacitor C are sampled at the rate of 100 Msps. This allows us to avoid studying the equivalent behavior when the measurements are not continuous but sampled-data since the discrete behavior is *hidden* by the high sampling rate. We made this decision since it allows keeping a flexible and easy framework where we can test several control laws and adjust the parameters. Moreover, the same consideration in Section 3.4.1 about the effect of the delay applies here. The sampled values of current and voltage are then rescaled in order to compensate for the acquisition chain and obtain values proportional to  $x_1$  and  $x_2$ , which are used in the controller.

Regarding the PI controller, the output current is sampled at 100 kHz, which is the same frequency at which the controller is running (i.e., when we have the data we process it). When implementing the digital version of the PI we need to take care of the binary representation in order to avoid digital overflow. This is critical for the representation of the integral state  $x_c$  in (5.10) that could overflow the size of the assigned register when the input error  $\varepsilon$  stays constant, making  $x_c$  growing linearly with the time. In other words, the converter can provide a maximum output current  $i_{bat,max}$  when  $\varphi = 0$ . If the current reference exceeds  $i_{bat,max}$ , the PI controller tries to reach it with negative values of  $\varphi$ , which is not allowed, resulting in a constant error  $\varepsilon = i_{bat,max} - i_{ref}$ . This is where the anti-windup action proportional to  $k_{aw}$  in (5.10) plays an important role by reducing the integral term and preventing its indefinite growth.

The continuous-time controller of Figure 5.11 needs to be implemented on a digital device, in our case an FPGA. The main difference between the continuous-time and discrete-time version is in the integral part. The integral part can be implemented in a digital device considering different integration schemes. We decided to use the simplest one that is the explicit Euler scheme

$$x_c^{\ k} = x_c^{\ k-1} + T_{PI}\dot{x}_c^{\ k},\tag{6.2}$$

where the previous value of the integral  $x_c^{k-1}$  is summed with the input  $\dot{x}_c^k$  multiplied by integration period  $T_{PI}$ . The digital counterpart of the integrator is shown in right of Figure 6.2 where the multiplication by  $T_{PI}$  is moved after the integrator. The integral action is possible thanks to the unit delay block  $z^{-1}$  of Figure 6.2, that keeps the memory of the previous value with an update frequency  $f_{PI}$ .



Figure 6.2: Integral part of a PI controller. At the left there is the continuous model with the integral. At the right there is the digital counterpart that is integrating en Euler scheme for the integration. The frequency at which the integral is updated is  $f_{PI} = \frac{1}{T_{PI}}$ .

## 6.2 Modulation control laws applied to the LLC prototype

In this section we show that the frequency, phase-shift, and mixed modulation control laws introduced in Chapters 3 and 4 and Section 5.1, respectively, for second-order resonant converters can be employed in third order LLC resonant converters. In this setup, the LLC resonant tank of Figure 5.6 is connected directly to a resistor without any other stage. Essentially, the electronic circuit is equivalent to the one in Figure 5.8. The voltage and current amplitudes measurements are acquired for different values of the output resistor, with input voltage  $V_g = 24$  V. Ideally, we should find similar relationships to the ones in Chapters 3 and 4 and Section 5.1, remembering that in this case the resonant tank is a third-order LLC and not a second-order one.

Let us remark that for the following results we are showing the amplitude of the states  $x_2$  and  $x_3$ , which are directly related to the input and output current  $i_s$  and  $i_T$ , respectively.

Let us notice that an LLC inverter dynamics is described by three states  $(x_1, x_2, x_3)$ , but the modulation control laws (3.2), (4.2), and (5.2) use just  $(x_1, x_2)$  to compute  $\sigma$ . This difference implies that the three-dimensional dynamics in the space  $(x_1, x_2, x_3)$  is projected on the state-plane  $(x_1, x_2)$ , where the jump sets are defined as in (5.2).

### 6.2.1 Frequency modulation

In this section we test the frequency modulation control laws in the *z* and *x* planes from Chapter 3 for different values of  $\theta$  and of the load *R*. Figure 6.3 reports the results obtained with the control law (3.2) in the *z*-plane, while Figure 6.4 reports the results obtained with the control law (3.5) in the *x*-plane. For both control laws (3.2) and (3.5), the frequency increases, and the amplitude decreases as  $\theta$  decreases. We could argue that the frequency range with (3.2) in the *z*-plane (left of Figure 6.3a)



(a) At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes, for different values of  $\theta$  and R.



(b) States  $\sigma$  (red) and  $x_2$  (light blue) from the experimental prototype with  $R = 22.8 \Omega$ , for different values of  $\theta$ .



(c) Limit cycles in the *z*-plane for different values of  $\theta$  and  $R = 22.8 \Omega$ . The violet lines represent the jump sets.

Figure 6.3: Experimental results with the frequency modulation law (3.2) in the *z*-plane. At the top we observe the influence of the load, at the middle the waveforms involved in the converter, and at the bottom the state-plane representation for some selected values of  $\theta$ .

is lower compared to the frequency range with (3.5) in the *x*-plane (left of Figure 6.4a), but let us notice that the results from the two control laws do not reach the same minimum amplitudes (right of Figures 6.3a and 6.4a). In particular, in the *z*-plane the frequency modulation control law is not robust enough, from the experimental side, to ensure oscillations for low current and voltage amplitudes.

Therefore, the controller stops (i.e., the converter turns off) when  $\theta$  is small. The steep growth of the frequency can be better appreciated at the left of Figure 6.4a where for  $\theta = \frac{\pi}{2}$  we have frequencies higher of a factor 1.5 with respect to the resonant one. Conversely, the frequency trend at the left of Figure 6.3a seems to have a linear behavior, but let us recall that there are no measurements for small values of  $\theta$ , which would have probably shown the drastic frequency increase. About the frequency behavior, let us remark that the frequency, for both cases, drops below the resonant frequency. This is a third-order converter, therefore it is expected that the *real* resonant frequency changes in the range  $[\omega_1, \omega_0]$  (see Section 1.3), depending on the value of the load. Considering the waveforms reported in Figures 6.3b and 6.4b, resulting from the two frequency modulation control laws (3.2) and (3.5), respectively, ZVS is ensured for all the range of  $\theta$ . Having ZVS is confirmed by two things: first, the input current (proportional to  $x_2$ ) is positive when  $\sigma$  is toggled from positive to negative, and vice versa for the opposite case; secondly, the  $\sigma$  waveform is *clean*, in other words, the ringing is limited or not present (to have a rapid comparison, see Figure 6.5b where significant ringing is visible). From both Figures 6.3b and 6.4b, we can observe that as  $\theta$  decreases, the frequency increases and the waveforms contain more harmonics (i.e., they are *less* sinusoidal).

The representations of the limit cycles in the state-plane, in Figures 6.3c and 6.4c, show that the control law is actually switching in the right place. There is a small difference, but this can be related to the effect of noise and time delays.

A last consideration regarding the implementation of the two control laws is that the one in x-plane is more robust and flexible since we do not need to know the value of  $V_g$  and any scaled version of  $(x_1, x_2)$  is enough to run the controller, whereas the control law in the z-plane needs the knowledge of  $V_g$  in order to compute  $z_1$ . Nevertheless, this is not a big deal since usually  $V_g$  is known and constant.

### 6.2.2 Phase-shift modulation

In the phase-shift case, the FPGA executes the phase-shift control law of Chapter 4 and the results for different value of  $\varphi$  are represented in Figure 6.5. As foreseen in Chapter 4, at the left of Figure 6.5, the oscillating frequency remains almost constant for all the range of  $\varphi$  and its value depends on the load. The load dependency can be understood considering that the load makes the magnetizing inductance more or less important, i.e., the smaller the load the closer the oscillating frequency is to  $\omega_0$ , while the bigger the load the closer to  $\omega_1$ . The shift from  $\omega_0$  to  $\omega_1$  is evident in the transfer functions at the left of Figure 1.8 corresponding to a low factor *l*, that is the case of our converter with  $l = L/L_m = 0.28$ . Regarding the relationships between the amplitude and  $\varphi$ , as shown at the right of Figure 6.5a, they still preserve a pseudo cosine behavior but not as much marked as in the SRC case in Figure 4.2. In this case, ZVS is not ensured at any switching instant, as visible in the waveforms of Figure 6.5b, where the ringing of  $\sigma$  is clearly visible when the switch occurs when the current has the wrong sign. The only situation where ZVS is ensured is with  $\varphi = 0$  (which corresponds to the frequency modulation case with  $\theta = \pi$ ). For this special case, ZVS is ensured thanks to the dead-time characterizing the switching instants (more details are given in Section 2.2.1). ZVS is also ensured in half of the switches when the current has the correct sign and can discharge the parasitic capacitors. Therefore, there is ZVS only in 50% of the commutations when  $\varphi \neq 0$ .

The representations of the limit cycles in the state-plane, in Figure 6.5c, show that the control law is actually switching in the right place. There is a small difference that can be related to the effect of noise and time delays, mostly for lower amplitudes where the effect of the noise and uncertainty in the sensing chain are higher.



(a) At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes, for different values of  $\theta$  and R.



(b) States  $\sigma$  (red) and  $x_2$  (light blue) from the experimental prototype with  $R = 22.8 \Omega$ , for different values of  $\theta$ .



(c) Limit cycles in the *x*-plane for different values of  $\theta$  and  $R = 22.8 \Omega$ . The violet lines represent the jump sets.

Figure 6.4: Experimental results with the frequency modulation law (3.5) in the *x*-plane. At the top we observe the influence of the load, at the middle the waveforms involved in the converter, and at the bottom the state-plane representation for some selected values of  $\theta$ .



(a) At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes, for different values of  $\varphi$  and R.



(b) States  $\sigma$  (red) and  $x_2$  (light blue) from the experimental prototype with  $R = 22.8 \Omega$ , for different values of  $\varphi$ .



(c) Limit cycles in the x-plane for different values of  $\varphi$  and  $R = 22.8 \Omega$ . The violet lines represent the jump sets.

Figure 6.5: Experimental results with the phase-shift modulation law (4.2). At the top we observe the influence of the load, at the middle the waveforms involved in the converter, and at the bottom the state-plane representation for some selected values of  $\varphi$ .



(a) At the left there is the frequency normalized by  $\omega_0$  and at the right the  $x_1$  and  $x_2$  amplitudes, for different values of  $\varphi$  and R.



(b) States  $\sigma$  (red) and  $x_2$  (light blue) from the experimental prototype with  $R = 22.8 \Omega$ , for different values of  $\varphi$ .



(c) Limit cycles in the *x*-plane for different values of  $\varphi$  and  $R = 22.8 \Omega$ . The violet lines represent the jump sets.

Figure 6.6: Experimental results with the mixed modulation law (5.2) with  $\delta = 10 \text{ deg}$ . At the top we observe the influence of the load, at the middle the waveforms involved in the converter, and at the bottom the state-plane representation for some selected values of  $\varphi$ .



Figure 6.7: States  $\sigma$  (red) and  $x_2$  (light blue) from the experimental prototype with mixed modulation with  $R = 22.8 \Omega$  and  $\varphi = \pi/6$ , and for different values of  $\delta$ . As  $\delta$  increases also the frequency increases, and ZVS is ensured.

### 6.2.3 Mixed modulation

The last control law to be validated is the mixed modulation control law from Section 5.1. Different values of  $\delta$  have been considered to study both the influence of  $\delta$  and  $\varphi$ . Figure 6.6a contains the results obtained with  $\delta = 10 \text{ deg}$ : at the left, the frequency increases as the amplitude decreases, which happens in order to ensure ZVS; at the right, the amplitude decreases mostly in a pseudo linear way when the load is neither high nor low. Let us remember that in the LLC there is no such thing as "low" quality factor behavior as in second-order resonant converters, but, both for low and high loads, the amplitudes in the resonant tank (i.e.,  $x_1$  and  $x_2$ ) are high but with different oscillating frequencies. Unfortunately, no measurements have been carried out with smaller loads. In Figure 6.6b, we see that ZVS is maintained over the whole range of  $\varphi$ , except when the input current  $i_s$  (proportional to  $x_2$ ) is low. Achieving ZVS is harder when the current amplitude is extremely low, which is expected since the intensity of the current is not enough to discharge the MOSFETs' capacitors. One could argue that the frequency modulation laws were able to always maintain ZVS, but let us remark that the amplitude reached in the mixed modulation is smaller compared to the frequency modulation. Additionally, not having ZVS in these low current conditions is not too much problematic since a battery charger must be efficient fundamentally at large currents, where it spends most of its working time.

The representations of the limit cycles in the state-plane, in Figure 6.6c, show that the control law is actually switching in the right place. There is a small difference that can be related to the effect of noise and time delays, mostly for lower amplitudes where the effect of the noise and uncertainty in the sensing chain are higher. Moreover, we can observe that there is a small offset that is shifting the limit cycle, which is probably due to a bias in the sensing stage.

In Figures 6.8 and 6.7, we can observe the effect of the load and the input  $\delta$ . In Figure 6.7 we see different waveforms corresponding to different values of  $\delta$  with  $\varphi$  fixed to  $\frac{\pi}{6}$ : with  $\delta = 5 \deg ZVS$  is already ensured at an acceptable level. The larger  $\delta$ , the more time the capacitors have to discharge in order to have ZVS. The counterpart is that to ensure ZVS the frequency needs to increase to ensure a sufficient phase lag and the higher circulating current causes conduction losses. Figure 6.8 shows a different line for each value of  $\delta$ , and as  $\delta$  increases also the frequency increase, i.e., in order to have a higher frequency. At the same time, in the different columns of Figure 6.8 we can see that the load changes the frequency range. In the first row of Figure 6.8, the frequency approaches  $\omega_1$  for high loads, while for smaller loads it approaches  $\omega_0$ . In the second row of Figure 6.8, we can see that the



Figure 6.8: Experimental results with the mixed modulation for different values of  $\delta$  and R. The behavior of the frequency and the output current amplitude can be observed on the top and bottom row, respectively.

maximum output current amplitude that can be reached depends mainly on the load as the kind of relationship. If we had executed more measurements for lower loads, we could have noticed that the ratio  $\omega/\omega_0$  is approaching 1.

### 6.2.4 Some considerations

These first experimental results on the modulation control laws let us draw some considerations. First, the proposed modulation control laws can be applied also to third-order resonant converter with satisfactory results. The self-oscillating behavior is ensured, and a first explanation could be that the dynamics of the LLC and of the SRC are not so different. In other words, the projection in the  $(x_1, x_2)$  plane keeps the important properties in order to ensure the oscillations.

Regarding the different control laws, we can draw similar conclusions to the one formulated with the second-order resonant converters. In details:

- Frequency modulation of Chapter 3 enables ZVS at the cost of increasing the operating frequency drastically for lower amplitudes, which poses also problems to the controller since the delays becomes relatively more important with respect to the oscillating period.
- Phase-shift modulation of Chapter 4 ensures a constant frequency near the resonant one, which depends on the load, at the cost of losing ZVS for half of the commutations.
- Mixed modulation of Section 5.1 ensures ZVS and keep the frequency range limited.

In the end, we are going to employ the mixed modulation control law (5.2) in the tests with the current regulation, since it is the control law that presents the better properties. Let us remark that the main advantage of mixed modulation is to keep the frequency range limited, as shown in Figure 6.9. Moreover, Figure 6.9 shows that in the experimental prototype we can reach lower output current, which is not the case for the frequency modulation case.



Figure 6.9: Comparison between the frequency range of the frequency modulation (3.5) and of the mixed modulation (5.2) with  $R = 11 \Omega$  and  $\delta = 10 \text{ deg.}$ 

### 6.3 Battery charger – Simulation

So far, we have only seen results for second-order resonant converters. Here we see how the mixed modulation control law behaves when the resonant tank is an LLC. First, we estimate the actual range of the equivalent resistor  $R_{eq}$  in (5.5). From the specifications, we have a nominal battery voltage of 48 V and a charging current that can go from 0.5 A up to 10 A. Using (5.5), we find that the theoretical value of  $R_{eq}$  is between 4.6  $\Omega$  and 92  $\Omega$ . Let us remark that the estimate  $R_{eq} = 92 \Omega$  for the low output current situation in an overestimate since the ZCS behavior changes the waveform shape as shown in Figure 6.10. In detail, there is a non-negligible period of time when the output transformer current is zero. Therefore, the output average value is no more  $I_{peak} \frac{2}{\pi}$ , but it is lower. A better estimate can be obtained directly from the simulations (samples of the waveforms in Figure 6.10):  $R_{eq} \approx 70 \Omega$  for  $I_{bat} = 0.5 \text{ A}$ , and  $R_{eq} \approx 4 \Omega$  for  $I_{bat} = 10 \text{ A}$ .



Figure 6.10: Simulations of the OBC prototype that show the effect of ZCS on the waveforms for the two limit values of  $i_{ref}$ : at the left  $i_{ref} = 0.5$  A and at the right  $i_{ref} = 10$  A. In the first row there are the voltages  $v_T$  and  $V_{bat}$ , while in the second row there are the currents  $i_T$  and  $i_{bat}$ .



Figure 6.11: Simulation results of the PI controller applied to the circuit in Figure 5.6 obtained with PSIM. From the top to the bottom there is:  $i_s$ ,  $i_{bat}$ ,  $\varphi$ , and the frequency.

**Outer loop – current regulation.** We have simulated the full electronic system of Figure 5.6 with the control loops in Figure 5.2. The simulation is done using the software PSIM, which allows us to include the most common analog and digital electronic components. From the feasibility problem (5.22), we can find a first tentative values for the gains of the PI controller (5.10). Using the parameters  $\alpha = 1550$ ,  $\bar{\kappa} = 5000$ ,  $c = -150 \cdot 10^3$ , and  $\rho = 200 \cdot 10^3$ , and the polytope corresponding to  $\tau \in [6.95, 9.82]$  µs and  $\nu \in [\frac{2}{\pi}0.5, \frac{2}{\pi}10]$  A, the values of the gains are:  $k_p = 0.1$ ,  $k_i = 1853$ , and  $k_{aw} = 12$  We simulated the converter with a battery voltage of 48 V and the following gains:  $k_p = 0.183$ ,  $k_i = 1525$ , and  $k_{aw} = 12$ , which are obtained by trial and error starting from the ones obtained with the LMI feasibility problem. The result of the simulation is shown in Figure 6.11 for a simulation time of 10 ms where the initial reference is  $i_{ref} = 0.5$  A and at t = 5 ms it changes with a step to  $i_{ref} = 8$  A. Figure 6.11 shows at the top the input current  $i_s$ , on the second row we see how the output current  $i_{bat}$  reaches the given reference. In the last two rows of Figure 6.11 we see that  $\varphi$  decreases in order to have a higher output current, and the frequency increases as the output current increases.

### 6.4 Battery charger – Experiments

After the validation of the open-loop behavior, we discuss here the closed-loop one. We will not focus too much on the transient response of the PI controller but rather on the steady-state behavior. The PI controller ensures operating within a safe range, allowing us to set the desired output current. Moreover, as we have already mentioned, we are not focused on the actual performance of the PI controller, since we can make it easily faster than the dynamics involved in charging the battery. For



Figure 6.12: Transient response of the output current (green signal at the bottom) when there is a step in the current reference (from 1 A to 3 A) for different values of the gains  $\hat{k}_p$  and  $\hat{k}_i$ . The input current  $i_s$  is at the top in orange, and the output transformer current  $i_T$  is at the middle in magenta.

example, a settling time in the order of tens of milliseconds is much shorter than the time required to charge a battery or to change the charging profile, which is at least in the order of tens of minutes. For this application, it is sufficient that the output current reaches the desired reference value in a reasonable time.

This section analyses of the converter when the load is a battery, i.e., the output voltage is kept constant. With respect to the experiments without the rectifier, the waveforms change, e.g., the experiments in Section 6.2 are not characterized by ZCS, while with the battery there is ZCS in the rectifier and therefore the output waveform of the resonant tank are no more sinusoidal.

### 6.4.1 Transient response to a step change

We first analyze the behavior of the PI loop for different values of the proportional and integral gains,  $\hat{k}_p$  and  $\hat{k}_i$ , respectively, which are the gains used in the FPGA related to  $k_p$  and  $k_i$  through (D.4). Let us remark that the anti-windup is not implemented experimentally due to some unresolved numerical problems in the FPGA programming. Nevertheless, this is not a limitation as far as we are not providing a large current reference pulse larger than the maximum output current, which is not the case during the testing phase.

Figure 6.12 shows three different screen captures of the step response for different values of the gains  $\hat{k}_p$  and  $\hat{k}_i$ . The reference current  $i_{ref}$  has a step of 2 A, changing from 1 A to 3 A. The reference gains are:  $\hat{k}_p = 3/2^{14}$  and  $\hat{k}_i = 1/2^{16}$ ; which are used also for the measurements in the following sections. We have tested the converter by scaling up the gains by a factor 4 and by a factor 8. Looking at the output currents in Figure 6.12 (green waveforms) for the different gains,

as expected, the response is faster as the gains increases, but we lose robustness since the ripple is higher. What is happening is that the controller is too aggressive and over-compensate small errors by changing  $\varphi$  to abruptly, which results in a noisy output. In other terms, we would like to have that control input  $\varphi$  changing slowly without interfering with the dynamics of the converter.

### 6.4.2 Experimental results with the electronic load

Before delving into the case where the load is a real battery, we have done some test with an electronic load in constant voltage mode. Essentially, the electronic load is a power converter that can keep some physical quantity constant, in our case the voltage in order to simulate a battery at different charging conditions, i.e., output voltage levels. Doing the same with a real battery is more difficult since the battery needs to be charged and discharged, and this requires time. Moreover, for the initial testing the electronic load is safer and allows us to easily change the voltage. In our case we have executed measurements at half of the nominal values:  $V_g = 24$  V and  $V_{bat} \in \{20, 24, 29\}$ V.

The objective is to observe the different relation between the quantities in the converter: frequency, RMS<sup>1</sup> input current  $i_{s,rms}$ , output current  $i_{bat}$ , battery voltage  $V_{bat}$ ,  $\varphi$ , and  $\delta$ . Ideally, we expect to find similar relations to the find with the experimental test on the resonant tank alone, with the link that higher battery voltage  $V_{bat}$  corresponds to higher equivalent resistance  $R_{eq}$ .

The effect of  $V_{bat}$  can be observed in Figure 6.13. The frequency range is influenced by the battery voltage, and it is larger for lower voltage, as for the case with the resistive load. At the same time, in the left of Figure 6.13, the maximum output current that we can reach is limited by the battery voltage: the higher the voltage the lower the maximum current. One thing that is worth to remark is that the relationship between  $\varphi$  and  $i_{bat}$  is almost linear, as we modeled in a simplified way in Section 5.3.1. Therefore, this shows to us the experimental validity of the approximation (5.11).



Figure 6.13: Relationships between  $\varphi$ , frequency, and input RMS current and the output current  $i_{bat}$ . The results are obtained with an electronic load,  $V_g = 24$  V and  $\delta = 10$  deg.

Another interesting effect is the one of  $\delta$ . Let us recall that in our controller  $\delta$  is considered as a constant parameter, which is tuned based on the trade-off to ensure ZVS and keep the frequency range limited. Figure 6.14 shows us the joint effect of  $V_{bat}$  and  $\delta$  on the limits in terms of output current and oscillating frequency. These experiments have been executed with  $\varphi = 0$  in order to appreciate what happens when the current that the converter can deliver is at its maximum. As  $\delta$  increases, also the frequency increase (left of Figure 6.14) and at the same time the maximum output current decreases (right of Figure 6.14). This current-voltage relationship is expected since we have seen in Section 5.2.1 that the output current and voltage influence the value of the equivalent resistance  $R_{eq}$  in (5.5), which influences the response, as we have seen at the beginning of this chapter in Section 6.2. Moreover, the frequency-amplitude relationship can be understood in the frequency

<sup>&</sup>lt;sup>1</sup>Root Mean Square.



Figure 6.14: Operating limits of the resonant converter with respect to  $\delta$  considering  $\varphi = 0$ .

response of the LLC at the bottom left of Figure 1.8, where for an increasing frequency the amplitude is decreasing.

### 6.4.3 Experimental results with the 48 V battery

In the end, we took some measurements using a 48 V battery. Indeed, using a battery removed some problems that we were facing in terms of stability with the electronic load, mostly at the start-up. The measurements are performed at 48 V appreciating the effect of different values of  $\delta$ . Figure 6.15 shows similar relations to the one in Figure 6.14, where the frequency increases with  $\delta$  while the output current decreases.



Figure 6.15: Effect of  $\delta$  on the frequency and input current for different operating points. The results are obtained with a 48 V battery.

Figure 6.16 reports the signal when the current reference is 1 A for different values of  $\delta$ . First, we recall that  $\delta$  must be greater than zero to ensure ZVS, which is not the case in the top left of Figure 6.16. At the top of each screen capture we have the input current and voltage  $i_s$  and  $v_s$ , where we observe that the current is not sinusoidal. This is related to the fact that the amplitude is small, i.e. higher frequency that implies more harmonics in the signals. In Figure 6.17, where  $i_{ref} = 5 \text{ A}$ , the waveforms are more sinusoidal. We can observe that in both cases,  $i_{ref} = 1 \text{ A}$  and  $i_{ref} = 5 \text{ A}$ , the rectifier is operating with ZCS, which can be recognized observing that there is a period of time in which the rectified current  $i_r$  (magenta waveform) is zero. This means that the current  $i_s$  is flowing mostly through the magnetizing inductance and not through the secondary side of the transformer. Moreover, we can observe that the period of time during which  $i_r = 0$ , corresponds more or less at the period with  $\sigma = 0$ .

Regarding ZVS, let us emphasize again that  $\delta$  alone cannot ensure it, but the input current  $i_s$  and



Figure 6.16: Effect of  $\delta$  when  $i_{ref} = 1$  A. In each screen capture we can observe at the top the input current (yellow) and voltage (blue)  $i_s$  and  $v_s$ , while at the bottom there are the rectified current  $i_r$  (pulsating magenta) and the output current  $i_{bat}$  (pseudo-constant green)

the dead-time need to be considered. As an example, we can see that in the top right of Figure 6.16 for  $\delta = 5 \text{ deg}$  there is no ZVS, while in top right of Figure 6.17, with the same parameters but higher current, ZVS is ensured. As explained in Section 2.2.1, this is normal as a higher current discharge the parasitic capacitors faster, reducing the voltage across the switch more rapidly.

Settling of limit cycles Summarizing, we have observed also the settling of limit cycles in the resonant tank. Figure 6.18 shows different limit cycles for different values of the output reference current  $i_{ref}$ . At the start-up of the converter, i.e., when the trajectory is spiraling out of the origin, we can see the desired soft-start property induced by the control law in the state-plane, which pushes the trajectory to spiral out towards the limit cycles without abrupt changes or overshoots. Moreover, it does not take more than about ten revolutions to reach the limit cycle.

# 6.5 Final considerations

Overall, we are satisfied with the experimental results since they replicate what expected from the simulations. This motivates us to pursue this research direction. If  $\delta$  is properly chosen, ZVS is ensured for all the operating conditions, enabling better efficiency for the converter. Having a PI controller for the output current regulation is enough, allowing for an easy and robust implementation. We have been able to observe the desired properties of ZVS and ZCS. Moreover, the relationship  $\varphi$ -*i*<sub>bat</sub> is well approximated by a linear function, which support the approximation that we made in



Figure 6.17: Effect of  $\delta$  when  $i_{ref} = 5$  A. In each screen capture we can observe at the top the input current (yellow) and voltage (blue)  $i_s$  and  $v_s$ , while at the bottom there are the rectified current  $i_r$  (pulsating magenta) and the output current  $i_{bat}$  (pseudo-constant green)

Section 5.3.1. Nevertheless, the prototype presents some limitations in terms of performance. First, some components have not been properly selected and therefore their efficiency is low. In particular the resonant inductor and capacitors overheat when the current is high. Secondly, the maximum input current is limited to 10 A by the sensing in the resonant tank, which induces to a maximum output current of 6 A more or less. Third, it is hard for the controller to keep the oscillation when the amplitude is small since we enter a region where the signal to noise ratio is too low. Practically, the ADC and the numerical representation are not precise enough to guarantee a proper functioning of the state machine in the controller. Nevertheless, this is not a strong limitation since we are not interested in reaching such small amplitudes. However, all these limitations can be solved by changing a few components in the circuit and by adapting the design of the sensing circuits, which are not directly related to the proposed control laws. At this stage we are satisfied with the fact that the converter behaves as desired and predicted, this showing the effectiveness of the control laws.



Figure 6.18: Oscilloscope screen captures for different limit cycles in the  $(v_C, i_C)$  coordinates for four values of the reference current  $i_{ref}$ .

# **Concluding Remarks**

In this dissertation, we saw how control theory and power electronics can interact. In particular, we kept the focus on resonant power converters and how they can be controlled and used in a battery charger application. We tackled the problem from a control perspective at the beginning, by modeling second-order resonant converters with hybrid dynamical systems tools. This approach led us to discover a new way to ensure the oscillations in the converter, i.e., the existence of a globally asymptotically stable limit cycle. In detail, we took advantage of the state-plane representation of the trajectories to induce a desired self-oscillating behavior, i.e., the oscillating frequency is self-induced and not externally imposed. In the setting of state-plane-based control laws we proposed three different approaches with different characteristics:

- Frequency modulation that ensures optimal switching conditions (ZVS) for any operating point with the counterpart that the oscillation frequency needs to drastically increase when requiring small output amplitudes.
- Phase-shift modulation that ensures a constant switching frequency at the cost of losing ZVS.
- Mixed modulation that enables ZVS while trying to minimize the oscillating frequency, i.e., keeping it close to the resonant one.

We showed that ZVS can be easily enforced using a state-plane approach to control the resonant converter, the important thing being that the input current must be considered for the representation in the state-plane, since it is the input current that defines ZVS together with the input voltage.

The mixed modulation control law is the one adopted in the rest of the dissertation for the battery charger application. We observed how the mixed modulation control law behaves well when it is applied to a third-order resonant converter, the LLC. The result is that the desired ZVS property is maintained. Moreover, the LLC implementation allows for a further feedback loop of a PI controller to regulate the output current charging the battery, without the need to consider the nonlinearities. We concluded by validating the mixed modulation control law and a PI regulation loop on a prototype to charge a battery with constant current. The controllers have been implemented digitally in an FPGA, and the results are promising since the ZVS is maintained over all the range of output currents.

# Perspectives and Future Outlooks

Starting from this work there are many possible future directions, both from the control and the power electronic side. I think that is impossible to finish doing research on some topic, the more you know, the more directions to explore you discover.

### **Control-oriented perspectives**

Focusing on the control-related future perspectives there is a world that can be explored. First, there is not yet a stability proof for second-order resonant converters with the mixed modulation

control law. Then, we properly analyzed only second-order topologies, but the analysis of thirdorder or higher-order topologies is still open. With an order higher than two, the dynamics cannot be described completely on a state-plane, which opens new challenges that deal with limit cycles in a space of dimension 3 or more. More generally we can consider the problem of stability of limit cycles in hybrid systems, which is still an open problem. Some work in this direction are [Simic et al., 2002; Lou et al., 2023], yet there is much more to be done to answer the question: "Is there an equivalent of Poincaré-Bendixson theorem for hybrid systems?". The first challenge is to define the Poincaré map and the conditions for its continuity, the second one is how to assess if there exists a limit cycle and if it is stable. Additionally, if we consider the digital implementation in the FPGA, we are working with sampled and quantized data. Therefore, additional considerations could be done about the stability and robustness of the control [Ferrante, 2015]. The hybrid dynamical model analysis of the resonant converter could be enhanced including some practical aspects as the dead-time and the sampling.

### Power electronics-oriented perspectives

On the power electronic side, we can distinguish two types of possible extensions: on the theory or on the prototype. From the theory side, since the controller is digital, it would be reasonable to study the equivalent discrete-time controller. In our case, we assumed that the sampling frequency is high enough to ensure the required behavior. However, maintaining a sampling frequency as high as 100 Msps can be demanding. Therefore, reducing the sampling frequency is a reasonable effort that would also simplify the implementation. Considering a discrete controller could be represented through a hybrid dynamical system where the measurements are no more continuous but sampleddata. From the prototype perspective, there are several other interesting directions. First, the code running in the FPGA can be optimized, and it can be made more robust. In particular, the problems related to the numerical representation could be solved in a clean way, like anti-windup implementation and the sampling through the ADC board for the measurements in the resonant tank. Another interesting direction is how the modulation controllers (Chapters 3 and 4) are implemented. Is an FPGA necessary? Could an analog implementation be feasible? Or a low-cost microcontroller? These are some questions to which we can try to answer. As a preliminary answer we could say: maybe. If we consider the solution adopted in [Bonache-Samaniego, 2017], since the switching surface is a line lying in a quarter of the state-plane it can be uniquely represented by its slope. In our case, for the frequency modulation in the z-plane, the representation through the slope is not possible since the line is spanning a half plane (a singularity is encountered either at  $\theta = 0$  or at  $\theta = \pi/2$ ). Instead, for the phase-shift modulation case this approach could be feasible. The last case of mixed modulation lies in between the two: the line defined by  $\delta$  in Figure 5.3 can be represented by its slope, and the same applies to the one identified by  $\delta + 2\varphi$ , if the angle is always different from zero, i.e.,  $\delta > 0$ . Of course, an analog implementation would make the system stiffer compared to the flexibility of an FPGA, but once set up it would be cheaper by some order of magnitude. For the implementation in a low-cost microcontroller, the effect of the sampling and elaboration time should be considered. If we consider a standard microcontroller, the limits come from the combination of the number of cycles needed to evaluate an expression and the clock frequency, resulting in a long delay between the sampling and the update of the output. This problematic could be mitigated by considering microcontrollers that integrate some operations with special units with lower latency.

Finally, from an efficiency point of view, the components used for the circuits could be optimized. Starting from the resonant inductor that is supposed to work in DC, but it is working in AC. The resonant capacitors should be of class COG. The current sensing range should be increased in order to exploit the full capability of the converter. Indeed, currently the limitation in the resonant current sensing is limiting the maximum output current.

Appendices

# A

# Proofs of technical lemmas

## A.1 Proof of Lemma 3.4

To prove Lemma 3.4 let us recall the following definitions for convex functions The *subdifferential* is an extension of the gradient for nonsmooth convex functions.

**Definition A.1 (Subdifferential)** The subdifferential of a convex function  $f : \mathbb{R}^n \to \mathbb{R}$  at a point x is the set

$$\partial f(x) = \{ v \in \mathbb{R}^n | f(y) \ge f(x) + v \cdot (y - x) \ \forall y \in \mathbb{R}^n \}.$$
(A.1)

Each element of  $\partial f(x)$  is a subgradient of f at x.

Let us consider an example with the convex function f(x) = |x|: "what is the value of the gradient at x = 0?". The gradient is not defined but the subgradient is. Intuitively, the subgradient can take all the values of the slopes of the line that stays under the graph of f, i.e., the values inside the subdifferential, which in this case is  $\partial f(0) = [-1, 1]$ . For a graphical representation refer to Figure A.1.



Figure A.1: Convex function f(x) = |x| and representative lines supporting the graph of f at x = 0, whose slopes belong to the subdifferential  $\partial f(0)$ .

**Definition A.2 (Strongly Convex)** A function  $\psi$  is  $\alpha$ -strongly convex if  $x \mapsto \psi(x) - \alpha |x|^2$  is convex. From [Aravkin et al., 2017, Def. 5.1], a function  $\psi : \mathbb{R} \to \mathbb{R}$  is  $\alpha$ -strongly convex if and only if, for each  $a, b \in \mathbb{R}$ , it holds that

$$\psi(a) - \psi(b) \ge \sigma(a-b) + \frac{\alpha}{2} |a-b|^2, \ \forall \sigma \in \partial \psi(b),$$
(A.2)

where  $\partial \psi(b) \subset \mathbb{R}$  is the subdifferential of  $\psi$  at b.

Based on the strongly convex definition (A.2) we can prove the following lemma, which is instrumental for the proofs of Theorem 3.3 and Theorem 4.2. This lemma is useful to show that given a linear function and a strongly convex function, under certain conditions, they cross only one time. A graphical representation is given in Figure A.2. Let us recall here for clarity the statement of Lemma 3.4.
**Lemma A.1** Consider two continuous functions of the scalar variable  $\xi \in \mathbb{R}_{\geq 0}$ . A linear function  $\xi \mapsto \psi_1(\xi) = \psi_0 + \gamma \xi$ , with  $\psi_0, \gamma \in \mathbb{R}$ , and a strongly convex function  $\psi_2$  with  $\psi_2(0) < \psi_0$ . Function  $\xi \mapsto \psi_2(\xi) - \psi_1(\xi)$  grows unbounded as  $\xi \to +\infty$  and has exactly one zero for  $\xi \geq 0$ .



Figure A.2: Graphical representation of Lemma A.1.

**Proof.** Denote  $\tilde{\psi}(\xi) := \psi_2(\xi) - \psi_1(\xi)$  and note that it is strongly convex because, for each  $a, b \in \mathbb{R}$  and each  $\sigma \in \partial \psi_2(b)$ , it satisfies, from (A.2) applied with  $\psi = \psi_2$ ,

$$\tilde{\psi}(a) - \tilde{\psi}(b) = \psi_2(a) - \psi_2(b) - \gamma(a-b)$$

$$\geq \tilde{\sigma}(a-b) + \frac{\alpha}{2}|a-b|^2,$$
(A.3)

where  $\tilde{\sigma} = \sigma - \gamma$  characterizes any vector in the subdifferential of  $\tilde{\psi}$  at b.

Let us first prove that function  $\tilde{\psi}$  has at least one zero for  $\xi \in [0, +\infty)$ . From  $\psi_1(0) = \psi_0 > \psi_2(0)$ , we have  $\tilde{\psi}(0) < 0$ . Applying (A.3) at the unique global minimum  $\xi^*$  (wherein  $\tilde{\sigma} = 0$  belongs to  $\partial \tilde{\psi}(\xi^*)$ ), we have  $\tilde{\psi}(\xi) \geq \tilde{\psi}(\xi^*) + \frac{\alpha}{2}|\xi - \xi^*|^2$ , which proves that  $\lim_{\xi \to +\infty} \tilde{\psi}(\xi) = +\infty$ , showing unboundedness of  $\psi(\xi)$  as  $\xi \to +\infty$ . Moreover, with  $\tilde{\psi}(0) < 0$  and continuity, there exists at least one  $\xi_0$  where  $\tilde{\psi}(\xi_0) = 0$ .

Let us now prove that  $\xi_0$  is unique. Assume that there are two points  $0 < \xi_0 < \xi_1$  where  $\tilde{\psi}$  is zero and fix  $a = \xi_1, b = \xi_0$ . Then from (A.3) with these selections, we get:

$$0 > \tilde{\sigma}(\xi_1 - \xi_0) + \frac{\alpha}{2} |\xi_1 - \xi_0|^2, \tag{A.4}$$

which clearly implies  $\tilde{\sigma} < 0$ . Since  $\tilde{\sigma} \in \partial \tilde{\psi}(\xi_0)$  and  $\tilde{\psi}(\xi_0) = 0$ , by definition of subdifferential, using  $0 < \xi_0$ , we have  $\tilde{\psi}(0) \ge \tilde{\psi}(\xi_0) - \tilde{\sigma}\xi_0 = -\tilde{\sigma}\xi_0 > 0$ , which is a contradiction, because we proved above that  $\tilde{\psi}(0) < 0$ .

# A.2 Proof of Lemma 3.5

For the next lemma, an autonomous linear dynamical system of a damped oscillator of the type  $\dot{z} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & -\beta \end{bmatrix} z$  is considered. The energy of the system is defined as

$$E := \frac{1}{2}(z_1^2 + z_2^2).$$

The lemma tells us how the dissipated energy along trajectories can be expressed. The following result is a corollary of [Bisoffi et al., 2016, Lemma 1]. Let us recall here for clarity the statement of Lemma 3.5.

**Lemma A.2** Consider any solution z to  $\dot{z} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & -\beta \end{bmatrix} z$  flowing between two points from ordinary time  $t_1$  to ordinary time  $t_2 > t_1$  and define the energy-like function  $E(z) = \frac{1}{2}z_1^2 + \frac{1}{2}z_2^2 = \frac{1}{2}|z|^2$ . The dissipated energy  $E(z(t_2)) - E(z(t_1))$  is equal to  $\frac{\beta}{\omega_0}\Pi$ , where  $\Pi$  is the (unsigned) area hatched between the graph of the trajectory z(t),  $t \in [t_1, t_2]$  and the coordinate axis  $z_2 = 0$ .



Figure A.3: Representation of a trajectory and quantities involved in the proof of Lemma A.2.

**Proof.** Consider the following standard representation of the dynamical system  $\dot{z} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & -\beta \end{bmatrix} z$ 

$$\ddot{z}_1 + \beta \dot{z}_1 + \omega_0^2 z_1 = 0, \tag{A.5}$$

which represents a typical equation for a damped harmonic oscillator. Equation (A.5) resembles a typical spring-mass-damper mechanical system of a unitary mass subject to a viscous force  $\beta \dot{z}_1$  and an elastic force  $\omega_0^2 z_1$ . The energy is typically defined as the sum of the kinetic and potential components:

$$\widetilde{E} := \frac{1}{2}\dot{z}_1^2 + \frac{1}{2}\omega_0^2 z_1^2 = \frac{1}{2}\omega_0^2 (z_1^2 + z_2^2).$$
(A.6)

The dissipated energy is determined by the work done by the viscous friction  $F := \beta \dot{z}_1 = \beta \omega_0 z_2$ to move the unitary mass from a point  $z_A = z(t_1)$  to a point  $z_B = z(t_2)$ , causing a change  $\tilde{E}_B - \tilde{E}_A$ of the total energy. Let us explain it on a generic trajectory z(t) with the help of Figure A.3. Since trajectory z(t) crosses  $z_2 = 0$ , the work performed by the force F from a point  $z_A$  to  $z_B$  along trajectory z(t) can be expressed as function of  $z_1$  for each half-plane

$$\begin{split} \widetilde{E}_B - \widetilde{E}_A &= \int_{z_{A,1}}^{z_o} (-\beta \omega_0 z_2) \mathrm{d}z_1 + \int_{z_o}^{z_{B,1}} (-\beta \omega_0 z_2) \mathrm{d}z_1 \\ &= -\beta \omega_0 \int_{z_{A,1}}^{z_o} z_2 \mathrm{d}z_1 + \int_{z_o}^{z_{B,1}} z_2 \mathrm{d}z_1 = -\beta \omega_0 (\Pi_A + \Pi_B) = -\beta \omega_0 \Pi, \end{split}$$

where  $\Pi_A$  and  $\Pi_B$  are the upper and lower areas between the graph of the trajectory z(t) and  $x_2 = 0$ , respectively. Having defined the normalized energy as  $E(z) = \frac{1}{2}(z_1^2 + z_2^2) = \frac{\tilde{E}(z)}{\omega_0^2}$ , the dissipated energy can be expressed as

$$E(z(t_2)) - E(z(t_1)) = -\frac{\beta}{\omega_0} \Pi$$

In other words, the dissipated energy is proportional to the area defined by the graph of the trajectory.  $\hfill \Box$ 

# В

# **Concepts in Electronics**

# **B.1** Passive components

The next table summarizes the main features of three basic passive components.

	Resistor	Inductor	Capacitor
Symbol	R	L	С
Drawing			
Voltage-current relation	v(t) = Ri(t)	$v(t) = L \frac{\mathrm{d}i(t)}{\mathrm{d}t}$	$i(t) = C \frac{\mathrm{d}v(t)}{\mathrm{d}t}$
Laplace	R	sL	$\frac{1}{sC}$
Impedance	R	$_{j\omega}L$	$-\jmath \frac{1}{\omega C}$
Phase	0°	90°	-90°
Stored energy	_	$\frac{1}{2}Li^2$	$\frac{1}{2}Cv^2$
Dissipated energy	$Ri^2$	-	-

# **B.2** Power MOSFET

The power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a power semiconductor composed of several cells in parallel. The structure is vertical (current flow direction) rather than planar, and the gate length is around 1 µm. An equivalent model is represented in Figure B.1. The current is flowing between drain (D) and source (S), the gate (G) is used to control the turn-on and turn-off thanks to the gate-to-source voltage  $(v_{gs})$ . The main advantage of the MOS technology is the possibly high switching frequency since there is no charge to move. The switching frequency is limited by the parasitic capacitors:  $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ; represented in Figure B.1. More details can be found in [Erickson and Maksimović, 2020, Section 4.4].



Figure B.1: Equivalent representation of the MOSFET with the body diode and terminal capacitors.

# **B.3** Transformer model

The electric transformer is an electric machine able to efficiently change the voltage level, provide galvanic insulation of a portion of a circuit, and adapt the impedance. An electric transformer can be modeled by the equivalent circuit shown in Figure B.2, which considers the:

- Joule losses: *R*<sub>1</sub> and *R*<sub>2</sub>;
- leakage flux: *L*<sub>1</sub> and *L*<sub>2</sub>;
- magnetic reluctance (magnetic energy): *L<sub>m</sub>*;
- eddy current losses (core or iron losses):  $R_m$ .

The transformation ratio n is given by the number  $N_2$  of turns in the secondary winding over the number  $N_1$  of turns in the primary winding. Under ideal conditions, the input-output relationships can be condensed as follows:

$$n = \frac{n_2}{n_1}, \qquad v_{sec} = nv_{pri}, \qquad i_{sec} = \frac{1}{n}i_{pri}, \qquad Z_2 = n^2 Z_1;$$
 (B.1)

where Z stands for a generic (complex) impedance at the terminals of the primary or secondary side,  $Z_1$  or  $Z_2$ , respectively.

Two typical tests that are carried out with transformers: the open-circuit (no-load) and the short circuit ones. The first test lets us measure the magnetizing inductance, while the second test is used to measure the Joule losses. We used the open-circuit to measure the properties of our transformers. Let us remark that the model in Figure B.2 is linear, thus it does not consider effects like the magnetic saturation that might occur at high frequencies. Transformer saturation is determined by the applied winding voltage waveforms (Volts-seconds), rather than the applied winding currents as happens in the inductors.



Figure B.2: Electric transformer model.

#### Signal Transformers

We refer to *signal transformer* when a transformer is used to change the level of signals that are not transferring power, but rather an information. In our case, we used them for the sensing in the resonant tank.

When building a signal transformer, we can in general avoid considering the losses, since they are negligible to the low power level. What we have to consider is the transformation ratio n, and the number of turns that influences the magnetizing inductance. Typically, n is defined by the application, while the absolute number of turns depends on the desired value of the magnetizing inductance.

**Design** The design procedure follows some basic rules that can be found in [Erickson and Maksimović, 2020, Part III]. If we consider a toroidal core, its typical parameters are:

- $\Sigma l/A$  core constant;
- $l_e$  effective path length (average circumference for a toroidal core);
- $A_e$  effective cross-sectional area perpendicular to the magnetic path;
- $V_e$  effective core volume;
- $A_L$  inductance factor  $(L/N^2)$ .

The reluctance – corresponding to the inverse of the inductance factor – and the inductance associated with a winding are given by

$$\mathcal{R} = \frac{l_e}{\mu_0 \mu_r A_e} = \frac{1}{A_L}, \qquad L_m = \frac{N^2}{\mathcal{R}},$$

where N is the number of turns of the side where we are interested to model the inductance, the value of permeability in the vacuum is  $\mu_0 = 1.256 \times 10^{-6} \text{ N/A}^2$ , equivalently  $\mu_0 = 4\pi \times 10^{-7} \text{H/m} = 4\pi \times 10^{-4} \text{H/mm}$ . In brief:

$$L_m = \underbrace{\frac{\mu_0 \mu_r A_e}{l_e}}_{\text{fixed by the core}} N^2 = A_L N^2.$$

# Prototype design: schematics and details

This chapter considers the practical implementation of what is discussed in Chapters 5 and 6. The design of the resonant tank and of the rectifier are discussed, together with the sensing needed for the control to work. The reference specifications considered for the design are:

- Input voltage  $V_g$  equal to 48 V.
- Nominal output voltage  $V_{bat}$  equal to 48 V, in the range 40 V to 58 V.
- Frequency  $f_0 = \frac{1}{2\pi\sqrt{LC}}$  of the resonant tank 60 kHz.
- Maximum output current  $i_{bat}$  equal to 10 A.
- Maximum resonant voltage  $v_C$  equal to 100 V.
- Maximum output power  $W_{bat} = i_{bat}V_{bat} = 500$  W.

The control part is implemented in an FPGA, which provides the capability to process data faster than standard microcontrollers. The board is the *DE4 Stratix IV Development Board* from Terasic Inc. powered by the FPGA Stratix<sup>®</sup> IV GX with chip **EP4SGX230KF40C2**, which is equipped with plenty of general purpose input-output pin allowing flexibility in the implementation. The clock frequency can go up to 300 MHz.

**Tip** As a good practice, in electronic circuits, capacitors are inserted here and there. The main use cases are: decoupling capacitor to decouple parts of a circuit to reduce noise effect, mainly near power supply; coupling capacitor to connect parts and avoid let only the AC components pass through.

Recalling the schematic in Figure C.1, there are three main circuits that need to be designed: the power stage in Section C.1, the resonant tank in Section C.2, and the rectifier in Section C.3.



Figure C.1: Representation of the stages in the prototype.

# C.1 Power stage

The power stage includes the H-bridge with four MOSFETs and their drivers. The board was developed during my master internship. We report here only some key information to give an overview.



Figure C.2: Full-bridge configuration for the power stage.

**H-bridge**, some considerations. The H-bridge is composed of four switches with the task of inverting the polarity of the input voltage  $V_g$ , as illustrated in Figure C.2. The switches are power MOSFETs, in particular two power modules for the half-bridges, the APTC60AM242G from Microsemi<sup>®</sup>. The other essential components are the drivers, which enable the MOSFETs' turn-on and turn-off. The driver is the IR2110, which contains in a single chip the high-side and low-side driver. For the high side it uses a bootstrap operation. The components that need to be properly selected are the resistor at the gates, which control the turn-on and turn-off slopes. Generally speaking, what is usually placed in the bridge are snubber circuits to reduce the distortion during the switch, and freewheeling diodes for inductive kick in case of high-impedance loads (additional to the body diodes already integrated inside the MOSFET). We can notice in Figure C.3 that an additional diode has been put in antiparallel with each MOSFET is turned off. In our case, we used four HFA06TB120 that are ultrafast recovery diodes. They have a continuous forward current of 6 A (single pulse 80 A), and a reverse voltage of 1200 V.



Figure C.3: Driver circuit for one leg of the H-bridge. The red line is the path of the current that charge the bootstrap capacitor  $C_B$ .

**Driver and Bootstrap.** The schematic of the driver is presented in Figure C.3 for one leg of the H-bridge. For the other leg it is exactly the same, and it will correspond to the termination  $v_s(-)$ . The input signals HIN and LIN are directly connected to the output of the controller (the FPGA in our case). For each MOSFET, there is a 10 $\Omega$  gate resistance and two protection diodes. Each MOSFET is driven by a totem-pole driver. Therefore, for the low-side it is enough to provide a gate voltage higher than the ground (COM) voltage; while, for the high-side we need to provide a voltage higher than  $v_s(+)$  (vS). This is where the bootstrap capacitor  $C_B$  comes into play: it provides a higher gate voltage than vs when it is charged. So, in order to be able to activate the high-side MOSFET,  $C_B$  must be charged and this is done by closing the low-side MOSFET. When it is closed, we can observe in Figure C.3 (red line) the path through which the current follows from  $V_{CC}$  to ground through  $C_B$ . This current charges the bootstrap capacitor. If this does not happen, the high side cannot be turned on. Hence, at every start-up of the converter, we need to ensure the charging of the bootstrap capacitors in order to have the proper behavior. More details on the bootstrap operation can be found in [Mamadou, 2018].

# C.2 Resonant Tank

The core of an LLC resonant converter is the resonant tank, which is composed by an inductor L, a capacitor C and a transformer T (with magnetizing inductance  $L_m$ ), placed as in Figure C.4.



Figure C.4: Electronic circuit of the LLC resonant tank.

Once the choice of the resonant components is done, we need to measure the current and voltage in the capacitor C, which are used by the controller in order to ensure the oscillations through a self-oscillating control law. Since the waveforms are almost sinusoidal, or nevertheless AC, we decided to measure them with transformers that have the double role of isolating the resonant tank from the acquisition circuit and to step-down the voltage and current.



Figure C.5: Photo of the PCB of the resonant tank.

# C.2.1 Resonant Elements

To define the requirements of the components, and also for the sensing, we can reason at the resonant frequency, which is the operating condition where we have the highest amplitudes stressing the components. The reference specifications that we are considering for the design for a tank with a low rated quality factor are:

- maximum inductor current 15 A;
- maximum capacitor voltage: 100 V;

The main resonance frequency is defined as  $f_0 = \frac{1}{\sqrt{LC}}$ . The transformer has a transformation ratio of 1 : *n* with a magnetizing inductance  $L_m$ .

**Inductor** It has to be an AC inductor. The design procedure differs from more common DC inductors used in power converters. In our case, we do not have a constant bias current, but it is only subject to an AC current. The most important difference in the design is that for AC inductors we need to pay attention to the core losses, which are usually neglected in DC inductors, where the Joule losses are higher. Designing an AC inductor is similar to designing a transformer subject to a high-frequency AC component. A procedure is outlined in [Erickson and Maksimović, 2020, Section 15.4].

In our case, we opted for a off-the-shelf inductor, more suited for DC operations, but sufficiently good for a proof-of-concept prototype, where we are relatively interested in the efficiency. This is not the optimal choice, but it is complicated to find an off-the-shelf AC inductor respecting the design criteria. Therefore, we opted for a inductor from the AGP series of *Coilcraft*. The counterpart is that it heats up when the flowing current is high.

**Capacitor** For the choice of the capacitors we need to consider that the voltage and the current is high, which may result in high temperatures. For the voltage there are different ratings, while for the current we need to look at the thermal coefficient. In brief, the best ones to this scope are the ceramic capacitors with temperature coefficient C0G with SMD package. They have the lowest value thermal coefficient (namely it is zero) with low tolerance, and the capacitance value is almost insensitive to temperature variations.

**Tip** Common available SMD capacitors are the X7R but with high current they tend to overheat, that is why C0G or NP0 are the preferred choice. C0G and NP0 are the same class: C0G is defined in standard EIA-RS-198, while NP0 in IEC/EN 60384-8/21.

Transformer The transformer is hand-wound using litz wire, its functions are:

- isolate the downstream of the circuit, i.e. isolate source and load;
- adapt the voltage level if needed;
- introduce a magnetizing inductance that makes the resonant tank of the third order (better frequency response for the scope since boot operation is enabled).

# Selected components

The selected components are given in Table C.1. Let us remark that these components may not be the best efficiency-wise, but for proof-of-concept results, they are good enough. The frequency response of the resonant tank has been measured for four different resistive loads, and it is reported in Figure C.6.



Figure C.6: Bode diagram from the resonant tank designed with low quality factor. Measurements obtained from the prototype with different resistive load.

Table C.1: Components for the low Q resonant tank.

Symbol	Value	Code/Description
L	$10\mu\mathrm{H}$	AGP4233-103ME from Coil Craft
C	$850\mathrm{nF}$	×8 C1825x153KGRAC (100 nF @ 1000 V X7R)
$L_m$	$35\mu\mathrm{H}$	Hand-made transformer with ratio $1:0.919$

# C.2.2 Sensing in the resonant tank

The current and the voltage on the capacitor C are measured in order to close the loop and ensure the oscillations. Two sensing circuits need to be designed to measure  $i_C$  and  $v_C$  Since these are AC quantities, and we need to step down the voltage and the current, we decided to use signal transformers. They have the desirable properties of introducing reduced distortions and galvanically isolate the resonant tank from the acquisition board or the control logic<sup>1</sup>. Some general considerations to keep in mind are:

- every sensing circuit should have the least influence possible on the resonant tank, i.e. it should not add drain too much current or add parasitic elements like magnetizing inductances;
- the outputs of the sensing need to be interfaced with a BALUN circuit (see Figure C.7) embedded in the acquisition card;
- every sensing stage is connected through a SMA connector via a coaxial cable to the ADC board.

<sup>&</sup>lt;sup>1</sup>Indeed, the FPGA is connected to the resonant tank through the gate drivers of the H-bridge. Again, this is not a problem for a prototype and this can be easily solved by isolating the drivers of the MOSFETs.

# Interaction with the FPGA

Before going into the electric design, let us discuss the acquisition side on the FPGA, which is necessary for the following choice of the interface.

For the acquisition, we rely on the daughter board AD/DA Data Conversion Card that can be directly connected to the FPGA development board Altera DE4. The board is equipped with two AD9254, ADCs that can work up to 150 Msps with 14-bit resolution. The ADCs are interfaced with the external through SMA connector and a BALUN circuit. The electronic circuit from the board schematic is reported in Figure C.7.



Figure C.7: BALUN circuit in the daughter board. Source: board's schematics.

**Warning** The ADC polarity is internally inverted if we look at the schematics of the daughter board. This fact is managed from a software point-of-view.

**Remark C.1** The BALanced-UNbalanced (BALUN) is a circuit used to transform an unbalanced signal to a balanced one. The output voltage ( $v_{ADC}$ =ADC\_A\_IN\_P-ADC\_A\_IN\_N) is the double of the voltage on R8,  $v_{ADC}$ . We have a 49.9  $\Omega$  input parallel resistor (R8), which naturally calls for an 49.9  $\Omega$  input series resistance for impedance matching in the sensing circuit. As shown in Figure C.8. In this setting, the analysis is simplified since the voltage  $v_{ADC}$  at the input of the ADC corresponds to the voltage  $\tilde{v}_{ADC}$ before the 49.9  $\Omega$  series resistor. This is true as far as there is no filter in the middle, if for instance there is a capacitor in parallel to R8, the voltage  $v_{ADC}$  will be filtered with static gain 1.



Figure C.8: Representation of the voltages involved in the acquisition stage of the daughter card.

To summarize, we have that  $v_{ADC}$  has a range of 1 Vpp and a resolution of 14-bit. The scaling factor of the ADC is

$$\gamma_{\text{ADC},14} = \frac{2^{13} - 1}{0.5} = 16382,$$

which corresponds to a  $61 \,\mu\text{V}$  precision in the range from  $0 \,\text{V}$  to  $1 \,\text{V}$ .

**Scaling in the FPGA** For the control law, once we have the sampled version of the measurements, we need to scale them in order to have values that allow computing a scaled version of the state of the system  $(x_1, x_2)$ , denoted as  $(\bar{x}_1, \bar{x}_2)$ . From the real physical value to the digital value, there is an acquisition chain with some specific gains as depicted in Figure C.9. The ADC gain is  $\gamma_{ADC,14}$  and the gains to  $v_{ADC}$  are  $\gamma_{i_C}$  and  $\gamma_{v_C}$ , for the sensed current and voltage, respectively.

In theory, what we could do is to compensate for the acquisition chain gain to compute  $(v_C, i_C)$ and therefore  $(\bar{x}_1, \bar{x}_2)$ . From the practical side, we need to deal with this only with integer numbers while taking care not to go on overflow with the digital representation. Since a generic scaled version  $(\bar{x}_1, \bar{x}_2)$  is enough, we consider a common scaling gain  $k_{com}$  that is useful to increase the precision since the operations are done with integers. The gain  $k_{com}$  should be high enough to make the gains greater than the unit (the higher, the better the precision), and not too high in order to avoid overflow<sup>2</sup>. The resulting gains are:

$$\mu_{x_2} = \frac{k_{com}}{\gamma_v \gamma_{ADC,14}}$$
 and  $\mu_{x_1} = \frac{k_{com}}{\gamma_i \gamma_{ADC,14}} \sqrt{\frac{L}{C}}$ 

In case we need to scale also something related to  $v_S$ , we can use the following gain  $\mu_{V_g} = k_{com}V_g$ .



Figure C.9: Simplified acquisition chain for the measurements in the resonant tank. From the physical system to the FPGA where  $\bar{x}_1$  and  $\bar{x}_2$  are uniform scaled version of  $x_1$  and  $x_2$ .

**Remark C.2** (Scaling by  $V_g$ ) Let us notice that all the scaling factors with respect to  $V_g$  are not considered. This is possible since the control law can use any scaled version of the states  $(x_1, x_2)$  or  $(z_1, z_2)$ . Another way to see this is that they have been incorporated in  $k_{com}$ . The knowledge exact of  $V_g$  is needed only for the z-coordinates.

#### **Current Sensing**

A current-transformer is used to measure the current  $i_C$  and to ensure isolation. The proposed circuit is shown in Figure C.10. The primary current is reduced at the secondary according to the transformation ratio  $1 : n_i$ , which is then transformed to a voltage thanks to the resistor  $R_i$ . The best choice is to have the least number of windings at the primary, so that the magnetizing inductance, in series with the resonant tank, is negligible with respect to the resonant inductance  $L_r$ . At the output there is a LPF that is also acting as an impedance matching circuit. The static equation relating input current  $i_C$  and output voltage  $v_{R_i}$  is

$$v_{R_i} = \underbrace{\frac{1}{n_i} \frac{2R_{rcf}R_i}{2R_{rcf} + R_i}}_{\gamma_i} i_C \approx \frac{R_i}{n_i} i_C,$$

where the approximation is valid in the case  $R_i \ll 2R_{rcf}$ .





 $<sup>^{2}</sup>$ A conservative possibility to check this is to take the worst scenario and use it to find an upper bound. Another way is to simulate the behavior.

Table C.2: Values of the components in the current sensing circuit.

$n_i$	18	Maximum nominal peak current: 10 A			
$R_i$	$0.5\Omega$	Current range	$\pm 10 \mathrm{A}$		
$R_{rcf}$	$49.9\Omega$	$\gamma_{1} = 0.0298$	$f_{c} = \frac{\omega_{ref}}{\omega_{ref}} = 1.36 \mathrm{MHz}$		
$C_{rcf}$	$4.7\mathrm{nF}$	$\gamma_i = 0.0298$	$Jrcf = \frac{1}{2\pi} = 1.50$ WIIIZ		

The dissipated AC power<sup>3</sup> on  $R_i$  is approximately  $P_{R_i} \approx \frac{R_i}{n_i^2} \frac{iC_{,peak}}{2}$ . The equivalent resistance at the primary side is:  $R_{T1,eq} = R_i/n_i^2$ . From this simple consideration, we can understand that the resistance  $R_i$  should be small enough not to influence the downstream and the upstream, and to have minimum losses. The transfer function between the current  $i_C$  and  $v_{ADC}$  corresponds to a low-pass filter with gain  $\gamma_i$  and cut-off frequency  $\omega_{rcf}$ 

$$\frac{V_{ADC}(s)}{I_C(s)} = \gamma_i \frac{\omega_{rcf}}{s + \omega_{rcf}}, \quad \text{with} \quad \omega_{rcf} := \frac{1}{R_{rcf}C_{rcf}} \frac{R_i + 2R_{rcf}}{R_i R_{rcf}} \approx \frac{2}{R_{rcf}C_{rcf}}.$$

The selected values for the components are reported in Table C.2.

#### Voltage Sensing

To measure the voltage  $v_C$ , the circuit in Figure C.11 is used. In this case the voltage is stepped-down by resistive voltage divided by a factor of  $\frac{R_{pv2}}{R_{pv1}+R_{pv2}}$ . The signal transformer  $T_v$ , with ratio  $n_v$ : 1, provides galvanic isolation and reduces the voltage. The final stage ensures the impedance matching and filters high frequency noise. The static equation linking  $v_C$  to the voltage read by the ADC is

$$v_{T_v} = \underbrace{\frac{1}{n_v} \frac{R_{pv2}}{R_{pv1} + R_{pv2}}}_{\gamma_v} v_C$$

This relationship is true as far as the equivalent resistor at the primary of the transformer satisfies  $R_{T2,eq} \gg R_{pv2}$ , where  $R_{T2,eq} = 2R_{rvf}n_v^2$ .



Figure C.11: Resonant voltage sensing circuit.

Then, the output of  $T_v$  is connected to a SMA connector through a low pass filter with cut-off frequency  $f_{rvf} = \frac{1}{\pi R_{rvf}C_{rvf}}$ . The transfer function between the voltage  $v_C$  and  $v_{ADC}$  is

$$\frac{V_{ADC}(s)}{V_C(s)} = \gamma_v \frac{\omega_{rvf}}{s + \omega_{rvf}}, \quad \text{with} \quad \omega_{rvf} := \frac{2}{R_{rvf}C_{rvf}}$$

**Remark C.3** The initial idea was to test also a "high" quality factor resonant tank. Then, we abandoned it because a high Q implies a high voltage capacitor, which is hard to measure directly. In our prototype, with a "high" Q, the voltage is supposed to arrive up to 1000 V. Therefore, the signal transformer would require a high number of turns (hard to manually do it), which implies also a high magnetizing inductance. A not-tested idea to solve this problem is to implement the resonant capacitance C with a grid of capacitors,

 $<sup>^3 {\</sup>rm The}$  current  $i_C$  is an AC signal, so we should consider the RMS value for the power or the peak divided by  $\sqrt{2}$ 

$n_i$	20.6	Maximum nominal peak voltage: 60 V			
$R_{pv1}$	$8.2\mathrm{k}\Omega$	Voltage range: $\pm 100  \mathrm{V}$			
$R_{pv2}$	$1\mathrm{k}\Omega$				
$R_{rvf}$	$49.9\Omega$	$\gamma_v = 0.00517$	$f_{rvf} = \frac{\omega_{rvf}}{2\pi} = 1.36 \mathrm{MHz}$		
$C_{rvf}$	$4.7\mathrm{nF}$				

Table C.3: Values of the components in the voltage sensing circuit.

so that they act as a first step-down stage. e.g., if we consider a grid of  $5 \times 5$  capacitors the voltage is divided by a factor 5, that means we need to step down with the transformer 200 V - which implies 5 times less than the number of initial turns. It is suggested to keep the grid symmetric with an odd number so that we measure in the central line. We might think of some other configurations, the important part is to preserve the overall value of the equivalent capacitance, which must be C.

**Tip** It is really important to consider the magnetizing inductance of the signal transformer. Its effect should be negligible and to evaluate this we can consider the equivalent impedance at the resonance frequency:  $Z_{eq} = \omega_0 L_{m,T_v}$ . Essentially, the parallel resistance  $Z_{eq}//R_{T2,eq}$  must be higher than  $R_{pv2}$ .

#### Signal transformers

The signal transformer used to measure the voltage and the current on the resonant capacitor have been handcrafted in-house. For the current transformer, the core 5977000301 from Fair-Rite (black coating) is used with the following properties:

$A_L$ (nH)	$A_e \ (\mathrm{mm}^2)$	$\Sigma l/A \ ({\rm cm}^{-1})$	$l_e \ (\mathrm{cm})$	$V_e \ (\mathrm{cm}^3)$	diameter (mm)
1180±25%	12.9	2.29	29.5	380	12.7

The primary turns are 1.5, and they are obtained with a thick wire that needs to bear the input current. The secondary consists of 27 turns of a thin wire. The final transformation ratio is approximately 1 : 18.

For the voltage transformer, the core B64290L0618X038 from TDK (blue coating) is used with the following properties:

$A_L$ (nH)	$A_e \ (\mathrm{mm}^2)$	$\Sigma l/A~({ m mm}^{-1})$	$l_e \ (\mathrm{mm})$	$V_e \ (\mathrm{mm}^3)$	diameter (mm)
10700±30%	51.26	1.17	60.07	3079	25.3

The primary turns are 60 and the secondary ones are 3, both wound with a thin wire. The final transformation ratio is approximately 20 : 1.

For each transformer we measured the magnetizing inductance to see the frequency response properties. The results have been obtained with the *IET/QUADTECH 1910 Inductance Analyzer*, and are reported in Figure C.12. The current transformer presents stable properties all over the tested range, from 10 kHz to 1 MHz. In the voltage transformer  $T_v$  the inductance drops around 100 kHz, which is a sign of saturation. Therefore, we can consider that the transformer is operating in proper conditions up to 100 kHz. Let us remark that:  $L_m$  for  $T_i$  needs to be sufficiently low, because it is in series; while  $L_m$  for  $T_v$  needs to be sufficiently high, because it is in parallel.



Figure C.12: Measurements of the magnetizing inductance of the transformers  $T_v$  and  $T_i$  used for the voltage and current sensing in the resonant tank.

#### Sensing characterization

The gains in the acquisition chain are characterized with measurements with the oscilloscope for different operating points, which are reported in Figure C.13 with the result of a linear interpolation. The estimated gains using linear regression are:

$$\hat{\gamma}_i = 0.0303, \qquad \hat{\gamma}_v = 0.00496.$$

Some screen captures used for the measurements are reported in Figure C.14. Let us remark that the measurements for the signals are taken at the entrance of the DCC board, therefore they are multiplied by two in order to reconstruct the gains.



Figure C.13: Characterization of the sensors in the resonant tank. The solid line is the interpolating line obtained with least-square method.



Figure C.14: Oscilloscope's captures of the signals – real and measured – in the resonant tank. The real signal is the less noisy one:  $v_C$  in green and  $i_C$  in magenta. The measurements for the sensed one are taken at the entrance of the DCC board,  $v_{Csense}$  and  $i_{Csense}$ , blue and orange, respectively. The measurements at the top and at the bottom are taken for two different scenarios with respect to the amplitude and the waveform shape.

# C.3 Rectifier and output stage

At high level, the objective is to control the DC current charging the battery while ensuring galvanic isolation between the battery and the FPGA (ideally, the FPGA should be isolated from both battery and H-bridge). From the electronic perspective, the objective of this stage is to rectify and filter the AC output of the transformer T in Figure C.4, so that the output of the stage is a DC current with an acceptable ripple level going to the battery. An overview of the schematic is given in Figure C.15. The board is composed of: a power part with a diode bridge rectifier, and a third-order low pass filter; a sensing part with a voltage sensor, a current sensor, and ADCs for the interface with the FPGA. The photo of the board is shown in Figure C.16.



Figure C.15: Overview of the main power parts of the output stage: rectifier, filter and load.



Figure C.16: Photo of the PCB of the rectifier.



Figure C.17: Bode plot of the filter in the output stage for the values in Table C.4.

# C.3.1 Diode Bridge

The diode bridge rectifies the AC input current. The diodes used for the bridge should have a fast recovery, and they should tolerate the reverse voltage when they are not conducting. The suggested solution is to use Schottky diodes. The two important parameters for the choice are: the flowing current, and the maximum reverse voltage. On the other side, the parameters that are influencing the behavior are the threshold voltage and recovery time. The diodes need to be equipped with a heat-sink in order to dissipate the heat generated.

The diode bridge output current is a pulsating wave  $i_r(t) = I_r |\sin(\omega t)|$ , with average DC value  $\frac{2}{\pi}I_r$ . The diodes are subject to 50% of  $i_r(t)$  since for half period they are not conducting. In the end, the average forward current is equal to  $\frac{I_r}{\pi}$ .

The chosen diodes are the B20100 with the following specifications: average rectified current 20 A, reverse voltage 100 V, and threshold voltage in the range 0.75 V to 0.95 V.

# C.3.2 Filter

The filter is composed of one capacitor  $C_f$ , two inductors  $L_{f1}$  and  $L_{f2}$ , and a resistor  $R_f$ . The input is a pulsating wave and the filter has the objective to smooth the oscillation (reduce the ripple). Ideally, we would like to get rid of all the harmonics while keeping only the DC component. The modeling and description has been presented in Section 5.2.2. Here we report the TF between the input and output current when the voltage of the battery is constant

$$H_i(s) = \frac{R_f\left(1 + s\frac{L_{f1}}{R_f}\right)}{s^3 C_f L_{f1} L_{f2} + s^2 R_f C_f (L_{f1} + L_{f2}) + sL_{f1} + R_f},$$

The two characteristic frequencies are

$$f_A = \frac{1}{2\pi\sqrt{C_f(L_{f1} + L_{f2})}}, \qquad f_B = \frac{1}{2\pi\sqrt{C_fL_{f2}}}.$$

The selected components are reported in Table C.4. With these values, the two frequencies are  $f_A = 17 \text{ kHz}$  and  $f_B = 24 \text{ kHz}$ . The frequency response of  $H_i(s)$  is reported in Figure C.17. In this case we are not interested in the phase since our objective is to get rid of all the harmonics.

Symbol	Value	Code/Description
$C_f$	$22\mu F$	M108137228 (K 100)
$L_{f1}$ , $L_{f2}$	$2.2\mu H$	WE 7443762504022 from Würth Elektronik
$R_{f}$	$0.33\Omega$	Generic 5% precision resistor

Table C.4: Components for the filter in the output stage.

# C.3.3 Sensing in the rectifier

The last part considers the sensing of the output current and voltage,  $i_{bat}$  and  $V_{bat}$ , which are used by the PI controller in the outer loop (Figure 5.2). We need to sense DC values to close the loop. We measure the current that is the quantity that we want to regulate, and the voltage in order to have protection from overvoltage. One important requirement is that the sensing stage, equivalently the FPGA board, is isolated from the battery. This is ensured from the power side because the transformer  $T_r$  is used, and from the sensing side thanks to the choice of the sensors. To say it easy, we want to keep different grounds for the battery and for the FPGA. In this direction, the choice of the sensors is a Hall effect sensor for the current, and an isolated operational amplifier for the voltage. The outputs of the sensors are actively filtered with an Operational Amplifier (OPAMP) to reduce the noise. Finally, ADCs are used to transform the signals in digital ones, directly connected to the FPGA with a parallel interface.

#### **Output Current Sensing**

Technically, for the current, there are two isolated options: a Hall-effect sensor, or a shunt resistor with an isolated op-amp. The choice is a *Hall-effect sensor* since it does not require a power supply in the power side. Sensors from LEM provide this possibility, in particular the HO series. They are distinguished by the current range (6/10/25) and the supply voltage in the output side (3.3/5 V).

Our choice is the LEM H0 10P/SP33, which has a nominal current of 10 A with range  $\pm 25$  A and supply voltage of 3.3 V. The sensor characteristic from the datasheet is the following

$$V_{\rm out} = \gamma \cdot N \cdot I_p + V_{\rm ref}$$

where  $\gamma = 0.07667$  is a fixed gain, *N* is the number of turns, and  $V_{\text{ref}} = 1.65$  V is an offset which corresponds to half of the supply voltage. The connection schematic from the datasheet is shown in Figure C.18. The output of the sensor,  $V_{\text{out}}$ , is then conditioned with an OPAMP in differential mode, which removes the offset, amplifies the signal and filters it with a LPF.



Figure C.18: Operating principle of the HO x-P series from the datasheet.

**Tip** The LEM HO 10P/SP33 provides two ways to sense the current: 1. using a wire wrapped around the hole on it and the number of turns N is free; 2. using the pins on the socket, every couple corresponds to a winding, therefore they can be connected in parallel, i.e. N = 1; 3. following a configuration to reach up to N = 3.



Figure C.19: Sensing circuit for the output current  $i_{bat}$ .

The sensing circuit is depicted in Figure C.19 and the static relationship for the differential OPAMP is

$$v_{ADC,i_{bat}} = (V_{\text{out}} - V_{\text{ref}}) \frac{R_{if2}}{R_{if1}} = \underbrace{\gamma N \frac{R_{if2}}{R_{if1}}}_{\gamma_{i_{bat}}} i_{bat}$$

More into the details of the frequency response, the signal  $V_{out}$  is the one filtered by the LPF since the capacitor  $C_{if}$  is on its side. The cut-off frequency is

$$f_{if} = \frac{1}{2\pi} \frac{R_{if1} + R_{if2}}{R_{if1}R_{if2}C_{if}}.$$

The values of the components for the current sensing circuit are reported in Table C.5.

Table C.5: Components for the current sensing in the rectifier.

$V_{CC}$	$R_{if1}$	$R_{if2}$	$C_{if}$
$3.3\mathrm{V}$	$3.9\mathrm{k}\Omega$	$10\mathrm{k}\Omega$	$3.3\mathrm{nF}$

#### **Output Voltage Sensing**

The sensing in this case is done with an isolated OPAMP. A common component is the ACPL from Avago Technologies. The functioning is intuitive: from a higher level perspective it works as a differential OPAMP with a fixed gain; from a lower level perspective it integrates an ADC, so that the isolation is done at the level of the digital signal, which is then transformed to an analog one with a Digital-to-Analog Converter (DAC). The drawback is that there is the need of a power supply in the input side in order to operate the isolated OPAMP. The implemented electric circuit is shown in Figure C.20. It is composed of a voltage divider and a passive LPF on the input side, the isolated ACPL in the middle, and a differential amplifier integrating a LPF on the sensing side to reference the signal to ground.

The selected isolated OPAMP is the ACPL-790B-000E that has a fix gain of 8.2 with differential input and output, a High Gain Accuracy of  $\pm 0.5\%$ , and a bandwidth of 200 kHz. The supply voltage can be in the range 3V to 55V for the output side and 5V for the input side. From the design point of view, we need to consider that it has a limited input range  $V_{in+} - V_{in-}$  of  $\pm 200 \text{ mV}$ , and a non-negligible input resistance of  $27 \text{ k}\Omega$ .

**Remark C.4** Having an input resistance of  $27 \text{ k}\Omega$ , we cannot treat it as a standard high-impedance input operational amplifier.



Figure C.20: Sensing circuit for the output voltage  $v_{bat}$ .

In steady state condition – which is mostly the case if we are operating with a battery as load – and if  $R_{p2} \ll R_{vf} + R_{in}$ , the differential voltage  $v_{in,OA}$  in the input stage corresponds to

$$v_{\rm in,OA} = \frac{R_{p2}}{R_{p1} + R_{p2}} \frac{R_{in}}{R_{vf} + R_{in}} v_{bat}.$$

The cut-off frequency of the input filter is

$$f_{vf} = \frac{1}{2\pi} \frac{R_{vf} + R_{in}}{R_{vf} R_{in} C_{vf}}.$$

In the middle stage we have the relationship  $v_{\text{out,OA}} = 8.2v_{\text{in,OA}}$ . In the output stage the differential OPAMP has a static relationship and a cut-off frequency of

$$v_{ADC,v_{bat}} = \frac{R_{v2}}{R_{v1}} v_{\text{out,OA}} \quad \text{and} \quad f_{vo} = \frac{1}{2\pi R_{v2}C_v},$$
  
respectively. The total chain gain is given by  $v_{ADC,v_{bat}} = \underbrace{\frac{R_{p2}}{R_{p1} + R_{p2}} \frac{R_{in}}{R_{vf} + R_{in}} 8.2 \frac{R_{v2}}{R_{v1}}}_{\sim} v_{bat}.$  The

values of the components for the voltage sensing circuit are reported in Table C.6.

Table C.6: Components for the voltage sensing in the rectifier.

$R_{p1}$	$R_{p2}$	$R_{vf}$	$C_{vf}$	$R_{v1}$	$R_{v2}$	$C_v$
$47\mathrm{k}\Omega$	$180\Omega$	$3.3\mathrm{k}\Omega$	$1\mathrm{nF}$	$10\mathrm{k}\Omega$	$12\mathrm{k}\Omega$	$1\mathrm{nF}$

**ACPL supply.** The voltage sensor needs to be powered from both sides. On the output side it is powered-up by the 3.3 V as the other integrated circuit (IC)s. On the input side it requires a 5 V supply. To ensure the power supply we have two possibilities: take the battery voltage and stabilize it through a linear regulator, or use an external supply. The first option is preferred in an integrated solution since it requires less external components, while the second option is preferred for testing since there is power supply is independent of the load. If we consider the battery, the drop voltage will be high, i.e. we are reducing to 5 V an input voltage which can be as high as 60 V. The adopted solution is the use the IC ZXTR2105FF, which allows a maximum input voltage of 60 V and regulates to 5 V. Bypass capacitors of 1  $\mu$ F and 10  $\mu$ F are suggested. The schematic is given in Figure C.21. For flexibility, the choice between battery voltage and an external supply is possible through a jumper on the board.



Figure C.21: 5V linear voltage regulator on the battery side.

**Characterization** Both sensors have been characterized by providing a constant DC input at the rectifier board. We took measurements for different levels, the results are reported in Figure C.22. The interpolating lines have been found by using the least square method since we know that the underlying relationship is linear. The resulting slopes (gains) are

$$\hat{\gamma}_{i_{bat}} = 0.1199$$
 and  $\hat{\gamma}_{v_{bat}} = 0.01932$ 



Figure C.22: Characterization of the sensors in the rectifier. The solid line is the interpolating line obtained with least-square method.

#### Analog-to-Digital Converter

The selected ADC is the AD7822 from Analog Devices, which is an 8-bit half-flash ADC with conversion time of 420 ns, a parallel interface, and a single-ended input. The AD7822 can be supplied with 3 V or 5 V, with a corresponding input signal range of 2 Vpp or 2.5 Vpp, respectively.

The interface with the FPGA is relatively easy and straightforward. The available logic signals are:

- DB0 to DB7 for the output data;
- CONVST to start the conversion;
- EOC to signal the end-of-conversion;
- RD signal that change the output buffer state to high-impedance;
- $\overline{\text{CS}}$  chip select needed when the data bus is shared;
- PD power-down pin to turn the ADC off.

The 8-pin of the data bus can be connected directly to the pin of the FPGA. The clock signal is given to the pin  $\overline{\text{CONVST}}$ , and the  $\overline{\text{EOC}}$  pulse can be latched with  $\overline{\text{RD}}$  since the interface is with a gate

array. Both  $\overline{\text{CONVST}}$  and  $\overline{\text{EOC}}$  need to be connected through a 1 k $\Omega$  resistor to the FPGA. In our case we connect  $\overline{\text{CS}}$  to the ground since the data bus is not shared, and  $\overline{\text{PD}}$  to the supply since we want it always ON. A general connection scheme is shown in Figure C.23



Figure C.23: Circuit for the connection of one ADC in the rectifier board.

# C.4 Electrical circuits summary

This section collects the electrical circuits of the resonant tank and rectifier PCB. Figure C.24 reports the resonat tank circuit with the sensing, while Figure C.25 reports the rectifier and filtering circuit with the relative sensing.



Figure C.24: Circuit of the resonant tank board in Figure C.5.



Figure C.25: Circuit of the rectifier board in Figure C.16 (except for the ADCs).

# FPGA – code

**Disclaimer.** The author is not an expert on Verilog programming and more in general in HDL programming. Therefore, if for some strange reason you are reading this: take care, there might be errors and, for sure, there is a better, more robust and more efficient way to do it. Yet, this is working in our prototype, and can work as an initial reference.

Verilog is Hardware Description Language (HDL) code, which has the duty to describe the structure and behavior of electronic circuits, like in ASICs<sup>1</sup> and FPGAs. Programming in Verilog is like to imagine a digital electronic circuit – made of logic ports, multiplexers, flip-flop, etc. – and code it in a formal way by writing the desired connections and timing requirements.

In Section D.1 the basics of Verilog coding are recalled. Section D.2 describes the TOP file with the instantiation of the necessaries modules, which are reported in the sections afterwards. Section D.3 contains the modules related to the control: frequency, phase-shift, and mixed modulation and PI controller. Last, Section D.4 describes the modules used for signal processing.

# D.1 Preliminaries on Verilog

When coding in Verilog, the code can be split in blocks called *modules*. Each module performs a specific function that can instantiated multiple times and that can take parameters. Essentially, from a programmer's perspective, it is like a standard function in C, while from an electronic perspective, it resembles a multi-purpose integrated circuit.

In each Verilog project we find the TOP file that refers to the "top-level" file of a hardware design. The top-level module is the entry point of the design hierarchy, which typically instantiates all other lower-level modules. The functions of a TOP file are:

- connecting all the instances of the submodules and defining the overall structure;
- declaring the input and output ports that interface with external signals.

# D.1.1 Data Types

All data types can take only one of the following four value

- 0 logic zero / false 1 logic one / true
- x unknown (0 or 1) z high-impedance state

<sup>&</sup>lt;sup>1</sup>ASIC: Application-Specific Integrated Circuit.

The data types used in this project are:

- Net: it is created with the command wire. A net is used to connect *hardware* entities; therefore, it does not store any value. i.e., a net is like a copper wire. wire is used for input and output of modules and with the command assign: assign a = b & c
- Variable: a variable is an abstraction of a data storage that stores and holds values. It is declared using the command reg. A physical example is a flip-flop, or more in general a memory element like a register. reg: values can be assigned with procedural blocks (always, initial, <=) but not with continuous (assign) because reg is capable of storing and does not require to be driven continuously.</li>
- Integer: it is a general purpose variable of 32-bit.

# D.1.2 Operators

The basic operators are:

&&	&	and	*	mul	===	equal, including x and z
		or	/	div	!==	not equal, including x and z
!	~	not	%	mod	==	equal, can be unknown
	^	xor	**	pow	!=	not equal, can be unknown

Additionally, the shift operator allows to shift the bits in a variable or wire to the left or to the right

- logical shift << or >> that adds trailing zeros;
- arithmetic shift <--- or >>> that keeps the sign bit.

An example of how it is working:

data = 10101  $\rightarrow$  data << 1 = 01010 data >> 1 = 01010 data << 2 = 10100 data >>> 1 = 11010

Let us recall that a shift to the left on n positions ( <<n) corresponds to the arithmetic operation of multiplication by  $2^n$ . Conversely, a shift to the right by n positions ( >>n) corresponds to a division by  $2^n$ . Indeed, shift operator is a really low cost (in terms of logic) operation with which we can perform division operation. Other operators are:

- Conditional operator: assign out = <condition> ? <if\_true> : <if\_false>.
- Replication: { y, y, y } = { 3{y} }.
- Concatenation: with curly brackets  $\{ \} \rightarrow \{a, b, c[1:0], 2'b00, \{2\{a\}\}\}$ .

**Tip** Algebraic operations have priority over logic operations. Therefore, A+(B+C)>>3 is equivalent to (A+(B+C))>>3, which is different from A+((B+C)>>3).

# D.2 TOP file

Here we present the TOP file used for the closed-loop that runs the mixed modulation control law, and offers the possibility to operate in open-loop (by choosing  $\varphi$ ) or closed-loop ( $\varphi$  is selected by the PI controller). In both cases, the parameter  $\delta$  can be manually changed. For the sake of simplicity, we are not reporting the complete file but a condensed version with the most relevant parts. The complete documentation and project can be found in the GitHub repository [Zaupa, 2024]. This TOP file contains the instantiations of the modules of the mixed modulation controller, the PI controller, the ADCs, and the turn on procedures. The program flow can be defined as follows:

- 1. the voltages and currents are sampled with the ADCs;
- 2. the parameters  $\varphi$  and  $\delta$  are determined either through the interface or by the PI controller;
- 3. the hybrid control compute  $\sigma$  and eventually the signal for the MOSFETs' drivers;
- 4. the dead-time is applied to the signal going to the drivers.

There is a part of code that manages the startup since a particular sequence of operation must be executed to ensure a proper behavior:

- the bootstraps capacitors are charged (bootstrap details in Section C.1) [signal ENABLE];
- $\sigma$  is forced to be 1 in order to charge the resonant elements [signal ON];
- then  $\sigma$  is determined by the hybrid control law [signal VG].

The sequence is represented in Figure D.1. The values of the intervals have been chosen on the base of the electronic circuit: 10 µs is more than enough to charge the bootstrap capacitors, and 4 µs is more or less one quarter of period with respect to the resonant frequency. From a state-plane point of view, the time to charge the resonant components is necessary to move the trajectory out of the origin. Therefore, this stage provides a proper initialization of the physical systems respecting the theoretical consideration that we should avoid the origin since it is a weak equilibrium.



Figure D.1: Sequence of the signals at the startup to ensure a proper turn on.

```
1
  11
        SWITCHES :
  11
           SW[0] --> ENABLE CONVERTER
2
3
  11
            SW[2] --> open-loop or closed-loop
  11
4
        BUTTONS:
  11
           BUTTON[0] --> reset angles
5
  11
            BUTTON[1] --> increase phi
6
                                       5deg
  11
            BUTTON[2] --> decrease phi
                                       5deg
7
            BUTTON[3] --> increase delta 1deg
8
  11
            CPU_RESET --> reset CPU and delta
9
  11
10
   module TOP_HybridControl_CL (
11
     //-----
12
     // PORT declarations
13
14
     //clock + reset
15
     input CPU_RESET,
16
     input
           OSC.
17
     //ADC
18
           signed [13:0] ADB_DATA,
     input
19
           signed [13:0] ADA_DATA,
20
     input
                   ADA_OR,
21
     input
                   ADB_OR,
22
     input
23
     inout
                   AD_SCLK,
                   AD_SDIO,
24
     inout
25
     output
                   ADA_OE,
                   ADA_SPI_CS,
     output
26
                   ADB OF.
27
     output
                   ADB_SPI_CS,
28
     output
                   FPGA_CLK_A_N,
     inout
29
30
   inout
                   FPGA_CLK_A_P,
```

```
FPGA_CLK_B_N,
31
    inout
                    FPGA_CLK_B_P,
      inout
32
      input
                    ADA_DCO,
33
      input
                    ADB_DCO,
34
      // ADCs 8bit
35
      input [7:0] ADC_BAT_V,
36
                  ADC_BAT_V_CONVST,
37
      output
                  ADC_BAT_V_EOC,
38
      input
      input [7:0] ADC_BAT_I,
39
                 ADC_BAT_I_CONVST,
40
      output
41
      input
                  ADC_BAT_I_EOC,
      //output
42
43
      output [3:0]
                   Q,
      //debug
44
45
      input [3:0] SW,
      input [3:0] BUTTON
46
47
   );
48
   49
50
   // REG/WIRE declarations
52
53
  // clock signals
54 wire clk_1M, clk_100M, clk_100k;
55 // signal for the MOSFETs
56 wire ENABLE, ALERT, Q1, Q2, Q3, Q4, ON, VG, ENABLE_RST;
57 wire [3:0] MOSFET, button, sw;
58 reg VG_PREV;
59 // ADCs
   reg [13:0] vC, iC;
60
   reg [7:0] ADC_Vbat, ADC_Ibat;
61
62 wire [7:0] Vbat_DEC, Ibat_DEC;
   // PI controller
63
64 wire [31:0] Ibat_mA, Ibat_mA_filt, Iref_dA, error;
65 wire [31:0] phi, delta, phi_HC;
66 wire [31:0] phi_PI, phi_PI_tmp, phi_PI_sat, phi_PI_dz;
67 // H-bridge control and startup
68 wire [7:0] cnt_startup;
69
   70
71 // Structural coding
assign ENABLE = sw[0];
73
74
75 // tank ADCs clocks
76 assign FPGA_CLK_A_P = clk_100M;
77
   assign FPGA_CLK_A_N = ~clk_100M;
78 assign FPGA_CLK_B_P = clk_100M;
79 assign FPGA_CLK_B_N = ~clk_100M;
80
   // rectifier ADCs clocks
   assign ADC_BAT_V_CONVST = clk_100k;
81
82 assign ADC_BAT_I_CONVST = clk_100k;
83
  // assign for ADC control signal
84
  assign AD_SCLK = 1'b1; // (DFS) Data Format Select: 1 -> twos complement
85
           _____ = 1'b0;
ADA_OE - '
                              // (DCS) Duty Cycle Stabilizer
86
   assign
           AD SDIO
                              // enable ADA output
87
   assign
88 assign ADA_SPI_CS = 1'b1; // disable ADA_SPI_CS (CSB)
89 assign ADB_OE = 1'b0; // enable ADB output
   assign ADB_SPI_CS = 1'b1;
90
                              // disable ADB_SPI_CS (CSB)
91
   // --- assign for the H-bridge ---
92
   assign ALERT = \sim((Q1 \& Q3) | (Q2 \& Q4)); // check if there is a short circuit
93
94
   11
                     normal
                                  boot-strap
                                               force sigma=1
   assign Q[0] = ( (Q1 & ON & VG) | (1'b0 & ~ON) | (1'b1 & ON & (~VG)) ) & ENABLE & ALERT;
95
   assign Q[1] = ( (Q2 & ON & VG) | (1'b0 & \simON) | (1'b0 & ON & (\simVG)) ) & ENABLE & ALERT;
96
   assign Q[2] = ( (03 & ON & VG) | (1'b1 & ~ON) | (1'b0 & ON & (~VG)) ) & ENABLE & ALERT;
97
   assign Q[3] = ( (Q4 & ON & VG) | (1'b1 & ~ON) | (1'b1 & ON & (~VG)) ) & ENABLE & ALERT;
98
99
   // start-up counter - charge the bootstrap capacitor by activating Q3 and Q4 (low side)
100
   assign ON = cnt_startup > 8'd10; //10us to charge bootstrap capacitor
101
   assign VG = cnt_startup > 8'd14; //4us forcing sigma=1
102
103
   // create a RESET signal every time the ENABLE button is turned ON
104
   // and the initialization sequence is terminated
105
   assign ENABLE_RST = ~( VG^VG_PREV );
106
```

```
107
    // --- assign for the control of the Resonant Tank ---
108
    assign phi_HC = sw[2] ? phi: phi_PI_sat;
109
110
111
   // ------
   // MODULES
112
   11 -----
113
   PLL PLL_inst ( // PLL - manage the clock generation
114
      .inclk0 ( OSC ),
115
116
       .c1 ( clk_100M ),
117
      .c2 ( clk_1M ),
      .c3 ( clk_100k )
118
119
   );
120
    // CONTROL PHI + DELTA OF THE RESONANT TANK
121
    hybrid_control_mixed #(.mu_x1(32'd154), .mu_x2(32'd90)) hybrid_control_mixed_inst (
122
      .o_MOSFET( MOSFET ),
123
      .i_clock( clk_100M ),
124
      .i_RESET( CPU_RESET & ENABLE_RST ),
125
126
      .i_vC( vC ),
      .i_iC( iC ),
127
128
       .i_delta( delta ),
      .i_phi( phi_HC )
129
   );
130
131
    //manual control of phi, delta, and Iref
132
      value_control #( // PHI
133
         .INTEGER_STEP(5), .INTEGER_RST (0),
134
          .INTEGER_MIN (0), .INTEGER_MAX (90),
135
136
          .N_BIT (8)
       ) phi_control (
137
         .i_CLK(clk_100M),
138
139
          .i_RST(button[0]),
          .inc btn(button[1]).
140
141
         .dec_btn(button[2]),
         .count(phi),
142
143
       );
144
      value_control #( // DELTA (ZVS)
145
146
          .INTEGER_STEP(1), .INTEGER_RST (0),
          .INTEGER_MIN (0), .INTEGER_MAX (40),
147
148
          .N_BIT (8)
149
       ) delta_control (
          .i_CLK(clk_100M),
150
          .i_RST(CPU_RESET),
151
          .inc_btn(button[3]),
152
153
          .dec_btn(1'b0 ),
          .count(delta),
154
155
       );
156
       value_control #( // Iref
157
          .INTEGER_STEP(1), .INTEGER_RST (5),
158
          .INTEGER_MIN (1), .INTEGER_MAX (100),
159
                                      (2′b01)
160
          .N_BIT (8), .DP
       ) Iref_control (
161
          .i_CLK(clk_100M),
162
          .i_RST(button[0]),
163
          .inc btn(button[1]).
164
165
          .dec_btn(button[2]),
166
          .count(Iref_dA),
167
      );
168
    // ----- PI CONTROLLER ----- //
169
170
       // add the offset phi_0
       assign phi_PI = phi_PI_tmp + 32'd50;
171
       172
173
      assign error = ((Ibat_mA_filt>>7) <<7) + (~(Iref_dA*100)+1);</pre>
174
175
       PI #( .Kp (3),
                       .shift_Kp (14),
                       .shift_Ki (16),
176
             .TsKi(1),
177
             .Kaw (0),
                        .shift_Kaw(0)
       ) PI_inst(
178
         .o_PI(phi_PI_tmp),
                             // output value
179
180
          .i_CLK(clk_100k),
         .i_RST(CPU_RESET & ENABLE_RST & sw[0]),
181
182
      .err(error), // input error
```

```
.aw(phi_PI_dz) // antiwindup
183
       );
184
185
        saturation_zero #(
186
           .UPPER_LIMIT(32'd80), .N_BIT(32)
187
        ) sat_PHI_zero(
188
           .u(phi_PI),
189
190
           .u_sat(phi_PI_sat),
           .u_dz(phi_PI_dz)
191
192
       );
193
    // +++ SEQUENTIAL BEHAVIOR +++
194
195
        always @(posedge clk_100M) begin
         VG_PREV <= VG;
196
197
        end
198
    // +++ DEAD TIME +++
199
        dead_time #(.DEADTIME(60), .N(4)) dead_time_inst_6(
200
           .o_signal( {Q4, Q3, Q2, Q1} ), // output switching variable
201
202
           .i_clock( clk_100M ),
                                                 // for sequential behavior
           .i_signal( MOSFET )
203
204
        );
205
    // +++ DEBOUNCE +++
206
207
        debounce #(.DEBOUNCE_TIME(5000), .N(8)) debounce_4bit_inst( // 5ms
           .o_switch({button[3:0],sw}),
208
209
           .i_clk(clk_1M),
           .i_reset(CPU_RESET),
210
           .i_switch({BUTTON[3:0],SW})
211
212
       );
213
    // +++ START UP counters +++
214
215
        // -- counter for the bootstrap and charge the tank
216
       counter_up counter_up_inst (
           .o_counter(cnt_startup), // Output of the counter
217
           .enable( {\sim}VG & ENABLE), {\ }/{\ } it start with ENABLE and it stops with VG
218
                                       // clock Input
219
           .clk(clk_1M),
220
           .reset(ENABLE)
                                       // reset Input
       );
221
222
    // +++ RECTIFIER READING +++
223
224
       // Conversion of the sampled data value to Volt and (deci/milli)-Ampere
       assign Vbat_DEC = (ADC_Vbat * 32'd11)>>5;
225
       assign Ibat_DEC = (ADC_Ibat*32'd10) >>4;
226
       assign Ibat_mA = ADC_Ibat <<6; // x64 update from estimation</pre>
227
228
229
        // filter the mA value: average on a 4 samples time window
       LPF LPF_Ibat(
230
231
           .o_mean(Ibat_mA_filt),
232
           .i_clock(clk_100k),
           .i_RESET(CPU_RESET),
233
234
           .i_data(Ibat_mA)
       );
235
236
237
    // +++ ADC +++
       // acquire data from ADC when available % \left( {{\left( {{{\left( {{{\left( {{{\left( {{{c}}} \right)}} \right.} \right)}_{c}}} \right)}_{c}} \right)} \right)
238
        always @(posedge ADA_DCO)
239
           vC <= ~ADA_DATA+14'b1;
240
241
242
       always @(posedge ADB_DCO)
           iC <= ~ADB_DATA+14'b1;
243
244
       always @(negedge ADC_BAT_V_EOC)
245
246
           ADC_Vbat
                        = ADC_BAT_V;
247
        always @(negedge ADC_BAT_I_EOC)
248
           ADC_Ibat
                      = ADC_BAT_I;
249
250
251
    endmodule
```

# D.3 Control modules

This section reports and describes how the different control law have been implemented. We start by the different control laws inducing a modulation behavior that have been introduced in Chapters 3, 4 and Section 5.1, and we finish with the PI controller described in Chapter 5.

# D.3.1 Oscillation control - hybrid modulation control

The control laws that ensure the oscillations are based on a state-plane representation, and they are detailed from a theoretical perspective in Chapters 3, 4 and Section 5.1. Each module, one for every modulation control law, takes as input the sampled voltage and current, which are then rescaled to either  $(\bar{z}_1, \bar{z}_2)$  or  $(\bar{x}_1, \bar{x}_2)$ , and the angles  $(\theta, \varphi, \text{ and } \delta)$  that describes the switching lines (jump sets) in the state-plane. The output is the signal that is going to drive the MOSFETs.

To understand how the modulation control laws are implemented, let us consider the mixed modulation control law of Section 5.1 that in some terms is the most general, since all the others can be seen as particular cases. Let us recall that so far we have described the switching conditions (jumps) with lines in the state-plane, as represented at the left of Figure D.2. A few considerations:

- From a practical point of view, we can consider any scaled version  $\overline{z}$  or  $\overline{x}$  of the coordinates z or x, respectively, since all the lines pass through the origin;
- The switching conditions can be described with at most two lines;
- A periodic subsequence of  $\sigma$  is of at most 4 values.

We can summarize the objective of the inner control law as: "*Enforcing a periodic sequence of*  $\sigma$  *where the jump condition is represented by crossing lines in the state-plane*". There are two key aspects that need to be considered for the implementation: how to enforce the sequence, and how to detect the jump conditions. The adopted solution is a Finite State Machine (FSM) that can only go forward at each jump, triggered by the trajectory crossing the switching line (considering clock-wise rotation of the trajectory).



Figure D.2: State-plane considerations in the FPGA.

The jump detection considers two lines, S1 and S2 in Figure D.2. A line is identified by the angle  $\alpha$  and the other by the angle  $\beta$ , e.g., for the mixed modulation case we have  $\alpha = \delta + 2\varphi$  and  $\beta = \delta$ , while for the phase-shift modulation we have  $\alpha = \varphi$  and  $\beta = -\varphi$ . Each line is related to an expression:

$$\alpha: \qquad \mathsf{S1} = x_1 \sin \alpha - x_2 \cos \alpha, \tag{D.1}$$

$$\beta: \qquad S2 = x_1 \sin\beta - x_2 \cos\beta, \tag{D.2}$$

The signs of expressions (D.1), (D.2) tell us in which half-plane the trajectory, i.e., Boolean signal  $C_1$  and  $C_2$ , which is the information used to detect a jump as described in the following part. From a theoretical perspective, knowing when S1 or S2 go to zero is enough to check the jump condition. Instead, from a practical perspective, it is impossible to find the right moment when they are at zero; that is why we look at the sign, i.e. in which half plane with respect to the lines the trajectory is.

From a digital design point of view (at the best of the author knowledge), in order to obtain a robust FSM several stages are necessary (represented in Figure D.3):

- the jump detection circuit with the clock generation;
- a 2-bit counter that increase at every clock impulse;
- the map from 2-bit signal b=[b1,b0] to the 4 MOSFETs signal.

First,  $\sigma$  is represented by a 2-bit variable b=[b1,b0], the state of the FSM, as follows:

σ	+1	0	-1	0
b=[b1 b0]	00	01	10	11

At every jump detection we have that b is increasing  $b^+=b+1$ , and the proper sequence is preserved by the overflow. So, as far as the jumps are correctly detected, we have the proper sequence for  $\sigma$ . The jump detection considers in which half-plane with respect to the switching line the trajectory is (signals C<sub>1</sub> and C<sub>2</sub>) and which is the current state of the FSM.

But the detection alone is not enough. In order to increment the counter b we need rising edges as clock. Therefore, the signal generated by the detection is transformed to a clock by forcing the signal back to zero (reset) once a jump is detected. The reset is done by anding the jump signal with its previous value as depicted in the *clock generation* block in Figure D.3. Indeed, a more robust solution turned out to be looking back of two clock cycles, i.e, the clock width is double. The final stage is the conversion from b to the signals M<sub>i</sub> for the drivers, which is done according to the Table D.1.

**Example.** The FSM is in the state b=2'b00 ( $\sigma = 1$ ), and  $C_1=1$  and  $C_2=1$  since the trajectory is above both lines. Then, we are interested at the moment when  $C_1=1$  becomes 0 since it means that trajectory has entered the zone where  $\sigma$  should be zero. This event is detected by a logical condition when all the signals are at zero:  $C_1$ , b1 and b0 (upper AND port in the jump detection block in Figure D.3). In other words, when b=2'b00 we wait for the falling edge of  $C_1$ . The other jump conditions are detected similarly by combing  $C_1$ ,  $C_2$ , b0, and b1 properly.

b=[b1 b0]	$M_1$	$M_2$	$M_3$	$M_4$	expression
00	1	0	0	1	b1+(b1b0)
01	1	1	0	0	$b1+(\overline{b1}b0)$
10	0	1	1	0	b1b0
11	1	1	0	0	b1+b0

Table D.1: Conversion from b to MOSFETs' drivers signals.



Figure D.3: State machine used to detect the jumps (switching instants).

#### Frequency modulation controller

Figure D.4 reports the module used to implement control law (3.2). The code is reported next. What the module does is to compute the scaled coordinates  $(\bar{z}_1, \bar{z}_2)$ , which are used to evaluate in which part of the state-plane with respect to the switching line the trajectory is. Regularization is applied to the signal SIGMA in order to avoid unwanted jumps due to noise. In Figure D.4, we can observe that the circuit needs the knowledge of the current  $\sigma$  in order to compute the coordinates  $(z_1, z_2)$ , which is not the case for the other controllers. Differently from the other control laws that we will see next, since  $\sigma \in \{-1, 1\}$ , a FSM is not necessary and for robustness it is enough to regularize signal S[31], which corresponds to  $\sigma$ .



Figure D.4: Representation of the frequency modulation controller for the FPGA implementation.

```
1 module hybrid_control_theta_z #(
2 parameter mu_z1 = 86,
3 parameter mu_z2 = 90,
4 parameter mu_Vg = 312000
5 )(
6 output [3:0] o_MOSFET,
```
```
input
                           i clock.
                                       // for sequential behavior
7
                           i RESET,
                                        // reset signal
8
      input
      input signed [13:0] i_vC,
                                        // [14bit-signed] input related to z1
9
      input signed [13:0] i_iC,
                                        // [14bit-signed] input related to z2
10
11
      input signed [31:0] i_theta
                                        // [32bit-signed] angle of the switching surface
12 );
13
14 wire signed [31:0] vC_32, iC_32; //
15 wire signed [31:0] ctheta, stheta; //
16
17
  // INTERNAL VARIABLE
18
      integer z1, z2, S;
19
      // reg_sigma_prev, sigma; // output variable sigma {0,1}
      wire SIGMA:
20
      wire signed [31:0] sigma_not; // state ~sigma {-1,1} !! is the negate
21
  // assign output variable
22
      // bit conversion from 14bit to 32bit
23
      assign vC_32 = { \{19\{i_vC[13]\}\}\, i_vC[12:0] };
24
      assign iC_32 = { {19{i_iC[13]}} , i_iC[12:0] };
25
26
      // sigma from \{0,1\} to \{-1,1\}
      assign sigma_not = { \{31\{SIGMA\}\}, 1'b1 }; // NOTE that is reverse to avoid minus sign
27
28
      assign o_MOSFET = { SIGMA , ~SIGMA , ~SIGMA , SIGMA };
29
30 // function instantiation
31 trigonometry_deg trigonometry_inst (
      .o_cos(ctheta), // cosine of the input
32
33
      .o_sin(stheta),
                         // sine of the input
      .i_theta(i_theta) // input angle
34
35 ):
36
  regularization #(
37
      .DEBOUNCE_TIME(5), // 20ns
38
39
      .DELAY(200), // 2us -> fmax=250kHz
40
      .N(1)
41 ) regularization_jump_inst (
      .o signal( SIGMA ),
42
43
      .i_clk( i_clock ),
44
      .i_reset( i_RESET ),
45
      .i_signal( S[31] )
46
  );
47
   always @(posedge i_clock) begin
48
49
      // compute coordinate transformation
      z1 = mu_z1*(vC_32)+sigma_not*mu_Vg; // sigma is already inverted
50
      z2 = mu_z2*(iC_32);
51
      S = z1*stheta + z2*ctheta;
52
53
   end
   endmodule
54
```

## Phase-shift and mixed modulation controllers

The phase-shift and mixed modulation controllers have a similar structure, which is the reason why we describe them together. What changes is how the signals S1 and S2, related to the switching lines, are computed. Then, once we have C<sub>1</sub> and C<sub>2</sub>, the state machine is the same (Figure D.3). Figure D.5 reports the module used to implement the phase-shift modulation control law (4.2), while Figure D.6 reports the module used to implement the mixed modulation control law (5.2) The code is reported next and the difference is marked at the bottom where the signals S1 and S2 are computed. What the module does is to compute the scaled coordinates ( $\bar{x}_1, \bar{x}_2$ ), which are used to evaluate in which part of the state-plane with respect to the switching lines the trajectory is. The corresponding signals are S1 and S2, to which regularization is applied, have a period similar to the one of the oscillations. The reason why signals S1 and S2 are regularized, and not others, is that we approximately know what is going to be their period, hence we can determine a regularization time. Then, the regularized signals C<sub>1</sub> and C<sub>2</sub> are used by the FSM of Figure D.3 to generate the periodic sequence. Let us remark that the frequency modulation control law in the *x*-plane (3.5) can be implemented through the mixed modulation block by fixing  $\varphi = 0$ .



Figure D.5: Representation of the phase-shift modulation controller for the FPGA implementation.



Figure D.6: Representation of the mixed modulation controller for the FPGA implementation.

```
module hybrid_control_mixed #(
1
      parameter mu_x 1 = 32' d86,
2
      parameter mu_x^2 = 32' d90
3
   ) (
4
                             o_MOSFET,
                                           // command signal for the MOSFETs
      output
                      [<mark>3:0</mark>]
5
                             i_clock,
                                           // for sequential behavior
      input
6
      input
                             i_RESET,
                                           // reset signal
             signed [13:0]
                             i_vC,
                                           // [14bit-signed] input related to z1
      input
      input
             signed [13:0]
                             i_iC,
                                           // [14bit-signed] input related to z2
             signed [31:0]
                                           // [32bit-signed] angle freq. mod.
10
      input
                             i_delta,
             signed [31:0]
                                           // [32bit-signed] angle phase mod.
11
      input
                             i_phi
12
   );
13
   wire signed [31:0] vC_32, iC_32; //
14
   wire signed [31:0] cdelta, sdelta, cphi, sphi;
15
16
17
   // INTERNAL VARIABLE
      integer X1, X2, S1, S2;
18
19
      wire C1, C2, CLK_jump, CLK_jump_OR, b1, b0;
      reg CLK_jump_prev, CLK_jump_tmp;
20
      reg [1:0] counter, counter_prev;
                                           // counter for the FSM
21
      wire [1:0] S;
                        // regularized version of the switching surface
22
23
24 // assign output variable
     // bit conversion from 14bit to 32bit
25
   assign vC_32 = { {19{i_vC[13]}} , i_vC[12:0] };
26
```

```
assign iC_32 = { {19{i_iC[13]}} , i_iC[12:0] };
27
       assign b0 = counter[0];
28
       assign b1 = counter[1];
29
       assign C1 = S[0];
30
31
       assign C2 = S[1];
       assign CLK_jump_0R = ((~C1) \& (~b1) \& (~b0)) | (C2 \& (~b1) \& b0)
32
                          | ( C1 & b1 & (~b0) ) | ( (~C2) & b1 & b0 );
33
       assign CLK_jump
                           = CLK_jump_OR & (~CLK_jump_prev);
34
       assign o_MOSFET[0] = (~b1) | (b1&b0);
35
36
       assign o_MOSFET[1] = b1 | ((~b1)&b0);
       assign o_MOSFET[2] = b1 & (~b0);
37
       assign o_MOSFET[3] = ~(b1 | b0);
38
39
   // function instantiation
40
    trigonometry_deg trigonometry_delta_inst (
41
42
       .o cos(cdelta),
43
       .o_sin(sdelta),
       .i_theta(i_delta) // input angle "delta"
 44
   );
45
46
47
    trigonometry_deg trigonometry_phi_delta_inst (
48
       .o_cos(cphi),
49
       .o_sin(sphi),
       .i_theta(i_delta+(i_phi<<1)) // input angle "delta+2*phi"
50
51
   );
52
53
    regularization #(
      .DEBOUNCE_TIME(5), // 20ns
54
55
       .DELAY(500), // 2us
56
       .N(2)
   ) regularization 4bit inst (
57
58
      .o_signal( S ),
59
       .i_clk(i_clock),
       .i_reset(i_RESET),
60
       .i_signal({S2[31],S1[31]})
61
62
   );
63
64
   // variable initialization
65
   initial begin
       counter_prev = 2'b00;
66
                     = 2'b00;
67
       counter
       CLK_jump_tmp = 1'b0;
68
69
       CLK_jump_prev = 1'b0;
70
   end
71
72 // latch for the signal feedback that looks two samples back
73
    // this was improving the case when two edges where detected one after the other
   always @(posedge i_clock ) begin
74
75
       CLK_jump_tmp <= CLK_jump;
       CLK_jump_prev <= CLK_jump_tmp;</pre>
76
       counter_prev <= counter;</pre>
77
78
   end
79
80
    always @(posedge CLK_jump or negedge i_RESET) begin
      if (~i_RESET) begin
81
82
          counter <= 2'b10;
       end else begin
83
         counter <= counter_prev + 2'b01;</pre>
84
85
      end
86
   end
87
    always @(posedge i_clock) begin
88
       // PHASE-SHIFT MODULATION version
89
90
          A = mu_x1 * vC_32 * sphi; // x1*sin(phi)
          B = mu_x2 * iC_32 * cphi; // x2*cos(phi)
91
          S1 = A + (~B+1); // x1*sin(phi)-x2*cos(phi)
92
          S2 = A + B;
                               // x1*sin(phi)+x2*cos(phi)
93
94
95
       // MIXED MODULATION version
                                  // x1
          X1 = mu_x1 * vC_{32};
96
          X2 = mu_x2 * iC_32;
97
                                  // x2
          S1 = X1 * sphi + (~(X2 * cphi) + 1);
                                              // x1*sin(delta+2*phi)-x2*cos(delta+2*phi)
98
          S2 = X1*sdelta + (~(X2*cdelta)+1); // x1*sin(delta)-x2*cos(delta)
99
100
   end
   endmodule
101
```

# D.3.2 Proportional-Integral Controller

The module implementing the PI controller is represented in Figure D.7. The gains are implemented as a multiplicative factor and a shift factor that corresponds to the division by a power of 2:

$$\hat{k}_P = \frac{\mathsf{Kp}}{2\mathsf{shift}_{\mathsf{Kp}}}, \qquad \hat{k}_I = \frac{\mathsf{TsKi}}{2\mathsf{shift}_{\mathsf{Ki}}}, \qquad \hat{k}_{aw} = \frac{\mathsf{Kaw}}{2\mathsf{shift}_{\mathsf{Kaw}}}. \tag{D.3}$$

The choice of the two factors, the multiplicative and the shift, is crucial in order to ensure a proper representation of the numbers. e.g., if the shift factor is too large compared to the variable value, the shift operation is going to clamp the value to zero. Moreover, the order of the operations is important. Let us remember that in this FPGA we are working only with integers. Then, the link between the gains of the FPGA ( $\hat{k}_P$ ,  $\hat{k}_I$ ,  $\hat{k}_{aw}$ ) and the gains ( $k_P$ ,  $k_I$ ,  $k_{aw}$ ) in Section 5.3 is as follows

$$\hat{k}_P = \frac{k_P}{1000}, \qquad \hat{k}_I = \frac{k_I}{1000f_{ADC}}, \qquad \hat{k}_{aw} = 1000k_{aw}.$$
 (D.4)

The factor 1000 is due to the fact that we are considering the error to be expressed in mA.



Figure D.7: Representation of the PI controller for the FPGA implementation.

```
module PI #(
1
2
      parameter Kp
                     = 1, parameter shift_Kp = 0, // proportional gain
      parameter TsKi = 0, parameter shift_Ki = 0, // integral gain
3
      parameter Kaw = 0, parameter shift_Kaw = 0 // antiwindup integral
4
5
   ) (
      output signed [31:0] o_PI,
                                     // output value
6
                              i_CLK, // for sequential behavior
      input
      input
                             i_RST, // reset signal
8
             signed [31:0] err,
0
      input
                                      // input error
      input signed [31:0] aw
10
                                      // antiwindup
11 );
12
   reg signed [31:0] err_sum, err_sum_prev;
13
14
   assign o_PI = ((err*Kp) >>> shift_Kp) + ((err_sum*TsKi) >>> shift_Ki);
15
16
   initial begin
17
      err_sum_prev = 32'b0;
18
19
      err_sum
                   = 32'b0;
20
   end
21
   always @(posedge i_CLK or negedge i_RST) begin
22
       if (~i_RST) begin
23
         err_sum_prev <= 32'b0;</pre>
24
25
                      <= 32′b0;
         err_sum
26
      end else begin
27
         err_sum_prev <= err_sum;</pre>
                      <= err_sum_prev + err + ( (~((aw*Kaw) >>> shift_Kaw))+1);
28
         err sum
29
      end
30 <mark>end</mark>
31
   endmodule
```

# D.4 Signal and data manipulation modules

# Dead-time

The dead-time module introduces a delay, corresponding to the dead-time in a rising edge of a signal, while there is no delay in falling edge, as depicted in Figure D.8. The dead-time is useful to control the MOSFETs in two ways: it let discharge the parasitic capacitors, and it avoids that two MOSFETs on the same leg conduct at the same time. From the parameter of the module, the dead-time is computed as

$$t_{dt} = \frac{\text{DEADTIME}}{f_{\text{CLK}}}$$

Let us remark that the module can work on N different signals at the same time since N instantiations of dead\_time\_core are done with the module dead\_time. The fact of having this nested structure is helpful in making the code flexible for different situations.



Figure D.8: Example of the signals involved in the dead-time module.

```
module dead_time_core #(parameter DEADTIME = 10 )(
1
                           // output delayed signal
2
      output o signal,
      input i_clock,
                            // clock to count the time
3
4
      input i_signal
                             // input signal
5
   );
      reg [9:0] delay; // keep track of the count
      reg signal_delay;
7
      assign o_signal = signal_delay;
8
      initial delay = 10'b0; // initialize the counter
10
11
      always @(posedge i clock ) begin
12
13
         if( i_signal==0 ) begin // if signal is zero do nothing
             signal_delay <= 0;</pre>
14
15
             delay <= 0;
          end else begin //if 1 check for the delay
16
            if( delay < DEADTIME ) begin</pre>
17
18
                signal_delay <= 0;</pre>
                delay <= delay+1'b1;</pre>
19
             end else begin
20
21
                signal_delay <= 1;</pre>
            end
22
         end
23
      end
24
25
   endmodule
26
   module dead_time #(parameter DEADTIME = 10, parameter N = 1)(
27
28
      output [N-1:0] o_signal,
29
      input
                  i clock.
30
      input [N-1:0] i_signal
31
   );
32
      genvar i;
33
      generate
         for (i = 0; i < N; i = i + 1) begin : DT
34
35
             dead_time_core #( .DEADTIME(DEADTIME) ) dt_core(
                .o_signal(o_signal[i]),
36
37
                .i_clock(i_clock),
                .i_signal(i_signal[i])
38
             );
39
40
         end
41
      endgenerate
42
   endmodule
```

#### Debounce

The debounce module lets a signal change Boolean state only if it is stable for a given amount of time. For example, it is useful when the signal is noisy during the commutation, and we want to be sure that the signal has actually changed level. A typical example is a push button: when we push a button, the signal received by an FPGA might be bouncing between 1 and 0, and to avoid several detections of the rising edges, the debounce module can be applied.

We report only the core module debounce\_core, the surrounding box that instantiates multiple time the core module debounce is omitted as it is similar to the one of the dead-time module. The operating mode of the module is depicted in Figure D.9. What it does it to let the output signal change according to the input only when the input is stable at the same value for a time  $t_{db}$ , which is tracked by a timer. Time  $t_{db}$  can be computed as



Figure D.9: Example of the signals involved in the debounce module.

```
module debounce_core #(
1
       parameter DEBOUNCE_TIME = 5000
2
   ) (
3
       output o_switch,
4
       input i clk,
5
       input
              i_reset,
       input i_switch
8
   );
       reg [31:0] counter;
10
       reg r_switch_state;
11
12
13
       assign o_switch = r_switch_state;
14
       initial begin
15
16
          counter = 0:
          r_switch_state = 0;
17
18
       end
19
       always @(posedge i_clk or negedge i_reset) begin
20
          if (~i_reset)
21
             counter <= 0;
22
23
          else begin
             if ( (i_switch != r_switch_state) & (counter < DEBOUNCE_TIME) ) begin</pre>
24
25
                 counter <= counter+1;</pre>
              end else begin
26
                 if (counter==DEBOUNCE_TIME) begin
27
28
                    r_switch_state <= i_switch;</pre>
29
                    counter <= 0;</pre>
                 end else begin
30
                    counter <= 0;</pre>
31
                 end
32
              end
33
34
          end
35
       end
36
   endmodule
```

#### Regularization

The regularization module consists of two sequential parts: first the signal is "debounced" with the debounce module; secondly, the signal is prevented from changing for a time  $t_R$ . Regularization is useful to keep a signal constant when we know that it is supposed not to change in order to avoid the effect of noise. For example, in our case it is useful when, after a switch, we know that the signal is not supposed to change, but the effect of the ringing could trigger undesired transition. For example, it is useful when the signal is noise during the commutation, and we want to be sure that the signal has actually changed level and that is not due to noise.

We report only for the core module regularization\_core. The surrounding box that instantiates multiple time the core module regularization is omitted as it is similar to the one of the dead-time module. The operating mode of the module is depicted in Figure D.10, the regularization time  $t_R$  is computed as follows



Figure D.10: Example of the signals involved in the regularization module. Every change in the input signal is followed by a debounce stage for a time  $t_{db}$ . Then, the output signal is not allowed to change for a time  $t_R$ .

```
module regularization_core #(parameter DEBOUNCE_TIME = 2, parameter DELAY = 20)(
1
2
       output o_signal,
3
       input i_clk,
4
       input i_reset,
5
       input
              i_signal
   );
6
7
       wire signal_debounced;
       reg signal_prev;
8
       reg [31:0] counter = 0;
0
       assign o_signal = (counter < DELAY) ? signal_prev : signal_debounced;</pre>
10
11
       debounce #(.DEBOUNCE_TIME(DEBOUNCE_TIME)) debounce_inst(
12
          .o_switch(signal_debounced),
13
          .i_clk(i_clk),
14
15
          .i_reset(i_reset),
          .i_switch(i_signal)
16
       );
17
       initial counter = DELAY;
18
19
       always @(posedge i_clk) signal_prev <= o_signal;</pre>
20
       always @(posedge i_clk or negedge i_reset) begin
21
          if (~i_reset) begin
22
             counter <= DELAY;</pre>
23
24
          end else begin
25
             if( counter < DELAY ) begin</pre>
                 counter <= counter+1'b1;</pre>
26
             end else begin
27
                if (signal_prev != o_signal)
28
29
                    counter <= 0;
                 else
30
31
                    counter <= counter:
32
                 end
             end
33
          end
34
35
       end
   endmodule
36
```

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$\mathbb{N}$	The set of Natural numbers
$\mathbb{Z}$	The set of Integer numbers
$\mathbb{R}$	The set of Real numbers
$\mathbb{R}^n$	The <i>n</i> -dimensional Euclidean space
$\mathbb{R}_{\geq 0}$	The set of nonnegative Real numbers
$\mathbb{R}_{>0}$	The set of positive Real numbers
$\mathbb{Z}_{\geq 0}$	The set of nonnegative Integer numbers
$A^{ op}$	The transpose of the matrix A
(x,y)	Equivalent notation for the stacking of vectors $\begin{bmatrix} x^{\top}, y^{\top} \end{bmatrix}^{\top}$
$ x _{\mathcal{A}}$	Euclidean distance of a point $x$ from a set ${\mathcal A}$
J	Imaginary unit
8	Laplace variable corresponding to $\jmath\omega$
$\mathcal{L}\{\cdot\}$	Laplace transform
$\dot{x}$	Derivative of $x$ with respect to continuous time
$x^+$	Next value of $x$ with respect to discrete time
$x^{(1)}$	First harmonic of <i>x</i>
$x^{(k)}$	<i>k</i> -th harmonic of <i>x</i> with $k \in \mathbb{N}$

# Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BALUN	BALanced-UNbalanced
DAB	Dual Active Bridge
DAC	Digital-to-Analog Converter
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
EV	Electric Vehicle
FHA	First Harmonic Approximation
FSM	Finite State Machine
FPGA	Field-Programmable Gate Array
GAS	global asymptotic stability
IC	integrated circuit
LMI	Linear Matrix Inequality
LPF	Low-Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Msps	Megasamples per second
OBC	On-Board Charger
OPAMP	Operational Amplifier
РСВ	Printed Circuit Board
PI	Proportional-Integral
PRC	Parallel Resonant Converter
PWM	Pulse-Width Modulation
SRC	Series Resonant Converter
TF	Transfer Function
VCO	Voltage-Controlled Oscillator
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching





### Title: Hybrid Limit Cycles: from theory to practice in resonant converters

Key words: Power converter, Hybrid dynamical systems, Hybrid limit cycle, Stabilization

Abstract: This dissertation addresses the stabilization of periodic trajectories in hybrid dynamical systems, focusing on resonant power converters from both theoretical and practical perspectives. The focus is twofold: on one side there are the theoretical analyses and simulations that show specific behaviors; on the other side there is the "on-the-field" work involving hardware and software development and coding to create a functioning controller that confirms the validity of the theory. The aim of this dissertation is to integrate the theoretical control aspects with the practical power electronics aspects, starting from the analysis of different control laws that ensure an oscillating behavior, and ending with a current regulation problem on a power converter prototype. Initially, we build the theoretical framework for the formal analysis of systems exhibiting both continuous and discrete behavior, the so-called hybrid dynamical systems. We focus particularly on second-order resonant converters, which are relatively easy to represent but present some challenges. In this initial part we overview control laws that ensure a desired self-oscillating behavior with different properties in terms of switching and design efficiency, with the focus on the Zero-Voltage Switching (ZVS) behavior. After focusing on the second-order resonant converter, we extend the control algorithm to the third-order LLC resonant converter. In other words, we apply the same controller used for second-order systems to a more complex converter with richer behavior and observe what is the outcome. This extension anticipates the eventual validation of our controller on a battery charger, which uses the LLC topology. Indeed, the latter part of the manuscript is dedicated to the realization and testing of an LLC prototype, with the objective of validating the theoretical results and the formulated conjectures. The prototype includes all power stages, from the resonant tank to the rectifier, as well as the necessary sensing. The control law is implemented in a Field-Programmable Gate Array (FPGA). The final step is the regulation of the output current of the converter while ensuring ZVS of the transistors.

Titre : Cycles Limites Hybrides : de la théorie à la pratique dans les convertisseurs résonants

Mots clés : Convertisseur de puissance, Systèmes dynamiques hybrids, Cycle limite hybride, Stabilisation

Résumé : Cette thèse traite de la stabilisation des trajectoires périodiques dans les systèmes dynamiques hybrides, en se concentrant sur les convertisseurs résonants de puissance, à la fois d'un point de vue théorique et pratique. L'objectif est double : d'un côté, des analyses théoriques et des simulations permettent de démontrer et mettre en évidence certains comportements ; de l'autre, une mise en œuvre expérimentale impliquant le développement de l'électronique et le codage pour créer un contrôleur fonctionnel illustre le bien-fondé des approches proposées d'un point de vue théorique. Le but de ce travail est d'intégrer les aspects théoriques du contrôle avec les aspects pratiques de l'électronique de puissance, en commençant par l'analyse de différentes lois de contrôle qui assurent un comportement oscillant, et en terminant par un problème de régulation de courant sur un prototype de convertisseur. Dans un premier temps, nous construisons le cadre théorique pour l'analyse formelle des systèmes présentant un comportement à la fois continu et discret, également appelés systèmes dynamiques hybrides. Nous nous concentrons particulièrement sur les convertisseurs résonants du second ordre, qui sont relativement faciles à représenter, mais qui présentent certains défis. Dans cette première partie, nous reproduisons et proposons des lois de contrôle qui garantissent un comportement auto-oscillant souhaité avec différentes propriétés en termes de commutation et d'efficacité de conception, en mettant l'accent sur le comportement de commutation à tension nulle (Zero-Voltage Switching – ZVS). Après nous être concentrés sur le convertisseur résonant de second ordre, nous étendons le contrôle au convertisseur résonant LLC de troisième ordre. En d'autres termes, nous appliquons le même contrôleur que celui utilisé pour les systèmes de second ordre à un convertisseur plus complexe au comportement plus riche, et nous observons le résultat. Cette extension anticipe la validation de notre contrôleur sur un chargeur de batterie, qui utilise la topologie LLC. Par conséquent, la dernière partie du manuscrit est consacrée à la réalisation et à l'essai d'un prototype LLC, dans le but de tester les résultats théoriques et les conjectures formulées. Le prototype comprend tous les étages de puissance, du réservoir résonant au redresseur et tous les capteurs nécessaires. La commande est mise en œuvre dans un circuit logique programmable (Field-Programmable Gate Array – FPGA). L'étape finale est la régulation du courant de sortie du convertisseur tout en garantissant le ZVS des transistors.