Towards ultra-low-power logic gates based on contactless capacitive mems operating in adiabatic regime

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Vers des Portes Logiques Ultra-Basse Consommation basées sur des MEMS Capacitifs Sans Contact Opérant en Régime Adiabatique

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To my mom, who is my biggest support and inspiration,
and to my sisters, who are my world.

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Abstract

This thesis details the development of a MEMS-based device aimed at enabling ultra-low-power electronics to operate in a contactless manner. This innovative approach addresses common issues in existing technologies, such as leakage currents, dynamic energy losses in MOSFETs, and contact degradation in micro-relays. The initial part of the thesis reviews the current state of digital circuits, particularly focusing on MOSFET transistors and micro-relays, and highlights their technological constraints. This sets the stage for introducing a contactless device capable of operating in an adiabatic regime, presenting a variable capacitor architecture as a promising solution.

The core of the thesis explores the design of a Capacitive Adiabatic Logic (CACL) inverter gate, featuring a dual-rail architecture realized through comb-drive structures. This design aims to minimize energy consumption while considering technological constraints. Comprehensive analytical and finite element method (FEM) analyses of the comb-drive structures inform the optimal design parameters. Factors such as the length, width, and thickness of the comb fingers, the gap between them, their overlap, and their number are analyzed for their impact on the variable, fixed, and parasitic capacitances of the actuator, as well as the induced force between the combs. Additionally, the analysis covers achievable displacement amplitudes essential for encoding logic states and examines the sensitivity of the MEMS device's stable positions to geometric variations.

The thesis also details the stages involved in designing and fabricating the MEMS logic structures, building on the differential capacitive design. It covers the design process for individual components, including conducting paths, springs, input and output combs, and fixed capacitors. Test structures used to evaluate component performance within the inverter gate are described, along with different implementations for a NAND gate. The fabrication process, beginning with initial microfabrication tests on silicon wafers to identify optimal conditions and account for dimensional changes due to underetching, is thoroughly detailed, culminating in the final fabrication of full MEMS logic gates on silicon-on-insulator (SOI) wafers.

The final part of the thesis presents a comprehensive investigation into the correlation between voltage and displacement in combs with near-zero overlap, emphasizing the significant influence of geometric variations on device performance. Detailed experimentation and analysis demonstrate the efficiency of the CACL MEMS inverter gate, particularly in the 4-phase operating mode crucial for adiabatic computation. The operational range, derived from experimental findings and a MATLAB model of the gates, provides specific voltage thresholds for optimal performance. Furthermore, the inverter gates have been successfully operated at temperatures up to 200°C, affirming their robustness and ability to withstand harsh conditions. The geometry of the CACL NAND gates, tested in the 4-phase operating mode, successfully confirmed NAND behavior, which opens the door to constructing any other gate type using one or more of these devices, enabling the creation of complex digital circuits.

The thesis concludes by demonstrating logic state transportation across a cascade of ten concatenated devices, with optical measurements confirming accurate logic state inversion between each pair of consecutive devices. This research represents a significant advancement in developing ultra-low-power, contactless electronic devices, addressing limitations of current technologies, and proposing a novel MEMS-based solution. This innovation is critical for enhancing performance, reducing energy consumption, and extending the lifespan of electronic components, thus paving the way for more efficient, durable, and versatile electronics.

Resumé

Cette thèse se concentre sur le développement d'un dispositif MEMS pour permettre aux composants électroniques ultra-basse consommation de fonctionner sans contact. Elle aborde les problèmes des technologies actuelles comme les courants de fuite, les pertes d'énergie dynamiques dans les MOSFETs et la dégradation des contacts dans les micro-relais. La première partie examine l'état des circuits numériques, mettant en lumière les contraintes technologiques des transistors MOSFET et des micro-relais, avant de proposer un dispositif sans contact fonctionnant en régime adiabatique avec une architecture de condensateur variable.

Le cœur de la thèse détaille la conception d'une porte inverseuse à logique adiabatique capacitive (CACL) avec une architecture à double rail utilisant des structures à entraînement à peigne. Des analyses analytiques et par méthode des éléments finis (FEM) déterminent les paramètres de conception optimaux. Les facteurs tels que la longueur, la largeur, l'épaisseur des doigts de peigne, l'écart entre eux et leur nombre sont étudiés pour leur impact sur les capacités et la force induite entre les peignes. L'analyse couvre aussi les amplitudes de déplacement pour coder les états logiques et la sensibilité des positions stables du dispositif MEMS aux variations géométriques.

La thèse décrit les étapes de conception et de fabrication des structures logiques MEMS, y compris les composants individuels comme les chemins conducteurs, les ressorts, les peignes d'entrée et de sortie, et les condensateurs fixes. Elle aborde également les structures de test pour évaluer la performance des composants et les différentes implémentations d'une porte NAND. Le processus de fabrication, débutant par des tests sur des substrats de silicium pour identifier les conditions optimales, est détaillé jusqu'à la fabrication finale des portes logiques MEMS sur des substrats de silicium sur isolant (SOI).

La dernière partie présente une étude approfondie de la corrélation entre la tension et le déplacement des peignes avec un chevauchement quasi nul, soulignant l'importance des variations géométriques sur la performance du dispositif. Des expérimentations et analyses montrent l'efficacité de la porte inverseuse CACL MEMS, particulièrement en mode de fonctionnement à 4 phases. Les résultats fournissent des seuils de tension pour une performance optimale. Les portes inverseuses fonctionnent à des températures allant jusqu'à 200°C, prouvant leur robustesse. La géométrie des portes NAND CACL, testée en mode à 4 phases, confirme le comportement NAND, permettant la construction de circuits numériques complexes.

La thèse se conclut par la démonstration du transport des états logiques à travers une cascade de dix dispositifs concaténés, avec des mesures optiques confirmant l'inversion précise des états logiques. Cette recherche représente une avancée significative pour les dispositifs électroniques ultra-basse consommation et sans contact, améliorant la performance, réduisant la consommation d'énergie et prolongeant la durée de vie des composants électroniques.

Table of Contents

Abbreviations and acronyms

BARC	Bottom Anti Reflective Coating
CACL	Complementary Adiabatic Capacitive Logic
CAL	Capacitive Adiabatic Logic
DRIE	Deep Reactive Ion Etching
ECRL	Efficient Charge Recovery Logic
EFD	Electrical Field Decomposition
FEM	Finite Element Method
fps	Frames per second
GEET	Génie électrique, électronique, télécommunications et santé
ICT	Information and Communication technology
MEMS	Micro Electro Mechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect transistor
NVC	Negative-type Variable Capacitor
PFAL	Positive Feedback Adiabatic Logic
PVC	Positive-type Variable Capacitor
RCA	Radio Corporation of America
RIE	Reactive Ion Etching

General Introduction

The increasing demand for digital services has led to a significant rise in the electricity consumption of electronic circuits, creating substantial societal and environmental challenges. Information and Communication Technology (ICT) now accounts for a considerable portion of global energy consumption, accounting for approximately 4-6% of global electricity use in 2020. ICT's share of global greenhouse gas emissions was estimated at more than 2% in recent reports, escalating concerns about climate change [1]. As the world becomes more reliant on digital infrastructure for communication, commerce, education, transportation and entertainment, the energy demands of data centers, servers, and consumer electronics continue to grow. This trend raises the urgency for sustainable energy solutions.

Moreover, the rapid expansion of portable electronic devices, such as smartphones, laptops, and tablets, has intensified the need for energy-efficient technologies. Consumers increasingly demand longer battery life, driving the industry to seek innovations that can reduce power consumption without compromising performance. Extending the battery life of portable devices is crucial for enhancing user convenience and reducing electronic waste, which poses significant environmental hazards. Additionally, the rise of the Internet of Things (IoT) and wearable technology underscores the importance of developing ultra-low-power electronic components to support widespread computing without an unsustainable increase in energy consumption.

Complementary metal-oxide-semiconductor (CMOS) technology, which typically uses silicon as the semiconductor material, forms the basis of almost all digital processing circuits, including CPUs. Over the past few decades, significant efforts and tremendous progress have been made in this field. However, even the most advanced CMOS logic circuits still dissipate about 1000 $k_{\mathrm{B}}T$[1] of energy per bit operation [2]. This is three orders of magnitude higher than the theoretical minimum energy dissipation, known as the Landauer limit [3]. Besides being an issue for global energy consumption, the energy dissipation imposes thermal constraints and limitations on integrated circuits, impacting their performance and reliability. Efforts to reduce energy dissipation face limitations due to the trade-off between dynamic and static losses, and the inherent constraints of CMOS technology, particularly the sub-threshold current slope. These limitations have spurred interest in nano/micro-electromechanical relays, which cut off power in the "off" state, eliminating leakage currents and static losses. However, these relays require physical

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[1] At room temperature the thermal energy amounts to approximately $4.14 \cdot 10^{-21}$ J.

contact for operation, leading to mechanical irreversibility, energy dissipation, reliability issues and overall limited lifetime, making them unsuitable for digital circuits with high switching frequencies (billions per second).

On the other aspect, additional challenges are presented by the application of electronics in harsh environments, such as high-temperature automotive or aerospace settings [4]. Conventional electronics have limited temperature tolerance, with current commercial high-temperature electronics rarely qualified for temperatures above 500 K. This limitation often necessitates placing processing units far from sensors, degrading readout performance. While there have been promising demonstrations of electromechanical computing at temperatures up to 773 K, the reliability of microelectromechanical systems (MEMS) relays is limited to millions of cycles due to mechanical contact, reducing their effectiveness in digital processing where frequent switching is needed. High temperatures also accelerate electrode oxidation in relays, compromising the distinction between on- and off-states.

Considering the societal challenges related to energy consumption, dissipation, sustainability, and the ever-increasing performance demands of electronic devices, alongside the need for technologies capable of operating in harsh environments, there is a strong motivation to develop a new computing paradigm. This paradigm would support adiabatic computation while being reliable, robust, and resilient to extreme temperatures. The concept of using contactless, capacitive devices for logic gate realization and information encoding has emerged as a promising solution. This innovative approach has sparked significant research in recent years, leading to the work presented in this thesis, which will introduce for the first time the dual-rail architecture of logic gates based on such components.

The first chapter of this thesis will address the main sources of heat dissipation in modern circuits, introducing the optimal (adiabatic) charging principle aimed at reducing dissipation. It will discuss the implementation of the adiabatic charging principle in electronic circuits and explain the incompatibility of metal-oxide-semiconductor field-effect transistor (MOSFET) technology with this approach. The chapter will consider alternatives such as micro and nano relays, highlighting their drawbacks. It will then present variable capacitors as potential candidates, summarizing extensive research conducted within the French collaborative network over recent years. This research has provided valuable insights into variable capacitor technology, leading to the current study. Finally, a dual-rail approach will be proposed to enhance device stability and simplify the manufacturing process and integration.

The second chapter will begin with an explanation of Complementary Capacitive Adiabatic Logic (CACL), proposing comb-drive actuators as a solution for implementation and explaining their operating principle. It will delve into the behavior modeling of the comb-drive actuators based on analytical descriptions and finite element method (FEM) simulations. The chapter will explain the benefits of the unconventional operation of comb-drives with no initial finger overlap and demonstrate how the contribution of fringing fields can be exploited to reduce dissipation during logic state computation. These models will form the basis for designing an elementary variable capacitor component and a complete inverter gate, simulating the information transport and the energy invested in coding.

In the third chapter, we will cover the various stages involved in the design and fabrication of MEMS logic structures. Starting with the concept of the inverter logic gate based on variable capacitors, this chapter will address the individual design process for the separate components of this device. It will outline the test structures used to investigate the performance of each element within the inverter gate and propose different possibilities for implementing a NAND gate. The chapter will further explore the fabrication process and its optimization, providing a detailed explanation of each step. Subsequently, the fabricated structures will be presented and discussed.

The fourth chapter will detail the experiments performed on the test structures, including fixed capacitors, individual inverter gates, NAND logic gates, and cascades of ten inverter gates. It will begin with an introduction to the setups and methodology, followed by the presentation of measurement results and discussions, deriving the signal requirements for successful operation. Experimental results will be compared with the previously developed models, providing a comprehensive evaluation of the system's performance.

1

State of the art

1.1 Tendency in research

Energy efficiency is currently at the forefront of electronic and computer evolution. Historically, the focus of the industry has shifted over the decades. From the 1950s to the 1990s, advancements were primarily driven by the need for increased speed and miniaturization, as highlighted by the relentless pursuit of Moore's Law [5, 6]. However, since the 1990s, there has been a notable shift towards prioritizing energy efficiency alongside continued miniaturization. This change has been propelled by the growing demand for portable devices and the need for longer lifetime of their batteries (lower power consumption and dissipation). Furthermore, large-scale integration, with billions of transistors on a single chip, imposes significant thermal constraints. Approximately 10% of electricity in France is consumed by electronic devices and digital services, which is similar to the global average [7, 8]. As technology progresses, reducing the environmental impact of energy consumption and achieving higher performance with lower power usage has become a key objective, driving innovation in ultra-low-power electronics and leading to the development of more energy efficient solutions [9].

A fundamental concept in the physics of information processing was introduced by an IBM researcher Rolf Landauer [3]. The principle highlights the connection between information theory and thermodynamics, claiming that the erasure of information is necessarily associated with an increase in entropy and consequently with the dissipation of a minimum amount of heat. This minimum amount of energy is known as the Landauer limit and is given by the formula:

$$E_{\text{min}} = k_{\text{B}} T \ln 2 \tag{1.1}$$

where E_{min} is the minimum energy dissipation per bit erased, k_{B} is the Boltzmann constant and T is the absolute temperature of the computing environment.

At room temperature (approximately 300 K), this energy is very small, around

2.9×10^{-21} joules per bit. Despite this small value, the Landauer principle underscores a fundamental limit on energy efficiency in computation, highlighting that no matter how efficient a computational device becomes, there is an irreducible energy cost associated with information destruction. It therefore provides a theoretical foundation for the potential energy savings in reversible computing. It highlights that energy dissipation is fundamentally linked to information loss, and by designing computing systems that avoid erasing information, one can reduce or even eliminate this dissipation.

The following sections will explore the primary sources of heat dissipation in modern circuits, introducing the optimal (adiabatic) charging principle aimed at dissipation reduction. Subsequently, they will discuss the implementation of the adiabatic charging principle in electronic circuits, explaining the incompatibility of MOSFET technology with this approach. Alternatives such as micro and nano relays will be considered, including their drawbacks. Variable capacitors will then be presented as potential candidates, summarizing the extensive research conducted within the French collaborative network over recent years. This research has provided valuable insights into variable capacitor technology, leading to the current study. This thesis builds on previous work by adopting a dual-rail approach to improve device stability and simplify manufacturing process and integration.

1.2 Sources of heat dissipation in circuits

Joule's effect, also known as Joule heating, is the phenomenon where electrical energy is converted into heat energy when an electric current passes through a conductor. The heat produced is due to the resistance that the conductor offers to the flow of current.

The amount of power dissipated by an electric current flowing through a resistor can be quantified by Joule's Law, which states that the power produced (P) in a resistor is directly proportional to the square of the current (I) and the resistance (R) of the resistor. As the potential difference at the terminals is $U = RI$, the dissipated power can mathematically be expressed as:

$$P(t) = RI(t)^2 \qquad \text{or} \qquad P(t) = U(t)I(t) \tag{1.2}$$

In essence, Joule's Law provides a way to calculate the thermal energy generated in an electrical circuit due to the resistance encountered by the flowing current.

In the case of an ideal capacitor, that is, a constant capacitance with no parasitic resistances in series or in parallel, there is no heat dissipation. The energy stored in an ideal capacitor is a function of the capacitance and the voltage across its plates. The formula to calculate this energy is derived from the work done to charge the capacitor and is given by a well-known relationship:

$$E = \frac{1}{2}CV^2 \tag{1.3}$$

1.2.1 Dynamic dissipation

Assuming that a resistor R and a capacitor C are connected in series and to a common voltage generator ($V(t)$) and that the voltage is introduced (at $t = 0$) from 0 to a value V_{dd}, we can describe the system with the following equation:

$$\begin{aligned} V(t) &= Ri(t) + V_C(t) \\ i(t) &= C\frac{dV_C(t)}{dt} \end{aligned} \tag{1.4}$$

The evolution of capacitor voltage V_C over time is expressed by:

$$V_C(t) = V_{\mathrm{dd}}\left(1 - e^{-\frac{t}{RC}}\right) \quad \text{for} \quad t > 0 \tag{1.5}$$

Giving the energy that is dissipated in the resistance over the infinite time duration:

$$\begin{aligned} E_R &= \int_0^\infty Ri^2(t)dt = R\frac{V_{\mathrm{dd}}^2}{R^2}\int_0^\infty \left(e^{-\frac{t}{RC}}\right)^2 dt \\ &= \frac{1}{2}CV_{\mathrm{dd}}^2 \end{aligned} \tag{1.6}$$

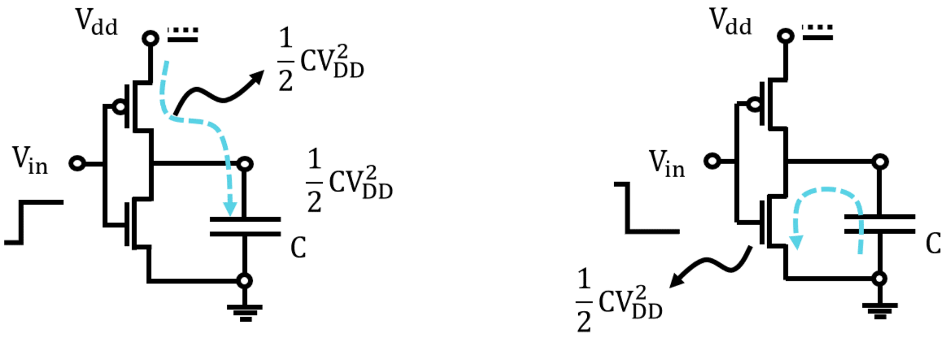
which is independent on the resistance value and amounts to the half of the energy provided by the power source, the other half being stored in the capacitor after the infinite amount of time. This behavior is illustrated in the example of a logic gate (inverter gate shown in Figure 1.1a). When the input logic state is 1, the PMOS transistor is ON and acts like a resistor, dissipating half of the energy supplied by the power source. The other half of the energy is stored in C, the equivalent capacitance of the interconnect lines and the following gate. However, this stored energy is lost during the next switching event when the state changes to zero, causing the NMOS transistor to turn ON and dissipate the energy previously stored in C.

When applying this principle to a logic gate, where the output capacitor is charged in the "on" state, the dissipated power per logic gate within a single clock period is:

$$P_{\mathrm{dynamic}} = \frac{1}{2}\alpha f C V_{\mathrm{dd}}^2 \tag{1.7}$$

Where α is the probability that a switching event occurs within a time period $T = 1/f$. The dissipated power can obviously be reduced by lowering the V_{dd} voltage.

In modern MOSFET technology, dynamic power dissipation per switching event is



(a) Input state 1 **(b)** Input state 0

Figure 1.1: Charging of the capacitor with (a) constant voltage, b) constant current.

typically on the order of microwatts. Given operating frequencies in the GHz range, the energy dissipated per operation is on the order of femtojoules. The power loss density in modern processors ranges from 10 to 100 µW µm^{-2}.

1.2.2 Static dissipation

The threshold voltage (V_T) in MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) transistors is the minimum gate-to-source voltage (V_GS) that is required to create a conductive channel between the source and drain terminals. This voltage ($\approx$ 300 mV in current technologies) is crucial because it determines when the MOSFET turns on and off.

Ideally, above V_T, the channel forms, and current can flow between the drain and source. Below V_T, the channel does not form, and the MOSFET is in the off state. However, in the sub-threshold regime a small current still flows due to the weak inversion layer formed in the channel. Even when V_GS is below V_T, a small number of carriers (electrons in n-channel MOSFETs or holes in p-channel MOSFETs) are present in the channel. These carriers enable a small current to flow from the drain to the source. This current in the sub-threshold region is exponentially related to the gate voltage and can be described by the following equation:

$$I_\mathrm{DS} \approx I_0 \cdot e^{\dfrac{V_\mathrm{GS} - V_\mathrm{T}}{nV_\mathrm{th}}} \tag{1.8}$$

where n is the sub-threshold slope factor and $V_\mathrm{th} = k_\mathrm{B}T/q$ is the thermal voltage ($\approx$ 26 mV at room temperature).

This means that even in the absence of V_GS voltage there is the residual current:

$$I_\mathrm{off} = I_0 e^{-\dfrac{V_\mathrm{T}}{nV_\mathrm{th}}} \tag{1.9}$$

Or in terms of static power loss:

$$P_{\text{static}} = I_0 V_{\text{dd}} e^{-\dfrac{V_{\text{T}}}{nV_{\text{th}}}} \tag{1.10}$$

The static power dissipation can be estimated to be on the order of nanowatts, which corresponds to picojoules in terms of energy.

Lowering of the threshold voltage increases exponentially the leakage current in the off state I_{off}. Increasing it would however result in higher dynamic dissipation during switching operations (Eq. 1.7).

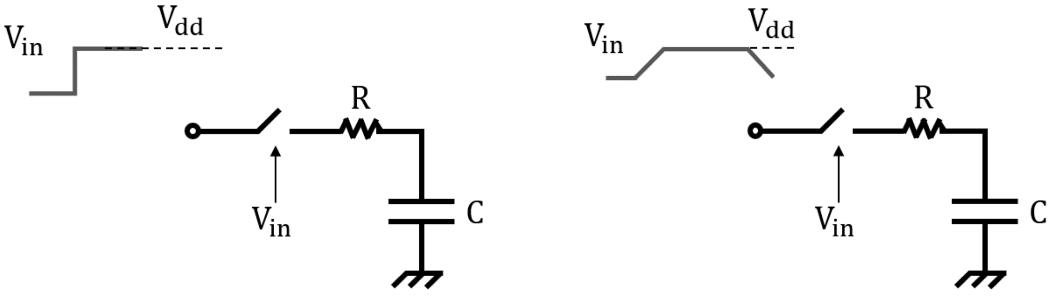
Trade-off is therefore necessary for the choice of V_{T}, V_{dd}, and the frequency of operation in order to achieve the most optimal operating conditions. According to [10] this trade-off for achieving the lowest energy consumption is such that $V_{\text{T}} = \frac{1}{3}V_{\text{dd}}$.

1.3 Principle of optimal charging of a capacitor

As described in the previous section, in the case of conventional charging a capacitor C through a constant resistor R by abrupt application of a constant voltage signal (Figure 1.2a), a capacitor voltage would develop over time according to the Eq. 1.5. The circulating current takes the form:

$$i(t) = \frac{V_{\text{dd}}}{R} e^{-\dfrac{t}{RC}} \tag{1.11}$$

Starting from value $\dfrac{V_{\text{dd}}}{R}$ at $t = 0$ and falling towards zero during the charging of the capacitor. The energy provided by the source is $E = CV_{\text{dd}}^2$, but only half of this energy is stored in the capacitor, while the other half is dissipated in the resistor, as derived in Eq. 1.6. So in the case of constant voltage and constant load, the dynamic dissipation when the states change is independent of the resistances.



(a) (b)

Figure 1.2: Charging of the capacitor with (a) constant voltage, b) constant current.

Adiabatic charging of a capacitor (Figure 1.2b) refers to a process in which the energy dissipation is minimized during the charging cycle. The resistive losses are minimized by slowly charging the capacitor, allowing the energy transfer to occur with minimal heat dissipation. This is achieved by controlling the rate at which the voltage is applied to the capacitor. If the supplied voltage V_{dd} is linearly increased with the ramp time $T > RC$, we can describe the simple circuit as:

$$\begin{aligned} V_{\mathrm{dd}}\frac{t}{T} &= Ri(t) + V_C(t) \\ i(t) &= C\frac{dV_C(t)}{dt} \end{aligned} \tag{1.12}$$

Solving this differential equation for V_C gives:

$$\begin{aligned} V_C &= V_{\mathrm{dd}}\frac{t}{T} - \left(\frac{RC}{T}\right)V_{\mathrm{dd}}\left[1 - e^{-\frac{t}{RC}}\right] && \text{for} \quad 0 \le t \le T \\ V_C &= V_{\mathrm{dd}}\frac{t}{T} - \left(\frac{RC}{T}\right)V_{\mathrm{dd}}\left[1 - e^{-\frac{t}{RC}}\right]e^{-\frac{t-T}{RC}} && \text{for} \quad t \ge T \end{aligned} \tag{1.13}$$

The dissipated energy in the resistor is then given by:

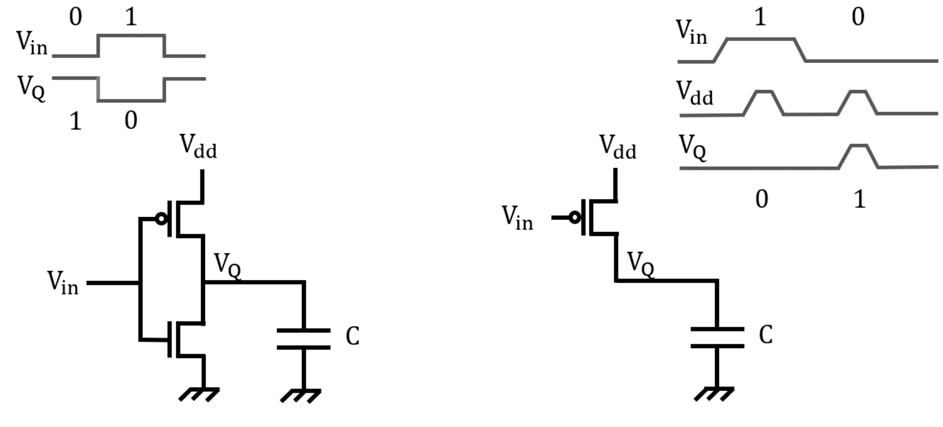
$$E_R = \int_0^\infty \left(V_{\mathrm{dd}}\frac{t}{T} - V_C(t)\right) i(t)dt = \left(\frac{RC}{T}\right) CV_{\mathrm{dd}}^2 \tag{1.14}$$

This means that by choosing the ramping time T that is much greater than the time constant RC of the circuit, that is, by slowing down the speed, the Joule-dissipation can be reduced to an arbitrarily low level. This is the fundamental principle of adiabatic operation.

1.4 Adiabatic electronics

A traditional MOSFET inverter (Figure 1.3a) is a fundamental component in digital electronics. It comprises a PMOS transistor at the top and an NMOS transistor at the bottom. When the input voltage is low, the PMOS transistor conducts, and the NMOS transistor is off, resulting in a high output voltage. Conversely, when the input voltage is high, the PMOS transistor is off, and the NMOS transistor conducts, leading to a low output voltage. This configuration ensures that the output is always the logical inverse of the input.

In adiabatic logic circuits (Figure 1.3b), to minimize power dissipation, the input signal V_{in} must remain stable (either high or low) during the variations of the clock signal. Additionally, the input signal needs to be longer in duration than the clock signal to ensure proper energy recovery and minimal power loss. Adiabatic circuits utilize slowly varying power supplies to transfer energy efficiently. By extending the input signal duration beyond

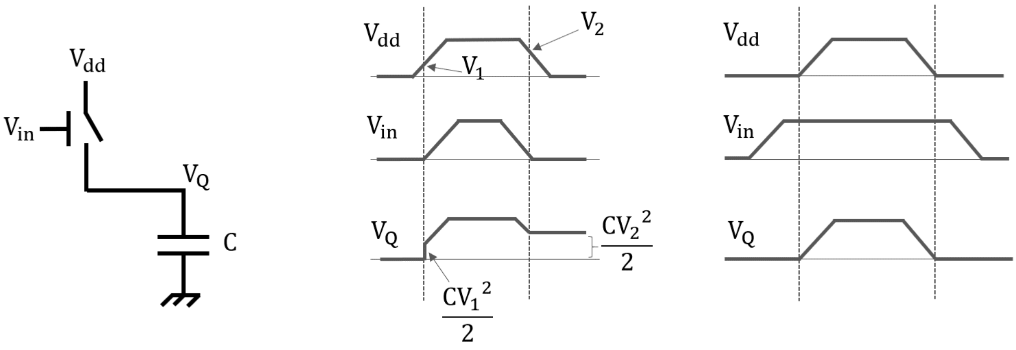


(a) Traditional MOSFET inverter **(b)** Adiabatic MOSFET inverter

Figure 1.3: MOSFET inverter gate in (a) traditional operating mode, b) adiabatic operation.

that of the supply signal, the circuit can complete charge and discharge cycles gradually, thereby avoiding abrupt voltage changes that lead to energy dissipation as heat. This precise timing alignment is crucial for maximizing energy efficiency in adiabatic logic gates.

Figure 1.4 illustrates the generation of the output signal V_Q with suboptimal and adiabatic synchronization of input and supply signals, as seen in Figures 1.4b and 1.4c, respectively. In the scenario depicted in Figure 1.4b, the supply signal begins to ramp while V_{in} remains at zero, meaning the supply is not connected to the capacitor C. When the input signal starts to increase, voltage V_1 is abruptly applied to the capacitor, resulting in non-adiabatic losses of $\frac{CV_1^2}{2}$. During the capacitor's discharge, the input signal reaches zero while the supply voltage only reaches V_2, leaving the output at this intermediate value. If in the next switching event the output is connected to a supply value of zero, it results in dissipation of $\frac{CV_2^2}{2}$.



(a) **(b)** **(c)**

Figure 1.4: Example of the generation of output signal V_Q (a) with the (b) non optimal and c) optimal synchronization of signals.

In the scenario depicted in Figure 1.4c, both the charging and discharging of the capacitor occur adiabatically because V_{in} remains stable throughout the entire ramping period of the supply signal, fully encompassing it. This approach is known as "Bennett clocking," named after IBM researcher Charles Bennett, who introduced the concept in 1973 [11].

1.5 Benett clocking and 4 phases architectures

In a system of cascaded gates, as shown in Figure 1.5, the output of each gate serves as the input for the next gate, reflecting the waveform of its power supply. As described in the previous section Figure 1.4c, input signal has to be wider and be stable during the rising and falling of the gate's power supply. This setup requires that the power supply and output width of each gate be greater than those of the subsequent gate.

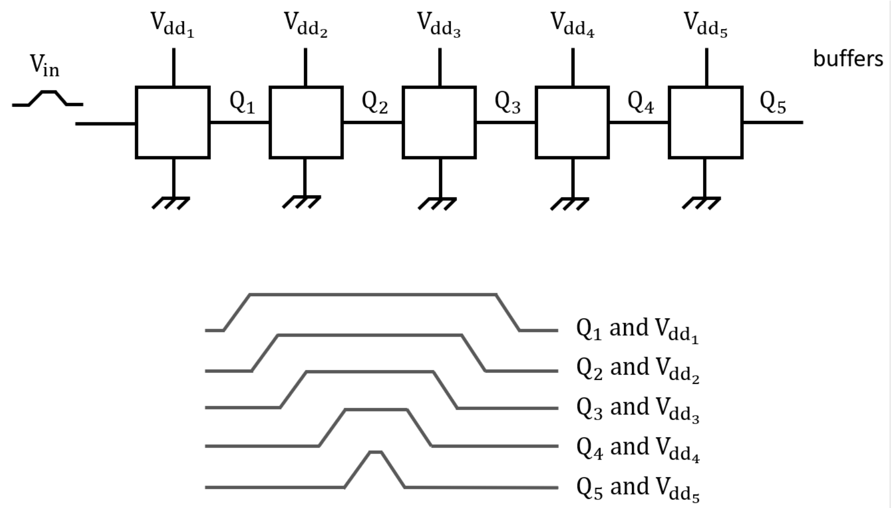


Figure 1.5: Principle of Bennett clocking

However, this configuration presents a challenge because each gate operates with a differently shaped supply signal, complicating the overall implementation. Additionally, the duration of the input signal, V_{in}, increases with the number of gates in the cascade, resulting in a very low-frequency signal. In Bennett architecture, the power supply must be reversible to recover charges. This means the power supply current can flow both positively and negatively, allowing it to act as a receiver during certain phases.

1.5.1 Four phase operation

A more realistic implementation of adiabatic principle compared to the above presented cascade operating under Bennett principle is to systematically delay the supply signal with respect to the input signal. The signals have the same shape and duration, with the shape being divided into four equally long phases. The time delay ensures that there is no signal variation during the capacitor's charging. As a duration of this delay, we can define the minimum possible value - the one of the ramping time of the input signal V_{in}.

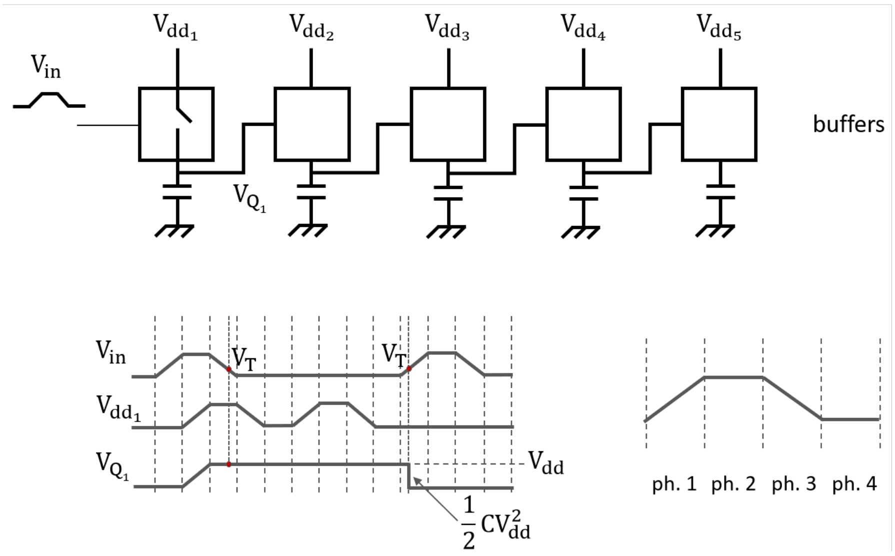


Figure 1.6: Incomplete pipeline

In the first phase, the input voltage is increased to its high value. During the second phase, while V_{in} remains constant, the supply signal is increased, causing the output voltage V_{Q_1} to rise correspondingly. In the third phase, the input voltage is reduced to zero, and the output Q_1 is disconnected from the supply, thus maintaining the V_{dd} value. When the input voltage starts to ramp up again, the output node is reconnected to the supply voltage, which is now at zero. This results in non-adiabatic dissipation of $\frac{CV_{\text{dd}}^2}{2}$. Consequently, there is not only significant thermal dissipation, but the output signal also fails to accurately follow the input's shape. Ideally, the signal should return to zero at the end of the third phase.

1.5.2 Quasi adiabatic pipeline

To ensure the output returns to zero at the end of the third phase, an additional "hold" signal is required to maintain the connection to the supply voltage if the output is high. Conversely, if the output is zero, this connection should be omitted. One approach is to use the output itself as the hold signal. Ideally, with perfect transistors, this would function correctly. However, real transistors have a threshold voltage V_{T}. When the output voltage drops below V_{T}, the connection with the supply is severed, causing the output to remain at V_{T}.

This situation leads to thermal dissipation of $\frac{CV_{\text{T}}^2}{2}$, hence the term "quasi-adiabatic." Although it is possible to further reduce this residual dissipation, doing so significantly increases the complexity of the circuit.

This additional signal effectively reduces the dissipated thermal energy from $\frac{1}{2}CV_{\text{dd}}^2$ to

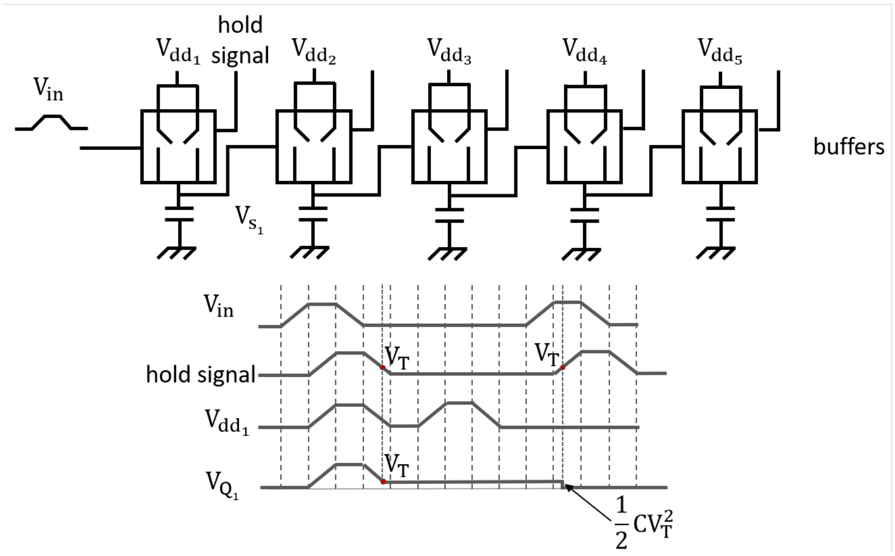


Figure 1.7: Quasi-adiabatic pipeline

$\frac{1}{2}CV_T^2$. Lowering the threshold voltage V_T results in less thermal dissipation. However, this reduction comes at the cost of increased static losses due to subthreshold leakage current, as previously discussed in the chapter.

For example, in 50 nm node MOSFETs, the typical supply voltage (V_{dd}) is around 1 V, while the threshold voltage V_T is around 0.3 V. The theoretical gain in dissipation of roughly one order of magnitude has a downside of increased complexity with an additional switch.

1.6 CMOS in adiabatic operation

Applying the classic MOSFET inverter architecture to the adiabatic principle results in the signal behavior illustrated in Figure 1.8. In phase 1, the input is set, turning the NMOS transistor on and pulling the output to zero. In phase 2, as the supply voltage increases, the PMOS transistor remains off because the source-gate voltage is below its threshold. During phase 3, the input voltage decreases, and once the source-gate voltage exceeds the threshold, the PMOS transistor turns on, allowing the output voltage to match the supply voltage. In phase 4, as the supply voltage decreases, the output voltage also drops but cannot reach zero. This occurs because when the supply voltage falls below the threshold, the PMOS transistor turns off, preventing the output from dropping further and holding its value until the next cycle.

The output signal has therefore a very different form from the (inverted) input signal. The application of adiabatic principle on CMOS is therefore more complex than simply changing the shape of the input signals to trapezoidal.

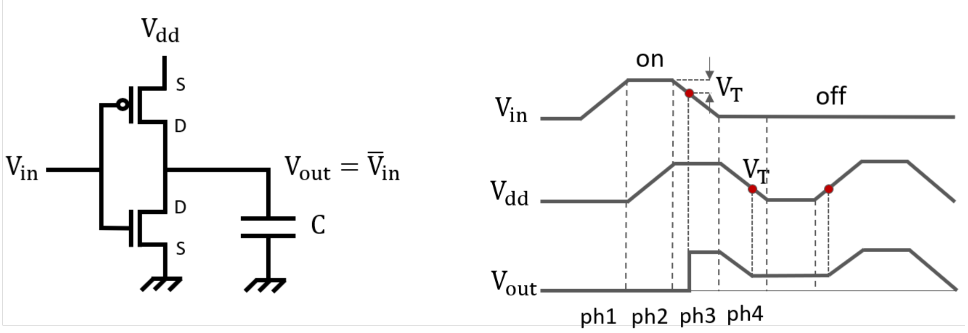


Figure 1.8: Incompatibility of CMOS architecture with adiabatic principle

1.6.1 Use of complementary gate

The above explained incompatibility of CMOS with adiabatic principle calls for different architectures that would circumvent the unwanted behavior due to threshold voltage.

The current solutions use a complementary gate to generate and stabilize a hold signal, V_{hold} (see Figure 1.9). This architecture processes both the input logical signals and their complements. Because the state is represented by two signals, it is referred to as dual-rail logic and is operated in four phases.

As an example, ECRL (Efficient Charge Recovery Logic) uses a pair of cross-coupled inverters and a complementary pass-transistor network to recover and reuse energy during the computation process [12]. PFAL (Positive Feedback Adiabatic Logic) is further improved by adding positive feedback to ensure the output remains stable during the evaluation phase [13].

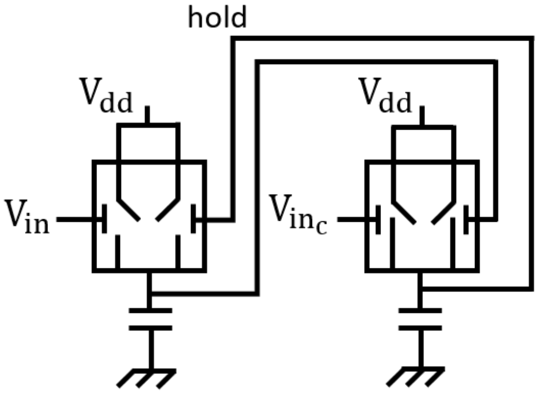


Figure 1.9: Use of complementary gate

It is therefore feasible to design CMOS architectures compatible with adiabatic principles. However, inherent non-adiabatic losses due to the threshold voltage remain a challenge, as these losses are deeply rooted in the physical properties of the technology and can only be marginally reduced. This limitation spurs interest in developing new technologies to overcome these intrinsic constraints and improve energy efficiency.

1.7 The interest in micro and nano relays

As discussed in the previous sections, CMOS technology faces inherent challenges in fully realizing the potential of adiabatic architectures. One of the primary issues is sub-threshold conduction, where current leakage occurs even when transistors are supposed to be off. This leakage leads to unwanted energy dissipation, undermining the efficiency gains of adiabatic computing.

Micro and nano relays, which function as mechanical switches, offer a promising alternative due to their extremely weak leakage currents when in the off state. When the switch is open, the air gap breaks the electrical path, preventing any current flow. Unlike transistors, relays can provide a near-perfect off state, dramatically reducing leakage currents and improving overall energy efficiency. Although relays have not been as extensively researched or developed as transistors, they did spark an interest as a candidate for transistor alternative.

Various mechanisms can be employed to actuate micro and nano relays, each with its own advantages and disadvantages [14, 15]. The primary actuation technologies include:

- **Magnetic Actuation**: Utilizes magnetic fields to move the relay contacts. This method can be effective but often requires complex and bulky external magnetic components, further requiring large power investment [16, 17].
- **Thermal Actuation**: Relies on thermal expansion to actuate the relay. While simple, it can be slow and energy-intensive, limiting its practicality for fast-switching applications [18].
- **Piezoelectric Actuation**: Uses piezoelectric materials that change shape when an electric field is applied. This method offers precise control but can be complex and expensive to implement [19, 20, 21].
- **Electrostatic Actuation**: Employs electrostatic forces to move the relay contacts [22, 23, 24]. This method is attractive due to its compatibility with microfabrication techniques and is the most studied one.

Electrostatic relays function by utilizing the Coulomb force generated between charged electrodes, involving a movable element (such as a cantilever beam or a diaphragm) and fixed electrodes. When a voltage is applied between these electrodes, electrostatic attraction forces the relay contacts to move, either opening or closing an electrical circuit. Figure 1.10 shows an example of a device with a suspended membrane proposed by [23].

While relays present an intriguing option, they come with their own set of challenges. Key limitations include:

- **Contact Reliability**: The mechanical nature of relays involves physical contacts that can wear out or degrade over time, affecting their reliability.
- **Relatively Large Size**: Compared to nanoscale transistors, relays tend to be larger,

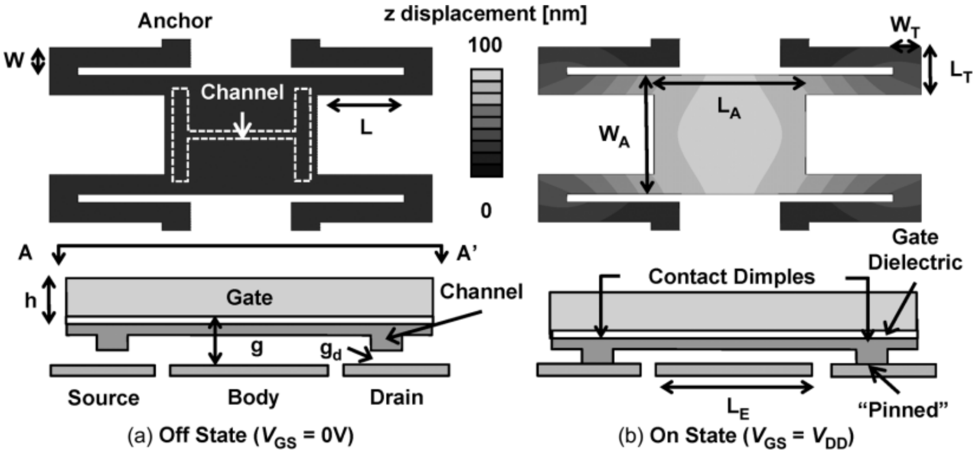


Figure 1.10: Micro-relay with a suspended membrane, taken from [23].

which can limit their integration density in microelectronic circuits.

- **Life Span**: The repeated mechanical movements in relays can lead to a finite lifespan, due to contact degradation and material fatigue due to stress and strain.
- **Speed limitation**: Due to the mechanical nature of their operation, which introduces inertia and damping, and response times that are dependent on actuation mechanism, the switching times are usually in the range of microseconds (compared to nano/picoseconds of MOSFETs). The speed is however scalable with the size of the devices.

As mentioned above, electrostatically actuated microrelays are the most widely studied ones. The simplest way to model the static behavior of micro relays is to model them as a membrane suspended by a spring and subjected to an electrostatic force (Figure 1.11). This system can also be considered as a capacitor having one fixed electrode while the second one is free to move once a electrostatic force is applied.

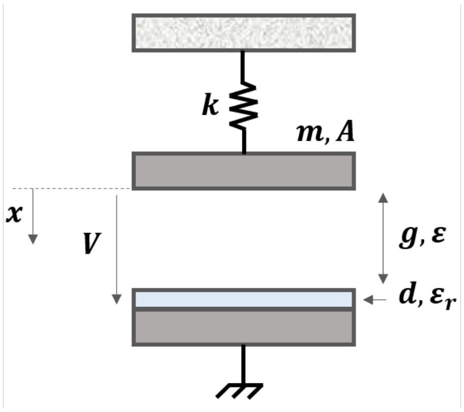


Figure 1.11: Dynamic model of a micro relay.

Without any applied voltage, g represents the initial gap between the electrodes. The electrodes are usually coated with a thin dielectric layer, to avoid short circuit between the plates. When a voltage V is applied, the resulting electrostatic attraction causes a displacement x of the upper electrode, altering the capacitance to:

$$C = \varepsilon \frac{A}{g - x} \tag{1.15}$$

The electrostatic force F_e generated in the relay is given by the equation:

$$F_e = \frac{1}{2} V^2 \frac{dC}{dx} = \frac{1}{2} \varepsilon V^2 \frac{A}{(g - x)^2} \tag{1.16}$$

where ε is the permittivity of the dielectric material between the electrodes and A is the area of the electrodes.

The restoring mechanical force, F_m, exerted by the spring on the movable electrode is directly proportional to the spring's stiffness, k, and the displacement from its original position, which represents the spring's extension.

$$F_m = -kx \tag{1.17}$$

At lower voltages, a stable equilibrium exists where the electrostatic force and the mechanical restoring force balance each other ($F_e + F_m = 0$). When the voltage exceeds a certain threshold, known as the pull-in voltage (V_{pi}), the electrostatic force overpowers the spring force, causing the movable membrane to contact the fixed plate. This pull-in voltage is the minimum voltage required to actuate the relay and can be calculated based on the equilibrium of forces.

$$V_{\text{pi}} = \sqrt{\frac{8kg^3}{27\varepsilon A}} \tag{1.18}$$

To release the contact, the voltage must be reduced to a value known as the pull-out voltage V_{po}. This voltage is typically lower than the pull-in voltage (V_{pi}), as less voltage is required to maintain the connection than to initiate it, meaning that there is hysteresis in the movement. The pull-out voltage can be determined through experimentation or detailed modeling.

Under dynamic conditions, the system's inertia and damping characteristics come into play, leading to more complex behavior. The voltage at which the movable element becomes unstable and pulls in under these conditions is known as the dynamic pull-in voltage, and is typically lower than the above derived static pull-in. These conditions have already been modeled in literature [25, 10].

In adiabatic architectures using micro-relays, the pull-out voltage can cause non-adiabatic dissipation $\frac{CV_{\text{po}}^2}{2}$ (similar to the $\frac{CV_{\text{T}}^2}{2}$ in CMOS). This dissipation can be lowered by optimizing the adhesive forces and geometrical parameters of the micro-relay. It can even be eliminated in an architecture based on a bistable relay, which would require additional electrode for the "restoring" signal. The remaining non-recoverable energy would then be the adhesive energy.

1.8 Capacitive nano device technology

In 2017, a team at CEA Leti introduced a novel approach to designing ultra-low-power combinational logic using a contactless method [26]. Figure 1.12 illustrates a basic comparison between a resistive-based buffer gate in non-adiabatic and adiabatic modes. They named this technique adiabatic capacitive logic (ACL). The output load C represents the capacitance of subsequent gates and interconnects. The timing sequence is similar to adiabatic logic, with the power supply being a trapezoidal voltage V_{PC}, known as the power clock, divided into four phases.

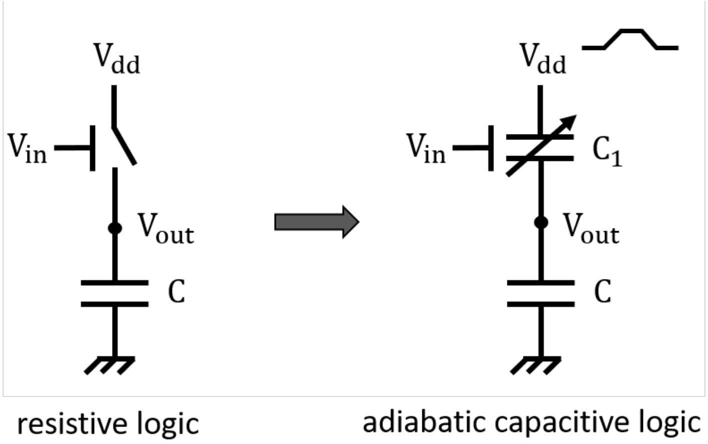


Figure 1.12: Basic principle of the Adiabatic Capacitive Logic for a buffer.

In this approach, the fundamental component is a variable capacitor (VC), referred to as C_1, which is controlled by an independent gate terminal V_G. For a negative-type VC device (NVC), the capacitance value decreases as the gate voltage V_G increases, as illustrated in Figure 1.13, where the nomenclature of the electrodes analogous to the one used for FETs is used (gate, source and drain).

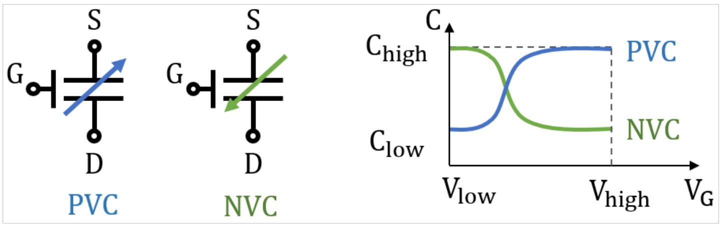


Figure 1.13: Characteristics of the variable capacitor (VC) device.

For a positive-type variable capacitor (PVC), the variation is reversed. By functioning as a variable capacitor, without establishing the electrical connection, physical contact between the two electrodes, S and D, is avoided. This enhances the mechanical reliability of the device and eliminates the requirement for low contact resistance. Additionally, this approach eliminates non-adiabatic dissipation that is present in micro relays due to hysteresis [27].

The output logic level from Figure 1.12 at any given time can be expressed as:

$$V_{\text{out}} = V_{\text{dd}} \frac{C_1}{C + C_1} \tag{1.19}$$

By using only NVC (negative-type variable capacitor) and PVC (positive-type variable capacitor) devices, it has been demonstrated in [26] that all combinational logic can be implemented in ACL. In this design, additional "hold" or "command" devices, which are typically required to maintain the logic state during the holding phase in resistive logic, are unnecessary. The output logic state is achieved by the charge and discharge of the output capacitor using the same device.

1.9 MEMS variable capacitor

In the following years, in the collaboration with ESYCOM, ESIEE, the group at CEA Leti has analyzed the possible implementations of variable capacitors. The most straight forward idea for implementation of variable capacitor is by coating the plates of a relay with a dielectric layer, that is, an approach with gap-closing MEMS devices.

In the study by Galisultanov et al. [28], the focus was on analyzing energy loss in capacitive adiabatic logic (CAL) gates built with gap-closing MEMS elements. This analysis was driven by the well-known issue of hysteresis in gap-closing variable capacitances, as mentioned earlier. When these capacitances charge, hysteresis causes energy loss due to kinetic impact during pull-in. During discharging, it results in the loss of stored mechanical energy during pull-out. To mitigate these losses, they proposed a gap-closing variable capacitance design with stoppers at the distance of $2g/3$, where pull-in typically occurs, which would prevent it from occurring. (Figure 1.14).

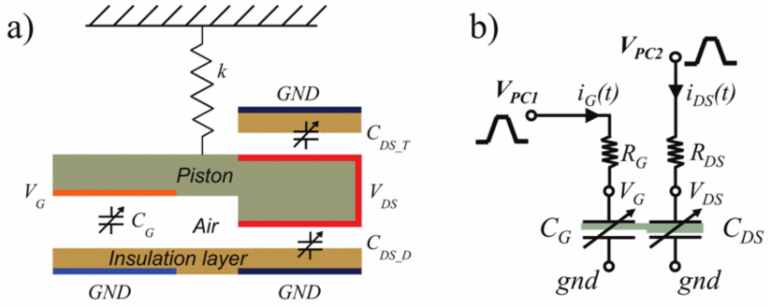


Figure 1.14: (a) Four-terminal gap-closing variable capacitor. (b) Test circuit. Figure from [28].

The device in question is a four-terminal gap-closing MEMS capacitive element. An analytical compact model of this variable capacitor was developed to understand all loss mechanisms. This design, using a four-phase power clock, demonstrated the possibility of cascadability, but also a non-adiabatic loss due to hysteresis in the output actuator.

To avoid the adiabatic loss, a solution without hysteresis and mechanical contact should be used for both electrical ports of the elementary CAL device. One way to achieve this is by using comb-drive actuators in the MEMS variable capacitance design, thereby eliminating mechanical contact. When the comb-drive fingers engage, the capacitance changes linearly with the displacement, resulting in a constant electrostatic force as the overlap changes. This force stability prevents the pull-in effect seen in parallel plate configurations. This investigation was undertaken by Perrin et al. [29, 30]. A solution for four-terminals variable capacitor was proposed (see Figure 1.15).

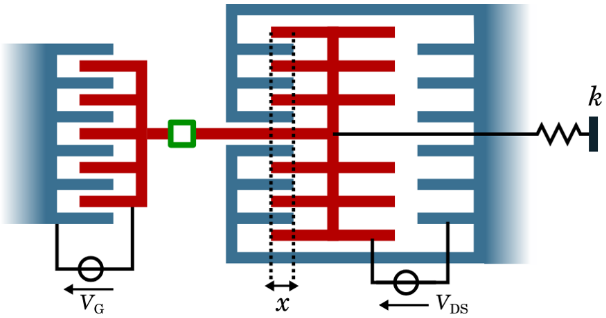


Figure 1.15: Sketch of the four-terminal variable capacitor studied in [29]. The blue combs are fixed to the substrate, while the red part is free to move along the x-axis and suspended over a spring with a stiffness k. The left comb-drive, controlled by V_G corresponds to the input electrodes. The right comb-drive is mechanically connected to the first one, but both are electrically insulated over mechanical link depicted with green square.

The comb-drive on the left functions as the input, while the one on the right serves as the output. Analogous to FET transistors, the input is controlled by a voltage denoted as V_G (gate voltage, with associated capacitance C_G), and the output voltage is referred to as V_{DS} (drain-source voltage, with capacitance C_{DS}). The symmetrical configuration of the output comb-drive is designed to render the system insensitive to the effects of V_{DS} when $V_G = 0$.

This design was advanced by Galisultanov et al. [31], who developed and simulated a series of buffer gates based on these comb-drive structures. However, a drawback of this design is the necessity of insulation on the movable part (represented with green square in the Figure 1.15). This insulation was necessary as the movable part needed to support two different voltages at the input and at the output stage. The challenge arose from the complexity of the fabrication process required to create this mechanical, but electrically insulating link.

In their study [32], Samaali et al. designed a combination of input electrodes using comb-drive structures and output electrodes using gap-closing structures (Figure 1.16).

They conducted electromechanical simulations and demonstrated cascadability of both buffers and inverters.

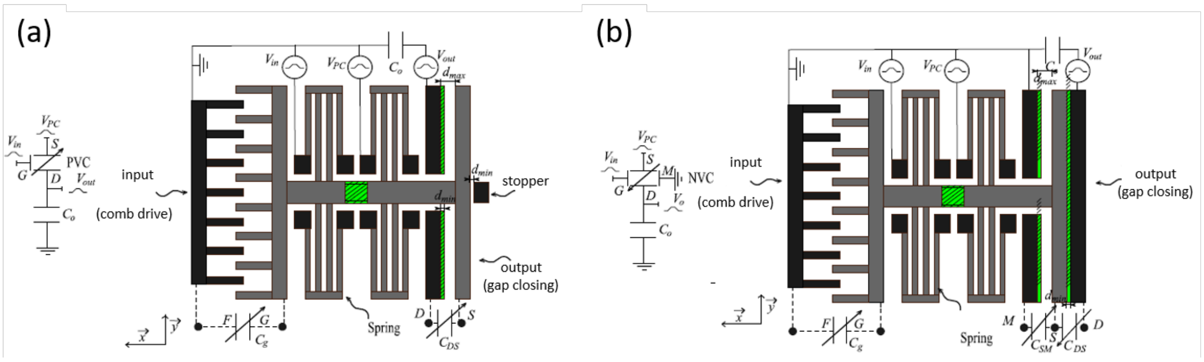
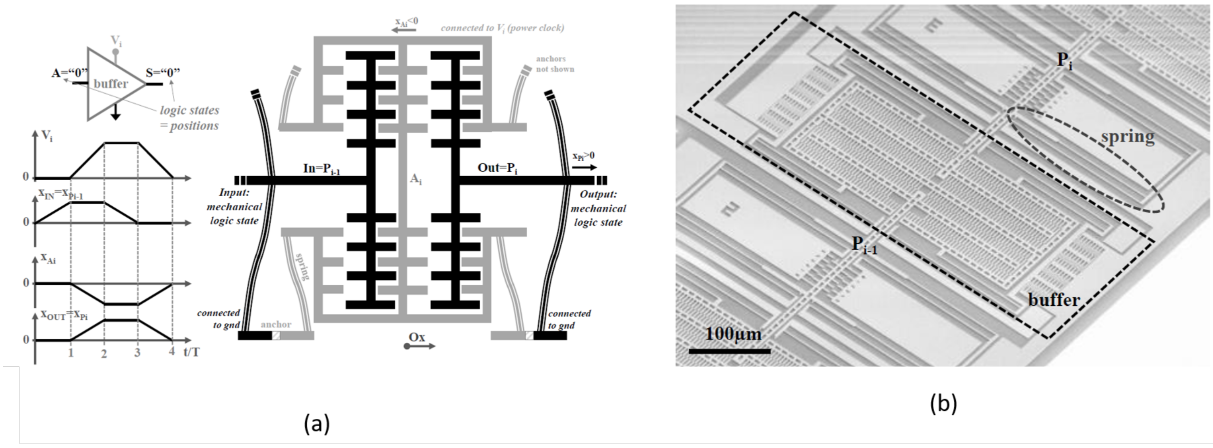


Figure 1.16: Electromechanical implementations of a four terminal variable capacitor with comb drive and gap closing structures. a) Implementation of a buffer with a PVC. b) Implementation of an inverter with a NVC. Figure from [32].

Their design featured a critical dimension of 40 nm, with simulations showing energy dissipation of 0.9 fJ, comparable to that of nano-scale FET transistors. Due to the cubic scaling of energy consumption with size, reducing the dimensions by an order of magnitude could lower the energy consumption to the attojoule range. However, the presence of dielectric insulation remains a challenge, complicating the microfabrication process.

The first experimental demonstration of this new electromechanical adiabatic logic family, operating without any electrical or mechanical contacts, was conducted by Perrin et al. [33]. They designed and fabricated a pipeline of four voltage-controlled (VC) devices based on comb-drive structures using standard MEMS microfabrication techniques (Figure 1.17). The EMAC pipeline functioned effectively up to 170 °C, which was the maximum temperature achievable with their experimental setup. Simulations indicated an energy dissipation of 0.1 pJ per operation at 2.5 kHz, with potential for further reduction as gate size decreases. However, their implementation had a drawback: both the active and the passive electrodes, that is, the signal-carrying and the grounded ones were suspended above the substrate by springs. This configuration was prone to out-of-plane interactions between the active electrodes and the substrate, causing vertical motion and risking potential pull-in. Additionally, information was transmitted between gates via a mechanical link, complicating and limiting the routing of information within the circuit compared to electrical links and increasing the overall movable mass of the devices.

Table 1.1 summarizes the properties of the circuits based on variable capacitors (Adiabatic Capacitive Logic) with respect to other computing paradigms.



(a)

(b)

Figure 1.17: a) Buffer logic gate in EMAC when the input logic state is "low". b) SEM picture of an EMAC buffer gate within a pipeline. Figure from [33]

	CMOS	µ/n relays	CACL
Electrical conduction path	Yes	Yes	No
Mechanical contact	N/A	Yes	No
Logic state coding	Charge	Resistance	Position
Leakage currents	Yes	No	No
Adiabatic compatibility	No	Yes	Yes
Mechanical reliability	N/A	No	Yes
Energy dissipation	10^{-18}J	10^{-15}J*	10^{-12}J*
Energy reversibility	No	No	Yes
Frequency range	GHz	MHz	kHz*
Maximum temperature	125°C	500°C	170°C

Table 1.1: Comparison between CMOS, micro/nano relay and ACL technologies. *Scales with the operation frequency and size of the device.

1.10 The interest in Dual Rail architectures

The "standard" four-terminal approach, developed since Pillonnet et al.'s introduction of the adiabatic principle using variable capacitors [26], has shown some limitations. These include microfabrication difficulties due to presence of the electrical insulation between the input and output stages, the risk of pull-in, and mechanical transportation of the information, as previously discussed.

The potential of this technology and the advancements made over the years led to the creation of the ZerÔuate project and subsequent ANR funding to further explore adiabatic computation based on variable capacitors. ZerÔuate project includes four institutions: CEA Leti, LAAS-CNRS, CNRS-G2ELAB and ESIEE-ESYCOM. The project aims to develop a dual-rail architecture for variable capacitors, which would be more stable against parameter variations and the presence of fringing fields. This architecture would also allow the grounding of movable parts, enhancing the device's overall stability and avoiding the electrical insulation within the movable part, simplifying largely the fabrication. Additionally, signal transmission could occur between the output of one device and the input of the next through electrical interconnections rather than mechanical links.

Figure 1.18 presents a simplified mechanical schematic of a dual-rail architecture using comb-drive actuators, along with the principle for controlling the movement direction of the movable electrode based on the combination of input signals.

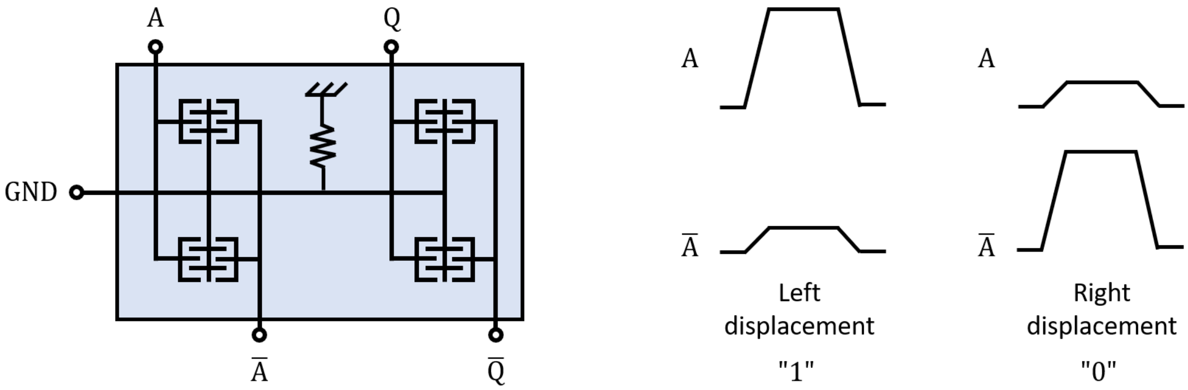


Figure 1.18: Simplified mechanical schematics of a dual-rail architecture and state coding with two complementary signals.

Unlike the standard configuration, where the state "1" is represented by a displacement and the state "0" by a resting position, the dual-rail configuration encodes both states as displacements in *opposite* directions. The goal of this thesis is to investigate this concept, develop the design, model the behavior, and ultimately fabricate and characterize the devices. This will experimentally validate the concept and demonstrate working logic gates and pipeline operations. These aspects will be explored in detail in the subsequent chapters.

2

Study of the dual rail logic

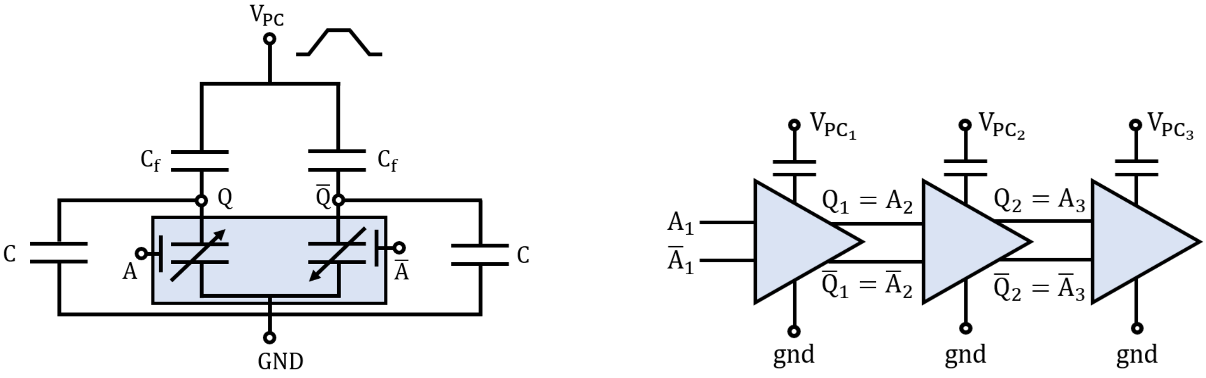
This chapter starts with the introduction of the ZerÔuate project and Complementary Capacitive Adiabatic Logic (CACL), proposing comb-drive actuators as the solution for implementation and explaining the operating principle. It then proceeds with the behavior modeling of the comb-drive actuators, based on the analytic description and FEM simulations. It further covers the benefits of the unconventional operation of comb-drives (with no initial finger coverage) and shows that the contribution of the fringing fields can be exploited to lower down the dissipation during the logic state computation. Finally, the models serve as a base for designing the elementary variable capacitor component, as well as a full inverter gate, simulating the transport of the information as well as the energy invested in the coding.

2.1 Dual-rail adiabatic capacitive logic

The previous chapter has introduced the challenges in reducing the energy consumption in digital circuits and obstacles that current technologies are facing, highlighting their limitations. We have also pointed out the interest in new technological approaches that could support adiabatic way of operation. The objective of the ZerÔuate project, that this thesis is part of, is to propose compact and reliable MEMS-based devices to enable the operation of a highly energy-efficient computing principle that diverges significantly from the current state of the art. The previously introduced limitations of CMOS and µ-relay technologies have inspired a new computing paradigm, both on device and system levels.

The team at CEA Leti has formerly introduced the principle of "soft and contactless logic" (SCL) [26], with the idea to combine gradual and reversible transformation of information coding with contactless manipulation achieved through electrostatic interaction with variable capacitors. Contactless operation gets rid of the physical connection between the power supply and the ground and therefore eliminates static losses due to leakage currents. The absence of physical contact during switching increases robustness of the devices. Capacitive transduction allows recovering of the invested electromechanical energy through charge transfer with the power supply.

The objective is to circumvent the causes of static and dynamic losses in logic circuits, aiming for energy dissipation approaching zero during quasi-static operation. In the initial phase of the project, the team in CEA Léti studied and designed a basic system of logic gates that meet the SCL criteria. Architecture of dual rail (complementary) logic was proposed, resulting in a term Complementary Adiabatic Capacitive Logic (CACL) that will from this point onward be used. In this work, the term "complementary" will be used to refer to signals A and $\bar{A}$, or Q and $\bar{Q}$. The electrical schemes of an inverter gate and cascade of gates are shown in the Figure 2.1.



(a) **(b)**

Figure 2.1: Electrical schematics of a gate. (b) Schematic of a cascade of multiple gates with the outputs of each gate serving as the inputs of the consecutive one.

The physical implementation of this principle posed one of the first obstacles, as the conventional transistors are not compatible with the envisaged principle and therefore can't ensure ultimate energy dissipation ($< 100\ k_{\mathrm{B}}T$). The key challenge for implementing the elementary CACL devices is being able to define a robust, contactless hardware technology for realization of variable capacitor (VC) components. The extensive discussions within the consortium on various MEMS topologies (planar, out-of-plane, gap-closing, comb-drive) and actuation principles (electrostatic, piezoelectric, magnetic) focused on the feasibility of implementing the CACL paradigm. Criteria considered included device size, technological risk, breakdown effect, and mechanical contact. Motivated by past project experience, parameter robustness, fabrication ease, electric field constraints, and performance potential, combdrive actuators were identified as viable candidates for VC implementation (Figure 2.2).

Comb-drive structures have been massively employed in MEMS devices since the 1990's as actuators, sensors and resonators, and have proven their usability for applications like inertial sensors [34, 35], micro-opto-electromechanical systems [36], or microgrippers [37] among many others. Numerous studies have been made about their properties, operation and limitations. They are basically composed of two interdigitated sets of fingers, with one set being fixed while the other is connected to a flexible suspension. Combdrive capacitance depends on distance between the two sets of fingers. It is regulated by a balance between

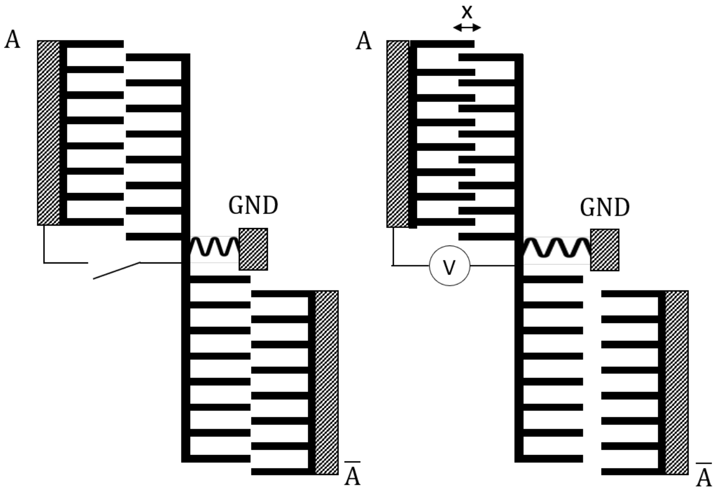


Figure 2.2: Comb-drive actuators as variable capacitors in complementary configuration..

the electrostatic force, dependent on the applied voltage, and the mechanical restoring force of the flexible suspension, influenced by the stiffness of the springs.

This design allows for control over the dynamics of MEMS displacement over a wide range ($\approx$ a few micrometers). When the comb-drive fingers engage, the capacitance changes linearly with the displacement, resulting in a constant electrostatic force with respect to overlap. This constant force (dependent on the square of the voltage) is advantageous for actuators as it prevents the pull-in effect seen in parallel plate configurations. For sensors, it offers a linear relationship between force or displacement and capacitance variation. The comb-drive design achieves high capacitive contrast (up to 10 times), ensures energy reversibility, has almost zero static power consumption, operates at a reasonable actuation voltage (tens of volts), and eliminates contact issues, ensuring the reliability of the structure without mechanical contact.

As aforementioned, the project was carried out as part of a large consortium, with different members addressing various aspects of the device design. Specifically, CEA Leti focused on system-level analysis, examining key parameters such as the spring constant, input and output capacitances, and fixed capacitance. Their goal was to determine the relationships among these parameters to ensure the operation of the inverter gate and produce output voltages suitable for driving the next gate in a complex digital circuit. Starting from CEA system level analysis, the individual components of the system were investigated and designed within this thesis work in order to implement a gate based on our MEMS technology. This "low-level" investigation involved studying the precise behavior of comb-drive structures as the overlap between opposing fingers changed. The findings were used to refine the model employed by CEA Leti and enhance their simulations. This manuscript will describe in detail only the research carried out in this thesis work and solely present the parameters provided by CEA Leti's simulations.

2.1.1 Concept of an inverter gate

The CACL inverter gate consists of two complementary inputs (A and $\bar{A}$) and generates two complementary outputs (Q, $\bar{Q}$). The inputs and outputs are mechanically connected by the shuttle beam, movable along x-axis. The shuttle is grounded to avoid vertical electrostatic forces towards the substrate and thus any vertical displacement/actuation and pull-in effect, which would cause a failure of the device. They are electrostatically coupled by interdigitated fingers (N_A, N_Q) of width d and separated by an air gap g. Unlike traditional logic gates that use constant high and low voltage levels to represent binary states (0 and 1), CACL principle relies on pulse logic, which uses the presence or absence of pulses within specific time intervals to encode information. The input voltages differentially actuate the movable part through electrostatic comb-drive influence, where movement in the positive or negative x-direction encodes the logical state for transmission between the input and output. This displacement modification creates a variable capacitance at the terminals of the two outputs (Q and $\bar{Q}$). Adding a fixed capacitance (C_f) coupled with an alternating power supply encodes information in voltage by creating a variable capacitive ratio depending on the logical state at the input. Thus, the outputs (Q and $\bar{Q}$) are voltage signals with amplitudes modulated by the logical state, which serve as the electrical signals controlling the next gate.

Adiabatic operation of a CACL inverter

The Figure 2.3a illustrates the applied (trapezoidal, according to adiabatic principle) signals A and $\bar{A}$, power clock signal V_PC which is applied with a time delay T, as well as the established output voltages V_Q and $V_{\bar{Q}}$. The gate operates over a time period of $4T$, with 4 phases of equal duration T. Signals at the complementary inputs (or outputs) are time-varying signals. They vary from 0 to a maximum value which is either V_H or V_L. If one of the input (output) electrodes reaches V_H, the complementary one reaches V_L. Figure 2.3b shows the position of the device at the end of each of the four phases of the operation.

In **phase 1**, signals A and $\bar{A}$, with respective amplitudes V_H and V_L, are applied. Two electrostatic forces act on the beam. Due to the symmetry of the air gaps (g), the beam experiences a greater force from electrode A because $V_\mathrm{H} > V_\mathrm{L}$. At the end of **phase 1** (called **set phase**), the beam has moved to the left by a distance $|x|$. As the movable output electrodes are mechanically connected to the input ones, this *pre-actuation* causes the output comb Q to be engaged while the comb $\bar{Q}$ becomes disengaged.

In **phase 2** (called the **evaluation** phase), the V_{PC} signal is gradually applied through the capacitive bridge formed by the fixed capacitors and the equivalent capacitance of nodes Q and $\bar{Q}$, establishing the output voltages:

$$V_Q = \frac{C_\mathrm{f}}{C_\mathrm{f} + C_Q} V_{PC} \qquad V_{\bar{Q}} = \frac{C_\mathrm{f}}{C_\mathrm{f} + C_{\bar{Q}}} V_{PC} \tag{2.1}$$

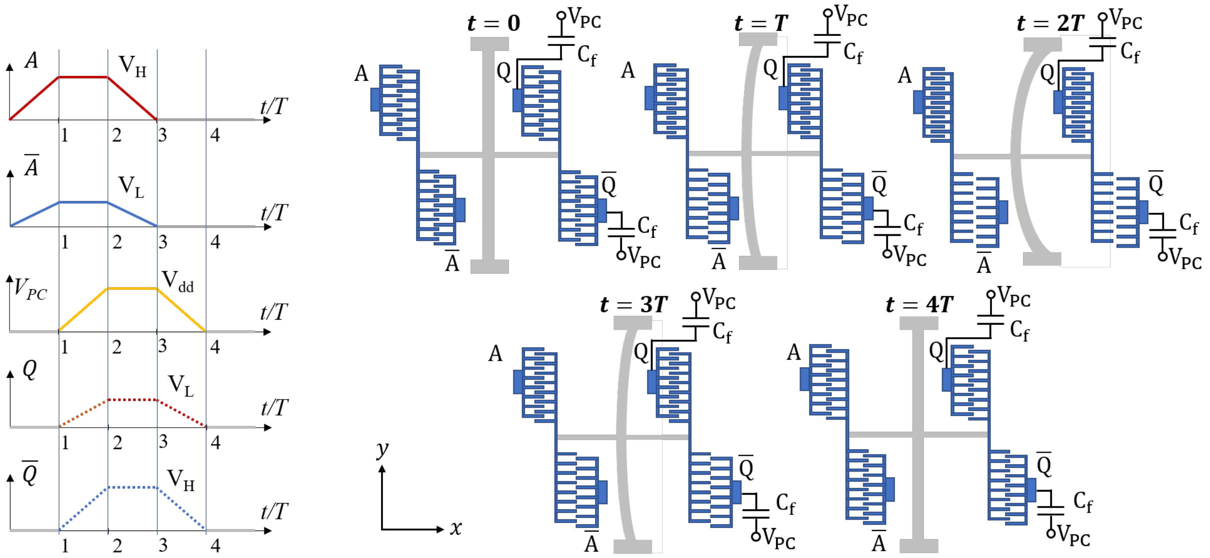


Figure 2.3: Encoding and transportation of logic state “1” through the inverter gate in four phases. Left: Applied and established voltage signals. Right: Displacement of the combs during encoding of state “1” during the period $0 < t \leq 4T$.

As the comb $\bar{Q}$ is disengaged, the force it exerts on the whole system is negligible compared to the force exerted by Q. The input’s pre-actuated movement is enhanced in the same direction ($|x(2T)| > |x(T)|$). At the end of this phase, as $C_Q > C_{\bar{Q}}$, the established output voltage at Q will be reach the value V_L, while the one of $\bar{Q}$ will reach V_H. This establishment of output voltages $V_Q < V_{\bar{Q}}$ is therefore inverted from the input signals.

In **phase 3** (called the **hold phase**), the input signals A and $\bar{A}$ are gradually reduced down to ground. At the beginning of this phase only one output comb (in this example Q) is engaged and generates a significant force, while the force within the other comb ($\bar{Q}$ is negligible). Therefore, despite the removal of the input signals, the position is kept stable, even though $V_Q < V_{\bar{Q}}$.

In the **Phase 4** (called the **recovery phase**) the V_{PC} signal is gradually decreased, bringing the movable electrodes back towards their central position.

The same reasoning applies when A and $\bar{A}$ represent a logical low state, meaning their roles are reversed. The movement of the beam would be towards the "right" (positive x-direction).

2.1.2 Down-scaling of physical dimensions

Down-scaling MEMS devices leads to lower energy dissipation due to decreased mass, surface area, and improved heat dissipation. At the same time, actuation voltages are reduced because of the increased effectiveness of electrostatic forces and enhanced electric fields at smaller scales. This makes down-scaled MEMS devices more efficient and easier to operate with lower power requirements. A study has been carried by CEA-LETI at the beginning of the project and the impact of down-scaling with the factor α on different aspects of the MEMS gate is presented in Table 2.1.

Down-scaling factor α	
Linear sizes	$1/\alpha$
Occupied area	$1/\alpha^2$
Mass	$1/\alpha^3$
Spring constant	α
Resonance frequency	α
Capacitance	$1/\alpha$
Actuation voltage	$1/\alpha$
Energy loss	$1/\alpha^2$

Table 2.1: Impact of the downscaling of physical dimensions of the gate on related values.

2.2 Analytic and FEM modeling of the combs

Understanding the behavior of MEMS devices under various conditions is essential for designing them to be efficient, reliable, and high-performing. Analytical modeling is a fundamental tool that uses basic principles of physics and engineering to methodically break down the complex behavior of MEMS structures, allowing us to predict their real-life performance. These models also help identify the most critical components of a MEMS device and determine which parameters most significantly affect overall performance.

In our proposed device, the key to gate operation lies in the behavior observed during phases 2 and 3. Despite a lower output voltage at Q (due to $C_Q > C_{\bar{Q}}$), the force generated by C_Q is greater than that by $C_{\bar{Q}}$. This occurs because comb-drive Q is "engaged" while combdrive $Q_{\bar{Q}}$ is "disengaged." However, due to the presence of fringing electric fields, this mechanism is complex, necessitating a thorough examination of the comb capacitance. Specifically, it is crucial to analyze both the capacitance and the capacitance gradient (which is proportional to the electrostatic force) in configurations with near-zero overlap. This analysis will help determine if gate operation is feasible, based on the initial overlap of the comb fingers and the displacement caused by pre-actuation.

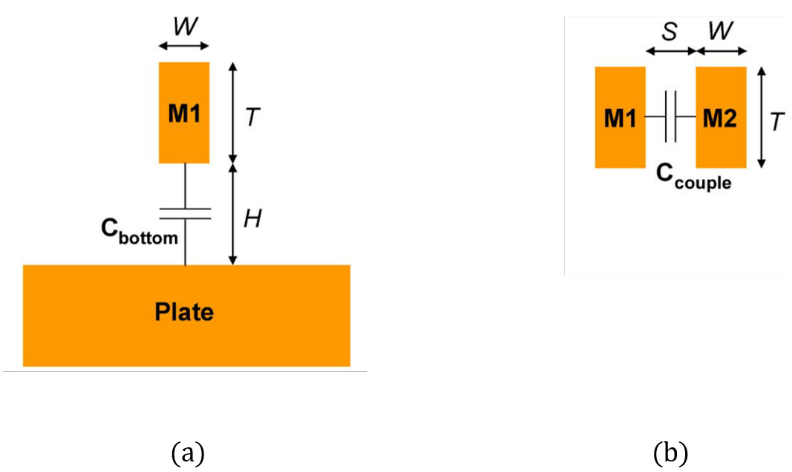
In the following sections, the analytical model of the capacitance within the comb-drive structure will be presented and compared to the model derived from FEM data.

2.2.1 Analytical model based on electrical field decomposition

The traditional formula for calculating the capacitance of a plate-to-plate capacitor, given by $C = \varepsilon S/d$, where ε is the permittivity of the medium in the capacitive gap, S is the surface of the plates and d their distance, is straightforward and provides reasonably accurate results when fringe effects are negligible. However, this equation becomes significantly inaccurate when fringe effects are prominent. In [38], a model was proposed based on a detailed analysis of the electric fields between lines and plates. This model decomposes the total capacitance into distinct components: plate capacitance, fringe capacitance, and terminal capacitance. Each component's value is derived from the localized and independent electric field associated with it. Moreover, the effects of electrical field shielding and charge sharing are considered and integrated into the model in the case of multiple electrodes.

EFD principle and general cases

In their article, [38] described different types of basic components that can be found the in back-end-of-the-line (BEOL) structures. Among them, they investigated a case of a single line above one plate, as well as parallel lines above one plate (see Figure 2.4). These two types of structures are a good representation of the geometry present in the comb-drives that are the subject of this thesis and are the ones that will be presented in the following.



(a) (b)

Figure 2.4: Capacitance components between (a) a line and a plate and (b) two parallel lines. These components represent well the capacitance between the fixed comb and the substrate (a), as well as the capacitance between the fingers of the opposing electrodes during the overlap (b). The illustrations are taken from [38].

The designations for dimensions of the structures that they used are T for wire thickness, W for wire width, S for wire space, and H for the distance between the wire and the plate.

For the basic structures in Figure 2.4, Figure 2.5a shows the equal potential contours derived by an electromagnetic field solver. The distribution of the electrical field is then derived (black lines in Figure 2.5a), allowing the approximate partition into separate regions whose boundaries are represented with dotted lines in Figure 2.5b. This partition allows description of each separate region and subsequent sum-up of distinct contributions to obtain the total capacitance.

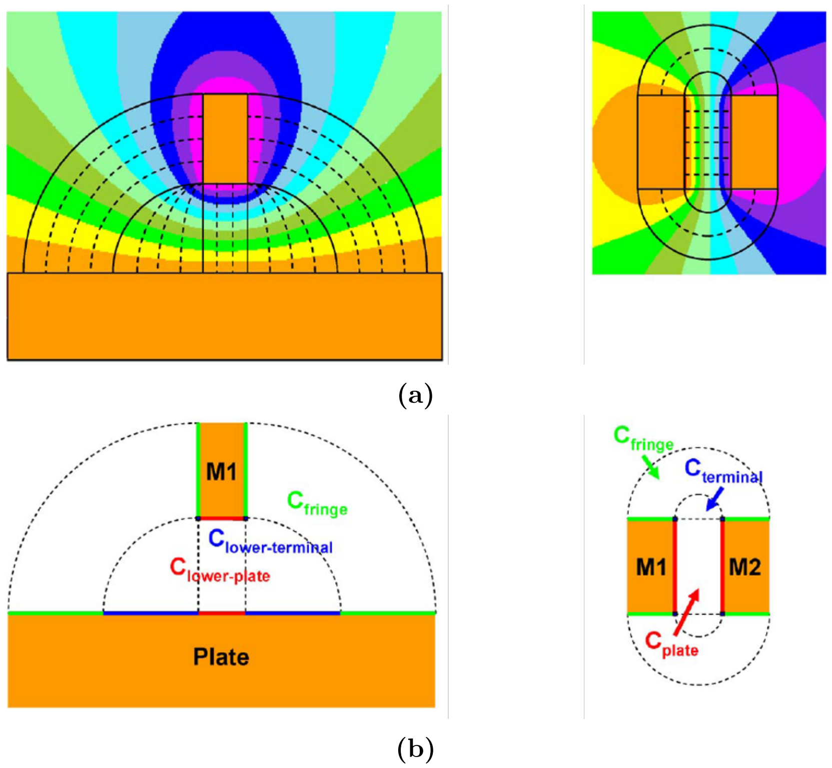


Figure 2.5: Distribution of electrical fields. (a) Equal potential contours from electromagnetic field solver and the corresponding electrical field distribution. (b) Decomposition of electrical fields. The illustrations are taken from [38].

Based on this electrical field decomposition (EFD) approach, the components of the total capacitance from the Figure 2.5b can be classified as:

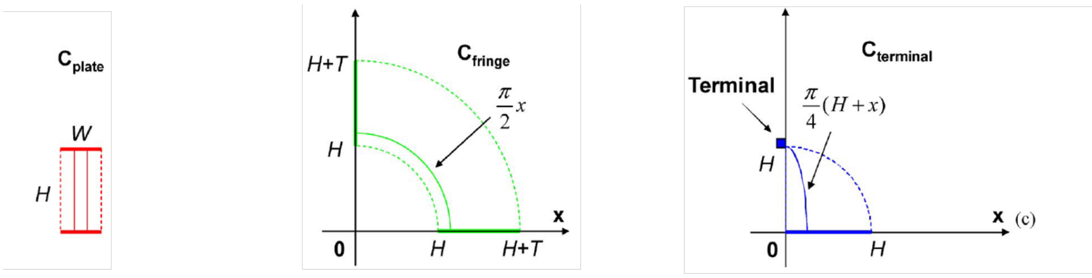
1. Plate capacitance: between two parallel metal surfaces (in our case between the bottom surfaces of the fingers and the substrate or between the side-walls of the interdigitated fingers).
2. Fringe capacitance: from the side walls of the structures (ex. comb-fingers) to another perpendicular surface, which would in our case be the substrate.
3. Terminal capacitance: from the corner of the structure to other metal surfaces.

For each of these cases Figure 2.6 shows the schematic of the electric field.

The plate capacitance can be calculated with the well-known $\frac{C_{\text{plate}}}{\varepsilon} = \frac{W}{H}$. The fringe capacitance can be approximated by observing the electrical field lines as arcs of a circle with radius ranging from H to $H + T$ on the substrate surface (Figure 2.6b). We can therefore obtain its value by integrating:

$$\frac{C_{\text{fringe}}}{\varepsilon} = \int \frac{\text{width}}{\text{distance}} = \int_{H}^{H+T} \frac{dx}{\frac{\pi}{2}x} dx = \frac{2}{\pi} \ln\left(1 + \frac{T}{H}\right) \tag{2.2}$$

Similarly, we can obtain the approximation of the terminal capacitance, by integrating



(a) (b) (c)

Figure 2.6: Fields of three basic components. (a) Parallel-plate capacitance. (b) Fringe capacitance. (c) Terminal capacitance. The illustrations are taken from [38].

the range of such a field from 0 to H along the x-direction (Figure 2.6c).

$$\frac{C_{\text{terminal}}}{\varepsilon} = \int \frac{\text{width}}{\text{distance}} \approx \int_0^H \frac{dx}{\frac{\pi}{4}(H+x)}\, dx = \frac{4}{\pi} \ln 2 \tag{2.3}$$

The total capacitance of an isolated structure suspended over substrate (like the one from Figure 2.5) can be obtained by summing up the individual contributions:

$$C_{\text{total}} = C_{\text{plate}} + 2C_{\text{fringe}} + 2C_{\text{terminal}} \tag{2.4}$$

Electrical field shielding and charge sharing

When there are multiple structures, some field lines do not terminate on a single conductive surface but instead land on neighboring structures. This phenomenon is known as the shielding effect when multiple neighboring structures are involved. For example, Figure 2.7a illustrates the fringe capacitance component C_{fringe} of the coupling capacitance C_{couple}. Only part of the electric field originating from the lower surface of M1, within W_1, reaches the lower sidewall of M2. The rest of the field is blocked by the plate beneath. Consequently, C_{fringe} stops increasing with W once W exceeds $H_{\text{B}} - S/2$.

Another significant effect in the case of multiple structures is the charge sharing effect. This effect occurs when the electric field from one conductor is shared by two or more surfaces. An example is shown in Figure 2.7b. The electric field originating from the right sidewall of M1 within T1 can couple with both the underlying plate and M2. Consequently, the total charge within T1 is distributed between the plate and M2. This causes the plate capacitance C_{plate} between M1 and M2 to be less than the original value of T/S. The model that was introduced in [38] to account for the charge sharing effect is the following:

(a) (b)

Figure 2.7: Effects of (a) field shielding and (b) charge sharing. The illustrations are taken from [38].

$$
\begin{aligned}
\bar{C_1} &= C_1 \cdot \frac{C_1}{C_1 + C_2} = \frac{C_1^2}{C_1 + C_2} \\
\bar{C_2} &= C_2 \cdot \frac{C_2}{C_1 + C_2} = \frac{C_2^2}{C_1 + C_2}
\end{aligned}
\tag{2.5}
$$

where C_1 and C_2 are the capacitances between two electrodes without considering charge sharing, and $\bar{C_1}$ and $\bar{C_2}$ are the capacitances when charge sharing is taken into account.

EFD applied on comb-drive structures

When applying the EFD approach to model a single comb structure depicted in Fig. 2.8, we divided the capacitance in 14 elementary components. Note that for simplicity in calculations, we assumed here a square shape for the finger tips. The capacitance calculation includes three main types of contributions: varying capacitance C_{v}, which depends on the degree of overlap and is formed within the comb-drive structure, the constant component C_{fix}, arising from the fixed electrode and the substrate, which remains unchanged across the whole range of overlap, and non-linear contributions, C_{nl}, such as those from fringing electric fields.

The physical and geometrical parameters used for modeling are indicated in Table 2.2. The choice of finger gap and width (d) was dictated by the achievable critical dimensions in terms of lithography and etching. In the common configuration of most comb-drive structures the gap equals the finger width.

To obtain the variation of capacitance with respect to the finger overlap, we separated the overlap region in four different sections based on different contributions: $u < -3d/2$, $-3d/2 \leq u < -d$, $-d \leq u < 0$ and $u \geq 0$. We divided the capacitance in 14 elementary components and described the total analytical capacitance as $C_{\mathrm{an}} = C_{\mathrm{fix}} + C_{\mathrm{nl}} + C_{\mathrm{l}}$. The

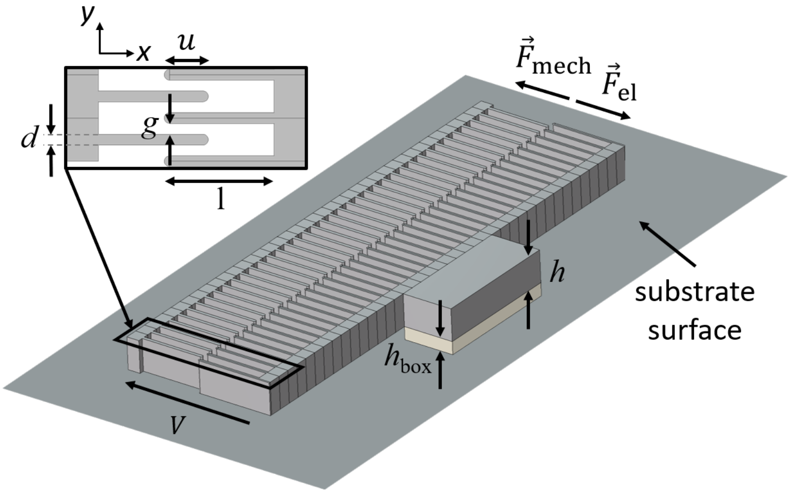


Figure 2.8: Schematic of a comb-drive actuator used for analytical and FEM modeling with h being the thickness of the device, h_{box} the thickness of buried oxide, l the length of the fingers, d their width as well as the gap between them and u being the overlap between the combs. The structure is suspended above a silicon substrate, grounded in the simulations. Fingers are modeled rounded in the FEM simulations, as this form represents better the shape of the fingers after microfabrication.

Table 2.2: Parameters of the comb structure used in simulations.

Parameter	Description	Value	Unit
E	Young's modulus of silicon	170	GPa
ε_0	Vacuum permittivity	$8.854 \cdot 10^{-12}$	F/m
ε_r	Relative permittivity of silicon oxide	4.2	
h	Thickness of the silicon layer	5	µm
h_{box}	Thickness of the oxide layer	2	µm
l	Length of the fingers	10	µm
d	Finger width and gap	0.5	µm
N	Number of fingers in the comb	60	

elementary components are described in Table 2.3.

Based on the EFD approach, the above mentioned contributions can be attributed to one of the three types: plate, terminal or fringe capacitance, as shown in the Table 2.4 and described using equations 2.2−2.5 introduced formerly.

Each of the four sections of the capacitance curve can then be described as follows:

Table 2.3: Description of capacitance contributions based on EFD approach.

Contribution	Capacitance description
C_1	Plate capacitance between the bottom of the device and the substrate
C_2	Anchor: fringe, bottom terminal, upper terminal cap
C_3	Fringe capacitance from the sides of the last two fingers to the substrate
C_4	Total bottom terminal capacitance from middle fingers to the substrate
C_5	Total bottom terminal capacitance from the last fingers to the substrate
C_6	Top terminal capacitance from the last fingers to the substrate
C_7	Fringe, bottom and top terminal capacitance from finger tips to the substrate
C_8	Fringe capacitance from the sides of the middle fingers
C_9	Fringe capacitance between finger tips and the finger sides
C_{10}	Terminal capacitance between finger tips and the finger tips
C_{11}	Plate to plate capacitance between vertical finger walls
C_{12}	Fringe capacitance from the sides of the middle fingers where there is overlap
C_{13}	Fringe capacitance from the sides of the middle fingers where there is no overlap
C_{14}	Fringe capacitance between the bottom plates of the fingers

Table 2.4: Capacitance types for each of the capacitance contributions, as described by EFD approach.

Capacitance type	Contributions
Plate capacitance	C_1, C_{11}
Terminal capacitance	C_2, C_4, C_5, C_6, C_7, C_{10}
Fringe capacitance	C_2, C_3, C_7, C_8, C_9, C_{12}, C_{13}, C_{14}

$$\begin{aligned}
&\underline{u < -3d/2}\\
&C_{\text{fix}} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 = C_1 + C_{\text{par}}\\
&C_{\text{nl}} = C_7 + C_8 + C_{10}\\
&C_{\text{l}} = 0\\
&\underline{-3d/2 \leq u < -d}\\
&C_{\text{fix}} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 = C_1 + C_{\text{par}}\\
&C_{\text{nl}} = C_7 + C_8 + C_9 + C_{10}\\
&C_{\text{l}} = 0\\
&\underline{-d \leq u < 0}\\
&C_{\text{fix}} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 = C_1 + C_{\text{par}}\\
&C_{\text{nl}} = C_7 + C_8 + C_9 + C_{10}\\
&C_{\text{l}} = 0\\
&\underline{u \geq 0}\\
&C_{\text{fix}} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 = C_1 + C_{\text{par}}\\
&C_{\text{nl}} = C_9 + C_{10} + C_{12} + C_{13} + C_{14}\\
&C_{\text{l}} = C_{11}
\end{aligned} \tag{2.6}$$

The dashed line plotted in Fig. 2.9 represents the capacitance value of the comb-drive structure based on this analytical model. The MATLAB code used for obtaining this Figure is available in Appendix A.

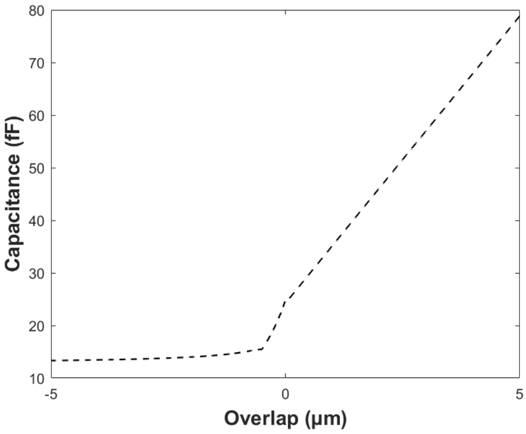


Figure 2.9: Analytical model of the variation of the capacitance with respect to the overlap between the comb-drive fingers, based on electrical field decomposition. Capacitance has three different contributors: variable capacitance formed by the comb electrodes (overlap dependent), constant component, formed by the fixed electrode and substrate (remains unchanged across overlap range) and non-linear contributions like fringing fields.

In the region where the overlap is highly negative, the calculated capacitance value remains relatively constant. Here, it is primarily determined by the capacitance formed between the polarized fixed electrode and the grounded substrate. An approximation of this capacitance can be obtained using the formula:

$$C_{\mathrm{fix}} = \frac{\varepsilon_0 (S_{\mathrm{comb}} + \varepsilon_r S_{\mathrm{fix}})}{h_{\mathrm{box}}} + C_{\mathrm{par}} \tag{2.7}$$

Where S_{comb} is the surface area occupied by the combs and S_{fix} is the surface area of the fixation. C_{par} designates parasitic contributions like fringe and terminal capacitances that are independent of the overlap. As the overlap between the comb fingers approaches zero, the fringing electric fields start contributing significantly to the capacitance. When the overlap becomes positive, the capacitance increases rapidly, with the dominant factor being the capacitance formed between the interdigitated fingers. This capacitance augmentation is linearly dependent on the overlap and can be described by the well known formula:

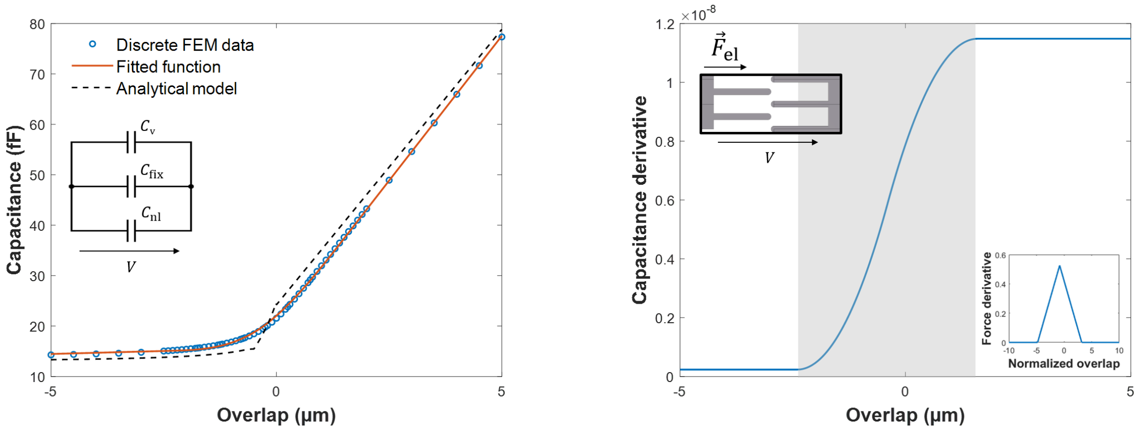
$$C_{\mathrm{v}}(u) = 2N\varepsilon_0 \frac{uh}{d} \tag{2.8}$$

Where N is the number of fingers in a single comb electrode and u is the overlap (Figure 2.8).

In the region around zero overlap, the model lacks smoothness, which means the analytical description may be somewhat inaccurate, even when broken down into many elementary contributions. This underscores the importance of conducting FEM (Finite Element Method) modeling in this area. Accurate FEM modeling is crucial for understanding the device's operation and how the fringing fields might affect the force balance within the system.

2.2.2 FEM analysis

To assess the accuracy of our analytical analysis, we conducted Finite Element Method (FEM) modeling using COMSOL Multiphysics software. The same set of parameters as in Table 2.2 was used to calculate the capacitance of the comb-drive structure. The movable electrode and the substrate were connected to ground, while the fixed electrode was subjected to a voltage V. The initial overlap between the combs was varied from -10 times the finger width (denoted as d) to $10d$, with steps of $1d$. Additionally, we employed smaller steps of $0.2d$ within the range of $-5d$ to $3d$. This allowed us to explore the influence of overlap with a fine analysis in the near-zero-overlap regime. The capacitance value between the grounded parts and the polarized electrode was then extracted (circles in Figure 2.10a). From these discrete FEM data, a continuous function that describes how capacitance changes with overlap u was then established (red line in Figure 2.10).



(a) **(b)**

Figure 2.10: Variation of the (a) capacitance and (b) force (derived from the fitted capacitance curve) with respect to the overlap between the comb-drive fingers. Analytical and FEM model are compared in (a).

This involved employing a cubic Hermite spline interpolator to effectively model the discrete FEM data presented in in Figure 2.10a [39]. The overlap range was separated into four distinct regions, with each region i individually subjected to fitting via a third-degree polynomial of a form:

$$C_i(u) = a_i u^3 + b_i u^2 + c_i u + d_i \tag{2.9}$$

This method was employed to guarantee the continuity of both the fitting function and its derivative at the boundaries of the regions.

As depicted in Fig. 2.10a, our analytical model is in a fairly good agreement with the FEM model. Nevertheless, the analytical description of the region of interest (near-zero-overlap) is not sufficiently accurate, with relative error up to 17%. This emphasizes the difficulty of modeling fringing fields, particularly when complex geometries are involved. Moreover, the derivative of this analytical function is not continuous, which prevents accurate description of the force established within the comb. We have therefore proceeded in the behavior analysis with the capacitance description of the device based on FEM simulations. FEM data considers the contribution of the fringing electric fields more precisely and completely and offers a more accurate representation.

Furthermore, the fitting function facilitated the calculation of the capacitance derivative, allowing the deduction of the attractive electrostatic force $F_{\mathrm{el}}(u) = \frac{1}{2}\frac{dC(u)}{du}V^2$ acting between the combs. The results in Figure 2.10b indicate that the force, directly proportional to the capacitive gradient, remains at nearly constant values for $u < -2.5$ µm and $u > 1.5$ µm, with a notable exception in an intermediate region where it undergoes rapid increase. We term this region, where the overlap u ranges from -2.5 to 1.5, the *gray zone* (Figure 2.10b). Within this zone, a significant force persists for negative overlaps due to the long-range influence of fringing electric fields. The structure also encounters the maximum force gradient within the gray zone (inset of Figure 2.10b). The effects of this force gradient, intricately linked to the second derivative of capacitance, will be discussed later.

2.3 Study of the complementary input stage

Figure 2.11 shows the system-level schematic of the elementary component of the complementary adiabatic capacitive logic (CACL) approach. The working principle is relying on two variable electromechanical capacitors C_A and $C_{\bar{A}}$ sharing the same grounded electrode.

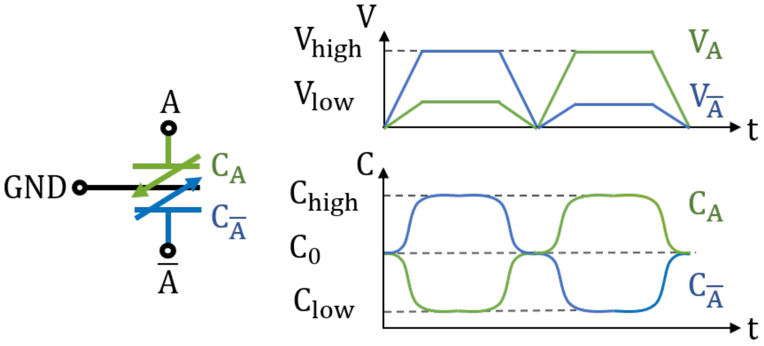


Figure 2.11: Schematic and characteristics of an elementary component based on two complementary variable capacitors (VC) C_A – between A and ground and $C_{\bar{A}}$ between $\bar{A}$ and ground.

Complementary voltages V_A and $V_{\bar{A}}$ are applied simultaneously to two independent gate terminals A and $\bar{A}$, respectively. If V_A is set to high and $V_{\bar{A}}$ to low, the capacitor value C_A will increase whereas the one corresponding to $C_{\bar{A}}$ will decrease, as shown in Figure 2.11. The variation is the opposite if the voltage $V_{\bar{A}}$ is set to high and V_A to low. This control of the direction of displacement of the comb, and therefore the capacitance within the comb drives, allows us to interpret the position of the movable electrode as a logic state. As the logic state representation depends on the displacement of the movable comb and the energy dissipation within the gate depends on the supplied voltage and the amount of invested charges, it is crucial to identify suspensions that are as soft as possible, allowing large deflections at low actuation voltage. Furthermore, it is essential to define the most optimal operating conditions, allowing the largest difference in the reached capacitance values at the end of the motion.

2.3.1 Stationary configuration

When applying the two complementary signals, the attractive electrostatic force (which is proportional to the square of the applied voltage) acting within the comb-drive subjected to lower signal V_{L} should ideally be negligible compared to the one acting within the actuator subjected to V_{H}. The largest capacitance contribution within the comb-drives comes from the plate capacitance between the overlapping fingers (Eq. 2.8) and the capacitance gradient (and therefore electrostatic force) increases rapidly from near zero to a constant value when the finger overlap changes from negative to positive one. We named this range of non-linear force the *gray zone* (Figure 2.10b).
In the resting state configuration of complementary architecture where the overlap of the fingers u_0 in both comb pairs is within the gray zone, a small displacement x in either direction would significantly increase the electrostatic force within the comb pair in which the total overlap u increased, whereas the force in the complementary comb would decrease. Figure 2.12 shows schematically three different situations for the position of the movable electrodes, depending on the the combination of input signals and direction of movement.

By taking a convention that the displacement in the negative x direction (increase of C_A and decrease of $C_{\bar{A}}$) at the input stage corresponds to logic state 1 and the one in positive x direction to logic state 0 (increase of $C_{\bar{A}}$ and decrease of C_A), we can summarize the combination of input signals and the corresponding logic states in the Table 2.5.

Logic state 1	Relaxed position	Logic state 0
$V_A = V_{\mathrm{H}}$	$V_A = 0$	$V_A = V_{\mathrm{L}}$
$V_{\bar{A}} = V_{\mathrm{L}}$	$V_{\bar{A}} = 0$	$V_{\bar{A}} = V_{\mathrm{H}}$
$x < 0$	$x = 0$	$x > 0$

Table 2.5: Applied signals and the corresponding displacement for the logic states 1 and 0

To identify the most optimal resting state configuration, we looked into the amount of invested charge per µm of induced displacement, with respect to the initial overlap of the

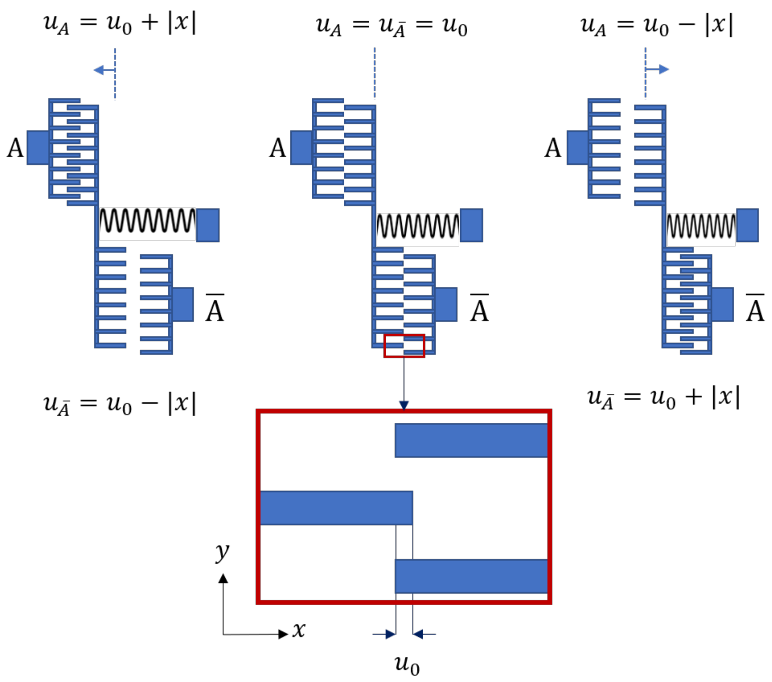


Figure 2.12: Applied signals and the corresponding displacement for the logic states 1 and 0 and the transition (resting) stage between two states.

fingers u_0 in the two complementary comb pairs. As the charge on the capacitor is given by $q = CV$, we can obtain the displacement in µm per amount of invested charges as:

$$\frac{x}{C(x+u_0)V_{\mathrm{H}} + C(-x+u_0)V_{\mathrm{L}}} \tag{2.10}$$

Where x is the displacement of the movable electrodes, u_0 is the initial overlap of the comb fingers in the absence of the external signals, and $C(x+u_0)$ and $C(-x+u_0)$ are the capacitances in the comb pairs A and $\bar{A}$ at the end of the movement.

Figure 2.13 shows the induced displacement of the movable part per amount of invested charges, depending on the value of the initial overlap u_0. The plot is obtained with a typical set of voltages $V_{\mathrm{H}} = 12$ V and $V_{\mathrm{L}} = 9$ V. Initial overlap is normalized to the length of the fingers l. Operation in the range close to zero-initial overlap can result in a four times larger displacement for the same amount of invested charges than the usual operation with the coverage of 50% of the finger length. This is beneficial for the present application as it allows reduction of the energy invested in the logic operation while maintaining the mechanical force required for coding of the logic state in the MEMS displacement and consequently ensuring logic differentiation.

2.3.2 Voltage induced displacement

Modeling of the capacitance and consecutively the force allowed us to predict the displacement magnitude for a given set of applied input voltages. In this approach, the initial

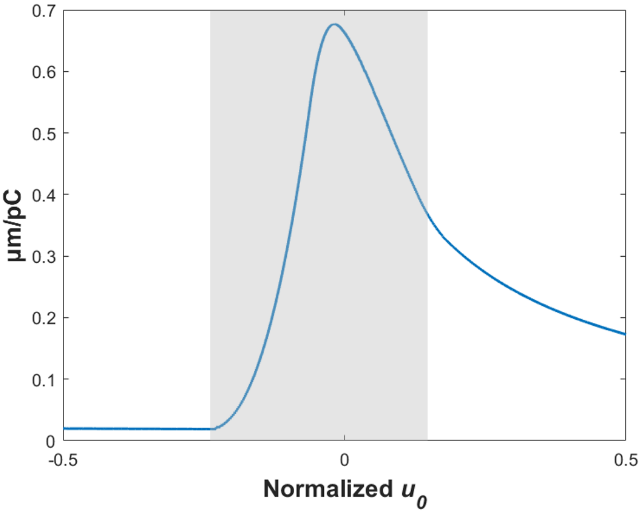


Figure 2.13: Induced displacement per invested amount of charges for different initial coverage of the combs. Finger overlap is normalized with the length of the fingers l. The gray rectangle indicates the extension of the gray zone.

overlap of $u_0 = 0$ is assumed. The potential energy at each position within the range of motion of the movable electrodes ($-l < x < l$, with l being the length of comb fingers) is calculated with the following equation:

$$\begin{aligned} E_p &= \frac{kx^2}{2} - \frac{C_A V_A^2}{2} - \frac{C_{\bar{A}} V_{\bar{A}}^2}{2} \\ &= \frac{kx^2}{2} - \frac{C(x) V_A^2}{2} - \frac{C(-x) V_{\bar{A}}^2}{2} \end{aligned} \tag{2.11}$$

Where $C(x)$ and $C(-x)$ are mutual capacitances corresponding to the displacement x in the comb-pairs A and $\bar{A}$ caused by applied voltages V_A and $V_{\bar{A}}$, respectively. The first term represents the potential energy of the mechanical spring, where k is the spring constant. The next two terms account for the potential energies of the comb structures A and $\bar{A}$. The stable equilibrium position, which corresponds to the minimum point on the potential energy curve, is identified from the data. This minimum point is then used as the displacement value of the movable electrode.

As an example, Figure 2.14 shows the potential energy of the MEMS mobile part within the displacement range between -5 μm and 5 μm for the set of input voltages $V_A = 4$ V and $V_{\bar{A}} = 24$ V and with the spring constant of $k = 1.5\ \mathrm{N\,m^{-1}}$. The values of $C(x)$ and $C(-x)$ are extracted for each value of displacement x from the FEM model described in the previous section.

When the signal on $\bar{A}$ is set to *high* and the signal on A is set to *low*, the electrostatic force within the comb pair $\bar{A}$ becomes stronger than the force within A. This imbalance creates a net electrostatic force in the positive x direction, which we previously defined as the logic state 0. In this specific scenario, the stable position is achieved at a displacement

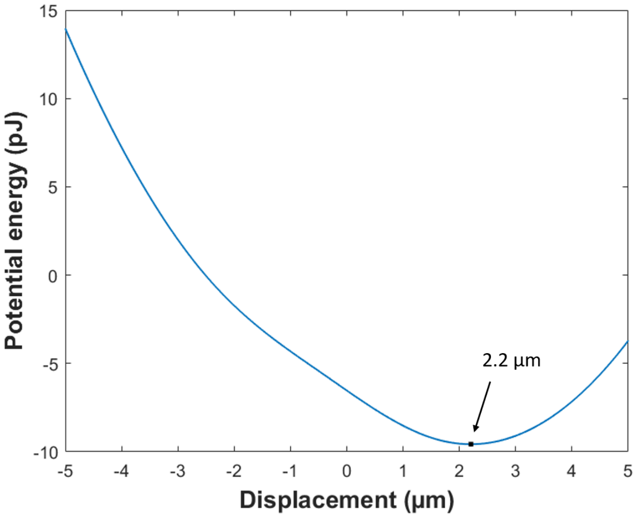


Figure 2.14: Potential energy of the MEMS moveable part for a set of input voltages $V_A = 4$ V and $V_{\bar{A}} = 24$ V and with the spring constant of $k = 1.5\ \mathrm{N\,m^{-1}}$. Minimum values of the curve corresponds to the stable equilibrium position of the movable MEMS part, relative to the resting position (when applied voltages and therefore displacement equal zero).

of $x = 2.2$ µm.

With the same approach we can visualize the position of the movable electrode during the state switching. In the adiabatic approach, the input signals are slowly introduced (the signals have trapezoidal shape). In Figure 2.15, different energy curves represent the potential energy of the moveable part at different time instants. The position **a** ($x_a = -2.2$ µm) is reached durint $T < t < 2T$ when V_A is set at V_H and $V_{\bar{A}}$ is set at V_L. The displacement is therefore negative and the encoded logic state is 1. When the signals are slowly reduced towards zero, during $2T < t < 3T$, the movable part passes through the position **b** at the moment when $V_A = V_\mathrm{H}/2$ and $V_{\bar{A}} = V_\mathrm{L}/2$. The displacement at the position **b** is $x_b = -0.45$ µm. During $3T < t < 4T$, in the absence of input signals, the potential energy of the system is the one of the mechanical spring and its minimum is at zero (position **c**). When the input signals are inverted, that is, V_A is raised towards V_L and $V_{\bar{A}}$ is towards V_H, the displacement is in the positive x direction. During $4T < t < 5T$ the movable electrodes pass through the position **d** ($x_d = 0.45$ µm). When V_A and $V_{\bar{A}}$ reach V_L and V_H, respectively, the displacement is at $x_e = 2.2$ µm during $5T < t < 6T$.

The signal values of V_A and $V_{\bar{A}}$ at various positions are shown in Table 2.6. Here, V_H and V_L represent the high and low signal voltages, which are set to 24 V and 4 V, respectively, for the simulation.

Transitioning between the two states involves gradually reducing the applied signals to zero. In the quasi-static case, the input signals are varied slowly compared to the natural frequencies of the device to ensure adiabatic operation. This causes the displacement of the movable combs to follow the input without significant lag and decrease toward the resting position, corresponding to the minimum potential energy of the mechanical spring.

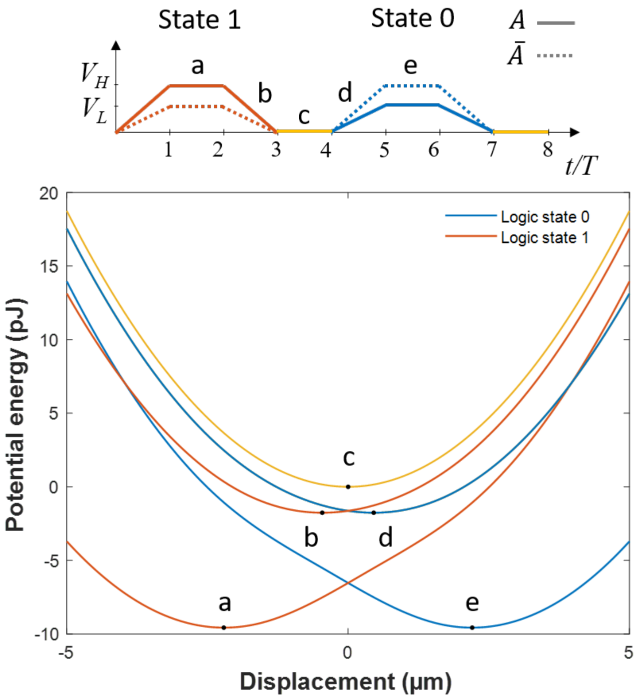


Figure 2.15: Potential energy of the MEMS moveable part for a given set of voltages applied to the comb-pairs A and $\bar{A}$. Minimum values of the curves correspond to the stable equilibrium positions of the movable MEMS part, relative to the resting position (when applied voltages equal zero).

	a	b	c	d	e
V_A	V_H	$V_\mathrm{H}/2$	0	$V_\mathrm{L}/2$	V_L
$V_{\bar{A}}$	V_L	$V_\mathrm{L}/2$	0	$V_\mathrm{H}/2$	V_H
x(μm)	-2.2	-0.45	0	0.45	2.2

Table 2.6: Values of the voltages V_A and $V_{\bar{A}}$ in different phases of the transitioning between the two logic states. V_H and V_L are set to 24 V and 4 V, respectively, while the spring constant is set at $k = 1.5\ \mathrm{N\,m^{-1}}$.

We can now examine the energy invested in state encoding, which can be described by Eq. 2.12:

$$E_{in} = \frac{kx^2}{2} + \frac{C(x)V_A^2}{2} + \frac{C(-x)V_{\bar{A}}^2}{2} \tag{2.12}$$

Figure 2.16 shows the invested energy curves derived for the whole displacement range. The same state-transition positions indicated in Figure 2.15 and Table 2.6 are outlined. The green line is the approximation of the change of the invested energy during adiabatic state switching. It follows a smooth trajectory, thereby minimizing energy dissipation. On the other hand, in a non-adiabatic (abrupt) state switching (approximated with black lines) a dissipation of a few tens of pJ during a single operation can be observed.

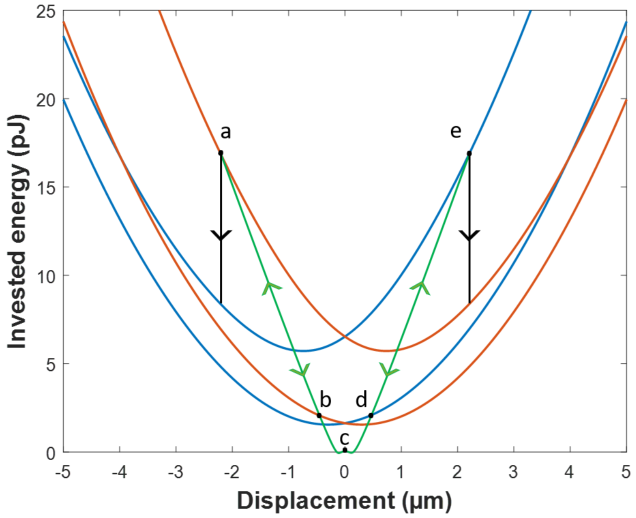


Figure 2.16: Energy invested in the encoding of the two logic states: 1 (red) and 0 (blue). Quasi-static moving between the logic states ensures non-hysteretic energy exchange between MEMS and the power supply (green curve). Abrupt switching involves inevitable energy losses (black curves).

Considering that the most energetically favorable resting state configuration is where the overlap of the fingers is nearly zero (as illustrated in Figure 2.13), we calculated the displacement of the movable (grounded) electrode when voltage is applied to the fixed electrode. We examined three different initial overlap configurations: u_0 equal to $-2d$, zero, or $2d$, with d representing the width of the fingers. Figure 2.17 displays the expected displacements for each of these configurations when voltages ranging from zero to 25 V are applied.

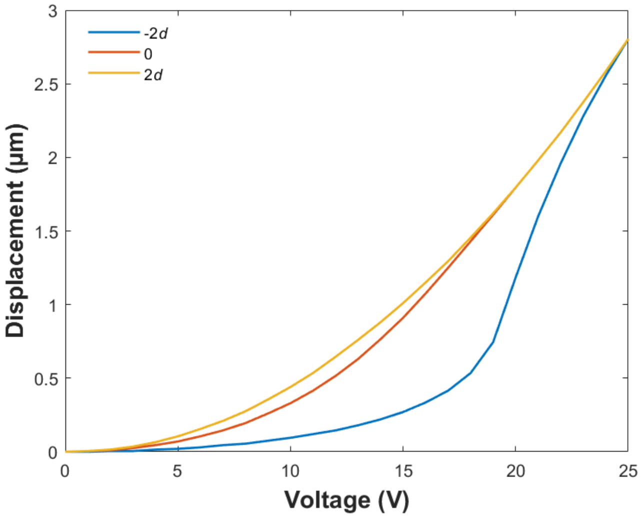


Figure 2.17: Simulated displacements with respect to the applied voltage for three different initial overlap situations: $-2d$, 0 and $2d$.

2.3.3 Sensitivity to the variations in geometry

The capacitance versus overlap model was developed using FEM analysis, based on the geometrical parameters and material properties listed in Table 2.2. This model and the resulting simulations formed the foundation for designing the individual components, test devices, and logic gates to be discussed in the next chapter. Considering that various steps in the micro-fabrication process (photolithography, etching) are influenced by environmental conditions such as temperature and humidity, and acknowledging the inherent variability and potential for human error, it is reasonable to anticipate that the fabricated devices may deviate from the original design.

For this reason, we investigated how dimensional changes separately affect the properties of the logic gate, focusing on its capacitance and spring constant. First, we examined the uniform change in the dimensions of comb-fingers and its impact on the capacitance within the comb-drive. Next, we analyzed how variations in the initial overlap, achieved by changing the finger length, influence the voltage-induced displacement. Lastly, we explored the sensitivity of the spring constant to changes in width and how this also affects the voltage-induced displacement.

We considered three example configurations with initial overlaps of $u_0 = -2d$, zero, and $2d$. Figure 2.18 illustrates the configuration with $u_0 = 0$, where the dashed lines indicate expected size variations. The figure shows that these size variations impact the finger width d, the gap g between them, and the overlap of the fingers u_0.

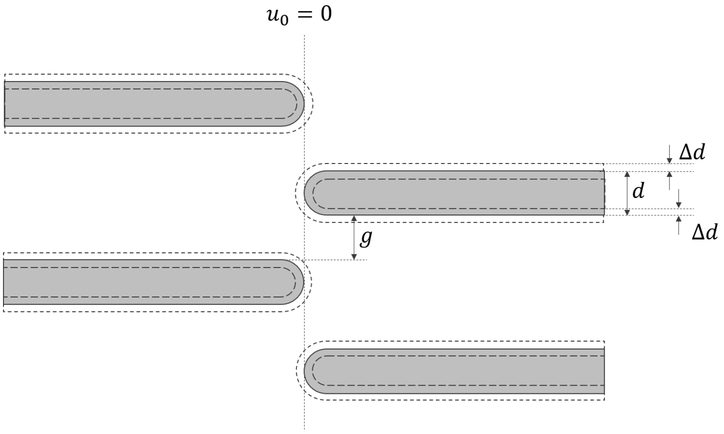


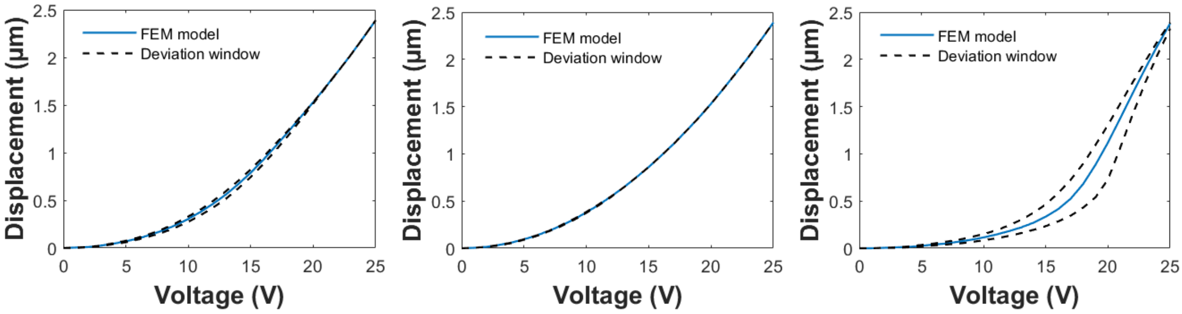
Figure 2.18: Variation of the size of the fingers in the initial configuration with zero overlap.

The majority of the constant capacitance contribution across the entire overlap region is due to the plate capacitance between the bottom of the fixed electrode and the substrate. The contribution from the comb fingers is $\varepsilon_0 N \frac{dl}{h}$, where l is the length of the fingers and h is their thickness. A variation in the width and length of the fingers by $2\Delta d$ and $\pm\Delta d$, respectively, would result in an offset in the capacitance-versus-overlap curve. Assuming that the dimension change $\Delta d << d, l$, the shift in capacitance can be expressed as:

$$\Delta C_{\text{fix}} = \varepsilon_0 N \frac{d + 2l}{h} \Delta d \tag{2.13}$$

In the overlapping region the main contribution to the capacitance value is given by the Eq. 2.8. This variable capacitance is inversely proportional to the width of the fingers and increases linearly with their overlap u. The slope of the curve is then given by $2N\varepsilon_0\frac{h}{g}$, which for the FEM model developed earlier (Figure 2.10a) equals 11.3 $\mathrm{fF\,\mu m^{-1}}$.
A change of the width of the fingers of $2\Delta d$ would result in the change of the slope by a factor of $\frac{g}{g+2\Delta d}$.

Variations in the length of the fingers (l) lead to changes in the resting state overlap (u_0) within the comb structures and alter the overall balance of electrostatic and mechanical forces when a voltage is applied. The finger overlap then becomes $u = u_0 + 2\Delta d + x$, where x is the displacement of the movable electrode. Figure 2.19 displays the simulated voltage-induced displacement curves for three initial overlap configurations, based on the FEM model with a spring constant of $k = 1.5\ \mathrm{N\,m^{-1}}$ (blue curves). The figure also shows the deviation range when the finger length varies by 100 nm (dashed lines).



(a) $u_0 = 0$ **(b)** $u_0 = 2d$ **(c)** $u_0 = -2d$

Figure 2.19: Simulated comb-displacement induced by applying a DC voltage on the fixed electrode for three different comb-drive configurations: initial comb-overlap of (a) 0, (b) $2d$, and (c) -$2d$. The dashed lines represent the extreme variations of the geometrical parameters that can occur during device fabrication and they correspond to cases where finger length l is varied by $\Delta d = 100$ nm consequently adding an offset to the overlap of ±200 nm.

In the zero overlap configuration (Figure 2.19a), displacement is slightly affected for voltage values below 20 V. Above this voltage, the displacement exceeds 1.5 µm, causing the fingers to move out of the gray zone where the electrostatic force becomes constant (see Figure 2.10b). Below 20 V, the fingers remain in the gray zone where the electrostatic force varies significantly with finger overlap, explaining the sensitivity to the overlap offset of $2\Delta d$.

As shown in Figure 2.19b, for the configuration with an initial overlap of $u_0 = 2d$ (1 µm), small changes in the overlap do not significantly affect the induced displacement. Since the finger overlap remains substantial and the fingers stay engaged, the initial electrostatic force is already on the edge of the gray zone and quickly becomes constant.

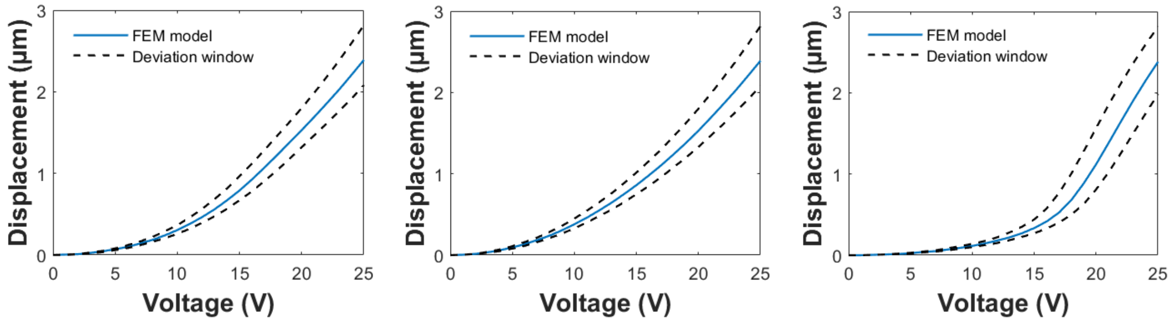
For a negative initial overlap of $u_0 = -2d$ (-1 µm), operation throughout the entire voltage range occurs within the gray zone. Due to the non-linearity and significant force variation in this region, the displacement is highly sensitive to the overlap offset of $2\Delta d$. This sensitivity is greatest around 20 V, where the displacement can vary by up to 0.7 µm depending on the offset. Around 25 V the displacement approaches the edge of the gray zone which is reflected in smaller sensitivity of the displacement.

Spring constant of a clamped-clamped beam is given by:

$$k = \frac{16Ehw^3}{L^3} \tag{2.14}$$

In this equation, E represents the Young's modulus of the material, h is the beam's thickness, w is its width, and L is its length. The thickness (h) and length (L) of the beam are assumed to remain unaffected during microfabrication since the beam is fixed. However, the width (w) may vary slightly due to the environmental sensitivity of the photolithography and etching processes. Consequently, a 5% change in the beam width (w) results in a 15% change in the spring constant (k).

Figure 2.20 presents the simulated voltage-induced displacement curves for three initial overlap configurations, as determined by the FEM model with a spring constant of $k = 1.5\ \mathrm{N\,m^{-1}}$ (blue curves). Additionally, the figure illustrates the deviation range when the spring constant varies by ±15% (dashed lines).



(a) $u_0 = 0$ **(b)** $u_0 = 2d$ **(c)** $u_0 = -2d$

Figure 2.20: Simulated comb-displacement induced by applying a DC voltage on the fixed electrode for three different comb-drive configurations: initial comb-overlap of (a) 0, (b) $2d$, and (c) -$2d$. The dashed lines represent the extreme variations of the geometrical parameters that can occur during device fabrication and they correspond to cases where spring width w is varied by 5%, which by design equals $\Delta w = 100$ nm and consequently changes the spring constant by 15%.

The position of the movable electrode (its displacement) is determined by the balance between the mechanical force $-kx$ of the spring and the electrostatic force $\frac{1}{2}V^2\frac{dC}{dx}$ within the comb structures. For all three configurations, the displacement increases when the spring constant k is reduced and decreases when k is increased.

As discussed above, geometric variations impact the force balance within the device, affecting the achievable displacement and state encoding. Changes in capacitance, whether an increase or decrease, can be compensated by adjusting the voltage signals accordingly. By assuming uniform geometric changes across the entire device, the compensations can be incorporated at the design stage before fabrication, within the limits of resolution. This topic will be explored further in the next chapter, where we will discuss the initial microfabrication tests.

2.4 CACL inverter gate

Building on the elementary component from Figure 2.11, with variable capacitors being implemented with comb drive structures, the inverter gate can be realized as shown in Figure 2.21. Note that input and output variable capacitors share the same movable grounded electrode as a mechanical link.

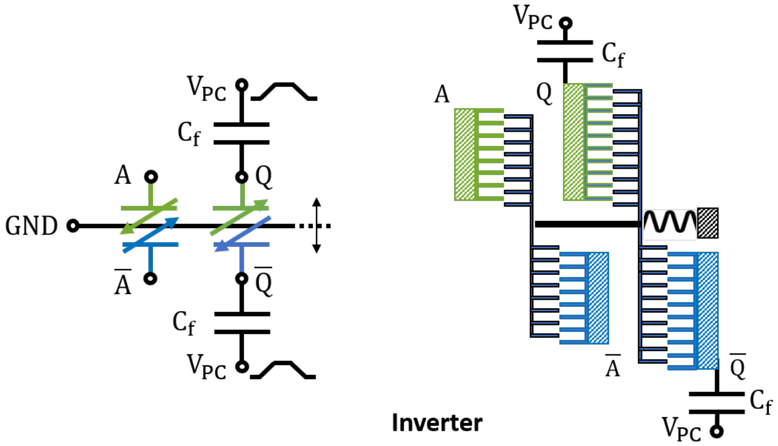


Figure 2.21: Simplified electromechanical model of an ACL inverter gate and the MEMS implementation.

Each comb-drive structure consists of two complementary electrode pairs (A and $\bar{A}$ at the input, Q and $\bar{Q}$ at the output) allowed to move along the x-axis with a stiffness k. The active electrodes are connected to the input signals and the passive ones to the ground (avoiding pull-in with the grounded substrate). They are electrostatically coupled by (N_A, N_Q) interdigitated fingers separated by an air gap g. The values of physical and geometrical features of the proposed implementations are given in Table 2.7.

The input signals A and $\bar{A}$ induce electrostatic forces that further cause shuttle displacement, establishing the capacitor values C_A and $C_{\bar{A}}$. As the movable input electrodes are mechanically connected to the movable output electrodes, the complementary output capacitors C_Q and $C_{\bar{Q}}$ are established at the same time. C_f are fixed capacitances forming capacitive bridges with C_Q and $C_{\bar{Q}}$. The power clock signal V_{PC}, a variable power supply, is applied over the bridge, yielding the complementary output electrical signals Q and $\bar{Q}$

of the gate. The timing sequence is similar to the one of adiabatic logic where the power supply V_{PC} is a trapezoidal voltage divided in four phases [10].

Parameter	Description	Value	Unit
E	Young's modulus of silicon	170	GPa
ε_0	Vacuum permittivity	$8.854 \cdot 10^{-12}$	$\mathrm{F\,m^{-1}}$
ε_r	Relative permittivity of silicon oxide	4.2	
h	Thickness of the silicon layer	5	µm
h_{box}	Thickness of the oxide layer	2	µm
l	Length of the fingers	10	µm
d	Finger width	0.5	µm
g	Gap between fingers	0.5	µm
k	Spring constant	1.5	$\mathrm{N\,m^{-1}}$
u_0	Overlap of the fingers in the resting state	0	µm
N_A	Number of fingers in the input comb	60	
N_Q	Number of fingers in the output comb	480	
α	Ratio between the number of output and input combs	8	

Table 2.7: Physical and geometric parameters used in simulations.

With the parameters from Table 2.7 and previously developed capacitance-versus-overlap model, we are able to simulate the state encoding, the corresponding displacement x, established output voltages V_Q and $V_{\bar{Q}}$, as well as the invested energy E_{in}, using MATLAB.

Analogously to the Eq. 2.11 the potential energy curves for the full inverter gate are obtained with:

$$\begin{aligned} E_p &= \frac{kx^2}{2} - \frac{C_A V_A^2}{2} - \frac{C_{\bar{A}} V_{\bar{A}}^2}{2} - \frac{C_Q V_Q^2}{2} - \frac{C_{\bar{Q}} V_{\bar{Q}}^2}{2} \\ &= \frac{kx^2}{2} - \frac{C(x) V_A^2}{2} - \frac{C(-x) V_{\bar{A}}^2}{2} - \frac{\alpha C(x) V_Q^2}{2} - \frac{\alpha C(-x) V_{\bar{Q}}^2}{2} \end{aligned} \tag{2.15}$$

The additional two terms (with respect to the Eq. 2.11) account for the potential energies of the output comb structures Q and $\bar{Q}$. The displacement magnitude, which corresponds to the minimum point on the potential energy curve, is extracted from this data. The values of V_Q and $V_{\bar{Q}}$ are obtained through the capacitive divider as:

$$\begin{aligned} V_Q &= V_{PC} \frac{C_\text{f}}{C_\text{f} + C_Q} \\ V_{\bar{Q}} &= V_{PC} \frac{C_\text{f}}{C_\text{f} + C_{\bar{Q}}} \end{aligned} \tag{2.16}$$

Therefore, the increase of capacitance C_Q causes reduction of V_Q. The same stands for $C_{\bar{Q}}$ and $V_{\bar{Q}}$. This demonstrates the fundamental behavior of an inverter gate. The invested energy of the full inverter is analogously to Eq. 2.12 given by:

$$E_{in} = \frac{kx^2}{2} + \frac{C(x)V_A^2}{2} + \frac{C(-x)V_{\bar{A}}^2}{2} + \frac{\alpha C(x)V_Q^2}{2} + \frac{\alpha C(-x)V_{\bar{Q}}^2}{2} \tag{2.17}$$

Figure 2.22 depicts the simulated behavior of the MEMS inverter and illustrates propagation and inversion of both logic states from the input to the output stage of the logic gate. The first graph shows the signals A and $\bar{A}$ applied to the input comb-pairs. The second graph represents the power clock signal applied to the output comb-pairs via capacitive bridge with a time delay T with respect to the input signals. The third graph shows the induced displacement of the moveable MEMS part. The fourth one depicts the generated signals on the output comb-pairs Q and $\bar{Q}$, demonstrating the inverter behavior. The last graph shows the energy invested by the PC in the operation.

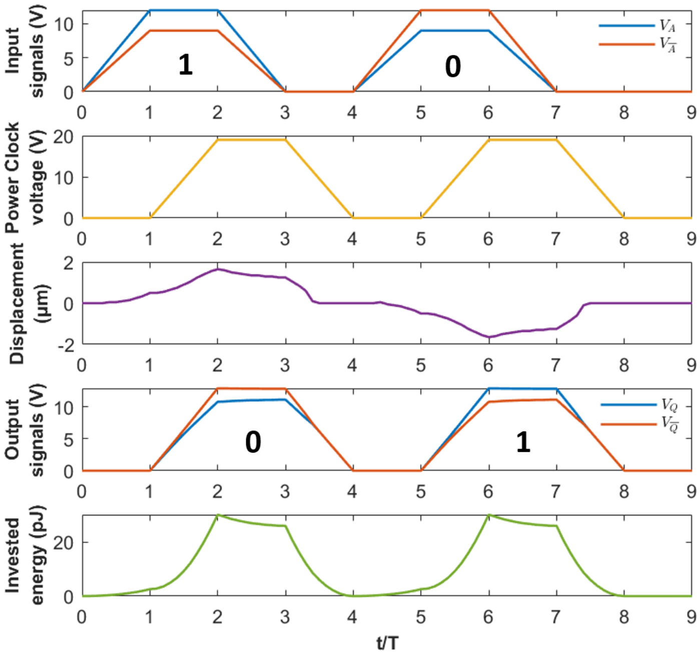


Figure 2.22: Dynamic behavior of the inverter MEMS gate: Signals applied to the input comb-pairs (states 1/0); PC signal applied to the output comb-pairs (via capacitive bridge) with a time delay T; Induced displacement of the movable MEMS part; Generated signals on the output comb-pairs (states 0/1); Energy invested by the PC in the operation.

During **phase 1** ($0 < t < T$), the complementary input voltages (V_H and V_L) cause an imbalance between the forces acting on the electrodes within comb-pairs A and $\bar{A}$. This imbalance initiates motion in the movable combs towards the electrode experiencing greater force (in this case, A), further inducing an initial imbalance within the output comb-pairs, representing pre-actuation.

In **phase 2** ($T < t < 2T$), the power clock signal V_{PC} is progressively applied to the output stage through a capacitive bridge formed by fixed capacitances C_f. This application establishes the output voltages (V_Q, $V_{\bar{Q}}$). With appropriate design parameters, this additional voltage amplifies the initial movement initiated by the inputs.

Phase 3 ($2T < t < 3T$) involves lowering the signals A and $\bar{A}$ to the ground. As the number of fingers in the input combs is significantly smaller than the one of the output combs, the logic state remains encoded in the position through the force generated by the output comb-pair and the power clock. During this phase, the established voltages V_Q and $V_{\bar{Q}}$ serve as the input voltages for evaluating the next logic gate. The established voltage levels are compatible with the input levels, meaning that this gate could cause a preactuation of a subsequent gate.

In **phase 4** ($3T < t < 4T$), the V_{PC} signal is reduced to 0, causing the movable parts to return to their initial position. By utilizing a trapezoidal waveform for the signals (inputs and PC), abrupt transitions are eliminated. This allows for optimal charging of the capacitors and enables energy recovery by the power clock, resulting in very low dissipation and even adiabatic operation.

The relatively high invested energy ($\approx$ 25 pJ) can be reduced by down-scaling the device (Table 2.1), as both the capacitances and required driving voltages would downscale as well. Moreover, in the adiabatic operation, if the appropriate power source is used, the energy should be fully recoverable [10]. Voltages established at the output stages correspond to the ones applied at the input, demonstrating the capability of cascadability and actuation of a subsequent gate.

2.5 Conclusion

We have introduced a new paradigm of logic gates using a flexible structure and variable MEMS capacitors arranged in a complementary setup. Combdrive actuators were chosen as strong candidates for proof-of-concept devices. Our study included detailed capacitance modeling of combdrive actuators using both analytical methods and Finite Element Method (FEM) simulations, particularly focusing on the unique scenario where the overlap between the fingers is minimal or even negative. This scenario, with near-zero initial overlap, is the most energy-efficient operating condition. In this condition, fringing electric fields cause a non-linear change in capacitance with displacement, leading to significant variations in electrostatic force. The FEM analysis provided a precise model of capacitance versus displacement, essential for accurate system-level modeling and design. Based on this model, we analyzed the energetic profile of a basic variable capacitor, identifying the optimal operating conditions and its sensitivity to variation of geometrical parameters. Using this component, we developed an inverter logic gate and simulated its ability to invert input logic states. The energy used during gate operation could be fully recovered by a reversible power supply and can be reduced by lowering the overall size of the device. Additionally, we demonstrated that the inverter gate can produce output voltages capable of driving subsequent gates.

3

Design and Fabrication

This chapter covers the various stages involved in the design and fabrication of the MEMS logic structures, based on the differential capacitive design introduced in the previous chapter. Starting with the concept of the inverter logic gate based on variable capacitors, this chapter addresses the design process for individual components of this device. Additionally, it outlines the test structures employed to investigate the performance of each element within the inverter gate, and proposes different possibilities for implementation of a NAND gate. The chapter further delves into the fabrication process and its optimization, providing a detailed explanation of each step. Subsequently, the fabricated structures are presented and discussed.

3.1 Architecture of the inverter gate

As explained in the previous chapter, the architecture of the inverter gate relies on a four-terminal (A, $\bar{A}$, V_{PC}, GND) MEMS device forming mechanically-variable capacitors. The terminals of the device are electrically isolated. The device geometry has to allow transfer of the logic state to another device within a cascade of several gates. Ultimately, a complex logical circuit where multiple inputs are being driven by a single output should be feasible.

The schematic of the device geometry is shown in Figure 3.1. This differential architecture consists of two pairs of comb-drive actuators - input and output pair. Each pair consists of a fixed (active) and a movable (passive) electrode while the movable electrodes are connected by a mechanical spring of a stiffness k. Active and passive electrodes at the input stage are connected to the supply voltages and to the ground, respectively. They have thickness h and are electrostatically coupled by N interdigitated fingers separated by an air gap g. The architecture being differential, the input combs are driven by complementary voltages V_A and $V_{\bar{A}}$, defining a dual-rail logic. They actuate the combs at the output (Q, $\bar{Q}$), varying their capacitance value and establishing the output voltages V_Q and $V_{\bar{Q}}$.

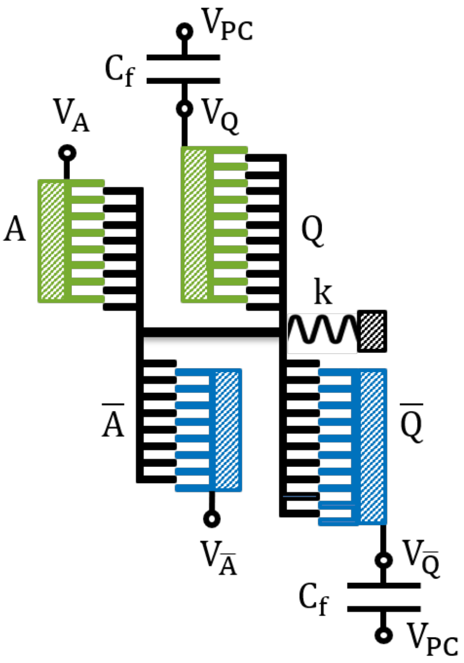


Figure 3.1: Schematic of a MEMS inverter gate where the active (fixed) electrodes are shown in color and the movable ones are depicted in black.

The mask design was performed in CleWin5 software, whereby the components were defined in a parametric way, allowing quick change of the dimensions, such as number of fingers within the combs, their width, length, spacing, as well as the size of the suspensions and fixed capacitors. MATLAB was used as a scripting language.

3.1.1 Electrical connections

The electrical connections between the contact pads and the electrodes (combs), as well as between consecutive devices contribute to parasitic capacitance, thus reducing the difference between high and low logic levels (state differentiation), and should therefore be designed carefully, so that their contributions are minimized. As capacitance depends on the surface of the conducting wires and their thickness is constant as they are embedded in the device layer ($h = 5$ µm), the parameters that can be optimized are the width and the length of the wires. The longest connection on our mask is the one between the input combs and contact pads. Due to the size of the other sub-parts of the gate (that measures about 540×620 µm^2), which will be addressed further in this chapter, its length has to be at least 200 µm.

The electrical connections can be viewed as clamped-clamped beams of length L, width W and thickness H (Figure 3.2). The spring constant (in the direction of the applied force $\overrightarrow{F}$) of a clamped-clamped beam can be calculated as:

$$k_{\mathrm{z}} = \frac{16EWH^3}{L^3} \tag{3.1}$$

Where E is the Young's modulus of silicon, W is the width of the electrical connection, H is its thickness and L is its length.

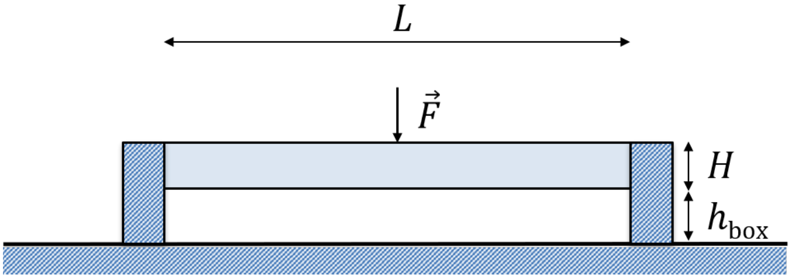


Figure 3.2: Design of the electrical connections.

Furthermore, as significant voltages are applied across electrical connections, their geometry should be such that their pull-in voltage is far above the ones that they are subjected to. Pull-in voltage of an electrically conducting wire is given by:

$$V_{\text{pull-in}} = \sqrt{\frac{8kh_{\mathrm{box}}^3}{27\varepsilon_0 LW}} \tag{3.2}$$

With h_{box} being the thickness of the buried oxide layer and ε_0 the permittivity of air.

By taking the length of the wire to be $L = 200$ µm and its width $W = 2$ µm (the same as the width of the supporting beams in the combs) we can obtain its spring constant of $k = 85\ \mathrm{N\,m^{-1}}$ and the pull-in voltage of 240 V, which is an order of magnitude above the voltages that out device is subjected to. Nevertheless, additional anchors have been added to support the electrical connections at half of their length.

3.1.2 Design of the spring

As explained in the previous chapter, the targeted spring constant of the suspension is $k = 1.5\ \mathrm{N\,m^{-1}}$. This low value is needed in order to reduce the voltage value required for the actuation and therefore to reduce the energy invested in the device displacement. With the suspension anchored between the input and output stage, the shuttle of the device can be viewed as a clamped-free beam (Figure 3.3a). Any small rotation of the shuttle would break the symmetry within the combs and cause pull-in and sticking of the fingers, ultimately damaging the device. By adding instead two suspensions in series and anchoring them on the sides of the output stage, the spring constant of the shuttle can be increased by factor of 48 ($\approx 300\ \mathrm{N\,m^{-1}}$), therefore significantly improving the stability of the whole device (Figure 3.3b). The two suspensions should consequently have spring constants of $0.75\ \mathrm{N\,m^{-1}}$ each. Furthermore, as the intended movement is in the $x-$direction, the spring constants along y and z axes should be significantly higher, preventing movements in these directions.

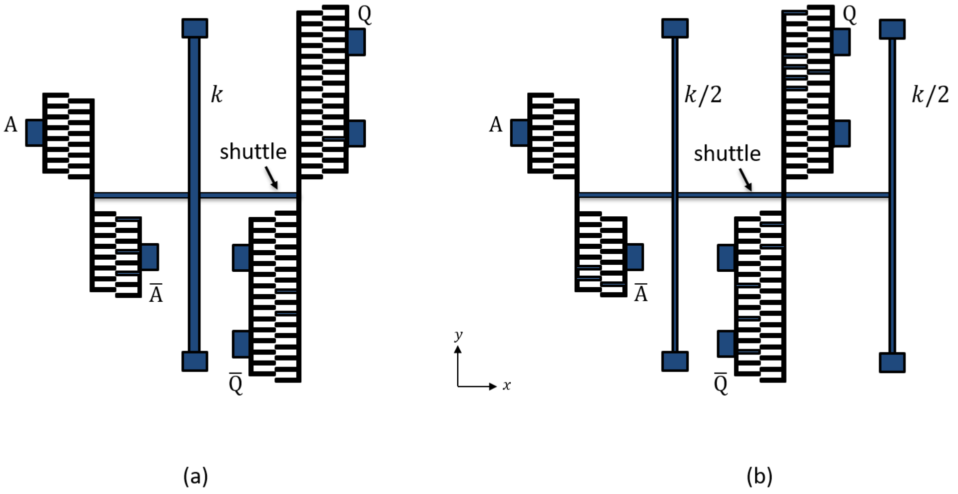


Figure 3.3: a) Inverter gate with a single suspension of a stiffness k, b) Inverter gate with two suspensions of a stuffness $k/2$.

The simplest geometry of a suspension is a double clamped beam, as represented in Figure 3.4. By taking the equation 3.1, we can estimate that a double clamped beam of thickness $H = 5$ µm and width $W = 2$ µm should be of a length $L \approx 0.53$ mm in order to have the lateral spring constant of $k_{\mathrm{x}} = 0.75\ \mathrm{N\,m^{-1}}$. A simple clamped-clamped suspension like this would have a vertical spring constant of $k_{\mathrm{z}} = 3.6\ \mathrm{N\,m^{-1}}$.

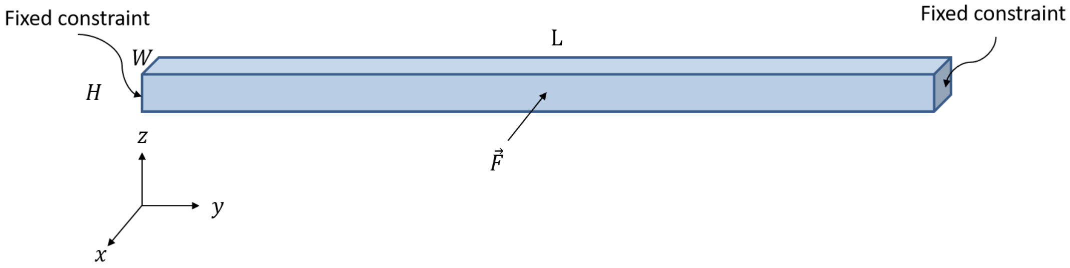


Figure 3.4: Double clamped beam, as defined in COMSOL Multiphysics.

Let us take a look at how the spring constant changes with the folding of the beam (Figure 3.5). As the spring constant k is proportional to the cube of the beam width and inversely proportional to the cube of the beam length ($k \propto \frac{W^3}{L^3}$), one half of the beam would have a spring constant eight times higher. Connecting two half-beams in parallel gives a structure with a spring constant of $4k$. So beam folding does not keep the same spring constant – it multiplies it with a factor of four. Keeping the same k after 1 fold requires either multiplying the total length of the beam with 1.59, or dividing the width by the same factor (multiplying it with 0.63).

Applying this principle to the design of a folded structure that should have thickness

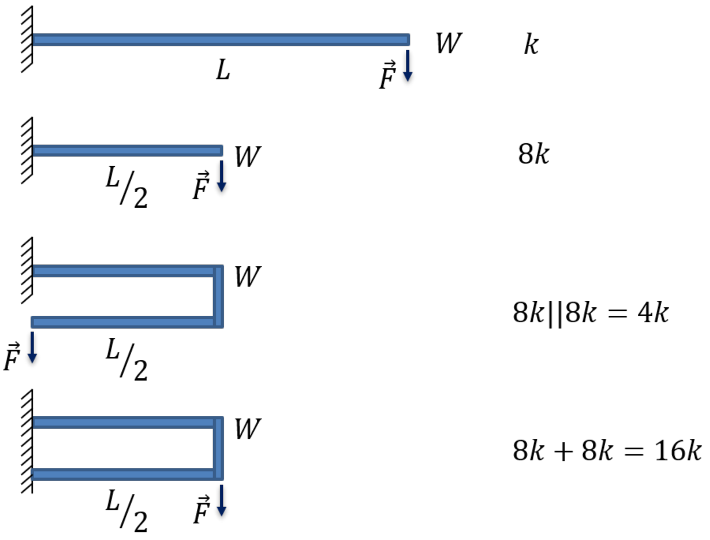


Figure 3.5: Influence of the beam folding on the spring constant.

of $H = 5$ µm and width of $W = 2$ µm, we came up with the geometry shown in Figure 3.6 where $L_1 = 270$ µm, $L_2 = 245$ µm and $d = 10$ µm.

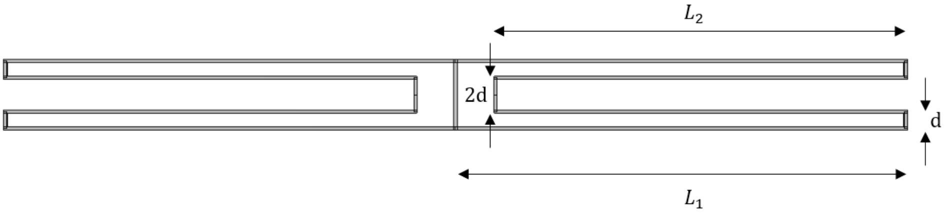


Figure 3.6: Folded beam of a spring constant $k = 0.75$ N m^{-1}, beam width $W = 2$ µm and arm lengths $L_1 = 270$ µm and $L_2 = 245$ µm.

These calculations were validated with COMSOL Multiphysics (Figure 3.7). FEM simulation of the beam deflection after applying a force in the $x-$direction yielded the spring constant of $k_{\text{FEM}} = 0.71$ N m^{-1}. The spring constant in the $z-$direction is an order of magnitude higher ($k_z = 8.6$ N m^{-1}) and is more that twice the size of the k_z of a double clamped beam ($k_z = 3.6$ N m^{-1}). The spring constant in the $y-$direction is $k_y = 150$ N m^{-1}, preventing any rotation of the combs within the $xy-$plane. Although both the spring and the substrate are grounded and therefore experience no attractive force between them, the folded structure is more stable than a double clamped beam. Furthermore, the folded geometry allows the compression and extension in $y-$direction and therefore reduces stress buildup compared to a double clamped beam.

Note that the wafers used during this project are (100) SOI wafers and the spring is oriented in the [110] direction. The values of Young's modulus and the Poisson's ratio of silicon used in the simulations are $E = 170$ GPa and $\nu = 0.064$, respectively. The value of the applied force was $F = 1$ µN.

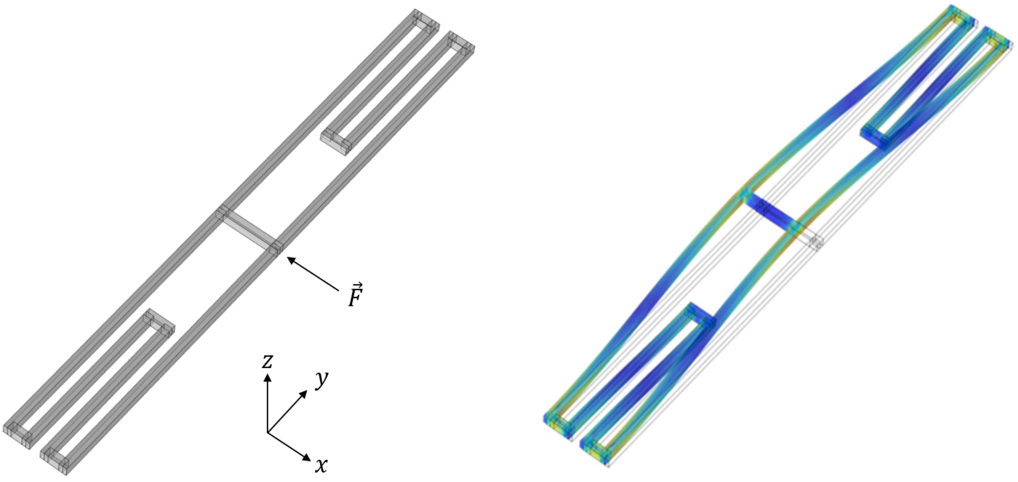


Figure 3.7: FEM simulation of beam displacement by application of a force along the x-axis.

3.1.3 Design of the input combs

The electrodes of the input combs should contain 60 fingers. The width and the spacing of the fingers were set to 0.5 µm, as is the limit of the resolution of the available equipment (Canon FPA 3000i4/i5 Stepper) at the time of the project. By choosing this lowest achievable value we make sure to obtain the highest possible capacitance values (as capacitance is inversely proportional to the gap g between fingers) and smallest gate footprint. The fingers are supported by 2 µm wide beams. These beams, supporting the two movable electrodes in both comb-pairs, are connected to the shuttle. Non-movable electrodes are fixed through 10×30 µm^2 anchors and are wired directly to the contact pads (Figure 3.8). This dimension of the anchors is sufficiently large for them to remain attached to the substrate during the HF releasing step, when 2 µm of SiO_2 are expected to be removed from each sidewall of the anchor. On the other hand, the size is kept as small as possible, so that the contribution to the parasitic capacitance is minimized.

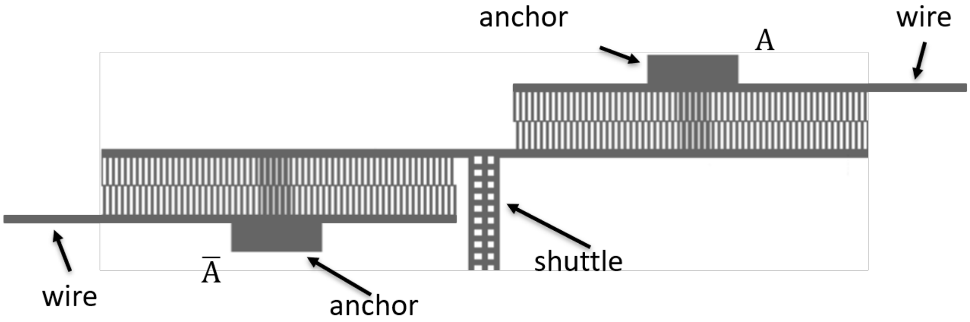


Figure 3.8: Dual rail architecture of the input stage of the inverter gate.

The fingers within combs are experiencing symmetrical pulling forces from adjacent fingers and are therefore in equilibrium. However, the last fingers are experiencing force only from one side. The spring constant of fingers is the one of a clamped-free beam

$k_{\text{finger}} = 26.6\ \mathrm{N\,m^{-1}}$. The pull-in voltage for these fingers is around 50 V, sufficiently above the actuation voltages.

3.1.4 Design of the output combs

The output combs have eight times more fingers than the input combs. In order to preserve a rather squared shape of the gate and to shorten the supporting beams of the movable combs that the fingers are attached to, the output combs are separated in four parallel combs. As the spring constant is inversely proportional to the cube of the beam length, the stiffness of each supporting beam in the output combs is therefore 64 times higher than the spring constant of a single, long comb. This change in geometry contributes to the overall stability of the device, as it drastically decreases the possibility of finger sticking due to comb rotations.

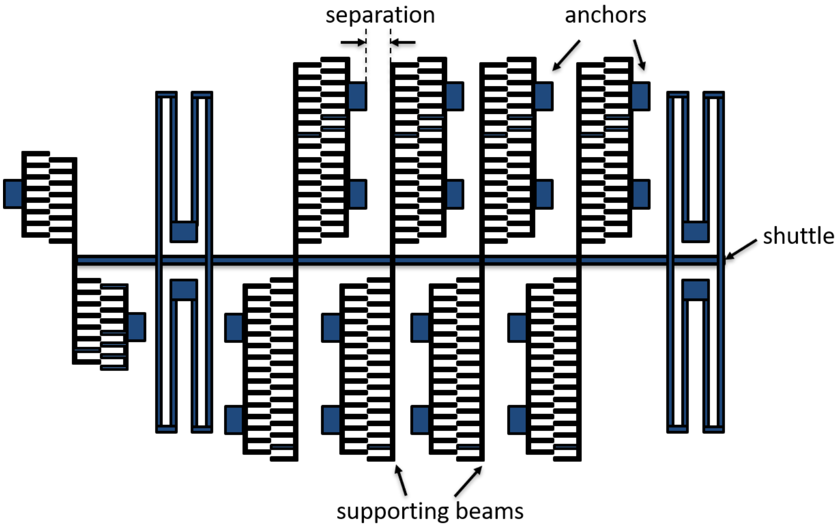


Figure 3.9: Splitting of the output comb into four parallel combs.

In order to reduce the parasitic capacitance, the fixed combs are anchored with fixations of $10 \times 30\ \mu\mathrm{m}^2$, while the supporting beam is kept thinner, at $2\ \mu\mathrm{m}$.

We have also looked into the need for electrical shielding between the supporting beams of the movable combs and anchors of the fixed combs, as they are subjected to different voltages and experience therefore an attractive force between each other. The separation between these two electrodes (see Figure 3.9) has to be at least $10\ \mu\mathrm{m}$ to allow the full displacement of the movable combs (the targeted displacement is a few micrometers, the maximal one is limited by the finger length which is $l = 10\ \mu\mathrm{m}$). Even with the smallest separation of $10\ \mu\mathrm{m}$, the pull-in voltage between the anchors and the supporting beams of the neighboring movable combs is 750 V, which is far above the voltages used for actuation of the device $(10 - 30\ \mathrm{V})$. The electrostatic force established between the supporting beams and adjacent anchors is 50 times lower than the force formed within the combs. The electrical shielding is therefore of no importance.

3.1.5 Design of the fixed combs

The computation of capacitance in the COMSOL Multiphysics software proves to be straightforward when dealing with only two conductors, as was the case with the input (C_A, $C_{\bar{A}}$) and output combs (C_Q, $C_{\bar{Q}}$). In this scenario, one conductor, specifically the movable comb-electrode, is grounded, while the other, the anchored comb-electrode, is designated as a terminal. Capacitance, defined as the charge required to elevate the electric potential by 1 volt relative to a grounded reference potential, can be quantified by utilizing a built-in variable within the simulation.
However, when confronted with more than two conductors, the complexity of the problem increases. This is the case of fixed capacitors (C_{fix}), where one comb-electrode is subjected to power clock (PC) voltage, and the potential at the other is dictated by the motion of the output combs, ultimately determining the gate's output voltage.

Mutual and Maxwell Capacitance Matrices

In an electrical system consisting of several conductors, mutual capacitance occurs between two charge-holding objects. In our case, the fixed capacitor can be schematically represented as in Figure 3.10 (left).

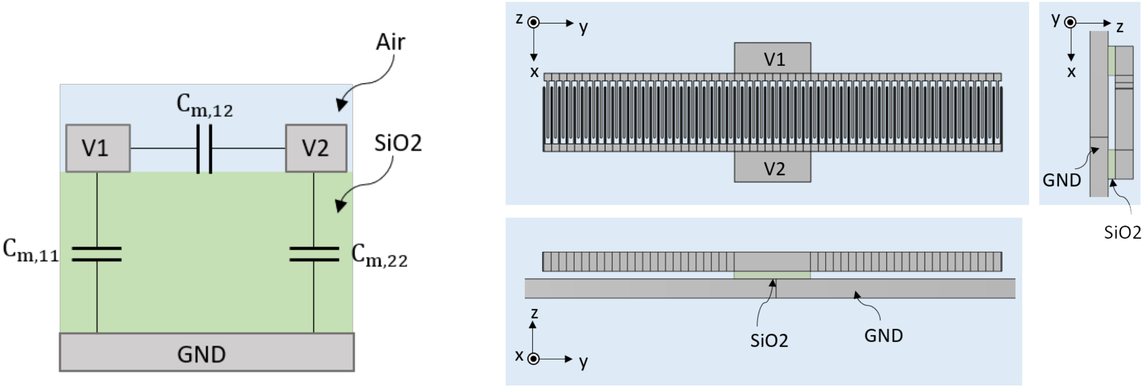


Figure 3.10: Left: Mutual capacitance in a system with three conductors. Right: Comsol multiphysics model of a fixed capacitor.

It is possible to use matrix form to represent a system of two conductors and one ground plane:

$$\begin{bmatrix} C_{m,11} & C_{m,12} \\ C_{m,21} & C_{m,22} \end{bmatrix} \tag{3.3}$$

The Maxwell capacitance matrix on the other hand describes a relation between the charge Q_n of the n^{th} conductor to the voltages of all conductors in the system. By measuring the charge Q_1 on conductor 1, when only the potential V_1 is applied and all other electrodes are keep at ground, we can determine the Maxwell capacitance matrix coefficient C_{11}.

$$\begin{pmatrix} Q_1 \\ Q_2 \end{pmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{3.4}$$

For a system with two conductors, the relation between the mutual and Maxwell capacitance matrices is then:

$$\begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \begin{bmatrix} C_{m,11} + C_{m,12} & -C_{m,12} \\ -C_{m,21} & C_{m,21} + C_{m,22} \end{bmatrix} \tag{3.5}$$

With this terminology clarified, we can proceed with the series of steps for defining the shape and size of the fixed combs with the help of the capacitance matrix. The value of the fixed capacitance C_{fix} should be around $380\varepsilon_0 h_{\text{e}} N \approx 500$ fF, which is about three times higher than the capacitance of the output combs Q and $\bar{Q}$ at the rest position (~ 170 fF). For the purpose of having a tolerable (tens of minutes) length of computation, the number of fingers in the comb-model was kept at 60 - as is the number of fingers in the input combs A and $\bar{A}$. The length of the fingers l_{fix} and their overlap u_{fix} were increased (compared to A, $\bar{A}$, Q and $\bar{Q}$) to 15µm and 13.5µm, respectively, in order to significantly increase the capacitance, while keeping the overall size of the C_{fix} small. The finger width and spacing are kept the same as in input and output combs at 0.5µm.

The interface of the Electrostatics module of COMSOL Multiphysics allows us to set terminal conditions to both of C_{fix} electrodes. In order to calculate capacitance matrices, we need to apply different voltages to the terminals. One electrode of the C_{fix} is subjected to the power clock voltage V_{PC}, whereas the other is established at the output voltage V_Q or $V_{\bar{Q}}$. Therefore, in our simulation the terminal voltages V_1 and V_2 were set to 30 V and 10 V, respectively. The resulting capacitance values are however independent of the voltage values used for simulation. By setting terminals as a sweep parameter and running a sweep over the terminals, COMSOL Multiphysics software sets activates one terminal at the time and sets all others to ground during the sweep. This simulation results in the two solutions, from which we can extract the Maxwell capacitance matrix:

$$\begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \begin{bmatrix} 176.93 & -165.45 \\ -165.45 & 176.49 \end{bmatrix} \text{fF} \tag{3.6}$$

The Maxwell capacitance matrix can be converted to Mutual capacitance matrix using Equation 3.5.

$$\begin{bmatrix} C_{m,11} & C_{m,12} \\ C_{m,21} & C_{m,22} \end{bmatrix} = \begin{bmatrix} 11.48 & 165.45 \\ 165.45 & 11.04 \end{bmatrix} \text{fF} \tag{3.7}$$

This conversion gives us the value of the capacitance between the two electrodes of $C_{m,12} = C_{m,21} = 165.45$ fF. As the fixed capacitor should have the capacitance of $C_{\text{fix}} = 500$ fF, the number of fingers in this structure should be increased to $60 \cdot 500/165.45 = 184$.

The value $C_{m,11} = C_{m,22} = 11.48$ fF corresponds to the self-capacitance of each electrode, that is, to the capacitance of each electrode with respect to ground.

Figure 3.11 shows the final design of the inverter gate in comparison to the device schematic introduced at the beginning of the chapter.

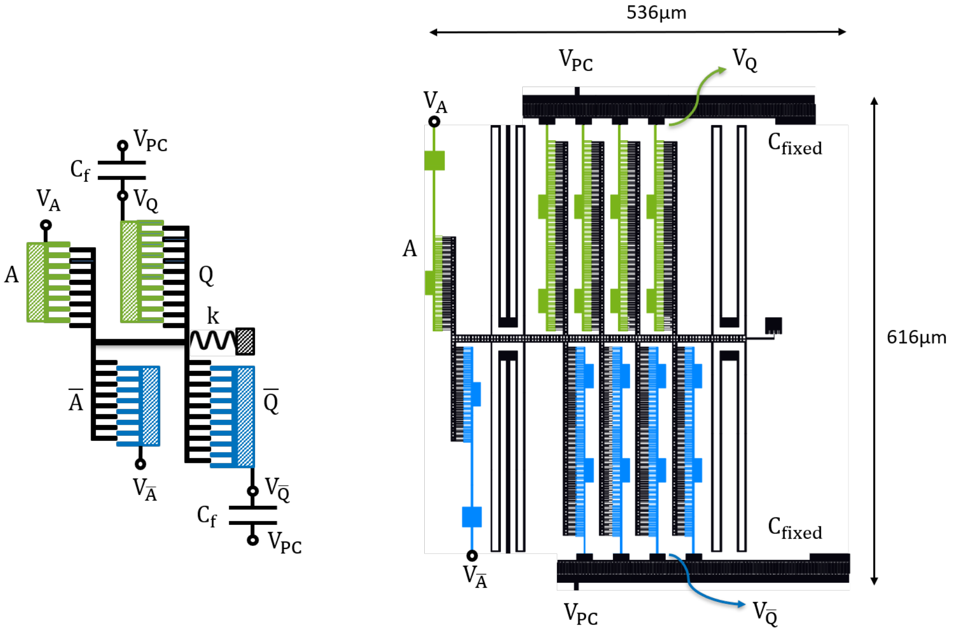


Figure 3.11: Schematic and the final design of the inverter gate.

3.2 Fabrication process optimization on silicon

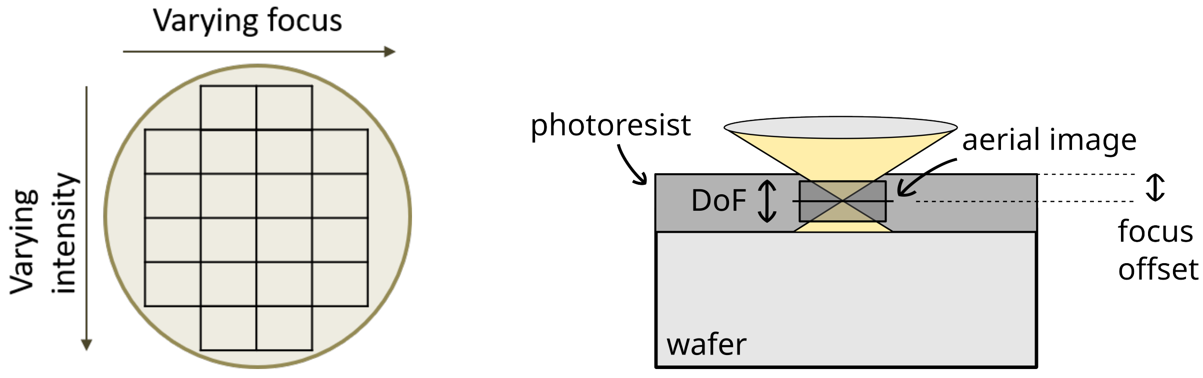
The complete microfabrication process was done in the clean room of LAAS-CNRS in Toulouse. The first fabrication experiments were performed on n-doped test-grade silicon wafers. These tests allowed me to optimize the parameters for photolithography and DRIE (Deep Reactive Ion Etching) before transferring the process to SOI wafers.

3.2.1 Lithography with the Stepper

The fabrication conditions have to be carefully controlled as the device operation is strongly dependent on the geometrical variations (chapter 2). The smallest feature (critical dimension of the process) is 0.5 µm and corresponds to the width of the fingers and gaps between them (d). This feature has to be transferred to silicon and etched to the depth of 5 µm. This pattern transfer requires a thick photoresist (~ 1 µm) that can sustain a long etching process. Furthermore, the pattern realized in the photoresist has to be well defined across the whole photoresist thickness.

The tool used for photolithography was Canon FPA 3000i4/i5 Stepper, which can perform variation of the exposure parameters in different parts of the wafer. It allows splitting wafer into multiple dies and exposure of the dies with exactly the same pattern, but with different exposure parameters. Each exposure area measures 6×7 mm^2, with achievable resolution up to ≤ 500 nm. The numerical aperture (NA) of the Canon Stepper is 0.63 and the depth of focus (DoF) is 0.7 µm

This feature allowed us to define a *matrix* of process parameters to modulate exposure dose along one axis of the wafer and focus-offset along the other. Consequently, a process window was identified, revealing the optimal combination of these parameters, as illustrated in Figure 3.12.



(a) (b)

Figure 3.12: a) Illustration of a wafer being exposed with Canon Stepper tool, by varying exposure dose and focus on each die. b) Illustration of projection lithography.

The wafers were prepared for photolithography in the following way:

1. Cleaning with the standard RCA process.
2. Applying BARC (**B**ottom **A**nti **R**eflective **C**oating):
   (a) Spin coating: 30 s at 4000 rpm
   (b) Baking on the hot plate: 60 s at 200°C.
3. Applying ECI (MicroChemicals) photoresist by spin coating.
   (a) EVG120 (EVG Group) tool: 30 s, 4000 rpm, 2900 acceleration, achieved thickness: 1.1 µm.
   (b) Deposition is followed by soft bake for 60 s at 90°C.

   Wafers are cooled down completely before proceeding to the exposure step.

The fabricated test-patterns on pure silicon wafers included sets of identical parallel lines (Figure 3.13). The sets were varying in line widths and gaps between them, from 0.1 µm to 5 µm. These test structures were used to determine the smallest line width that could be used as the width of the fingers in comb-drive structures. The narrower the fingers are in the comb-drive, the smaller is the footprint of the entire gate. Exposure dose for 1.1 µm thick ECI photoresist was varied from 700 $\mathrm{mJ\,cm^{-2}}$ to 1600 $\mathrm{mJ\,cm^{-2}}$ in 100 $\mathrm{mJ\,cm^{-2}}$ steps, whereas the focus-offset was varied from -1 µm to 0.3 µm in 0.1 µm steps.

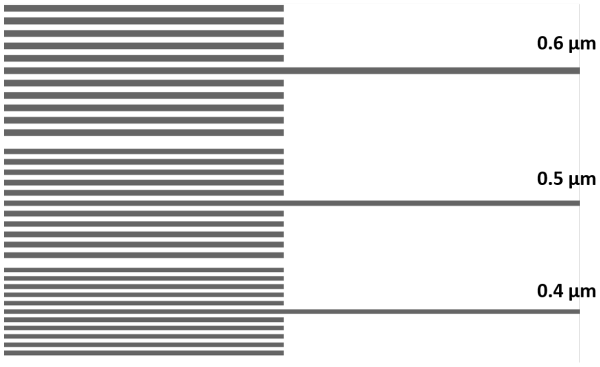


Figure 3.13: Snippet of a test pattern fabricated on n-doped silicon wafers and used to optimize the microfabrication parameters. The width of the lines and gaps varies from 0.1 µm to 5 µm.

3.2.2 Deep reactive ion etching of silicon

Reactive Ion Etching (RIE) and its extended form, Deep Reactive Ion Etching (DRIE), represent methodologies that blend physical and chemical procedures to eliminate material from the surface of a wafer. The etch rate achieved through RIE surpasses that of purely physical processes significantly. DRIE, as an expansion of RIE, facilitates high-rate etching of deep and narrow structures. The process itself unfolds in a gaseous environment, typically executed in a vacuum. Fluorine, chlorine, or bromine plasma is commonly employed for etching silicon and its compounds. Additionally, many etching processes incorporate the use of oxygen.

The optimization of the Deep Reactive Ion Etching (DRIE) process involves adjusting various parameters such as the concentration of etchant gases, flow rate of selected gases, bias voltage, radio frequency (RF) power, pressure, and temperature during the process. A high-density plasma is generated through an inductively coupled plasma (ICP) source, and a second capacitively coupled power source controls the bias voltage. Processes utilizing fluorine-based etching demonstrate superior etch rates for silicon and high selectivity to the mask material. In DRIE, it becomes feasible to achieve a photoresist mask selectivity one order of magnitude higher than conventional Reactive Ion Etching (RIE) systems ($10 - 100 : 1$ compared to $1 - 10 : 1$).

Nearly vertical structures are achieved by using Bosch process which alternates between two different process steps. The first one is a standard plasma etch (isotropic), in which sulfur hexafluoride (SF_6) is commonly used for etching silicon. The second step is passivation during which C_4F_8 creates a protective layer across the whole substrate, preventing therefore further etching. In the subsequent plasma etching step, ions are accelerated towards the substrate and bombard the bottom of the trenches, thereby removing the passivation layer and allowing another round of isotropic removal of silicon, while protecting the sides of the previously etched layer. By adjusting the time of etching/passivation, we can tune the process to have either higher etch rate (larger cycles) or yield smoother sidewalls (shorter cycles). Both of these steps are illustrated in Figure 3.14.

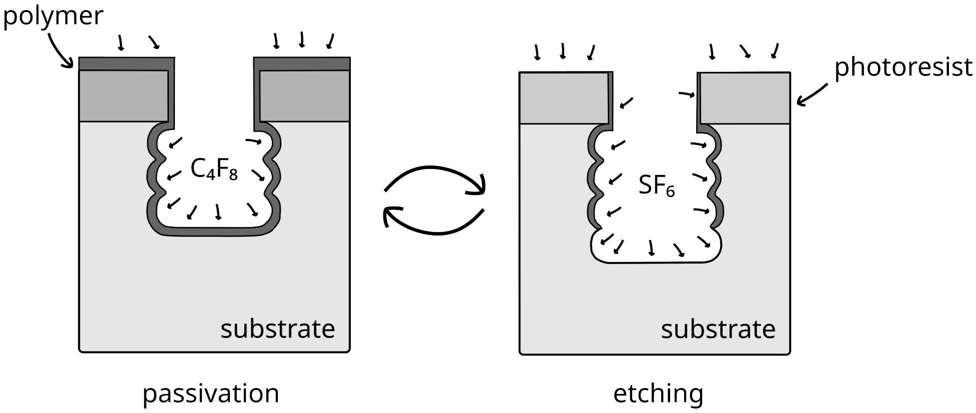


Figure 3.14: Illustration of Bosch process with alternating etching and passivation steps, resulting in a wall profile with increased roughness.

The etching of the previously prepared wafers was performed in Alcatel AMS4200, a high-density plasma reactor, for 65 s with cycle 2.2s/2s (SF_6/C_4F_8). This time was sufficient to reach the depth of around 4.5 µm, which is near the value of the top silicon layer thickness of the SOI wafers that will later be used.

The combination of exposure dose and focus that yielded the structures closest in size to the ones on the mask is with the exposure dose of $620 - 680$ mJ cm^{-2} and focus offset of 0.3 µm – 0.4 µm.

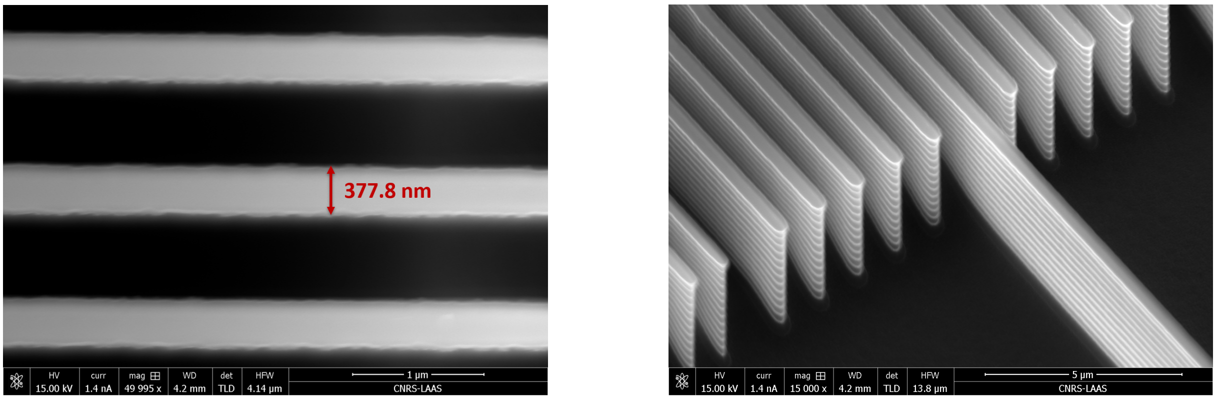


Figure 3.15: SEM micrographs of the parallel lines designed to be 0.5 µm wide, viewed from the top (left) and under an angle (right). The resulting geometry features underetched lines with the width reduced by $\sim$ 120 nm.

Underetching was measured to be about 120 nm. This can be compensated at the design level by adjusting the feature sizes in order to compensate for the size reductions during photolithography and etching steps. Furthermore, the finger tips, designed as squared, have turned out to have a rounded shape after the fabrication. This change of the shape of the finger tips was considered in our modeling in order to ensure the closest description of the device behavior.

3.3 Process on SOI

The examinations conducted on silicon wafers yielded valuable insights into the microfabrication process, including aspects such as attainable resolution, variations in pattern size subsequent to photolithography and etching stages, and the etching speed along with selectivity between photoresist and silicon. These acquired insights were further considered during the design phase of the mask, incorporating logic devices and test patterns.

3.3.1 Varying underetching compensation

The Canon Stepper reticle accommodates nine distinct designs for exposure (Figure 3.16). Three of these designs are allocated for various layers in the microfabrication process, encompassing the device layer, metal deposition, and electrode protection. The remaining six slots are dedicated to the evaluation of underetching compensation. Specifically, the dimensions of features within the structures were systematically augmented by a parameter denoted as d_{comp} to counteract size reduction. The incremental adjustment of the d_{comp} value ranged from 0 to 240 nm, with increments of 40 nm.

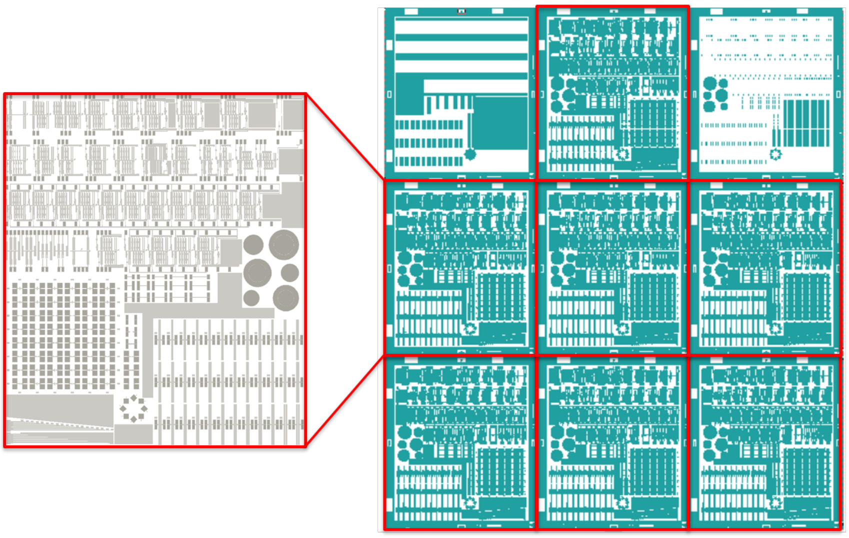


Figure 3.16: Reticle of the Canon Stepper with nine exposure patterns. Seven of them correspond to the *device layer* with varied underetching compensations from $d_{\text{comp}} = 0$ to $d_{\text{comp}} =$ 240nm.

3.4 Test structures

Beyond the inverter-gate devices, the mask layout integrates an array of structures strategically designed to perform the testing of distinct components within the inverter gate. These components encompass the input and output stages, spring, fixed capacitors, and other relevant elements. Additionally, supplementary components are incorporated to assess both the fabrication process and material properties. Figure 3.17 shows the layout of the mask with numbering of all the designed test-structures. A comprehensive list of all these elements is provided in Table 3.1.

1	Characterization of the input stage: only input stage + springs + displ. measurement
2	Characterization of the output stage: only input stage + springs + displ. measurement
3	Device with 2 output stages + springs + displ. measurement
4	Full standalone logic gate ($n = 20$, $u_{0A} = u_{0Q} = 0$)
5	Logic gate with load imitating the next gate
6-8.	Logic gate with load for direct readout. Variation in the load size.
9	Calibration patterns for measurement
10	Standalone logic gate with $n = 10$
11	Standalone logic gate with $\mathrm{C_{fix}}/2$
12	Standalone logic gate with $\alpha = 4$
13	Standalone logic gate with $u_{0A} = u_{0Q} = 1$ µm
14	Standalone logic gate with $u_{0A} = u_{0Q} = -1$ µm
15	Standalone logic gate with increased capacitance to the ground
16	Standalone logic gate with a single spring
17-20	Shrunken device (variations) – halved number of fingers in input, output and fixed comb, halved spring constant
21	Cascade of 11 logic gates, pad pitch 230 µm
22	Characterization of different springs – resonance measurement, releasing process
23	Standalone logic gate with the output directly connected to the pad
24	Cascade of 4 logic gates, pad pitch 230 µm
25	Silicon resistance measurement, influence of underetching
26	Measurement of the capacitance to the ground per unit area
27	Measurement of residual stress in Si after releasing – clamped-free and clamped-clamped bream
28	Fixed capacitance – varying finger overlap from 13.5 µm to −13 µm (step size is finer in the gray zone)
29	Electrical field in a a) plate-plate, b) tip - tip (0.5 µm), c) tip – tip (5 µm) and d) plate – tip (0.5 µm) configurations. Leakage current and max voltage measurement. Varying gap size (0.3 µm to 2 µm). Plate height 50 µm.
30	Young modulus depending on the orientation of the tip compared to wafer's crystal orientation.

Table 3.1: List of all the test structures - V1.

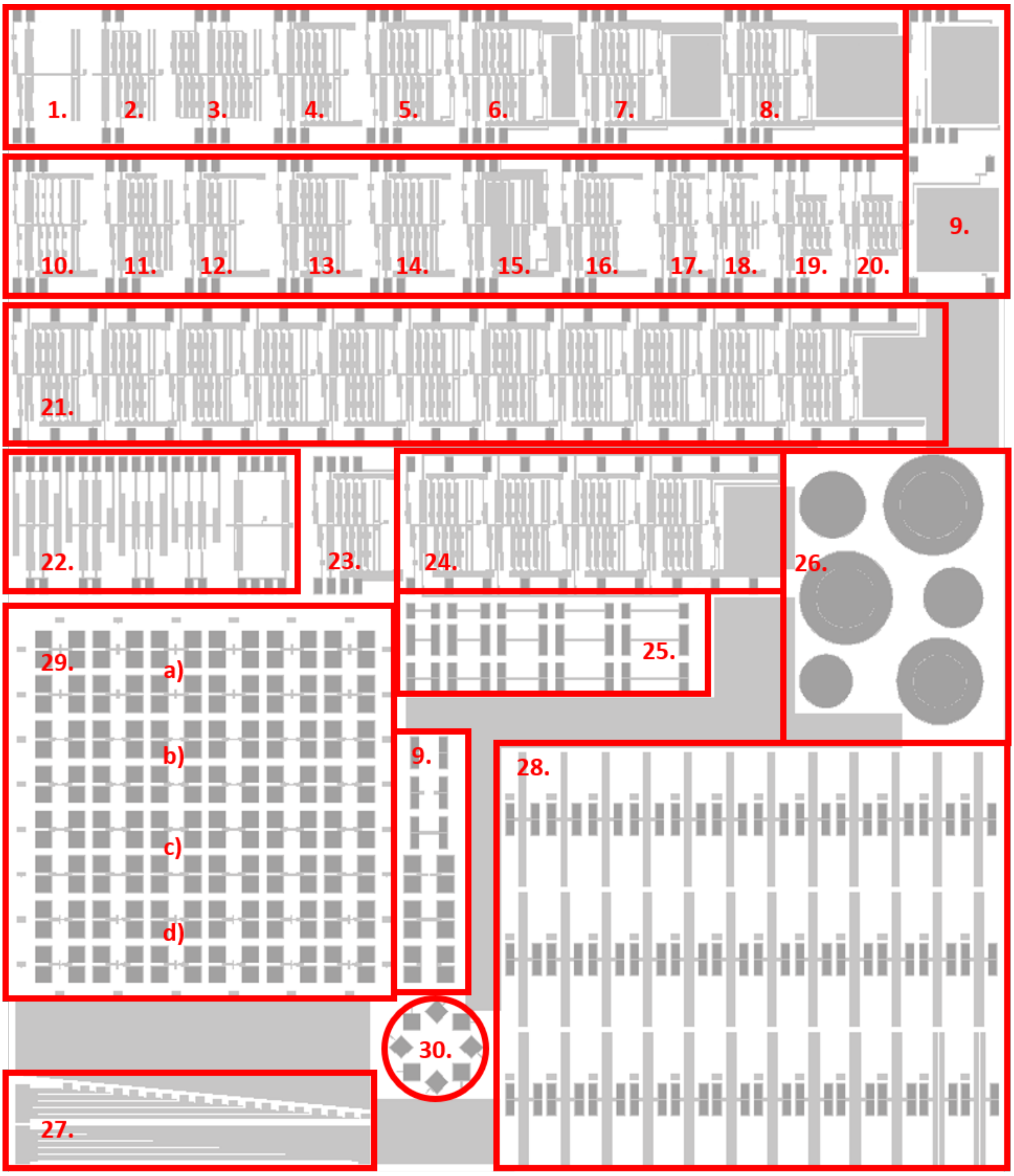


Figure 3.17: The first iteration of the microfabrication mask, containing 30 test structures.

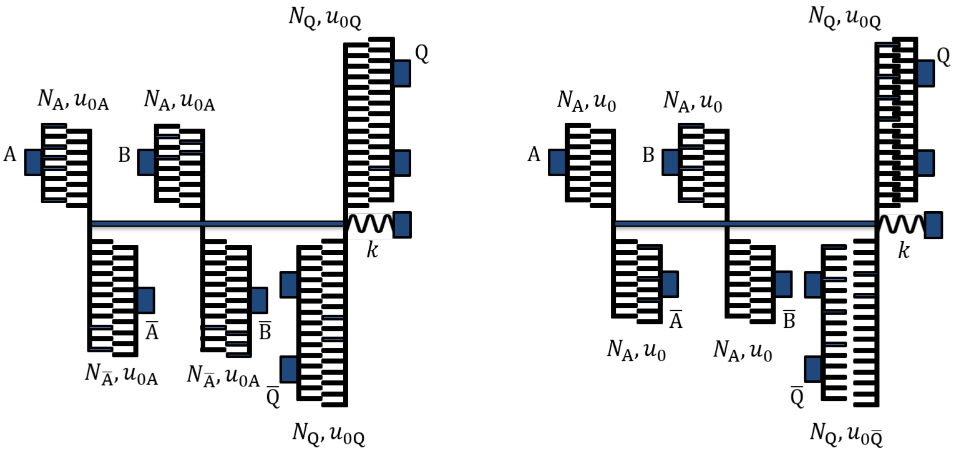
3.5 Design of a NAND gate

A NAND gate, a fundamental component in digital electronics, operates on two inputs and produces an output. It yields a logic high (1) output unless both inputs are logic high, in which case it outputs a logic low (0) (see truth table 3.2). Along with the inverter (NOT) gate, NAND gates can be used to create any other logic gate, including AND, NOR, OR and XOR. Employed extensively in constructing logic circuits, NAND architecture allows for the creation of complex systems, making it a cornerstone in digital logic design and computation.

A	B	Q
1	1	0
1	0	1
0	1	1
0	0	1

Table 3.2: Truth table of a NAND gate.

This section describes the operational characteristics of two potential implementations of a NAND function derived from a previously developed inverter gate. The first one suggests the asymmetry of the numbers of fingers between the complementary electrode pairs in the input combs. In contrast, the second implementation suggests asymmetry in the finger overlap between the complementary combs at the output stage. The NAND function is important in logic because it allows execution of both combinatorial and sequential functions. Both geometries are represented in Figure 3.18.



(a) (b)

Figure 3.18: Schematic of two different realizatons of NAND gate with asymmetrical number of fingers between the complementary electrodes at the input stage (a) and asymmetrical overlap of the fingers (b).

Asymmetric number of fingers

In the resting state all the comb-pairs have finger overlap of $u_{0A} = u_{0Q} = 0$. However, the number of fingers in the complementary comb-pairs A and $\bar{A}$, as well as B and $\bar{B}$ is different (Table 3.3).

N_{A}	$N_{\bar{\mathrm{A}}}$	N_{Q}	u_{0A}	u_{0Q}
30	60	240	0	2 µm

Table 3.3: NAND gate with the variation of the number of fingers at the input stage.

Asymmetric finger-overlap at the input stage

In the resting state the input comb-pairs have finger overlap of $u_{0A} = 0$ (Both A and $\bar{A}$, as well as B and $\bar{B}$ have the same initial overlap). The output comb-pair has asymmetrical geometry. The overlap u_{0Q} in the resting state is different for Q and $\bar{Q}$ (Table 3.4).

N_{A}	N_{Q}	u_{0A}	u_{0Q}	$u_{0\bar{Q}}$
60	480	0	2 µm	−2 µm

Table 3.4: NAND gate with the variation of the finger overlap.

If both A and B are set to 1, the force acting on the movable part of the output comb is sufficiently large to overcome the asymmetry stemming from either overlap (a) or the number of fingers (b) and bring the movable comb to the left – resulting in the positive overlap at $\bar{Q}$ and negative at Q – corresponding to the state 1 at the output.

In all the other cases the force acting on the movable part of the output comb is not sufficient – movement will be to the right.

Regarding the fabrication process and its impact on device's operation, the design with asymmetric number of fingers is expected to perform better, as its working principle would be less affected by the underetching and small changes in size.

3.6 Fabrication process

Figure 3.19 illustrates the main steps of the fabrication process. We use 4-inch (100 mm) (1-0-0) SOI wafers with the device layer of 5 µm and buried oxide of 2 µm thickness. Device layer has resistivity of $0.001 - 0.005\,\Omega\,\mathrm{cm}$, it is n-doped with As with concentration $10^{19}\ -\ 10^{20}\ \mathrm{cm}^{-3}$.

Before the beginning of the fabrication wafers are cleaned in the standard RCA procedure. This step ensures removal of all the organic and ionic contaminants from the wafer surfaces. Cleaned wafers are first coated with bottom anti reflective coating (BARC) and baked

at 200°C for 60 s. On top of the cooled-down BARC a positive ECI (MicroChemicals) photoresist is applied and soft-baked for 90 s using EVG120 (EVG Group) automatic resist processing system. Exposure is done on Canon FPA 3000i4/i5 Stepper (Figure 3.19a), which allows photoresist exposure at 365 nm (i-line), followed by a development in MF-CD-26 (Microposit) developer with EVG120 system (Figure 3.19b).
Pattern transfer into silicon is performed with Alcatel AMS4200, a high-density plasma reactor (Figure 3.19d). The reactor is ICP-RIE (Inductively Coupled Plasma) and is used for treatment of 4-inch wafers. The top silicon layer is etched in a DRIE procedure (Bosch process) with cycle 2.2s/2s (SF_6/C_4F_8).
Movable parts are finally released in the hydrofluoric acid that etches the buried oxide beneath the structures (Figure 3.19d). During this step, samples are submerged in buffered HF (5%) for 35 min. Following this step, DI water is slowly introduced, reducing the concentration of buffered HF. After 20 min when the HF is flushed away, the sample is transferred into ethanol. Finally, the sample is dried in supercritical CO_2 dryer (Tousimis 915B) by bypassing the critical point (31°C, 73 bar).

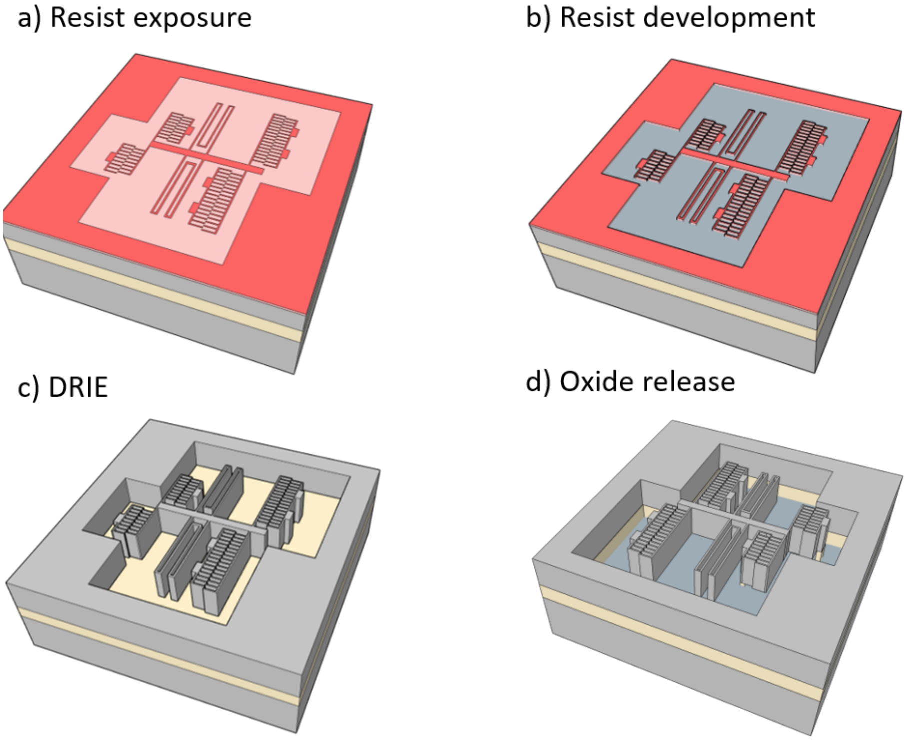


Figure 3.19: Process flow for the microfabrication of the contactless capacitive MEMS device: a) Coating with the ECI photoresist and mask exposure; b) Pattern development in MF-CD-26; c) Bosch process – pattern transfer in the top silicon layer; d) Releasing of the movable structures in hydrofluoric acid – wet etching of buried oxide.

3.7 Fabrication results

During the testing of the underetching compensation u, wafer surface was divided into four regions, whereby each region was exposed with a pattern featuring one single underetching compensation. In the first test run, underetching compensations were set at $d_{\text{comp}} = 40$ nm, 80 nm, 120 nm, and 160 nm. The exposure doses were systematically varied, ranging from lower values (600 $\text{mJ}\,\text{cm}^{-2}$) to higher values (760 $\text{mJ}\,\text{cm}^{-2}$). SEM imaging was employed to examine the resulting structural features.

It is important to note that the lithography and etching conditions are not the same for fixed capacitors whose opposing fingers have significant overlap (13.5 nm, compared to their length of 15 nm) and variable capacitors whose fingers have no overlap. In the case of fixed capacitor, the distance between vertical surfaces of the neighboring structures is 0.5 nm (d), whereas in the case of variable capacitors it is 1.5 nm ($3d$). This means that the C_{fix} are more challenging for definition during photolithography, whereas the underetching is more prominent in the variable capacitors.

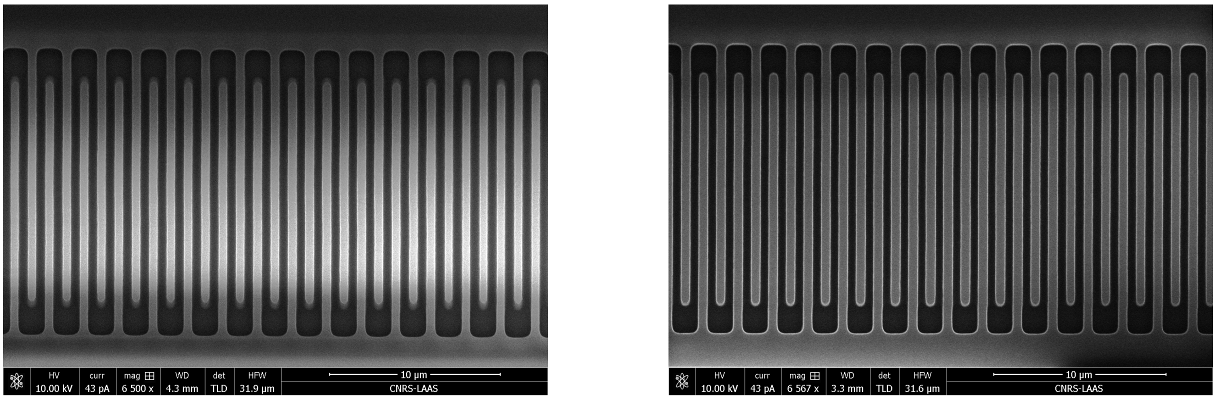
Figure 3.20 showcases SEM images of fixed capacitors C_{fix} with underetching compensations of $d_{\text{comp}} = 40$ nm, 80 nm, 120 nm and 160 nm, respectively. These components pose the highest demands for fabrication, as they feature patterns of the dimensions around the resolution limit of the available equipment ($\sim$ 0.5 µm). The spacings between the fingers have to be well defined during the photolithography and thoroughly etched in a Bosch process.

As shown in sub-figures 3.20 (a) and (b) ($d_{\text{comp}} = 40$ nm and 80 nm), even at the lower exposure doses of $600 - 660$ $\text{mJ}\,\text{cm}^{-2}$, features are well defined, indicating successful exposure and development. Conversely, in the cases shown in sub-figures 3.20 (c) and (d), with underetching compensations of $d_{\text{comp}} = 120$ nm and 160 nm, the resulting images reveal poorly defined features after development, despite using a higher exposure dose of 760 $\text{mJ}\,\text{cm}^{-2}$.

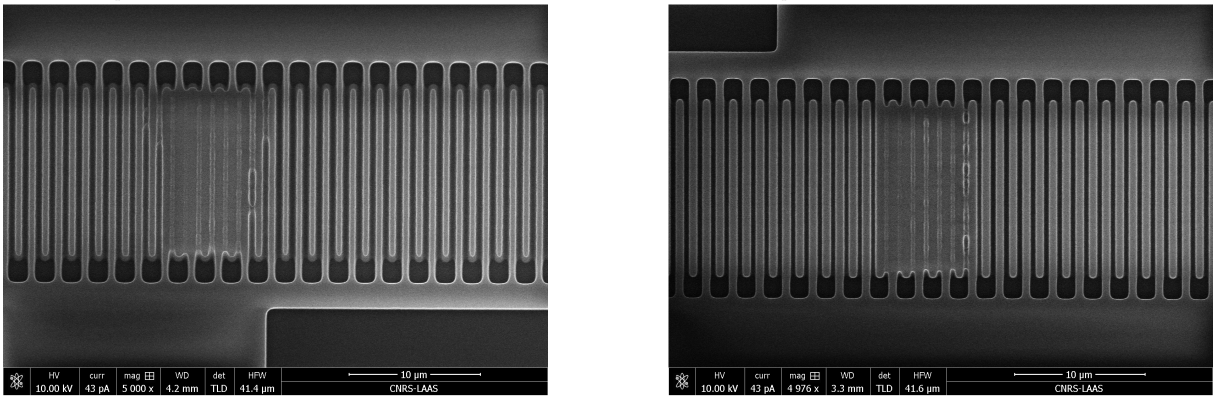
The clarity of finger patterns in fixed capacitors was frequently compromised when employing higher underetching compensation values ($d_{\text{comp}} \geq 120$ nm), although this issue was less prevalent when patterns were exposed with higher doses ($\geq$ 700 $\text{mJ}\,\text{cm}^{-2}$). Despite the existence of devices with well-separated fingers (Figure 3.21 (a)) in this context, these devices exhibited a notable overexposure of finger tips in the input capacitors (Figure 3.21 (b)).

Conversely, devices exposed with lower doses, particularly those at the lower end of the tested spectrum ($\leq$ 700 $\text{mJ}\,\text{cm}^{-2}$), demonstrated distinct and well-defined finger tips in the input combs (Figure 3.21 (b)).

This suggests that underetching compensations of $d_{\text{comp}} = 40$ nm and 80 nm yield favorable results, even with reduced exposure energy, whereas the underetching compensations of $d_{\text{comp}} = 120$ nm and 160 nm do not yield satisfactory results, even with an increased exposure dose. For that reason, underetching compensations of $d_{\text{comp}} = 200$ nm



(a) $d_{\mathrm{comp}} = 40$ nm, exp. dose: 600 $\mathrm{mJ\,cm^{-2}}$ **(b)** $d_{\mathrm{comp}} = 80$ nm, exp. dose: 660 $\mathrm{mJ\,cm^{-2}}$



(c) $d_{\mathrm{comp}} = 120$ nm, exp. dose: 760 $\mathrm{mJ\,cm^{-2}}$ **(d)** $d_{\mathrm{comp}} = 160$ nm, exp. dose: 760 $\mathrm{mJ\,cm^{-2}}$

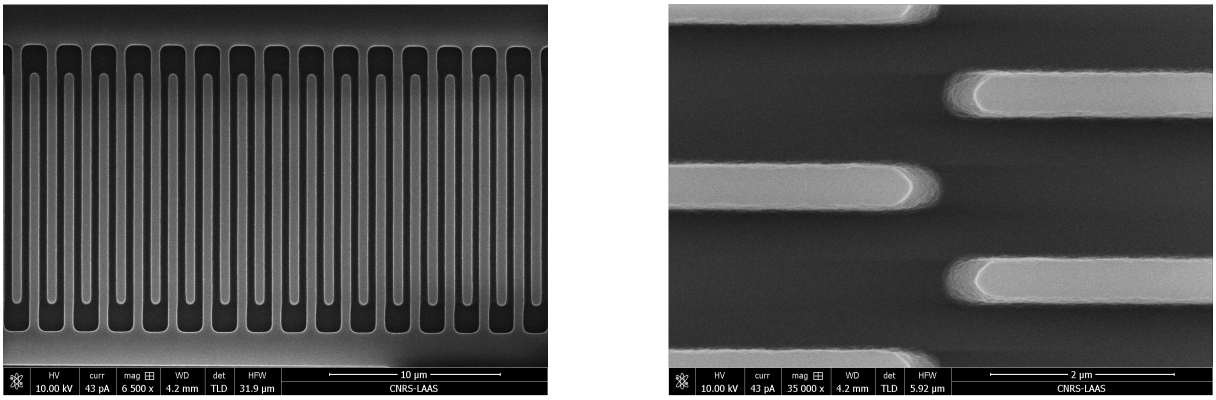
Figure 3.20: SEM images of the fixed capacitors with different underetching compensations and exposed with different doses. The images are made after exposure and development of the photoresist.

and 240 nm were not even taken into consideration.

The beam supporting the comb-fingers in the movable electrode at the output stage is characterized by dimensions of 245 µm in length, 5 µm in width, and 2 µm in thickness, with a corresponding spring constant of 0.31 $\mathrm{N\,m^{-1}}$, obtained by FEM. During device testing, the electrodes within the combs experienced bending of the supporting beams, leading to instances of sticking (Figure 3.23).

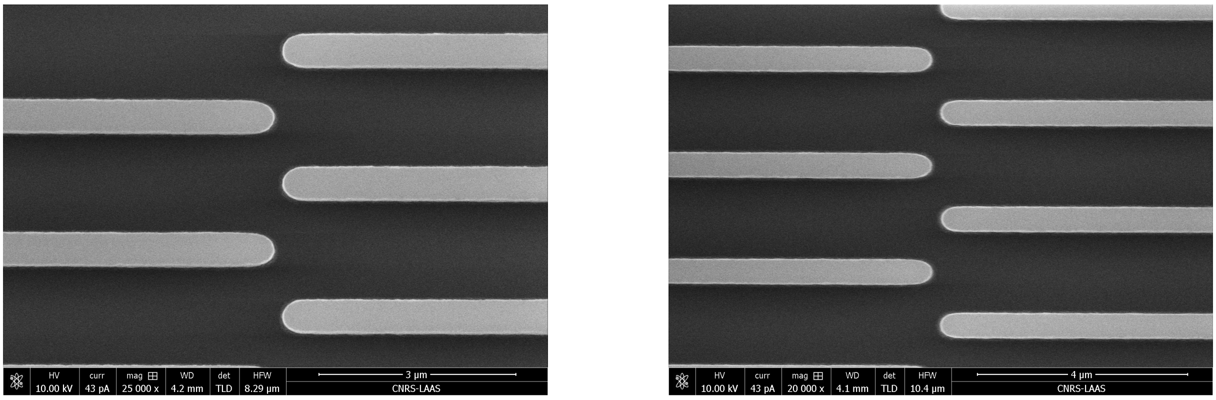
To address this issue and enhance the stiffness of the supporting beam, in the second iteration of the device design, the beam width was tripled, resulting in a new spring constant of approximately 8.4 $\mathrm{N\,m^{-1}}$, representing a 27-fold increase. To facilitate the microfabrication process step involving release in hydrofluoric acid (HF), 2×2 $\mu\mathrm{m}^2$ openings were strategically incorporated into these larger supporting beams, allowing HF to permeate through these openings during the release step (Figure 3.24). This modification aims to optimize the overall performance and reliability of the device.

The subsequent version of the photolithography mask replicated test structures $1. - 20.$ from the first one (Figure 3.25), but with the enhanced stiffness of the supporting beams. However, modifications were made to test structures 21 through 30, which were substituted



(a) **(b)**

Figure 3.21: SEM micrographs of the fixed and input capacitors with $d_{\text{comp}} = 120$ nm underetching compensation and exposed with 760 mJ cm^{-2}. The images are made after exposure and development of the photoresist.



(a) $d_{\text{comp}} = 20$ nm, exp. dose: 640 mJ cm^{-2} **(b)** $d_{\text{comp}} = 40$ nm, exp. dose: 660 mJ cm^{-2}

Figure 3.22: SEM micrographs of the input capacitors with different underetching compensations and exposed with different doses. The images are made after exposure and development of the photoresist.

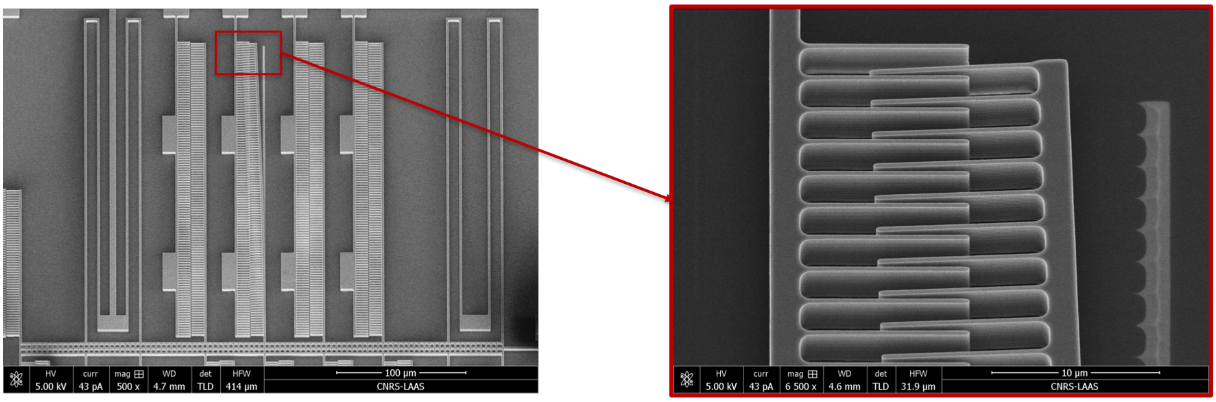


Figure 3.23: SEM micrographs of the movable electrode being bent due to low stiffness of the beam supporting the fingers of the comb.

with configurations including four cascades of 11 inverter gates, four cascades of 4 inverter gates, and various NAND structures.

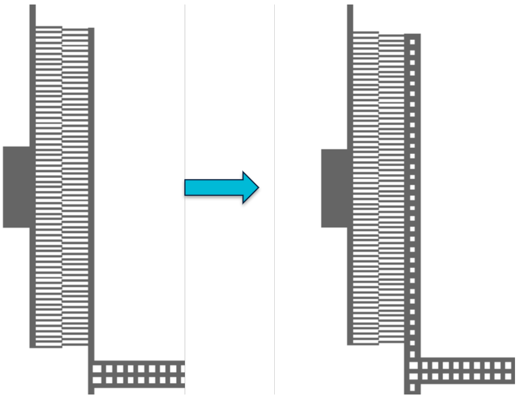


Figure 3.24: Proposed improvement of the stiffness of the supporting beams

A comprehensive list of these test structures is provided in Table 3.5, while a visual representation of the mask with numbered test devices can be found in Figure 3.25.

1	Characterization of the input stage: only input stage + springs + displ. measurement
2	Characterization of the output stage: only input stage + springs + displ. measurement
3	Device with 2 output stages + springs + displ. measurement
4	Full standalone logic gate ($n = 20$, $u_{0A} = u_{0Q} = 0$)
5	Logic gate with load imitating the next gate
6-8.	Logic gate with load for direct readout. Variation in the load size.
9	Calibration patterns for measurement
10	Standalone logic gate with $n = 10$
11	Standalone logic gate with $\mathrm{C}_{\mathrm{fix}}/2$
12	Standalone logic gate with $\alpha = 4$
13	Standalone logic gate with $u_{0A} = u_{0Q} = 1$ µm
14	Standalone logic gate with $u_{0A} = u_{0Q} = -1$ µm
15	Standalone logic gate with increased capacitance to the ground
16	Standalone logic gate with a single spring
17-20	Shrunken device (variations) – halved number of fingers in input, output and fixed comb, halved spring constant
21	Cascade of 11 logic gates, pad pitch 230 µm
22	Standalone logic gate with the output directly connected to the pad
23	Cascade of 4 logic gates, pad pitch 230 µm
24	NAND gates: a) A and B in series, asymmetric u_{0Q}; b) A and B parallel, asymmetric u_{0Q}; c) A and B in series, asymmetric N_{A}

Table 3.5: List of all the test structures - V2.

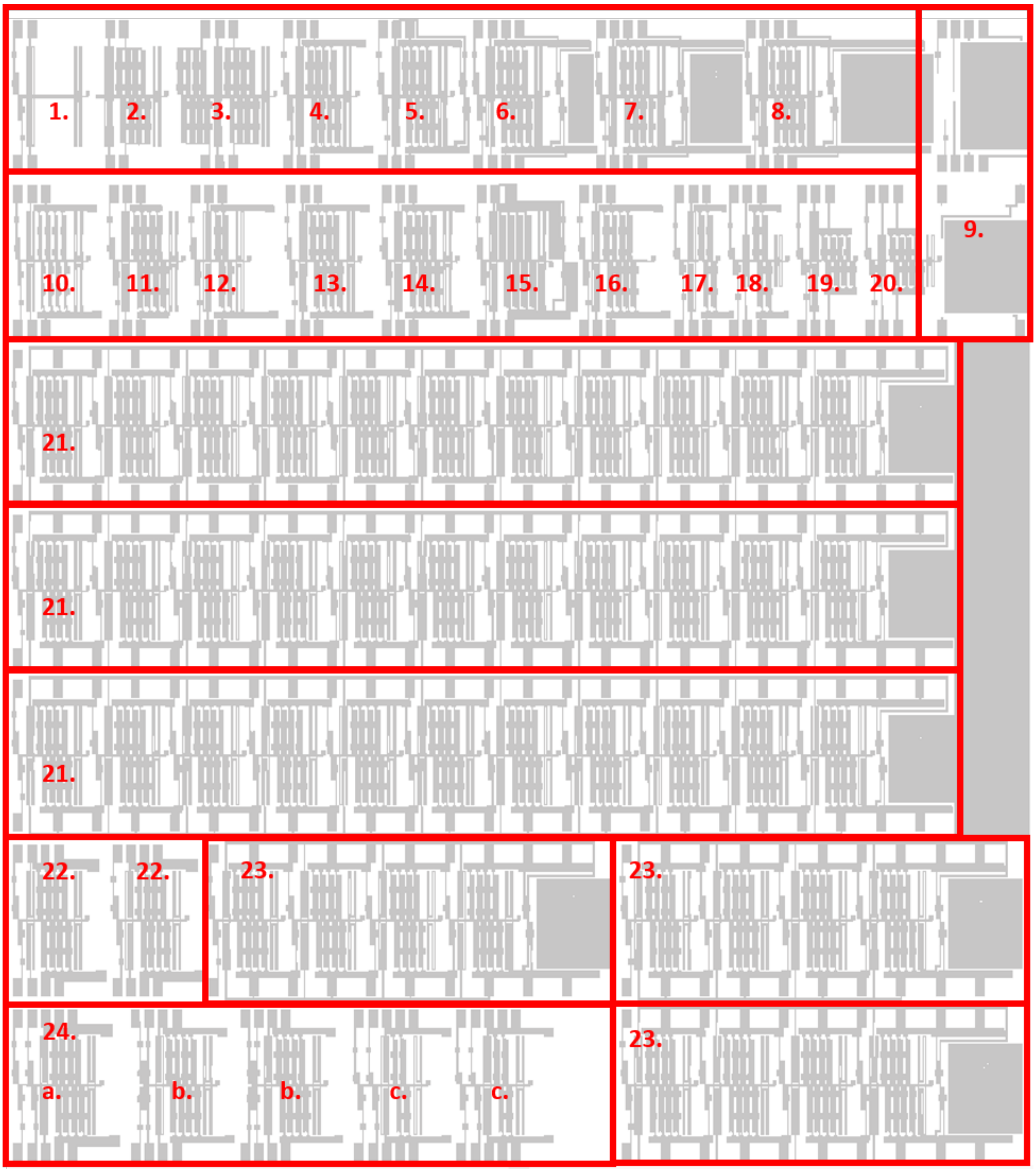


Figure 3.25: The second iteration of the microfabrication mask containing test structured with improved geometry, as well as NAND gates and cascades of inverter gates.

Figure 3.26 presents an SEM image depicting the top view of the initial three inverter logic gates within an 11-gate cascade. These micrographs were captured following 110 s of etching. Prior to etching, the devices underwent exposure at 640 mJ cm^{-2} and with a focus at -0.3 µm.

Figure 3.27 provides a closer view of both the input stage (a) and fixed capacitors (b), as captured through SEM imaging. Notably, the comb fingers exhibit clear definition in both scenarios, whether there is no overlap or a significant one.

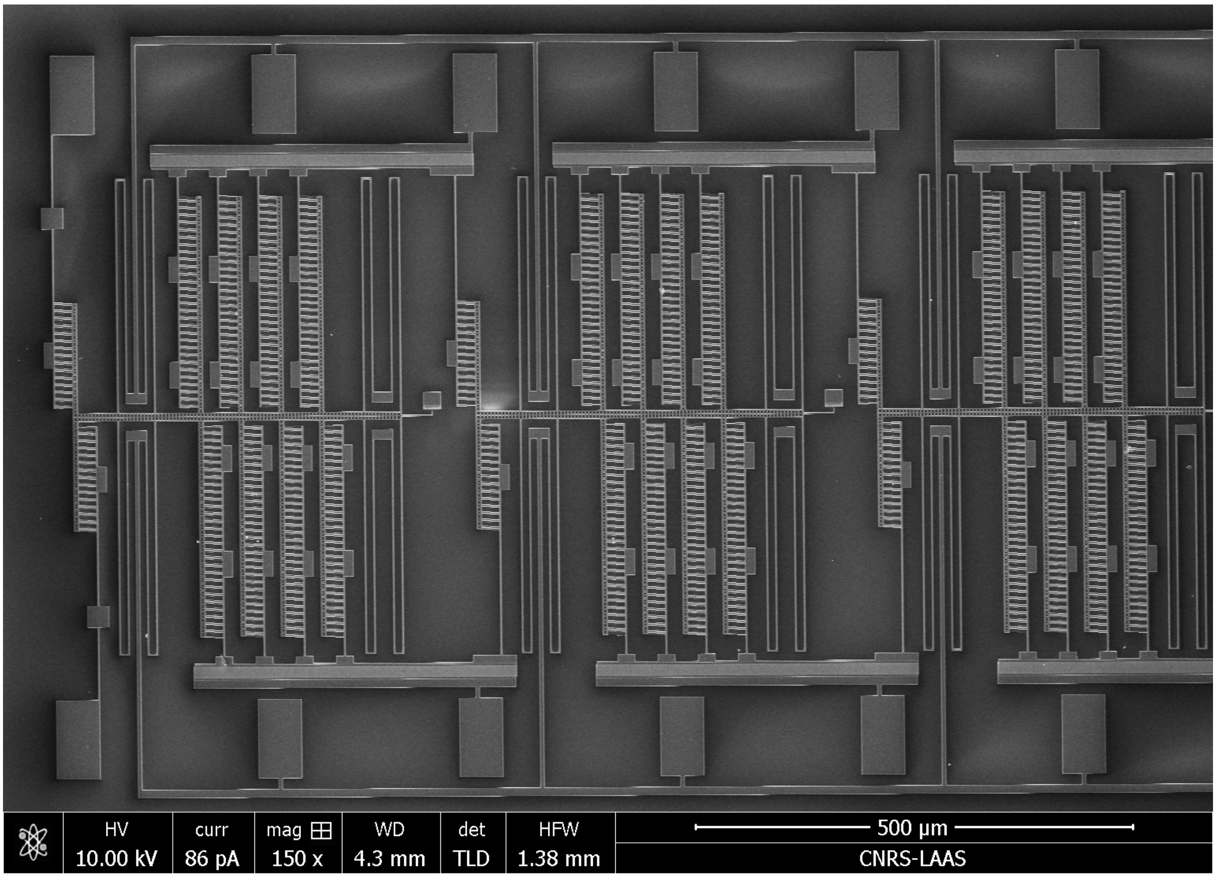
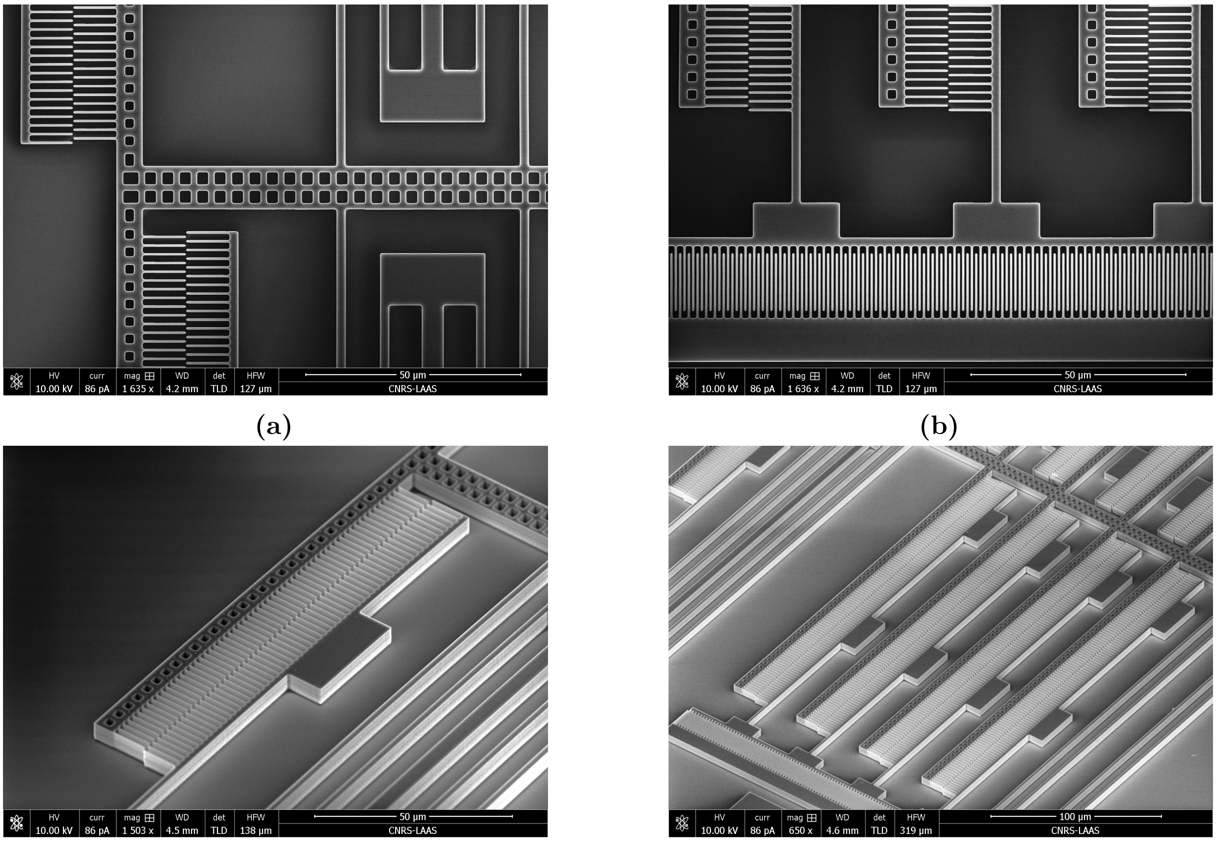


Figure 3.26: SEM micrograph of the first three logic gates in a 11-gate cascade.

Sub-figures 3.27 (c) and (d) display an angled perspective of the input comb-pair $\bar{A}$ and output comb-pair $\bar{Q}$, respectively. Etching is conducted throughout the entire top silicon layer, which measures 5 µm in thickness, thereby reaching the buried oxide layer.

Overall, in terms of realized dimensions after photolithography, the underetching compensations had different impact on the widths of fingers between variable and fixed combs. Smaller openings present in C_{fix} caused lower reduction in the finger width than the larger openings in variable capacitors. This difference in width was in a range of $10 - 30$ nm for $d_{\text{comp}} = 40$ nm, $30 - 45$ nm for $d_{\text{comp}} = 80$ nm and $70 - 110$ nm for $d_{\text{comp}} = 120$ nm and 160 nm.

Figure 3.28 illustrates the devices following the final fabrication step, which involves release in buffered hydrofluoric acid. The SEM micrographs provide a closer view of the spring anchor, fixed combs at the input stage, and the shuttle. In the micrograph depicting the spring anchor, slight underetching of the oxide layer is evident due to the isotropic nature of the etching process. Nevertheless, the anchor's size is sufficiently large to ensure fixation. Additionally, complete liberation of the combs and shuttle is observed, with minor remnants of the oxide present on the substrate, posing no obstruction to device functionality.



(a) **(b)**

(c) **(d)**

Figure 3.27: SEM micrographs of the top view of input stage and a spring (a) and fixed capacitor (b), as well as the tilted view (45 deg) of the input comb-pair $\bar{A}$ (c) and output comb-pair $\bar{Q}$ (d) after etching.

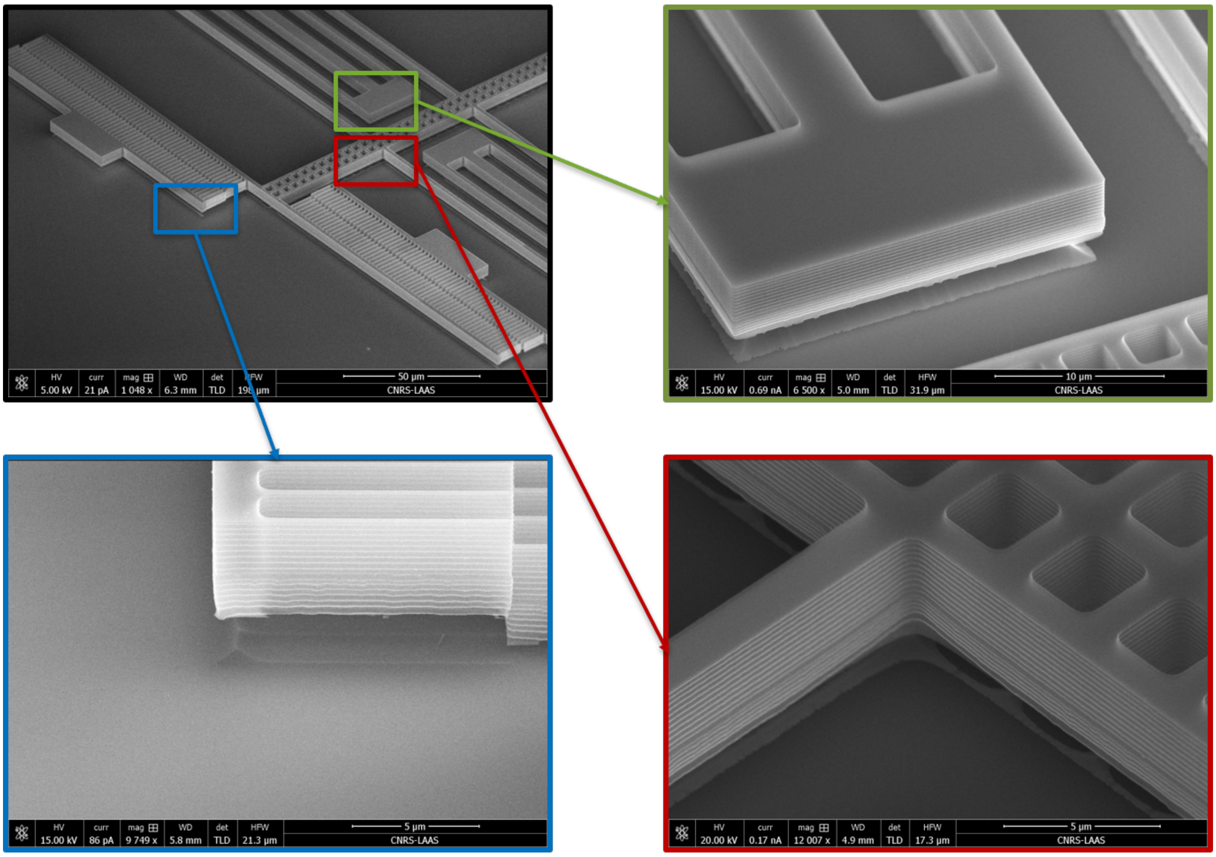


Figure 3.28: SEM micrographs of the device released in buffered HF with the zoom on the anchor of the spring, the input comb and the shuttle.

3.8 Conclusion

In conclusion, this chapter has provided a comprehensive overview of the design stages of a MEMS-based inverter gate. Building upon the foundational concepts introduced in the previous chapter, the individual components of the inverter gate were designed using analytic and FEM methods. Moreover, the implementations of a NAND gate were proposed.

The initial microfabrication tests were performed on silicon wafers, allowing us to identify the most optimal fabrication conditions, which for the photolithography step correspond to exposure dose within the span of $620 - 680\ \mathrm{mJ\,cm^{-2}}$ and focus offset of $0.3\ \mu\mathrm{m} - 0.4\ \mu\mathrm{m}$. Pattern transfer into silicon was performed using Bosch process. These tests also yielded information about the change of component dimensions due to underetching which was further taken into account when designing the microfabrication mask. Different underetching compensations, ranging from 40 to 240 nm were tested, which resulted in different outcomes for fixed and variable capacitors. The change of dimensions was more prominent in the case of variable capacitors, as the distance between vertical surfaces of the neighboring structures is 1.5 µm, compared to fixed capacitors with 0.5 µm openings. The underetching compensation of $d_{\mathrm{comp}} = 40$ nm still yielded structures with reduced dimensions, while the structures with $d_{\mathrm{comp}} \geq 120$ nm couldn't provide well defined fixed capacitors without overexposing finger tips within the variable capacitors. The $d_{\mathrm{comp}} = 80$ nm provided the best compromise between the design and realized dimensions and was used for fabrication of the devices that underwent characterization that will be presented in the following chapter.

4 Characterization

This chapter covers the experiments performed on the test structures, including fixed capacitors, individual inverter gates, cascade of the devices, as well as the NAND logic gates. At the beginning, I will introduce the setups and methodology, following with the measurement results and discussion. Experimental results will be compared with the previously developed models.

4.1 Equipment, characterization methods and tools

4.1.1 Experiment stations and environments

Characterization of the devices was performed on two test stations.

Capacitance measurement was performed on Signatone Checkmate 200mm high precision manual probe station using Keysight 4294A Impedance Analyzer. As any change in the instrument's operating conditions, such as ambient temperature or humidity can have significant effect on measurement accuracy, the tool was calibrated in reference to an "open" standard termination. Compensation (correction) was also performed, likewise in an "open" setting.

Sample was heated to 60°C as a precaution to reduce the water layer adsorbed on the sample surface in the air environment. Potential issue of leakage of the charges from the capacitors is therefore prevented. Impedance was measured versus frequency between 10 kHz and 1 MHz with the amplitude of the oscillator set at $V_{\mathrm{AC}} = 1$ V. Capacitance values were fitted with an Rs-Cs model (Figure 4.1).

The dynamic actuation of the devices was performed on Karl SUSS PA200 Semiautomatic Probe System. During the dynamic actuation, custom-made multi-contact DC probes with flat-tip needles have been used. These FormFactor™multiprobes feature tungsten ceramic needles for low noise, high temperature stability and high performance. For the purpose of the project, two types of multiprobes were designed, featuring four tips

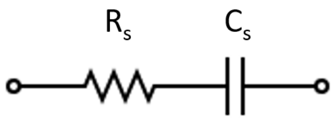
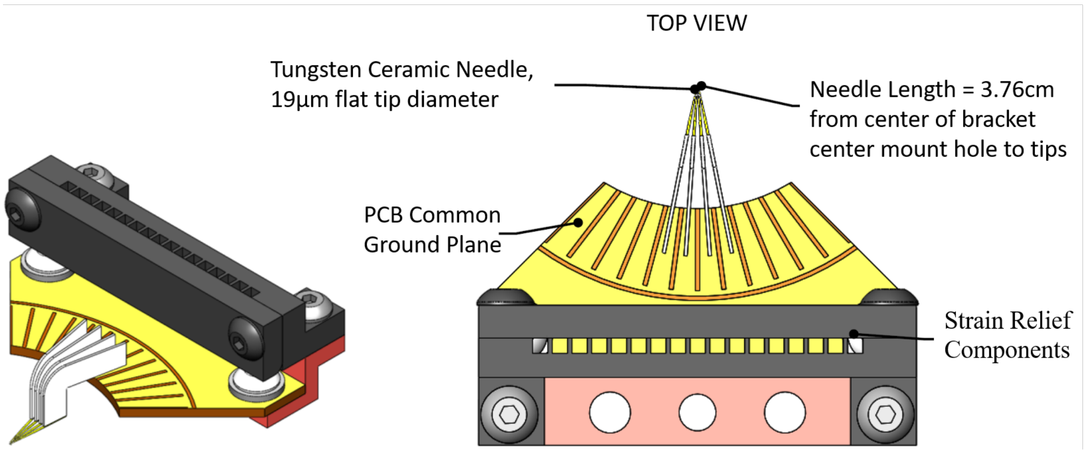
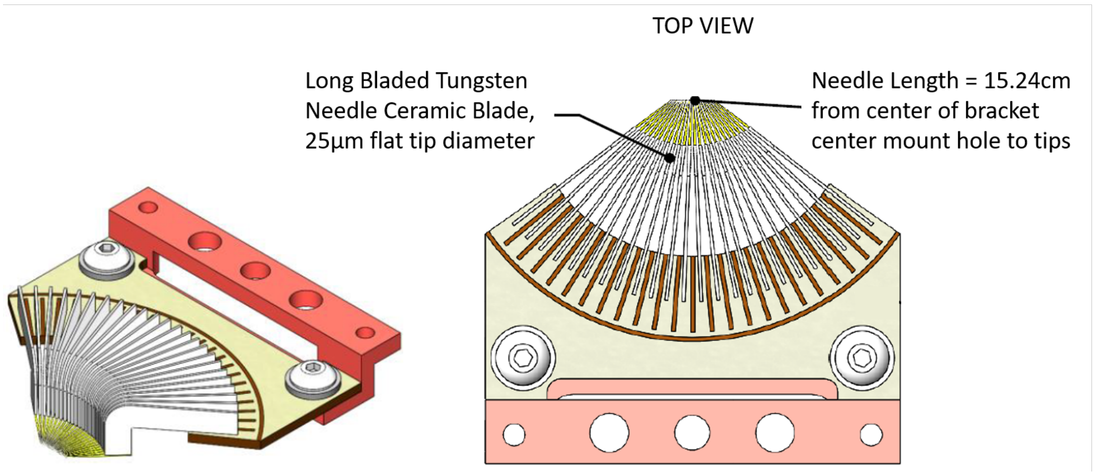


Figure 4.1: Lumped model consisting of resistor and capacitor connected in series, representing the real and imaginary components of total equivalent circuit impedance.

(Figure 4.2a) and eighteen tips (Figure 4.2b) in a multiprobe. In the 4-tip design the probe pitch is constant and equals to 80 µm. These multiprobes are used for characterization of individual devices. In the 18-tip multiprobe the probe pitch is not constant. The probe spacing equals either to 230 µm or to 460 µm. These larger multiprobes are used for actuation of the cascade of the devices.



(a) Side and top view of a FormFactor probe containing 4 tips with 80 µm spacing.



(b) Side and top view of a FormFactor probe containing 18 tips with probe spacing varying between 230 µm and 460 µm.

Figure 4.2: FormFactor multiprobes with (a) 4 and (b) 18 tips.

As explained in the chapters 1 and 2, the MEMS based logic gates are compatible with adiabatic operating principle, meaning that the actuation signals are not abruptly applied, but rather gradually introduced. Transport of the state between consecutive devices is done in phases governed by power clock signals that are shifted for a quarter of a period between each two consecutive devices. Therefore, we have developed a circuit board that generates input (V_A, $V_{\bar{A}}$) and power-clock signals with modifiable frequency and amplitude, shown in Figure 4.3.

The PWM outputs of an Arduino are amplified using optocouplers. The signals are subsequently converted to analog signals using low-pass filters. The amplitude of the power clock signals can be varied between 15 V and 28 V, by varying the input voltage of the circuit board. The input voltages V_A, $V_{\bar{A}}$ can be varied from 0 up to power clock voltage using variable resistors. Maximum achievable frequency is 1 Hz.

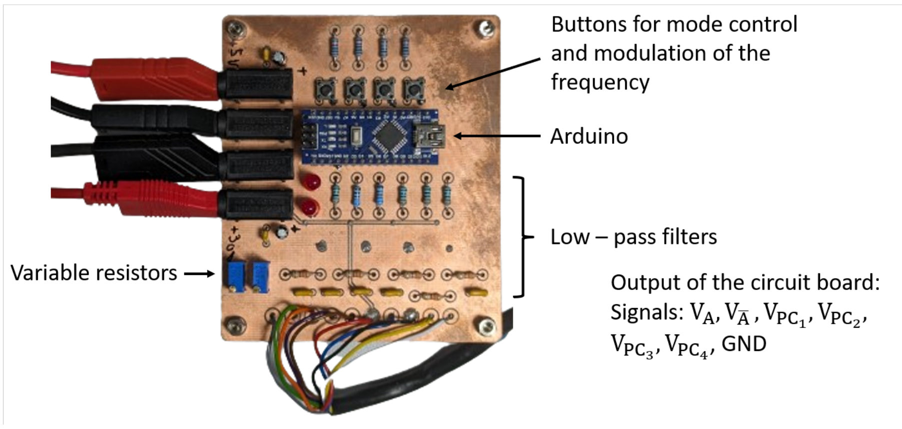


Figure 4.3: Circuit board developed to generate trapezoidal voltage signals with modifiable frequency and amplitude and with a corresponding period shift.

4.1.2 Image acquisition and processing

The frames recorded by the XIMEA xiQ camera (model MQ013-E2) were captured at the maximum frame rate of 60 fps, through 20x Mitutoyo Plan Apo SL Infinity Corrected Objective and with an additional manual zoom. The pixel resolution of the camera is 1280 × 1024 with a pixel size being 5.3 µm. The actual recording magnification was determined using calibration patterns, shown in Figure 4.4. The pattern has a format of a ruler, with the largest lines having a pitch of 0.1 mm and the smallest ones having the pitch of 10 µm.

By focusing the 20x objective on the smallest pattern and adding the maximal manual zoom, the pattern was recorded as represented in Figure 4.5a. The gray value was extracted along the yellow stripe and the profile was plotted against the distance expressed in pixels (Figure 4.5b). The width of the stripe was increased from one pixel line to 50, resulting in an intensity profile that is averaged along those 50 adjacent pixel lines, consequently reducing the measurement noise. The distance between the two furthest peaks in the gray value graph equals 1170 pixels and corresponds to a distance of 150 µm. This means that at the recording magnification and with the given resolution of the camera, 1 µm on the

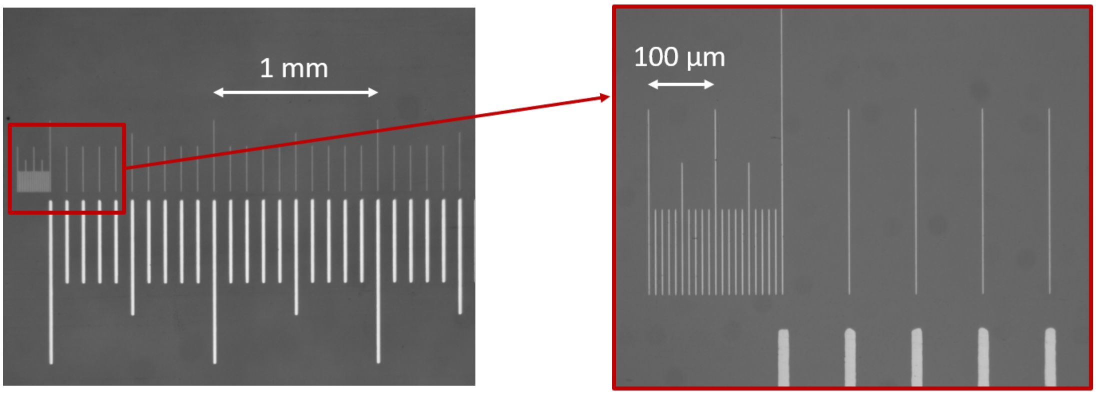
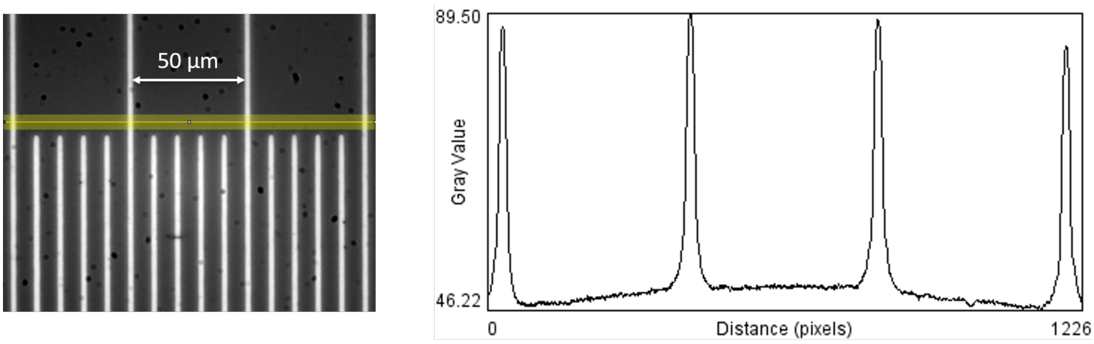


Figure 4.4: Calibration pattern used for determination of the magnification and calibration of the pixel size for image processing and displacement extraction. The thickest lines have a pitch of 0.1 mm, whereas the narrowest ones have the pitch of 10 µm.

device corresponds to 7.8 pixels on the image (1 pixel $\triangleq$ 0.128 µm), giving the actual magnification of $5.3 \times 7.8 \approx 41$x.



(a) (b)

Figure 4.5: (a) Calibration pattern used for calculation of the magnification with yellow stripe showing the direction along which the intensity profile, shown in (b), was extracted and plotted against the distance expressed in the number of pixels.

This information was essential during the image processing step, performed on the recorded frames in order to extract the displacement magnitude during the actuation of the devices. The area within the image (i.e. part of the device) that was chosen for monitoring the displacement covers the arm of a spring, as well as its anchor as the reference (non-movable) point, as depicted by a yellow rectangle in the Figure 4.6. The thin yellow line within this rectangle represents a line along which the gray level of the recorded images is extracted. The width of this window of interest determines the number of pixel lines for which the gray level will be averaged and was set to 78 pixels during all of the measurements, as that value corresponds to the width of the spring's anchor (10 µm). For each image frame, a list of gray values was extracted and plotted with respect to a position within the observed window of interest. As shown in the image 4.6 on the right, the local minimums and maximums within the gray value profile indicate the position of the edges and surfaces of the arm of the spring and the anchor.

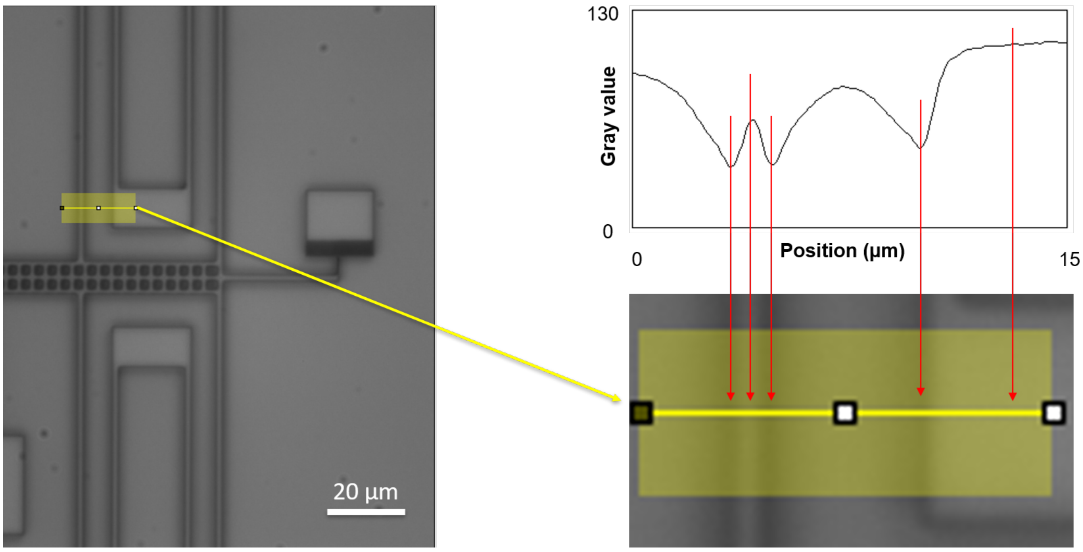


Figure 4.6: On the left side of the figure, area of interest for the measurement of the displacement magnitude is indicated with a yellow stripe. Extraction of the intensity profile is performed along this yellow line whose width is set to 78 pixels. On the right, the local minimums and maximums within the gray value profile indicate the position of the edges and surfaces of the arm of the spring and the anchor.

By tracking the change of the position of the arm of the spring (Δx) with respect to the anchor, we can determine the displacement magnitude induced during the actuation of the device. As an example, Figure 4.7 shows gray value profiles extracted from the recorded frames during the actuation of the device by applying a trapezoidal signal of an amplitude of 20 V to the input electrode A while grounding the rest of the device. The upper graph corresponds to the resting position (applied voltage is 0 V), while the lower one corresponds to the maximum displacement at the reached $V_A = 20$ V.

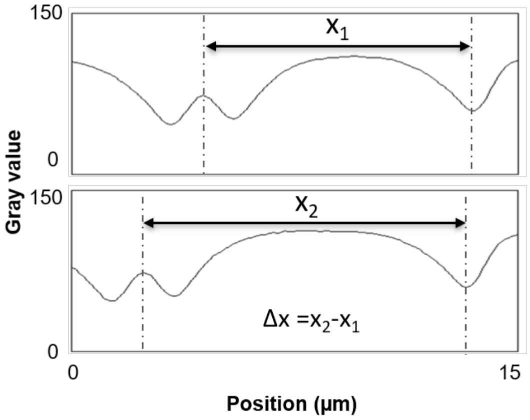


Figure 4.7: Displacement measurement by peak tracking. The two graphs correspond to the gray value extracted from optical images of the device in the resting position (top) and at the maximum displacement during device actuation with 20 V (bottom). The local maximum and minimum correspond to the position of the arm of the spring and edge of the anchor, respectively. By tracking the change of their distance, we can determine the amplitude of the device's displacement during actuation.

In order to reduce the noise on the position curve, the gray-level-data is first smoothed using a moving average filter with a span of five data points, reducing the noise by a factor of $\sqrt{5} = 2.24$. The first local maximum in the intensity profile is then identified (see Figure 4.6 top right) corresponding to the movable arm in the suspension. The 7 points around this local maximum are fitted with the second order polynomial function (Figure 4.8). The maximum of this fitted function is taken as a tracking point for the position of the beam. The same procedure is followed for the local minimum corresponding to the edge of the anchor. When looking at two different recorded frames, we can measure the magnitude of the beam movement by measuring the change of the position between the tracking points (local maximums) with respect to fixed anchor (local minimum) in the intensity profiles.

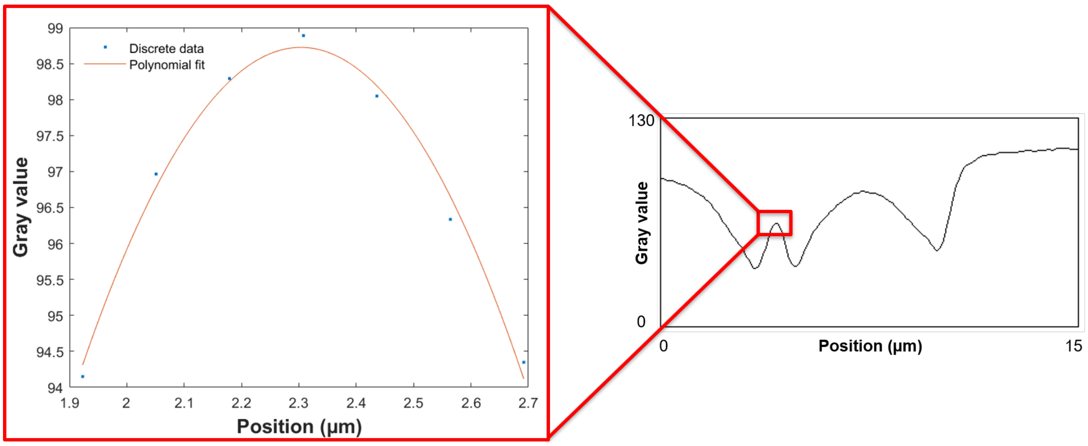


Figure 4.8: Polynomial fitting of the 7 data points around the local maximum with the second order polynomial function.

Plotting the change of the beam's position over all the recorded frames yields a beam displacement profile as shown in Figure 4.9b. A block diagram of the data processing method, as well as the corresponding MATLAB code are available in Appendix B.

The displacement of the beam, that is, the distance between the resting position and the one achieved when the voltage is applied, corresponds to the difference between the maximum and the minimum values within the position profile. As the applied voltage has trapezoidal shape and during the length corresponding to a quarter of a period the signal has constant value (corresponding either to V_{dd} of 0, see Figure 4.9b), the position during those period phases reaches a plateau. By averaging the position at those plateaus, the measurement noise was further decreased. The number of data points (frames) across which the averaging was made is 30, corresponding to gray and blue rectangles in Figure 4.9b. As peak to peak value of the noise at a displacement plateau measures to about ≈ 25 nm, this additional averaging over 30 data frames ensures the noise reduction by a factor of $\sqrt{30} \approx 5.5$ [1] and presumably yields measurement resolution of less than 10 nm.

It is important to mention that the image acquisition is affected by the ambient conditions and is impacted by the external vibration of the environment. At higher

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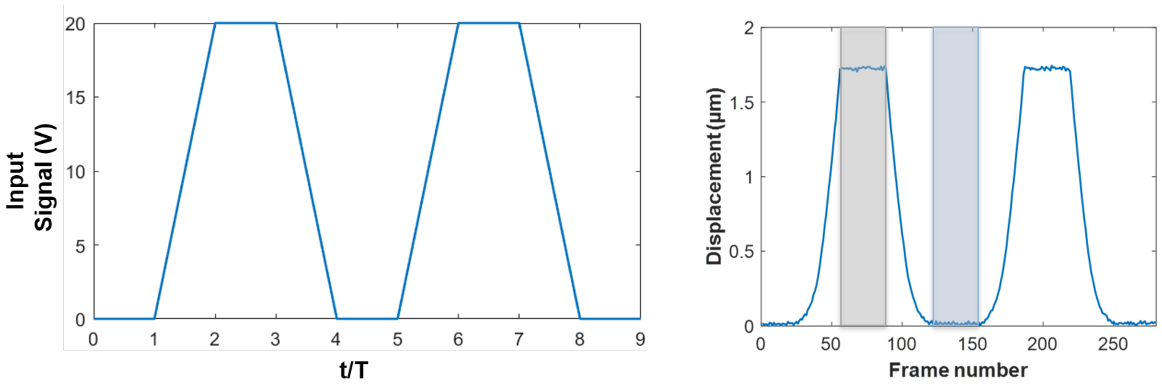
[1] Considering N uncorrelated measurements of the same value, with an added Gaussian noise, averaging those measurements leads to an enhancement of the resolution by a factor $\sqrt{N}$.



(a) Trapezoidal signal with the amplitude $V_{dd} = 20$ V and period $T = 2$ s applied to the input electrode A.

(b) Displacement extraction from the position of the spring arm.

Figure 4.9: Trapezoidal signal (a) is applied to the input electrode A, while the rest of the device is grounded. The induced displacement is calculated as the difference between the maximum and minimum values in the position profile (b), with the resting position taken as 0. Both of these values are obtained after averaging over windows with 30 data points, corresponding to gray and blue rectangles. Averaging windows correspond to constant actuation voltages and therefore plateaued displacements. Averaging at these steady states reduces noise by $\sqrt{30} \approx 5.5$.

temperatures ($\geq 60°$C) the air above the sample's surface becomes visibly less dense, changing its refractive index and resulting in significant shifting of the images with some of them appearing blurry.

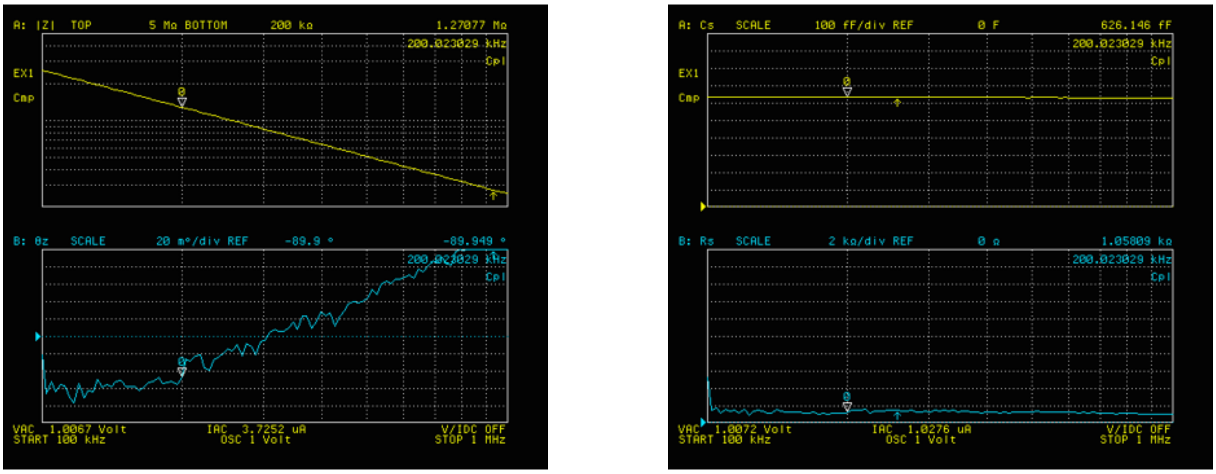
The *differential* measurement of the beam position, that is, the position relative to the anchor, circumvents the error due to vibrations and image shifting due to refracting index change.

4.2 Measurements of the capacitance of the comb-structures

These measurements were performed on the test structures #28 (Figure 3.17) which are designed as interdigitated comb capacitors, featuring 400 fingers with the finger width of $d = 0.5$ µm, length of $l = 15$ µm and thickness of $h = 5$ µm. Both combs are fixed through 10 µm wide anchors and are connected to 50×90 µm^2 contact pads. The devices have undergone wet etching in buffered HF, meaning that there is no SiO_2 underneath the comb-fingers, but the oxide is present below the supporting beams and contact pads. 36 fixed capacitors are at disposal, with varying finger overlap from -13 µm to 13.5 µm. In the area of the *gray zone*, (between -2 µm to 2 µm) the overlap variation is done in smaller 0.25 µm steps, while outside of it the steps of 1 µm were made.

The measurement data was acquired with the impedance meter, as previously explained in 4.1. Samples were heated at 60°C to remove humidity from the surface of the devices.

The chuck of the probe-station and therefore the substrate below the devices were grounded through the impedance analyzer . An example of an impedance measurement on a device with the finger overlap of 10 µm is shown in Figure 4.10. Impedance and phase are measured over the frequency range spanning between 10 kHz and 1 MHz, with oscillator amplitude set at $V_{AC} = 1$ V. The data is subsequently fitted with an Rs-Cs model.



(a) Impedance and phase measurement over the 10 kHz – 1 MHz frequency range.

(b) Impedance fitting with an Rs-Cs model, capacitance is taken at 200 kHz.

Figure 4.10: An example of a measurement of an impedance of a device with the finger overlap of 10 µm. Impedance and phase (a) are measured over the 10 kHz – 1 MHz, frequency span, with $V_{AC} = 1$ V. The data is subsequently fitted with an Rs-Cs model (b) and the capacitance value is extracted at 200 kHz.

Capacitance values were extracted at 200 kHz and were rounded to a fF. The precision chart of the used equipment (Agilent 4294A) indicated a measurement precision of 5 fF for the present measurement conditions. When looking at the fitted capacitance value (Figure 4.10b) we can see that over the whole 10 kHz – 1 MHz frequency range the capacitance value stays constant within ±1 fF. Therefore we can deduce a measurement error of ±6 fF.

The lowest observed value of Rs was 500 Ω, giving a value of the contact resistance of about 250 Ω. Figure 4.11 shows the extracted Cs values (blue dots) for each of the overlap values within the range between −13 µm and 13.5 µm. Represented in the same plot with the full red line is the FEM simulated capacitance for the same geometry. The simulated values were reduced for the value of 32.4 fF, corresponding to the parasitic contribution from the substrate.

For the negative overlaps the measurement values are quite close to the simulated ones ($\approx$ 15 fF difference). In the linear capacitance region the FEM model gives a capacitance slope of ≈ 76.9 fF µm^{-1}, while the measurements give a slope of ≈ 62 fF µm^{-1}.

As the capacitance in the linear region corresponds to:

$$C = 2N\varepsilon_0 \frac{hu}{g} \tag{4.1}$$

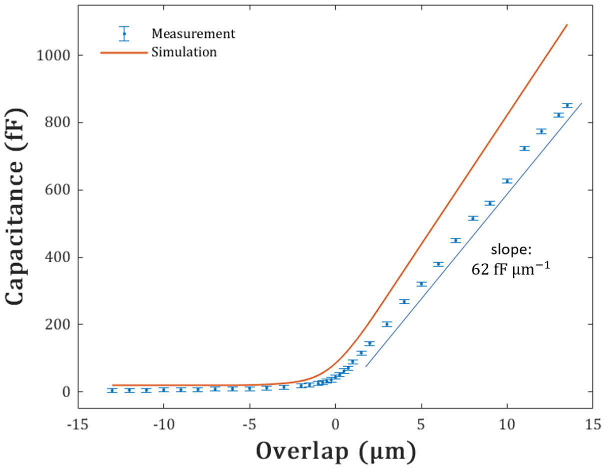


Figure 4.11: Cs values (blue dots) extracted from impedance measurements, versus the overlap of the fingers. The full red line shows the corresponding FEM-simulated capacitance, without the parasitic contribution of the substrate.

with h being the device thickness, u the finger overlap and g the gap between the fingers, we can deduce the slope to follow the $2N\varepsilon_0\frac{h}{g}$ behavior. The slope difference can be explained by the reduction of the width of the fingers d due to underetching. The real value of the gap can then be calculated from the slope values of the FEM simulation and the measurement, knowing that the $d_{\text{FEM}} = g_{\text{FEM}} = 0.5$ µm, yielding:

$$\frac{76.9}{62} = \frac{g_{\text{real}}}{g_{\text{FEM}}} \quad \Rightarrow \quad g_{\text{real}} = 0.62\ \mu\text{m} \tag{4.2}$$

This gives the real value of the finger width of $d = 380$ nm, and the underetching value of 60 nm (total width reduction of 120 nm), despite the underetching compensation introduced in 3.3.1.

The aim of this thesis is to develop MEMS logic gates, where distinguishing between two logic states is reliant on sufficient displacement of the comb structures in both directions. Within the region where the fingers of the combs overlap, the electrostatic force generated between the comb-pairs, which drives their movement, is directly proportional to the rate of change of capacitance (slope) and the square of the applied voltage V^2. Since the measured capacitance deviates from the predicted values obtained from simulations, achieving the same force as modeled can be accomplished by increasing the applied voltage by a factor of $\sqrt{\frac{76.9}{62}} = 1.11$. This adjustment assumes that the spring constant k remains unaffected by any dimensional changes. However, the suspension beams are indeed impacted by underetching, leading to a reduction in their spring constant k. Consequently, this counteracts the need for increasing voltage (and force) to achieve the simulated displacement values. Further elaboration on this matter will be provided in the subsequent section when measuring the displacement of movable combs induced by applied voltage.

4.3 Inverter (NOT) gate

In the chapter 2 the architecture of the MEMS inverter gates was introduced as well as the FEM and analytic models that describe their behavior and allow us to anticipate the response (movement) of the gate to the applied DC signal. The simulation of the inverter gate operation in four phases was also shown. In the following section, the experimental validation of those simulations will be presented, as well as performance at elevated temperatures.

4.3.1 Electrical actuation of the gates

The goal of these experiments was to compare the observed displacement magnitude of the movable electrodes when subjected to a DC voltage and to compare these values to the two previously introduced models.

The measurements were performed on the devices with comb-drive actuators exhibiting three different initial overlaps $u_0 = -2d$, 0 and $2d$, d being the finger width. In these three configurations the initial (resting) states fall within the gray zone. Studying these overlap variations can give us information about the effect of the gray zone on the device behavior, as well as give us the information about the sensibility of the operating behavior regarding variations of device dimensions (with respect to design) due to microfabrication process.

The measured values were compared to the expected equilibrium positions calculated from the potential energy, as described previously.

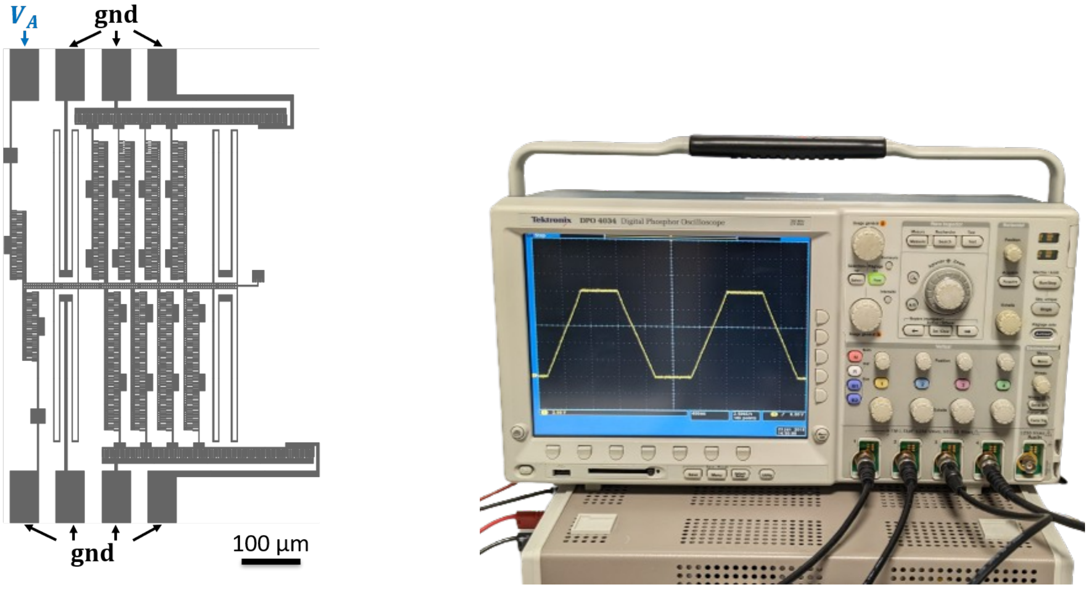
Experimental setup

Devices were actuated on a probe station by applying a trapezoidal signal on terminal A, whilst grounding $\bar{A}$ and all the other device's components. The substrate was also grounded through the chuck of the test station. Figure 4.12 shows the connection of the pads as well as the snapshot of the oscilloscope showcasing the corresponding signals.

The displacement x of the movable part was measured at equilibrium in response to the applied voltage V, which was increased in 0.5 V steps. The corresponding displacement of the shuttle was optically recorded using an optical camera (XIMEA xiQ, model MQ013-E2), as presented in Figure 4.13.

Voltage-induced displacement

The measured displacements for three different device configurations ($u_0 = -2d$, 0 and $2d$) are shown in Figure 4.14 (right), where the values are represented with circles in the graphs. The measurements are plotted alongside the simulated values (represented in solid lines), that were derived from the FEM capacitance data, introduced in chapter 2. This

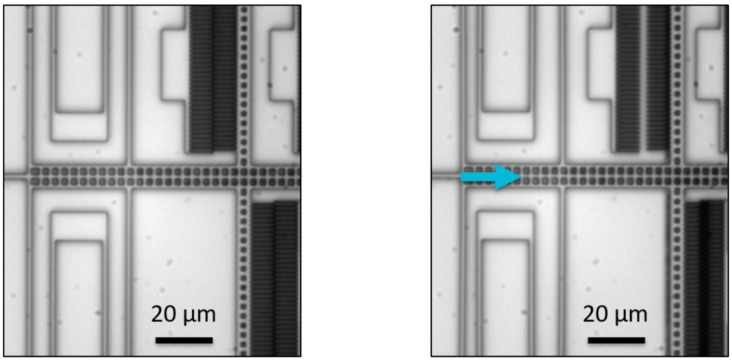


p

(a)

(b)

Figure 4.12: a) Connection of the active electrode A of the complementary input combs to signal V_A while grounding the remaining components of the device. b) Oscilloscope showing an example of the applied signal V_A with an amplitude of 10 V and a frequency of 0.5 Hz.



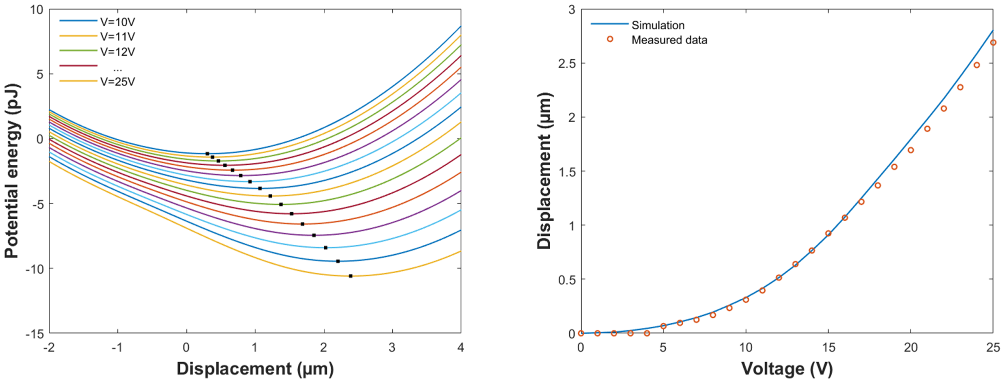
Resting state

Logic state

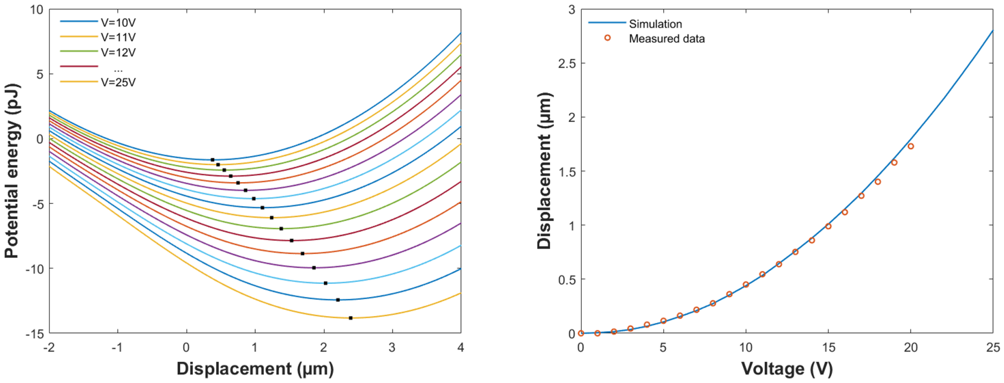
Figure 4.13: Logic state encoding in a comb displacement. Left: relaxed position. Right: logic state.

derivation of the expected displacement values comes from the potential energy curves, that were plotted for each value of the applied voltage across the whole displacement spectrum (Figure 4.14 left). The minimums of the potential curves for each voltage value correspond to the equilibrium positions, which are taken as movement magnitudes.

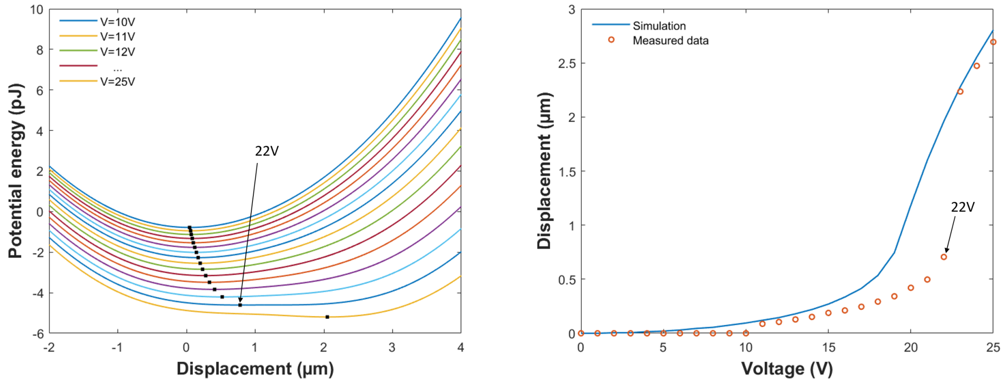
For zero and positive initial overlaps u_0, Figure 4.14a and b reveal a very good agreement between measurements and simulations. At first order, the displacement x versus the applied voltage V follows the expected quadratic trend typical of a conventional comb-drive actuator configuration. On the other hand, Figure 4.14c illustrates that for the negative initial overlap ($u_0 = -2d$), the measurement exhibits a steep increase as the



(a) Zero initial overlap



(b) $+2d$ initial overlap



(c) $-2d$ initial overlap

Figure 4.14: Left: Potential energy curves for different values of applied voltages with black dots indicating the curve minimums (equilibrium positions) for three different comb-drive configurations: (a) initial comb-overlap of 0, (b) $2d$, and (c) -$2d$. Right: Comparison of the simulated (full line) and measured (circles) comb-displacement induced by applying a DC voltage on the fixed electrode, the movable electrode and the substrate being grounded for the same three configurations.

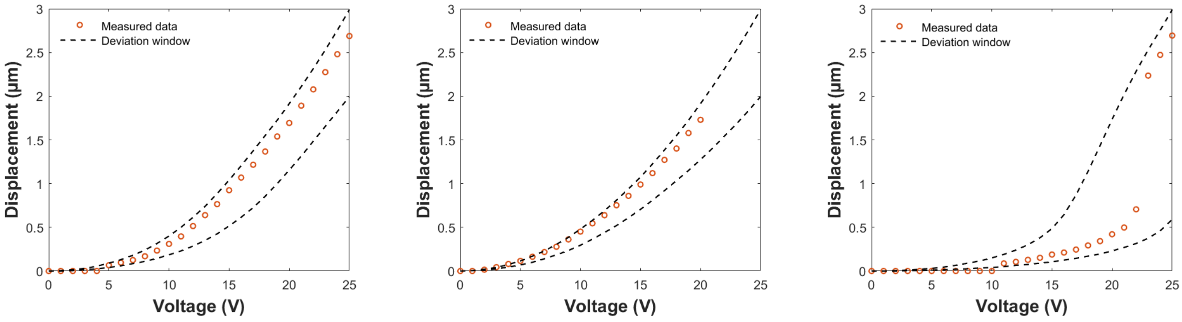
displacement x exceeds 0.5 µm. Although the calculated displacement (solid line) also displays this steep increase, it is shifted in voltage compared to the experimental data.

As previously shown in the section 2.3.3 the device behavior is highly sensitive to geometrical variations. Therefore, in order to understand and explain this shift in voltage concerning the structures with $u_0 = -2d$ initial overlap, we compared the measurements with the FEM calculations of the capacitance that included slight variations of the structure's dimensions. These variations account for changes in dimensions resulting from the fabrication process during lithography and etching steps and affect in particular the length l of the fingers and the width of the suspension beams (that spring constant k is highly dependent on). In the previous chapter (3.2.2) we have shown that the underetching amounts to about $\sim$ 60 nm. Taking this value as the variation of the width of the spring beams (corresponding to $\approx \pm 6\%$ change, which results in the change of the spring constant of about $\pm 20\%$), as well as a change of finger length l ($\approx \pm 1.2\%$), we can simulate the possible displacement range whose borders are represented by dashed lines in Figure 4.15. Notably, for the negative initial overlap in Figure 4.15c, the displacement-voltage characteristics are highly sensitive to these parameters. A change of less than 1.2% in the finger length and 20% in the spring constant is sufficient to align the simulation with the experimental data.

An interesting insight emerges from the potential energy curve of Figure 4.14c, where the potential energy E_p versus displacement x at the actuation voltage $V = 22$ V, corresponding to the voltage right before the steep increase in displacement, is pointed out. It highlights that the potential energy at $V = 22$ V remains rather flat over a span exceeding 1 µm. With a small voltage increase ($V = 23$ V), the minimum of the potential energy curve shifts for more than 1 µm. As the shape of the potential energy curve depends on the geometrical parameters governing the force balance of the comb-drive actuator, the displacement itself is extremely sensitive to those parameters as well. This observation also indicates that within this operation range, variations in the stored electrical and mechanical energies of the system offset each other, meaning that the electrostatic force gradient counterbalances the mechanical spring constant. This behavior is linked to the well-known electrostatic spring softening effect, resulting in the present case to a comb-drive actuator with a reduced apparent stiffness in the restricted region of the *gray zone*.

This could pave the way for actuators operating within the gray zone with an enhanced displacement-versus-voltage ratio and for force sensors with heightened sensitivity. In MEMS capacitive sensors, sensitivity is proportional to variation of capacitance caused by the displacement. In the case of a force sensor (e.g. an accelerometer), the displacement is caused by external forces acting on the mobile part of the sensor (e.g. the inertial force), meaning that the lower its stiffness, the larger the displacement, the greater the sensor sensitivity. In other words, the sensitivity of a force sensor is inversely proportional to its stiffness. As discussed previously, operation within the gray zone may significantly reduce apparent stiffness when the electrostatic spring constant counterbalances the mechanical spring constant of the comb-structure. Thus, we envision that a force sensor made of a comb-structure with negative initial overlap and adequately operated in the gray zone would experience significantly greater displacement for a given external force to sense. This would lead to enhanced sensitivity compared to an operation with engaged comb fingers.

This effect is also observable in Fig. 4.16, where the displacement gradient over voltage



(a) Zero initial overlap **(b)** $+2d$ initial overlap **(c)** $-2d$ initial overlap

Figure 4.15: Introducing parameter variation into simulation of the induced displacement versus the applied voltage for the cases of (a) zero, (b) $+2d$ and (c) $-2d$ initial overlaps. The dashed lines correspond to the ±1.2% variation of finger length and ±20% in spring constant.

is plotted for the three configurations. In case of initial overlap of -2d, the displacement gradient follows a steep increase within this region and reduces once outside of the *gray zone.*

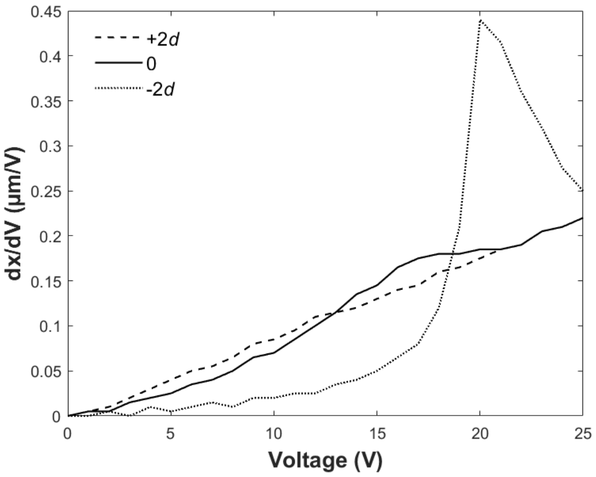


Figure 4.16: Derivative of displacement over voltage for three different initial overlaps, highlighting the highest sensitivity of the -2d geometry.

Further investigations involved the actuation of the device with forward and backward voltage sweeps at 60°C. Actuation of the devices was performed withing the voltage range of 19 V – 24.5 V. The corresponding displacements are shown in Figure 4.17, with the blue line corresponding to the upward voltage sweep and the red line to the downward one. The two curves reveal no hysteresis effect associated with the actuator displacement, showing that there are no associated energy losses.

This interesting behavior with the heightened displacement-to-voltage sensitivity within the narrow region of the *gray zone* could pave the way for actuators operating with amplified displacement-versus-voltage ratio and sensors with increased responsiveness. The narrow operating window of enhanced sensitivity would however be highly position-

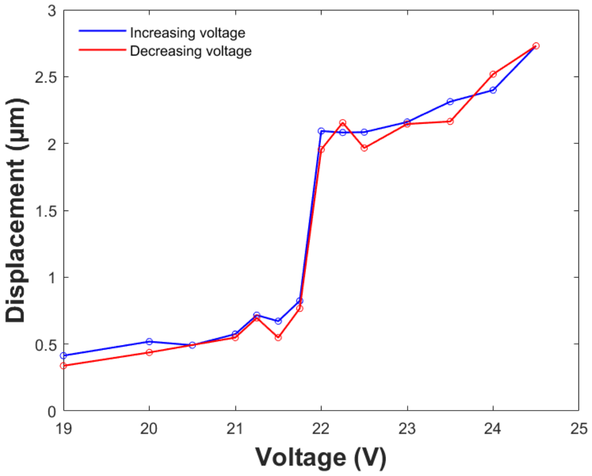


Figure 4.17: Actuation of the devices with $-2d$ initial overlap by increasing the voltage from 19 V to 24.5 V (blue line), followed by the decrease to 19 V (red line).

and geometry-sensitive, with low tolerance for fabrication irregularities.

4.3.2 Four-phase operation of the inverter gate

Full operation of an adiabatic inverter gate is performed in four phases and requires two complementary input signals A and $\bar{A}$, as well as the power clock signal that is applied to the output stage over the fixed capacitors. This principle has been thoroughly explained in chapter 2.

As a reminder, in the **first phase** ($0 < t \leq T$, "set") signals A and $\bar{A}$ are introduced, with their level being slowly increased from 0 to V_{H} and V_{L} (or V_{L} and V_{H}), depending on the state being encoded. Depending on which signal is set at a *high* or *low* voltage level, the shuttle will displace the movable electrodes in a *positive* or *negative* x-direction and pre-encode the logic state.

In the **second phase** ($T < t \leq 2T$, "evaluate") the power-clock signal V_{PC} is applied via the capacitive bridge formed by the fixed capacitors C_{fix} and the equivalent capacitance of the nodes Q and $\bar{Q}$. The beam continues to move in the predefined direction. At the end of the phase ($t = 2T$) the output signals Q and $\bar{Q}$ are established at values V_{H} and V_{L} (or V_{L} and V_{H}) corresponding to an inverted input logic state.

In the **third phase** ($2T < t \leq 3T$, "maintenance/hold"), the input signals A and $\bar{A}$ are gradually lowered to ground. The preserving of the logic state is due to the output electrodes that are still polarized via V_{PC} which is maintained at its level.

In the **fourth phase** ($3T < t \leq 4T$, "recovery") the V_{PC} signal is gradually reduced, leading the position of the beam towards the center – the "resting" position which is reached at $t = 4T$.

In order to test the four-phase state encoding with the fabricated inverter gates, the devices with zero-initial-overlap were actuated on Karl SUSS PA200 Semiautomatic probe station. Complementary input signals A and $\bar{A}$ used for pre-actuation, as well as the power clock signal were generated with the circuit board introduced in 4.1.

An example of 4-phase operation with actuation signals $V_A = 10$ V, $V_{\bar{A}} = 4$ V and $V_{\mathrm{PC}} = 24$ V is presented in Figure 4.18. The top graph shows the complementary input signals (the blue line corresponding to signal A and the red one to $\bar{A}$). The second one shows the power-clock signal, introduced with a delay of $t = T$ with respect to the input signals. The third graph shows the optically measured displacement of the movable shuttle (blue) compared to the simulated one (purple). As shown in the displacement graph in the Figure 4.18, the pre-actuation by signals A and $\bar{A}$ (of about 0.44 µm for the given set of input voltages) is demonstrated during the phase $0 < t \leq T$. In the subsequent phase ($T < t \leq 2T$), the displacement is drastically increased through PC signal. In the case presented, where the PC voltage is set at $V_{\mathrm{PC}} = 24$ V, the displacement is increased to 3.4 µm. We can also observe the maintenance of the state after removal of input signals ($2T < t \leq 3T$), with displacement being reduced by about 0.3 µm. In the final phase ($3T < t \leq 4T$) the removal of the PC signal results in the shuttle returning to its initial position, indicated by the displacement regressing to zero. Interestingly, the simulations predict accurately the preactuation, but the actual displacement augmentation by the PC signal is significantly larger than the one predicted by simulations ($2 - 2.33$ µm). As a reminder, the expected measurement accuracy of the optical measurement is < 10 nm. This could mean that the actual ratio between the fixed capacitors and variable capacitors is larger than designed, as well as that the spring constant is much lower due to fabrication process and dimensions' change. As the overlap of the fingers in the fixed capacitor is significant (90 % of the length) and their separation is much smaller than the distance between adjacent fingers in variable capacitors (0.5 µm and 1.5 µm, respectively), the underetching of the fingers within the fixed capacitor is smaller than the one of the variable capacitors. As the capacitance is inversely proportional to the distance between the adjacent fingers, this can explain the increase of the ratio between the two capacitance values.

The output state is established during the third phase ($2T < t \leq 3T$) through the complementary signals Q and $\bar{Q}$. As in the example given above, the voltage at the comb-pair A is larger than the one at the $\bar{A}$, the difference between the electrostatic forces will allow the movement that would bring the combs within the comb-pair A closer together, while pushing the electrodes within $\bar{A}$ further apart. This means that the output comb-pairs Q and $\bar{Q}$ will follow the same movement, resulting in the increased capacitance C_Q and a reduced $C_{\bar{Q}}$. As at the time of the experiment it was not possible to measure the real time change of the output capacitances, their values were calculated in dependence on the displacement (reached overlap between the fingers). For the example given above, the output capacitances reached at the $t = 3T$ are $C_Q(x = 3.1\ \mu\mathrm{m}) = 446$ fF and $C_{\bar{Q}}(x = -3.1\ \mu\mathrm{m}) = 120$ fF. The corresponding output voltages can be calculated with the following equations:

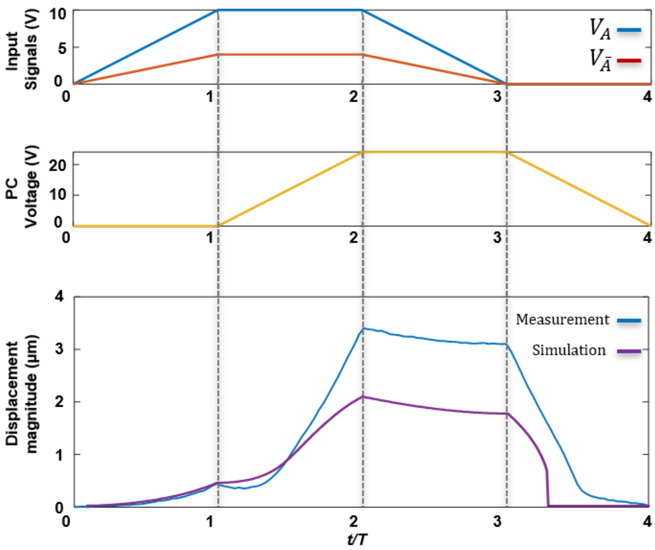


Figure 4.18: Experimental demonstration of the 4-phase logic state encoding with state preservation through PC signal. The first graph shows the complementary input signals A (blue) and $\bar{A}$ (red). The second one shows the power-clock signal, introduced with a delay of $t = T$ with respect to the input signals. The third graph shows the magnitude of the induced displacement (purple - simulated, blue - measured).

$$V_Q = \frac{C_{\text{fix}}}{C_{\text{fix}} + C_Q} V_{\text{PC}} \qquad V_{\bar{Q}} = \frac{C_{\text{fix}}}{C_{\text{fix}} + C_{\bar{Q}}} V_{\text{PC}} \tag{4.3}$$

As C_Q is higher than $C_{\bar{Q}}$, the output voltage V_Q will be lower than $V_{\bar{Q}}$, corresponding to the inverted input logic state. In the example above, the complementary output nodes reach the voltage levels of $V_Q = 12.8$ V, $V_{\bar{Q}} = 19.4$ V, demonstrating the inverter behavior of the MEMS logic gate. In a simple digital circuit where multiple gates are concatenated together, the output of the former would be used to actuate the input of the subsequent gate. As the obtained output voltages are larger than the input voltages used for the preactuation, the power clock voltage could be reduced and the proper operation would still be maintained. Moreover, the difference between the obtained *high* and *low* output voltages is larger than the difference predicted by the simulation ($V_Q = 14.3$ V, $V_{\bar{Q}} = 19.35$ V), meaning that the preactuation of the following gate would be larger that the one anticipated by the model. This further means that we are able to regenerate the signals as the gate is able to amplify the voltage level of a logic state.

Requirements for device operation

In the absence of input signals A and $\bar{A}$, and when applying only the power clock signal PC to the output stage via fixed capacitors, the movable electrodes are theoretically expected to either remain stationary (in an unstable equilibrium), because the forces (F_A and $F_{\bar{A}}$) exerted on the shuttle should be equal and cancel each other out, or move randomly to either direction, towards one of the stable equilibrium positions, the direction being

determined by the environmental noise.
However, due to fabrication imperfections, this perfect symmetry is compromised. Consequently, the power clock signal induces movement in one preferred direction, which is varying randomly among different devices.
The prerequisites for a successful actuation of the inverter gate is that the preactuation is sufficiently large to overcome the undesired preferential movement due to fabrication inhomogeneity and potentially environmental noise. The experiments have shown that when grounding one of the input electrodes, placing a voltage of 3 V on the complementary electrode is sufficient to induce the preactuation in the desired direction, even if the other one is preferred in the absence of input signals. These tests were performed on five different devices, with the correct actuation over 20 cycles. This gave the error rate of the preactuation with 3 V of less than 1%. According to our model, actuation with a 3 V signal induces a displacement of around 30 nm.
To ensure consistent movement in the desired direction, without conducting an extensive quantitative study, we chose to target a minimum pre-actuation three times larger ($\approx$ 100 nm) than the one experimentally determined. When one of the input electrodes is grounded, this displacement can be obtained when the complementary electrode is subjected to 6 V.

When both input electrodes are subjected to voltages V_A and $V_{\bar{A}}$ and forces exerted on movable shuttle cause its displacement x, the force balance equation can be expressed as:

$$F_A - F_{\bar{A}} = kx \tag{4.4}$$

with F_A and $F_{\bar{A}}$ being the opposing electrostatic forces acting on the shuttle and k being the spring constant of the suspension. By expressing the electrostatic forces through the applied voltages V_A and $V_{\bar{A}}$ and the capacitance derivatives at the given displacement x this equation can further be expressed as:

$$\frac{1}{2}V_A^2\frac{dC(u)}{du}\bigg|_{u=x} - \frac{1}{2}V_{\bar{A}}^2\frac{dC(-u)}{du}\bigg|_{u=-x} = kx \tag{4.5}$$

Knowing that the minimum set of the input voltages to achieve a displacement of 100 nm are 6 V and 0 V and using the equation 4.5, we can derive the operating window for the input voltage levels V_{H} and V_{L} (see Figure 4.19).

The blue line in the Figure 4.19 satisfies the equation:

$$V_{\mathrm{L}} = \sqrt{\frac{V_{\mathrm{H}}^2\frac{dC(u)}{du}\Big|_{u=x} - 2kx}{\frac{dC(u)}{du}\Big|_{u=-x}}} \tag{4.6}$$

while the red one corresponds to $V_{\mathrm{L}} = V_{\mathrm{H}}$. The shaded area represents a window

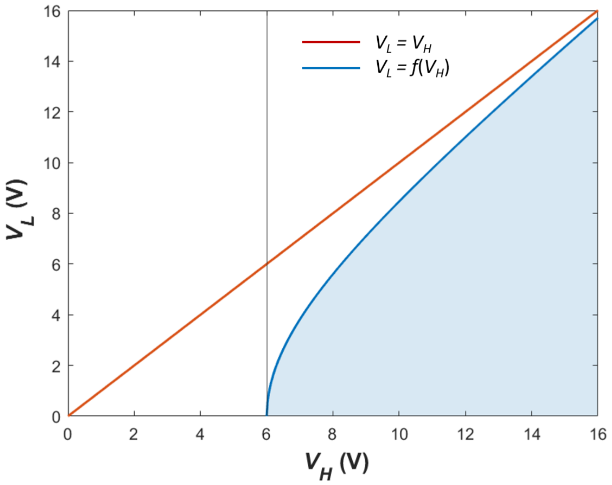


Figure 4.19: The blue-shaded area represents the operation window for V_H and V_L that are applied to input electrodes, required to induce a preactuation of at least 100 nm and successfully operate the gate.

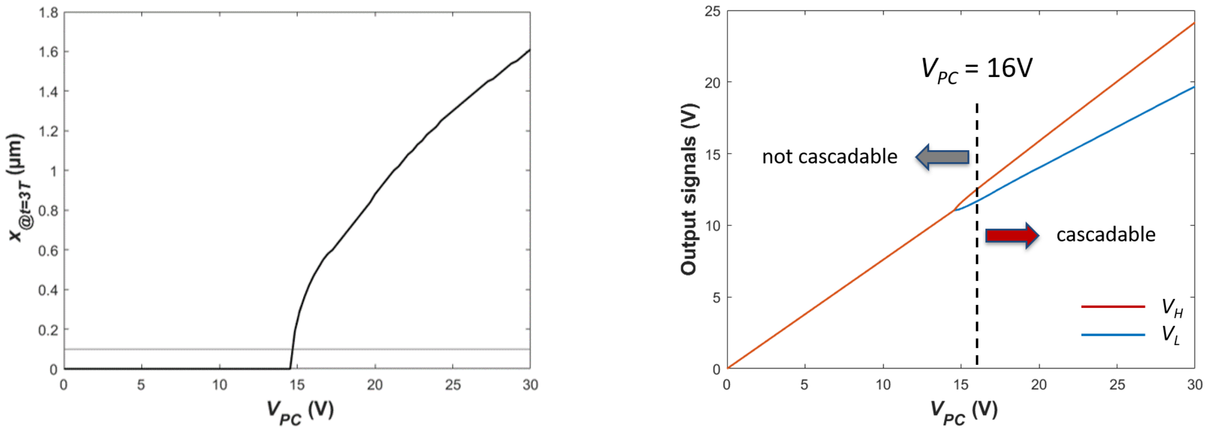
in which the combination of V_H and V_L would induce a preactuation of at least 100 nm, required to successfully operate the gate.

The operating range for V_PC is slightly less straight-forward. As explained in the chapter 2 and briefly reminded in the text above, the output state is established in the **third phase** called "maintenance" or "hold". In a digital circuit, the transfer of the logic state to the subsequent device would happen precisely at this stage. That means that the established output voltages at the $t = 3T$ should satisfy the requirements for high and low states, presented in the Figure 4.19, as these voltages will be used for preactuation of the subsequent device.
At the moment $t = 3T$ the input signals are back to 0. That means that the position of the movable shuttle is established solely through power clock and the capacitive dividers at the output. This position is plotted against different power clock levels in the Figure 4.20a.

The horizontal black line corresponds to 100 nm of the minimal displacement. From the calculated displacement values and corresponding PC voltages, we can calculate output states:

$$V_\mathrm{H} = \frac{C_\mathrm{fix}}{C_\mathrm{fix} + C_\mathrm{out}(-x)} V_\mathrm{PC} \qquad V_\mathrm{L} = \frac{C_\mathrm{fix}}{C_\mathrm{fix} + C_\mathrm{out}(x)} V_\mathrm{PC} \tag{4.7}$$

Where C_fix is the fixed capacitance of 500 fF and C_out is the established output capacitance at a displacement x reached at $t = 3T$. These states are shown in Figure 4.20b. We can see that only for the power clock voltages above around 15 V we can achieve state differentiation. Below $\approx$ 15 V the electrostatic forces are not large enough to maintain any displacement. This becomes more evident when looking at the potential energy curves at the $t = 3T$ (Figure 4.21).



(a) (b)

Figure 4.20: (a) Displacement at $t = 3T$ during the 4-phase actuation of an inverter gate, as a function of the power clock voltage. The horizontal black line corresponds to 100 nm of the minimal displacement. (b) Established output voltage levels at $t = 3T$ as a function of applied power clock voltages.

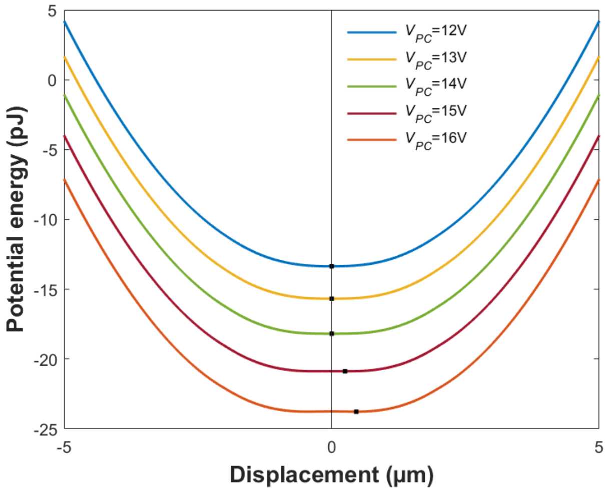


Figure 4.21: Potential energy vs. the position of the movable part of the inverter gate at $t = 3T$ (when the input signals are reduced to 0) for different power clock voltages: 12 V, 13 V, 14 V, 15 V, 16 V, with the minimum of each curve corresponding to the stable position of the movable part of the gate.

Below PC voltages of around 15 V the lowest potential energy value (stable position) is at the zero displacement. As the output voltages are established through the capacitive divider, low PC voltages are not sufficient to preserve the displacement. It is worth noting that although the potential energy curves are symmetrical in the absence of input signals and have two local minimums of the same magnitude, but different signs, the minimum that will be "chosen" as a displacement will be predefined by the preactuation through the input signals.

We can compare the above derived output voltage levels from the Eq. 4.7 to the ones obtained from Eq. 4.5 and presented in Figure 4.19. This comparison is shown in

Figure 4.22.

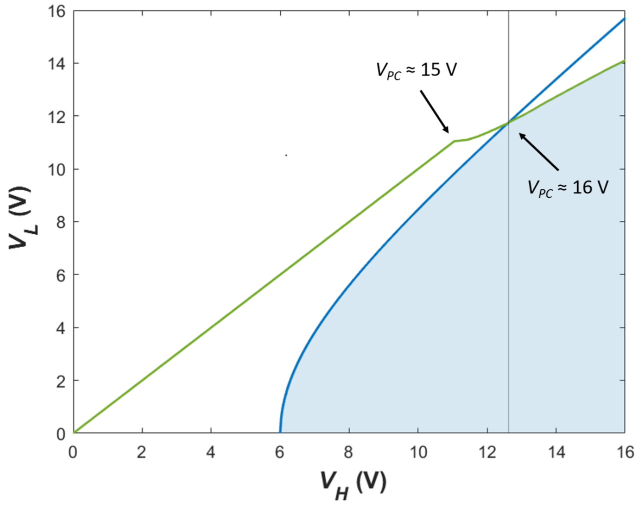


Figure 4.22: The operation window for V_{PC} for successful operation of the gate.

The intersection of the two curves corresponds to the power clock voltage of around 16 V. Below it, the preactuation of the following device would not be sufficient. Therefore, the minimum power clock voltage required for causing sufficient force imbalance for successful operation of the inverter logic gate is 16 V. The upper limit is set to around 30 V, as above this value the displacement becomes too large for the given geometry and the length of the fingers, which are determining the range of motion.

These experiments have demonstrated the full operation of an inverter gate, showing that both design and the microfabrication of the devices were successful. They are the first major proof of the CACL concept. These experiments also showed that the fixed capacitors successfully perform in the capacitance dividers and establish the output voltages through the applied power clock signals. Furthermore, they demonstrated that we can obtain output voltages that fulfill requirements for a preactuation. This confirms that one gate's outputs could be connected to another gate and used as its input signals. Moreover, the preactuation can be significantly amplified by the power clock, meaning that the input signals can be quite low, still allowing proper coding and propagation of the logic state.

4.3.3 Operation at high temperatures

The operating temperature of the silicon-based MOSFETs is limited to below 175°C [40]. They exhibit physical issues that limit the high-temperature functionality of p-n junctions, such as the increase of carrier density and junction leakage current with the temperature increase [41]. Nevertheless, harsh environments like those in the automotive, aerospace, and deep-earth drilling sectors are driving the need for advancements in device technologies, pushing higher temperature requirements higher. This has contributed to the development of wide band gap semiconductors such as SiC, GaN and diamond, which have pushed the temperature limits to the 300°C range (commercial SiC MOSFETs are still limited to operations below 200°C [42]). It has also motivated this set of experiments, which aim at investigating performance of a MEMS inverter logic gate at elevated temperatures. The displacement measurements were performed up to 200°C, which is the upper obtainable limit of the available equipment at the time of experiment. Starting from 100°C, the optical measurements became substantially more difficult, as the refractive index of air was modified due to increased temperature and was resulting in blurry and shifted images. The operation over the temperature range from 50°C to 450°C was investigated in air, using impedance measurements. The upper temperature limit was also determined by the equipment's capabilities and not by the device's failure.

The dynamic actuation of the inverter logic gates was done on Karl SUSS PA200 Semiautomatic probe station. The devices were actuated in four phases, using input signals $V_A = 10$ V, $V_{\bar{A}} = 4$ V and $V_{\mathrm{PC}} = 17$ V, with the temperature of the chuck being increased from 50°C up to 200°C. Their displacement was recorded with optical camera XIMEA xiQ and the maximum displacement value (measured at $t = 2T$) was plotted against the operating temperature and represented with blue dots in Figure 4.18.
For higher temperatures, we conducted electrical measurements to characterize the capacitance versus displacement when the input voltage was applied, a crucial metric for confirming MEMS functionality. This actuation corresponds to the pre-actuation (the first phase) in the 4-phase operation, the capacitance was measured on the input combs. No significant shift in capacitive values was observed, indirectly validating proper operation up to 450°C (pink dots in Figure 4.18). During this experiment the actual temperature of the sample surface was checked using a pyrometer, confirming that the sample surface was at the temperature set for the chuck.

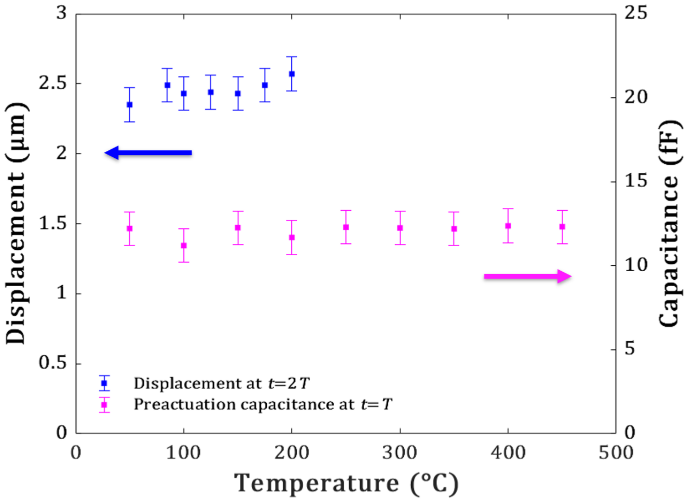


Figure 4.23: Characterization of NOT gate operation across different temperatures, ranging from 50°C to 450°C, constrained by the probe station capabilities. The displacement of the mobile part, encoding the logic state, is optically measured up to 200°C. Capacitance is measured using an impedance-meter, reflecting the variation of input capacitance during preactuation.

As shown in Figure 4.23, our CACL device remains functional at temperatures as high as 450°C. As our device relies on electrostatic interactions and mechanical movements, it exhibits remarkable resilience during high temperature operation. As a result, CACL is capable of withstanding high temperatures that could otherwise limit transistors and cause oxidation problems with relay contacts. It would be of further interest to conduct additional experiments at even higher temperatures (above 450°C) as well as to perform them under vacuum, which would avoid variations of the refractive index of the medium and make optical measurements achievable.

However, it is worth noting that different research works have demonstrated temperature-dependent properties of silicon, such as thermal expansion coefficients [43] or Young's modulus [44]. This means that at higher temperatures a change of mechanical properties would influence the device operation. As Young's modulus of silicon decreases with increasing temperature [44], the spring constant of the suspension will be reduced. This further changes the potential energy of the movable part of the device, influencing its equilibrium positions (displacements). Lower Young's modulus would therefore result in higher displacements, which for CACL device is rather beneficial, as it would allow reduction of voltage signals. Moreover, the mismatch between thermal expansion coefficients between silicon and silicon-oxide can cause stress within the device, subjecting it to additional forces and influencing its natural frequency.

More thorough investigation of the relationship between the operating temperature and driving parameters of the device is required.

4.4 Analysis of the operation in dynamic mode

As our MEMS device is driven by external voltages that induce the electrical forces within the combs, we can observe the device as a damped-driven oscillator. Each of the oscillation modes can be described by an equation, whereby the fundamental mode of vibration sets the upper limit for the operation speed (frequency) of the gates and is therefore the main focus of the further analysis. The device's motion in the dynamic mode can then be described with the following equation:

$$m_{\text{eff}}\ddot{x} + \alpha\dot{x} + k_{\text{eff}}x = F_{\text{el}}(x, \omega, t) \tag{4.8}$$

where m_{eff} and k_{eff} denote the effective mass and spring constant of the system, respectively, and α represents the damping coefficient. x is the time-varying position of the shuttle.

We can also define natural angular frequency $\omega_0 = \sqrt{\frac{k_{\text{eff}}}{m_{\text{eff}}}}$ and quality factor $Q = \dfrac{\omega_0 m_{\text{eff}}}{\alpha}$.

By taking the assumption for the external driving force $F_{\text{el}}(\omega, t) = Re\left\{F_0 e^{j\omega t}\right\}$ and the steady state solution of the equation of motion $x(t) = Re\left\{z(t)\right\} = Re\left\{Ae^{j(\omega t+\phi)}\right\}$ we can rewrite the Eq. 4.8 as:

$$-\omega^2 mz + j\omega\alpha z + kz = F_0 e^{j\omega t} \tag{4.9}$$

allowing us to express the amplitude of the motion $|x|$ as:

$$|x| = \frac{F_0}{\omega_0^2 m_{\text{eff}}} \frac{1}{\sqrt{(1-\frac{\omega^2}{\omega_0^2})^2 + (\frac{1}{Q}\frac{\omega}{\omega_0})^2}} \tag{4.10}$$

and the phase as:

$$\phi = \arctan(\frac{1}{Q}\frac{\omega/\omega_0}{(\omega/\omega_0)^2} - 1) \tag{4.11}$$

The natural frequency of a MEMS structure is determined by its effective mass and stiffness, as shown in the following equation:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_{\text{eff}}}{m_{\text{eff}}}} \tag{4.12}$$

The effective mass and effective stiffness differ from the static mass and static stiffness of the device and are different for each vibration mode. However, we assume here that the mass is the one corresponding to the static mass of the shuttle of the device and the movable combs. The stiffness is the one of the suspension beams. This is a reasonable assumption, because the shuttle and movable combs contain the major part of the mass of the system and experience the maximum of displacement. As for the stiffness, we know that the flexural stiffness of a beam is very close to the effective stiffness of its fundamental mode.

By estimating the mass of the movable part of the inverter logic gate to be around 190 ng and recalling the spring constant of $k = 1.5\ \mathrm{N\,m^{-1}}$, the first mechanical mode has been analytically calculated to be around 16 kHz.

4.4.1 Experimental analysis of dynamic behavior

In order to experimentally confirm this finding, we subjected the device to a frequency sweep from 5 kHz to 500 kHz and measured the input impedance. Figure 4.24 shows the measured impedance plotted against the whole frequency range, as well as the zoom on the first detected mode, which was observed to occur at a value of 10.9 kHz (Figure 4.24). This lower than predicted value can be explained by a lower $\frac{k_{\text{eff}}}{m_{\text{eff}}}$ ratio, which stems from geometrical changes due to microfabrication process and underestimation of m_{eff} in the fundamental mode. We can also observe higher order modes at 34.4 kHz, 45.7 kHz, 59.9 kHz, 97.8 kHz and 109.8 kHz.

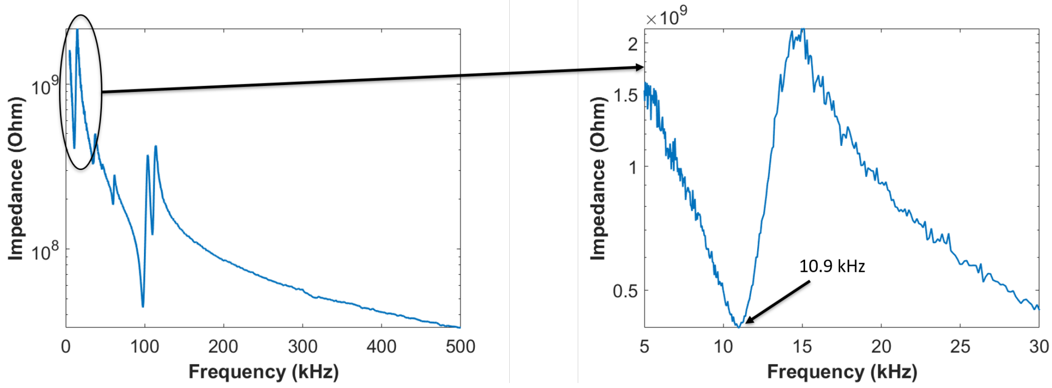
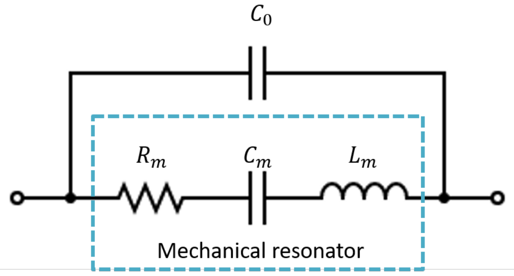


Figure 4.24: Frequency response of the input impedance of the gate and the zoom on the first resonance mode.

To characterize the electromechanical properties of the inverter logic gate we measured its response to a frequency sweep (5 kHz to 20 kHz) around the first resonance mode as this one will limit the frequency range of operation of the device. We performed the frequency sweep for different values of the V_{DC} signals, superposed by a V_{AC} signal with 0.5 V RMS. The electrical response was fitted with an RLC-C_0 model. Figure 4.25 shows the electrical equivalent of the mechanical resonator, indicating the link between the device's mechanical parameters and the extracted RLC values.



$$R_m = \frac{\sqrt{km}}{Q\eta^2} \quad C_m = \frac{\eta^2}{k} \quad L_m = \frac{m}{\eta^2}$$

Figure 4.25: Electrical equivalent circuit for micro resonator.

The exact RLC values and corresponding DC voltages are presented in Table 4.1.

This data allowed us to further calculate the fundamental frequency f_{r}, quality factor Q, the effective spring constant k_{eff} and the damping coefficient α for each of the V_{DC} voltages. For this calculation, we assumed a constant value for m_{eff}, corresponding to the one of the shuttle of the device and the movable combs, which we estimated to be about 190 ng.

In an ideal series RLC circuit the Q factor and resonant frequency f_{r} can be calculated as:

$$Q = \frac{1}{R_{\mathrm{m}}}\sqrt{\frac{L_{\mathrm{m}}}{C_{\mathrm{m}}}} \qquad f_{\mathrm{r}} = \frac{1}{2\pi}\frac{1}{\sqrt{L_m C_m}} \tag{4.13}$$

V_{DC} (V)	C_0 (fF)	C_{m} (fF)	L_{m} (kH)	R_{m} (MΩ)
14	25.34	17.33	10	159.2
13	19.37	12.98	13.59	213.9
12	16.05	10.65	17.24	268.7
11	13.67	8.83	21.72	353.1
10	11.97	6.83	28.65	474
9	10.56	4.7	41.03	671.6
8	9.06	3.31	55.93	974
7	7.72	2.15	82.73	1482
6	7.16	1.46	113.7	2313
5	7.13	0.74	218.2	3902

Table 4.1: RLC values extracted around the first resonance.

Knowing that the MEMS logic gate can be represented by an equivalent electrical circuit shown above in the Figure 4.25, where the series RLC circuit corresponds to the movable part of the gate and C_0 represents the non-motional current path, we can express the connection between the electrical and mechanical components through the following set of equations:

$$\eta = \sqrt{\frac{m_{\mathrm{eff}}}{L}} \qquad k_{\mathrm{eff}} = \frac{\eta^2}{C} \qquad Q = \frac{\sqrt{k_{\mathrm{eff}}}}{R\eta^2} \tag{4.14}$$

with η being the electromechanical transduction factor.

For the extracted RLC data presented in Table 4.1, and assuming a constant value of $m_{\mathrm{eff}} = 190$ ng, the corresponding values of f_{r}, Q, k_{eff} and α are shown in the Table 4.2, giving the average value of the Q of 4.4. This low value of the quality factor indicates high dissipation of the first resonance mode, as the dissipation coefficient $\alpha = \dfrac{m\omega_0}{Q}$. This energy loss is influenced by the velocity of the movable part, as described in Eq. 4.8 and 4.9. Consequently, lower velocities (power clock frequencies) result in reduced dissipation.

With the above calculated average value of the quality factor Q, average mechanical resonance frequency $f_r = 11.9$ kHz of the tested devices (Table 4.2), estimated mass of $m_{\mathrm{eff}} = 190$ ng and by using the equations 4.10 and 4.11 we can plot the magnitude and phase of the displacement of the movable part of the inverter gate with respect to the frequency of the driving force. The corresponding graphs are shown in Figure 4.26. The displacement magnitude is normalized to the amplitude of the force.

As shown in the lower graph of the Figure 4.26, the phase shift of the movement with respect to the driving force approaches zero for driving frequencies below the resonance frequency f_0. In this range the displacement follows a linear relationship with the force $x = \frac{F}{k}$ with a minimal phase delay. The maximum operating frequency for the power clock is therefore limited to the range far below the first resonance mode. Operating at a frequency close to f_0 would increase the displacement magnitude by a factor Q, which

V_{DC} (V)	η^2	k_{eff} ($\mathrm{N\,m^{-1}}$)	Q	f_{r} (kHz)	α
14	1.9^{-14}	1.1	4.77	12.1	3.3^{-6}
13	1.4^{-14}	1.08	4.78	12	3.29^{-6}
12	1.1^{-14}	1.03	4.74	11.8	3.33^{-6}
11	8.75^{-15}	0.991	4.44	11.5	3.55^{-6}
10	6.63^{-15}	0.971	4.32	11.4	3.65^{-6}
9	4.63^{-15}	0.985	4.4	11.5	3.58^{-6}
8	3.4^{-15}	1.03	4.22	11.7	3.73^{-6}
7	2.3^{-15}	1.07	4.19	11.9	3.76^{-6}
6	1.67^{-15}	1.14	3.82	12.4	4.13^{-6}
5	8.71^{-16}	1.18	4.4	12.5	3.58^{-6}

Table 4.2: Calculation of η, k_{eff}, Q and f_{r} from the RLC values extracted around the first resonance.

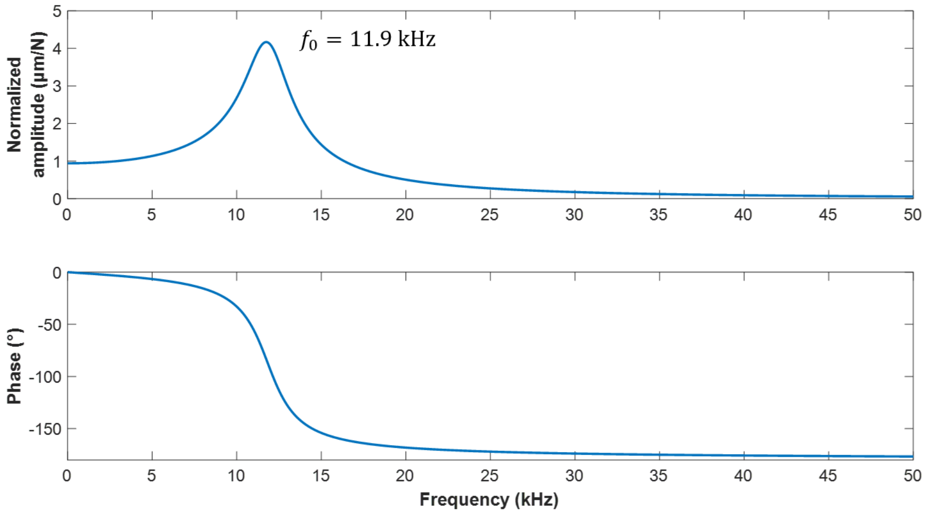


Figure 4.26: Frequency response of the mechanical structure of the gate: displacement magnitude, normalized to the force (top) and the phase shift (bottom) with respect to the frequency of the driving force.

would be detrimental for the device, considering the limited possible range of motion of l, corresponding to the length of the comb fingers. Furthermore, we can determine the mechanical time constant of the device $\tau = \dfrac{Q}{\omega_0} = 58.8$ µs, which is limiting the operating frequency of the power clock to below 17 kHz. Furthermore, the time constant introduces a delay between the applied voltage and the actual displacement of the structure. The delay that can be accommodated is defined by the duration of the phase of the power clock T ($4T = \frac{1}{f}$) and the fact that the state has to be evaluated in order to supply the following gate. A delay which is an order of magnitude below the phase duration T would correspond to 9°. Looking at the Figure 4.26 we can extract the maximum operating frequency which is allowing a phase delay of 9° to be about 6.1 kHz.

4.4.2 Spring softening effect in the dynamic mode

The spring softening effect, introduced in the 4.3.1, becomes further evident in the dynamic mode by examining the first resonance frequency f_0 of the spring-mass system of the comb-drive actuator. When a voltage $V(t) = V_{\mathrm{DC}} + V_{\mathrm{AC}}\sqrt{2}\cos(2\pi f t)$ is applied to the device, the DC part induces a static displacement of the shuttle leading to an overlap u_{DC} of the comb fingers. Meanwhile, the AC part generates a time-varying force F_{AC} driving the vibration at frequency f.

The electrostatic force F_{el} within a comb-capacitor with a finger overlap u is given by

$$F_{\mathrm{el}}(u,t) = \frac{1}{2}\frac{dC(u)}{du}V(t)^2 \tag{4.15}$$

Where V and C correspond to the voltage applied to the terminals and the comb-capacitance, respectively.

Around the equilibrium position u_{DC}, the position of the shuttle is $u = u_{\mathrm{DC}} + x$. Using Taylor expansion we can express comb-capacitance $C(u) = C(u_{\mathrm{DC}} + x)$ as following:

$$C(u_{\mathrm{DC}} + x) = C(u_{\mathrm{DC}}) + \frac{dC(u)}{du}x\bigg|_{u=u_{\mathrm{DC}}} + \frac{1}{2}\frac{d^2C(u)}{du^2}x^2\bigg|_{u=u_{\mathrm{DC}}} + O(x^3) \tag{4.16}$$

This then gives us the electrostatic force in the form:

$$F_{\mathrm{el}}(u_{\mathrm{DC}} + x, t) = \frac{1}{2}V(t)^2\left[\frac{dC(u)}{du}\bigg|_{u=u_{\mathrm{DC}}} + \frac{d^2C(u)}{du^2}x\bigg|_{u=u_{\mathrm{DC}}} + O(x^2)\right] \tag{4.17}$$

Knowing that $V(t) = V_{\mathrm{DC}} + V_{\mathrm{AC}}\sqrt{2}\cos 2\pi f t$ and $V_{AC} << V_{DC}$, we can rewrite $F_{\mathrm{el}}(t)$ as:

$$F_{\mathrm{el}}(u_{\mathrm{DC}}+x,t) = \frac{1}{2}\left[V_{\mathrm{DC}}^2 + 2\sqrt{2}V_{\mathrm{DC}}V_{\mathrm{AC}}\cos 2\pi f t\right]\left[\frac{dC(u)}{du}\bigg|_{u=u_{\mathrm{DC}}} + \frac{d^2C(u)}{du^2}x\bigg|_{u=u_{\mathrm{DC}}}\right] \tag{4.18}$$

and by keeping only the terms at frequency f:

$$\begin{aligned} F_{\mathrm{el}}(u_{\mathrm{DC}} + x, t) &= \sqrt{2}V_{\mathrm{DC}}V_{\mathrm{AC}}\cos 2\pi f t\frac{dC(u)}{du}\bigg|_{u=u_{\mathrm{DC}}} + \frac{1}{2}V_{\mathrm{DC}}^2\frac{d^2C(u)}{du^2}x\bigg|_{u=u_{\mathrm{DC}}} \\ &= F_{\mathrm{AC}}(t) - k_{\mathrm{el}}x \end{aligned} \tag{4.19}$$

where $F_{\mathrm{AC}}(t) = V_{\mathrm{DC}}V_{\mathrm{AC}}\sqrt{2}\frac{dC(u)}{du}\bigg|_{u=u_{\mathrm{DC}}} \cos 2\pi f t$ and $k_{\mathrm{el}} = -\frac{1}{2}V_{\mathrm{DC}}^2\frac{d^2C(u)}{du^2}\bigg|_{u=u_{\mathrm{DC}}}$.

$F_{\mathrm{AC}}(t)$ is the time-varying force driving the vibration at frequency f and k_{el} is the electrostatic spring constant arising from the second derivative of the capacitance at the overlap u_{DC}. The resonance frequency f_{r} is then calculated as:

$$f_{\mathrm{r}} = \frac{1}{2\pi}\sqrt{\frac{k_{\mathrm{eff}} + k_{\mathrm{el}}}{m_{\mathrm{eff}}}} \tag{4.20}$$

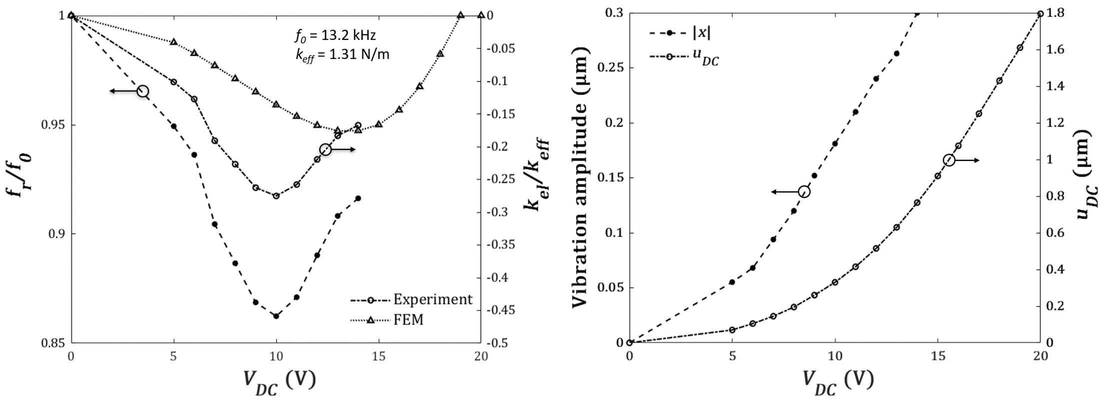
whereas the amplitude of the vibration at resonance is given by:

$$|x| = \frac{QF_{\mathrm{el}}}{k_{\mathrm{eff}}} = \frac{Q}{k_{\mathrm{eff}}} V_{\mathrm{DC}} V_{\mathrm{AC}} \frac{dC(u)}{du}\bigg|_{u=u_{\mathrm{DC}}} \tag{4.21}$$

In the previous subsection, we measured the impedance of a comb-drive actuator versus frequency. The electrical response was then fitted with an RLC-C_0 circuit, allowing to deduce the resonance frequency f_{r} [45], whose values were shown in the Table 4.2. In Figure 4.27a, normalized f_{r} is plotted versus V_{DC} for a comb-drive actuator with zero initial overlap. Values of f_{r} are normalized to the resonance frequency f_0 at $V_{\mathrm{DC}} = 0$ which cannot be electrically measured since no oscillation amplitude can be detected. In this study, we estimated f_0 through data extrapolation. Assuming a linear relationship between the resonance frequency and V_{DC}^2 for voltages below 8 V and using the data points at $V_{\mathrm{DC}} = 5$, 6, 7 and 8 V, we derived a fit to the data yielding $f_0 = 13.2$ kHz. This f_0 value was then utilized to generate the Figure 4.27a.

f_{r} exhibits variations greater than 10% towards low frequencies, indicating a substantial electrostatic spring constant k_{el} in the gray zone. Interestingly, a notable feature is observed in the measurements. Despite the quadratic dependence of k_{el} on V_{DC}, $|k_{\mathrm{el}}|$ peaks at $V_{\mathrm{DC}} = 10$ V and diminishes for larger voltages, leading in turn to an increase in f_{r}. This observation aligns with the evolution of capacitance: as V_{DC} increases, the overlap u_{DC} also increases, causing the capacitance to vary more linearly with displacement (see Figure 2.10a), approaching the behavior of a comb-structure with engaged fingers. Consequently, the second derivative of capacitance tends towards 0 (as illustrated in the inset of Figure 2.10b). Since $|k_{\mathrm{el}}|$ is proportional to the second derivative of capacitance, it is also expected to decrease towards 0, as observed in Figure 4.27a, resulting in the resonance frequency f_{r} tending to revert back to f_0. The difference in voltage values at which the maximum $|k_{\mathrm{el}}|$ is observed between experimental measurements ($V_{\mathrm{DC}} = 10$ V) and FEM simulations ($V_{\mathrm{DC}} = 13$ V) can be explained by the device's high sensitivity to microfabrication process and geometric variations.
The vibration amplitude $|x|$ is represented in Figure 4.27b in dependence on V_{DC} along with the static displacement u_{DC}. The vibration amplitude is also dependent on the amplitude of the AC voltage V_{AC}, as derived in the Eq. 4.21. The significant electrostatic spring constant within the *gray zone* could offer the possibility to design comb-drive micro-resonators capable of frequency tunability.

In this section, the dynamic mode was analyzed for small vibration amplitudes using



(a) **(b)**

Figure 4.27: (a) Variation of the resonance frequency f_r and of the electrostatic stiffness k_el of a comb-drive actuator measured for V_DC ranging from 5 to 14 V. Values marked with triangles are calculated from FEM data, the ones marked with circles are experimental. The resonance frequency $f_0 = 13.20$ kHz for $V_\mathrm{DC} = 0$ V is extrapolated from the measurements. $k_\mathrm{eff} = 1.31\ \mathrm{N\,m^{-1}}$ is the effective stiffness obtained assuming an effective mass of $m_\mathrm{eff} = 190$ ng. The comb-drive actuator was designed and fabricated with a zero initial overlap. $V_\mathrm{AC} = 500$ mV was used for the measurements. (b) Equilibrium position u_DC and the vibration amplitude $|x|$ calculated for each of the DC voltages represented on the x-axis.

the linear model given by Eq. 4.8. The description takes into account the non-linear variation of capacitance within the gray zone through the calculation of the electrostatic spring constant k_el. Higher-order non-linear terms could be introduced into the description, paving the way for an in-depth investigation of the non-linear dynamics of the system. This could potentially reveal a variety of complex behaviors like bifurcations and transitions between different coexisting response regimes, as has been widely studied in MEMS devices [46, 47, 48].

4.5 NAND logic gates

NAND gate, a fundamental component in digital electronics, operates on two inputs and produces an output. It yields a logic high (1) output unless both inputs are logic high, in which case it outputs a logic low (0). Employed extensively in constructing logic circuits, its versatility allows for the creation of complex systems (like D Flip-Flop and the XOR/XNOR), making it a cornerstone in digital logic design and computation.

In this experiment, the CACL NAND gates introduced in the previous chapter were tested and their performance was compared to the expected behavior derived by simulations.

When adapted to the dual rail architecture and the NAND gate design developed in the previous chapter, the truth table of a CACL NAND reflects a behavior represented in Table 4.3. As the size of comb-pairs A and B is smaller than the size of $\bar{A}$ and $\bar{B}$, the electrostatic forces F_A and F_B will overcome $F_{\bar{A}}$ and $F_{\bar{B}}$ only when both V_A and V_B are set to V_{H}. In all the other cases $F_A + F_B < F_{\bar{A}} + F_{\bar{B}}$. Figure 4.28 highlights the direction in which the individual electrostatic forces are acting within the input stage, resulting in a total force $F_{\mathrm{total}} = F_{\bar{A}} + F_{\bar{B}} - F_A - F_B$ which determines the preactuation direction and therefore the output logic state.

A	$\bar{A}$	state	B	$\bar{B}$	state	Q	$\bar{Q}$	state	displacement
V_{H}	V_{L}	1	V_{H}	V_{L}	1	V_{L}	V_{H}	0	negative
V_{H}	V_{L}	1	V_{L}	V_{H}	0	V_{H}	V_{L}	1	positive
V_{L}	V_{H}	0	V_{H}	V_{L}	1	V_{H}	V_{L}	1	positive
V_{L}	V_{H}	0	V_{L}	V_{H}	0	V_{H}	V_{L}	1	positive

Table 4.3: Truth table of a NAND gate based on dual rail architecture.

For the interpretation of the results a following convention was made: if V_A is set to a higher voltage level (V_{H}) than $V_{\bar{A}}$ (V_{L}), the logic state of the comb-pair $A\&\bar{A}$ will be set to 1. Analogously, configuration where $V_A = V_{\mathrm{L}}$ and $V_{\bar{A}} = V_{\mathrm{H}}$ corresponds to the logic state 0 at comb-pair $A\&\bar{A}$. State encoding on the comb-pair $B\&\bar{B}$ follows the same convention. At the output stage, the displacement in the positive x direction represents a logic state 1, whereas the negative x displacement corresponds to state 0. For the sake of simplicity, the comb-pair $A\&\bar{A}$ will be further referred to as $\underline{A}$ and comb-pair $B\&\bar{B}$ as $\underline{B}$.

Analogously to the operation of the inverter gate, previously discussed in 4.3.2, the state encoding in a NAND gate is performed in four phases.

In the **first phase** two sets of input signals $\underline{A}$ and $\underline{B}$ are introduced. Only in the case where both $\underline{A}$ and $\underline{B}$ are set at state 1, the electrostatic forces acting in the negative x direction will become sufficiently large to overcome the ones acting in the positive x direction, resulting in the negative x preactuation. In all the other cases, the preactuation will yield positive x values.

In the **second phase** the power-clock signal V_{PC} is applied via the capacitive bridge, continuing the movement of the beam in the predefined direction and establishing the output signals Q and $\bar{Q}$ at corresponding values. In the case of negative x preactuation, the output voltages V_Q and $V_{\bar{Q}}$ will be established at levels V_L and V_H, respectively, corresponding to the output state 0.

In the **third phase** the input signals $\underline{A}$ and $\underline{B}$ are gradually lowered to ground, while the V_{PC} is maintained at its V_{dd} value. During this phase the output signals (logic state) would be transferred to the subsequent device and used as its inputs (preactuation signals).

In the **fourth phase** the V_{PC} signal is gradually reduced, leading the position of the beam towards the resting position.

Starting from the sets of signals corresponding to each of the input-logic-state combinations shown in Table 4.3, the expected displacements were simulated as if they were applied consecutively to the device. The displacements were retrieved from the potential

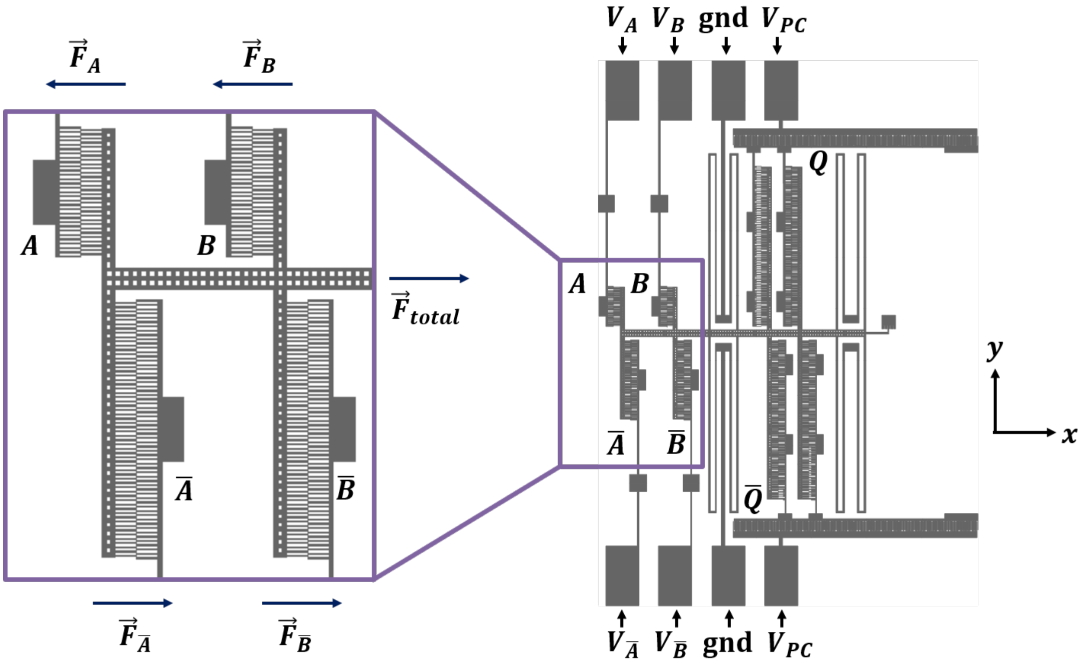


Figure 4.28: Design of the NAND gate with the asymmetric number of fingers in the complementary input comb-pairs, with the zoom on the input stage, highlighting the direction in which the individual electrostatic forces are acting. In the design snapshot the connections of the active electrodes of the complementary input combs to signals A and $\bar{A}$ as well as B and $\bar{B}$ are indicated, as well as application of power clock signal V_{PC} to the active electrodes of the output combs through the fixed capacitor C_{fix}. The spring and the movable part of the device are grounded.

energy curves as in the previous subsections, where the minimums of the curves were taken as stable positions and displacement magnitudes. They are presented in Figure 4.29.
The first combination of the input states is "$\underline{A} = 1$, $\underline{B} = 0$", meaning that $V_A = V_{\mathrm{H}}$, $V_{\bar{A}} = V_{\mathrm{L}}$, $V_B = V_{\mathrm{H}}$ and $V_{\bar{B}} = V_{\mathrm{L}}$. In this case $F_A + F_B > F_{\bar{A}} + F_{\bar{B}}$ giving $F_{\mathrm{total}} < 0$ and the preactuation in the negative x direction. This displacement is subsequently augmented through the application of PC signal, giving the output state 0.
The the remaining three combinations of the input states, $F_A + F_B < F_{\bar{A}} + F_{\bar{B}}$, giving the preactuation in the positive x direction and the output state 1.
For the input-state-combinations "$\underline{A} = 1$, $\underline{B} = 0$" and "$\underline{A} = 0$, $\underline{B} = 1$" the F_{total} is the same and causes a preactuation of 160 nm. In the case of "$\underline{A} = 1$, $\underline{B} = 1$" the preactuation is the largest and amounts to 320 nm. When the inputs are set to "$\underline{A} = 0$, $\underline{B} = 0$" the magnitude of the preactuation is the smallest and equals 20 nm. The maximal displacement magnitudes are between 2.6 µm and 2.72 µm, while the displacements reached at the moment when the inputs are reduced to 0 ($t = 3nT, n = 1, 2, 3, 4$) are in each simulated case 2.46 µm.

In order to test the proposed geometry for the NAND devices, the devices were actuated on a probe station, with the chuck heated to 60°C to eliminate surface humidity from the sample. Voltages were subsequently applied to input electrodes A, $\bar{A}$, B, and $\bar{B}$, followed by power clock V_{PC} application after time T. The device's movable part, including

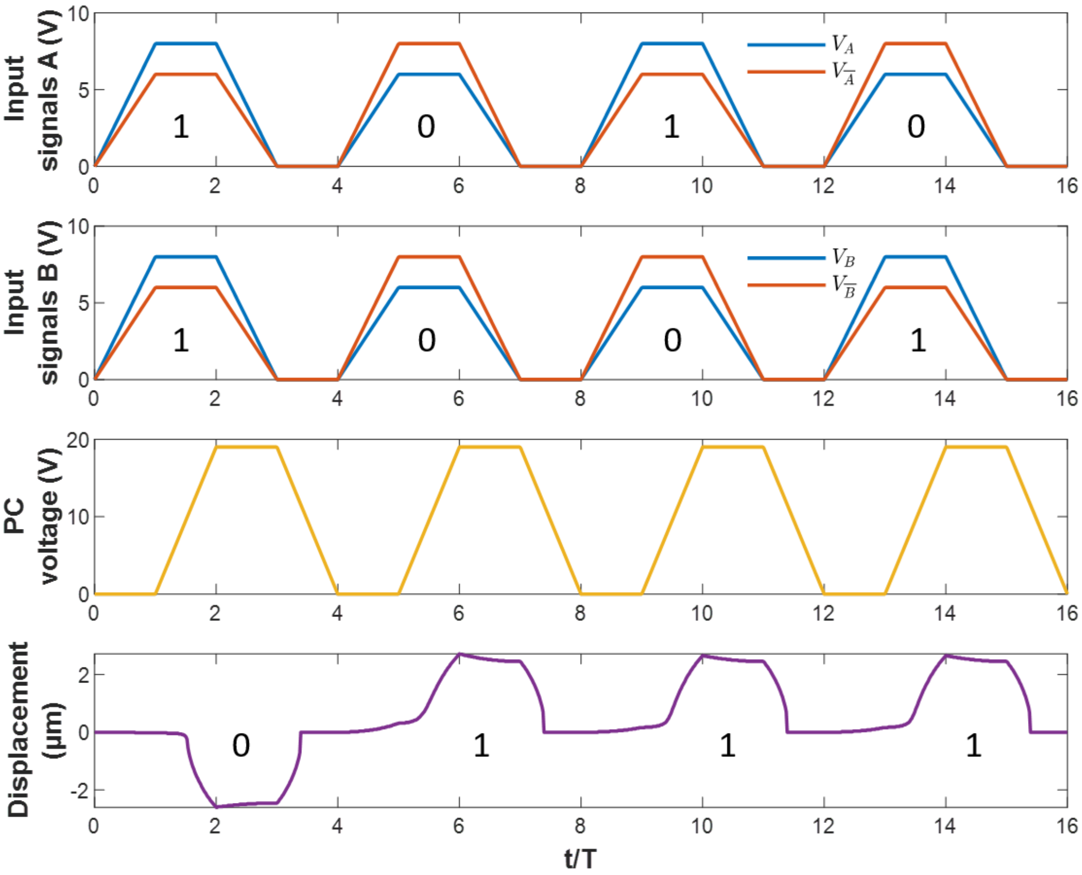
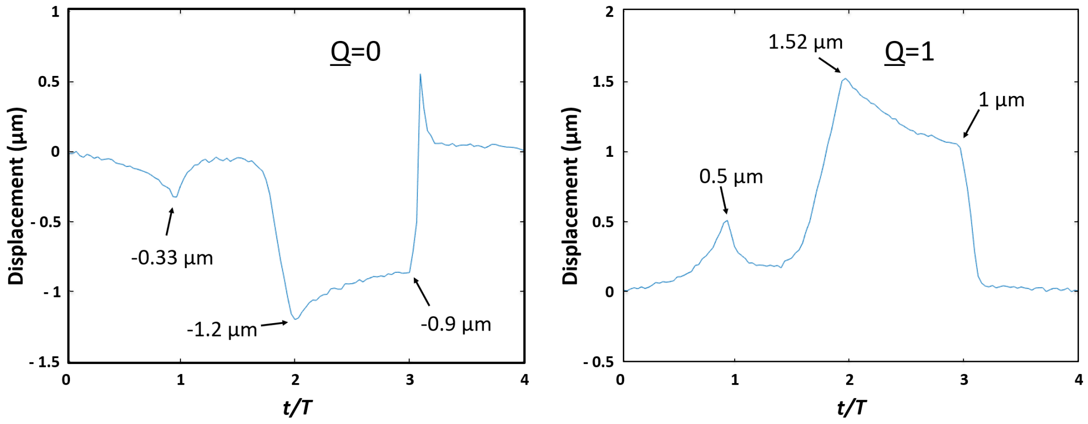


Figure 4.29: Simulation of displacement with respect to the applied signals at the inputs A and B. The first two graphs show the four combinations of states at the inputs (1-1, 0-0, 1-0 and 0-1). The third graph shows the PC signal applied with a delay T with respect to the inputs. The fourth graph shows the corresponding displacement for each of the combinations of the input logic states A and B.

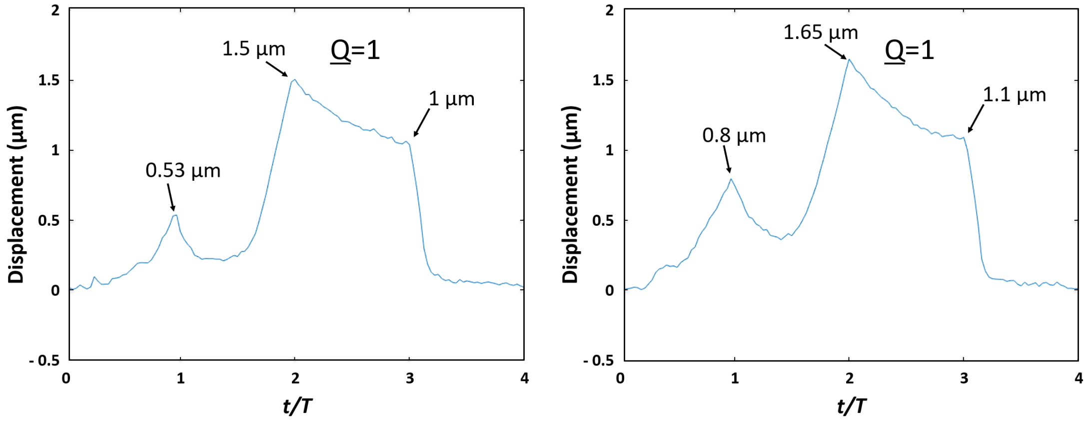
its spring, is grounded. Voltage waveforms exhibit a trapezoidal shape, aligning with the adiabatic principle outlined in chapter 2. Displacement is monitored using an optical camera (XIMEA xiQ), with image processing detailed previously in subchapter 4.1.2. Systematic application of voltages representing each truth state outlined in Table 4.3 is carried out, with high, low, and PC voltages set at 8 V, 6 V, and 19 V, respectively as depicted in Figure 4.28.

The optically measured displacements are depicted in Figure 4.30. As was the case with the simulated results, positive displacement aligns with the establishment of a high logic state at the output, illustrated in Figure 4.28 as positive x-direction.

Table 4.4 summarizes and compares the simulated and optically measured displacement values for each of the logic states at three instants: $t = T$, corresponding to preactuation, $t = 2T$, at which the maximal displacement is reached and $t = 3T$, showing the displacement



(a) $\underline{A} = 1$, $\underline{B} = 1$, $\underline{Q} = 0$ **(b)** $\underline{A} = 1$, $\underline{B} = 0$, $\underline{Q} = 1$



(c) $\underline{A} = 0$, $\underline{B} = 1$, $\underline{Q} = 1$ **(d)** $\underline{A} = 0$, $\underline{B} = 0$, $\underline{Q} = 1$

Figure 4.30: Displacement of the movable device part with respect to the combination of the signals applied to input pairs A and B. The state evaluation is taking place during the phase $2 < t/T < 3$. Positive direction for the displacement is taken as the one yielding a high output state.

maintained through power clock.

		$\underline{A}0\underline{B}0$	$\underline{A}0\underline{B}1$	$\underline{A}1\underline{B}0$	$\underline{A}1\underline{B}1$
	t	Displacement (µm)			
Simulation	T	0.32	0.16	0.16	-0.02
	$2T$	2.72	2.66	2.66	-2.6
	$3T$	2.46	2.46	2.46	2.46
Measurement	T	0.8	0.53	0.5	-0.33
	$2T$	1.65	1.5	1.52	-1.2
	$3T$	1.1	1	1	-0.9

Table 4.4: Comparison of the simulated and measured displacement values for each of the input logic state combinations at three instants: $t = 1T$ (pre-actuation), $t = 2T$ (maximal displacement) and $t = 3T$ (PC maintained displacement).

Interestingly, the measured preactuations are larger than the simulated ones. This can be attributed to the fact that the fabricated spring features a lower spring constant due to underetching of the beams. As a consequence, the difference between the used *high* and *low* voltages causes a larger observable preactuation of the NAND gate. On the other hand, the measured maximal achieved displacements of the movable electrodes (1.2 − 1.65 µm) are lower than the ones predicted by the simulation (2.6 − 2.7 µm). This can be explained by the slight variations in realized geometry of the device during microfabrication. Underetching of the fingers strongly influences the achievable capacitance values, whereas the underetching of the spring causes variations of the potential energy of the device during logic operations and therefore the achieved displacement.

During the gradual removal of the input signals ($2 < t/T < 3$) we observe a reduction in displacement of around 0.6 µm, compared to the simulated value of 0.28 µm. The larger-than-predicted reduction may be explained by the leakage of the charges. Namely, as the capacitances within the device add up to a a value of the order of magnitude of pF and the leakage resistance was measured at about 400 GΩ, the associated time constant is in the order of magnitude of seconds. As the experiments were performed at a frequency of 0.5 Hz, the leakage is a consequence of the fact that the RC time constant and the period of logic operation are of the similar value.

These experiments have successfully demonstrated the state-encoding with the NAND gate, paving the way for other logical operations. In a digital circuit the output displacement of the NAND gate and therefore the established voltages should reach a minimum value in order to preactuate a subsequent device. These analyses, yielding an operation window for the driving voltages of a NAND gate are still to be done.

Moreover, the dual-rail architecture of the NAND gate allows interchanging the output capacitors Q and $\bar{Q}$, enabling the realization of an AND gate ($\wedge$) using the same architecture. Additionally, knowing that $\neg(A \wedge B) = (\neg A) \vee (\neg B)$, the same device can be adapted to implement an OR ($\vee$) gate and, subsequently, a NOR gate by also switching the complementary outputs. This versatility is made possible solely due to the dual-rail architecture and concept. Consequently, NAND, AND, OR, and NOR operations can be achieved with this single device by simply changing the electrical routing of complementary inputs and outputs.

4.6 Cascade

One crucial property for establishing a logic family is the ability to cascade logic operations. This means that information must be preserved and successfully transferred to the next device. For CACL inverter gates, the input state from the first gate is inverted at the output stage and used as a pre-actuation signal for the following device.

The logic state encoding and transportation within a cascade of devices is carried out in four phases, governed by four power clock signals. These signals have identical amplitudes and trapezoidal waveforms, and are shifted by a quarter period relative to each other.

To demonstrate this cascading capability, we experimentally tested a pipeline of 10 NOT gates. Each gate, identical to the previously tested individual NOT gates, is connected to the next. The differential output signals (Q, $\bar{Q}$) of one gate serve as inputs (A, $\bar{A}$) for the next gate in the pipeline. The additional capacitive interconnects slightly reduce the capacitive ratios but do not affect logic differentiation. The experiment was conducted on a probe station with the chuck heated to 60°C to eliminate surface humidity. Pre-actuation voltages were applied to the input electrodes (A and $\bar{A}$) of the first gate, followed by the application of the power clock V_{PC1} after time T. The remaining three power clock signals were each applied with an additional delay T relative to the previous power clock signal. The movable part of the device, including its spring, was grounded.

According to the adiabatic principle, voltage signals exhibit a trapezoidal shape. A single logic state ("0") was tested, with high, low, and power clock voltages set at 8 V, 4 V, and 12 V, respectively. Pads were connected through an 18-tip probe as depicted in Figure 4.31. The displacement of each gate was monitored individually using an optical camera (XIMEA xiQ), followed by image processing as described previously in section 4.1.2.

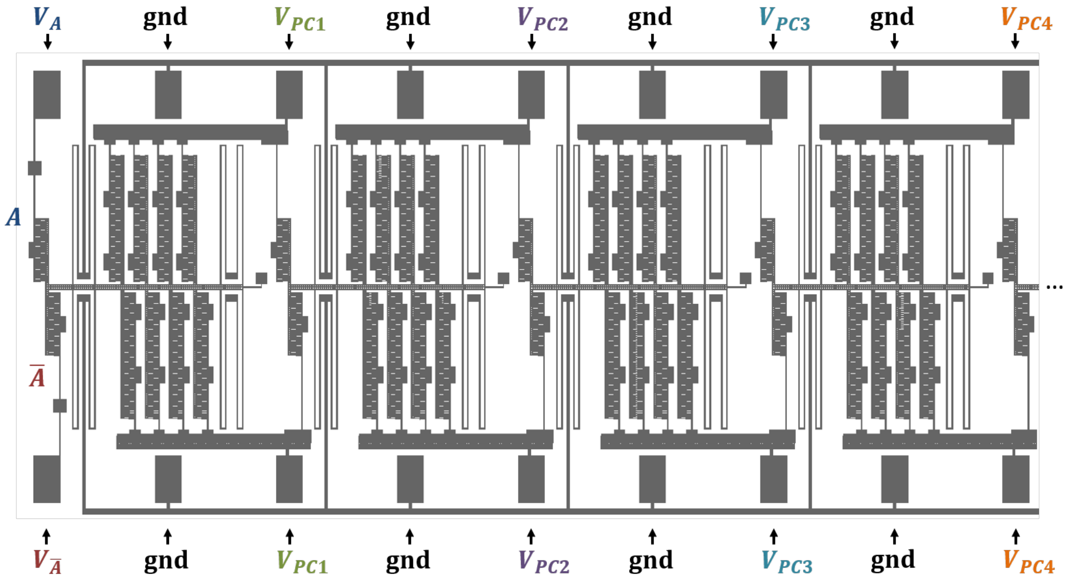


Figure 4.31: The first four inverter gates in a cascade of ten concatenated devices. In the design snapshot the connections of the active electrodes of the complementary input combs to signals A and $\bar{A}$ are indicated, as well as application of power clock signals $V_{\mathrm{PC1}} - V_{\mathrm{PC4}}$ to the active electrodes of the output combs through the fixed capacitors C_{fix}. The springs and the movable parts of the devices are grounded.

The optically measured displacements of each of the ten consecutive inverter gates are shown in Figure 4.32. According to the convention established in section 4.5, if V_A is set to a lower voltage level (V_{L}) than $V_{\bar{A}}$ (V_{H}), the input logic state of the comb-pair will be 0. Displacement in the positive x-direction indicates a high logic state at the output (logic state 1), while displacement in the negative x-direction corresponds to logic state 0.

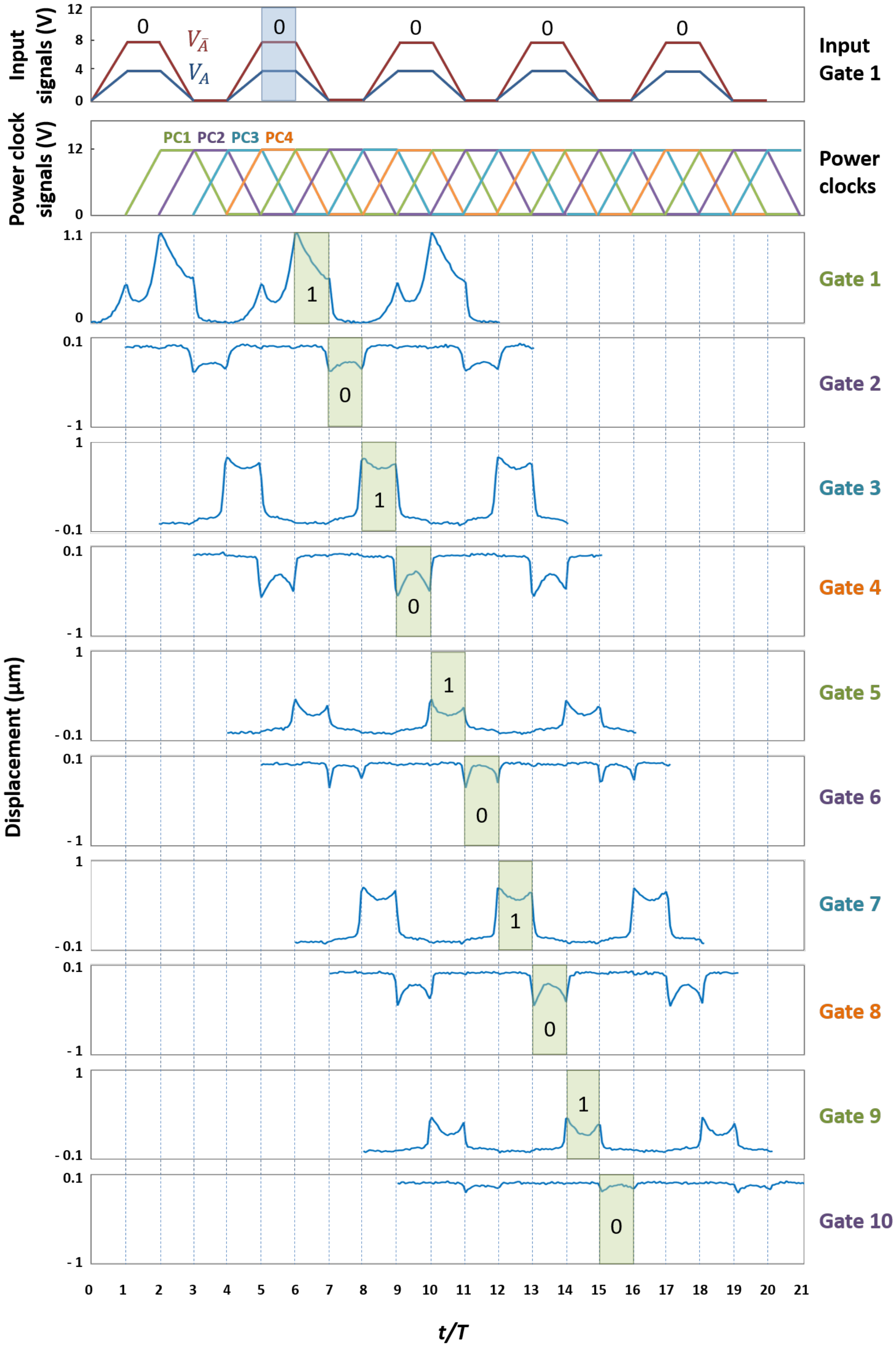


Figure 4.32: Measured displacements on ten consecutive inverter gates. The first graph shows the input signals at the first gate, which are causing preactuation, encoding the logic state 0 ($V_A = V_{\mathrm{H}}$, $V_{\bar{A}} = V_{\mathrm{L}}$). The second graph shows the four PC signals whereby the PC1 is applied with a delay T with respect to the inputs. The remaining three PC signals are each applied with additional T delay with respect to the previous PC signal. The state is inverted between each two consecutive gates.

The first graph displays the input signals at the first gate, which cause pre-actuation and encode the logic state 0 ($V_A = V_\mathrm{H}$, $V_{\bar{A}} = V_\mathrm{L}$). The second graph shows the four power clock (PC) signals. PC1 (green) is applied with a delay T relative to the inputs. The remaining three PC signals are each applied with an additional delay T relative to the previous PC signal. Graphs 3-13 show the displacements of each of the ten inverter gates, measured over three consecutive periods of state encoding.

As evident from the Figure 4.32 the state is inverted between each two consecutive gates. The shape of the first gate's displacement is quite consistent with what the simulations predict and what was demonstrated in the case of a single gate (Figure 4.18).

However, starting from the second gate, the behavior is quite different. The pre-actuation is very low, with the rapid displacement increase occurring when the V_{PC} has almost reached its maximum value. Maximum displacements of the gates 2-10 are lower than the displacement of the first gate. Moreover, they have varying amplitudes. This can be attributed to the electrical leakage that could vary from one gate to another. As the output node is high impedance, voltage may vary with the leakage rate, and with it, the displacement. On the other hand, the displacement amplitude does not necessarily decrease from gate to gate. For example, we see an increase in displacement from gate 2 to gate 3 as well as from gate 6 to gate 7. That means that the CALC concept features the capability to regenerate the logical levels from gate to gate, which is an utmost requirement in digital circuits (particularly for noise immunity).

Another interesting observation is that for gates 2 through 10, a displacement peak occurs when V_PC reaches the end of the plateau, just before it starts to decrease. This peak is absent in the first gate. Specifically, in the first gate, the input signals are linearly decreased to zero during this phase ($2T < t < 3T$). However, for the other gates, during the corresponding phase, the input signals decrease more rapidly to zero. Meanwhile, the subsequent gate ($N + 1$) experiences an increase in the power-clock signal, which varies the input capacitance of gate $N + 1$ and further alters the capacitive divider ratio at the output of gate N. This "*back action*" phenomenon and the complex interaction of various simultaneous changes could be analyzed through behavioral modeling of multiple cascaded gates using Verilog or similar software.

Although the specific shape of the displacement curves requires further investigation, these experiments have demonstrated successful logic state inversion across a pipeline of ten inverter gates, as summarized in the Figure 4.33. Additionally, they have shown that after the displacement decreases at gate N, the displacement at gate $N + 1$ is not hindered; it can be regenerated and amplified, satisfying an important requirement for the robustness of operation of complex circuits.

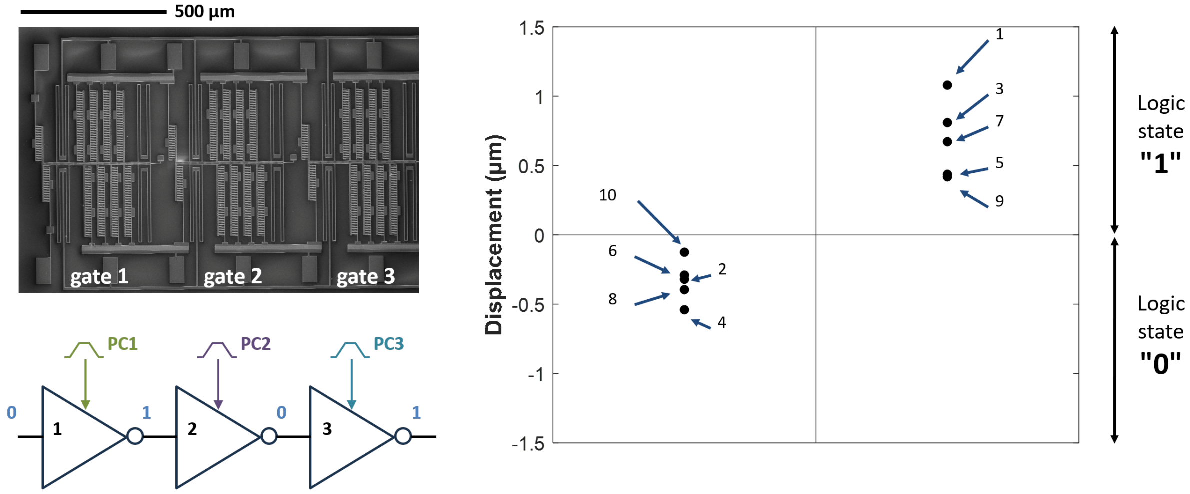


Figure 4.33: Cascade of 10 Pipelined Inverting Buffers: Each NOT gate inverts the state of the previous output. In the example shown, the logical state 0 at the input propagates through the gates, resulting in a state 0 at the output. The SEM image displays three successive NOT gates in the cascade. The displacements of the mobile parts for each gate are plotted against the encoded logical state, indicating some variability in the displacements.

4.7 Conclusion

In summary, this chapter has presented the results of a comprehensive investigation into the correlation between voltage and displacement in combs featuring near-zero overlap, highlighting the significant influence of geometric variations on device performance. Through detailed experimentation and analysis, it has been demonstrated that the CACL MEMS inverter gate operates efficiently, particularly in the 4-phase operating mode, crucial for adiabatic computation. The depiction of an operational range, derived from a synthesis of experimental findings and a MATLAB model of the gates, provides information about the specific voltage thresholds necessary for optimal device performance. Furthermore, the inverter gates have been successfully operated at elevated temperatures of up to 450°C, affirming their robustness and capacity to withstand harsh environmental conditions.

Furthermore, the geometry of the CACL NAND gates, which were introduced in the previous chapter, underwent testing in the 4-phase operating mode, successfully confirming NAND behavior. The dual-rail architecture of these gates allows for the electrical rerouting of the input and output signals and therefore realization of AND, OR and NOR gates, with exactly the same architecture. This proof-of-concept therefore opens a new range of possibilities for creating more complex digital circuits.

Finally, the transportation of a logic state within a cascade of ten concatenated devices was successfully demonstrated. As the devices in a cascade were inverter gates, the optical measurements observed successful inversion of the logic state between each two consecutive devices, as well as recovery of the state after signal attenuation.

5

Conclusion and prospects

Among the many challenges faced by society, energy consumption and the resulting emissions are among the most significant. The constant demand for innovation in the digital market pushes even further the requirements for longer battery life spans and more efficient information processing. The limitations of current technologies used in digital electronics, discussed in the first chapter, have inspired the development of a new computing paradigm compatible with ultra-low-power consumption. This paradigm, introduced in 2017, is based on MEMS variable capacitors. Research performed in the following years advanced this technology from a more developed concept, initially realized with gap-closing structures and later with comb-drive actuators. This thesis undertook a task to further develop this technology using a dual-rail (complementary) architecture.

The second chapter of the thesis introduced a new paradigm of logic gates utilizing flexible structures and variable MEMS capacitors arranged in a complementary setup, with comb-drive actuators being selected as strong candidates for proof-of-concept devices. The study included detailed capacitance modeling of comb-drive actuators using both analytical methods and Finite Element Method (FEM) simulations, particularly focusing on scenarios with minimal or even negative initial overlap between the fingers.

This near-zero overlap scenario was shown to be the most energy-efficient operating condition, where fringing electric fields cause a non-linear change in capacitance with displacement, leading to significant variations in electrostatic force. The FEM analysis provided a precise model of capacitance versus displacement, essential for accurate system-level modeling and design. Based on this model, the energetic profile of a basic variable capacitor was analyzed, identifying the optimal operating conditions and its sensitivity to variations in geometrical parameters. Using this component, we developed an inverter logic gate and simulated its ability to invert input logic states. The energy used during gate operation could be fully recovered by a reversible power supply and can be reduced by minimizing the device's overall size. Additionally, simulations demonstrated that the inverter gate could produce output voltages capable of driving subsequent gates.

The third chapter provided a comprehensive overview of the design stages of a MEMS-based inverter gate. Building upon the foundational concepts introduced in the previous chapter, the individual components of the inverter gate were designed using analytic and FEM methods. Additionally, the possible implementations of a NAND gate were proposed. Initial microfabrication tests on silicon wafers identified the optimal fabrication conditions, particularly for the photolithography step, which required careful tuning of the exposure dose and a focus offset. Pattern transfer into silicon was performed using the Bosch process. These tests also provided information about changes in component dimensions due to underetching, which was considered in designing the microfabrication mask. Various underetching compensations were tested, yielding different outcomes for fixed and variable capacitors. The change in dimensions was more prominent in variable capacitors due to the larger spacing between vertical surfaces of neighboring structures compared to the openings in fixed capacitors. An underetching compensation that provided the best compromise between the designed and realized dimensions was identified and used for fabricating the devices. The critical dimension of 0.5 µm in the design was at the resolution limit of the available equipment. This dimension was successfully transferred to a substrate with a thickness of 5 µm, ensuring an aspect ratio of 10 for all the comb structures within the whole inverter and NAND gates, which have a surface area of 0.3 mm^2. By carefully tuning the microfabrication process, we achieved successful exposure, etching, and release of individual devices with 1450 finger pairs, or 2900 individual fingers, while avoiding short circuits, sticking, or buckling. In a cascade of ten devices, the total number of successfully fabricated comb fingers was 29000, covering a 5 mm wide surface.

The fourth chapter presented the results of a comprehensive investigation into the correlation between voltage and displacement in comb-drives with near-zero overlap, highlighting the significant influence of geometric variations on device performance. Detailed experimentation and analysis demonstrated that the CACL MEMS inverter gate operates efficiently, particularly in the 4-phase operating mode crucial for adiabatic computation. The depiction of an operational range, derived from a synthesis of experimental findings and a MATLAB model of the gates, provides insights into the specific voltage thresholds necessary for optimal device performance. Furthermore, the inverter gates operated successfully at elevated temperatures up to 450°C, affirming their robustness and capacity to withstand harsh environmental conditions. Additionally, the CACL NAND gates were tested in the 4-phase operating mode, successfully confirming NAND behavior. As NAND gates are universal gates, they enable the construction of any other gate type using one or more of these devices. This proof-of-concept opens new possibilities for creating more complex digital circuits. Finally, the successful transportation of a logic state within a cascade of ten concatenated devices was demonstrated. The optical measurements observed successful inversion of the logic state between each pair of consecutive devices and the recovery of the state after signal attenuation, validating the feasibility of cascading such devices in pipeline operation.

This thesis concluded with the successful demonstration of the proof-of-concept of a dual-rail architecture of variable capacitors for digital data processing. The achieved results, including the functioning inverter and NAND gates as well as an operational pipeline, have opened up new and promising avenues for future development.

An AND gate ($\wedge$) can be realized using the same architecture as the proposed NAND gate by switching the Q and $\bar{Q}$ signals at the output. Moreover, using the identity $\neg(A \wedge B) = (\neg A) \vee (\neg B)$, the same architecture can be adapted to implement an OR ($\vee$) gate and, subsequently, a NOR gate by additionally switching the complementary outputs. These configurations could be experimentally verified in the near future, as the necessary devices are readily available.

The overall size (0.3 mm^2) and critical dimensions of the devices (0.5 µm) were determined by the resolution limit of the photolithography tool used. Initial tests aimed at reducing the size using an e-beam tool are also planned for the upcoming period. Downscaling of the devices would allow for increase of operating frequency, decrease of voltage signals and the energy invested in the coding.

Current commercial high-temperature electronics are seldom qualified for temperatures above 500 K, necessitating the placement of processing units far from sensors, resulting in degraded readout performance. In the long term, in-sensor computing using add-on MEMS on the same die as the MEMS sensor could be envisioned to address this challenge.

Finally, recent work has shown that a few MEMS devices can perform pre-processing tasks, such as gesture recognition [49]. Implementing the first layers of a neural network could be achieved by adjusting the combs and connections, enabling in-sensor AI edge computing.

A

MATLAB code used to calculate the capacitance of the comb-structure based on EFD approach

```
%C1 = Plate cap - constant
%C2 = Anchor: fringe, bottom terminal, upper terminal cap - constant
%C3 = Fringe capacitance from the sides of the last two fingers to
    the substrate
%C4 = Total bottom terminal capacitance from middle fingers to the
    substrate
%C5 = Total bottom terminal capacitance from the last fingers to the
    substrate
%C6 = Top terminal capacitance from the last fingers to the substrate
%C7 = Fringe, bottom and top terminal capacitance from finger tips to
     the substrate
%C8 = Fringe capacitance from the sides of the middle fingers
%C9 = Fringe capacitance between finger tips and the finger sides
%C10 = Terminal capacitance between finger tips and the finger tips
%C11 = Plate to plate capacitance
%C12 = Fringe capacitance from the sides of the middle fingers where
    there is overlap
%C13 = Fringe capacitance from the sides of the middle fingers where
    there is no overlap
%C14 =fringe capacitance between the bottom plates of the fingers

d=0.5e-6;
h=5e-6;
EPS0=8.9e-12;
h_box=2e-6;
N=60;
l=10e-6;
w=2e-6;
L=20e-6; % Length of the anchor
W=8e-6;  % Width of the anchor
```

```
x_anal=linspace(-5,5,1001)*1e-6;
S1=N*d*l+(4*N-3)*d*w;
S2=L*W;
EPSr=4.2;

% Fixed contributions, independent of the overlap
C1=EPS0/h_box*(S1+EPSr*S2);
C2=2*EPS0*(L/2+W)*2/pi*log(1+h/h_box)+2*EPS0*4/pi*(L/2+W)*log(2)+2*
    EPS0*4/pi*(L/2+W)*log(3/2);
C3=2*EPS0*l*2/pi*log(1+h/h_box);
C4=2*EPS0*4/pi*l*(N-1)*log(1+3*d/(2*(h_box)));
C5=2*EPS0*4/pi*l*1/2*log(2);
C6=2*EPS0*4/pi*l*log(3/2);
C7=N*EPS0*de*2/pi*log(1+h/h_box)+N*EPS0*d*log(2)*4/pi+N*EPS0*d*4/pi*
    log(3/2);
C8=2/pi*(N-1)*EPS0*l*log(1+9*(d/h_box)^2);

for i=1:length(x_anal)
    if x_anal(i)<-3*d/2
        C10(i)=(4*N-2)*EPS0*h*4/pi*log((abs(x_anal(i))+3*d/2)/(abs(
            x_anal(i))+d));
        C_anal(i)=C1+C2+C3+C4+C5+C6+C7+C8+C10(i);
    else if x_anal(i)<-d
        C9(i)=(4*N-2)*EPS0*h*2/pi*log(3*d/(2*abs(x_anal(i))));
        C10(i)=(4*N-2)*EPS0*h*4/pi*log(2*abs(x_anal(i))/(abs(x_anal(i
            ))+d));
        C_anal(i)=C1+C2+C3+C4+C5+C6+C7+C8+C9(i)+C10(i);
    else if x_anal(i)<0
        C9(i)=(4*N-2)*EPS0*h*2/pi*log(3/2);
        C10(i)=(4*N-2)*EPS0*h*4/pi*log(2*d/(d+abs(x_anal(i))));
        C_anal(i)=C1+C2+C3+C4+C5+C6+C7+C8+C9(i)+C10(i);
    else
        C9(i)=(4*N-2)*EPS0*h*2/pi*log(3/2);
        C10(i)=(4*N-2)*EPS0*h*4/pi*log(2);
        C11(i)=EPS0*x_anal(i)*(2*N-1)*h/d;
        C12(i)=2/pi*(N-1)*EPS0*x_anal(i)*log(1+(d/h_box)^2);
        C13(i)=2/pi*(N-1)*EPS0*(l-x_anal(i))*log(1+9*(d/h_box)^2);
        C14(i)= 2*2*(N-1)*EPS0*x_anal(i)*1/pi*log(2);
       C_anal(i)=(C1^2+C14(i)^2)/(C1+C14(i))+C2+C3+C4+C5+C6+C9(i)+C10
           (i)+(C11(i)^2+C12(i)^2)/(C11(i)+C12(i))+C13(i);
    end end end end
```

B

Image processing

```
%Var1 Pixel number
%Var2 Distance in um
%Var3 ... VarN   Data frames
%
%This version was improved from imageJ file by measuring the
%displacement relative to the anchor

clc
clear all
close all

addpath(genpath('... DataPath ...'))
To = readtable('TableName.csv');

%Individual for each measurement, has to be chosen manually
a=82;
b=113;
c=140;
d=186;

w=width(To);       %number of frames+24
h=height(To);      %the length of the line +1 --> plot width +12
T = To(10:50,1:w); %cutting out the window of interest
T=table2array(T);
E = To(end-30:end,1:w);
E=table2array(E);
N_frames = w-2;

for i = 3:w
TT(:,i) = medfilt1(T(:,i), 3);      %smooth(table2array(T(:,i)));
I_max(:,i) = islocalmax(TT(:,i));   %gives the position of the local
```

```
   maxima
EE(:,i) = medfilt1(E(:,i), 3);
I_min(:,i) = islocalmin(EE(:,i));
end

%Extracting beam position for each frame
for i = 3:w
        index(i) = find(I_max(:,i), 1, 'first');
        position_beam(i) = T(index(i), 2);
        intensity(i) = T(index(i),i);

        index_fix(i) = find(I_min(:,i), 1, 'first');
        position_fix(i) = E(index_fix(i), 2);

        position(i) = -position_fix(i)+position_beam(i);
end

displacement = position-position(67);

figure(1)
plot(1:N_frames, displacement(3:w))
xlabel('Frame number', 'FontSize', 14, 'fontweight', 'bold')
ylabel('Displacement (um)', 'FontSize', 14, 'fontweight', 'bold')
box on
grid off

%Polynomial fitting of the peak for each frame
for i = 3:w
        for j=1:7
                x_discrete(j)=T(index(i)-4+j, 2);
                x_fixation(j)=E(index_fix(i)-4+j, 2);
                int_discrete(j) = T(index(i)-4+j,i);
                int_fixation(j) = E(index_fix(i)-4+j,i);
        end

        [p_cont, S_p] = polyfit(x_discrete, int_discrete,2);
        x_inter=linspace(x_discrete(1), x_discrete(7));
        int_inter=polyval(p_cont,x_inter);

        pos_cont(i-2)= -p_cont(2)/(2*p_cont(1));
        int_cont(i-2)=-p_cont(2)^2/(4*p_cont(1))+p_cont(3);

        [p_fix, S_f] = polyfit(x_fixation, int_fixation,2);
        x_inter_fix=linspace(x_fixation(1), x_fixation(7));
        int_inter_fix=polyval(p_fix,x_inter);
```

```
        pos_cont_fix(i-2)= -p_fix(2)/(2*p_fix(1));
        int_cont_fix(i-2)=-p_fix(2)^2/(4*p_fix(1))+p_fix(3);

        pos_smooth = pos_cont - pos_cont_fix;

end

%Adjusting the zero, has to be chosen manually for each measurement
displacement_smooth = -(pos_smooth - pos_smooth(56));

figure(2)
f = figure;
f.Position = [100 100 1040 150];
hold all
plot(1:N_frames,(displacement_smooth))
xlabel('Frame number', 'FontSize', 14, 'fontweight', 'bold')
ylabel('Displacement (um)', 'FontSize', 16, 'fontweight', 'bold')
set(gca, 'FontSize', 15)
box on
hold off

max_displacement = mean(displacement_smooth(a:b))-mean(
   displacement_smooth(c:d));
```

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Scientific contributions

Journal publications

A. Marković, M. Lefebvre, L. Mazenq, S. Charlot, M. Gély, M. Arribat, G. Jourdan, and B. Legrand, Suspended tip overhanging from chip edge for atomic force microscopy with an optomechanical resonator*, J. Opt. Microsyst.* **4**(3), 033501, 2024, doi: 10.1117/1.JOM.4.3.033501.

Marković A, H. Fanet, G. Pillonnet, B. Legrand, Behavior analysis of comb-drive actuators operating in near-zero-overlap configuration, *Sensors and Actuators A: Physical*, Volume 376, 2024, 115652, ISSN 0924-4247, https://doi.org/10.1016/j.sna.2024.115652.

M. Rostami, **A. Marković**, Y. Wang, J. Pernollet, X. Zhang, X. Liu, J. Brugger, Multi- and Gray-Scale Thermal Lithography of Silk Fibroin as Water-Developable Resist for Micro and Nanofabrication. *Adv. Sci.* 2024, 11, 2303518. https://doi.org/10.1002/advs.202303518.

Publications in conference proceedings

A. Marković, L. Mazenq, A. Laborde, H. Fanet, G. Pillonnet, B. Legrand. Adiabatic logic gates for ultra-low-power operation using contactless capacitive MEMS. 22nd International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers), Jun 2023, Kyoto, Japan. pp.546-549. ⟨hal-04241697⟩

A. Marković, L. Mazenq, A. Laborde, H. Fanet, G. Pillonnet and B. Legrand, Ultra-Low-Power Logic with Contactless Capacitive MEMS, *2022 21st International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS)*, Salt Lake City, UT, USA, 2022, pp. 223-227, doi: 10.1109/PowerMEMS56853.2022.10007572.

A. Markovic, G. Pillonnet, B. Legrand. Towards near-zero-power logic gates based on capacitive MEMS devices operating in adiabatic regime. Workshop nano, meso, micro: Science and innovation for radio and photonics, International Union of Radio Science, URSI France JS22, URSI, Mar 2022, Paris, France. ⟨hal-03649053⟩

Conference and workshop presentations

Poster presentation at 38st International Conference on Micro Electro Mechanical Systems (IEEE MEMS), Jan 2025, Kaohsiung, Taiwan.

Oral presentation at 22nd International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers), Jun 2023, Kyoto, Japan.

Invited talk at Nonlinear Micro/Nanosystems Symposium, May 2023, Grenoble, France.

Poster presentation at 21st International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS), Dec 2022, Salt Lake City, United States.

Poster presentation at 2022 Advanced Manufacturing for Energy and Transportation International Summer School (AMETIS), June 2022, Taglio, Corse, France.

Oral presentation at the Workshop nano, meso, micro: Science and innovation for radio and photonics, International Union of Radio Science, URSI France JS22, URSI, Mar 2022, Paris, France.

Patents

D. Foresti, **A. Markovic**, J. A. Lewis**,** Subwavelength resonator for acoustophoretic printing, Publication number: 20220176694, Candidate: President and Fellows of Harvard College.

Awards

Best poster award at the 21st International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS 2022) in Salt Lake City, Utah (USA).

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Titre : vers des portes logiques ultra-basse consommation basées sur des mems capacitifs sans contact opérant en régime adiabatique

Mots clés : Logique adiabatique, MEMS, Capacités variables, micro et nanotechnologie, actionneurs à peigne

Résumé : Cette thèse se concentre sur le développement d'un dispositif MEMS pour permettre aux composants électroniques ultra-basse consommation de fonctionner sans contact. Elle aborde les problèmes des technologies actuelles comme les courants de fuite, les pertes d'énergie dynamiques dans les MOSFETs et la dégradation des contacts dans les micro-relais. La première partie examine l'état des circuits numériques, mettant en lumière les contraintes technologiques des transistors MOSFET et des micro-relais, avant de proposer un dispositif sans contact fonctionnant en régime adiabatique avec une architecture de condensateur variable.

Le cœur de la thèse détaille la conception d'une porte inverseuse à logique adiabatique capacitive (CACL) avec une architecture à double rail utilisant des structures à entraînement à peigne. Des analyses analytiques et par méthode des éléments finis (FEM) déterminent les paramètres de conception optimaux. Les facteurs tels que la longueur, la largeur, l'épaisseur des doigts de peigne, l'écart entre eux et leur nombre sont étudiés pour leur impact sur les capacités et la force induite entre les peignes. L'analyse couvre aussi les amplitudes de déplacement pour coder les états logiques et la sensibilité des positions stables du dispositif MEMS aux variations géométriques.

La thèse décrit les étapes de conception et de fabrication des structures logiques MEMS, y compris les composants individuels comme les chemins conducteurs, les ressorts, les peignes d'entrée et de sortie, et les condensateurs fixes. Elle aborde également les structures de test pour évaluer la performance des composants et les différentes implémentations d'une porte NAND. Le processus de fabrication, débutant par des tests sur des substrats de silicium pour identifier les conditions optimales, est détaillé jusqu'à la fabrication finale des portes logiques MEMS sur des substrats de silicium sur isolant (SOI).

La dernière partie présente une étude approfondie de la corrélation entre la tension et le déplacement des peignes avec un chevauchement quasi nul, soulignant l'importance des variations géométriques sur la performance du dispositif. Des expérimentations et analyses montrent l'efficacité de la porte inverseuse CACL MEMS, particulièrement en mode de fonctionnement à 4 phases. Les résultats fournissent des seuils de tension pour une performance optimale. Les portes inverseuses fonctionnent à des températures allant jusqu'à 200°C, prouvant leur robustesse. La géométrie des portes NAND CACL, testée en mode à 4 phases, confirme le comportement NAND, permettant la construction de circuits numériques complexes.

La thèse se conclut par la démonstration du transport des états logiques à travers une cascade de dix dispositifs concaténés, avec des mesures optiques confirmant l'inversion précise des états logiques. Cette recherche représente une avancée significative pour les dispositifs électroniques ultra-basse consommation et sans contact, améliorant la performance, réduisant la consommation d'énergie et prolongeant la durée de vie des composants électroniques.

Title: towards ultra-low-power logic gates based on contactless capacitive mems operating in adiabatic regime

Key words: Adiabatic logics, MEMS, Variable capacitances, micro and nanotechnologies, comb-drive actuators

Abstract: This thesis details the development of a MEMS-based device aimed at enabling ultra-low-power electronics to operate in a contactless manner. This innovative approach addresses common issues in existing technologies, such as leakage currents, dynamic energy losses in MOSFETs, and contact degradation in micro-relays. The initial part of the thesis reviews the current state of digital circuits, particularly focusing on MOSFET transistors and micro-relays, and highlights their technological constraints. This sets the stage for introducing a contactless device capable of operating in an adiabatic regime, presenting a variable capacitor architecture as a promising solution.

The core of the thesis explores the design of a Capacitive Adiabatic Logic (CACL) inverter gate, featuring a dual-rail architecture realized through comb-drive structures. This design aims to minimize energy consumption while considering technological constraints. Comprehensive analytical and finite element method (FEM) analyses of the comb-drive structures inform the optimal design parameters. Factors such as the length, width, and thickness of the comb fingers, the gap between them, their overlap, and their number are analyzed for their impact on the variable, fixed, and parasitic capacitances of the actuator, as well as the induced force between the combs. Additionally, the analysis covers achievable displacement amplitudes essential for encoding logic states and examines the sensitivity of the MEMS device's stable positions to geometric variations.

The thesis also details the stages involved in designing and fabricating the MEMS logic structures, building on the differential capacitive design. It covers the design process for individual components, including conducting paths, springs, input and output combs, and fixed capacitors. Test structures used to evaluate component performance within the inverter gate are described, along with different implementations for a NAND gate. The fabrication process, beginning with initial microfabrication tests on silicon wafers to identify optimal conditions and account for dimensional changes due to underetching, is thoroughly detailed, culminating in the final fabrication of full MEMS logic gates on silicon-on-insulator (SOI) wafers.

The final part of the thesis presents a comprehensive investigation into the correlation between voltage and displacement in combs with near-zero overlap, emphasizing the significant influence of geometric variations on device performance. Detailed experimentation and analysis demonstrate the efficiency of the CACL MEMS inverter gate, particularly in the 4-phase operating mode crucial for adiabatic computation. The operational range, derived from experimental findings and a MATLAB model of the gates, provides specific voltage thresholds for optimal performance. Furthermore, the inverter gates have been successfully operated at temperatures up to 200°C, affirming their robustness and ability to withstand harsh conditions. The geometry of the CACL NAND gates, tested in the 4-phase operating mode, successfully confirmed NAND behavior, which opens the door to constructing any other gate type using one or more of these devices, enabling the creation of complex digital circuits.

The thesis concludes by demonstrating logic state transportation across a cascade of ten concatenated devices, with optical measurements confirming accurate logic state inversion between each pair of consecutive devices. This research represents a significant advancement in developing ultra-low-power, contactless electronic devices, addressing limitations of current technologies, and proposing a novel MEMS-based solution. This innovation is critical for enhancing performance, reducing energy consumption, and extending the lifespan of electronic components, thus paving the way for more efficient, durable, and versatile electronics.