Low bandgap nanostructures and topological materials for quantum computing and spintronic applications

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Habilitation à Diriger les Recherches

Low Bandgap Nanostructures and Topological Materials for Quantum Computing and Spintronic Applications

Soutenue le 12 Novembre 2024 par

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Preamble and structure of the manuscript:

Summarizing more than twenty years of research that are driven by curiosity, projects, collaborations and different opportunities is a challenge that requires choices. In this manuscript, I decided to only present results obtained between 2009 and 2024 that are directly linked to my CNRS project and the new research areas that I developed afterwards.

I obtained my engineering degree from the ENSPG school (currently Phelma) in 2003, with a specialization in physics and instrumentation. The same year, I also received an advanced study diploma (DEA) from the Grenoble Institute of Technologies (INPG) in optics, optoelectronic and microwaves. Between 2003 and 2007, I worked during my PhD at the CEA Grenoble focusing on the p-doping of the HgCdTe by molecular beam epitaxy (MBE) under the supervision of Philippe Ballet and Engin Molva. In 2008, I moved to the IEMN laboratory (Epiphy group), to work with Xavier Wallart, Ludovic Desplanque and Philippe Caroff on the growth of antimonide-based metamorphic buffer layers for optical amplifiers and the synthesis of III-V nanowires by MBE. In 2010, I got a post-doctoral position at the Technical University of Eindhoven (TU/e) collaborating with the group of Prof. Erik Bakkers on the growth of high mobility III-V nanowires by metalorganic vapor phase epitaxy (MOVPE), in collaboration with the group of Prof. Leo Kouwenhoven from the Technical University of Delft (TU/D). Finally, in December 2013, I joined the LAAS-CNRS laboratory in Toulouse as a senior independent scientist (CR2 CNRS).

The structure of this manuscript is thus influenced by these different research experiences and is divided in four chapters:

- The first chapter deals with the integration of III-V nanowires on silicon for nanoelectronics applications. This activity, that I started during my stay at IEMN (2009), is the core of my CNRS project. It benefited from the work of two master's students and a doctoral student at my arrival in Toulouse. This activity has persevered despite various challenges over the years.
- The second research theme is focused on the development of high mobility III-V nanowires and hybrid interfaces for quantum computing. This activity started mostly at my arrival at TU/e (2010), and reached its peak in 2016. Two PhD and one master students were involved in this topic.
- The third area or research concerns the development of novel topological materials for applications in quantum computing and spintronics. It was mainly motivated by the limits of the materials developed in the second chapter of this document and by the emergence of this new class of materials. This activity, which I started in 2017, constitutes today my main research area and has benefited from the work of two doctoral, three post-doctoral and a master's students.

- Finally, the last chapter of this manuscript is focused on the perspectives linked to the topological materials and their integration into hybrid interfaces with superconductors or ferromagnets. This new opportunity was made possible by the start of EpiCentre, a joint laboratory between Riber SA and the LAAS-CNRS, in 2021: (https://epicentre.cnrs.fr/en/). I belong to both the steering comity and the supervision board of EpiCentre and I am the responsible of the advanced material research axis.

Several annexes are added at the end of the manuscript that include a CV, a list of publications, conferences and expertise; the supervised students and their topics, the different projects funded along the years and the bibliographic references.

Abbreviation list:

ARPES – angular resolved photoemission spectroscopy
BEOL – back end of line
BEP – beam equivalent pressure
BL – buffer layer
BST – BiSbTe
BSTS – BiSbTeSe
BTS – BiTeSe
CBE – chemical beam epitaxy
CMOS – complementary metal-oxide-semiconductor
DFT – density functional theory
DRAM – dynamic random access memory
FET – field effect transistor
FFT – fast Fourier transform
FL – free laer
FM – ferromagnet
GAA – gate all around
HAADF – high-angle annular dark-field
JJ – Josephson junction
MBE – molecular beam epitaxy
ML – magnetic layer
MOVPE –metalorganic vapor phase epitaxy
MRAM – magnetic random access memory
MTJ – magnetic tunnel junction
MZM – Majorana zero mode
NID – non-intentionally doped
NW – nanowire
PMA – perpendicular magnetization anisotropy
QEC – quantum error correction
RHEED – reflection high energy electron diffraction
RKKY – Ruderman–Kittel–Kasuya–Yosida
RL – reference layer
SAF – synthetic antiferromagnet
SEM – scanning electron microscopy
SOI – spin orbit interaction
SOT – spin orbit torque
SRAM – static random access memory
STT – spin transfer torque
TEM – transmission electron microcopy
TMR – tunnel magnetoresistance
TI – topological insulator
VLS – vapor liquid solid
VS – vapor solid
WZ – wurtzite
XRD – X-ray diffraction
ZB – zinc-blend

Chapter 1:
High mobility III-V nanowires for nanoelectronics

1.1 Context and working method

We live in the "Information Age", which according to the sociologist Manuel Castells corresponds to the time that large amounts of information are widely available to many people[1]. This fundamental change in our societies is intimately linked to the development of computer technologies. From the first transistors developed in 1947 by John Bardeen, Walter Brattain and William Shockley in the Bell Labs to the latest generation of smartphones, more than 75 years of microelectronic changed our vision of the world. If the "Moore's law" has driven the industry for more than 50 years[2], silicon chips are reaching their fundamental physical limits. Indeed, as chips are getting smaller, the insulating films cannot prevent short circuit anymore. Moreover, the amount of heat generated by the electrical currents flowing through the miniaturized transistors is sufficient to cause meltdown, if not sunk correctly. Since 2013, the International Technology Roadmap for Semiconductors (ITRS) highlights the power management as main issue for continued miniaturization[3], which was later confirm by the International Roadmap for Devices and Systems (IRDS). Ongoing research efforts on new material integration into silicon chips may result in one or two generations of smaller transistors using high-dielectrics, high mobility materials or new architectures, but further improvements in performance require a fundamentally different approach such as integration of 3D architectures *(**chapter 1**)*, new paradigms such as quantum computing *(**chapter 2**)* and spintronics devices *(**chapter 3**)*.

The development of new materials, adapted to the quantum physics paradigms, is thus crucial. The graphene material is a perfect example of this evolution which must include a holistic approach. Materials are no longer considered as imperfect entities that must be dealt with, but represent real opportunities for developing new concepts. In my different studies, I have tried as much as possible to follow this approach; from the synthesis of high-quality nanoscale materials, to their structural and electrical characterizations and their engineering in heterostructures and hybrid interfaces.

1.2 The nanowires: definition, advantages and growth modes

Electronic and optoelectronic devices commonly developed nowadays employ top-down approaches based on the silicon technology. Improved performances are mostly obtained from scaling down feature sizes. As this silicon-based approach is reaching its physical limits, the development of new nanomaterials that integrate the combined advantages of both bottom-up and top-down technologies arise thus as a key technology for the future of nanodevices. In this context, nanowires (NWs) have emerged as one of the most promising platforms to develop devices for both fundamental and applied physics leading for example to

breakthroughs in quantum physics[4], spintronics[5], mesoscopic physics[6], biological sensing[7] and energy nanogenerators[8]. These objects are one-dimensional (1D) nanostructures, whose diameter is measured in few tens of nanometers (nm) and length in few microns (µm). Their surface-to-volume ratio is high compared to their 2D counterparts. Their biggest advantage lies in their 1D geometry that can withstand high strain, and allows fabrication of defect-free structures with high crystalline quality. This enables the manipulation of their inherent properties, rendering them highly suitable for pioneering advancements in nanoelectronics. Furthermore, since the nanowire diameter can be smaller than the Bohr radius, quantum mechanical properties start to become prominent, which makes them ideal experimental tools for exploring the quantum world. Finally, the large number of synthesis options available (MBE, MOVPE, CBE, liquid phase, etc.) explains why this area has become the frontier of many multidisciplinary research themes.

So far, the bottom-up NW synthesis has been the most studied since it allows the combination of materials previously incompatible both axially and laterally (**figure 1**). Among the different possibilities, III-V based materials benefit from the most interesting intrinsic properties such as direct bandgaps, high mobilities, and large wavelength coverage. In addition, it has been shown that good control can be obtained over the dimension, morphology, position, material combination and crystalline structure for nanowires based on this semiconductor family. Unfortunately, their integration on silicon and their combination with the CMOS technology suffer two major drawbacks: they are mostly grown using a gold catalyst which creates detrimental mid-gap defect states in silicon and their growth direction is <111>, in most of the case, which is incompatible with the CMOS technology.

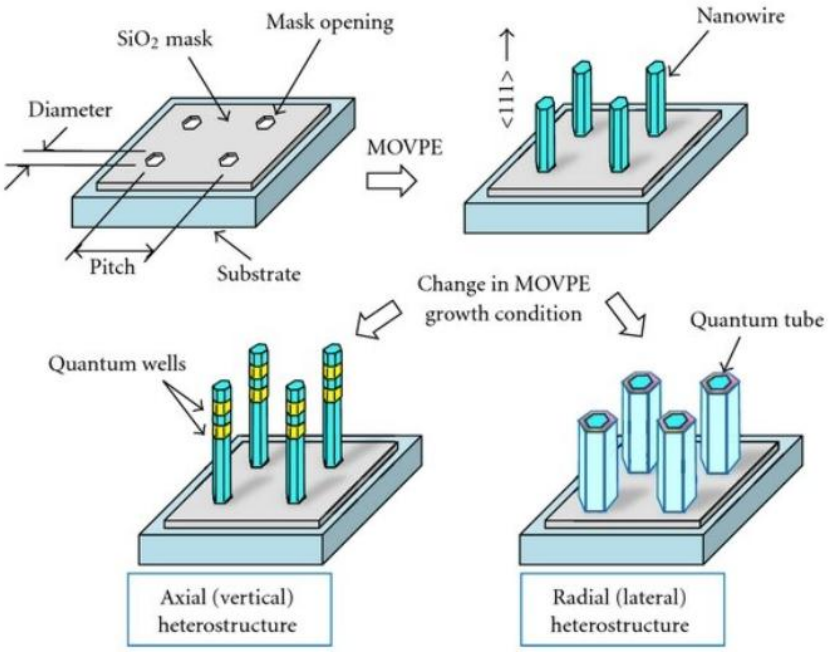


Figure 1: Example of nanowire heterostructures

Historically, the first report of crystalline structures looking like nanowires dates back to 1964 when Wagner and Ellis from the Bell Telephone Laboratory used the Vapor-Liquid-Solid (VLS) mechanism (figure 2) to grow single crystalline Si whiskers[9]. It was however only in the mid-1990s that the group of Prof. K. Hiruma, from Hitachi in Japan, synthesized the first III-V nano whiskers[10]. As their diameter decreased over subsequent years, they were eventually renamed as "nanowires". The VLS growth mechanism involves the deposition of a metallic droplet before growth that serves as a physical or a chemical catalyst. These nanoparticles modify the surface chemical potential and thus allow the collection of materials. They are a key ingredient for promoting nanowire nucleation and then the vertical growth. The most widely used metal to act as a catalyst is gold since it does not oxidize in air, and forms eutectic alloys with a lot of materials: Ge, Si, In, Ga, Al, Zn ... etc. In addition, it is possible to control the size and the density of nanoparticles by either using gold colloids or dewetting of a thin gold layer. Despite the high degree of control over nanowire morphology and density that Au mediated growth offers, it is prohibited for some applications such as nanoelectronics. Indeed, gold is a deep level impurity in silicon, creating mid-gap defects in the band structure, and thus degrading the electrical and optical device properties. Therefore, two options are possible for growing CMOS compatible III-V nanostructures on silicon: either using a self-catalyzed growth mechanism or using a third-party metal catalyst compatible with CMOS such as Ag, Pt, or Pd. Furthermore, the self-catalyzed growth can either be assisted by a droplet, where an element III (Ga or In) takes the role of gold, or can occur thanks to a Vapor-Solid or a Selective-Area growth process. In the former case, metallic droplets are deposited in-situ prior to nanowire growth, whereas in the latter case substrates can be pattern beforehand.

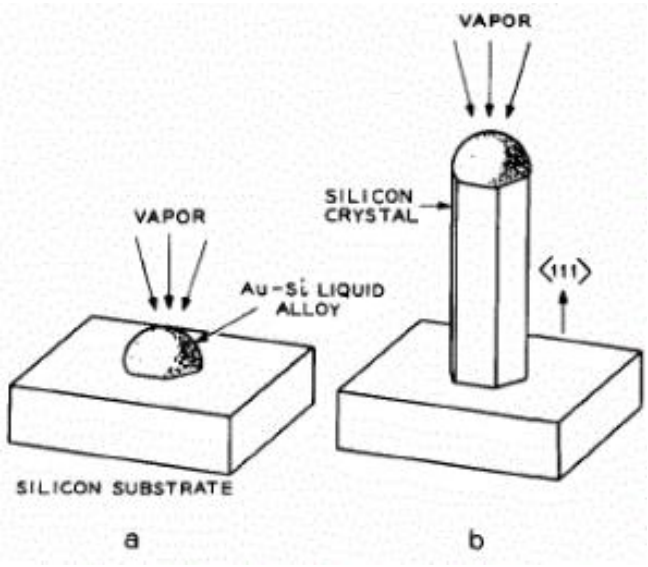


Figure 2: Growth of a silicon crystal by VLS.
***(a)** Initial conditions with liquid droplet on substrate.*
***(b)** Growing crystal with liquid droplet at the tip.*

1.3 The gate-all-around geometry and the III-V materials

Since 1947, the transistor architecture has evolved significantly from planar geometries to 3D ones. An example of this evolution is given in **figure 3** for the field effect transistor (FET) family.

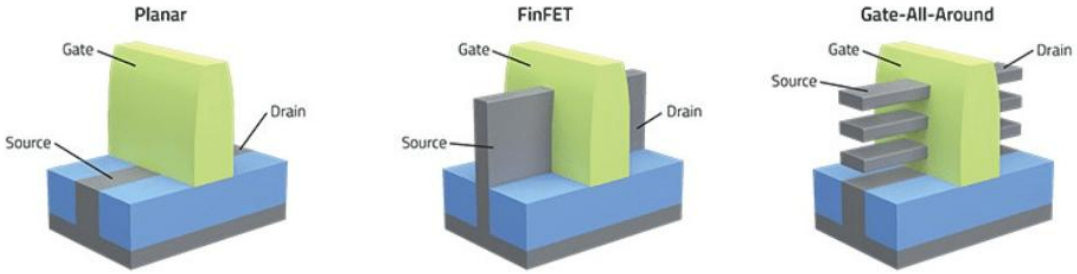


Figure 3: *Planar transistors vs. finFETs vs. gate-all-around.*

In these devices, the current flowing in the channel is controlled electrostatically by the gate voltage. The device performances are thus directly dependent of the insulating layer quality between the gate and the channel. Initially, planar FETs featured a simple flat channel, but as transistors shrunk in size, it became harder to control the channel effectively. FinFETs came next, introducing a 3D fin-shaped channel that improved gate control by wrapping the gate around the fin. However, the most advanced design, the gate-all-around (GAA) FETs, takes it a step further by surrounding the channel entirely with the gate. This design offers superior control, reducing leakage and enhancing efficiency. Essentially, GAA-FETs promise better performance, lower power consumption, and increased reliability compared to older designs, marking a significant leap forward in semiconductor technology. The horizontal configuration presented in **figure 3** can be advantageously converted into a vertical one using high mobility III-V nanowires as a channel (**figure 4**)[11].

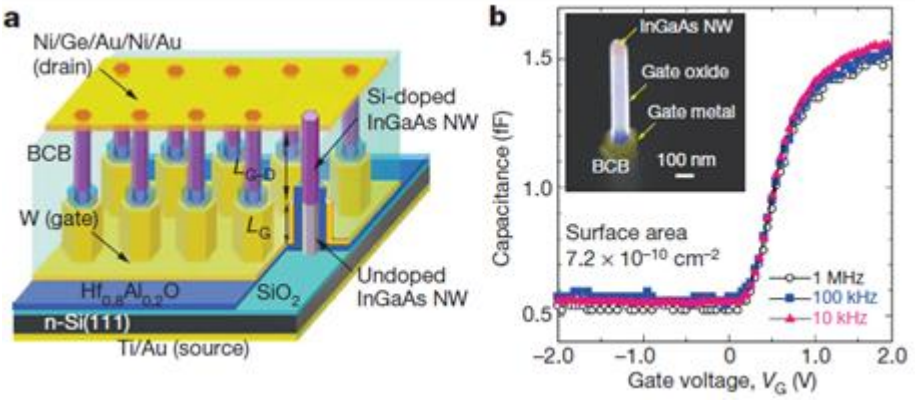


Figure 4: ***(a)*** *Example of a GAA-FET containing ten NWs connected in parallel with the drain metal.* ***(b)*** *Capacitance/gate voltage curves of the device. The sample has 250 nanowires aligned in parallel. The capacitance indicated is that for a single wire. Inset is a representative SEM image showing the GAA-FET structure.*

When selecting materials for integration onto silicon, criteria include superior intrinsic properties, comply with industrial standards, and be readily accessible. Figure 5 illustrates the lattice parameters and energy bandgaps of conventional II-VI and III-V semiconductors. Both semiconductor families offer distinct advantages in nanoelectronics applications. While II-VI materials excel in optical and high-speed electronic devices, III-V semiconductors shine in applications requiring high electron mobility and compatibility with silicon substrates. The choice between these semiconductor families ultimately depends on the specific requirements of the target nanoelectronics application, balancing performance, cost, and integration feasibility.

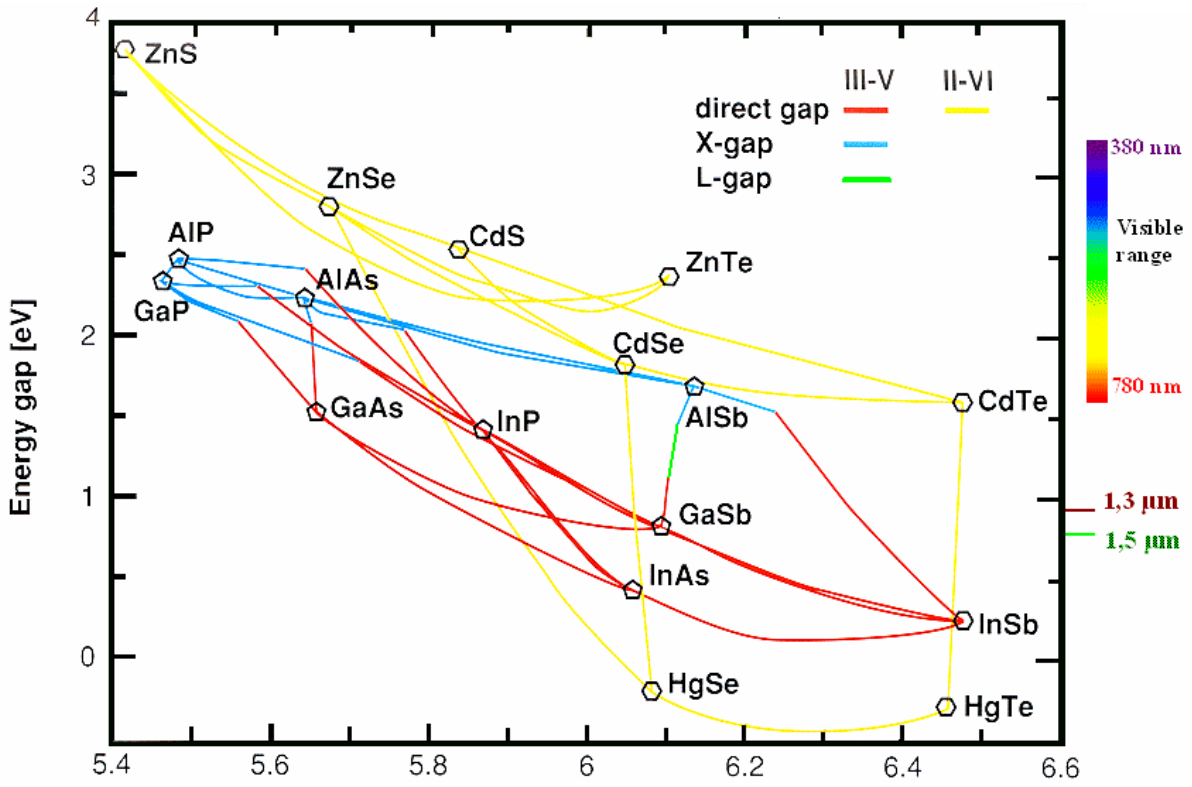


Figure 5: Band gap energies and lattice parameters of classical II-VI and III-V semiconductors.

In our context, III-V materials, and more specifically binary InAs and InSb semiconductors stand out for having the highest electron mobilities, with values of 40000 $cm^2V^{-1}s^{-1}$ and 77000 $cm^2V^{-1}s^{-1}$, respectively, at 300K. Their large Lande g-factor (>10) makes them exceptionally well-suited for nanoelectronics, quantum computing, and spintronics devices. Nonetheless, their widespread adoption in bulk and 2D devices has been impeded by a critical challenge: their substantial lattice mismatch with standard substrates. Here, nanowires offer a promising solution by releasing strain on the sidewalls, thereby facilitating the direct integration of these materials onto silicon. Another promising material for GAA-FETs is GaAs since ultra-high-mobility 2D electron systems are reported in GaAs-AlGaAs interfaces[12]. Embracing a core-shell geometry opens thus the possibility of directly growing these heterostructures on silicon.

In the following sections, I will elaborate on the strategies we developed to integrate these materials (GaAsSb, InAsSb) onto silicon substrates. Given that the prevailing direction for nanowire growth is (111)B, we opted for Si(111) wafers.

1.4 The integration of GaAs nanowires on silicon by MBE [13–17]

1.4.1 Influence of the growth parameters on the nanowire shape

When we started working on growing gold-free nanowire on Si(111) substrates, only a few groups had already reported this possibility[18,19]. We chose to start with GaAs nanowires because they are catalyzed using gallium droplets, unlike those of InAs. The presence of a metallic particle on the silicon surface decreases locally the chemical potential, helping nucleation and growth of nanowires. The first parameters we studied were the influence of the growth temperature and the native oxide / oxide-free substrate termination on the GaAs nanowire shape, keeping all other parameters the same (figure 6).

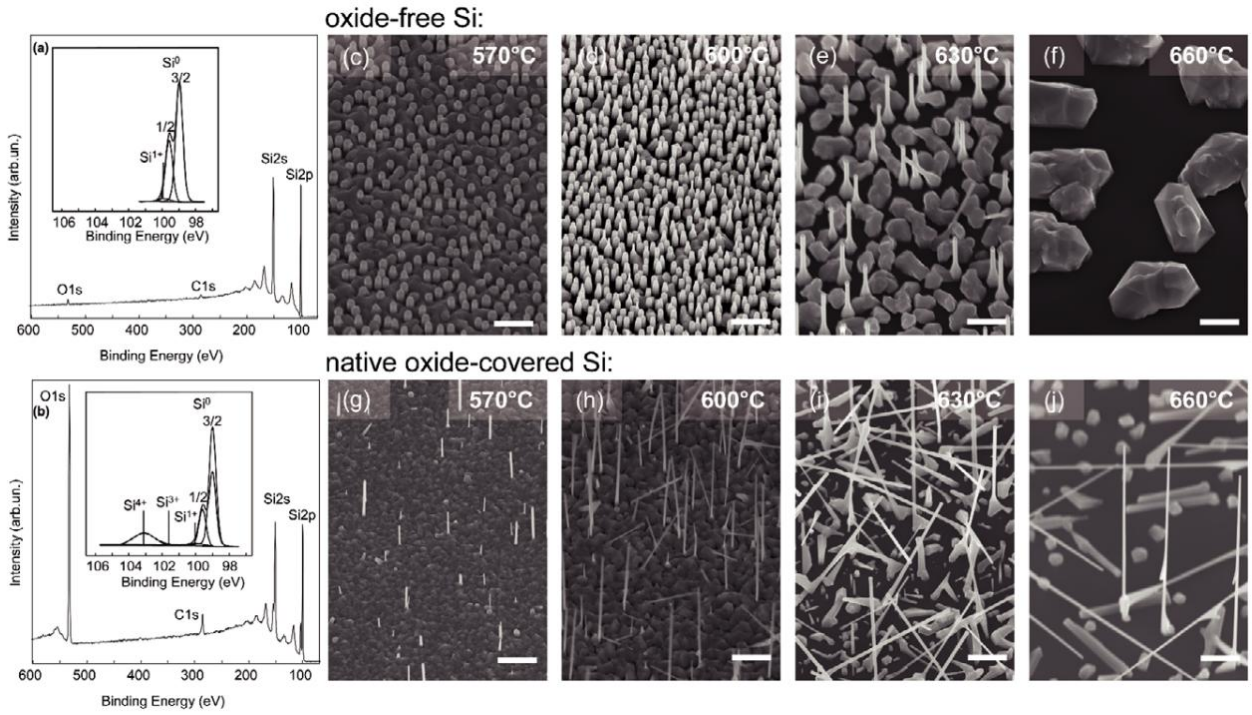


Figure 6: (a) Widescan XPS spectra of the oxide-free and oxide-covered substrates (b) with insets showing high resolution Si 2p core level decompositions. The SEM images (tilt 30°, scale bar 1 µm) show the evolution of nanowire morphology as a function of temperature for oxide-free ((c)–(f)) and native oxide-covered Si ((g)–(i)) substrates. Nanowires shown for each temperature are grown in the same run at each temperature on oxide-free and native oxide-covered.

Our first observation was to establish a growth window for GaAs nanowires, between 570°C and 630°C. Interestingly, we noted that nanowires could grow indiscriminately on oxide-free or oxide-covered silicon wafers (< 2nm). This phenomenon was later explained by the reaction between metallic gallium and the native oxide at the substrate surface:

$$Ga + SiO_x \Rightarrow GaO_x + Si$$

This reaction creates etch pits in the SiO_x layer, which allow nucleation of vertical nanowires.

Next, we studied the influence of the V/III ratio on the nanowire morphology at the optimized temperature of 630°C (**figure 7**). This temperature corresponds to the highest one preventing large material re-evaporation, and also limits the parasitic 2D growth.

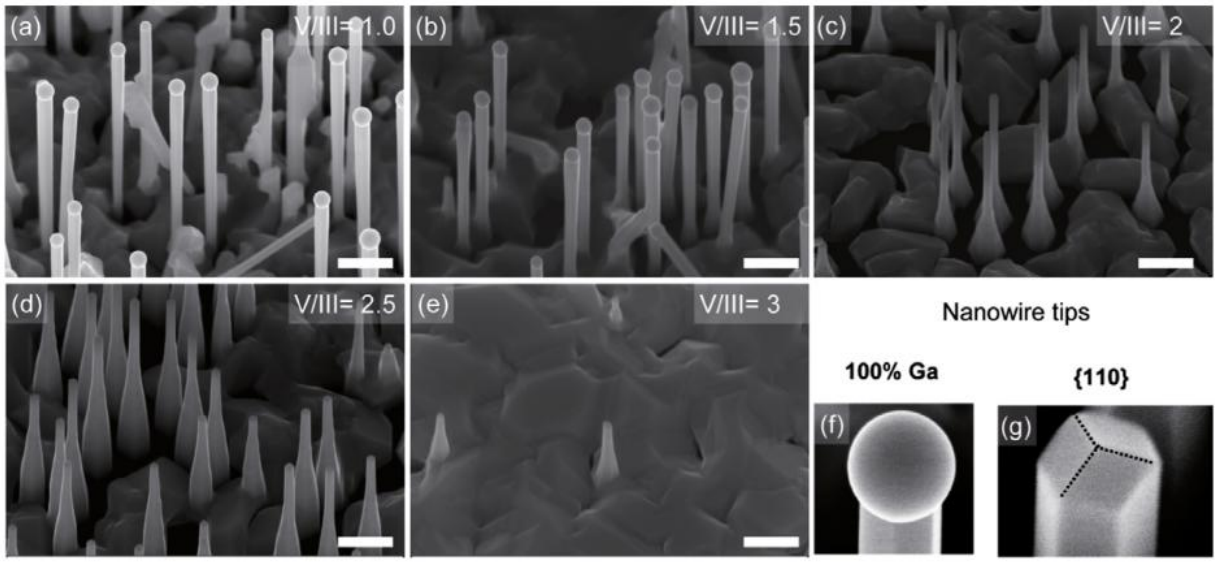


Figure 7: ***(a)–(e)*** *Evolution of nanowire morphology at 630 ◦C under increasing V/III ratio for growth on oxide-free Si(111). Growth time is constant for all samples.* ***(f)–(g)*** *Higher magnification of a nanowire tip representative of* ***(a)*** *and* ***(b)*** *and* ***(c)–(e)****, in* ***(f)*** *and* ***(g)*** *respectively.*

Interestingly, for a nominal V/III ratio of 1, nanowires have an inverse tapered shape with the top wider than the bottom. By increasing the arsenic flux, the diameter becomes homogeneous over the whole length. In **figure 7c,d**, nanowires are tapered, with a wider base and smaller top diameter. In **figure 7(e)** the density of nanowires is low and mostly only bulk 2D growth is observed. The V/III ratio has thus a crucial influence on the nanowire shape, and a fine tuning of this parameter is mandatory to grow optimized nanostructures. Note that it is also possible to "keep alive" or "kill" the gallium droplet at the nanowire tip by changing the cooling down conditions after growth as shown in **figure 7f,g**.

1.4.2 Patterning of the substrate and control of the nucleation

After further optimizations of the nanowire geometry in order to enhance their aspect ratio, we tried to force the nucleation at precise positions on the wafer. This technological step is mandatory in order to create vertically integrated GAA-FETs, since these devices contain generally several nanowires in parallel. Following numerous attempts, we developed the following optimal technological steps: **(i)** an array of holes is defined in a SiO_x layer deposited on the Si(111) wafer thanks to electron beam lithography and wet etching, **(ii)** gallium droplets are deposited in-situ prior to growth to match the hole diameters and **(iii)** the GaAs nanowire growth is optimized to achieve the highest aspect ratio. An optimized process is presented in **figure 8**.

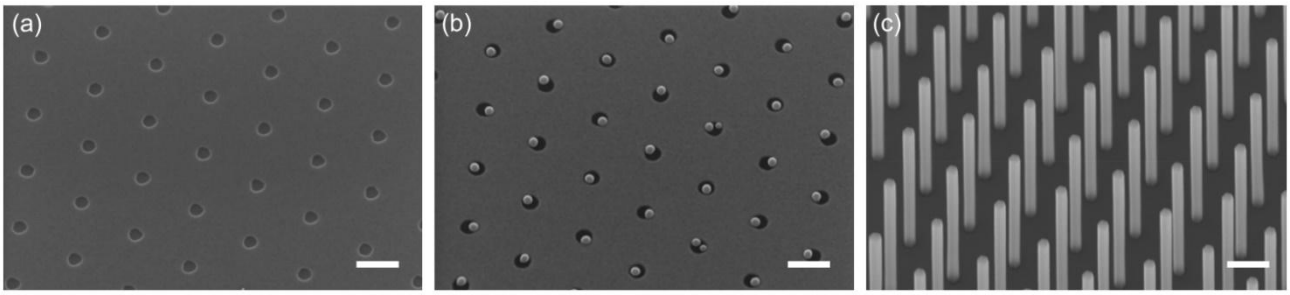


Figure 8: ***(a)*** *hole array defined into the dielectric layer on an Si(111) substrate using electron beam lithography and etching,* ***(b)*** *gallium droplets formed in situ prior to the nanowire growth, with controlled diameter to fit into the holes and* ***(c)*** *GaAs nanowire array growth assisted by Ga droplets in a vapor–liquid–solid growth mechanism. The scale bar corresponds to 200 nm.*

Several comments can be made regarding the optimization of this process (figure 9):

- The thickness of the SiOx layer significantly impacts the yield of vertical nanowires, its optimal value being 10 nm with our growth conditions.
- The gallium droplet deposition prior to growth allows to force the nucleation of all nanowires simultaneously. This remove the randomness originating from the dewetting of a Ga layer. Moreover, the droplet diameter should not be adapted to the hole diameter but to the final diameter of the GaAs nanowires. This reduces the transient regime present at the start of nanowire growth. If the droplet and the hole diameters are not adapted, multiple wire can nucleate within the same hole.
- When the nanowire density is too high, a competitive growth regime appears, reducing the homogeneity in the nanowire arrays.

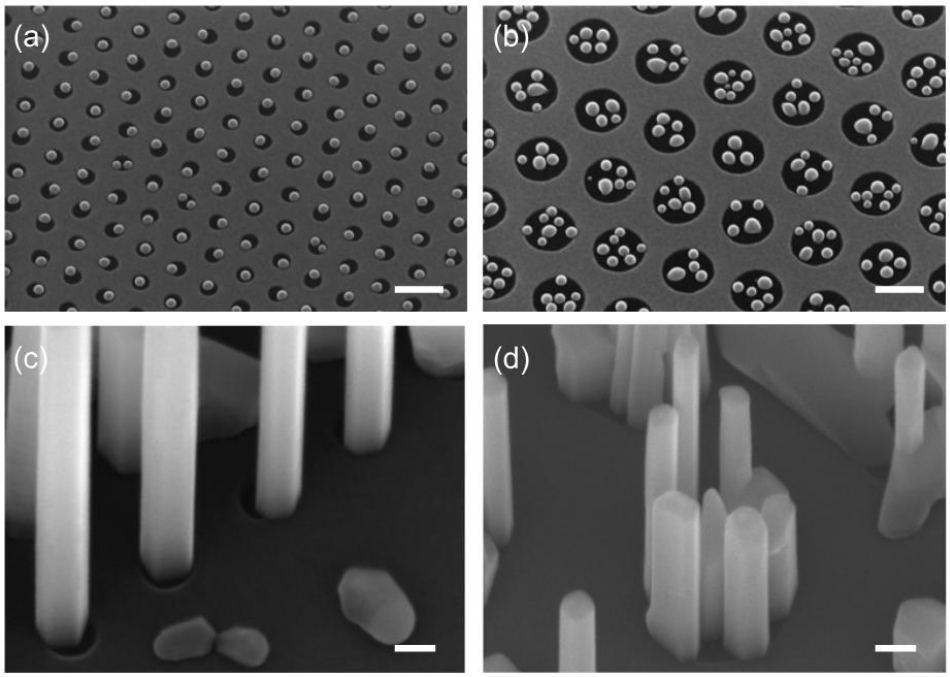


Figure 9: *30◦ tilted SEM images of gallium droplets and GaAs nanowires. The scale bar corresponds to 200 nm in* ***(a)*** *and* ***(b)*** *and to 50 nm in* ***(c)*** *and* ***(d)****.* ***(a)*** *Gallium droplets in 60 nm holes,* ***(b)*** *gallium droplets in 200 nm holes,* ***(c)*** *GaAs nanowires grown with the droplets presented in* ***(a)*** *and* ***(d)*** *GaAs nanowires grown with the droplets presented in* ***(b)****.*

This last comment has strong implications for the vertically integrated GAA FET devices. Indeed, the channel resistance in FETs depends on the material resistivity and its section. In the case of nanowire based GAA FETs, a better electrostatic control of the channel is obtained by decreasing the nanowire diameter. This strongly increases the channel resistance, but can be compensated by parallelizing the conduction by adding multiple nanowires. If the nanowire density is too high, the competitive growth regime introduces randomness on the nanowire lengths and diameters (**figure 10**). This could limit the downscaling of the such architectures.

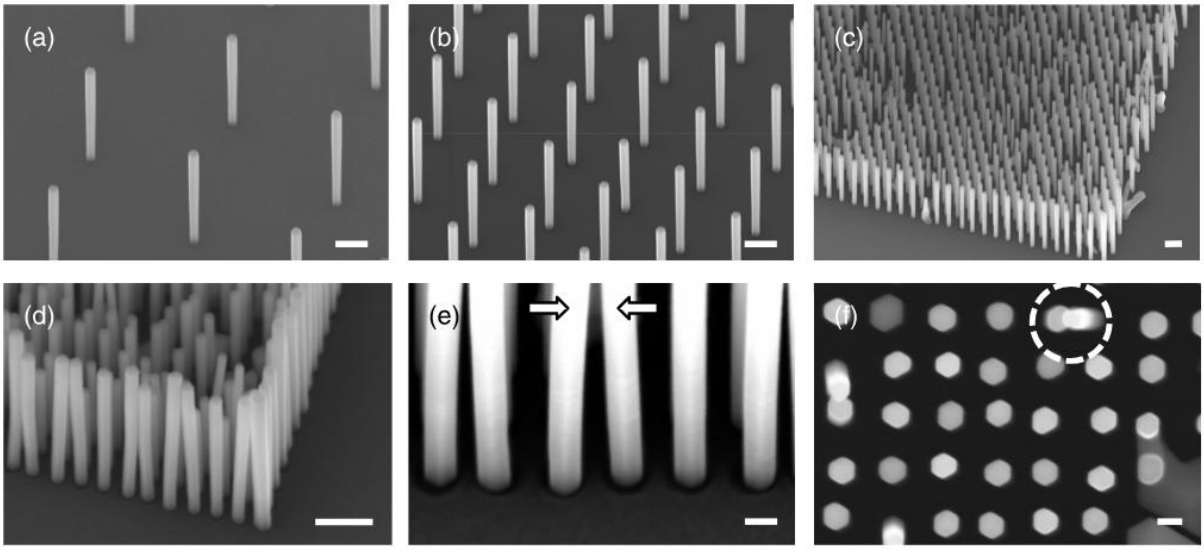


*Figure 10: Nanowire arrays with different pitches. The scale bar corresponds to 200 nm in **(a)–(d)** and to 40 nm in **(e)** and **(f)**. The hole diameter is 60 nm, the SiO_2 thickness is 10 nm, the growth temperature is 630 ◦C and the gallium predeposition time is 45 sec. **(a)–(b)** 30◦ tilted SEM images of nanowire arrays with a yield over 95% and a pitch of respectively 1 µm and 500 nm, **(c)** yield over 85% for the 100 nm pitch, **(d)** yield over 75% for the 80 nm pitch, and **(e)–(f)** respectively 30◦ and 0◦ tilted SEM images of the 80 nm pitch array.*

It can also be observed in **figure 10e,f** that at highest densities, charging effects can occur, which could influence the process flow for the fabrication of GAA FETs, which has already been observed elsewhere during top-down fabrication of nanowire arrays. All these effects seriously limited the successful integration of III-V nanowires into working GAA FET devices.

1.4.3 Self-equilibration of the nanowire diameter

In order to efficiently control the channel in a vertically integrated GAA FET, the nanowire diameter should be reduced to the maximum. The applied voltage on the gate would be otherwise too high to have efficient devices. The issue with self-catalyzed nanowires is that their diameter is not related to the catalyst size but to the growth conditions. We reported this effect as the “self-equilibration of the diameter of Ga-catalyzed GaAs nanowires” and modeled it theoretically[16] as reported in **figure 11**. From our knowledge, the minimal diameter for Ga-catalyzed GaAs nanowires up to now is 50nm, which is twice the targeted diameter for working devices.

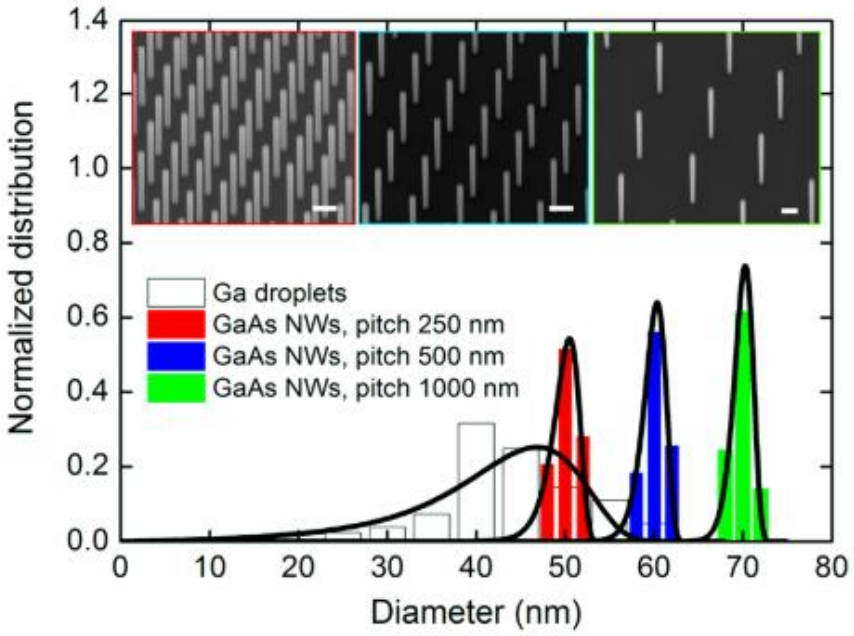


Figure 11: *Histograms showing the distribution of the Ga droplet size and nanowire diameter for arrays with a hole size of 60 nm and three different pitches (left, 250 nm; middle: 500 nm; right, 1000 nm). Inset: 30° tilted SEM images of the corresponding GaAs nanowire arrays. The scale bar is 200 nm. The solid lines show the theoretical fits obtained in reference 16.*

Here, the model developed in ***reference*** 16 shows that the stationary diameter of nanowires can be tuned by the pitch of the Ga droplet array. The normalized histograms of the diameter distributions show the large dispersion of the Ga droplet sizes that equilibrate to regular arrays of 50, 60, and 70 nm diameter nanowires in the course of growth for the pitch of 250, 500, and 1000 nm, respectively. The increase of the stationary diameter is understood through the shadowing effect, which is important for the smallest pitch but vanishes for the large pitches. Thus, the effective collection length of Ga increases for larger pitches and finally becomes limited by the Ga incorporation to the growing shells around the nanowire since this process is necessary to maintain a uniform nanowire diameter from base to top. Finally, the Ga transport into the droplet can be regulated by the wire-to-wire spacing and the resulting nanowire diameter can be finely tuned to the desired value down to 50 nm.

1.4.4 The GaAs nanowire crystalline structure

Another important parameter to consider is the crystalline structure. III-V nanowires are known to crystallize in either a Zinc-blend (ZB)[20], a Wurtzite (WZ)[21] or a mixed-phase structure[22] depending on materials, growth temperatures and fluxes (see **figure 12**). This parameter is thus crucial to control, since it can change the electrical and optical properties of the nanowires. Moreover, stacking defects and phase boundaries can act as scattering centers for carriers, which affect the device performances. Arsenide-based gold-catalyzed nanowires are known to be very versatile regarding this parameter since it is possible to perfectly control their crystallinity by mainly modifying the growth temperature[23]. On contrary, self-catalyzed III-As nanowires present generally a mixed phase, when randomly grown on Si(111) wafers. In our case, the careful optimization of the growth parameters and the adaptation of the gallium droplet size to the final nanowire diameter, at the beginning of the growth, reduce transient

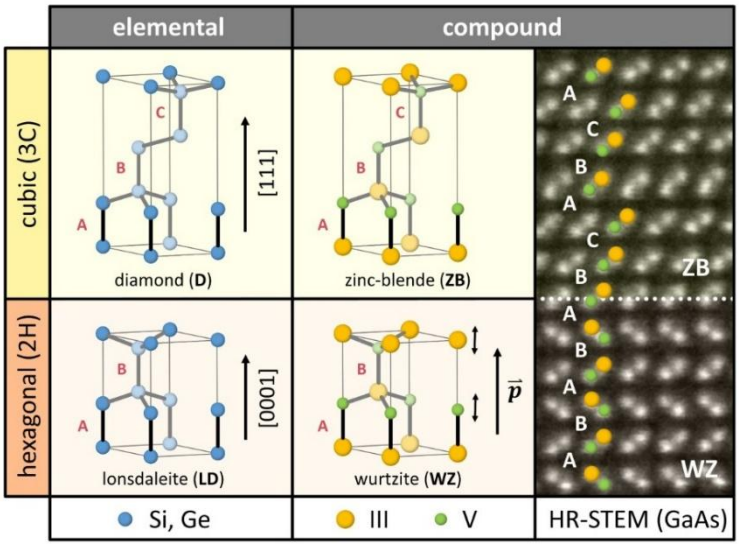


Figure 12: The difference between the cubic (3C) and the hexagonal (2H) crystal symmetries is defined by the atomic bilayer stacking along the [111] or [0001] direction. The corresponding phases are called diamond and lonsdaleite for elemental semiconductors, and zinc-blende and wurtzite for compound semiconductors. The loss of symmetry combined with the ionicity results in spontaneous polarization effects in wurtzite semiconductors, which are absent in other symmetries. A high-resolution scanning transmission electron microscopy image reveals the zinc-blende and wurtzite configurations of GaAs, and shows that a transition between these two phases is possible along the stacking axis.

regimes. As a consequence, the nanowire crystalline structure evolves from pure ZB, to a mixed phase and finally to pure WZ as reported in figure 13. This can be used advantageously by limiting the nanowire length to the first segment, which is typically long enough to construct a complete GAA FET device (< 500 nm). In that case, the "neck" segment, observed at the tip of the nanowire and corresponding to the droplet crystallization, is the only mixed phase. Since a metallic contact should be deposited on this segment, its crystalline structure has no importance for future device performances.

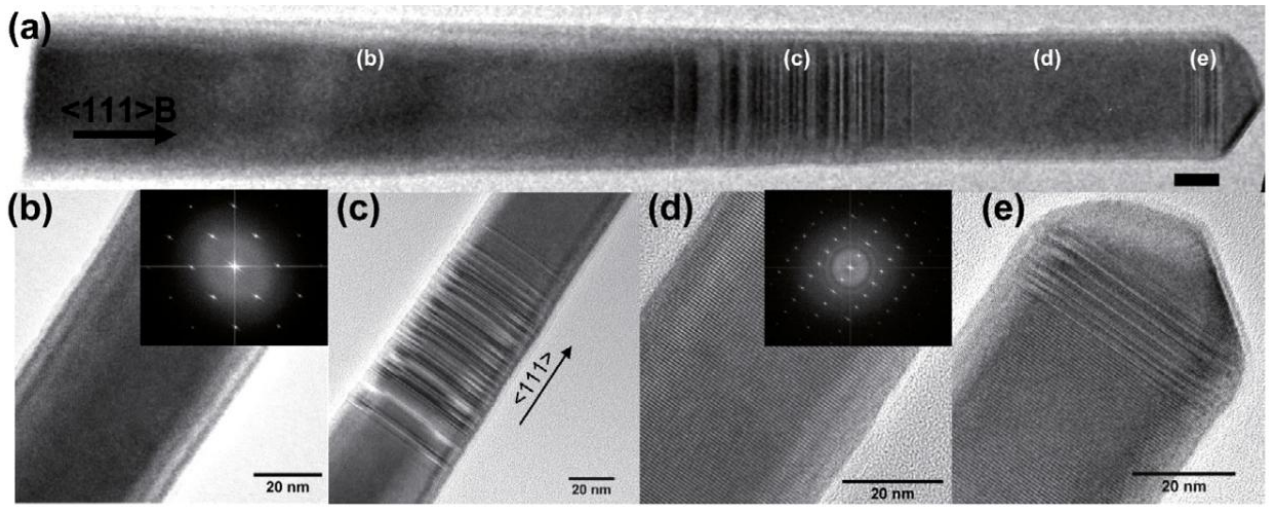
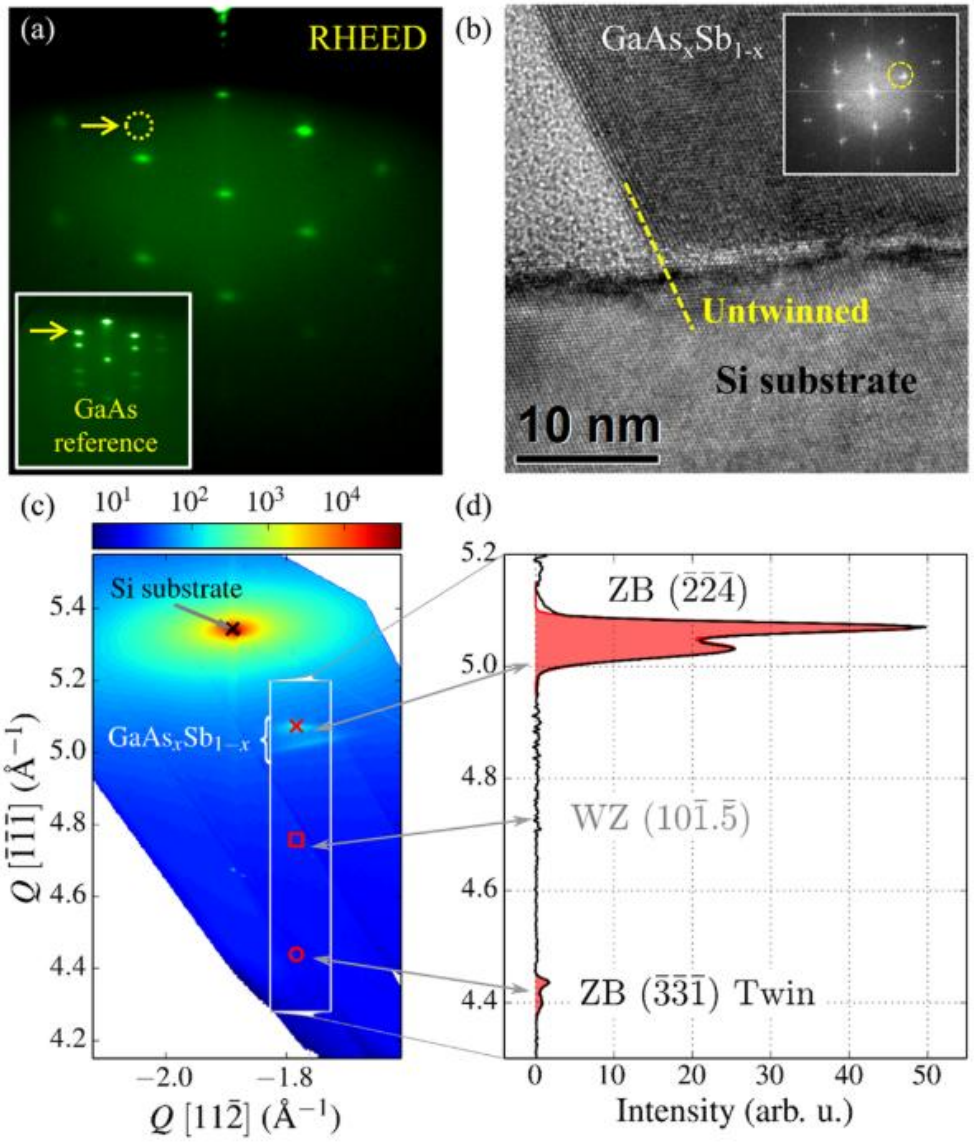


Figure 13: (a) TEM image of a full GaAs nanowire, viewed in the <1-10> zone axis (cubic notation). The sample was grown on oxide-free silicon at 630 ◦C, with V/III = 1.8. The bottom of the nanowire has a ZB crystal structure, with very low stacking faults density in the segment. Then a transition with twin planes and stacking faults occurs in the middle, before a pure WZ structure is observed (right). The neck region forms a ZB tip with a transition region containing stacking faults below. Higher magnification images of the bottom, middle segment, and top including neck are shown respectively in (b), (c), (d). The inset fast Fourier transforms (FFT) show a pattern characteristic of ZB structure (b) and WZ structure (c).

Another possibility to control the nanowire crystalline structure, is to slightly change the nanowire composition. Indeed, the addition of about ten per cent of antimony in GaAs nanowires switch the crystalline structure to pure ZB regardless of the length[17]. Here, it is even possible to force the nanowire nucleation in particular orientations as reported in **figure 14a**. Indeed, the RHEED diffraction pattern on the fluorescent screen comes from the diffraction of a large number of nanowires. Single or multiple twins, forming at any position in the nanowire give rise to a double-spot pattern, which is characteristic of a twinned material (see inset in **figure 14a**). The addition of antimony during growth, force nucleation in a particular orientation and prevent any twins to appear.



*<u>Figure 14:</u> **(a)** Typical RHEED diffraction pattern during $GaAs_{1-x}Sb_x$ NW growth, and diffraction pattern for a reference GaAs NWs as inset. **(b)** High-resolution TEM image of the $GaAs_{1-x}Sb_x$/Si interface and associated fast Fourier transform as the inset, revealing the perfect epitaxial relationship: $(-1-1-1)[01-1]_{GaAsSb}$ $||(111)[01-1]_{Si}$ and differences in lattice parameters. The yellow line illustrates the epitaxial relationship. **(c)** X-ray diffraction reciprocal space map showing the diffracted intensity around an asymmetric (−2−2−4) Bragg reflection, on a logarithmic scale, for the $GaAs_{1-x}Sb_x$ nanowire array illustrated in **figure 14a**. **(d)** Ensemble averaged intensity distribution of the ZB (−3−3−1) twin/ZB(−2−2−4) and WZ (10−1−5) reflections showing that the vast majority of NWs grows untwinned.*

1.4.5 The growth of axial and lateral heterostructures

Next is the growth of axial and lateral heterostructures. Indeed, as reported previously, the interest for GaAs materials, in the context of GAA FETs, lies in the GaAs-AlGaAs core-shell heterostructure. In order to demonstrate the feasibility to integrate both axially and laterally such materials and taking advantages of the previous developments, we reported the gold-free growth of such structures on silicon. For that purpose, two GaAsSb segments are integrated inside a GaAs nanowire, before an AlGaAs shell is grown all-around. The whole structure is presented in **figure 15b**.

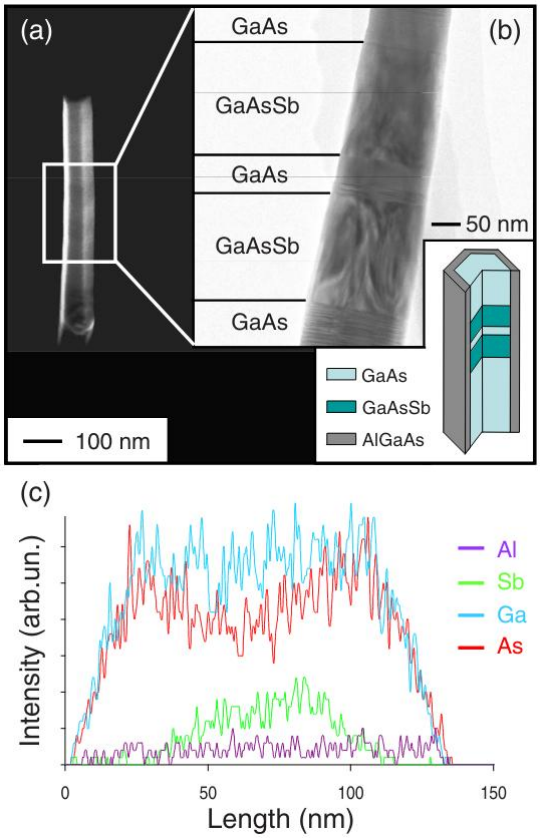


__Figure 15:__ (a) SEM and (b) TEM images of GaAs nanowires containing two GaAsSb axial segments, and coated by an AlGaAs shell. The TEM image is taken along the <-110> zone axis. A schematic of the structure is also provided. (c) Cross-sectional EDS measurement across a segment in a nanowire, showing the $GaAs_{1-x}Sb_x$ core and the $Al_yGa_{1-y}As$ shell.

In this study, the first GaAs segment typically exhibits stacking faults and a wurtzite phase. On the contrary, the GaAsSb segments exhibit perfect twin-free zinc blende phase, and the middle GaAs segment has a wurtzite crystal structure. The transition from GaAsSb to GaAs on the bottom side shows some stacking faults, whereas the transition from GaAs to GaAsSb on the upper side is abrupt. This is related to antimony traces remaining in the particle after the switching sequence to GaAs is done. Finally, a strain field is observed on the GaAsSb segments (**figure 15b**), due to the presence of a lattice mismatched AlGaAs shell, which is not observed on GaAs segments. This heterostructure demonstrates thus the possibility to grow GaAs-AlGaAs or defect-free GaAsSb-AlGaAs core-shell nanowires directly on silicon.

1.4.6 Assessment of GaAs(Sb) nanowires for GAA FETs

As reported in the previous sections, we managed to integrate highly homogeneous self-catalyzed GaAs nanowire arrays on Si(111). We studied and optimized the growth conditions in order to decrease the nanowire diameters down to 50 nm. We report a perfect control of their ZB crystalline structure down to the first bilayer, and fabricated the first axial and lateral heterostructures.

Nevertheless, several problems have arisen, making GaAs nanowires, at the moment, a dead end for GAA FET devices. First, the thinnest achieved diameters (50 nm) do not allow an effective pinch off of the channel. This effect is further accentuated by the core-shell geometry of GaAs-AlGaAs heterostructures. Moreover, complementary studies[24,25] from other groups reported an inhomogeneous integration of aluminum during the shell growth as reported in figure 16. This accumulation of aluminum in the corners can create local quantum dots that prevent efficient vertical transport in the nanowires.

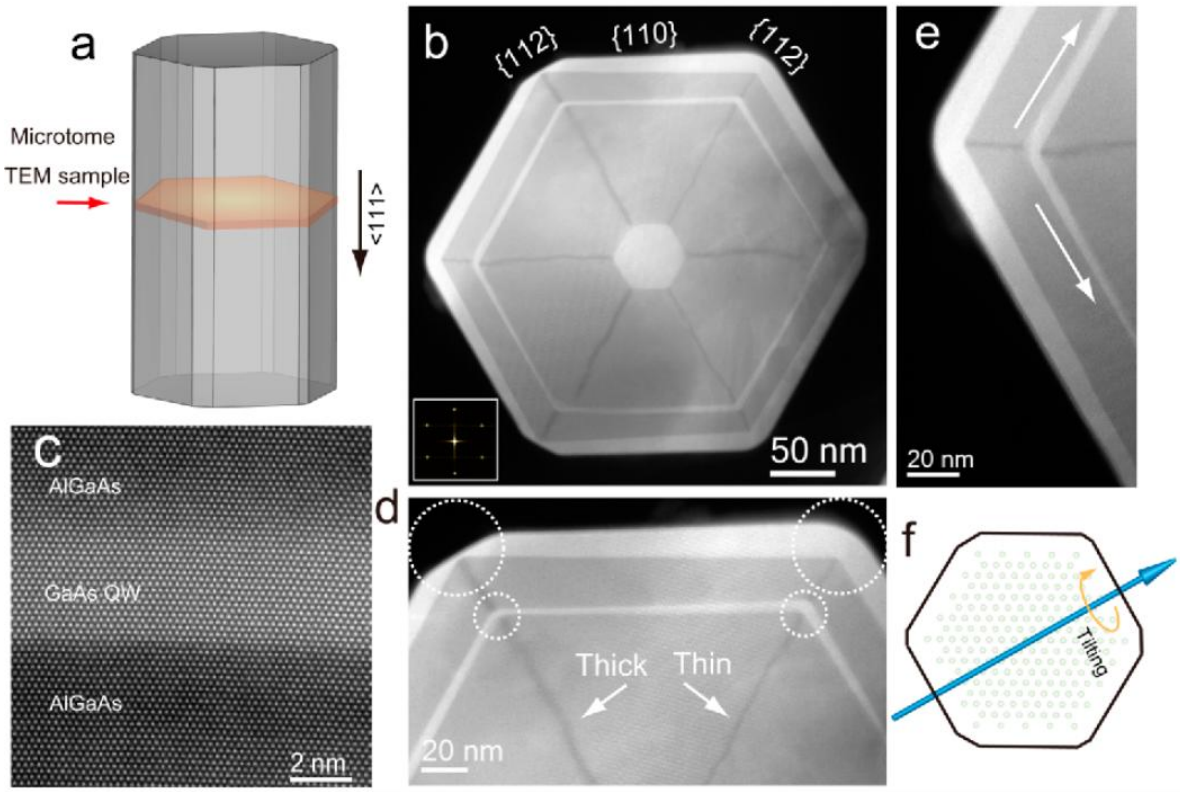


*Figure 16: **(a)** Schematic of the TEM cross-section of the nanowire prepared by microtoming. **(b–e)** HAADF-STEM images of an AlGaAs/GaAs nanowire cross-section viewed along the ⟨111⟩ direction; **(b)** low magnification overview (inset: Fourier transform spectrum from a corresponding atomic resolution image); **(c)** atomic resolution image of the GaAs quantum well and the AlGaAs barrier layers. **(d)** Higher magnification image of the top region of **(b)** and **(e)** higher magnification image of the left region of **(b)**. **(f)** Schematic showing the tilt direction from ⟨111⟩ toward ⟨110⟩ (around the blue arrow).*

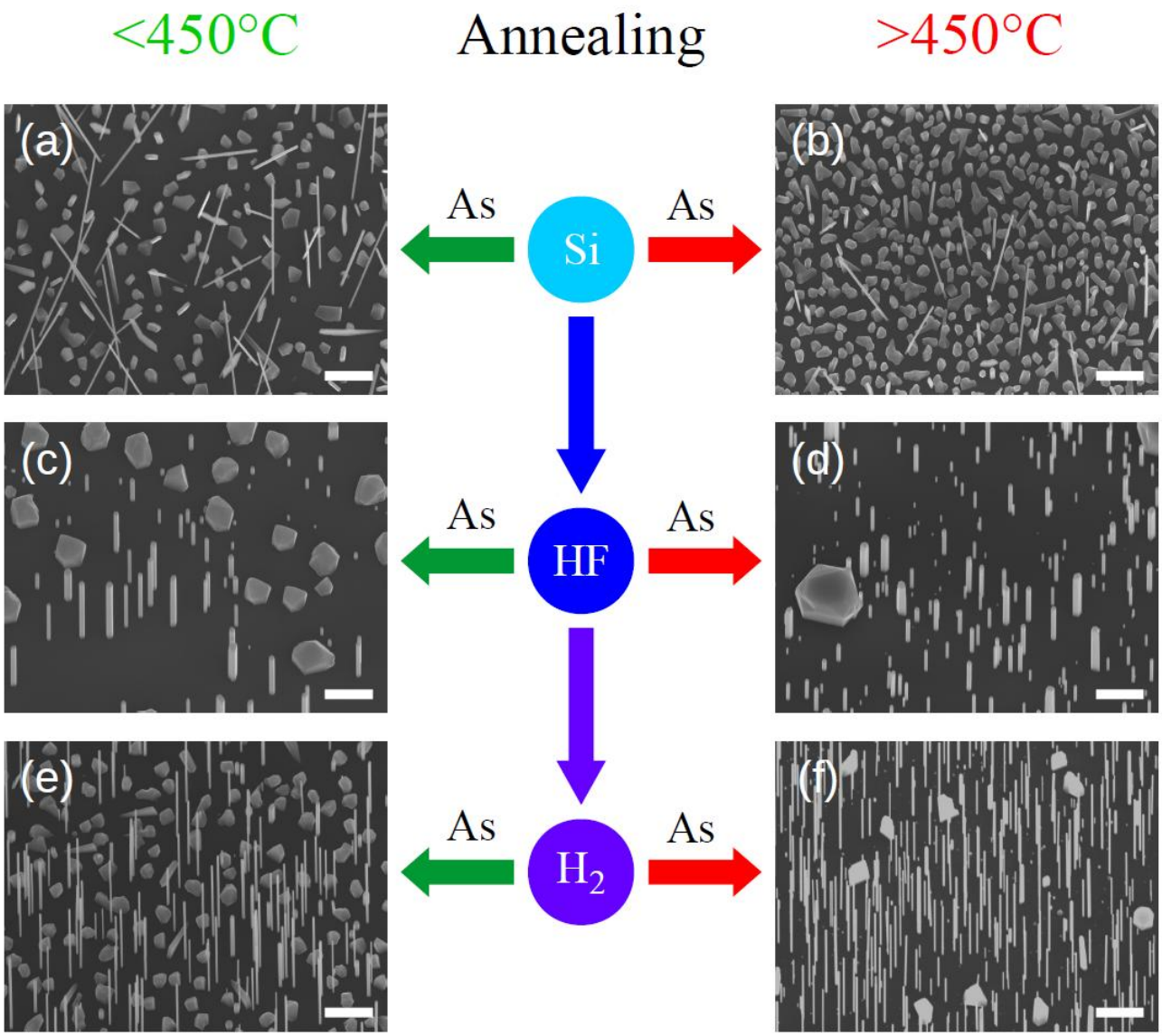
These limitations motivated the community to work on other binaries such as InAs and InSb. If the integration of the former on silicon is widely reported in literature, the surfactant effect of antimony prevents the successful growth of the second.

1.5 The integration of InAs nanowires on silicon[22,26–30]

Contrary to the GaAs nanowires, the self-catalyzed InAs ones grow generally without the presence of any indium droplet at their tip. Here, the driving force for nucleation and vertical growth is the difference in chemical potential between the Si(111) substrate and the InAs facets. This major difference has several consequences for their integration on silicon by MBE. First, the presence of silicon oxide on the substrate surface prevent the nucleation. Since indium is less reactive with SiO_x than gallium, and because its oxide (InO_y) is less volatile than the gallium one, the surface preparation is more challenging: the deposition of a metallic indium layer on the native oxide does not open etched pits. An ex-situ chemical etching (HF, H_2O_2, H_2O) is thus mandatory prior to growth. Moreover, the nucleation of the nanowires can no longer be forced at the start of growth by deposition of indium droplets, the transient regime is thus longer and the aspect ratio homogeneity decreases on the wafer. If the growth parameters have globally the same influence on the nanowire shape than for the Ga-catalyzed ones, the surface preparation has more impact.

1.5.1 Influence of the surface preparation on the InAs nanowire growth

Figure 17 illustrates the different wafer preparation we studied in order to improve the nucleation and growth of thin InAs nanowires on Si(111) substrates. First it can be noticed that, similarly to what is reported in literature for other growth methods (MOVPE)[31], the presence of any oxide on the substrate surface leads to nanowires growing in all directions (**figure 17a,b**), even when arsenic is used to promote vertical integration. Adding HF etching before growth solves this problem, but the lengths, diameters, and densities of the nanowires are rather inhomogeneous (**figure 17c,d**). Saturating the Si dangling bonds at the Si(111) surface by an hydrogen surface preparation allows to increase the indium diffusion length at the substrate surface. The InAs nanowire grown subsequently can thus collect more material, exhibit higher aspect ratios and better homogeneity (**figure 17e,f**). The nanowire diameters are significantly reduced, while lengths are increased, which is favorable for future GAA FETs. It can be noticed that this whole process can be Back End of Line (BEOL) compatible with a maximum temperature below 450°C (left column in **figure 17**), which offers more flexibility for industrial integration. A parasitic growth can be observed between nanowires, but the use of patterned substrates will solve this issue. The last problem of concern lies in the nanowire length inhomogeneities, since the planarization and contacting steps of the device fabrication are impossible here. Forcing nucleation by depositing indium droplets, prior to nanowire growth, prevents nucleation and results in more parasitic growth. Contrary to gallium droplet, the indium ones wet the Si(111) substrate, which is detrimental to nucleation. Possible solutions to this issue could be to either increase the growth kinetics, which should decrease the waiting time prior nucleation, change the growth temperature or the V/III ratio. These different options should also strongly impact the nanowire aspect ratio but have not been studied yet. Thereafter, and unless otherwise indicated, the only used process will correspond to that of **figure 17e**.



*<u>Figure 17:</u> Surface preparations and InAs nanowire growths. **(a)–(f)** SEM images of InAs nanowires grown on silicon (111) wafers using the same growth conditions but different surface preparations. The processes are divided in two: [**(a)**, **(c)** and **(e)**] are compatible with the BEOL limitations with an in-situ annealing at growth temperature whereas [**(b)**, **(d)** and **(f)**] are annealed at higher temperature. For **(a)** and **(b)**, the native oxide is present when samples are loaded into the growth chamber. For **(c)** and **(d)**, the native oxide is removed using an HF 5% solution for 1 min prior to the loading into the MBE reactor. For **(e)** and **(f)**, a flux of hydrogen is used during the sample degassing (after the native oxide removal). The scale bars correspond to 500 nm.*

1.5.2 Parametric growth study and optimization of the aspect ratio

Next, a parametric growth study was carried out based on the **figure 17e** surface preparation. All samples are degassed at 200°C for one hour under a hydrogen flux (either gas or plasma) before being annealed in the growth chamber for one hour at 410°C under arsenic. The InAs nanowire growth is then initiated by opening simultaneously the indium and arsenic shutters. **Figure 18** illustrates the statistics obtained by automatically measuring more than 150 nanowires per sample.

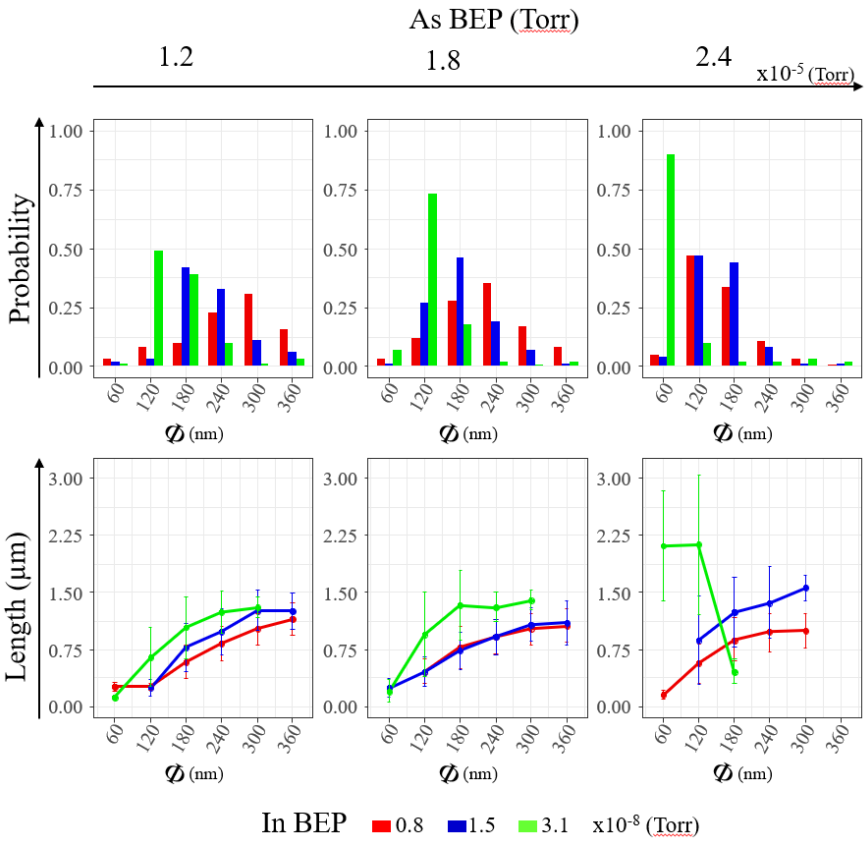
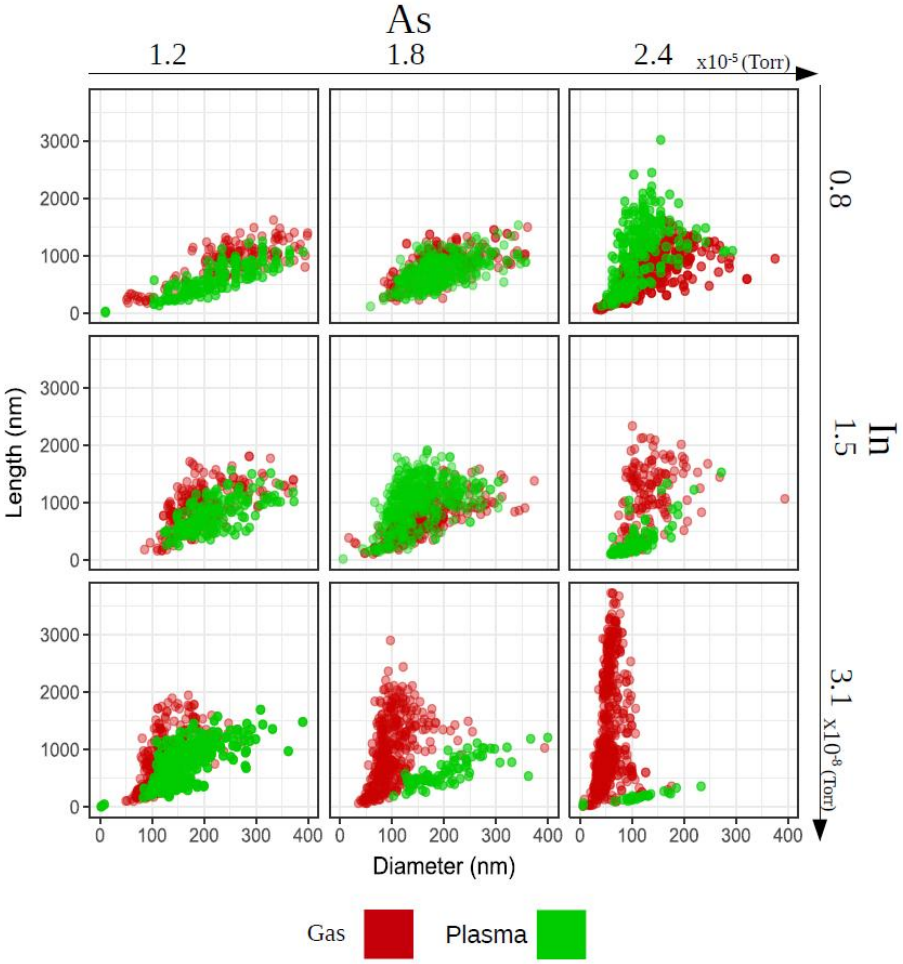


*Figure 18: Statistic plots for the H_2-gas treated surfaces corresponding to the **figure 17(e)** process. Nanowires are grouped in families of different diameters. The three colors (red, blue, green) correspond to different indium beam equivalent pressures (BEP). On top, the proportion of each family is reported as a function of the arsenic flux (As BEP). On bottom, the mean length of each family is reported as a function of the arsenic flux. These statistics graphs allow to evaluate the influence of the indium and arsenic fluxes on the diameter and the length of the InAs nanowires.*

Similarly to what we observed previously for GaAs, the nanowire diameter decreases when the arsenic flux is increased, whatever the indium flux is. This is consistent with other MBE studies about InAs nanowire growth[32] and a self-catalyzed growth mechanism [vapor solid (VS) growth mechanism]. Interestingly, when the indium and arsenic fluxes are both increased simultaneously (green histograms in the top and middle right panels), long and thin nanowires can be obtained. This "abnormal" behavior is the consequence of a change in the growth mechanism from VS to VLS as already reported for InP nanowires[33]. Thus, filling the Si dangling bonds at the substrate surface and optimizing the growth conditions allow to maximize the aspect ratio of VLS InAs nanowires on silicon. If the nanowire diameters are still too large for GAA FETs devices, the VLS growth mechanism observed here opens new perspectives.

In order to assess possible differences between a H_2-gas and a H_2-plasma treatment, all the growth conditions investigated in **figure 18** have been repeated in the case of the H_2-plasma preparation and statistics are reported in **figure 19**.



<u>Figure 19:</u> Comparisons between the H_2-gas (in red) and H_2-plasma (in green) surface preparations. Each of the 9 scatter plots correspond to one specific growth condition associated with the arsenic and indium fluxes reported on top and on right. For each plot, the x-axis corresponds to the diameter and the y-axis to length of the nanowires. Each point represents a unique nanowire measured either for the H_2-gas (in red) or the H_2-plasma (in green) surface preparations. Red and green points are almost superimposable for low indium and arsenic fluxes but are well separated for high indium and arsenic fluxes.

Surprisingly, it is clear from these statistics that nanowires growing from either H_2-gas (Red) or H_2-plasma (Green) surfaces are different when increasing the arsenic and indium fluxes. Although the H_2-gas and H_2-plasma preparations are not expected to give dramatically different surfaces, major changes are observed. While H_2-gas treated surfaces favor long and thin wires when indium and arsenic fluxes are increased, the opposite is observed for H_2-plasma treated surfaces. This could be explained by a better filling of the Si dangling bonds and a smoother surface for the H_2-gas preparation in comparison with the H_2-plasma one. Group III elements arriving at the substrate surface would have longer diffusion length in the former case. Each nanowire collecting atoms on longer distances, the overall growth kinetics is increased and the growth mechanism changes from VS to VLS. This observation is still not well understood at the moment and further investigations are required in order to unwell the differences between both surface preparations.

1.5.3 Modeling of the surface preparations

In order to understand the role of hydrogen and arsenic on the Si(111) surface during nanowire nucleation, we performed density functional theory (DFT) calculations. Two different surface terminations are then considered, depending on the surface treatments. The first one is mainly covered by hydrogen atoms that fill the dangling bonds [H-terminated Si(111):1×1]. In the second, an arsenic layer substitutes to the topmost layer of the silicon substrate [As-terminated Si(111):1×1]. Results of the simulations are reported in **figure 20**.

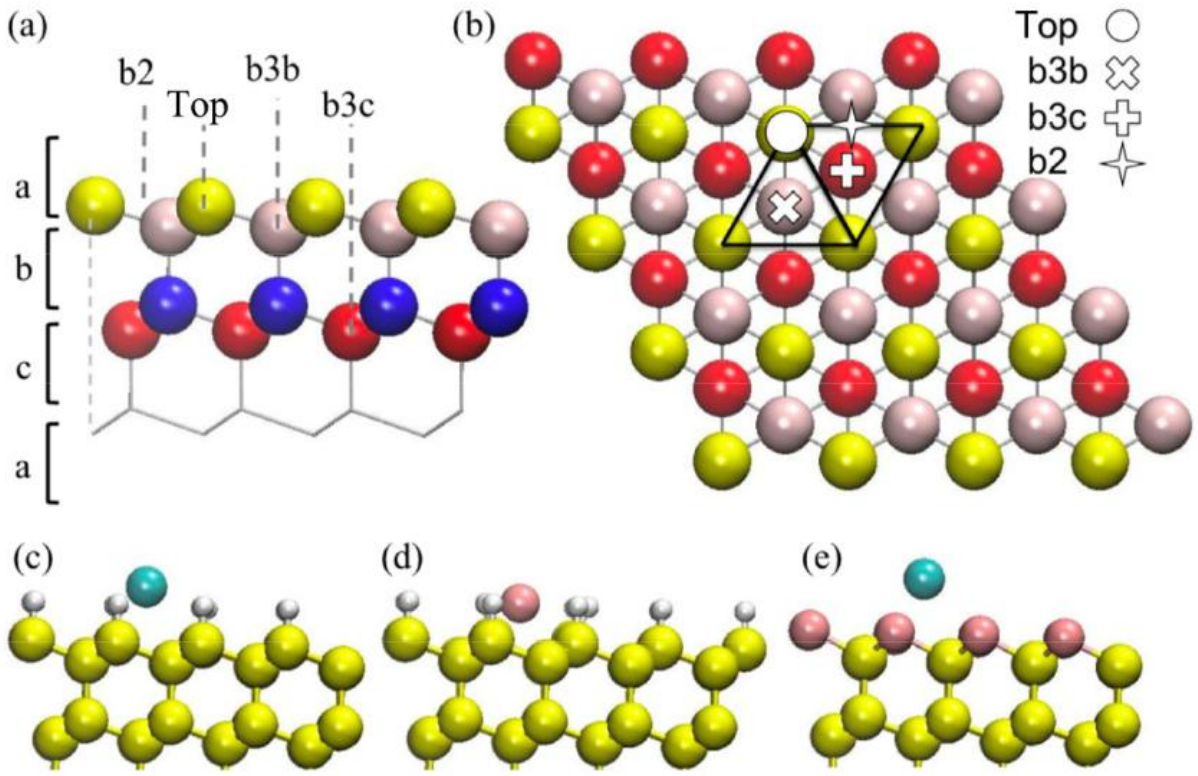


Figure 20: ***(a)*** *Side view and* ***(b)*** *top view of the Si(111) slab used in the DFT calculations where the investigated adsorption sites are shown: top, b2, b3b, b3c. The first to fourth layers are colored in yellow, beige, blue and red, respectively in order to highlight repeating pattern observed in the layers stacking of (111) oriented Si crystal. In* ***(c)****,* ***(d)*** *and* ***(e)****, yellow, white, cyan and pink spheres are respectively Si, H, In and As atoms.* ***(c)*** *Adsorbed configurations of In on H-terminated Si(111):1×1 surface.* ***(d)*** *Adsorbed configurations of As on H-terminated Si(111):1×1 surface.* ***(e)*** *Adsorbed configurations of In on As-terminated Si(111):1×1 surface as after an arsenic treatment.*

The adsorption of both indium and arsenic atoms has been studied at several initial positions on the Si(111) substrate, taking advantage of the crystal symmetry. In the following, only the four most favorable ones are discussed: the Top, b3b, b3c and b2 positions as illustrated in **figure 20b**. The Top configuration corresponds to an atom adsorbed above one atom of the topmost layer (either H or As atom as a function of the surface treatment). Three other configurations are discussed, where As or In atom can adsorb as a bridge configuration either between two atoms of the topmost layer (As or H species) referred as b2 adsorption site or between three atoms of the topmost layer, either As or H species, and named b3b and b3c

depending on the layer stacking of the silicon Si(111) substrate as schematized (figure 20a,b). It results from these simulations that the hydrogen preparation not only fills all dangling bonds, increasing the diffusion length of elements III, but also prevents from indium and arsenic incorporation at low temperature. By keeping "clean" surfaces, hydrogen allows thus to reduce the annealing temperature at which is formed the As-terminated Si surface.

Adsorption energies and typical bond lengths are provided in table 1.

	H-terminated Si(111):1 × 1				As-terminated Si(111):1 × 1	
	As adsorption		In adsorption		In adsorption	
	Eads (eV)	d(As-H) (Å)	Eads (eV)	d(In-H) (Å)	Eads (eV)	d(In-As) (Å)
Top					−1.24	2.88
b2	−0.41	2.12	−0.83	2.55	Non stable	—
b3b	0.73	2.70	−0.83	2.54	−1.58	3.15
b3c	0.33	2.70	−0.85	2.54	−1.60	3.17

Table 1: Adsorption energy (Eads in eV) and typical bond length (d in Å) for single As and In atoms on H-term surface and adsorption energy for single In on As-terminated surface.

Regarding the adsorption of arsenic and indium atoms on a H-terminated surface, the adsorption processes are endothermic or slightly exothermic. For instance, it is –0.85 eV for the indium atoms on the H-terminated surface as calculated for the figure 20c configuration. Moreover, these simulations highlight that the adsorption of As atom implies a deep deformation in the H atoms layer: H atoms are repelled from As ones to allow the later to come closer to the underlying topmost layers of the Si substrate, revealing a favorable interaction between Si and As species (figure 20d). Such a deformation of the whole system involves a significant deformation cost as revealed by the energetic penalty of the adsorption energy. This confirms that the adsorption reaction of both As and In on H-terminated surface is not favorable at low temperature. The H-terminated surface prevents thus any contaminant incorporation prior to the high temperature annealing under arsenic. At this point, the As-terminated Si(111):1×1 surface is formed and passivates the substrate surface.

1.5.4 Growth of InAs nanowires on patterned substrates

Similarly to the process developed for integrating GaAs nanowires on silicon, we attempted to transfer the optimized growth conditions developed on bare silicon substrates to patterned ones. Results are rather disappointing as reported in figure 21. First, a good selectivity is observed between holes and the SiOx layer: no parasitic growth is observed out of the patterns. The growth time was reduced in order to decrease both the InAs nanowire lengths and diameters (~35-40nm). The yield of vertical nanowires reaches 80 percent at best and the overall homogeneity is improved. Still, some parasitic growth is observed inside the patterns and length differences complicate device fabrication.

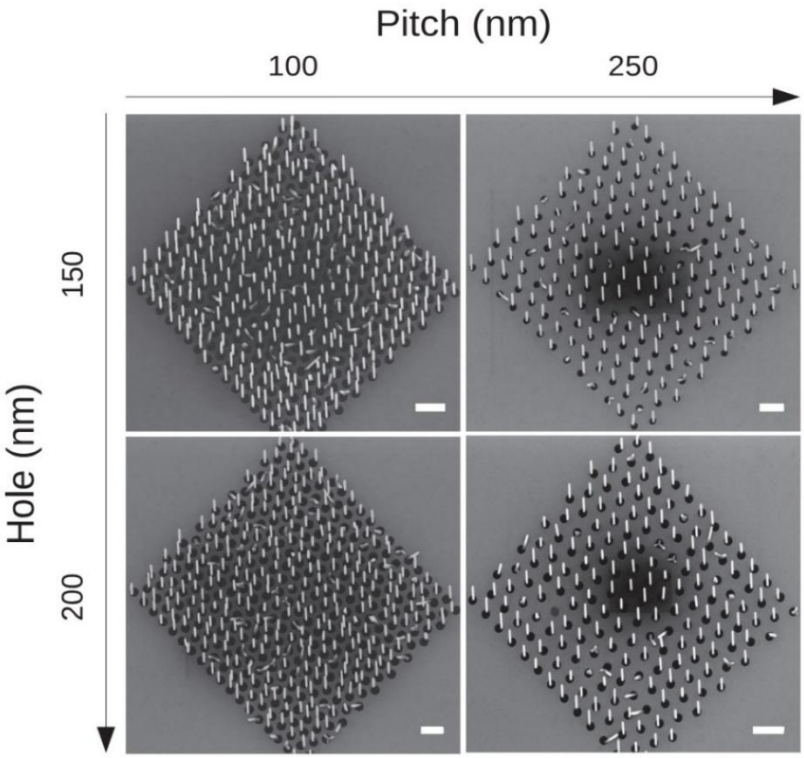


Figure 21: SEM images of InAs nanowires grown on patterned substrates. The pitch increases from left to right and the hole diameter from top to bottom. Scale bars are 500 nm.

1.5.5 The InAs nanowire crystalline structure

The crystalline structure of the self-catalyzed InAs nanowires using both the VS and the VLS growth mechanisms has been probed by TEM measurements. In both cases a mixed-phase crystalline structure is observed with a majority of ZB segments at the bottom of the nanowires and more WZ toward the tip. This observation is in good agreement with the evolution of the crystalline structure observed for GaAs nanowires. It should be noticed that controlling the crystalline structure in self-catalyzed InAs nanowires by MBE remains challenging, if not ever reported. We previously studied the influence of the crystalline structure on the transport properties of gold seeded InAs nanowires[22] and no significant effect on the room temperature resistivity was found. The transport properties are more sensitive to the surface roughness and band bending in these nanostructures. When looking at the interface between the silicon substrate and the InAs nanowires, a 90° dislocation network can be observed with ten silicon planes corresponding to nine InAs ones (**figure 22b**). The geometrical phase analysis (GPA) of the interface confirms the presence of five dislocations within a distance of roughly 11 nm, which is in agreement with a full relaxation of the strain after only a few monolayers (**figure 22e**). The optimized surface preparation presented in **figure 17** leads thus to the totally relaxed epitaxial growth of InAs NWs on silicon respecting a BEOL compatible thermal budget (<410°C). The minimum diameters measured are around 25 nm, which is low enough for good channel control in GAA-FET devices. Nevertheless, following the strategy developed for GaAs, we tried to add antimony during growth for switching the crystalline structure to a pure ZB one and for improving the intrinsic material properties (higher mobilities, lower effective mass). Achieved results are comparable to those reported previously[26] for gold-catalyzed InAsSb nanowires with a switching of the crystalline structure to pure ZB for antimony composition above 10% (**figure 23**).

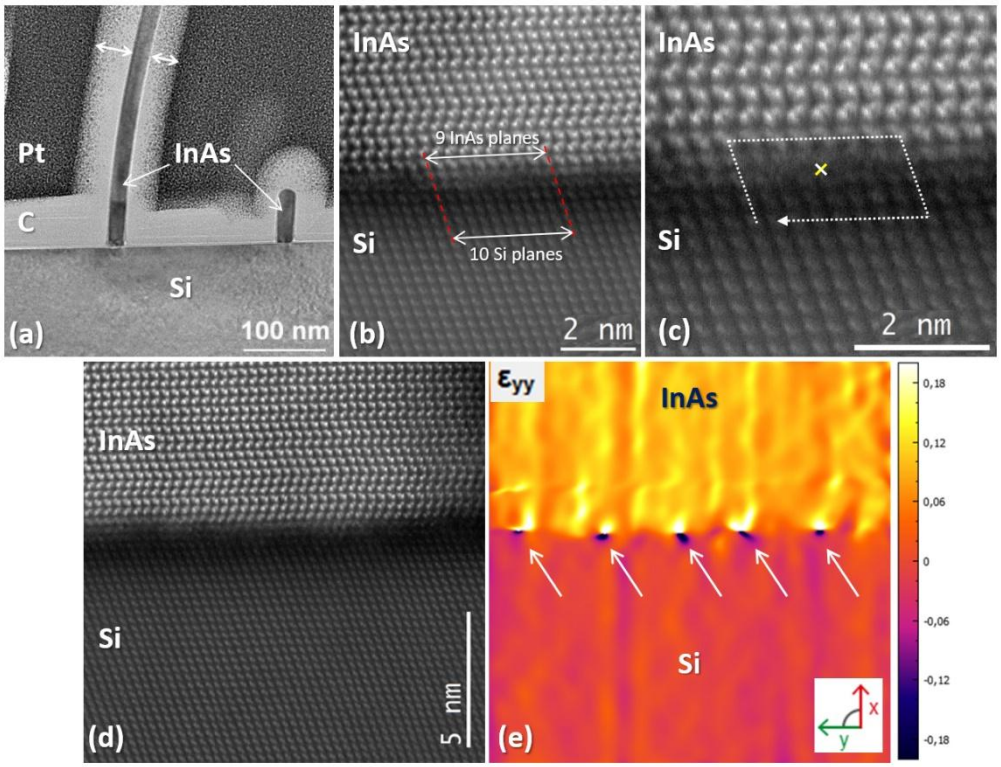


Figure 22: ***(a)*** *Cross-section TEM image of InAs nanowires still attached to the Si(111) substrate. Non-uniformity in the carbon deposition on each side of the NWs (cf. white arrows) may result in stress-induced bending of long nanowires.* ***(b)–(d)*** *STEM/HAADF images taken at the interface between an InAs nanowire and the Si substrate indicating that the InAs growth occurs epitaxially on the Si substrate. The weak contrast band located at the InAs/Si interface corresponds to the native SiO_2 layer covering the Si surface around the nanowire.* ***(b)*** *Along the direction parallel to the interface, about 9 InAs(111) planes are observed for every 10 corresponding Si(111) planes, in agreement with the ratio between the lattice constants of InAs and Si (a[Si]/a[InAs] = 0.897). The InAs nanowires can therefore be considered as fully relaxed.* ***(c)*** *A Burgers circuit drawn at the InAs/Si interface allows to identify the position of an isolated misfit dislocation.* ***(d)*** *STEM/HAADF image of the InAs/Si interface region and* ***(e)*** *corresponding strain mapping (ε_{yy}) in the direction parallel to the interface obtained by GPA. Five dislocations are visible within a distance of ~ 11 nm along the interface, in agreement with a complete relaxation of the InAs lattice.*

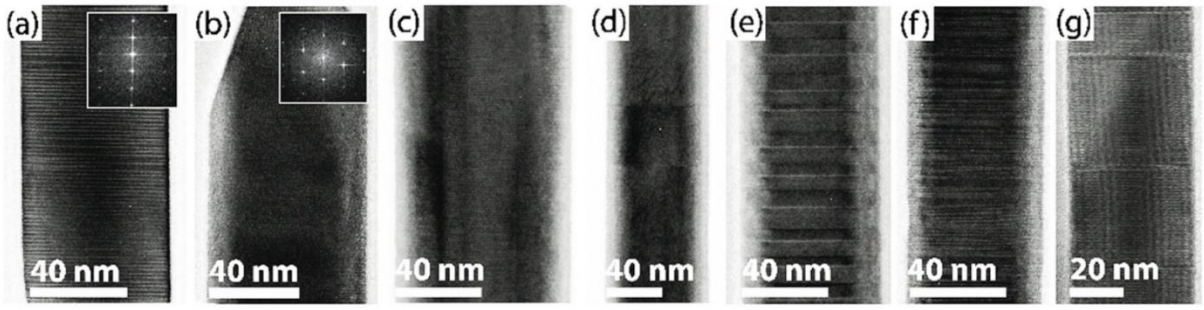


Figure 23: *Transmission electron microscopy images, taken along the <1-10> zone axis, of $InAs_{1-x}Sb_x$ top segments from InAs/$InAs_{1-x}Sb_x$ heterostructure nanowires all having similar seed particle diameters (40–50 nm):* ***(a)*** *InAs (x = 0) with pure wurtzite (WZ) structure, with associated fast Fourier transform (FFT) as inset;* ***(b)*** *InSb (x = 1) with pure zinc blende (ZB) structure, with FFT as inset;* ***(c)*** *x = 0.12, pure ZB structure;* ***(d)*** *x = 0.08, ZB with occasional twin planes;* ***(e)*** *x = 0.05, ZB with pseudo-periodic twin planes;* ***(f)*** *x ≈ 0.03, mixed ZB and WZ with frequent stacking faults and twins;* ***(g)*** *Sb content below EDS detection limits (nominal Sb flux two-thirds of* ***(f)****), WZ structure with regular stacking faults.*

1.5.6 Electrical characterizations of InAs(Sb) nanowires

The fabrication of GAA FETs is process heavy and requires numerous optimizations before significant characterizations can be performed. To our knowledge, only two groups managed to fabricate such devices using bottom-up nanowires[31,34]. Since our growth process is not mature enough to develop such architectures, we focused our electrical characterizations on individual InAs(Sb) nanowires. Moreover, due to a shift of the research activity over the years toward new applications (chapters 2 and 3), electrical characterizations were only performed on gold-catalyzed nanowires (available earlier). **Table 2** summarizes these measurements performed on WZ InAs, WZ InAsSb, ZB InAsSb and ZB InSb nanowire grown by MBE.

Sample	Material	Crystal phase	NWs	D (nm)	L_G (nm)	$C_{G,model}$ (aF)	ρ (mΩ cm)	V_T (V)	μ_{peak} (cm^2/Vs)
A	InAs	WZ	7	67	580	33	8.1	−5.4	1560
B	$InAs_{0.91}Sb_{0.09}$	WZ	6	68	550	32	50	−0.6	2410
B	$InAs_{0.87}Sb_{0.13}$	ZB	6	72	550	33	4.1	−5.8	3410
C	InSb	ZB	2	56	590	31	93	1.8	450
C	InSb	ZB	3	74	600	36	66	1.1	760
C	InSb	ZB	4	98	580	39	45	−0.1	1010

Table 2: *Averaged electrical characterization of WZ InAs, WZ InAsSb, ZB InAsSb and ZB InSb nanowires grown by MBE.*

For similar device geometries, $InAs_{1-x}Sb_x$ nanowires have higher transconductance and field-effect mobility compared to their binary counterparts (InAs, InSb). Interestingly, InSb nanowires only show low extracted values for field-effect mobility, although with a strong diameter dependence. Further improvements require passivating schemes to reach higher room temperature mobilities in Sb-based nanowires (chapter 2). Overall, the improved transport properties of InAsSb nanowires prove them to be ideal candidates for future GAA FET devices.

1.5.7 Assessment of InAs(Sb) nanowires for GAA FETs

In the context of the bottom-up integration of GAA FET on silicon, InAs(Sb) nanowires remain the most promising materials. The selective area growth and the control of the crystalline structure are demonstrated. The nanowire diameters (~ 25nm) are compatible with an efficient electrostatic control of the channel. The superior transport properties of the InAs(Sb) nanowire are reported, and contrary to pure InAs nanowires, no pining of the Fermi level at the surface is observed. This leads to transport properties less sensitive to the surface, and thus an easier integration into devices.

Nevertheless, several issues should be tackled in the future. First the yield of vertically integrated thin InAs(Sb) nanowires should be improved. Several studies report better yields, using higher V/III ratio, which also leads to thicker nanowires (>80nm)[35]. Instead, we propose to study the possible VLS integration of InAs(Sb) nanowires on Si(111). This approach should also improve length homogeneity in nanowire arrays and facilitates fabrication of GAA FET devices. Finally, the device fabrication steps should be optimized for this new material, specially the conformal high-K deposition.

1.6 Conclusion

The research activity focused on the integration of self-catalyzed high mobility III-V nanowires on silicon led to numerous breakthroughs. The parametrical growth studies allowed to unveil the physical mechanism involved in the nucleation and the growth of GaAs and InAs nanowires on silicon. The optimization of the substrate preparation and of the growth conditions yielded to the integration of highly homogeneous nanowire arrays on silicon, which is a mandatory step toward GAA FET devices. A perfect control of their crystalline structure is achieved thanks to the addition of roughly 10 percent of antimony in the alloys. Both axial and lateral heterostructures are reported in the case of GaAs nanowires, demonstrating the possibility to integrate high mobility 2D electron gas in a core-shell geometry. Electrical characterizations of InAs nanowires demonstrate the low influence of their crystalline structure on the transport properties and the interest of adding antimony to increase mobilities. Finally, these developments were the perfect base for a new research activity based on InSb nanowires and developed in chapter 2.

Chapter 2:
InSb nanostructures for Topological Qubits

2.1 The context: classical and quantum computers

In classical computers, information is stored and processed using transistors, that can be turned "On" or "Off" to represent the Boolean values "0" or "1", respectively. Quantum computers, on the other hand, use quantum bits (Qubits), which are fundamentally different from classical ones. Qubits can take not only |0> or |1> states, but also a superposition of both at the same time, thanks to the principles of quantum mechanics (**figure 24**). Qubits can thus represent multiple states simultaneously, and computations can be performed in parallel. Moreover, Qubits can be entangled, meaning that any operation affecting one instantly changes the state of the other, no matter how far apart they are. When the two objects are entangled, the joint system can explore a larger space of states than the two individual objects. As more objects are added to such a system, the space of entangled states grows exponentially.

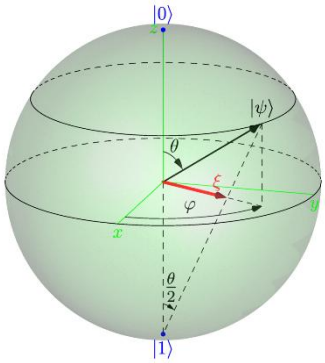


Figure 24: *The Bloch sphere*

The simplest quantum state, namely a Qubit, can be written:

$$|\psi> = cos\frac{\theta}{2}\,|0\rangle + e^{-i\varphi}\,sin\frac{\theta}{2}\,|1\rangle$$

and shown on the Bloch sphere as the vector with spherical polar coordinates θ *and* φ.

The biggest limitation to the development of Quantum computers is the fragility of the quantum information, since Qubits suffer from decoherence due to a non-ideal environment[36]. Indeed, quantum states interact strongly with particles and fields surrounding them, meaning that a quantum mechanical system can remain in a coherent superposition of states only for a short time: from a few milliseconds for a superconducting system[37] to at most one hour for an ion qubit[38]. Several routes are currently explored by both industrial and academic teams such as superconductor resonators based on Josephson junctions, gate defined spin Qubits, spin defects in solids, hyperfine states in trapped ion systems, etc.

An alternative approach, known as topological quantum computing, eliminates the issue of decoherence by making the system immune to the environment. Here, Qubits are prepared non-locally meaning that local interactions with the environment are impossible. However, most physical systems only have local degrees of freedom that are sensitive to local perturbations, making material systems with topological degrees of freedom uncommon in the real world.

2.2 Majorana Zero-Modes and Topological Qubits

In Quantum Physics, the Schrödinger equation is used to describe the wave-function of a quantum mechanical system. It was proposed in 1926 by Erwin Schrödinger[39] and is conceptually the quantum counterpart of Newton's second law describing the path of a physical system over time depending of the initial conditions. It can be written:

$$i\hbar \frac{\partial}{\partial t}|\psi(r,t)\rangle = \hat{H}|\psi(r,t)\rangle \qquad (1)$$

where i is the imaginary unit, $\hbar$ is the Planck constant divided by 2π, $\frac{\partial}{\partial t}$ indicates a partial derivative with respect to time t, ψ is the wave function of the quantum system and $\hat{H}$ is the Hamiltonian operator.

In order to make equation (1) consistent with the special relativity, Paul Dirac proposed a new relativistic wave equation in 1930[40]. Considering the four-dimensional spacetime symmetry, the introduction of 4x4 matrices is needed, turning equation (1) into:

$$i\hbar \frac{\partial}{\partial t}\psi(x,t) = (\beta\, mc^2 \,-\, c\, \sum_{n=1}^{3} \alpha_n p_n)\, \psi(x,t) \qquad (2)$$

with m is particle mass, x and t are the space and time coordinates, c is the speed of light and p_n are the components of the movement operator. α_n and β are 4x4 matrices implying that $\psi(x,t)$, the wave function, has four components.

A direct consequence of this formulation is the concept of "particle and antiparticle" also proposed by Dirac. When considering spin ½ particles (fermion), the positive-energy solutions of equation (2) describe electrons, and negative-energy solutions describe particles with the same mass and spin but opposite charge, known as positrons. Their existence was later confirmed in 1932 by Carl David Anderson. Dirac's fermions are thus described by complex wave functions; the wave function of the positron (the antiparticle) being the complex conjugate of the wave function of the electron (the particle). In 1937, Ettore Majorana proposed a new solution for Dirac's equation, excluding imaginary numbers, and thus theoretically predicted a new class of fermions : the Majorana fermions (MFs)[41]. They correspond to the real wave functions solutions of equation (2), and are thus particles that are their own antiparticles. So far, there has been no evidence of the existence of MFs as elementary particles.

In a theoretical paper from 2001[42], Kitaev proposed to engineer Majorana operators in solid-state-systems. They can be described as quasi-particles or mathematic operators that have the same properties as Majorana fermions, and correspond to "vortex" in condensed matter systems. They are interesting tools for building a Quantum computers due to their exotic non-Abelian exchange statistics[43]. Indeed, all known bosons and fermions obey the following principle: when two indistinguishable particles exchange their positions, the ground state of the system remains unchanged. On the other hand, when two Majorana quasiparticles exchange positions, the system transition from one quantum ground state to another distinct one. This unique behavior can be used to store and process information in pairs of Majorana

quasiparticles spatially separated by a superconducting gap. Qubits would thus be topologically protected against local perturbations, which would increase their coherence time. Finally, two theoretician groups[44,45] proposed in 2010 a simple recipe to engineer pairs of Majoranas in nanowire devices: if a one-dimensional semiconductor nanowire with strong spin-orbit Rashba interactions is weakly coupled to a superconductor, Majorana quasiparticles should emerge at the ends of this hybrid system as a single state in the middle of the proximity-induced superconducting gap. Two years after this proposal, we reported "signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices"[6] (figure 25).

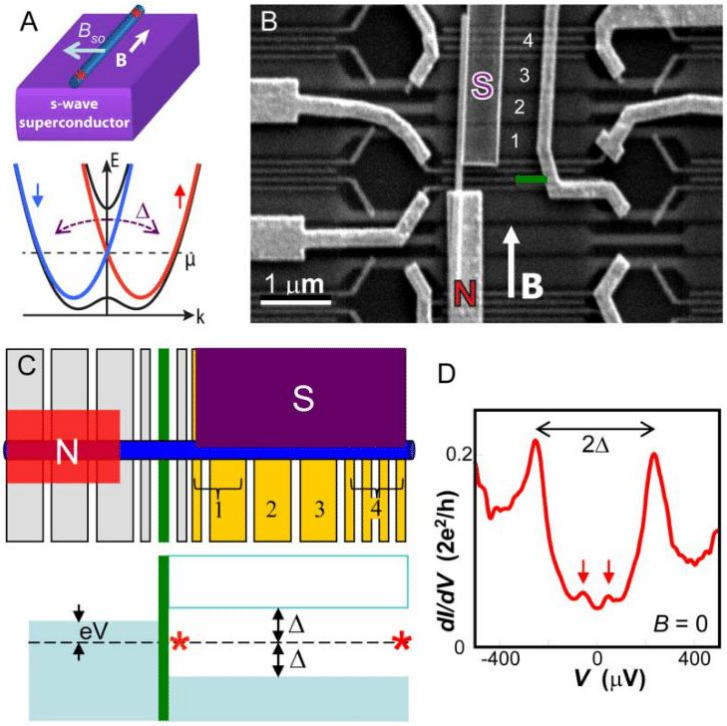


Figure 25: ***(A)*** *Outline of theoretical proposals. (Top) Conceptual device layout with a semiconducting nanowire in proximity to an s-wave superconductor. An external B-field is aligned parallel to the wire. The Rashba spin-orbit interaction is indicated as an effective magnetic field, B_{so}, pointing perpendicular to the nanowire. The red stars indicate the expected locations of a Majorana pair. (Bottom) Energy, E, versus momentum, k, for a 1D wire with Rashba spin-orbit interaction, which shifts the spin-down band (blue) to the left and spin-up band (red) to the right. Blue and red parabola are for B = 0. Black curves are for B ≠ 0, illustrating the formation of a gap near k = 0 of size $g\mu_B B$. (μ is the Fermi energy with μ = 0 defined at crossing of parabolas at k = 0). The superconductor induces pairing between states of opposite momentum and opposite spin creating a gap of size Δ.* ***(B)*** *Implemented version of theoretical proposals. Scanning electron microscope image of the device with normal (N) and superconducting (S) contacts. The S-contact only covers the right part of the nanowire. The underlying gates, numbered 1 to 4, are covered with a dielectric. [Note that gate 1 connects two gates and gate 4 connects four narrow gates; see (C).]* ***(C)*** *(Top) Schematic of our device. (Down) illustration of energy states. Green indicates the tunnel barrier separating the normal part of the nanowire on the left from the wire section with induced superconducting gap, Δ. [In (B) the barrier gate is also marked green.] An external voltage, V, applied between N and S drops across the tunnel barrier. Red stars again indicate the idealized locations of the Majorana pair. Only the left Majorana is probed in this experiment.* ***(D)*** *Example of differential conductance, dI/dV, versus V at B = 0 and 65 mK, serving as a spectroscopic measurement on the density of states in the nanowire region below the superconductor. The two large peaks, separated by 2Δ, correspond to the quasiparticle singularities above the induced gap. Two smaller subgap peaks, indicated by arrows, likely correspond to Andreev bound states located symmetrically around zero energy. Measurements are performed in dilution refrigerators using standard low-frequency lock-in technique (frequency 77 Hz, excitation 3 μV) in the four-terminal (devices 1 and 3) or two-terminal (device 2) current-voltage geometry.*

2.3 Necessary ingredients for Majorana quasiparticles

Following the 2010 recipes[44,45], four ingredients are mandatory to engineer Majorana quasiparticles in solid-states systems:

- A one-dimensional (1D) system with a few (ideally one) conducting channels
- A semiconductor with strong spin-orbit interactions
- An induced superconductivity
- An external magnetic field

If the external magnetic field is linked to the experimental setup, the three other requirements are more stringent and need to be optimized together. Indeed, the induced superconductivity will depend of the nature of the superconductor, the quality of interfaces and the applied external magnetic field. The strong spin-orbit semiconductor needs to be one dimensional with few conducting channels, no structural defects and flat surfaces. Moreover, it is important to find semiconductors having large Landé g-factors to ensure that the generation of Majorana quasiparticles happens at the lower values of the applied magnetic field. In 2012, all these requirements narrowed down the semiconductor material choice to InAs or InSb nanowires[6,46], both having advantages and drawbacks listed in the following table.

Properties	InAs nanowires	InSb nanowires
Controlled crystalline structure	Wurtzite	Zinc-blend
Maximum length	< 2 µm[46,47]	< 1 µm[23,48]
Diameter of longest nanowires	> 50 nm[46,47]	> 80 nm[23,48]
Landé g-factor	~ 10[49]	~ 70[50]
Surfaces / facets	{11-20} flat	{110} atomically flat

Table 3: *Fundamental properties of InAs and InSb nanowires.*

Considering the device fabrication requirements (see **figure 25b**), nanowires should be at least 2µm long, their diameter should be reduced to limit the number of parallel conduction channels and facets should be as flat as possible to optimize interfaces. If the InAs nanowire morphological aspects are more fitting the necessities, the fundamental InSb properties remain best adapted for Majorana devices. Another advantage of InSb compared to InAs is the possibility to grow single crystalline Zinc-blend (ZB) nanowires without any stacking fault or structural default[50,51]. Spin-orbit coupling effects are indeed expected to be stronger in ZB materials compared to WZ one[52] when grown in the $[\bar{1}\bar{1}\bar{1}]$ direction.

Our expertise in this field led us to define a roadmap articulated around four axes:

- The optimization of the InSb nanowire aspect ratio
- The determination of the InSb nanowire transport properties
- The synthesis of hybrid semi- / super- conductor interfaces
- The growth of multi-branched InSb nanostructures for braiding

2.4 Optimization of the InSb nanowire aspect ratio[53]

General remark: *I choose to extensively developed this 2.4 section in order to give hints about the research methods and analysis tools I used during my carrier. Following sections are more synthetized and only provide main results.*

InSb is a narrow bandgap semiconductor (0.17 eV) with a high electron mobility (77 000 $cm^2V^{-1}s^{-1}$ in part due to the small electron mass (0.015 m_e)[54]. It crystalizes in a Zinc-blend crystalline structure, with a 6.48 Å lattice constant. InSb nanowires can be grown by molecular beam epitaxy (MBE)[27], chemical beam epitaxy (CBE)[48] and metal organic vapor phase epitaxy (MOVPE)[51]; using gold as a catalyst. The growth direction is $[\bar{1}\bar{1}\bar{1}]$, as for most of the nanowires grown using the Vapor-Liquid-Solid (VLS) growth mechanism. Due to the antimony surfactant effect, stems[51] or patterning[55] are mandatory for InSb nanowire nucleation. Moreover, because of the Majorana devices manufacturing constraints, InSb nanowires should be at least 2 µm long for the establishment of a robust topological superconducting phase and less than 100 nm thick for electrostatic gating (**figure 25b**). Best aspect ratios are obtained by MOVPE since low growth temperature are possible, with precursors being cracked only around the gold catalyst in the gas phase. This reduces the lateral growth on the nanowire facets due to the Vapor-Solid (VS) parasitic overgrowth. Our first option was thus to conduct a parametric growth study in order to understand and optimize the InSb nanowire growth by MOVPE. We defined ordered arrays of Au islands on (111)B InP substrates by electron beam lithography before growth of InP and InAs stems. Here our goal was to perfectly control the growth environment. The InP is used to facilitate uniform nanowire nucleation, and the InAs is used to reduce the lattice mismatch with InSb. Since the InSb growth temperature is low (470°C) precursors are mostly cracked around the gold droplets and not on the substrate, which limit the nanowire diameter increase. An example of optimized growth[53] is reported in **figure 26**.

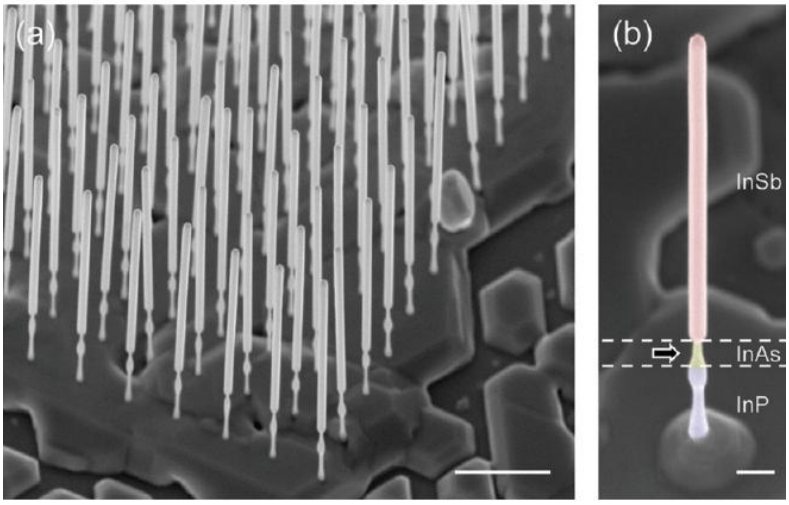


Figure 26: *30° tilted SEM images of an InSb nanowire array.* ***(a)*** *Low-magnification image of a 25 × 25 nanowire array with a yield of over 95% grown using optimized parameters for 50 nm droplets: pitch = 500 nm and V/III = 26.4. Scale bar corresponds to 1 µm.* ***(b)*** *High magnification image of a single nanowire. Color indicates the stacking of materials: InP (blue), InAs (yellow), and InSb (red). Scale bar corresponds to 200 nm.*

2.4.1 Influence of the V/III ratio

Since we fixed the InSb growth temperature to 470°C, the next most important parameter controlling the nanowire shape is the V/III ratio. Indeed, in these conditions, less than ten percent of the precursors [trimethylindium (TMI) and trimethylantimony (TMSb)] are cracked at the substrate surface. The catalytic role of gold droplets is thus predominant and lateral growth is limited. A qualitative examination of the nanowire morphology relative to the V/III ratio is reported in **figure 27**. Here, the V/III ratio is increased from 44 to 166 by maintaining a constant TMI flow, while increasing the TMSb one at constant pitch (500 nm) and a droplet diameter (50 nm). Note that, with a yield exceeding 90%, statistical analysis of lengths and diameters become possible. Throughout this series, the morphology of InSb transformed from thin and elongated nanowires (**figure 27a**, aspect ratio ~14), to thick and shorter nanowires (**figure 27b**, aspect ratio ~6), and finally to nanocubes (**figures 27c,d**, aspect ratio ~1). Typically, an increase in radial growth rate accompanies higher V/III ratios, a phenomenon already observed for other III/V semiconductor nanowires growth[56,57]. Lower V/III ratios tend thus to produce longer and thinner InSb nanowires.

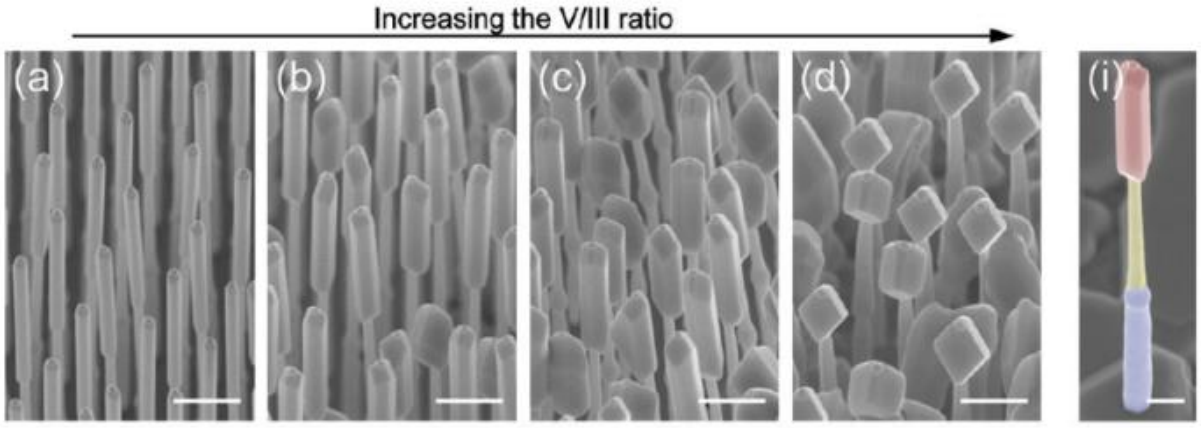


Figure 27: *The 30° tilted SEM images illustrating the evolution of the InSb nanowire morphology. In all cases, the gold catalyst size is 50 nm. (a–d) Nanowire morphology as a function of the V/III ratio: (a) 44, (b) 66, (c) 88, and (d) 166 for a constant pitch of 500 nm. Scale bars correspond to 500 nm. (i) Nanowire material stacking, colors are the same as in* ***figure 26****. Scale bar correspond to 200 nm.*

2.4.2 Influence of the nanowire interdistance

Next, we probed the influence of the local environment on the InSb nanowire shape. In **figure 28e–h**, we depict the evolution of the InSb segment as we increase the wire-to-wire distance (pitch) from 400 to 1200 nm, while maintaining a constant V/III ratio of 44 and a droplet diameter of 50 nm. A similar transformation from thin nanowires (**figure 28e**) to thicker nanowires (**figure 28f**) and ultimately to nanocubes (**figure 28g,h**) is evident. Given that the only variable here is the nanowires interdistance, we deduce that the "local" V/III ratio around the nanowire is contingent upon nanowires density. This fluctuation in the V/III ratio arises from differences in the diffusion lengths of various precursors on the substrate surface. By observing the resemblance between the structures obtained by altering the V/III ratio and the pitch, we surmise that decreasing the density (increasing pitch) results in more antimony available per

wire, thereby elevating the V/III ratio. This fundamental insight, indicating the paramount importance of the "local" environment at the nanoscale compared to global growth parameters, serves as the guiding principle for all subsequent studies.

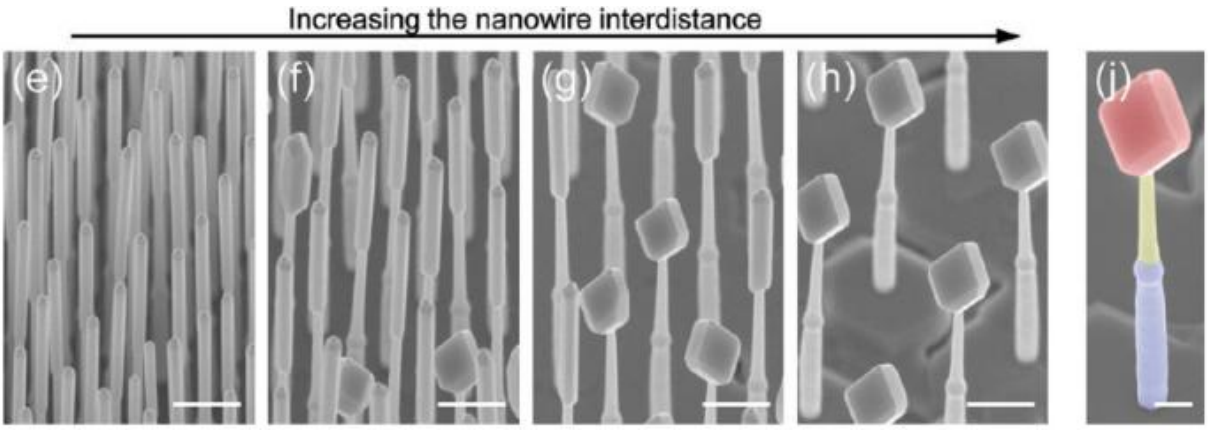


Figure 28: *The 30° tilted SEM images illustrating the evolution of the InSb nanowire morphology. In all cases, the gold catalyst size is 50 nm. (e–h) Nanowire morphology as a function of the pitch: (e) 400, (f) 600, (g) 800, and (h) 1200 nm for a constant V/III ratio of 44. Scale bars correspond to 500 nm. (j) Nanocube material stacking, colors are the same as in* ***figure 26****. Scale bars correspond to 200 nm.*

2.4.3 Statistical analysis of the InSb nanowire growth

Now that the qualitative evolution of the nanowire morphology is understood, we switch to a quantitative study. Here, mean nanowire lengths and diameters are extracted from SEM images and reported in figure 29. Several conclusions can be drawn from this dataset:

- An optimum aspect ratio is achieved around 500 nm pitches, where wires have a reduced diameter, and length are almost maximized. This underlines the fundamental importance of controlling the local environment and adapting the growth parameters to the density and the droplet diameter.
- For smaller pitches, a competitive growth mode[58] is observed due to a too high density of nanowires. In that case, the nanowire growth rate increases with the Sb pressure, confirming that Sb diffusion is the rate-limiting factor for vertical growth: the amount of antimony available per wire decreases with decreasing pitch.
- Above 500 nm pitches, the vertical growth rate also decreases. Unlike in GaP wires, where a similar decrease was attributed to the catalytic decomposition of one of the precursors[59], here the particle composition and the local V/III ratio are the limiting factors.

Indeed, the relationship between the V/III ratio and droplet composition during growth is crucial[60]. At the optimum, we observe an $AuIn_2$ droplet composition, which aligns with predictions from the Au/In/Sb ternary phase diagram ($AuIn_2$ is a stable phase[61]). Expanding on this observation, we propose an hypothesis: a low local Antimony concentration, occurring at low V/III ratios and small pitches, leads to an Indium accumulation in the droplet, forming $AuIn_x$

(x > 2) particles. This accumulation, with a constant gold content, increases the droplet volume and consequently the nanowire diameter. If we apply this hypothesis to the curve corresponding to the smallest V/III ratio in **figure 29b**, it suggests three distinct regimes. First, a minimum diameter is observed for $AuIn_2$ droplets (at a 500 nm pitch). For smaller pitches, $AuIn_x$ (x > 2) droplets form, resulting in an increased particle volume and consequently in an increased nanowire diameter. Conversely, for larger pitches (>400 nm), $AuIn_xSb_y$ droplets are formed[62], where both radial growth induced by the high local V/III ratio and an increase in particle volume contribute to larger nanowire diameters. Remarkably, when correlating **figures 29a,b** a "sweet spot" emerges, where nanowires exhibit the lowest radial and highest axial growth rates, leading to the highest aspect ratio. Further optimization of the V/III ratio allowed the production of InSb nanowires with an enhanced aspect ratio of 35, a diameter < 100 nm, and a length of 3.5 µm, as depicted in **figure 26**.

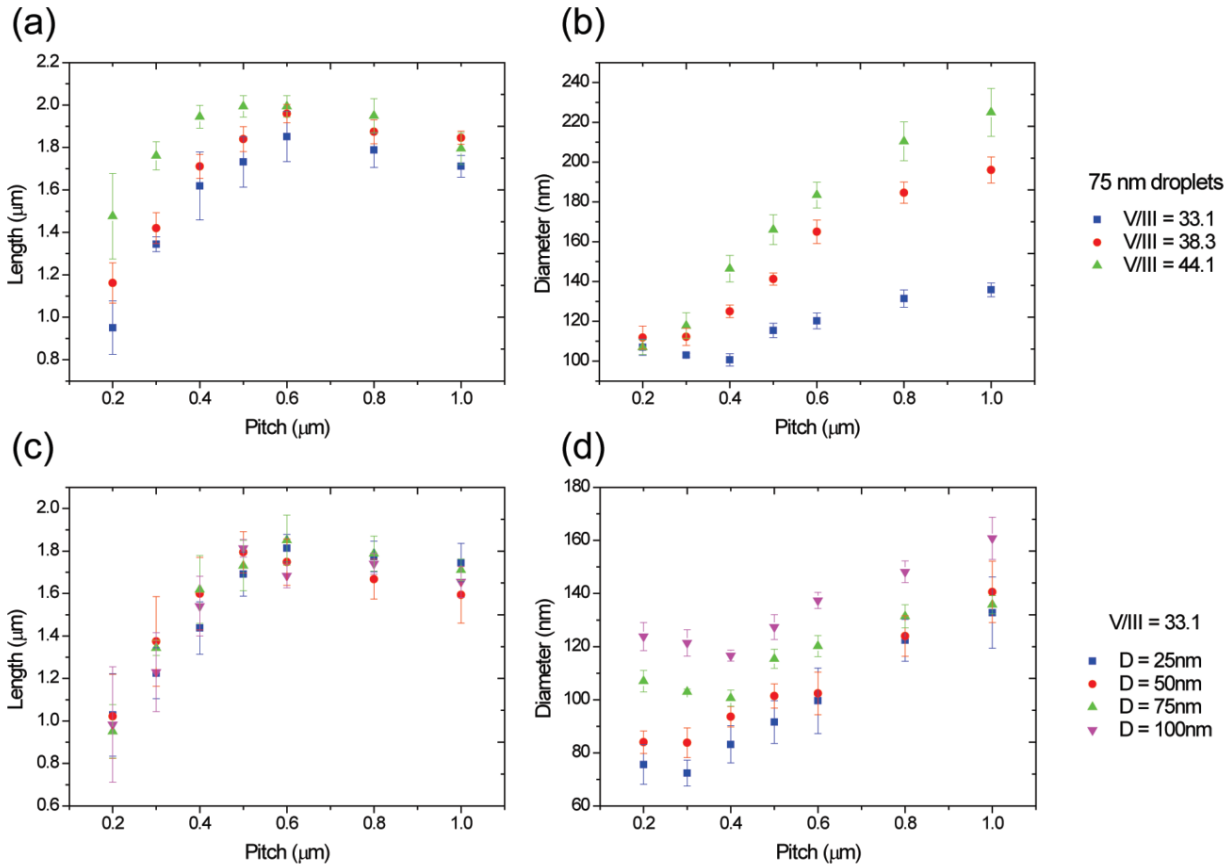


Figure 29: *Statistics on the InSb nanowire arrays. At least 10 nanowires were measured for each point and the error bars represent the standard deviation. Since the InSb growth time is constant (20 min) length and vertical growth rate are proportional.* ***(a)*** *Evolution of the length of the InSb segment as a function of the pitch for a droplet size of 75 nm and for different V/III ratios.* ***(b)*** *Evolution of the diameter of the InSb segment as a function of the pitch for a droplet size of 75 nm and for different V/III ratios.* ***(c)*** *Evolution of the InSb length as a function of the pitch for a V/III ratio equal to 33.1 and for different droplet sizes.* ***(d)*** *Evolution of the diameter in function of the pitch for a V/III ratio equal to 33.1 and for different gold diameters.*

The evolution of InSb wire length with pitch, for a range of droplet sizes but a fixed V/III ratio (33.1), is depicted in **figure 29c**. It is noteworthy that the maximum growth rate coincides with the same pitch as in **figure 26a**. Surprisingly, the droplet diameter, ranging from 25 to 100 nm, has no significant effect on the vertical growth rate for the pitches used here. This stands in contrast to other III-V nanowire growth reports[63,64], which typically suggest a synergetic effects[59], implying an increased growth rate for larger particles and pitches. If growth at the smallest pitches were solely controlled by the competitive mechanism, one would expect a higher vertical growth rate for smaller particles. However, no diameter dependence is observed, suggesting that the diffusion-limited process is compensated by another mechanism. One possible candidate is the Gibbs–Thomson effect, although its effect should be relatively small at these relatively large droplet sizes[65,66]. Importantly, the observed vertical growth rates significantly surpass those reported in previous studies[48,51], which is crucial for enhancing the InSb nanowire aspect ratio. **Figure 29d** illustrates the evolution of the nanowire diameter as a function of the pitch for different gold particle sizes but a constant V/III ratio (33.1). Logically, the nanowire diameter increases with the gold particle size, with the minimum diameter shifting towards smaller pitches for smaller droplets. Assuming that this minimum diameter corresponds to $AuIn_2$ droplets, we can deduce that smaller droplets require a lower local V/III ratio (a higher In concentration) for efficient Indium uptake, potentially confirming the relevance of the Gibbs–Thomson effect. Despite the relatively large droplet size, this effect could convincingly explain the observed trends. This was later confirmed by energy dispersive X-ray (EDX) measurements performed on the droplets, where a slight decrease of the In concentration (from 66 to 63%) with increasing pitch was observed.

Finally, the growth of optimized InSb nanowires by MOVPE was obtained in 2012. A fine tuning of both the growth conditions and the wire density was mandatory in order to achieve highest nanowire aspect ratios (35). This is mostly linked to the droplet composition during growth. These optimizations remain today the state of the art for the growth of InSb nanowires with a diameter below 100nm.

2.5 The InSb nanowire transport properties[53,67]

Now that the InSb nanowire morphology is optimized, the fundamental transport properties of these nanostructures need to be probed extensively. A general routine we developed is to transfer these nanostructures on p-doped silicon wafers covered by ~ 300 nm of SiO_2 thanks to a nanoprobe. Ohmic contacts are established through electron beam lithography followed by the deposition of Ti/Au stacks (25 nm/250 nm). Subsequently, the devices are cooled down to 4.2K for electrical measurements. The nanowire mobility is determined by analyzing the change in current with the gate voltage. This methodology relies on the field-effect mobility formalism, assuming a classical transport. To ensure operation within this regime, a source-drain bias of approximately 10 mV is applied. This bias helps to average out transport effects arising from quantum interference.

2.5.1 Method for extracting the field-effect mobility

In the Drude model of conductivity, the mobility, μ (cm^2 / Vs), is defined as the proportionally factor between an applied electric field, E, and the resulting drift velocity, v_d:

$$v_d = \mu E \qquad (3)$$

From this equation, it can be derived that the mobility is also the proportionality factor between the carrier density, n (m^{-3}), and conductivity, σ $(\Omega m)^{-1}$, of a material:

$$\sigma = \frac{J}{E} = \frac{n e v_d}{E} = n e \mu \qquad (4)$$

with J the current density and e the electron charge.

Moreover, mobility is related to the mean scattering time, τ, by the equation:

$$\mu = \frac{e\,\tau}{m^*} \qquad (5)$$

with m^* being the effective electron mass.

In semiconducting materials, several source of scattering, such as ionized impurity scattering, phonon scattering, surface scattering, defect scattering, etc., can limit the mobility. According to the Mathiessen rule[68] the net mobility μ depends on these contributions as:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \qquad (6)$$

The lowest mobility contribution therefore determines the net mobility, and mobility can therefore be improved by identifying the limiting contribution and subsequently reducing or eliminating it. In the case of nanowire-based FETs, the mobility is determined from measurements of the conductance as a function of the back-gate voltage. Indeed, the channel conductance is described by the linear region of the accumulation regime of the FET and the source drain current equals the total carriers flowing in the channel divided by the time needed to travel from source to drain:

$$I = \frac{Q}{t} = \frac{Q\,v_d}{L} \qquad (7)$$

where L is the channel length and we assume a constant drift velocity v_d

Since v_d is constant, the electric field E is also constant and equal to the source-drain voltage V_{sd} divided by the channel length L. Combining equations *(3)* and *(7)*, it comes:

$$I = \frac{Q\mu E}{L} = \frac{Q\mu V_{sd}}{L^2} \qquad (8)$$

In a FET, the charge density Q, in the active channel is proportional to the applied gate voltage V_g, and the proportionality constant is the gate-oxide capacitance C. Moreover, the charge density is null at and below the threshold voltage V_t.

$$Q = C\left(V_g - V_t\right) \; for \; V_g > V_t \quad (9)$$

Combining *(8)* and *(9)*, the expression of I in the linear regime becomes:

$$I = \mu C\left(V_g - V_t\right)\frac{V_{sd}}{L^2} \quad (10)$$

This expression is only valid in the case of $|V_{sd}| \ll \left(V_g - V_t\right)$ since this ensures that velocity, electric field and charge density remain constant between source and drain.

The conductance G is then defined as the variation of the current I as a function of the source-drain voltage V_{sd} at a fixed gate voltage V_g.

$$G\left(V_g\right) = \frac{dI}{dV_{sd}} = \frac{\mu C}{L^2}\left(V_g - V_t\right) \quad (11)$$

If the capacitance C and the channel length L are known, the field-effect mobility μ can be calculated via the transconductance g_m.

$$g_m = \frac{dG}{dV_g} \quad (12)$$

The most commonly used method to determine the mobility in nanowire-based FET is the "peak transconductance method". It involves considering a small gate voltage range to determine μ, where the transconductance has its maximum. This is typically close to the threshold voltage, when the mobility is at its maximum, which is not representative of standard working conditions. A more accurate method to determine μ is to fit the transconductance g_m over a large gate voltage range as described in figure 30. Contrary to InAs materials, InSb nanowires do not present band bending at the surface, which leads to the absence of a surface accumulation layer. A contact resistance of a few kilo ohms is thus present in the devices. Such interface resistances are known to reduce the transconductance, resulting in an underestimation of the intrinsic mobility. In this model, the interface resistances R_S has a fixed value (no gate voltage dependence), and is connected in series to the nanowire channel (figure 30a). The device conductance is then given by:

$$G\left(V_g\right) = \frac{1}{R_{NW} + R_S} = \frac{1}{\frac{L^2}{\mu C\left(V_g - V_t\right)} + R_S} \quad (13)$$

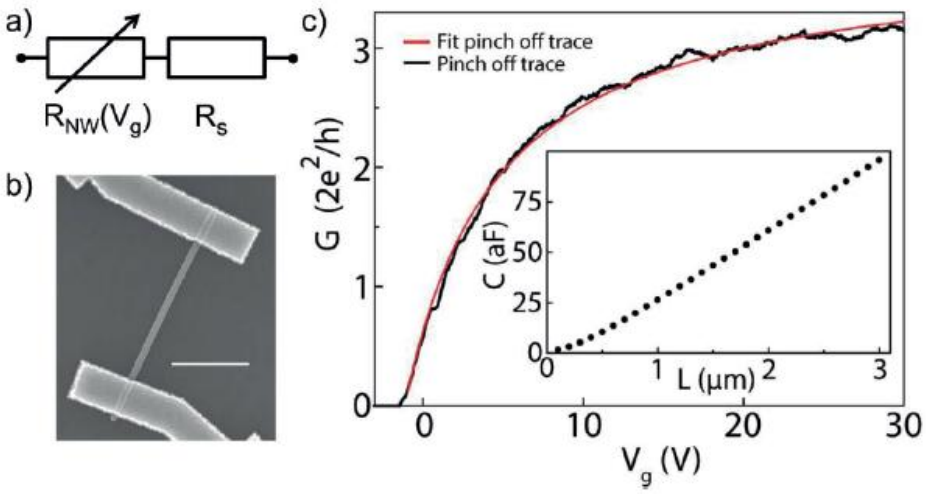


Figure 30: *Low-temperature InSb nanowire FET measurements.* ***(a)*** *Electrical diagram of the InSb nanowire FET. The FET is modelled as a nanowire channel with a resistance controlled by a nearby gate, $R_{NW}(Vg) = G_{NW}^{-1}(V_g)$, in series with fixed interface resistances, R_S.* ***(b)*** *Scanning electron micrograph of a representative InSb nanowire FET. The scale bar corresponds to 1 µm.* ***(c)*** *Conductance G, as a function of back gate voltage V_g (black curve). Source-drain bias is set to 10 mV. Field effect mobility is extracted from a fit to the conductance (red curve) using equation (13), resulting in reproducible average mobility of 2,5 x 10^4 $cm^2V^{-1}s^{-1}$. Measurements are performed at a temperature of 4.2 K. Inset: Gate-nanowire capacitance C, as a function of source-drain contact spacing L. Capacitance is extracted from a finite element model of the device geometry. Contacts are included in the simulated device geometry and lead to a non-linear C(L) at small contact spacing.*

Fitting the measured values $G(V_g)$, it is then possible to extract the field effect mobility using equation *(13)*. Here, the product of mobility and capacitance μC, interface resistance R_S and threshold voltage V_t are the free fit parameters. The mobility can be obtained from μC upon determining the capacitance. As a result, for a measured $G(V_g)$ curve, the extracted mobility is inversely proportional to the capacitance value. The capacitance for different channel lengths is calculated from a finite element model of the device, considering that quantum confinement reduces the classical capacitance by roughly twenty per cent[69]. The main drawback of this method is the uncertainty in the calculated capacitance value which directly affects the extracted mobility.

2.5.2 The particular case of InSb nanowire in Majorana devices

In the context of Majorana devices (**figure 25b**), this general method can be applied as follow. First, our goal is to induce the superconductivity in the InSb nanowire at low temperature. Phenomena occurring at higher temperatures, such as phonon scattering, can therefore be neglected. As presented in **figure 23**, the crystalline structure of the InSb nanowires is pure Zinc-Blend without any stacking fault or punctual defect, nanowires are non-intentionally doped and facets are atomically flat on large terraces[26]. We assume a mobility independent of gate voltage. The saturation of conductance at high gate voltage is then due to the presence of both an instrumental resistance and interface resistances. Note that the

instrumental resistance is subtracted in all following gate traces. The field-effect mobility obtained from peak transconductance and the field-effect mobility obtained from the fit according to equation *(13)* yield to very similar values.

We applied this method to the high aspect ratio nanowires presented in **figure 26**. The current–voltage characteristics reveal an ohmic (linear) behavior for a wide range of gate voltages away from pinch-off (**figure 31b**). To determine the electron mobility, the source–drain current ***I*** is measured at a fixed source–drain voltage V_{sd} = *10 mV* as a function of the global gate voltage ***Vg*** as shown in **figure 31c**. From the linear part of the transconductance $g_m = \frac{dG}{dV_g}$, (**figure 31c**) the field-effect mobility $\mu = \frac{L^2 g_m}{C}$ can be calculated, where L is the length of the nanowire segment between the two contacts. The C capacitance between the nanowire and the back gate is estimated from a finite elements model that includes charge screening from source and drain contacts. Mobilities are determined for six devices and values ranging from 2.0×10^4 to 3.5×10^4 cm^2 V^{-1} s^{-1} are obtained. For an electron density of 1×10^{17} cm^{-3}, a mean free path of 260 nm is calculated. **The mean free path exceeds the nanowire diameter of ~100 nm suggesting a quasi-ballistic transport regime with multiple specular reflections**. These mobilities were the highest reported in 2012 for InSb nanowires but much lower than that of bulk material. Possible mechanisms for electron scattering, reducing the mobility, include surface roughness and impurity induced disorder inside the nanowires due to the device fabrication processes. For few devices, a sulfur passivation of the wire was performed, prior to covering them with SiO_2, but no influence on mobilities is observed.

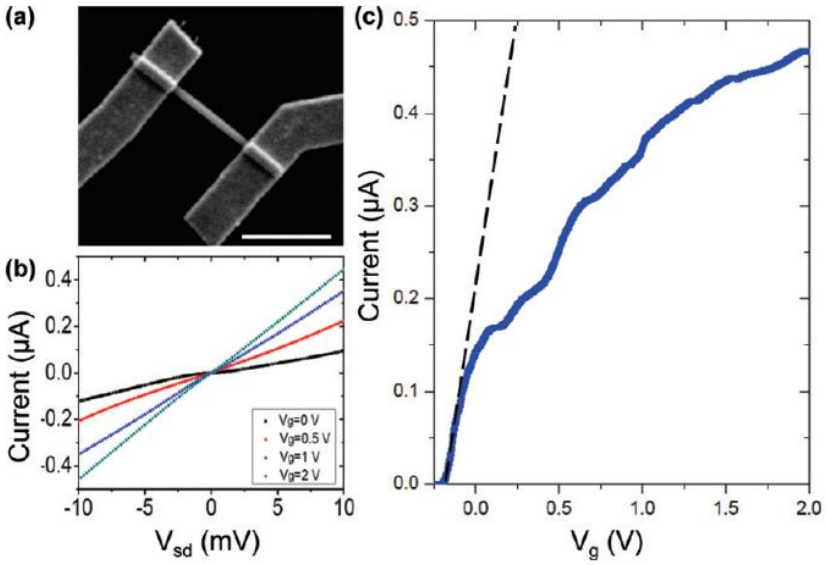


Figure 31: Electrical measurements on the InSb nanowires. **(a)** A SEM image of an InSb nanowire with Ti/Au source–drain contacts, lying on a 285 nm thick SiO_2 substrate. A p-doped Si layer underneath the SiO_2 acts as a global back gate. Scale bar corresponds to 1 µm. **(b)** Current as a function of source–drain voltage for a global gate voltage of 0, 0.5, 1, and 2 V. **(c)**. Current through the nanowire is modulated by the voltage applied to the global back gate, source–drain bias voltage V_{sd} = 10 mV. The dashed line indicates the transconductance in the region near pinch-off from which the field-effect mobility is obtained. A series resistance of 15 kΩ originating from the wirecontact interface and measurement setup was subtracted. Capacitance obtained from finite elements calculations is 40 aF.

2.5.3 Quantized conductance in InSb nanowire devices

The formation of subbands in (ballistic) 1D wires is shown in transport measurements by quantization of conductance, where each spin-degenerate subband contributes a conductance of $g_Q = \frac{2e^2}{h}$ [70]. In semiconductor nanowires, conductance quantization is hard to achieve, as it requires strong suppression of disorder between source and drain contact, a distance of typically several hundred nanometers to a few micrometers. Disorder, both due to structural imperfections and surface states, leads to scattering of electrons. Due to the nanowire radial confinement, this often results in reflection of electrons back to the reservoir from which they originated: the backscattering (**figure 32a**), which erases the conductance quantization. In two-dimensional geometries, scattering centers outside of the 1D constriction are less harmful to conductance quantization, as they will only affect the trajectories of a small percentage of electrons. In 2012, only a few core-shell Si/Ge nanowire presented signs of conductance quantization[71,72].

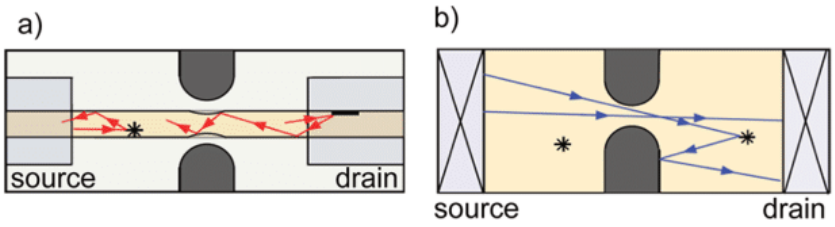


Figure 32: *Consequences of scattering in nanowires and two-dimensional geometries.* ***(a)*** *Transport through a constriction in a nanowire. Scattering at an impurity reflects an electron back to the source reservoir. Reflection at the reservoirs, here drawn for the drain reservoir, also leads to backscattering.* ***(b)*** *Transport through a constriction in a two-dimensional geometry in the presence of scattering centers. Note that, compared to the 1D nanowire in panel* ***(a)****, a scatterer only affects a small number of the ballistic trajectories from source to drain reservoir and that scattering is less likely to lead to scattering through the 1D constriction.*

In order to probe possible quantification of conductance in InSb nanowires, a device similar to the one presented in **figure 31** was measured at low temperature, under an external magnetic field of 4T. The spacing of the two metal contacts in the device studied in **figure 33a** (~200 nm) is comparable to the electron mean free path of ~260 nm extracted from measurements of field-effect mobility. On application of an in-plane magnetic field we observed different conductance steps as a function of backgate voltage (**figure 33c**). The conductance at the two plateaus is $g \approx 0.5g_Q$ and $g \approx 1g_Q$, corresponding to transport through the lowest subband 1↑ and through the 1↑ and 1↓ subband, respectively (**figure 33d**). Subbands are denoted by an index, with 1 the subband lowest in energy, and spin-split subbands (↑ or ↓) that are degenerate in the absence of magnetic field have the same number.

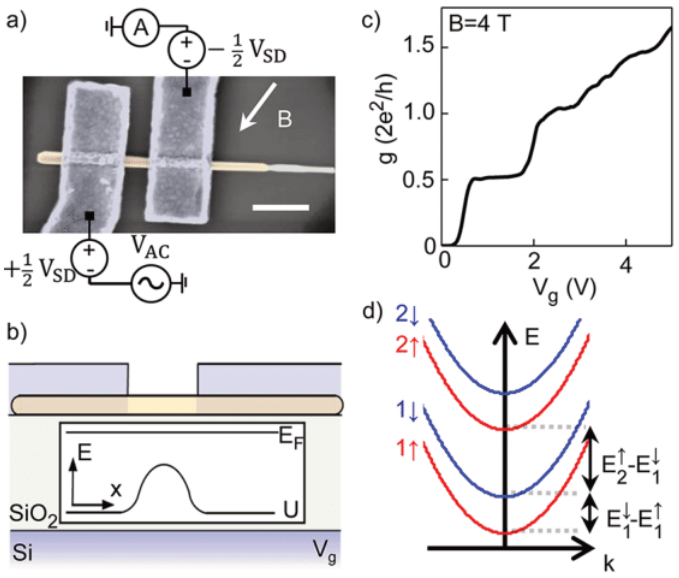


Figure 33: *Quantized conductance in an InSb nanowire.* ***(a)*** *SEM image of a contacted InSb nanowire similar to the one measured. The direction of the in-plane magnetic field B with respect to the wire is indicated by a white arrow. The angle between nanowire and magnetic field is 53° ± 5°. Differential conductance g = dI/dV = I_{AC}/V_{AC} is obtained from a 50 μV_{RMS} excitation V_{AC}. The source-drain bias V_{SD} is applied antisymmetrically across the sample. The scale bar is 500 nm. All measurements were performed at a temperature of 4.2 K.* ***(b)*** *Schematic drawing of the nanowire lying on a Si substrate covered with 285 nm SiO2. The highly p-doped Si acts as a global backgate to which a voltage V_g is applied. The inset shows the electrostatic potential U created by the backgate voltage V_g. The electrostatic potential leads to the formation of a constriction in the wire in the region between the two contacts.* ***(c)*** *Conductance g as a function of backgate voltage V_g at B = 4 T (V_{SD} = 0 mV) shows plateaus at 0.5 and 1.0 conductance quanta g_Q ($2e^2/h$). A series resistance of 6 kΩ has been subtracted, corresponding to the impedance of the current amplifier (3 kΩ) and the contact resistance at the interface of the InSb wire and the metal contact. In these conditions, the conductance of the second plateau is 1.0 g_Q.* ***(d)*** *At nonzero magnetic field the energy spectrum consists of spin-split subbands n{↑,↓}. The energy spacing between subbands 1↓ and 1↑, where g = 0.5g_Q, is denoted as E1↓ − E1↑. The energy spacing between 2↑ and 1↓ (g = 1.0g_Q) is denoted as E2↑ − E1↓.*

Here, the 1D conductance channels show a nonlinear conductance as a function of the DC source-drain bias V_{SD}. So-called half-plateaus at intermediate conductance values (g ≈ 0.25g_Q, 0.75g_Q) arise at high V_{SD}, when the number of subbands available for electrons from source or drain reservoir differs by 1[73]. Moreover, the 0.5g_Q and 1.0g_Q plateaus (**figure 34a,b**) observed for V_{SD} = 0 mV, evolve into these intermediate plateaus at high source-drain bias (V_{SD} ~ ± 11 mV), which further confirms the quantized conductance.

The derivative of conductance to gate voltage, the transconductance dg/dV_g, of the same nonlinear transport data (**figure 34c**) shows the subband alignment with respect to source and drain reservoir as a function of gate voltage and source-drain bias. Zero-bias and high-bias plateaus (zero transconductance) are separated by lines of high transconductance that arise when a subband aligns with source or drain reservoir. Two high transconductance lines intersect at finite V_{SD} when source and drain are aligned with successive subbands. This is seen in **figure 34c** for the 1↑ and 1↓ subbands at V_{SD} = 14 mV (point marked with *). In this configuration[74], the source-drain potential eV_{SD} equals the subband spacing E1↓ − E1↑, as depicted schematically in **figure 34d**. We therefore extract an energy spacing E1↓ − E1↑ (B = 4T), which is also the Zeeman energy at B = 4T, of 14 meV.

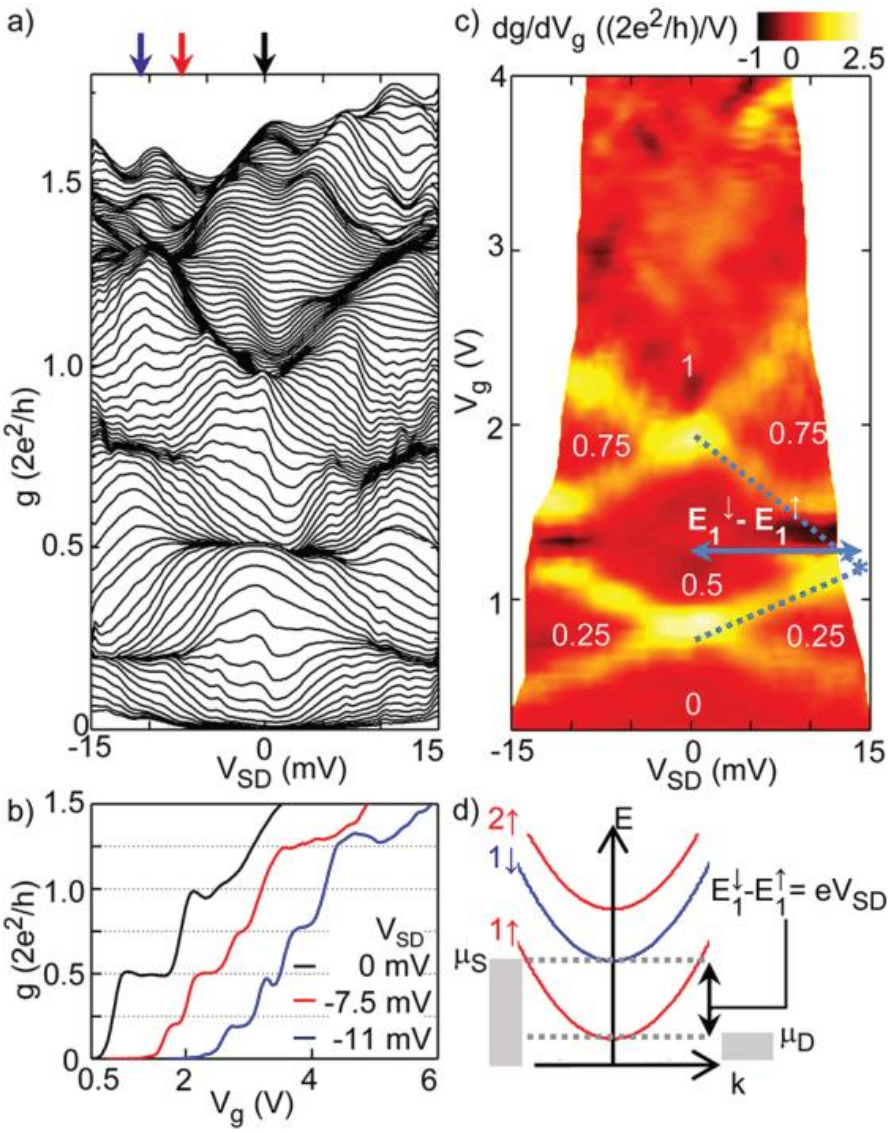


Figure 34: *Voltage bias spectroscopy.* ***(a)*** *Conductance as a function of source–drain voltage V_{SD}. Each trace is taken with fixed V_g between −0.25 and 4 V and plotted without offset between traces. Dense regions correspond to conductance plateaus. Data obtained at B = 4T.* ***(b)*** *Gate traces at V_{SD} = 0 mV (black), V_{SD} = −7.5 mV (red), and V_{SD} = −11 mV (blue), corresponding to the location of the arrows in panel* ***(a)****. The bump at g = 0.5g_Q in the trace taken at V_{SD} = −11 mV is an electronics artifact.* ***(c)*** *Transconductance dg/dV_g of the data in panel a shows plateaus (zero transconductance, red) separated by transitions between plateaus with high transconductance (yellow / white). The conductance of the plateaus is indicated. The intersection of two regions of high transconductance surrounding the 0.5 plateau at finite V_{SD} (indicated with *) allows extraction of the energy E1↓ − E1↑.* ***(d)*** *The intersection of the high-transconductance regions at high source-drain bias (point * in panel c) corresponds to the alignment of the electrochemical potential of the source with spin-split subband 1↓, while the drain potential is aligned with spin-split subband 1↑. The source–drain potential eV_{SD} equals the subband spacing E1↓ − E1↑.*

Moreover, we observed that the subband spacing E1↓ − E1↑, obtained from voltage bias spectroscopy measurements, increases with magnetic field[67]. We extracted from a linear fit, a |g| factor of the first subband $|g_1| \sim 60$, which is higher than the bulk InSb value of 51. Although the spin-orbit interaction is known to influence |g| factors in confined geometries[50,75], the enhanced value extracted here most likely originates from exchange enhancement in low density quantum point contacts[76,77].

To summarize, we reported electron mobilities up to 35 000 $cm^2V^{-1}s^{-1}$ in InSb nanowire FETs, which remains the state-of-the-art for sub-100nm InSb nanowires. A clear quantized conductance was observed at nonzero magnetic fields, and Landé g factors about 60 and a subband spacing of ∼14 meV were measured. These physical properties are compatible with requirements presented in **section 2.3** for implementing Majorana zero modes in hybrid interfaces. Next ingredient is to induce superconductivity in the wires.

2.6 The Hybrid semi- / super- conductor interfaces[78]

Now that optimized InSb nanowires having good enough transport properties are obtained, the next step is to locally deposit a superconductor such as aluminum (Al) or niobium (Nb). Both materials are widely used for device fabrication in the quantum physics field, and their fundamental properties have been extensively studied. Aluminum is a type I superconductor with a critical temperature T_c of 1.2K and a critical magnetic field H_c of 0.01T, whereas Nb is type II with a T_c of 9.26K and a H_c of 0.82T. Niobium is rarely used alone, and is often combined with Ti and/or N, since NbTi and NbN are both type II superconductors having higher T_c (10K and 16K respectively) and H_c (15T and 35T respectively). Nevertheless, the important parameter is not the fundamental material properties but the induced superconductivity in the InSb nanowires, that mostly depend on the interface quality. Since Majorana devices are measured at low temperature using an external magnetic field, niobium appears to better meet the recipe requirements; however, aluminum can be epitaxially integrated at low temperatures, which improves the interface quality[79]. The MBE integration of a high-quality Al layer requires growth at cryogenic temperature in order to prevent Al to diffuse on the substrate surface and merge into faceted island. Due to this technical limitation, we started to work with evaporated and sputtered superconductors. Cryogenic growth of superconductors will be discussed in the perspectives.

Tunneling spectroscopy studies on proximitized InSb nanowires have revealed a substantial density of states within the superconducting gap[6,80,81], known as a soft gap, indicating an inhomogeneous interface. These subgap states destroy the topological protection by allowing excitations with arbitrarily small energy, and prevent any measurement of MZM. Realizing a hybrid device begins thus with a surface preparation of the host material prior to the superconductor deposition. In our case, InSb nanowires are mechanically transferred on a SiO_2 wafer thanks to a nanoprobe in a SEM and the superconductor is deposited afterward. The InSb surface is thus oxidized and partially polluted (carbon in the SEM). Several devices have been fabricated using the procedure developed for measuring the mobility in InSb nanowires, adding

a cleaning step of the surfaces and testing different superconductors. First, either a sulfur-based solution or an in-situ argon etching plasma is used to clean the wire facets. Next, the superconductor is deposited by either evaporation of Al (**figure 35c**) or sputtering of NbTiN (**figure 35e**). Note that in the case of Al, a Ti wetting layer is added in order to improve the Al homogeneity and reduce its roughness. For all devices, the distance between contacts is small (~150 nm) and the carrier density in the InSb nanowire can be tuned thanks to the global backgate. The small electrode separation allows to electrostatically define a tunnel barrier in the wire section between the electrodes by applying negative gate voltages.

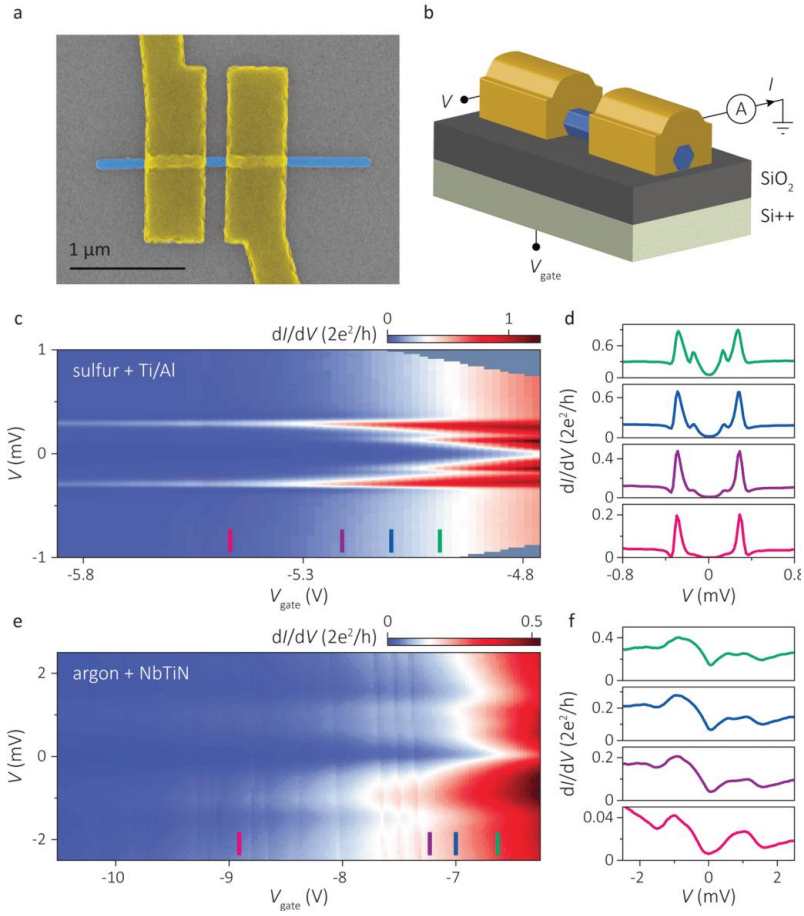


Figure 35: *InSb nanowire hybrid device and induced superconducting gaps for different device realizations.* ***(a)*** *Top-view false-color electron micrograph of a typical device consisting of an InSb nanowire (blue) with a diameter ~80 nm coupled to two superconducting electrodes (yellow) with ~150 nm separation.* ***(b)*** *Schematic of the devices and the measurement setup with bias voltage V, monitored current I, and the voltage V_{gate} applied on back gate (Si++ substrate) that is separated from the device by a 285 nm thick SiO_2 dielectric.* ***(c,d)*** *Spectroscopy of a device realized using sulfur cleaning followed by evaporation of superconducting Ti/Al (5/130 nm) electrodes. T = 250 mK. The differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate}. dI/dV traces in panel* ***d*** *are vertical line cuts from panel* ***c*** *at gate voltages marked with colored bars. dI/dV is symmetric around zero bias with two conductance peaks at V ~ ± 0.3 mV seen for all gate voltages that result from the coherence peaks in the superconducting density of states at the edge of the induced gap Δ. For our device geometry with two superconducting electrodes 2Δ ~ 0.3 meV. For sufficiently low V_{gate}, where dI/dV ≪ $2e^2/h$ at above-gap bias (V > 2Δ), tunneling is weak, which suppresses the Andreev reflection probability revealing a hard-induced gap. Larger gate voltages decrease the tunnel barrier height where increased Andreev reflection probability results in finite subgap conductance.* ***(e, f)*** *Spectroscopy of a device realized using argon cleaning followed by sputtering of superconducting NbTiN (90 nm) electrodes. T = 250 mK. We find 2Δ ~ 1 meV, much larger than that of the Al-based InSb hybrid device shown above. dI/dV traces in panel* ***f*** *show an above-gap conductance comparable to those in panel* ***d****. The induced gap is soft with a nonvanishing subgap conductance even for the weak tunnelling regime at low V_{gate}, indicating a deviation from Andreev transport.*

Here, we measure an induced hard-gap of 2Δ∼0.3 meV for the sulfur-Ti/Al device, whereas a soft-gap of 2Δ∼1 meV is measured in the argon-NbTiN case. Both device realizations present a challenge toward topological protection. In the first case, the magnetic field (∼0.5 T) required to drive the wire into the topological state destroys the superconductivity of Al. The subgap states present in the second device render the topological properties experimentally inaccessible. After several optimizations, a mix of both processes allowed to obtain a hard-induced gap and supercurrent in InSb nanowires in the presence of high magnetic fields (∼0.5 T) (figure 36).

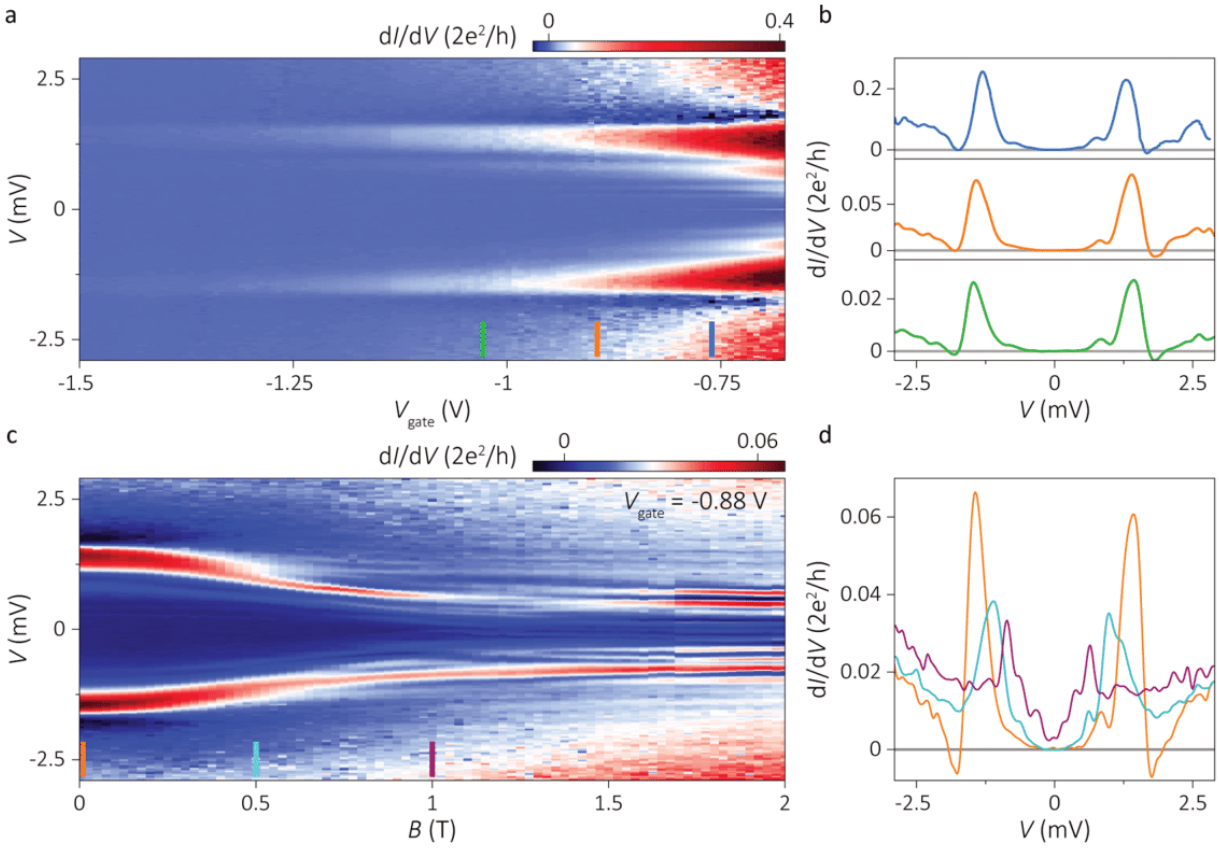


Figure 36: *Tunneling spectroscopy and magnetic field response of InSb nanowire hybrid devices with engineered interface.* ***(a, b)*** *Spectroscopy of a device realized with NbTi/NbTiN electrodes using sulfur cleaning followed by an in situ low-power argon cleaning. Differential conductance dI/dV is plotted as a function of bias voltage V for varying gate voltages V_{gate}. dI/dV traces in panel* ***b*** *are vertical line cuts from panel* ***a*** *at gate voltages marked with colored bars. dI/dV is symmetric in bias with two peaks at V ∼ ±1.5 mV seen for all gate voltages from which we find 2Δ ∼ 1.5 meV. The induced gap is hard with vanishing subgap conductance in the tunneling regime.* ***(c, d)*** *dI/dV of the same device is plotted as a function of bias voltage V for an increasing magnetic field B along the nanowire. Gate voltage is set to V_{gate} = −0.88 V, the same as in the middle panel in panel* ***b****. dI/dV traces in panel* ***d*** *are vertical line cuts from panel* ***c*** *at magnetic fields marked with colored bars. The induced gap remains hard up to ∼0.5 T. Increasing fields decrease the induced gap size and increase the subgap conductance, but induced superconductivity persists up to 2 T where dI/dV shows a gap feature with suppressed conductance at small bias and symmetrically positioned coherence peaks.*

All these material and device developments resulted in 2012 in the realization of full Majorana devices, and their optimizations in the following years (**figure 25**). If it remains unclear nowadays if the conduction peak appearing at zero energy in reference 6 corresponds to Majorana zero modes[6] or Andreev modes[80,82], this simple 1D geometry is anyway not sufficient for realization of topological Qubits. Indeed, the main idea using Majorana zero mode (MZM) is to braid information in order to use their non-Abelian statistics. Since MZM are real solution of the Dirac equation, they are their own antiparticles and thus annihilate when brought together. Using a 1D geometry, it is thus impossible to invert their position without killing them. Two theoretical alternatives were proposed in 2011 based on T- or X- shaped nanostructures to perform quantum computing by Alicea's[83] and Beenakker's[84] groups, both requiring development of high mobility multi-branched nanostructures as reported in **figure 37**.

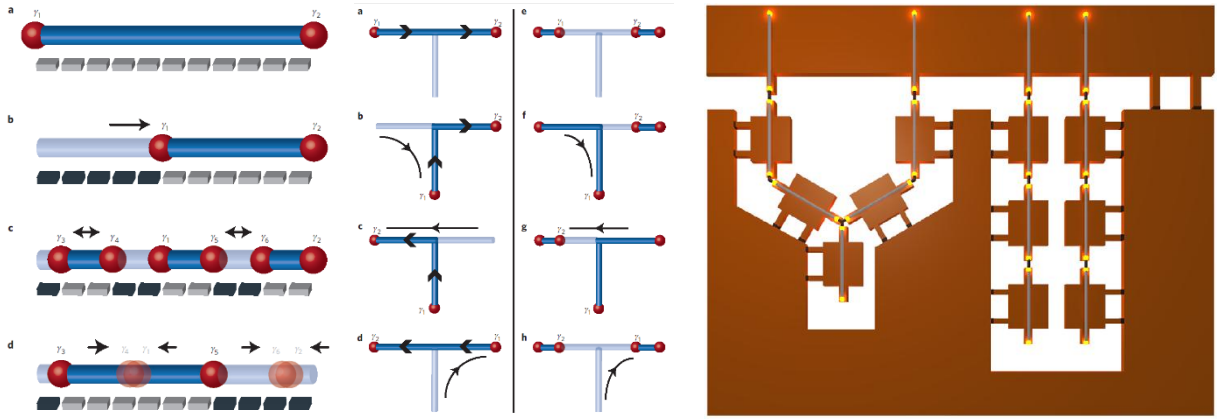


Figure 37: *Two theoretical alternative schemes for Majorana braiding. On the left, the proposal by Alicea et all. makes use of simple gate voltages, however, applied to a complicated ('keyboard') pattern of gates. On the right, the proposal by Beenakker et all. makes use of superconducting-loops and employs magnetic fluxes to realize braiding operations.*

2.7 Realization of branched InSb nanostructures[85]

Based on these two proposals, our goal was to develop new branched InSb nanostructures having the same transport properties than those of the wires. Considering the final devices, the branched wires must form a planar structure to enable electronic device fabrication by standard lithography techniques and should be of high crystalline quality in order to have nearly ballistic transport. Despite continuous progress in the control and understanding of nanowire growth, there are only a few studies that focus on three-dimensional branched nanowire networks[86–89]. Here, we proposed a new approach to grow InSb T- and X-shaped nanostructures using the VLS growth mechanism. The procedure includes four steps, which are presented schematically in the insets in **figure 38**, accompanied by corresponding dft electron microscopy (SEM) images. The first step corresponds to the fabrication of uniform InP–InAs stems (**figure 38a**). In step 2, the structure is thermally annealed at 470°C in the reactor chamber without any precursor, resulting in partial evaporation of the InAs nanowire and indium enrichment in the Au–In droplet. Because the particle volume increases and the InAs nanowire diameter decreases, the droplet falls to one of the three {112} InAs side. It is then

possible to start the growth of InSb nanowires in a horizontal direction, parallel to the substrate (figure 38c), using the optimal growth conditions developed previously for high-mobility wires. If an optimal diameter and density of gold colloids are used, InSb nanowires growing from different stems can meet and merge into nanostructures with T or X shapes (figure 38d).

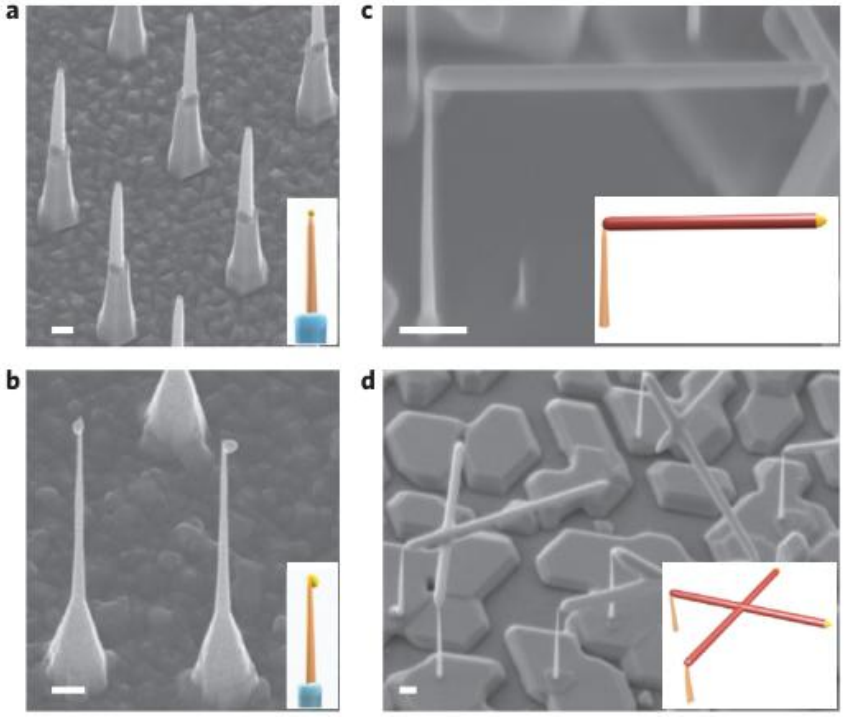


Figure 38: The four-step process for synthesizing branched InSb nanowires. ***a,*** *A 30° tilted SEM image of the InP/InAs stems.* ***b,*** *Au–In droplets on side facets after the annealing step.* ***c,*** *InSb nanowire grown parallel to the substrate surface.* ***d,*** *InSb nanocrosses resulting from the merging process between two InSb nanowires. All scale bars, 200 nm. Insets: InP, InAs and InSb segments are in blue, orange and red, respectively, and the Au–In droplet is in yellow*

Contrary to natural intuition, the merging process is not random and has been studied in detail. To describe the nanowire intersection, three angles are defined (figure 39b,c). ψ corresponds to the angle between the vertical stem and the growth direction of the InSb nanowire, φ is the in-plane angle of the InSb nanowire, and γ is the rotation angle of the InSb nanowire around its long axis. SEM side-view inspection of the samples shows that ψ is close to 90°, implying that the tapering of the InAs nanowires is minimal. To investigate the exact crystalline orientation of the InSb wires, X-ray diffraction (XRD) measurements were performed in a symmetric 2ϑ-ω configuration. Figure 39a shows a diffraction spectrum of the sample, where the (111) peaks of InP, InAs and InSb originate from the stems and a thin layer on the substrate. Importantly, a fourth peak also appears around the InSb(220) Bragg angle, which corresponds to InSb nanowires having one of their {110} side facets parallel to the substrate surface. The fact that no other sets of InSb lattice planes perpendicular to the <111> growth direction show up in the XRD pattern proves that φ and γ are fixed to 90° and 0°, respectively. Because stems and substrate have no horizontal <111> crystalline directions, this demonstrates that the InSb nanowires have no epitaxial relation with the InP–InAs stems, and the stems only serve as a mechanical support.

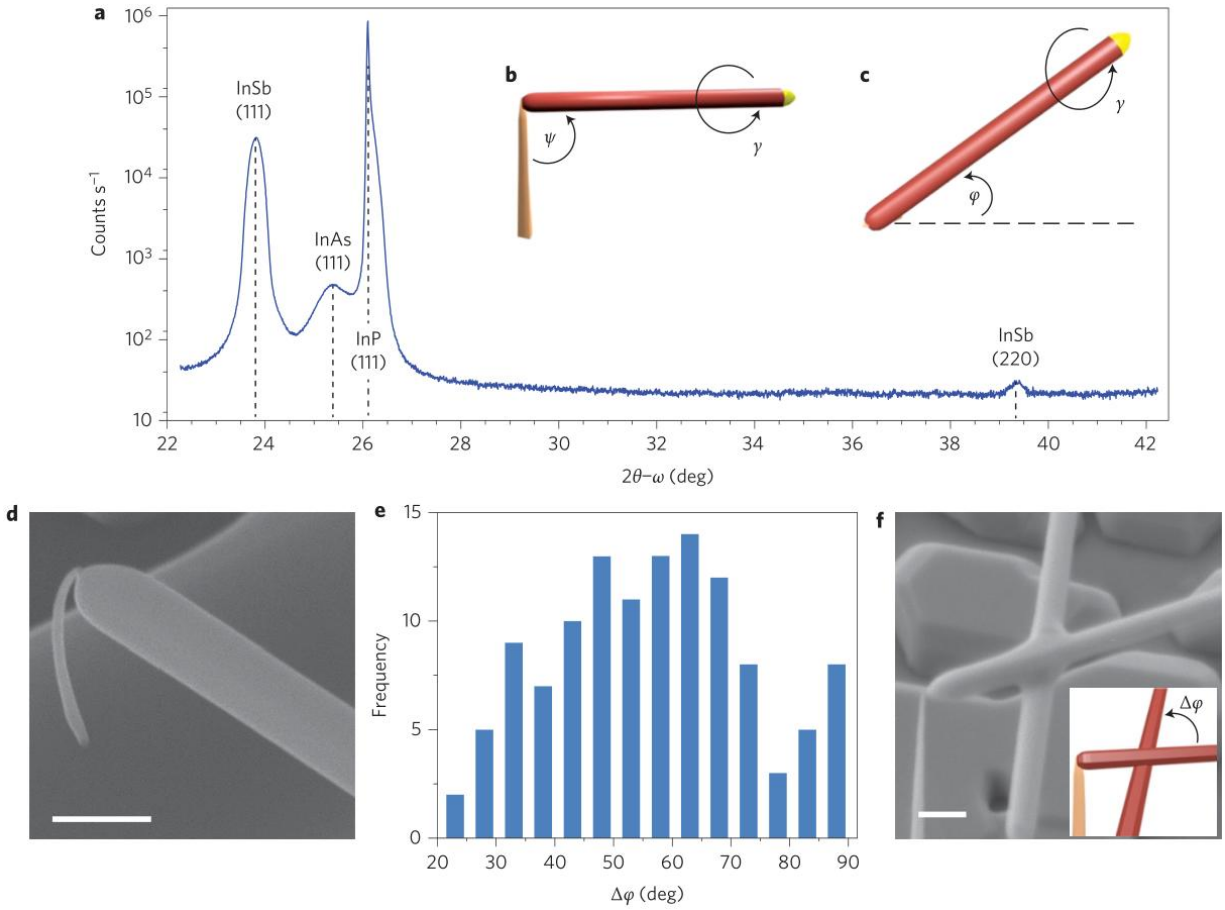


Figure 39: *Merging process for two InSb nanowires.* ***a,*** *Symmetrical (2ϑ-ω) XRD measurement on an as-grown sample.* ***b,c,*** *Side view* ***(b)*** *and top view* ***(c)*** *schemes of the InSb nanowires grown horizontally. The three angles defining the InSb growth direction are* ***ψ, φ*** *and* ***γ****.* ***ψ*** *corresponds to the angle between the vertical stem and the growth direction of the InSb nanowire,* ***φ*** *is the in-plane angle of the InSb nanowire with respect to the <1-10> direction of the InP(111)B substrate, and* ***γ*** *is the rotation angle of the InSb nanowire around its long axis, taking the alignment of the (220) InSb planes with the substrate surface as a reference.* ***d,*** *High-resolution SEM image of an InP/InAs stem bent during the merging process.* ***e,*** *Statistics about the* ***Δφ*** *angle between two crossing InSb nanowires.* ***f,*** *Example of a branched structure: the two InSb nanowires should have a slight difference in altitude in order to merge into a nanocross. All scale bars, 200 nm.*

In order to investigate ***φ***, we measured the angle ***Δφ*** between two legs for T- and X-shaped nanostructures (figure 39e,f) and found a maximum around ***Δφ*** = *60*°. This maximum can be explained by the triangular cross-sectional shape of the InAs segment. Indeed, the fall of the droplets on the lateral facets during the annealing step forces the InSb growth in six preferential ***φ*** directions, hence a maximum for ***Δφ*** around 60°. Owing to stem evaporation, it is also possible to change the InAs cross-section from a triangle to and hexagon. In this particular case a droplet can cover more than one facet because of its large volume leading to smaller maxima every ***Δφ*** = 30°. Finally, during the fourth step, wires can merge and form a planar, branched nanostructure having either a T- or X-shape. Soldering two wires is possible thanks to the lateral VS growth occurring at the same time as that VLS one. Note here that the distance between two InSb wires can be reduced due to the flexibility of the InAs stems, as shown in figure 39d.

If the crystal structure of InSb nanowires is pure ZB, the fusion of two wires should create a grain boundary that could influence the transport properties. The junction region was thus probed by HR-TEM, as reported in **figure 40**. When the crossing angle between two InSb nanowires is $\Delta\varphi$ = 70.5° (**figure 40a**), which corresponds to the angle between two [111] directions in a ZB crystal, single-crystalline nanostructures can sometimes be obtained, as demonstrated by the perfect match of the FFT patterns in **figure 40d-i.** In the most probable case ($\Delta\varphi$ = 60°), we observe a Moiré fringe pattern, characteristic of the superposition of two randomly oriented crystals.

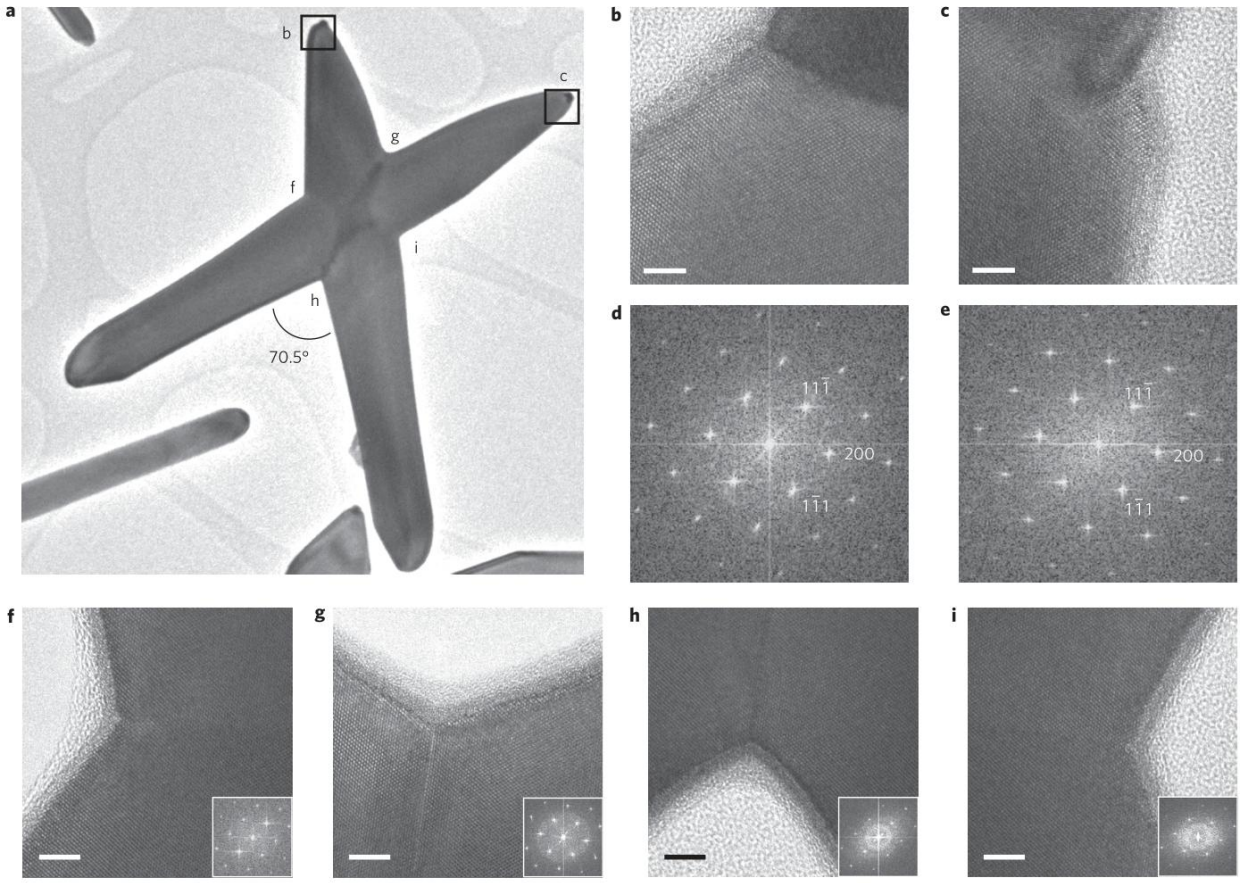


Figure 40: *Crystal structure of a single-crystalline nanocross.* **a,** *Low-resolution TEM image of a single-crystalline InSb nanocross.* **b,c,** *HR-TEM images just below the droplet for both branches.* **d,e,** *FFT patterns corresponding to* **b** *and* **c**, *respectively. The crystalline directions are perfectly superposed, proving the nanocross in a is a single crystal.* **f–i**, *HR-TEM images of each corner of the nanocross and the corresponding FFT pattern showing a single-crystalline orientation. Scale bars, 5 nm.*

If this growth method leads to the synthesis of InSb nanostructures filling the requirements for Majoranas braiding, the percentage of single-crystalline nanocrosses remains low (~8%). In this context, the rational bottom-up assembly of nanowire networks may be a way to overcome this issue, as reported in the following.

2.8 Toward rational nanowire networks[90,91]

Another method to grow crossed nanostructures is to move on (001) oriented substrates. Since InSb nanowires grow in a (111)B direction, a careful surface patterning and new kinked stems allow to perfectly control the merging process, as described below. Arrays of gold islands are patterned on (001) InP substrate, and InP nanowires are used as stems. The InAs segment is not needed anymore due to InSb nucleation optimizations, which further limit doping in the InSb nanostructures. First, a vertical <001> InP segment is grown (**figure 41a**)[91], before changing its growth direction into <111>B (**figure 41b**) by changing the contact angle of the catalyst droplet[92]. These kinked InP nanowires are then used as stems for the growth of InSb nanowires (**figure 41c**). On such (001) substrates, only two <111>B are present, which limits the geometrical options: 50% of the InSb wires will grow in the [11–1]B direction and the remaining 50% in [–1–1–1]B. Since the InSb wires are epitaxially connected to the substrate they will meet under an angle of 109.5° (**figure 41e**), which is precisely the angle between two <111>B directions in a ZB monocrystal (109.5° = 180°-70.5°). This alternative approach is expected to result in a high yield of single-crystalline junctions.

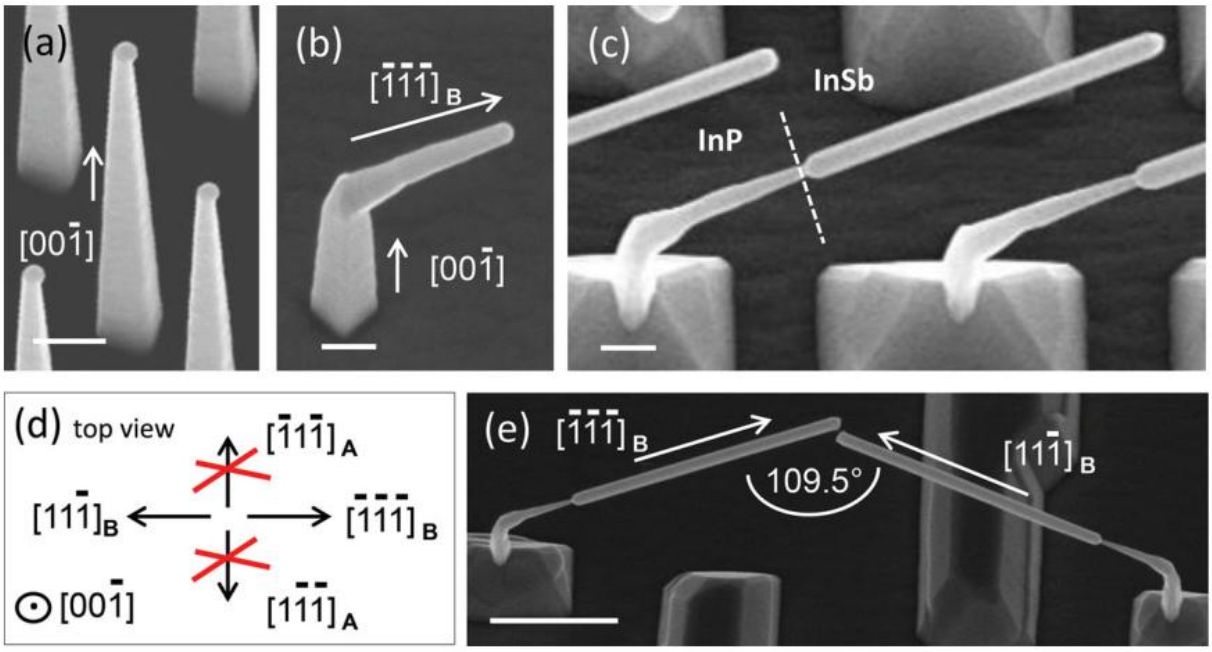


Figure 41: *InSb nanowires grown on an (001) InP substrate.* ***a)*** *<001> InP nanowires grown on an (001) InP substrate.* ***b)*** *A kinked <111>B InP segment on top of the vertical <001> InP nanowire.* ***c)*** *High aspect ratio <111>B InSb nanowires grown on kinked InP stems in* ***(b)****.* ***d)*** *A scheme indicating four [111] directions pointing upwards from (001) substrate. InSb nanowires only grow in <111>B directions.* ***e)*** *Two InSb nanowires growing at an angle of 109.5° with respect to each other. For images* ***(a)****,* ***(b)****, and* ***(c)*** *the scale bar is 200 nm. For image* ***(e)*** *the scale bar is 1 µm. For all SEM images the viewing angle is 30°.*

In the first configuration, the gold droplets are exactly aligned along the substrate [–1–10] crystalline direction (figure 42a). When two InSb nanowires growing towards each other meet, the gold droplets coalesce into a bigger one and a nanowire "bridge" is formed (figure 42b,c)[89]. Although this is an interesting approach to double the length of the InSb wires while maintaining the relatively small diameter, we are interested in multi-branched structures. In the second configuration, a misalignment is designed in the y-direction (figure 42d), allowing InSb nanowires growing towards each other to cross and merge into multi-branched nanostructures (figure 42e,f).

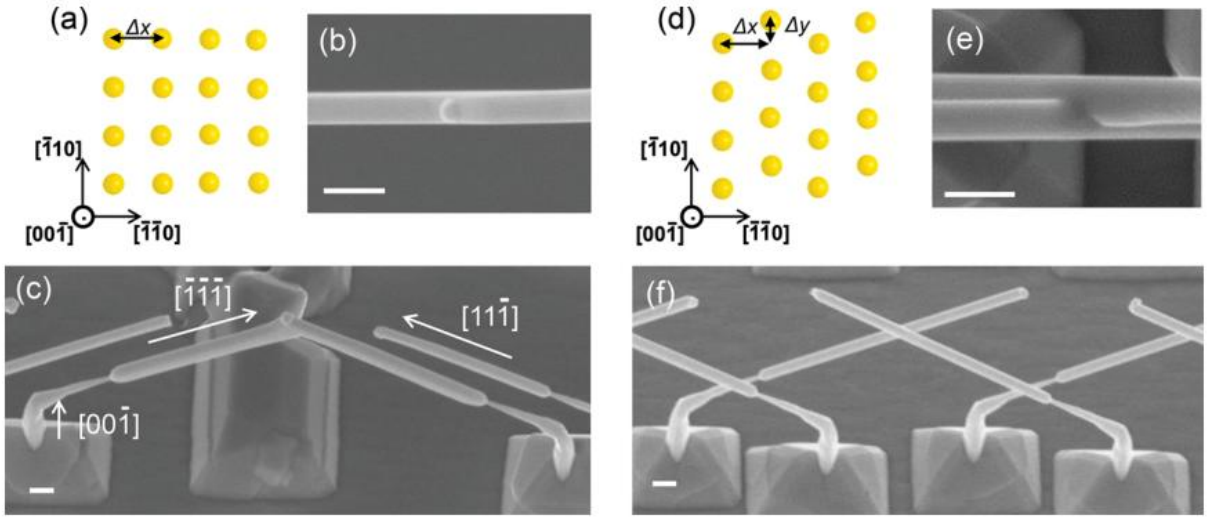


Figure 42: Position- and direction-controlled growth of InSb nanowire networks. ***a)*** *Scheme of a gold droplet array defined by electron beam lithography.* ***Δx*** *denotes the pitch between the two neighboring droplets.* ***b)*** *Top-view SEM image of two merged nanowires. A single gold droplet on top of the nanowire bridge structure can be easily seen.* ***c)*** *30° tilted SEM image of the complete bridge structure (kinked InP stems + merged InSb nanowires) with growth directions indicated by arrows.* ***d)*** *Introducing the misaligned electron beam lithography array of gold catalysts to favor crossed nanowire structures.* ***Δx*** *denotes the pitch and* ***Δy*** *the offset between the two neighboring droplets.* ***e)*** *Top-view SEM image showing an InSb crossed junction.* ***f)*** *30° tilted SEM image of the crossed structure. All scale bars correspond to 200 nm.*

Similarly to section 2.7, the crystalline structure of the junctions was investigated by TEM and once again, single-crystalline nanocrosses are reported (figure 43). This result confirmed the relevance of our approach, however alternative structures have also been observed. Indeed, Moiré interference pattern are present at some junctions, which is a signature of two differently oriented crystals. The corresponding FFT pattern reveals that a twin-related 36.5° angle is present between the <200> crystalline directions of the merging InSb nanowires. A grain boundary is thus formed at the junction, which however does not imply the formation of polarity inversion domains[93]. This means that polarity is always preserved and then the merging process provides clean interfaces with no charging effects. The formation of the grain boundary can be explained by rotational defects in the <111>B InP segment: after an odd number of twins the top of the InP stem and the (001) InP substrate are twin-related, whereas the crystalline orientation remains identical for even numbers of twins. Thus, if an even number of rotational

twins is present in both the [11–1]B and [–1–1–1]B InP stem, the resulting crystalline orientations at the end of the two InP segments are identical. The same applies for InSb nanowires growing on top of them, and the resulting crossed junction is in that case single-crystalline. It is important to notice that the orientation of a [11–1]B InP segment after an odd number of twins is not the same as the orientation of the [–1–1–1]B InP segment after an odd number of twins, since the rotations occur around different axes. In this case, a grain boundary is formed at the junction between the two InSb nanowires. The FFT pattern of such a twinned-twin junction will show a 36.5° angle between the two <200> directions. Finally, an InSb nanocross can be formed from two InSb nanowires, one growing from an InP stem with an even number of twins, and one from an InP stem with an odd number of twins. The FFT diffraction pattern of such a twinned junction will show a 109.5° angle between the two <200> directions. Considering all possible crystalline orientations of InP nanowires, and the fact that there is a 50% chance for an even and odd number of twin boundaries in the InP segment, we are left with four possible options: even-even, odd-odd, and even-odd/odd-even; each of which having a 25% probability.

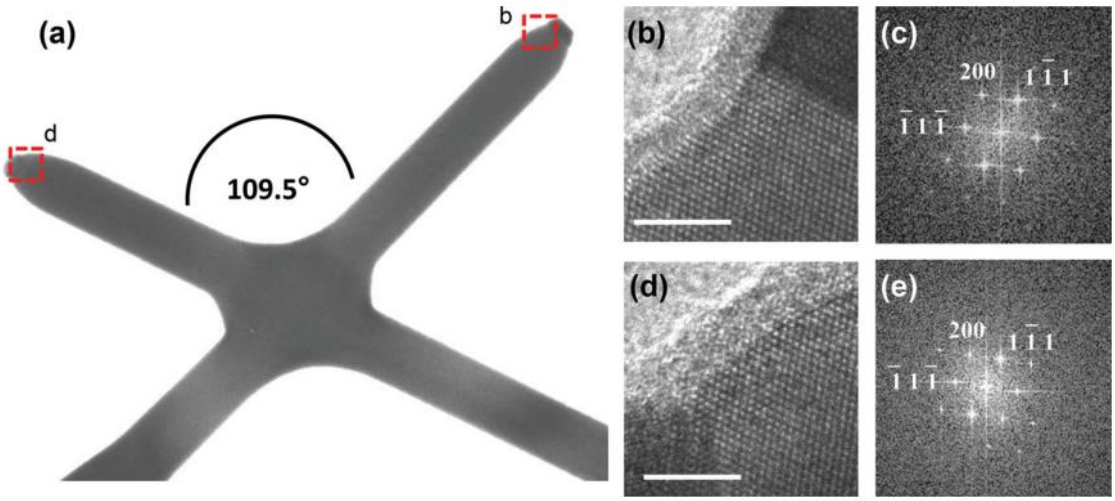


Figure 43: *TEM study of a single-crystalline junction.* ***(a)*** *Bright field TEM image of a single-crystalline junction.* ***(b,d)*** *HR-TEM images taken just below the droplets of each leg. Scale bars correspond to 5 nm.* ***(c,e)*** *The corresponding FFT patterns. The crystalline directions in* ***(c)*** *and* ***(e)*** *are perfectly superposed, which proves the single-crystallinity of the junction.*

With this method the yield of single crystalline junctions has increased significantly compared to the previous approach (from 8% to 25%)[85]. Reaching 100% require the development of defect-free zinc-blende <111>B InP wires, which has not been reported yet in literature. An alternative route is to directly grow InSb nanowires on the vertical <001> InP stems, but nucleation remains challenging in that case. Importantly, alternative geometries are possible by changing the catalyst spacing and offset. A new zoology of nanostructure is therefore accessible, which includes π-structures (**figure 44a,b**), nano-loops (**figure 44d, e**), and nanowire networks (**figure 44c,f**). An example of a single-crystalline π-junction was measured in reference [90], showing that this approach can be scaled up and is suitable for fabricating key components of future Majorana random access memories.

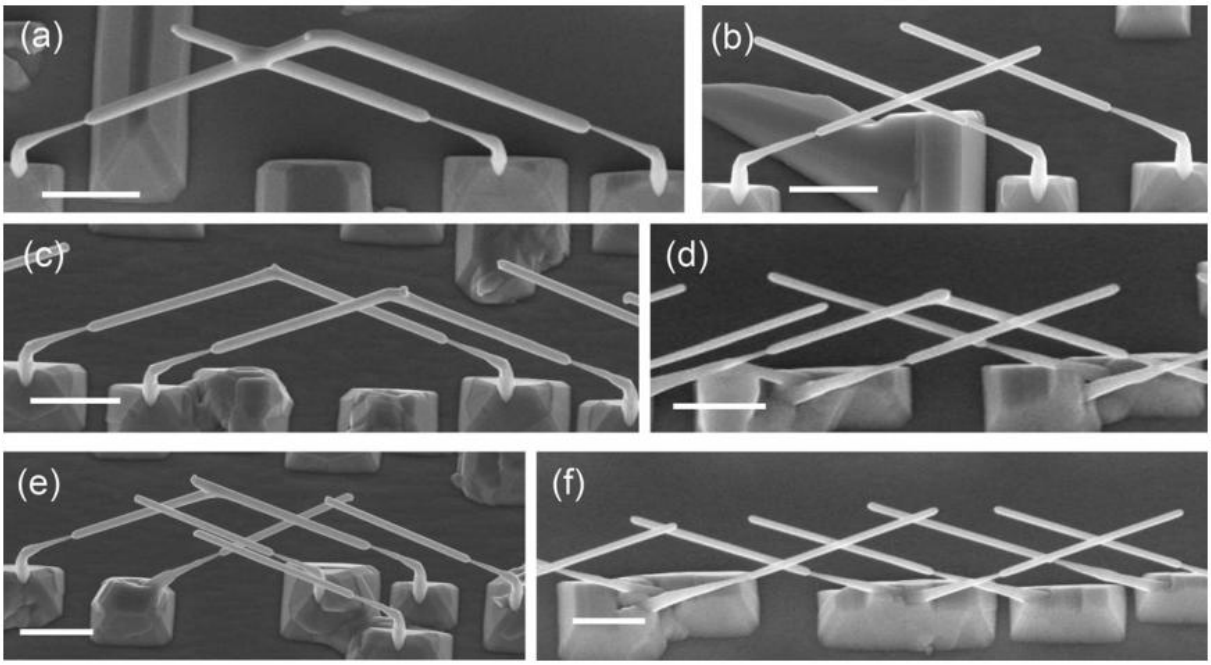


Figure 44: *Nanowire networks.* ***a)*** *30° tilted SEM image of the nanowire π-structure. Two nanowires growing from mutually aligned droplets merge into a bridge. A third nanowire growing from a misaligned droplet forms a crossed junction with one leg of the bridge.* ***b)*** *30° tilted SEM image of the nanowire π-structure consisting of three nanowires and two crossed junctions.* ***c)*** *30° tilted SEM image of a 4-nanowire architecture: two nanowire bridges connected by one crossed junction.* ***d)*** *30° tilted SEM image of the nanowire loop formed out of four interconnected InSb nanowires, two of which are growing in the [11–1]B and the other two in the [-1–1–1]B direction.* ***e)*** *30° tilted SEM image of the 6-nanowire network: 4 nanowires connected in a closed loop whose one leg is forming a π-structure with the other 2 nanowires.* ***f)*** *30° tilted SEM image of a 7-nanowire network. All scale bars 1 µm.*

2.9 Electrical measurements of the InSb nanostructures[85]

Contrary to standard nanowires, multibranched nanostructures allow both, the extraction of a FET mobility following the procedure presented in **section 2.5.2** and the direct measurement of a Hall mobility. Several nanocrosses, synthetized from both growth methods, have been contacted. Linear I–V sweeps are reported for all contact combinations (**figure 45b,c**), which indicates ohmic contacts and the absence of localization in the junctions. Since the crossing angle between InSb nanowires is not always optimal, these measurements confirm the high electrical transparency of the non-polar grain boundaries. The electron density n, extracted from these Hall measurements, increases linearly with gate voltage, from ~ 5×10^{16} cm^{-3} to ~ 2×10^{17} cm^{-3}. Gate–nanocross capacitances of 50 aF are derived from a linear fit of $n(V_g)$. We then extract the field-effect mobility from a fit to the gate traces and find values ranging from 6 500 to 10 000 $cm^2V^{-1}s^{-1}$. These high mobilities indicate that the transport properties of InSb nanowires are preserved in complex wire structures, even in the presence of a grain boundary at the junction. Moreover, gate traces of nanocrosses and T junctions with various crossing angles $\Delta\varphi$ between 40° and 70° are comparable. Accordingly, we infer that the electron mobility is probably limited by scattering at the surface or at impurities. Single-

crystallinity is thus not a limiting factor for the transport properties of the complex structures presented in figure 44.

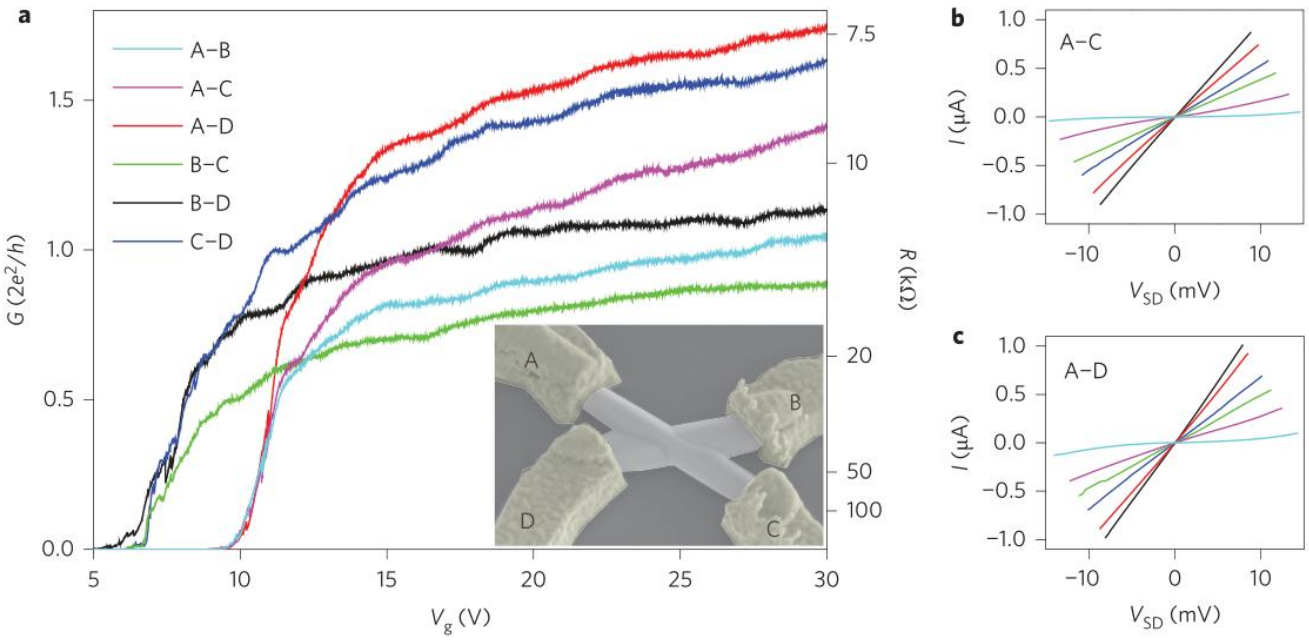


Figure 45: *Transport through a nanocross. All data were taken at a temperature of 4.2 K.* ***(a)*** *Conductance $G=I/V_{SD}$ of all six contact pairs as a function of gate voltage V_g. V_{SD} is the voltage bias across the device; I is current. For all traces, V_{SD} is between 10 mV (near pinch-off) and 5 mV (at V_g = 30 V). Right axis: resistance R = 1/G. Inset: SEM image (50° tilted) of the measured nanocross.* ***Δφ****, the angle between nanocross legs, is 45°.* ***(b,c)*** *Bias voltage sweeps of contact pairs A–C* ***(b)*** *and A–D* ***(c)*** *at several gate voltages V_g. For* ***(b)****, from light blue to black, V_g = 9.8, 10.5, 11.1, 12, 15 and 22.5 V. For* ***(c)****, from light blue to black, V_g = 9.8, 10.2, 10.7, 11.7, 15 and 22.5 V.*

Finally, superconductivity was induced in these nanostructures by depositing superconducting leads instead of normal metals at each end of a nanocross (figure 46a). The contact pairs of the device have a normal state conductance at large positive gate voltage between $1.1G_0$ and $3.5G_0$ ($G_0 = 2e^2/h$). The *V(I)* characteristic of all measured contact pairs exhibits a supercurrent branch, indicating proximity-induced superconductivity[72,94]. Switching to a resistive state occurs when the current bias exceeds the critical current I_c (figure 46b). I_c is gate-tunable (figure 46c) and increases with the nanocross normal state conductance. By comparing different contact pairs, we find that I_c depends on the contact separation and varies between ~ 4.6 nA (section A–C, separation of 620 nm) and ~ 0.25 nA (C–D, separation of 1.5 mm). The critical currents within a single nanowire (section A–C) and through the nanocross junction (B–C) are comparable. Moreover, the supercurrents through these nanocross sections are similar to that through an InSb nanowire Josephson junction contacted with the same superconductor and with similar contact separation. These results substantiate the expectation that crossed nanowires will enable advances in topological superconducting systems such as the development of the proposed Majorana fermion braiding devices.

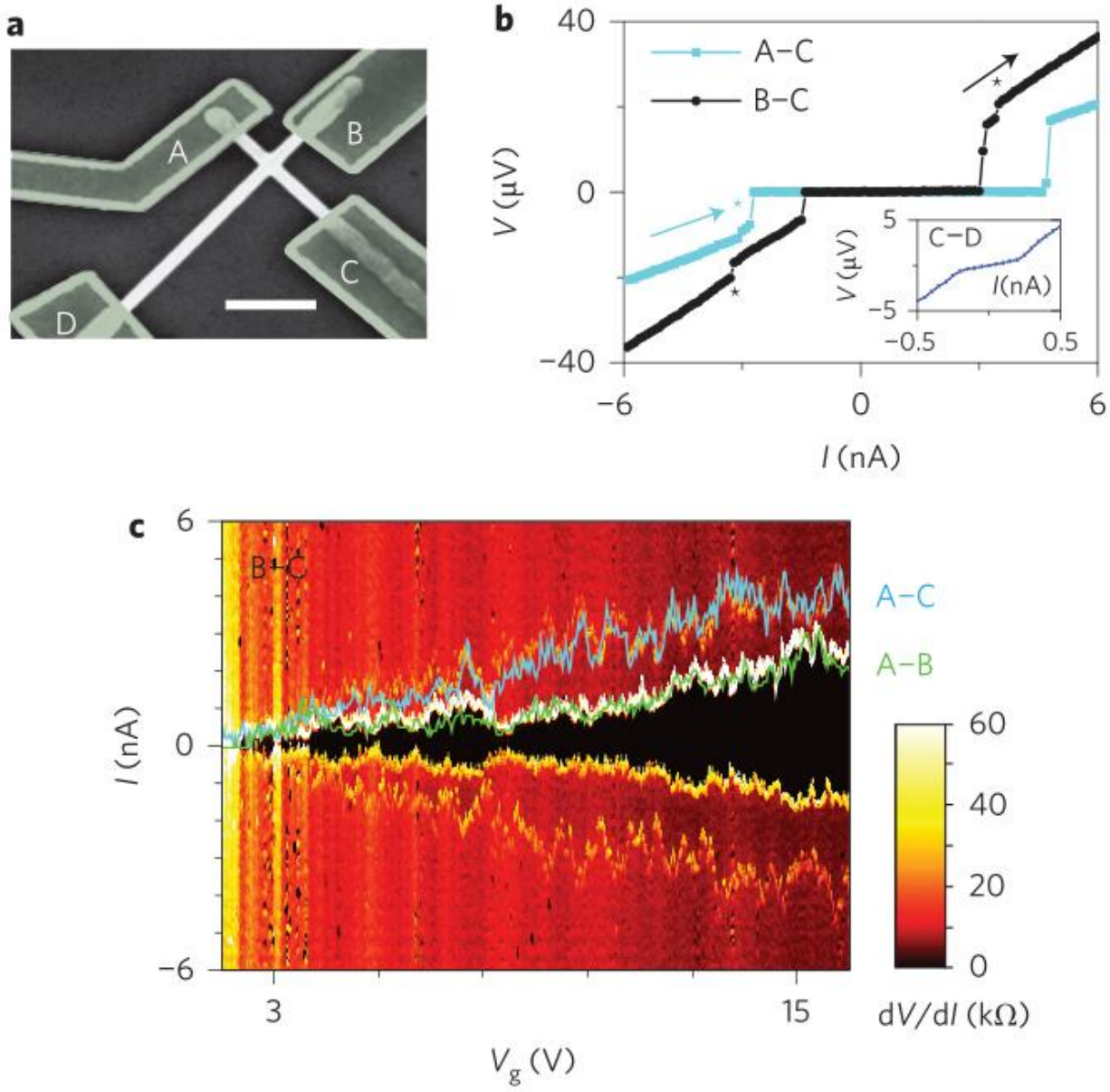


Figure 46: *Gate-tunable supercurrent through a nanocross. Data taken at 20 mK. Instrumental resistance has been subtracted.* ***(a)*** *Top-view SEM image of the device. To decrease the wire diameter, the nanocross was etched by HCl in the growth chamber directly after growth. Scale bar, 0.5μm. Contact spacings are 440 nm (section A–B), 620 nm (A–C and B–C), 1,300 nm (A–D and B–D) and 1,480 nm (C–D). Contact material is NbTiN/Al (50/70 nm).* ***(b)*** *V(I) characteristics for current bias I between contacts A–C (global backgate voltage V_g = 14.8 V, blue) and B–C (V_g = 14.4 V, black). The asymmetry in the V(I) trace, indicating hysteresis, is due to environmental shunting or self-heating of the device. The kinks in the dissipative branches (indicated with asterisks) are probably Fiske steps. Both features are commonly observed in underdamped Josephson junctions.* ***Inset:*** *V(I) characteristic for section C–D (V_g = 13.5 V).* ***(c)*** *Colour plot: differential resistance, dV/dI as a function of I and V_g for section B–C. The black region (dV/dI = 0) indicates supercurrent through the nanocross. Superimposed with the same horizontal and vertical scale is the critical current for B–C (white), A–B (green) and A–C (blue).*

2.10 Conclusions of Chapter 2

This second research activity resulted in numerous breakthroughs. The optimization of the InSb nanowire growth led to a deep understanding of the growth mechanisms and demonstrated the crucial role of the droplet composition. High aspect ratio nanowires are obtained having a diameter below 100 nm and a length around 3.5 µm. These results are still the states-of-the-art for InSb nanowires having diameters under 100 nm, and were only exceeded recently by stemless InSb nanowires[55]. First multibranched InSb nanostructures were synthetized by developing two original growth methods: from random to rationally designed networks. Transport properties in these nanostructures demonstrated their high quality, leading to electron mobilities up to 35 000 $cm^2V^{-1}s^{-1}$ [85]. Quasi ballistic transport is reported for both InSb nanowires[67] and nano-networks[95] and proximitized superconductivity can be induced in both structures[78,85]. If the presence of Majorana zero modes in these hybrid interfaces is still unclear[6,80,82,96], these studies paved the way to possible topological qubits.

Now that essential ingredients are developed and that physics is best understood, several improvements are possible. First, the induced superconductivity can benefit from the epitaxial growth[97] of a higher Tc superconductor such as Pb[98] or Sn[99]. Next, the semiconductor material can be shifted to either another one without nuclear spin such as PbTe[100], or a topological insulator[101] in order to improve the topological qubit coherence time. Finally, the device geometry should change from VLS nanowires to 2D structures for scaling-up problematics[102].

Chapter 3:
Topological materials for quantum computing and spintronics applications

3.1 Context and topological insulators

As presented in **chapter 2**, InSb nanostructures are good candidates for implementing topological qubits in solid states devices, but the presence of nuclear spins and the difficulty to induce a hard superconductive gap in thick (60-100nm) nanostructures[78] slow down the development of topological devices. Moreover, the necessity to manipulate individual nanowires limit the scaling up of such architectures. An alternative approach was recently developed by Microsoft using a 2D geometry[102] and the InAs-Al interface. The advantage of such devices is the ease to scale up, but the graded buffer used to adapt the lattice mismatch between the InP substrate and the InAs layer can also induce dislocations that reduce the electron mean free path[103]. An alternative option is to use Topological Insulators (TI) instead of low-bandgap semiconductors, since transport at the surface of such materials is “topologically” protected. Devices built from TI should thus present longer coherence times and be less sensitive to external perturbations[104].

Topological insulators are a new class of materials that birth root back in 1985 when Volkov and Pankratov noticed the presence of a 2D Dirac cone at the interface between PbTe and SnTe materials[105]. In order to explain their results, they proposed the existence of non-degenerate 2D metallic states at the interface between two semiconductors provided that one of them has an inverted band structure. Later in 1987, together with Pakhomov, they suggested that a HgTe layer sandwiched between two CdTe barriers has the same features as the PbTe/SnTe heterostructure[106], which was confirmed experimentally 20 years later[107,108]. Despite numerous theoretical studies, this new class of materials was considered “strange” by scientists until the pioneer publication of Kane and Mele in 2005[109]. In their article, they proposed to distinguish these materials from ordinary insulators by introducing a new topological invariant "Z2", which highlights the importance of time reversal symmetry (TRS) in the protection of metallic states. In addition, they underlined the crucial role of strong spin orbit interactions (SOI) on the material band structure: the electron spin cannot be neglected anymore. The combination of these two quantum characteristics leads to the creation of a topological phase called the quantum spin Hall one. Shortly after this theoretical proposal, Bernevig et al.[107] suggested a reasonable experiment for realizing a 2D TIs based on HgTe quantum wells. They supposed the existence of a critical HgTe thickness, where a transition from a normal insulator to a quantum spin Hall phase occurs. This was verified experimentally one year later by König et al. [108]. Subsequently, Fu and Kane[110] introduced the concept of "3D topological insulators" and differentiate them from the 2D quantum spin-Hall phase by the number of Z2 invariants. They defined a single Z2 for 2D-TIs, while four Z2 are required for 3D TIs. They also distinguished two types of TIs: trivial (weak TIs) and nontrivial (strong TIs) ones. Strong TIs are distinguished

from weak ones by an odd number of crossings between the Fermi level and the surface states. This prevents the metallic states from being gapped even in the presence of non-magnetic perturbations[111] and regardless of the position of the chemical potential[112]. In the case of 3D TIs, the four Z2 indexes are denoted "ν_0, ν_1, ν_2, ν_3". When ν_0 = 0 the TI behavior is considered as "weak", whereas it is “strong” when ν_0 = 1, which means a better protection of the topological surface states (TSS). Moreover, this study identified "strong" TIs including Bi compounds such as BiSb, Bi_2Se_3, Bi_2Te_3 and $Bi_{2-x}Sb_xTe_{3-y}Se_y$ alloys. The electronic structure of a topological insulator is presented in **figure 47**.

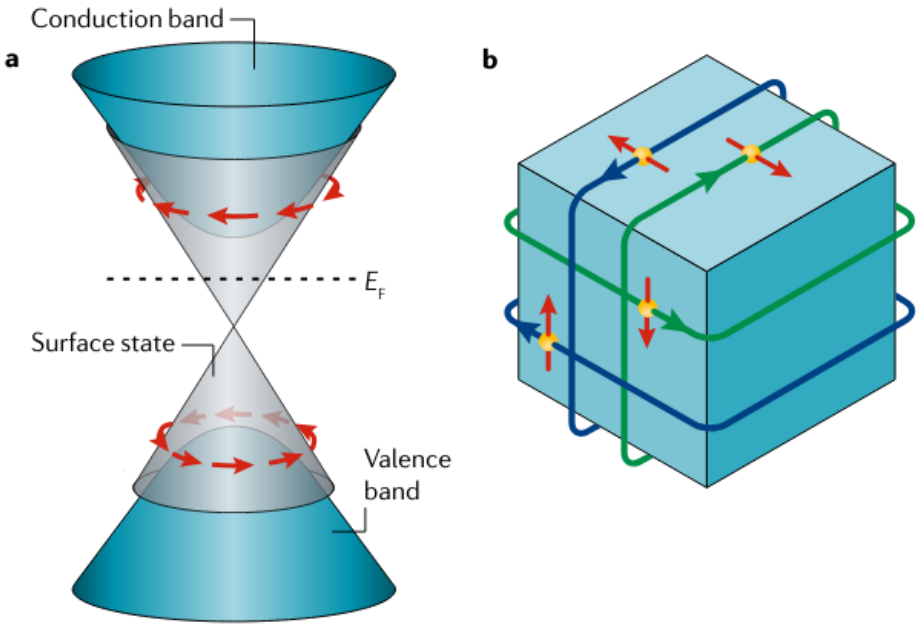


Figure 47: *(Extracted from **figure 1** of reference [113]): The electronic structure of a topological insulator. **(a)** The massless Dirac-like dispersion of the surface state with spin–momentum locking in a topological insulator. The surface state band connects the bulk valence and the bulk conduction bands. **(b)** Real-space picture of the surface state in a topological insulator. Electrons with spins pointing up and down (red arrows) move in opposite directions.*

Since the mid 2000’s, numerous TI have been reported in literature. Indeed, despite $Bi_{1-x}Sb_x$ being the first 3D TI confirmed experimentally, the alloy exhibits a random substitutional disorder and its surface states are expected to present multiple Dirac cones. Moreover, the $Bi_{1-x}Sb_x$ alloys can host impurities bands within the bulk bandgap, which could mimic the surface state signatures[114]. This motivated the search of new TIs with well-defined electronic structures and a single Dirac cone. Since bismuth is quite unique, many theoretical and experimental efforts have focused on V_2VI_3 Bi-chalcogenides materials such as Bi_2Te_3, Bi_2Se_3, $Bi_{2-x}Sb_xTe_3$ and $Bi_{2-x}Sb_xTe_{3-y}Se_y$. Despite these numerous candidates, none of them definitively prevailed due to several limitations.

The Bi_2Te_3 material is considered as a non-trivial 3D TI with extremely simple topological surface states and a large bulk bandgap. Its surface states present only one Dirac cone at the Γ point of the Brillouin zone, but theoretical and experiment studies demonstrated that it is buried inside the bulk valence band[114,115]. The transport is thus dominated by bulk carriers, leaving the Dirac cone away from the Fermi energy level E_F. The p-doping of the bulk allows to suppress its conduction, but induces disorder that influence the TSS. Bismuth Selenide (Bi_2Se_3) shares almost the same electronic and structural properties as Bi_2Te_3, and excess of Selenium during growth and vacancies induce a n-type bulk conductivity[116]. The excess of electron pins the Fermi level within the bulk band conduction. Unlike Bi_2Te_3, the electronic spectral weight distribution along the Γ-M and Γ-K directions shows that the single Dirac point is inside the bulk bandgap at 0.09 $Å^{-1}$ along Γ–M and at 0.10 $Å^{-1}$ along Γ-K[117]. The upper Dirac cone crosses the Fermi level within the bulk conduction band. P-doping of the bulk has the same advantages and drawbacks that for Bi_2Te_3.

The main issue with binary materials is the large bulk conduction that prevent the dominance of the surface states transport. Except from using an external doping, another option is to combine n-type (Bi_2Te_3, Bi_2Se_3) and p-type (Sb_2Te_3, Sb_2Se_3) TIs in order to create a semi-insulating alloy. For instance, the ternary compounds $(Bi_{1-x}Sb_x)_2Te_3$ has a lower bulk conductivity than binaries, which allows to measure the surface states. Across the whole Sb composition, this material presents a single Dirac cone which makes it a nontrivial TI[118] Its lowest bulk conductivity is reached for a Sb composition of 50%, which correspond to a sheet carrier density of 3×10^{12} cm^{-2}. Interestingly, the Sb composition controls the $Bi_{2-x}Sb_xTe_3$ electronic properties by changing the Fermi energy position and for a composition x of 0,88 the Dirac point and Fermi energy level are in the bulk bandgap, making this material an ideal TI[119].

The strategy we decided to follow first in LAAS, was to grow $Bi_{1-x}Sb_x$ TIs. The main reason for this choice was the possibility to add a bismuth cell in our MBE 412 system without polluting this III-V chamber with Se or Te group VI atoms, since this system produces other III-V structures for LAAS researchers such as Vertical-Cavity Surface-Emitting Lasers (VCSEL). Moreover, the absence of a high temperature oven did not allow for preparation of standard and clean Si(7x7) surface reconstructions. Possible choice for the substrates were then limited to InP, InSb, GaAs, and sapphire. If the InSb substrate has the lowest lattice mismatch with BiSb, its low bandgap is detrimental for building devices due to possible leakage currents. Ideal substrates should be semi-insulating. Ultimately our choice fell on GaAs substrate because of the possibility to grow a clean buffer layer before the TI integration.

3.2 The $Bi_{1-x}Sb_x$ structural and electrical properties

Bismuth (Bi) and Antimony (Sb) are both heavy elements of the V_A column of the periodic table that have a rhombohedral crystalline structure and a R-3m space group[120]. Their lattice structure can be seen as two inter-penetrating face centered cubic (FCC) sub-lattices elongated along the trigonal direction of the FCC diagonal. The $Bi_{1-x}Sb_x$ alloys inherit of the same crystalline structure and space group as both elements (**figure 48**). Note here that, contrary to III-V materials of other chalcogenides, both elements are perfectly interchangeable in the matrix since they belong to the same column of the periodic table. Vacancies are therefore less likely to appear during the crystal growth of the alloy. The C_3 symmetry of the trigonal axis makes it easier to use the hexagonal notation system compared to the Cartesian one.

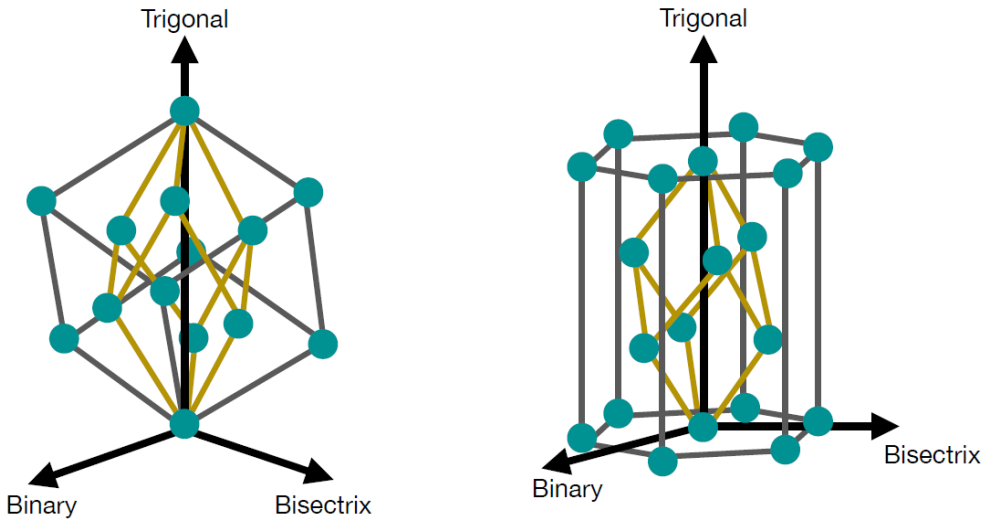


Figure 48: *Crystalline structure of the Bi, the Sb and the $Bi_{1-x}Sb_x$ alloys considering a cubic (left) and an hexagonal (right) coordinate system.*

The $Bi_{1-x}Sb_x$ phase diagram is characterized by a continuous solid solution phase between both elements, and growth at too low temperature can lead to compositional segregation (**figure 49**).

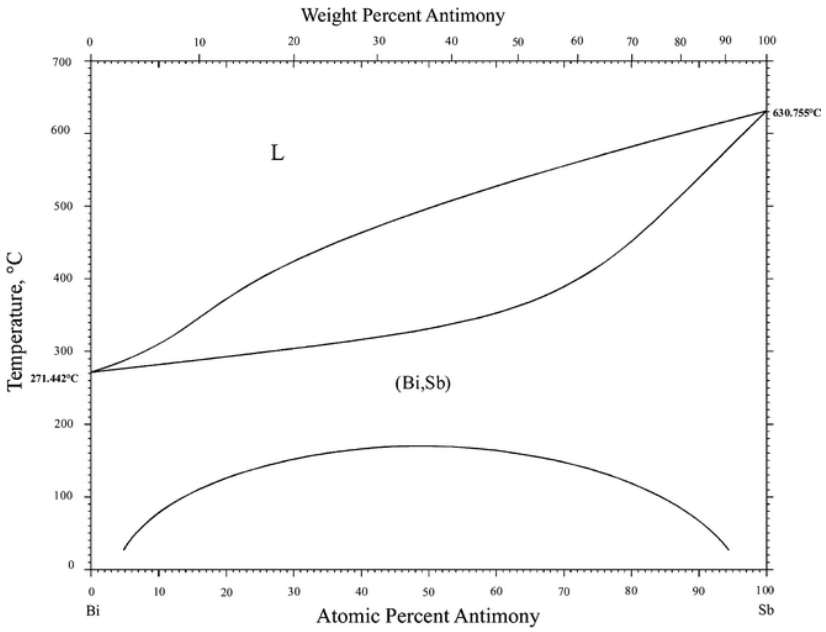


Figure 49: *$Bi_{1-x}Sb_x$ phase diagram from reference [121].*

The $Bi_{1-x}Sb_x$ lattice parameter is composition dependent, as shown in **figure 50**. Note that the **a** and **b** lattice parameters are almost obeying the Vegard's law, contrary to **c**.

$Bi_{1-x}Sb_x$		
x	c (Å)	a (Å)
100	11,2732	4,3085
95	11,3195	4,3198
90	11,3588	4,3313
85	11,3945	4,3427
80	11,4282	4,3542
75	11,4605	4,366
70	11,4906	4,3772
65	11,52	4,3887
60	11,548	4,4
55	11,576	4,412
50	11,6037	4,4242
45	11,631	4,436
40	11,6585	4,4483
35	11,6846	4,4605
30	11,7105	4,473
25	11,736	4,4855
20	11,7615	4,4978
15	11,7867	4,51
10	11,812	4,5225
5	11,8365	4,5347
0	11,8616	4,5465

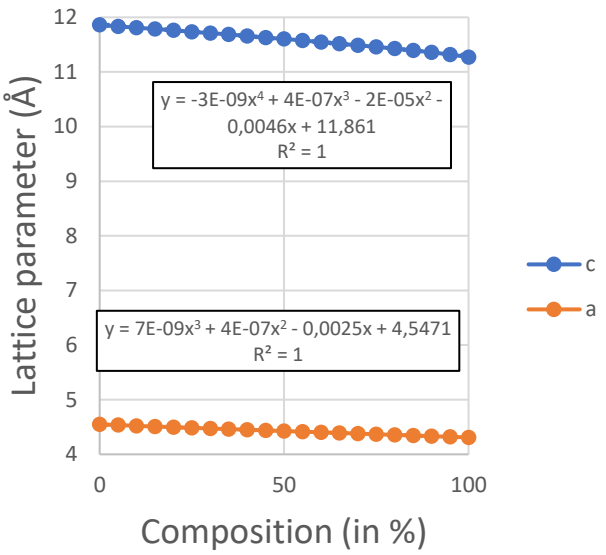


Figure 50: *$Bi_{1-x}Sb_x$ lattice parameters as a function of the composition.*

Since Bi and Sb have similar chemical properties, their electronic band structures are close. Both are semimetals with indirect negative bandgaps: -40meV for Bi between the T and L_s points and -177meV for Sb between the H and the L_a points. Moreover, both materials have different Z_2 topological invariant due to different SOI strength. Bi is topologically trivial ($Z_2 = 0$) with strong SOI, whereas Sb is topologically nontrivial ($Z_2 = 1$) and exhibits a SOI strength three times weaker. Thus, substituting Bi atoms by Sb ones, the SOI strength is reduced, which allows to tune the material properties[122] by switching the alloy from a trivial topological material into a non-trivial one.

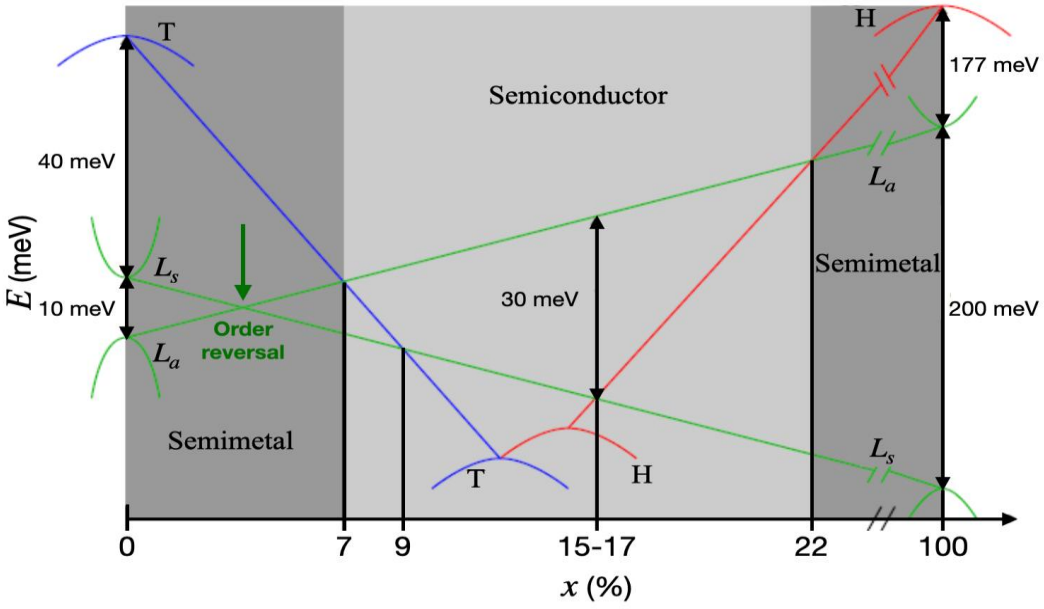


Figure 51: *$Bi_{1-x}Sb_x$ band structure as a function of the Sb composition*

For x < 0.07, the $Bi_{1-x}Sb_x$ behaves as a semimetal with a valence band (VB) at T above the conduction band (CB) at L. Importantly, for x = 0.04, the gap between the CB and the VB at the three equivalent L-points closes leading to the appearance of a massless, three-dimensional Dirac cone. By increasing x further, a gap opens with an inverted symmetry ordering, leading to a negative band gap at each of the three equivalents L-points in the Brillouin zone. For 0.07 < x < 0.09 and 0.17 < x < 0.22, the gap is indirect, whereas it is direct for 0.09 < x < 0.17. The theoretical maximum of the bandgap (~ 35 meV) is reached for x = 0.17. Finally, increasing x above 0.22, leads to a semimetal behavior.

In their pioneering article, Fu and Kane[110] predicted the $Bi_{1-x}Sb_x$ alloys to be a strong TI for 0.07 < x < 0.22, which was later measured experimentally by Hsieh et al.[123] using Angle Resolved Photo Emission Spectroscopy (ARPES) measurements on a $Bi_{0.9}Sb_{0.1}$(111) surface (**figure 52**). Here, an odd number of crossings is observed at the Fermi energy level, indicating the TI nature of the material. Furthermore, changing the $Bi_{1-x}Sb_x$ surface orientation can affect the band topology and thus the number of Dirac cones. Zhu et al.[124] have reported that $Bi_{1-x}Sb_x$(110) surfaces exhibit similar topological metallic surface states than $Bi_{1-x}Sb_x$(111) but with three Dirac cones instead of one. Finally, controlling the number of Dirac cones at the $Bi_{1-x}Sb_x$ surface is possible by changing either the growth direction or the induced strain[125].

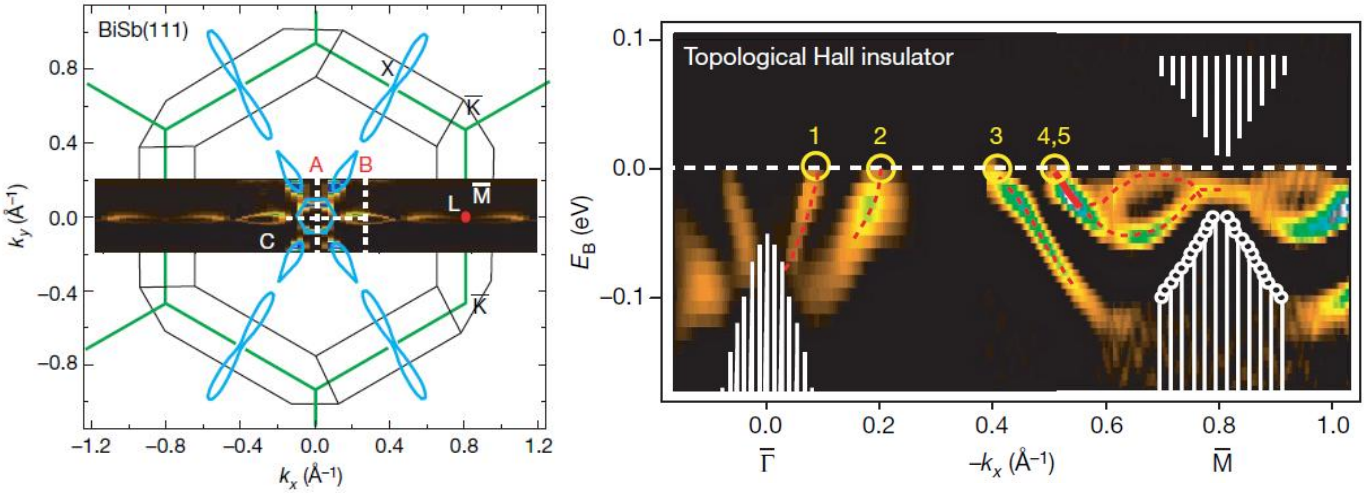


Figure 52: ***(from reference*** *123****): On left:*** *Projection of the bulk Brillouin zone (black lines) onto the (111) surface Brillouin zone (green lines). The overlay shows the high-resolution Fermi surface of the metallic surface state mode, which was obtained by integrating the ARPES intensity (taken with hν=20 eV) from -15meV to 10 meV with respect to E_F. The six teardropshaped lobes of the Fermi surface close to $\bar{\Gamma}$ (the centre of the Brillouin zone) show some intensity variation between them that is due to the relative orientations between the axes of the lobes and the axis of the detector slit. The six-fold symmetry was however confirmed by rotating the sample in the k_x–k_y plane.* ***On right:*** *The surface-band-dispersion second-derivative image of $Bi_{0.9}Sb_{0.1}$ along $\bar{\Gamma} - \bar{M}$. The shaded white area shows the projection of the bulk bands based on ARPES data, as well as a rigid shift of the tight binding bands to sketch the unoccupied bands above the Fermi level. A non-intrinsic flat band of intensity near E_F generated by analysis of the second-derivative image was rejected to isolate the intrinsic dispersion. The Fermi crossings of the surface state are denoted by yellow circles, with the band near $-k_x$<0.5 Å^{-1} counted twice owing to double degeneracy. The red lines are guides to the eye. An in-plane rotation of the sample by 60° produced the same surface state dispersion. There are a total of five crossings between $\bar{\Gamma} - \bar{M}$, which indicates that these surface states are topologically non-trivial.*

3.3 The $Bi_{1-x}Sb_x$ integration on GaAs(001) substrates[126,127]

Despite numerous studies reporting the growth of BiSb materials[128–131] the integration of high quality thin films on industrial substrates remains challenging due to large lattice mismatches, different crystalline matrices, and difficult surface preparations. As reported previously, our choice of material for the substrate is GaAs due to technical limitations and our long experience with its surface preparation. Moreover, combining GaAs based optical devices and TI could also bring new breakthrough in the field of spin–photon conversion[132]. Our first objective is thus to study the growth of $Bi_{1-x}Sb_x$ alloys on industrial GaAs(001) substrates. The $Bi_{1-x}Sb_x$ crystalline structure is rhombohedral (R-3m), while that of GaAs(001) is cubic and the lattice mismatch between both is 13.7%. Only a few papers report the synthesis of BiSb on GaAs(001), and the growth is either amorphous[133] or the surface is (012)[131,134]. Our first objective was thus to optimize the growth of polycrystalline BiSb layers on GaAs and probe their transport properties. Indeed, the TSS of different grains should mix at their junction and, depending on faceting, could be preserved at the macroscopic scale. Since the quality of the substrate surface is primordial for integrating high quality TI layers, an optimized 1µm-thick GaAs buffer layer is grown prior to BiSb deposition. Note that, the surface reconstruction of this GaAs(001) layer changes from $\beta_2(2\times4)$ to $c(4\times4)$ during cooling down.

3.3.1 Influence of the growth temperature

Typically, when developing a new material, the first step is to define an optimal growth temperature window. Therefore, five 250 nm thick $Bi_{0.9}Sb_{0.1}$ samples have been grown at temperatures (T_g) of 132°C, 144°C, 155°C, 166°C, and 177°C (**figure 53**).

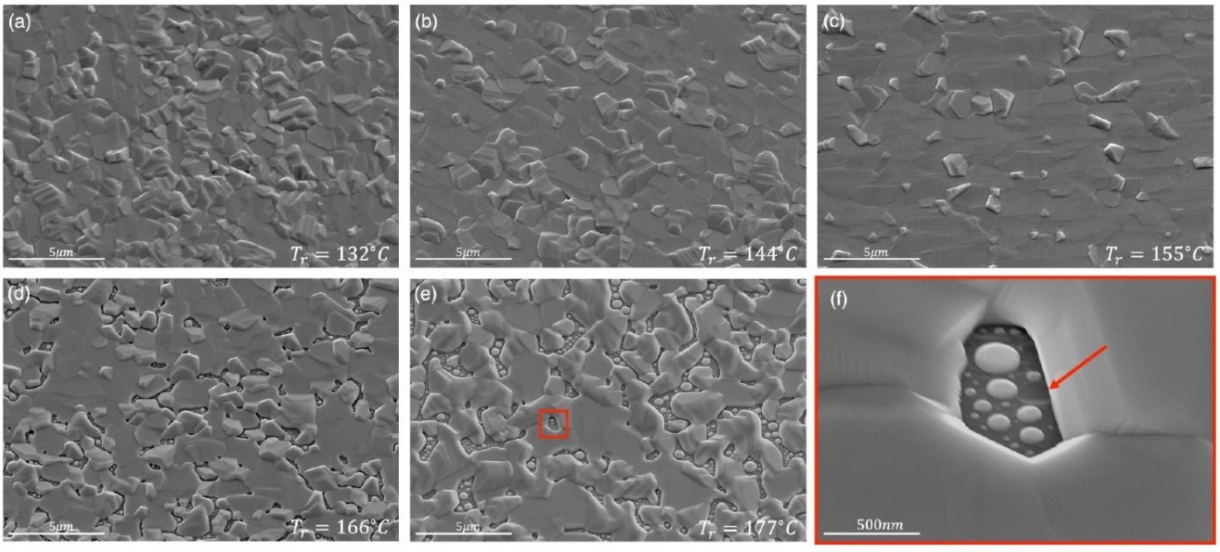


Figure 53: *SEM images showing the surface morphology of as-grown $Bi_{0.9}Sb_{0.1}$ layers for a growth temperature of* ***(a)*** *132°C,* ***(b)*** *144°C,* ***(c)*** *155°C,* ***(d)*** *166°C, and* ***(e)*** *177°C. The SEM image in panel* ***(f)*** *is a zoomed image of the area indicated by the red square in panel* ***(e)****, where adatoms are re-evaporated.*

As expected, the growth is polycrystalline and the surface morphology is directly dependent on the temperature. A reduced surface roughness can be observed for T_g=155°C (figure 53c). At higher temperatures, BiSb evaporates and holes can be observed in the TI layer (figure 53d,e). Figure 53f clearly shows this effect: the red arrow highlights a BiSb droplet that was evaporated after being absorbed at the substrate surface. The melting point under UHV conditions seems to be around T_g=177°C, which is about 100°C lower than the theoretical one at atmospheric pressure.

In order to investigate the in-plane epitaxial relationship between BiSb and GaAs and to probe the temperature dependence of the BiSb texture, XRD pole figure measurements have been carried out at the BiSb(0006) Bragg diffraction angle (figure 54).

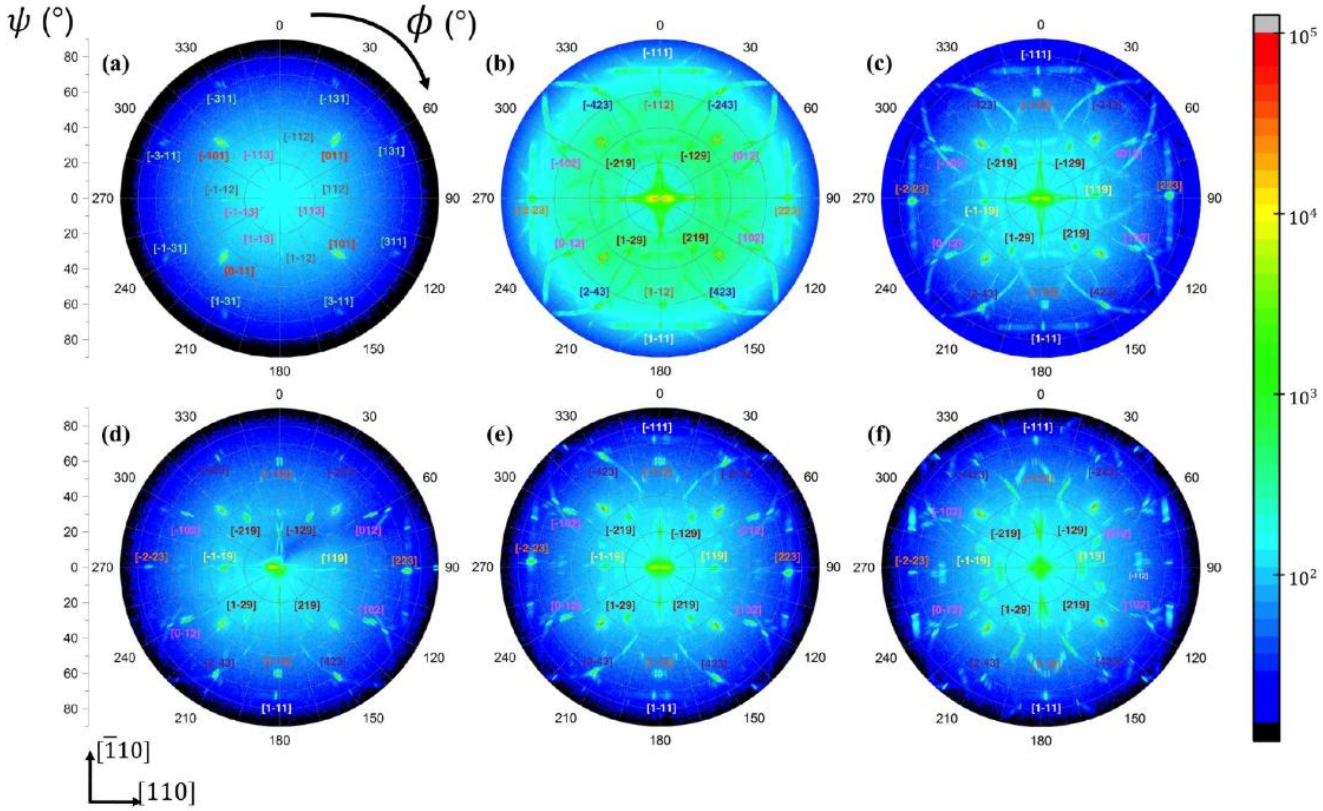


Figure 54: XRD pole figures of different samples using a ϑ–2ϑ configuration around the diffraction Bragg angles of the BiSb {0006} planes. (a) A reference measure on the GaAs(001) substrate is provided. The XRD pole figures of the BiSb thin films are reported (b) for the growth temperature of 132°C, (c) for 144°C, (d) for 155°C, (e) for 166°C, and (f) for 177°C. The color scale on the right corresponds to the X-ray diffracted intensity of the samples in a logarithmic scale. Labels near each spot correspond to the (hkl) planes. All pole figures are performed by rotating the sample around its normal axis (ϕ) at an angular orientation (ψ) of the sample, ranging from 0 to 90°.

On the reference sample [GaAs(001) substrate] (figure 54a), no peak is present at Ψ = 0° and a square geometry is observed for other families of planes: {011}, {112}, {113}, and {311}. For all growth temperatures (figure 54b-f), the central peak, corresponding to Ψ = 0°, has a strong intensity, which demonstrates the preferential [0001] growth direction of the BiSb layer.

Moreover, all diffraction spots detected in the reference pole figure are also observed at the same position in **figure 54b–f** demonstrating the absence of rotation between both layers: [11$\bar{2}$0]BiSb = [110]GaAs. Interestingly, the central peak is elongated along the [110] direction for all $Bi_{0.9}Sb_{0.1}$ samples (**figure 54b–e**) except the one grown at T_g = 177°C (**figure 54f**). This indicates a [110] anisotropic tilt direction for temperatures below 166°C. For the optimized growth temperature T_g = 155°C (**figure 54d**), the stereographic projection presents focused diffraction peaks, which highlights the good crystallinity of the BiSb layer. On the contrary, axiotaxial rings[135] are visible for other temperatures, indicating an increase of the misoriented grain density in different directions.

3.3.2 Influence of the composition

After fine-tuning the growth temperature to T_g = 151°C to reduce the surface roughness, we studied the influence of the antimony composition of the BiSb layer. Four 250 nm thick samples were grown having compositions of $Bi_{0.95}Sb_{0.05}$, $Bi_{0.9}Sb_{0.1}$, $Bi_{0.85}Sb_{0.15}$ and $Bi_{0.8}Sb_{0.2}$, respectively (**figure 55b-f**). For the lowest composition (5%), the surface is rough, disorganized, and has a large number of holes compared to other samples. When the composition is increased to 10%, the surface morphology is better organized and grains present a flat top facet. It can be noticed additionally that some grains have a triangular shape pointing upward (red triangles) or downward (triangles) in the [$\bar{1}$10] direction. This indicates a good epitaxial relationship between BiSb films and the GaAs(001) substrate. Increasing the composition further (15 and 20%) increases the surface disorder. This trend proves the necessity to adapt the growth temperature to the Sb composition, as expected from the bismuth–antimony phase diagram (**figure 49**). More antimony yields to an increase of the melting point and therefore changes the optimal growth temperature. This point is illustrated in **figure 55a,d** for $Bi_{0.95}Sb_{0.05}$ and $Bi_{0.85}Sb_{0.15}$ samples grown at 141 and 163 °C, respectively.

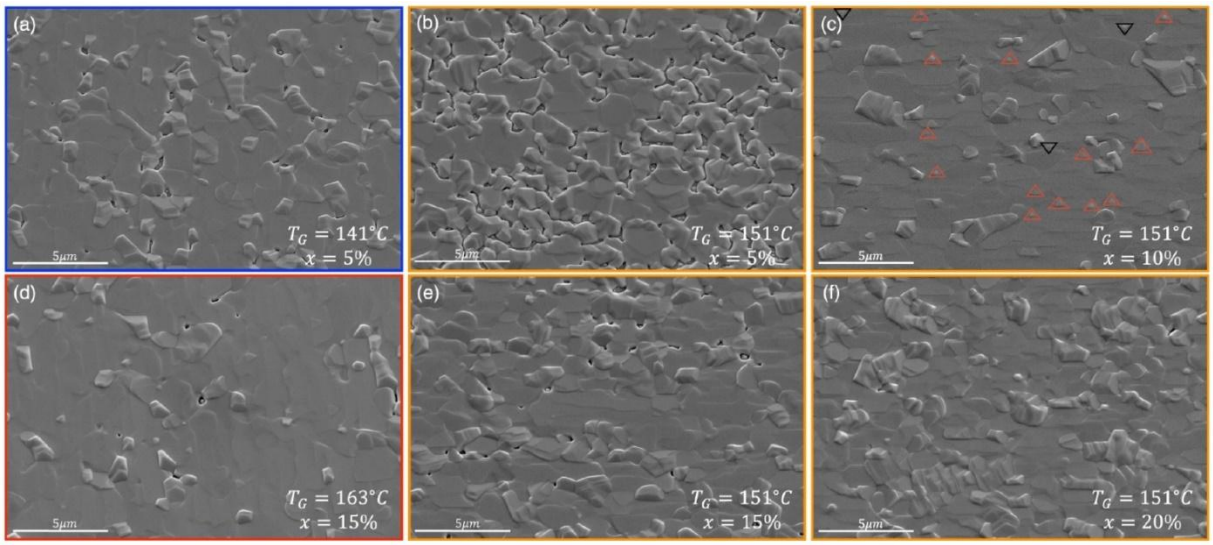


Figure 55: *Evolution of the BiSb surface morphology as a function of the temperature (T_g) and the Sb composition (x). SEM images of the BiSb layer grown on a GaAs(001) substrate with different compositions (a, b) 5%; (d, e) 15%; (c) 10%; and (f) 20%. The blue, orange, and red frames indicate growth temperatures of 141°C, 151°C, and 163°C, respectively.*

To further probe the influence of the Sb composition on the BiSb layer growth mechanism, electron backscattering diffraction (EBSD) measurements have been carried out on the four samples grown at Tg = 151°C (**figure 56**). The high crystallinity of the $Bi_{0.9}Sb_{0.1}$ layer is confirmed with more than 80% of grains that have a negligible tilt (lower than 5°) with respect to the substrate. Moreover, if the tilting angle is directly dependent of the composition, the growth direction remains [0001]. Interestingly, there is a link between the grain size and their orientation: the more negligible their tilt, the larger they are. Indeed, grains having a flat top facet overgrow laterally until they develop enough and coalesce. On the other hand, some misoriented grains keep developing while others disappear and merge with flat topfaced grains. This definitively demonstrate the possibility to integrate high quality BiSb layers on GaAs(001) substrates.

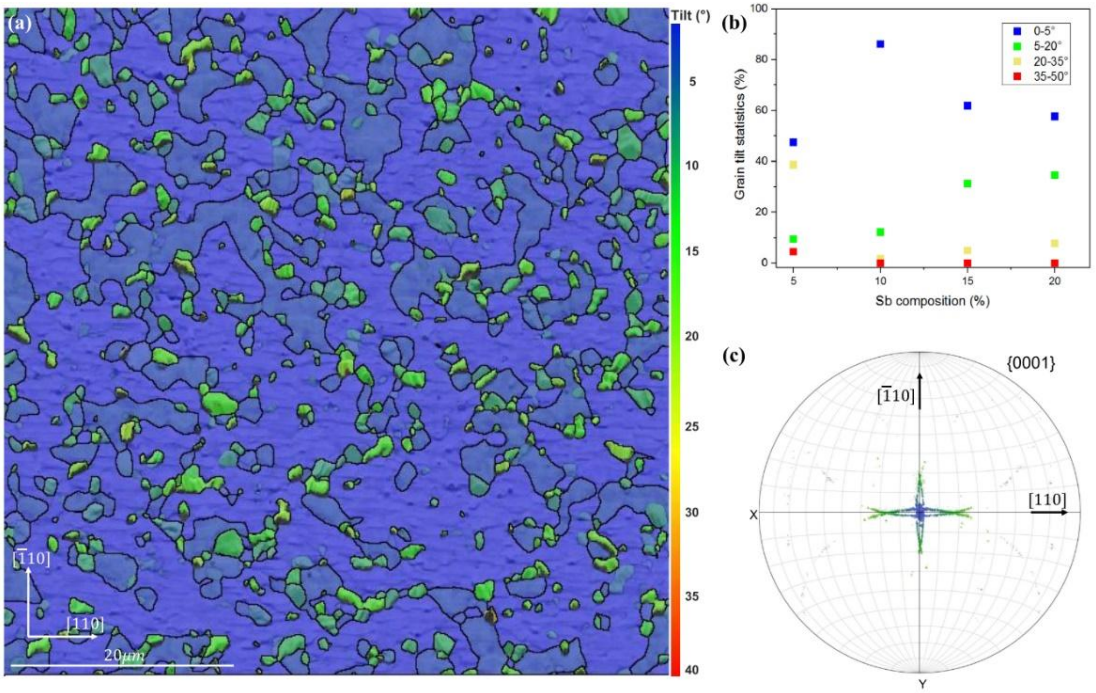


Figure 56: *Determination of the grain orientation. (a) EBSD map showing the angular deviation between the (0001) $Bi_{0.9}Sb_{0.1}$ grains and the GaAs(001) substrate. The color scale corresponds to the tilt ranging from 0 to 40° with respect to the substrate direction. (b) Grain tilt statistics as a function of Sb composition (5, 10, 15, and 20%). (c) Corresponding pole figure displaying the (0001) grain orientation and showing distribution with respect to the [110] and [$\bar{1}$10] GaAs directions.*

3.3.3 Influence of the layer thickness

The growth of thick TI layers allows to probe their fundamental properties and to optimize the growth conditions. Nevertheless, their integration into devices requires to reduce the thickness in order to maximize the surface over bulk conduction ratio. A thickness series was thus synthetized under optimized conditions for $Bi_{0.9}Sb_{0.1}$ films, as reported in **figure 57**. It can be noticed that during nucleation (**figure 57a**), different islands are present at the substrate surface, which indicates a Volmer–Weber growth mode. Thanks to in-situ optical monitoring of the wafer curvature, the stress accumulation is measured during growth[136] and highlights the

different growth steps. The initial islands expand over time, merge with neighbor ones (~ 12 nm) and form bigger grains (**figure 57b**), that later coalesce (~ 30 nm) into a continuous layer (**figure 57c-f**). These observations indicate that the surface chemical potential of BiSb is lower than that of GaAs and that reducing this energy difference will favor 2D growth. Moreover, it confirms that the $Bi_{1-x}Sb_x$ growth is controlled by thermodynamics rather than kinetics, within our optimized conditions. Finally, holes observed in these samples are worrying because they modify the surface topology and can thus "kill" the TSS.

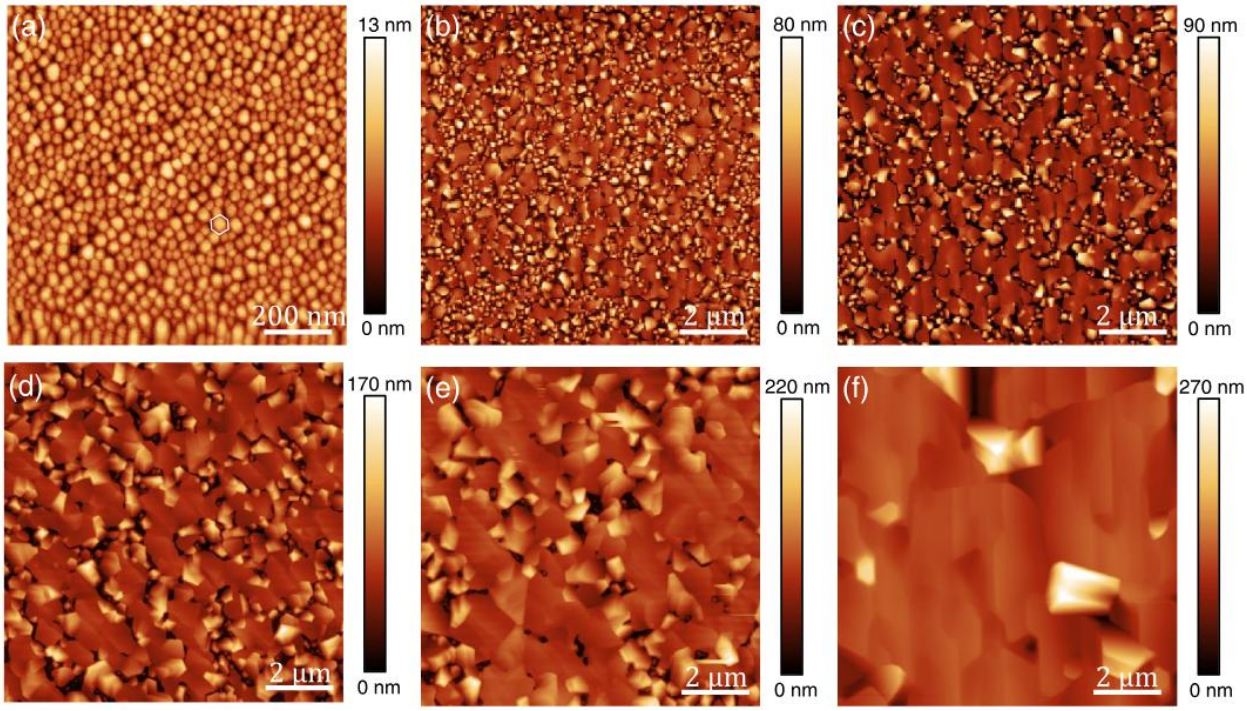


Figure 57: *Evolution of the surface morphology as a function of the BiSb layer thickness. The AFM images are taken for thicknessess of (a) 2 nm, (b) 20 nm, (c) 30 nm, (d) 60 nm, (e) 90 nm, and (f) 450 nm. Note that holes are present in the BiSb layer for thicknesses below 450 nm.*

3.3.4 Influence of Kinetics

After optimizing the growth thermodynamic parameters, we probed the role of kinetics to fine tune the TI surface morphology. Four $Bi_{0.9}Sb_{0.1}$ samples are thus synthesized with growth rates of 0.064, 0.129, 0.26, and 0.385 µm/h and a total layer thickness of 200 nm (**figure 58**). From this series, it is clear that low growth rates favor two-dimensional epitaxy, whereas 3D islands can be observed for higher kinetics. Here, if the mean time interval between the atoms' arrival at the substrate surface is large enough, they can reach their thermodynamics equilibrium and stick to an existing island; i.e. flat-topped grains. Therefore, if the growth rate decreases these islands will attract a larger number of adatoms so that their lateral size increases. In the extreme case of a very low growth rate (**figure 58d**), a continuous layer of flat-topped grains is achieved leading to an optimized surface morphology of the BiSb layer. Nevertheless, further optimizations are required to reduce the hole density and the layer thickness.

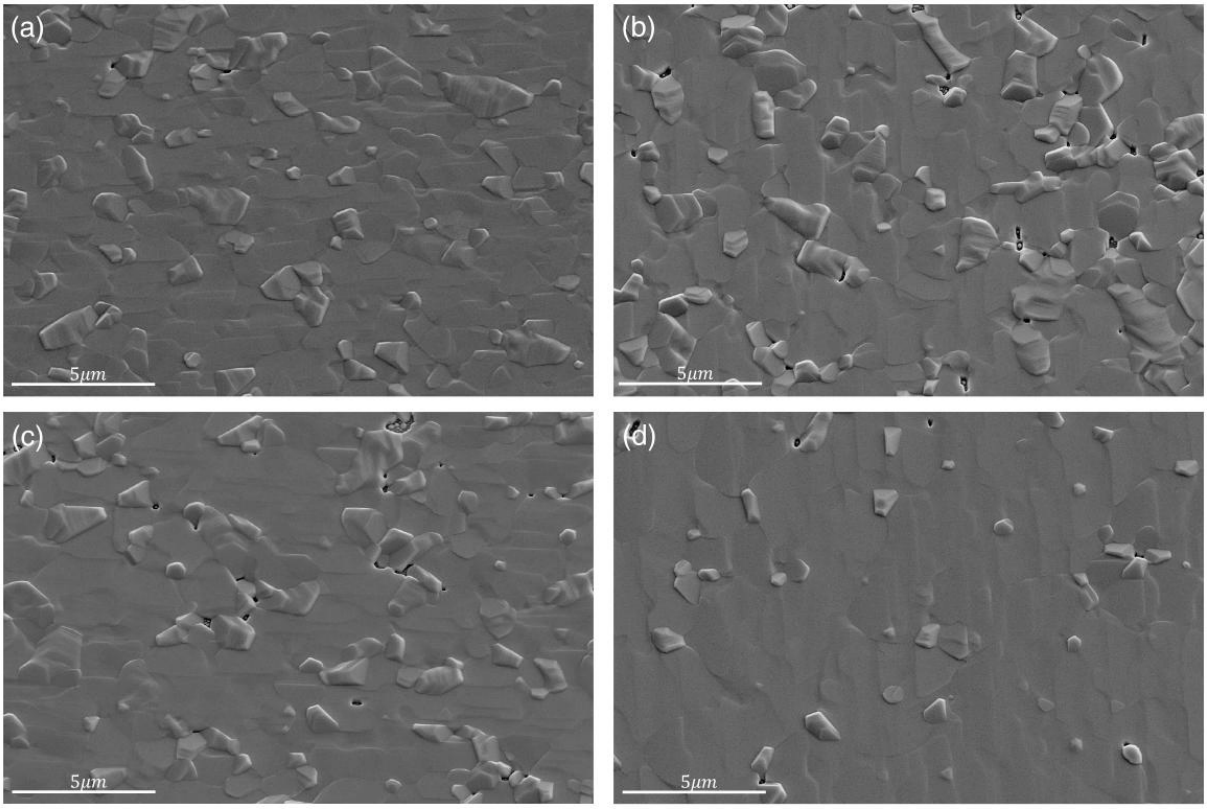


Figure 58: *Evolution of the BiSb surface morphology as a function of the growth rate. All layers have the same composition and thickness, and the respective growth rates are (a) 0.385, (b) 0.26, (c) 0.129, and (d) 0.064 µm/h.*

3.4 The $Bi_{1-x}Sb_x$ integration on GaAs(111)A substrates [137,138]

In addition to the integration on GaAs(001), we choose to also study the integration of $Bi_{1-x}Sb_x$ thin films on GaAs(111)A substrates. (111) surfaces are a "natural" choice for integrating hexagonal or rhombohedral crystals, and several studies already report the integration of BiSb on GaAs(111)[131,139]. The main difference between GaAs(111)A and GaAs(111)B surfaces is the surface reconstructions in both cases and the presence of Ga atoms one monolayer below the reconstruction in the case of GaAs(111)A. This is of firm importance since a van de Walls nucleation process is expected in the case of GaAs(111)B, whereas a covalent nucleation mechanism is possible in the other. If a van der Walls epitaxy is generally preferred for reducing strain during nucleation, it limits possibilities for scaling up and can lead to grain nucleation in different directions, which results in a polycrystalline layer after coalescence. On contrary, we demonstrated thanks to density functional theory (DFT) calculations performed on GaAs(111)A surfaces that the deposition of Bi or Sb atoms on a β(2x2) reconstructed GaAs(111)A surface, lead to the formation of Ga-Bi or Ga-Sb bounds (figure 59). Standard heteroepitaxy of BiSb on GaAs is thus possible in the latter case, which opens new integration possibilities and a better scaling up for devices.

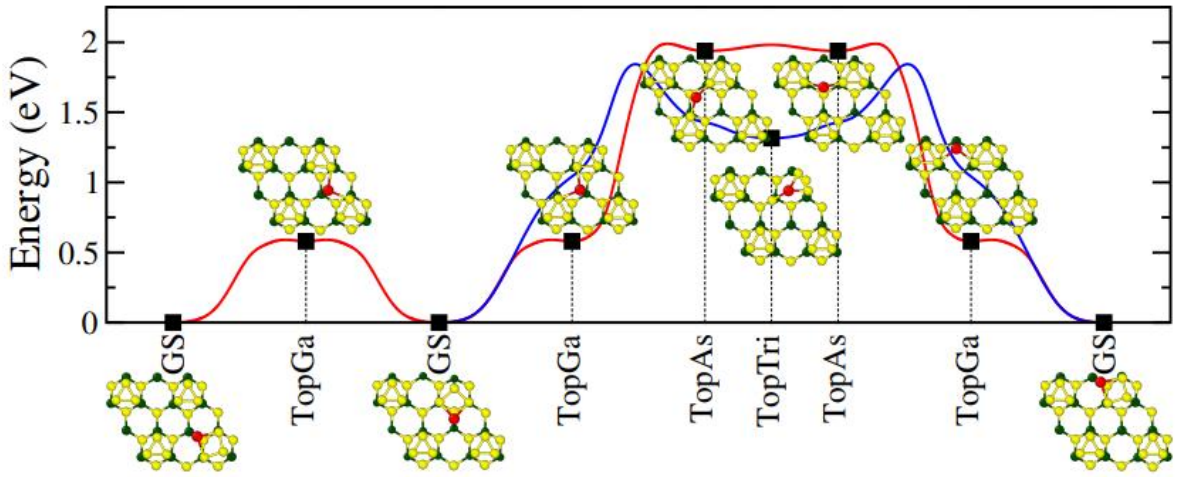


Figure 59: *Minimum energy pathways (blue and red lines) of the Bi atom between the ground state positions above the GaAs (111)A surfaces. Red balls represent the adsorbed Bi atom.*

Indeed, four stable adsorption sites are possible on the GaAs(111)A surface:

- In the ground state site (GS^{111}, E^{1}_{ad} = −3.69 eV), Bi adatoms can brake one of the As trimer bonds and be bonded to two As atoms of this trimer and to a Ga atom of the sublayer.
- In the top Ga adsorbed site ($TopGa$, ΔE=0.57 eV) and top As adsorbed site ($TopAs$, ΔE=1.94 eV), the Bi atom is bonded to one Ga atom (resp. to one As atom with non-covalent bond) of the sublayer and bonded to two different trimers.
- In the top trimer adsorbed site ($TopTri$, ΔE=1.29 eV), the Bi atom is on top of the trimer, changing its geometry from equilateral to isosceles-like and breaking two As–As bonds of the trimer.

From these calculations, it is clear that reducing kinetics favours the GS^{111} configuration, and that it is almost impossible for Bi atoms at this position to diffuse on the substrate surface. Indeed, each site can be reproduced three times per trimer due to the centro-symmetry. To diffuse from a GS^{111} site to another topologically equivalent one on the GaAs(111)A surface, two minimum energy paths are possible with a similar energy barrier. In the first one, the Bi atom diffuses by contouring the trimers passing through the intermediate configurations according to the sequence $TopGa$, $TopAs$, $TopAs$, $TopGa$ (E_b = 1.99 eV), while in the second one, it diffuses by passing over the As-trimer using the adsorbed configuration $TopTri$ (E_b = 1.84 eV). In both cases, the energy barrier is too high to move a Bi atom from the GS^{111} configuration during growth, which thus prevents the diffusion of Bi on the surface once the GS^{111} configuration is reached.

Considering the optimal $Bi_{1-x}Sb_x$ growth conditions found for GaAs(001), a series of four samples (x = 0.07, 0.11, 0.15, 0.19) is grown on GaAs(111)A substrates at 151°C (figure 60). Two distinct area can be observed on these SEM images: a smooth matrix surrounding rough grains. If the surface morphology is comparable with growths on GaAs(001) substrates, its evolution with the antimony composition differs. Here, increasing the antimony composition leads to larger grains having a lower density.

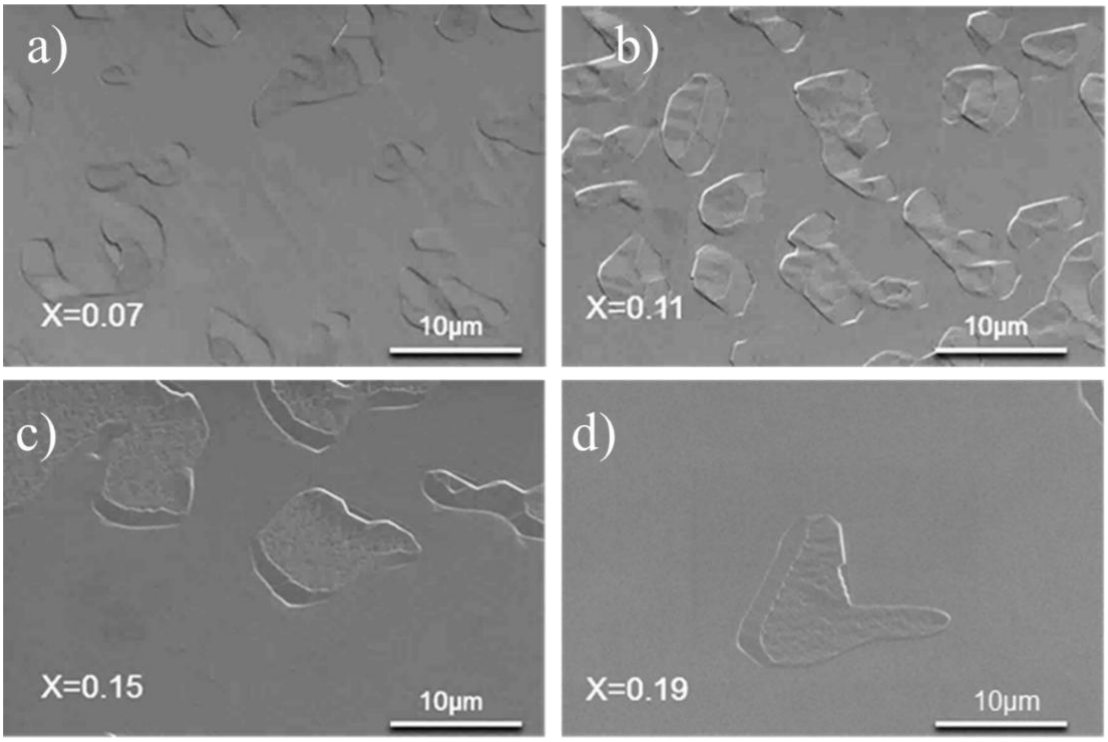


Figure 60: SEM images showing the surface morphology of 2µm thick $Bi_{1-x}Sb_x$ thin films grown on GaAs(111)A substrates. The x composition is equal to (a) 0.07, (b) 0.11, (c) 0.15 and (d) 0.19.

The films' crystallinity was probed by X-ray diffraction measurements in a ϑ-2ϑ geometry (figure 61a). As expected, a BiSb(0001)/GaAs(111)A epitaxial relationship is found between the layer and the substrate and no parasitic phase is observed. The zoomed-in ϑ-2ϑ diagrams presented in figure 61b indicates a BiSb(0006) peak shifting to higher angles when increasing the antimony composition. Such a trend reveals the expected evolution of the out-of-plane lattice parameter as a function of the composition. Interestingly, unfamiliar peaks' intensity changes are observed depending on both the azimuthal angle (Φ) and whether alignments are performed along the substrate or the film. In order to understand and identify the origin of such behaviour, reciprocal space maps (RSM) were collected around the $Bi_{0.89}Sb_{0.11}$(0006) diffraction peak at different azimuthal Φ angles, as reported in figure 61c-f. First, it can be noticed that only two peaks are visible in these maps for different q_z positions, which corresponds to both the BiSb (0006) film and the GaAs (222) substrate. If the GaAs peak is narrower than the BiSb one, no trail is observed between both, which indicates strain relaxation at the layer-substrate interface by misfit dislocations. When changing the Φ angle, the BiSb(0006) peak is shifted laterally, indicating a tilted orientation of the $<0001>_h$ axis of BiSb

film compared to the <111>$_c$ one of the GaAs substrate (**figure 61g-i**) close to 1.0°. Such a small value is not expected to affect the TSS properties.

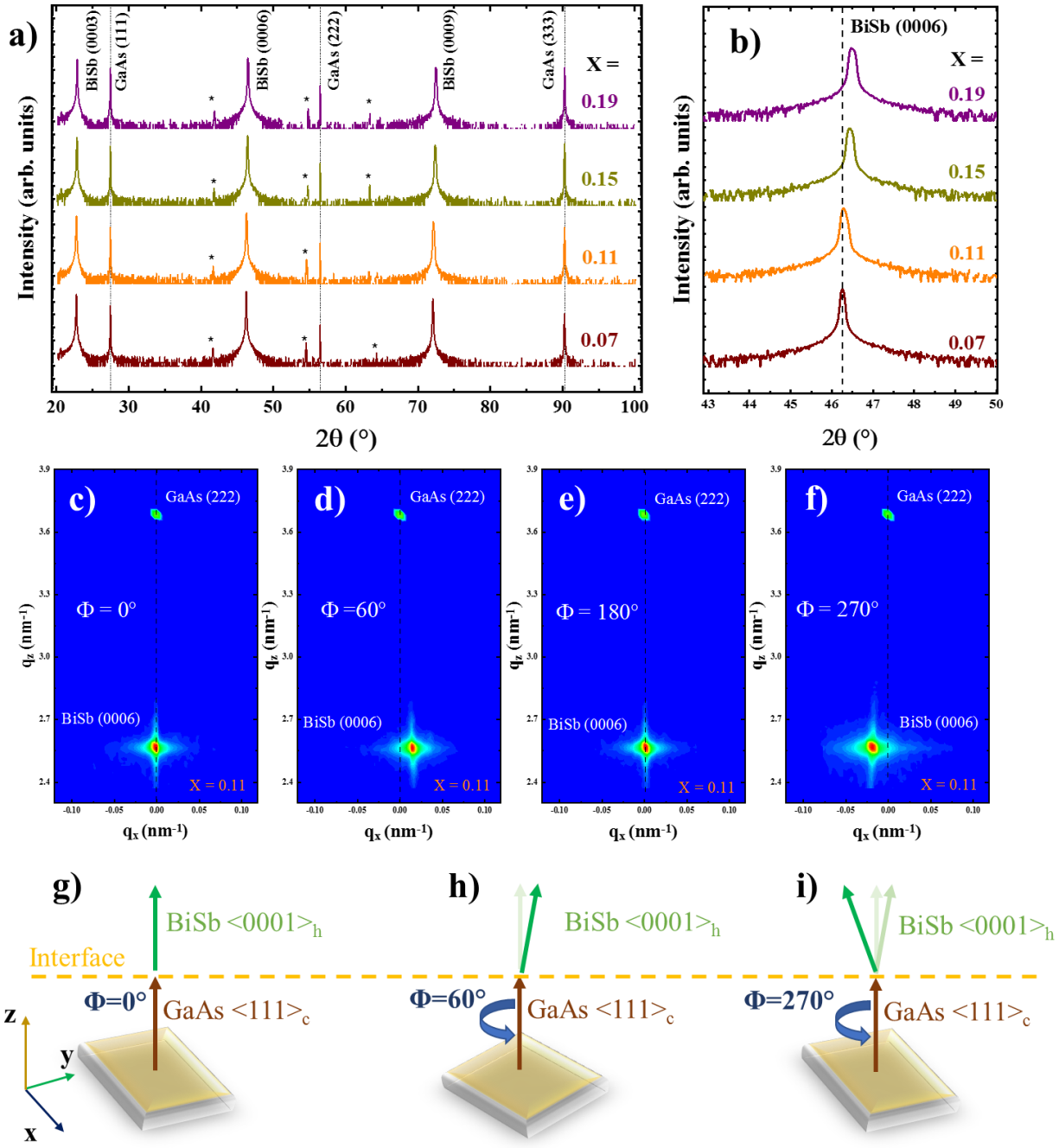


Figure 61: *X-ray diffraction analysis of four $Bi_{1-x}Sb_x$ thin films with x = 0.07, 0.11, 0.15 and 0.19.* ***(a)*** *ϑ-2ϑ diffraction patterns up to the third diffraction order. Peaks indicated by asterisks (*) are generated by the sample holder.* ***(b)*** *Zoomed-in region at an angular range around the BiSb (0006) reflection. The dashed line is a guide for the eyes. The peaks shift to higher angles when increasing the antimony composition. Reciprocal space mapping around the $Bi_{0.89}Sb_{0.11}$ (0006) reflection and the GaAs (222) reflection are presented for azimuthal angles of* ***(c)*** *Φ=0°,* ***(d)*** *Φ=60°,* ***(e)*** *Φ=180°, and* ***(f)*** *Φ=270°. The BiSb (0006) reflection shifts along q_x when rotating the sample around Φ.* ***(g)***, ***(h)*** *and* ***(i)*** *Schematics of the real-space crystallographic-axis relation at the film-substrate interface for Φ azimuthal angles of 0°, 60° and 270°, respectively. The Φ origin is arbitrarily defined for a condition where the BiSb(0006) and GaAs(222) reflections are axis-aligned with q_x=0 nm^{-1}.*

After probing the BiSb layer crystallinity at the macroscopic scale, we focused on the grains and the domain walls they form within the continuous layer. Indeed, such interfaces can have a crucial influence on the transport properties as discussed in section 2.8. High-resolution scanning transmission electron microscopy (HR-STEM) measurements of these interfaces are reported in figure 62.

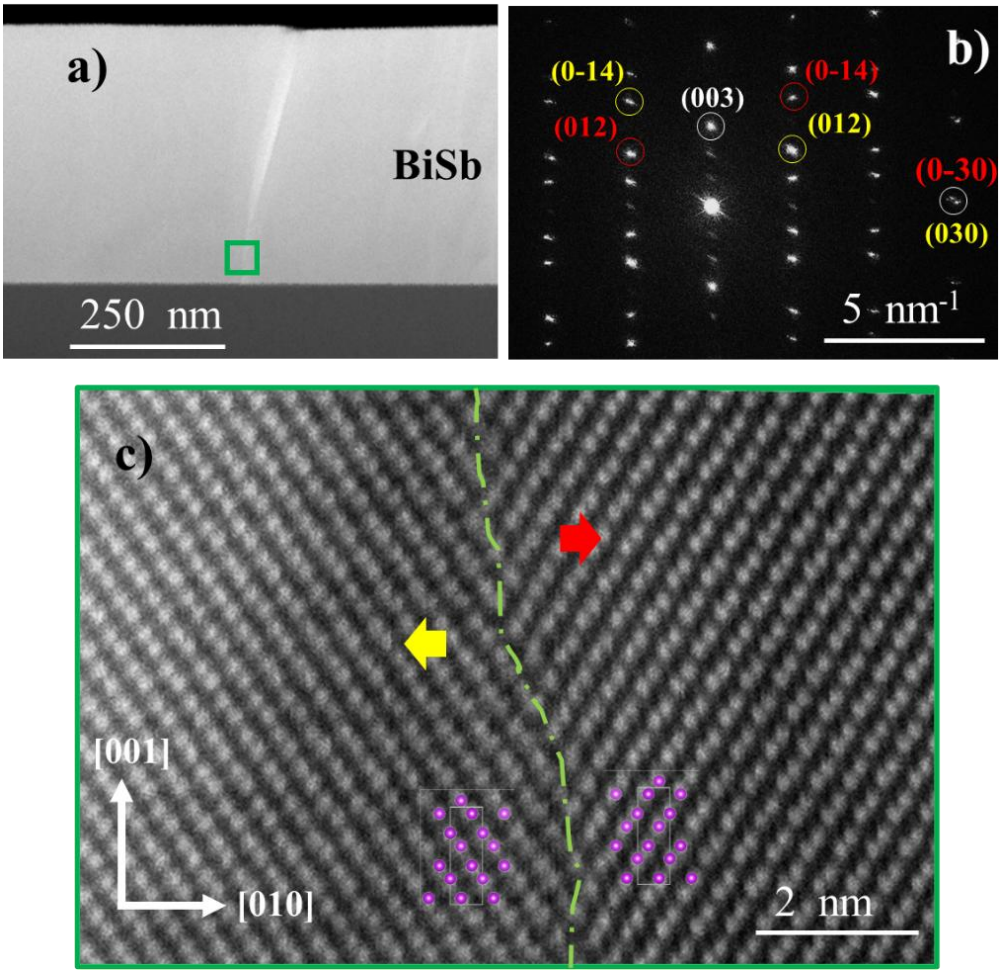


Figure 62: ***(a)*** *Cross-sectional STEM-HAADF image of a 450 nm-thick BiSb film grown on GaAs (111)A substrate. The grain boundary originates at the interface and reaches the film's surface.* ***(b)*** *Corresponding fast Fourier transform (FFT) showing the diffraction pattern of the two BiSb grains in the <100> zone axis. Red and yellow annotations indicate the two different grains.* ***(c)*** *High-angle annular dark-field (HAADF) scanning TEM image acquired in the green area, showing atomic arrangement within both domains' boundaries. The respective crystalline structures on both sides of the grain boundary are indicated in purple.*

Here, the grain and the continuous 2D layer are separated by a slightly tilted boundary. The corresponding FFT pattern shows equivalent but inverted in-plane crystal structures for the two domains. Reflections in red and yellow are equivalent to the same (hkl) families but appear at different reciprocal space positions due to a 180° in-plane rotation of the crystalline structure (figure 62b). On contrary, the out-of-plane component exhibits no change across the grain boundaries. The atomic resolution STEM image of the interface (figure 62c) highlights the abrupt change in the crystal structure orientation, as is indicated by the green dotted line.

Such a texture is confirmed at the macroscopic scale by XRD pole figures acquired around the $Bi_{0.89}Sb_{0.11}$ (0009) Bragg reflection for a 300 nm-thick sample (figure 63).

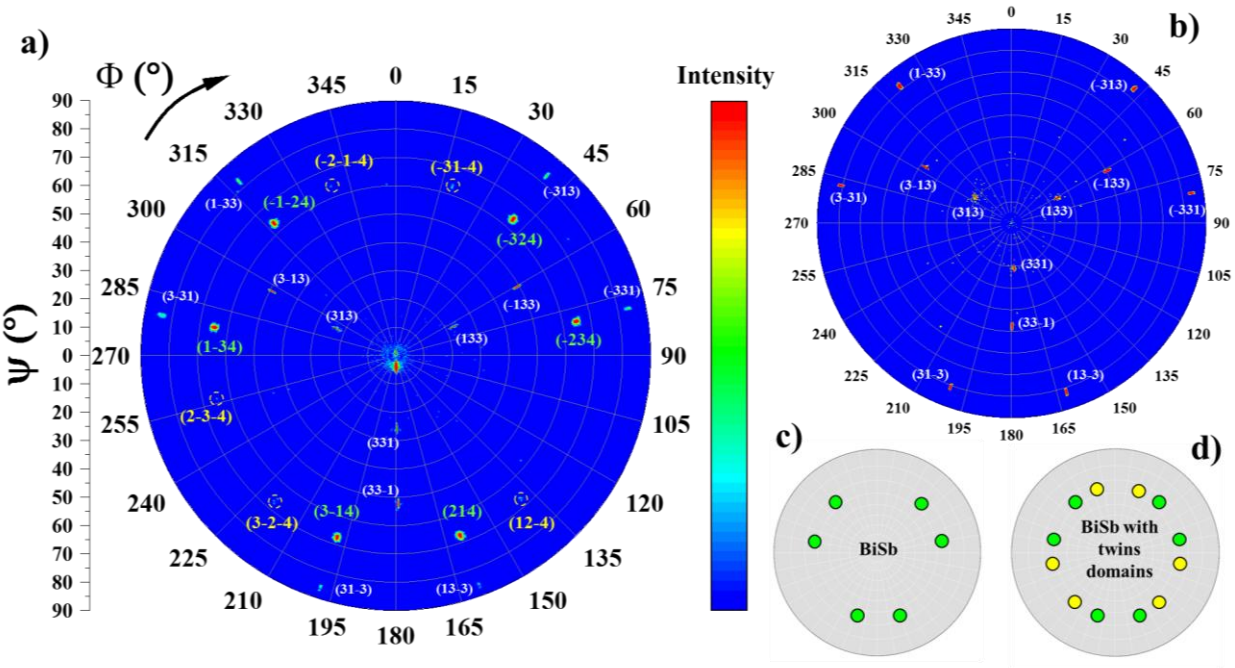


*Figure 63: X-ray diffraction pole figures performed around the $Bi_{0.89}Sb_{0.11}$ (0009) Bragg reflection ($2\vartheta \approx 72.2°$) of **(a)** a 300 nm-thick film, and **(b)** on a GaAs (111)A substrate. The diffracted intensities are presented in a logarithmic scale. The labels near each reflection correspond to the attributed (hkl) planes. A specific colour code is used for each type of reflection: white for the cubic GaAs substrate, green and yellow for both trigonal BiSb twins, using a hexagonal (hkl) system. Models obtained using WinWulff software for single crystalline and twinned BiSb films are presented in **(c)** and **(d)**, respectively.*

Here, both substrate and film exhibit a threefold symmetry, and the substrate's reflections are labelled in white in figure 63a,b. WinWulff simulations are conducted to identify the twinned BiSb crystalline structures as reported in figure 63c,d, and the layers without and with twins are labelled in green and yellow, respectively. Six intense reflections, (green in figure 63a), aligned with the substrate's ones, are observed for the untwined crystal, which corresponds to the 2D matrix. Such an alignment points-out the epitaxial relationship between the GaAs and BiSb through the interface and during the growth process as reported previously. Moreover, weak extra reflections are observed (yellow circles) at the same ψ angular positions but with an 180° in-plane ϕ rotation. These peaks correspond to the twined grains observed in both HR-TEM and SEM images, that similarly to GaAs(001) originate from the GaAs-BiSb interface. Interestingly, the intensity of twin related diffraction peaks is decreasing when the antimony composition is increased. This trend, consistent with SEM observations (figure 60), might be explained by the favourable Sb atoms bonding to the As-rich surface compared to Bi ones. Indeed, ionic Sb-As bounds are more stable and easier to create than Bi-As ones[137].

Therefore, an hypothesis we formulate is that the deposition of a Sb bilayer, before the BiSb film, could affect the domain walls formation and promote the BiSb single crystalline growth.

In order to probe this hypothesis, a 500nm-thick BiSb film was grown after deposition of an antimony bilayer on the GaAs(111)A substrate (figure 64b). Contrary to the conventional process (figure 64a), this surface preparation allows the nucleation of monocrystalline BiSb films with no domain structure. Instead, multiple triangular-shaped defects are observed on the film's surface, always pointing in the same in-plane direction. This is to our knowledge the first large scale single crystalline integration of a topological insulator on an industrial substrate.

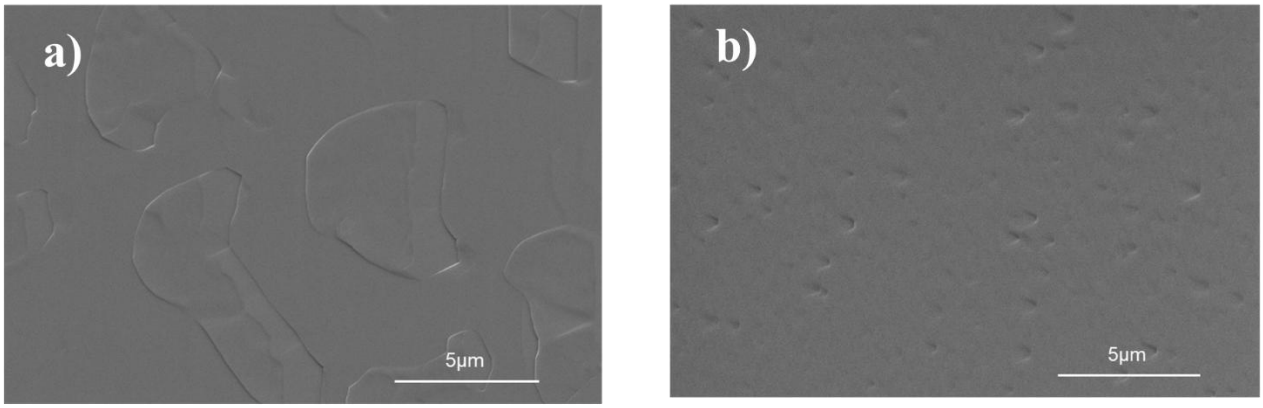


Figure 64: ***(a)*** *SEM image of the surface morphology of the 500nm thick $Bi_{0.85}Sb_{0.15}$ layer grown directly on GaAs(111)A substrate.* ***(b)*** *SEM image of the surface morphology of a 500nm thick $Bi_{0.85}Sb_{0.15}$ layer grown in identical conditions but starting with an Sb bilayer on the GaAs (111)A surface.*

By combining this surface preparation with reduced kinetics, as already reported for GaAs(001) substrates, it is possible to grow optimized BiSb layers on GaAs(111)A having a reduced thickness (< 25nm) and a low surface roughness (figure 65). This result is of primordial importance for future integration of high-quality TI in quantum computers and spintronics devices (Chapter 4).

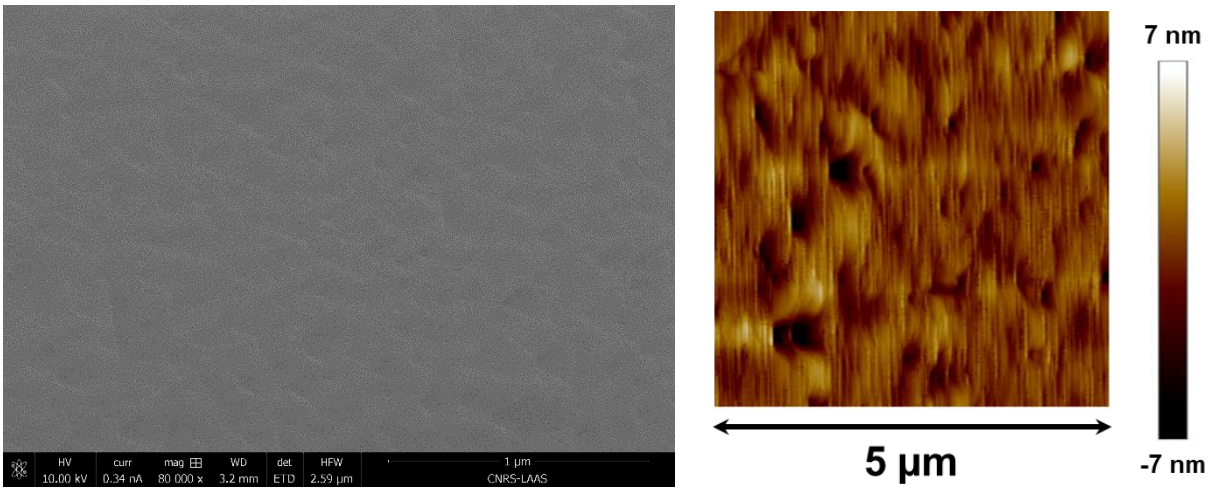


Figure 65: *On left: SEM image of a 25nm thick $Bi_{0.9}Sb_{0.1}$ layer integrated on GaAs(111)A. On right: AFM image of the surface, showing a R_a roughness about 1 nm.*

3.5 The transport properties of the $Bi_{1-x}Sb_x$ layers

Now that growths have been optimized on both substrates, it is crucial to probe the transport properties of these BiSb layers. Indeed, their fundamental interest lies in their unique topological surface states. Charge carriers occupying these states have their spin degree of freedom locked to their momentum thus reducing the backscattering and enabling spin-charge conversion. Nevertheless, the big challenge is to disentangle the electronic contribution of the surface metallic states from that of the bulk, in particular at the nanoscale. The presence of impurities and structural defects in TI materials strongly affects their electronic properties and can even mimic their TSS signature, making it difficult to detect their true nature.

3.5.1 On the GaAs(001) substrates

In order to distinguish between both contributions, several $Bi_{0.9}Sb_{0.1}$ samples, having different thicknesses, have been grown on GaAs(001) substrates under optimized conditions (see section 3.3). The samples are then prepared for electrical characterizations using standard lithography techniques as reported in figure 66.

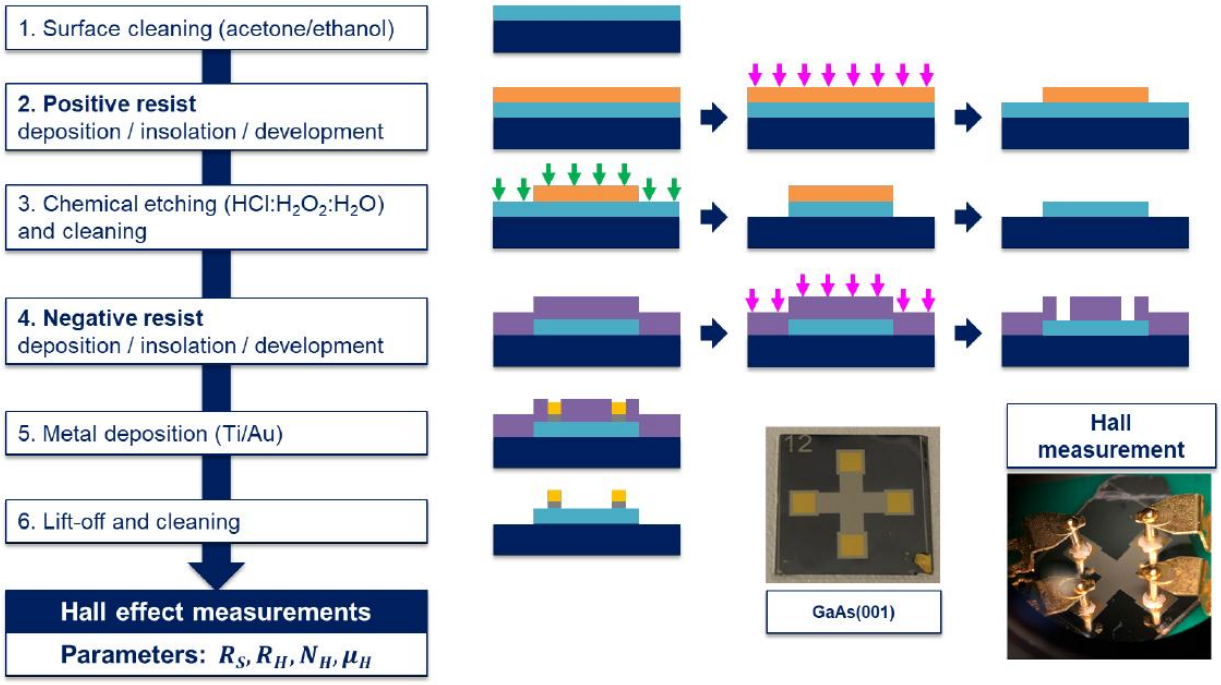
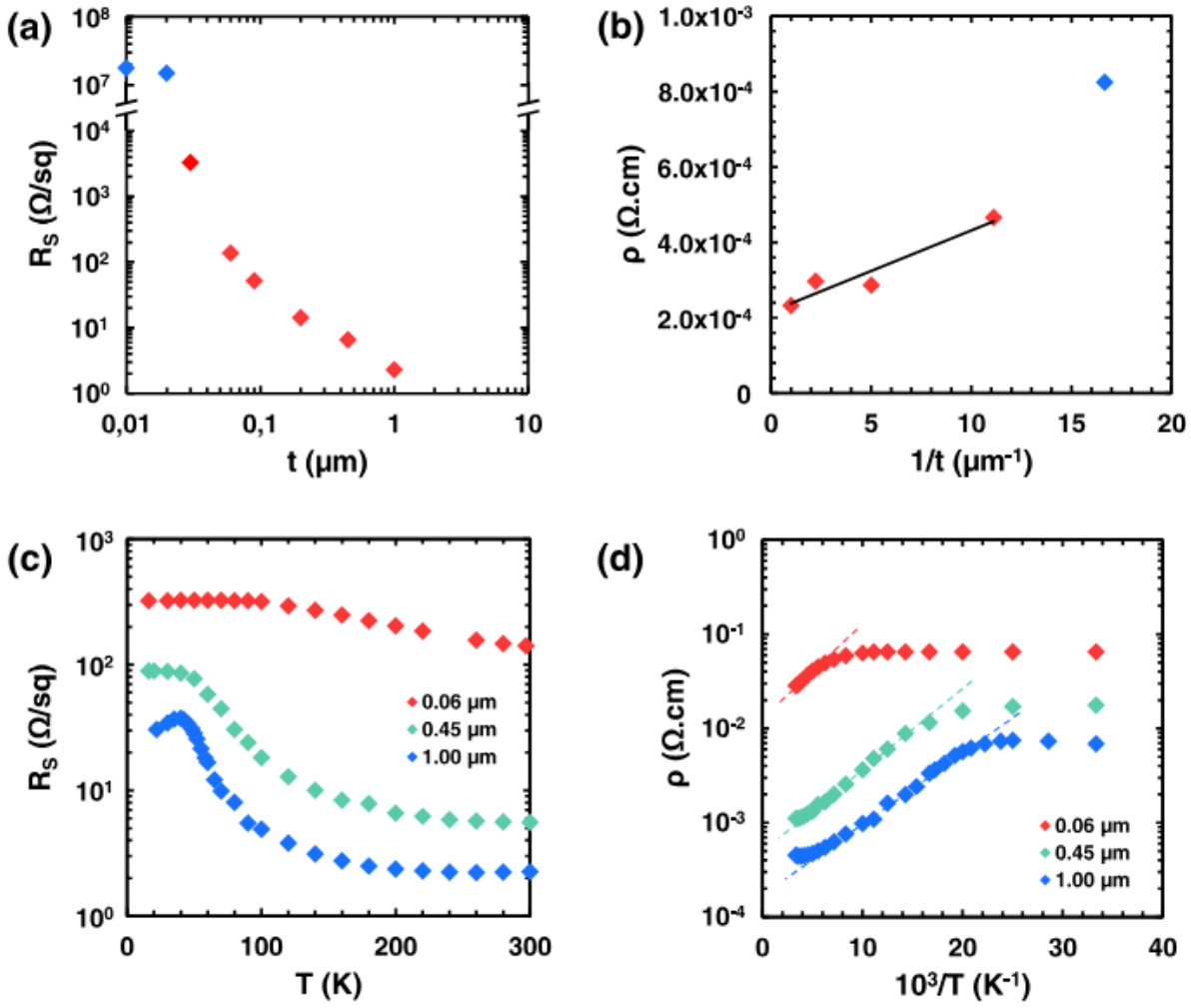


Figure 66: Standard fabrication steps of the Hall effect samples

The electronic properties of BiSb layers are studied using the van der Pauw method. First, the sample sheet resistance R_S is extracted from the standard four-point probe (4PP) measurement. The Hall coefficient R_H is then measured using an external magnetic field of 0.3 Tesla orthogonal to the sample's surface. From these two parameters, we calculated the Hall sheet carrier concentration N_H and the Hall mobility μ_H.

The summary of the electrical measurements in reported in **figure 67**. First, it can be noticed that the evolution of the sheet resistance as a function of the BiSb layer thickness is in good agreement with previous structural characterizations. Indeed, for thicknesses smaller than 20 nm, (blue squares in **figure 67a**), the samples exhibit a high sheet resistance, which correspond to the configuration with small isolated grains (**figure 57**). In these conditions, the current is carried through the GaAs substrate rather than in the BiSb grains, which explains the measured sheet resistance of ***Rs*** *~10^7 Ω/□* close to the substrate one *(~5×10^7 Ω/□)*. At 30 nm, the sheet resistance decreases quickly, indicating the coalescence of small grains into larger, interconnected domains, opening thus a new, highly conductive channel. Further increases in thickness do not enlarge these domains but increase the cross-sectional area of the conductive channel. As a result, the sheet resistance continues to decrease, reaching as low as 2.3 Ω/□ for a 1 µm thick layer.



*<u>Figure 67:</u> Four-point probe measurements on the BiSb layers. **(a)** Evolution of the sheet resistance **Rs** as a function of the BiSb layer thickness **t**. Blue and red dots refer to nonuniform and continuous grown layers, respectively. **(b)** Evolution of the resistivity with the inverse thickness. Values depicted in red dots fulfill the Tellier et al.[140] limitation conditions. The electron mean free path is extracted from the slope of the black straight line. **(c)** Sheet resistance evolution with the temperature for three different BiSb layer thicknesses. **(d)** Calculated values of the resistivity (from **Rs**) plotted as a function of the inverse temperature. The activation energies of the BiSb layers can be extracted from the linear dependences at high temperatures, shown in dashed lines*

Assuming that the current flowing through the GaAs substrate is negligible for thicknesses of 60 nm and beyond, we calculated the resistivities ρ from the corresponding sheet resistance values and the BiSb layers' thicknesses. As shown in figure 67b, resistivity appears to be thickness-dependent. Using an extended version of the Fuchs-Sondheimer model[140–142], which predicts the electrical properties of polycrystalline thin layers, we determined an electron mean free path l_g of approximately 265 nm, a value that surpasses those reported in the literature[143–145] (~150 nm). According to this model, the thin film resistivity is given by:

$$\rho_f = \rho_0[1 + \frac{3}{8t}(1 - p)l_0]$$

where ρ_0 and l_0 are, respectively, the bulk crystal resistivity and mean free path, t is the thickness, and p is the probability of carriers being scattered at the surface. In the case of a polycrystalline thin film, Tellier *et al.*[140] showed this equation remains valid when using ρ_g, the hypothetical polycrystal bulk resistivity, instead of ρ_0 and substituting l_0 by an effective mean free path l_g defined by:

$$l_g \approx \frac{\rho_0}{\rho_g} l_0$$

The validity of this model is limited by the assumption that grains and boundaries are identical for different thicknesses and that $t/l_0 > 0.6$. These conditions are met for layer thicknesses exceeding 90 nm (red diamonds in figure 67b). In our calculations, we assume that all charge carriers are diffusely scattered at the surface, implying that the probability p of specular reflection at the layer surface is zero and that the calculated value for l_g is minimized (for $p = 0.5$, the value of l_g is doubled).

Considering the evolution of the sheet resistance R_s as a function of temperature in figure 67c, the TI behavior of the BiSb layer is confirmed, regardless of the sample thickness. Indeed, R_s increases as the temperature decreases (starting at T = 300 K), indicating the semiconductor behavior of the BiSb films. For temperatures below 100K, R_s saturates before following an opposite trend, which is the signature of metallic states. For these temperatures, the 2D carrier density is constant, which indicates a 2D conducting channel. These trends, together with the analysis of the carrier mobility values that will be presented in the following, are consistent with TSS, as published in many studies[146].

Finally, the Arrhenius plot of the resistivity ρ (figure 67d) indicates a thermally activated behavior. From the slope of the linear fit, we extract activation energies for the different thicknesses: 15.4 meV for a 1 µm thick sample, 17.7 meV for the 450 nm one, and 18.0 meV for the 60 nm one. These activation energies are of comparable values to the half of the BiSb band gap energy indicated in the literature[147], which confirms the non-intentionally doped (NID) semiconductor behavior of the BiSb bulk materials.

To further probe the transport properties of such layers, temperature dependent Hall measurements have been carried out and are reported in **figure 68**. The most noticeable observation is that the Hall coefficient R_H changes sign from negative to positive at 55 K for the 450 nm and 1 µm thick samples (**figure 68a**). At high temperatures, R_H is negative, indicating that electrons are the majority carriers. However, as the temperature decreases, R_H undergoes an abrupt transition to positive values, signifying that holes become the majority carriers. This transition occurs at the same temperature observed in **figure 67c** and aligns with a shift from bulk to surface conduction. For the 60 nm thick sample, R_H remains negative across the entire temperature range, showing different behavior compared to the thicker layers. At high temperatures, carriers are thermally activated as expected for NID semiconductors, and their concentration decreases with lowering temperature (**figure 68b**). At 300K, the carrier concentrations for all three samples are of the same order of magnitude (3–9 × 10^{19} cm^{-3}), indicating similar bulk behavior. In contrast, below 55K, a clear distinction between thick (450 nm and 1 µm) and thin (60 nm) samples emerges (**figure 68a-c**). These results are consistent with a BiSb TI behavior at low temperatures and strongly suggest n-type bulk conduction for all samples at high temperatures (>100 K) and p-type TSS for the 450 nm and 1 µm thick samples at low temperatures (<55 K).

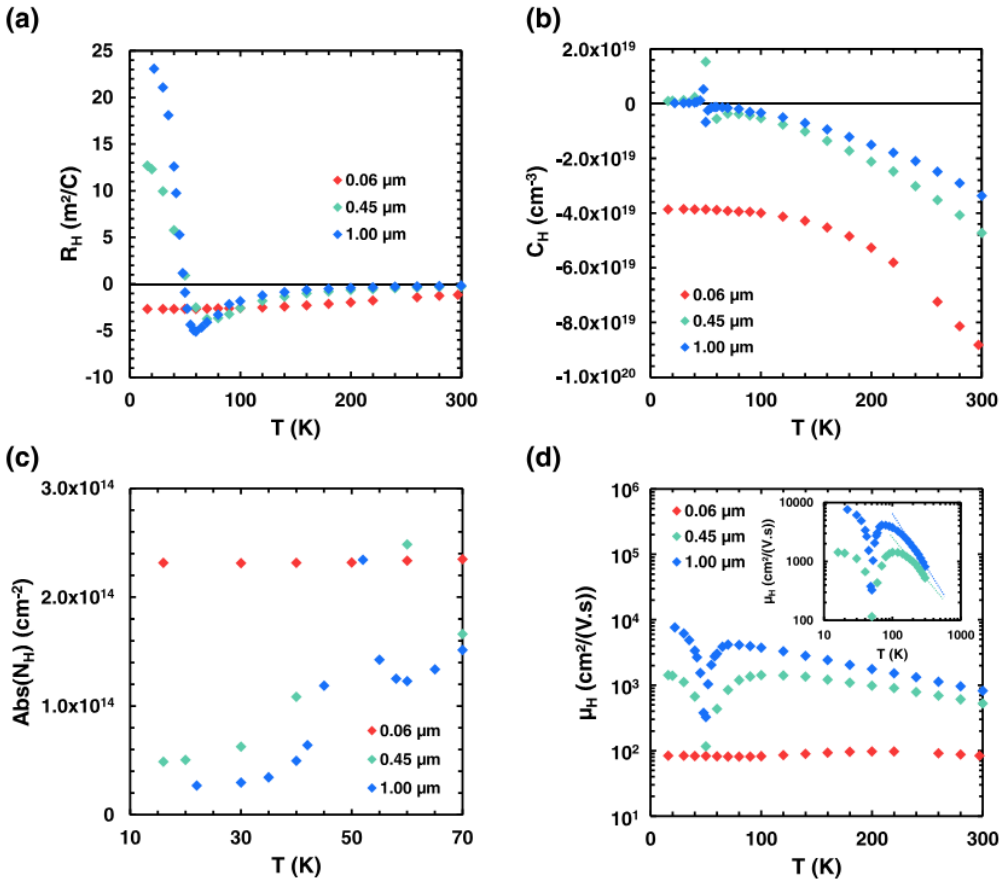
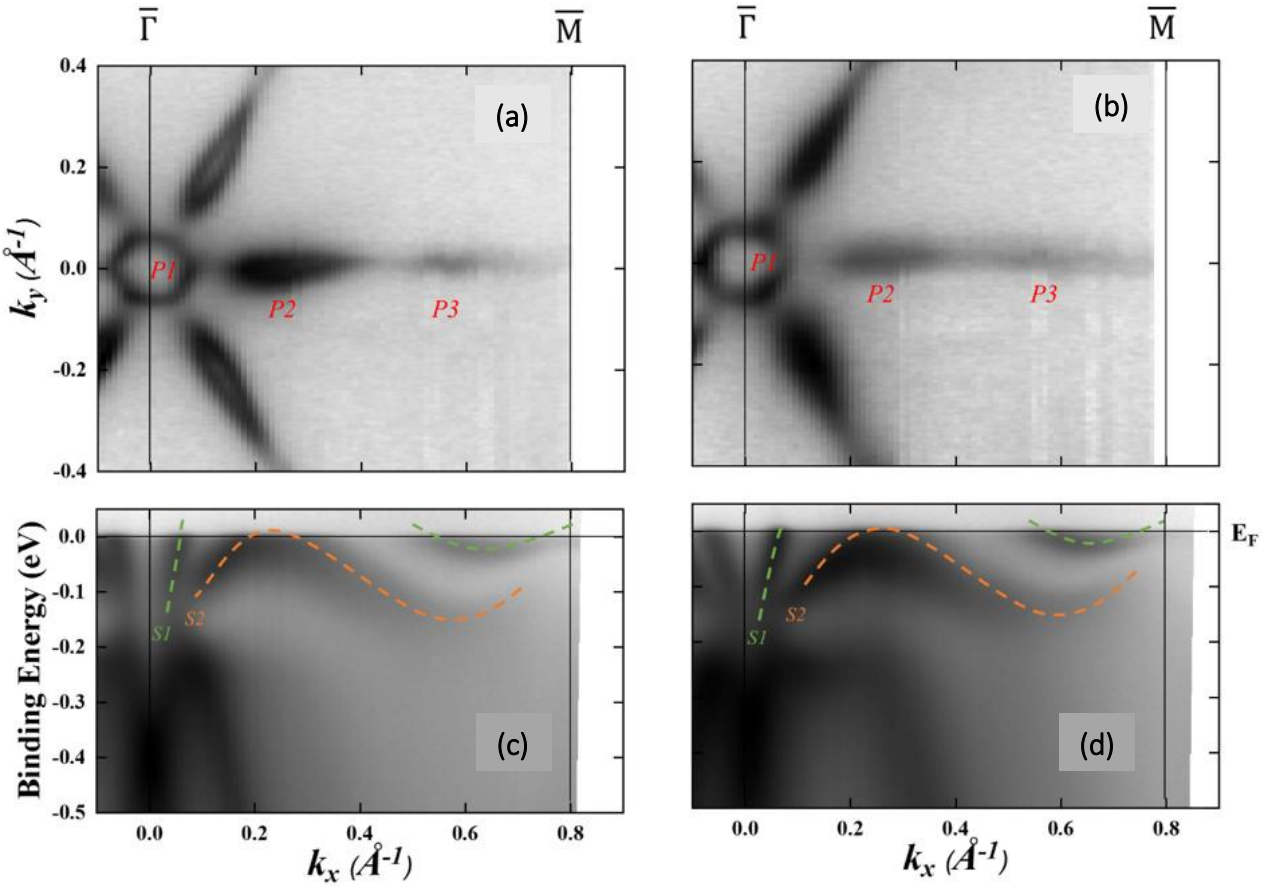


*Figure 68: Hall measurements on the BiSb layers. **(a)** Evolution of the Hall coefficient R_H, **(b)** the Hall concentration C_H, **(c)** the absolute values of the Hall sheet concentration N_H, and **(d)** the Hall mobility μ_H as a function of the temperature. The inset in panel **(d)** shows the Hall mobility as a function of the temperature, in logarithm scales, along with the T^{α} dependencies, in dashed lines.*

The Hall mobilities' evolution with temperature is depicted in **figure 68d**, where a clear distinction between thin and thick samples is evident. In the case of the 450 nm and 1 µm samples, the Hall mobilities exhibit a temperature dependence between 100 and 300 K, close to $T^{-1.9}$ and $T^{-2.3}$, respectively. These trends closely resemble those induced by phonon scattering of electrons within the bulk, known to have a $T^{-1.5}$ dependence in conventional semiconductors such as silicon. However, for the thinnest layer, a $T^{-0.9}$ dependence is observed between 220 and 300 K. The reduction in slope from -2.3 to -0.9 with decreasing thickness might be attributed to enhanced surface scattering due to degraded surface morphology. At low temperatures (<55 K), the electron Hall mobility of the 60 nm thick sample remains relatively constant around 80 $cm^2V^{-1}s^{-1}$, likely due to its poor morphology and the presence of structural holes in the BiSb layer. Conversely, a continuous increase in hole Hall mobility is observed for the thick samples as temperature decreases from 55 to 20 K. The hole mobilities reach 1430 $cm^2V^{-1}s^{-1}$ at 16 K for the 450 nm thick sample and 7620 $cm^2V^{-1}s^{-1}$ at 22 K for the 1 µm thick sample. The combination of metallic surface states observed at low temperatures (**figure 67c**) and the exceptionally high hole mobilities (**figure 68d**) suggests that these states are topologically protected, affirming the high quality of the BiSb layers directly integrated into GaAs(001). This finding aligns well with the BiSb topological insulator phase on (111) surfaces, where hole-like bands are predicted to contribute significantly to surface conduction[148,149].. Lastly, it's worth noting that for temperatures below 55 K, a temperature dependence of $T^{-0.4}$ is observed for hole mobility (**figure 68d**), a behavior not corresponding to any known scattering mechanism, warranting further investigation.

3.5.2 On the GaAs(111)A substrates

Before embarking on the same study for BiSb layers grown on GaAs(111)A substrates, it's essential to comprehend the impact of the two growth processes on the TSS. Indeed, the presence of grain boundaries and the surface roughness could move the Fermi energy level in the bulk and change the surface transport properties. Consequently, the electronic structure evolution of both $Bi_{0.85}Sb_{0.15}$ films presented in **figure 64** was measured by angular resolved photoemission spectroscopy (ARPES) to track any change in the topological surface states. Fermi surface maps obtained by measuring the band dispersion along $\bar{\Gamma} - \bar{K}$ direction for conventional and domains-free films are shown in **figure 69a,b**, respectively. As previously reported[123,150,151] the surface state intensity shows a hexagonal core (**P1**) centered at the $\bar{\Gamma}$ point and associated with the **S1** surface states band crossing the Fermi level. The **P1** hexagon is encircled by six petals oriented in $\bar{\Gamma} - \bar{M}$ directions, representing the **P2** hole pockets of the **S2** band and the **P3** electron pockets of the **S1** band's local minima. It's worth noting here that despite the surface states exhibiting a sixfold symmetry in both films, the photoemitted intensity of the bulk bands displays a pronounced threefold **C3** symmetry, which reflects the underlying crystalline structure, as illustrated in **figure 70**. A shift in the shape of the **P2** petals is noticeable, accompanied by bands' broadening in the case of the film without domains, which makes it challenging to discern the opening or closing of the petals.



*<u>Figure 69:</u> **(a)** and **(b)** Fermi surfaces recorded on conventional and domains-free films, respectively. **(c)** and **(d)** respective cross sections showing the band dispersion along the $\bar{\Gamma} - \bar{M}$ direction of the same two samples. Vertical black lines indicate the $\bar{\Gamma}$ and $\bar{M}$ points positions, respectively. Horizontal black lines indicate the Fermi level position. Green and orange dashed lines are guides for the eyes.*

When looking at the energy dispersion along the $\bar{\Gamma} - \bar{M}$ direction (**figure 69c,d**), two **S1** and **S2** surface states are observed (green and orange dashed lines). Apart from the initial crossing of **S1** near $\bar{\Gamma}$, the **S2** band displays two additional Fermi level crossings for both films. A distinct shift is noticeable in the domain-free film, possibly stemming from a slight misalignment of the sample. Moreover, the **S1** band double-crosses the Fermi level near the vicinity of the $\bar{M}$ point, resulting in an odd number of Fermi level crossings for both samples, which is a direct signature of their topological nature and the presence of the TSS. It's worth mentioning that no **S3** state is observed in our samples near the $\bar{M}$ point, as reported by Hsieh et al[123]. Subsequent theoretical and experimental investigations suggest that this **S3** band arises from surface imperfections, and only **S1** and **S2** surface bands should be observable[122,150]. The TSS in our samples are thus comparable to those recently reported for ultrathin BiSb layers, and only achieved through growth in a MBE chamber directly connected to the ARPES setup in an ultra-high vacuum environment[150,152]. Notably, there is no significant difference in the TSS observed between samples grown with or without the Sb bilayer.

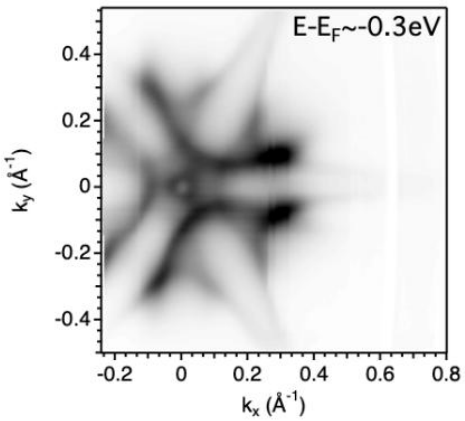


Figure 70: *Iso-energy cut (**E-E$_F$**≈-0.3eV) showing photoemitted intensity around **Γ** point along **K$_x$** and **K$_y$** directions for the conventionally grown BiSb film. The photoemitted intensity has a strong **C3** symmetry, i.e. the same feature is repeated each 120° rotation angle. Thus, two **E vs. k** cuts aligned 60° apart are expected to show different photoemitted intensities.*

With the confirmation of the TI behavior of the BiSb layers integrated on GaAs(111)A substrates, the next crucial step for future devices is to comprehend their electrical transport properties. Consequently, four $Bi_{0.9}Sb_{0.1}$ samples have been grown with different thicknesses of 50 nm, 100 nm, 500 nm and 2 µm under optimized conditions. Hall devices are fabricated using the procedure presented previously. First, transport measurements are carried out in a four-terminal Van der Pauw configuration at room temperature and zero-magnetic field. Figure 71a shows the thickness dependence of the sheet resistance per square R_s at 300 K. It can be seen that the sheet resistance decreases from *80* to *1 Ω/□* with the thickness increasing. This trend is the same compared to the growth on GaAs(001) substrates. For thicknesses greater than 25 nm, the surface is covered with large interconnected domains that finally merge and form a continuous layer for thicknesses above 60 nm. In the following, we will assume that the current passing through the GaAs substrate is close to zero for thicknesses greater or equal to 50 nm. Figure 71b illustrates that the resistivity ρ exhibits a linear dependence on the inverse thickness for h > 100 nm, which is in good agreement with Tellier's model[140]. Here again, we only used this model on samples having a h/l_0 ratio greater than 0.6 and thus to sample thicknesses greater than 100 nm. In contrast to the situation with GaAs(001), we consider here $p = 0.5$ since BiSb films grown on GaAs(111)A are monocrystalline. l_g is about 350 nm which is slightly better than for GaAs(001) (265 nm) and better than that mentioned in the literature (162 nm)[143]. In the model, the grain boundaries, which are present in the polycrystalline BiSb films grown on GaAs(001), are viewed as disordered regions that trap the charge carriers, resulting in a reduction of the electron mean free path l_g. However, as previously mentioned, a high conductivity is measured in the case of GaAs(001), comparable to that of GaAs(111)A. This phenomenon can be explained by two potential mechanisms: the presence conducting dislocations in the bulk or the spreading of the TSS to several grains. As discussed previously, 90° dislocations exist at the BiSb/GaAs(001) interface, which may induce one-dimensional (1D) gapless states, as reported in the $Pb(Bi_{1-x}Sb_x)_2(Te_{1-y}Se_y)_4$ TI[153]. Therefore, dislocation conduction could partially offset the decrease in conductivity caused by trapped carriers at grain boundaries.

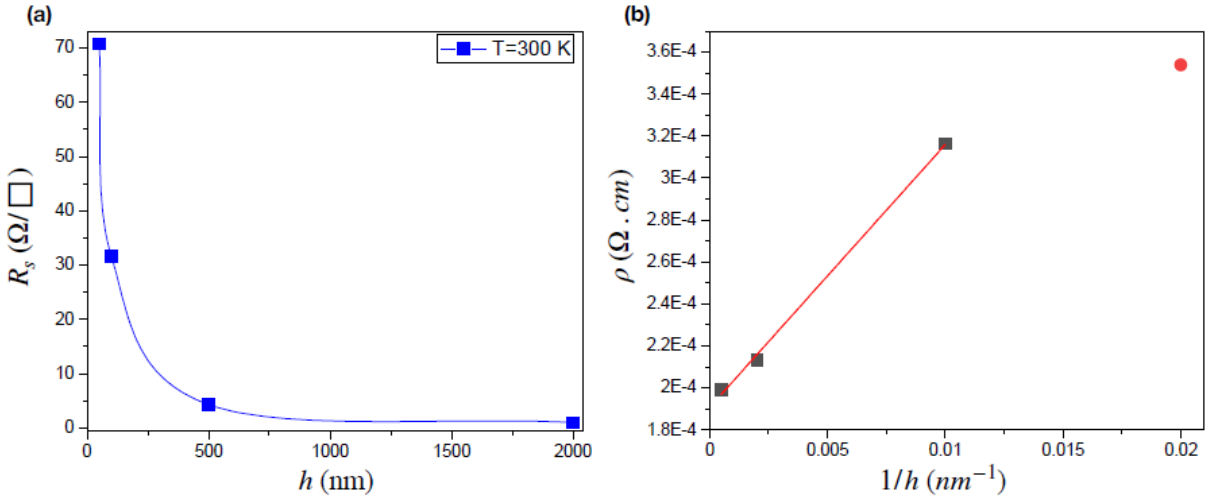


Figure 71: *The influence of the film thickness on the BiSb electrical resistance.* ***(a)*** *Evolution of the sheet resistance as a function of the BiSb film thickness.* ***(b)*** *Electrical resistivity as a function the thickness inverse.*

The temperature dependence of the sheet resistance R_s for different thicknesses is shown in **figure 72a**. Similarly to what is observed for GaAs(001) samples, R_s increases when the temperature decreases for temperatures above 150K, which indicates a semiconductor behavior. Moreover, the two thickest samples show a decrease in R_s for temperatures below 70K, which is attributed to the TSS. By decreasing the thickness to 100 and 50 nm, this metallic behavior appears at higher temperature (100K).

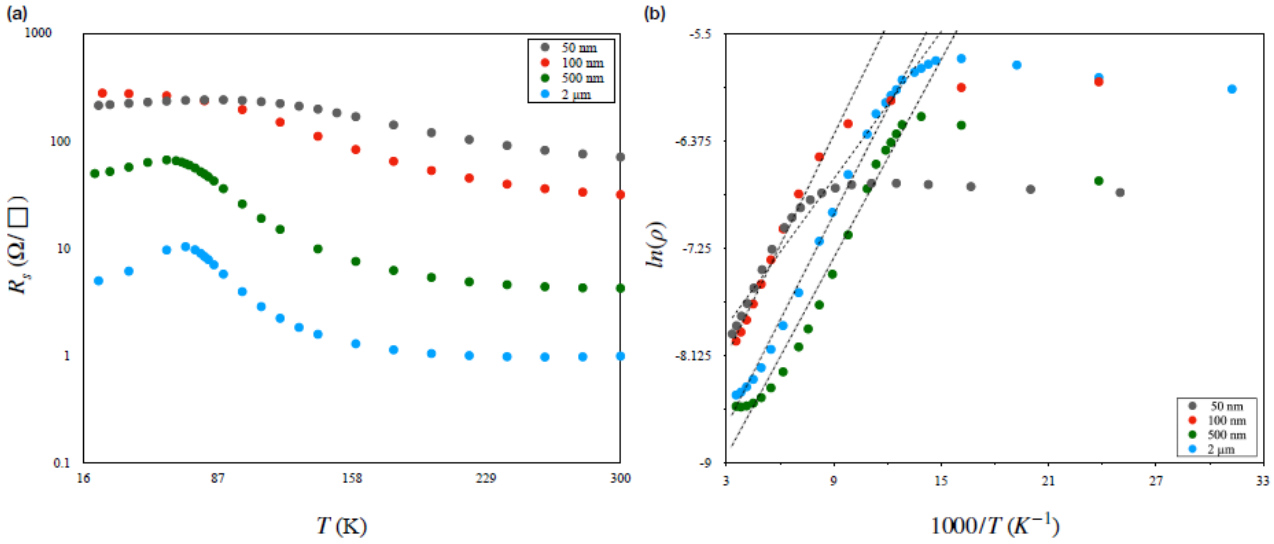
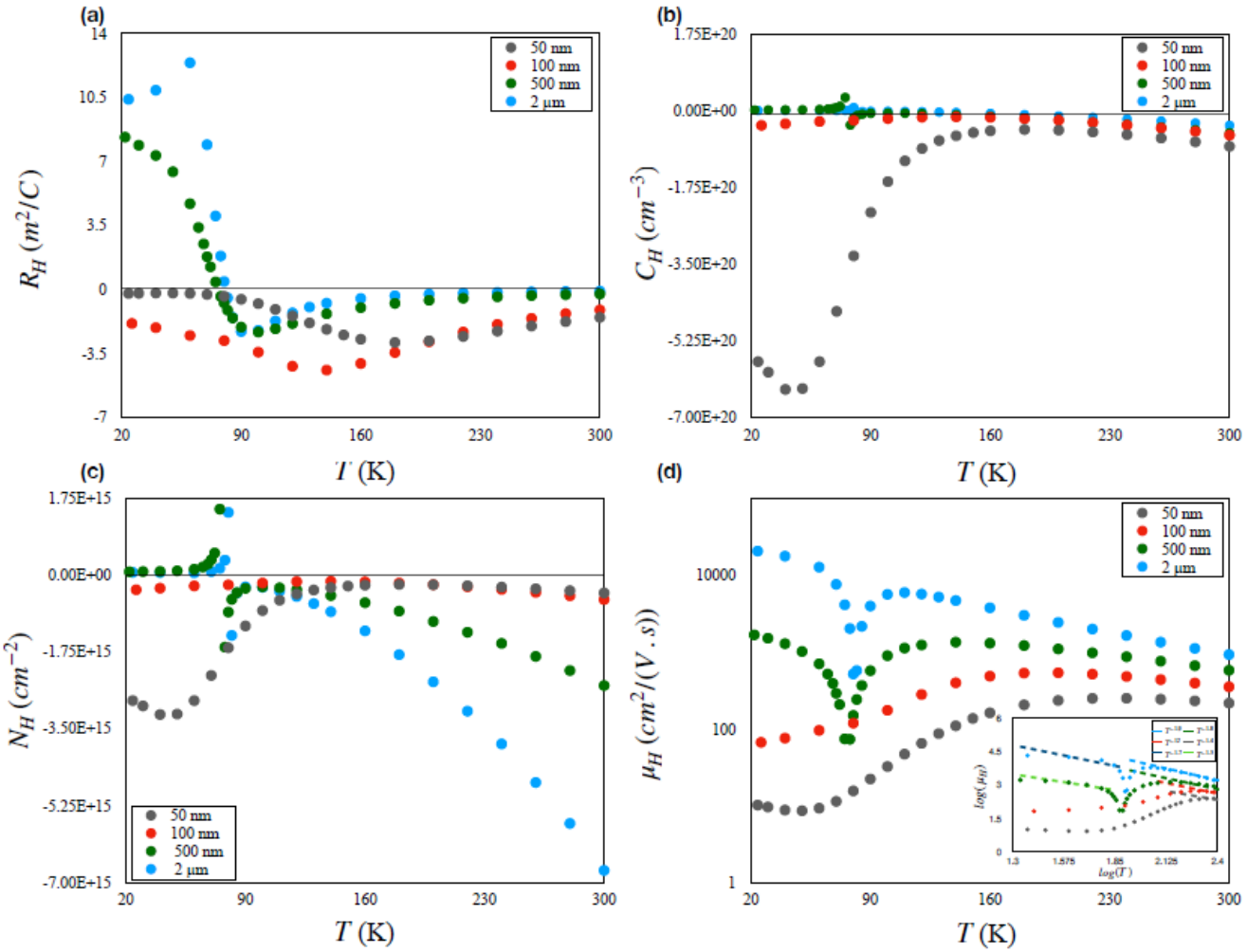


Figure 72: ***(a)*** *Sheet resistance evolution with the temperature for four BiSb layer thicknesses, highlighting bulk conduction at high temperature and surface states currents at low temperature.* ***(b)*** *Plot of* ***ln(ρ)*** *as function of the temperature inverse. Activation energies can be extracted from the linear dependences at high temperature, showed by dotted lines.*

Similarly to GaAs(001) samples, Arrhenius activation energies (E_a) are calculated from a linear fit in figure 72b and are equal to 25.3 meV, 24.3 meV, 22.5 meV and 21.7 meV for thicknesses of 50 nm, 100 nm, 500 nm and 2 µm, respectively. These values are slightly greater than the half BiSb bandgap energy reported in the literature[147]. Contrary to the fully relaxed BiSb layers grown on GaAs(001), a compressive stress accumulation is present for GaAs(111)A samples due to their monocrystallinity. Here, the biaxial residual strain can increase the bandgap width, which has already been observed in other materials[154,155].

The temperature dependent Hall effect measurements reported in figure 73 are in good agreement with the (001) samples. Indeed, for temperatures exceeding 150K, the Hall carrier concentration C_H is equivalent for all thicknesses and decreases as the temperature is reduced (figure 73b). This behavior is characteristic of the thermal activation of carriers, and thus of the n-type semiconductor nature of the bulk material. On the contrary, at low temperature the evolution of the Hall coefficient R_H differs between thick (2µm and 500 nm) and thin samples (100 nm and 50 nm). In the first case, R_H evolves from negative to positive values when decreasing the temperature, which indicates a change in carrier type from electrons to holes. Interestingly, the transition occurs at the same temperature than the one for R_s (figure 72a), and the sheet carrier concentration N_H is equivalent in both samples. This is compatible with hole-like TSS. In contrast, the two thinnest samples exhibit a negative R_H over the entire temperature range and high sheet carrier concentration N_H at low temperatures. This evolution of N_H is not fully understood yet but could be related to strain induced band shifting at low temperature. Due to the thermal activation of charges in the high temperature range (figure 73b), the mobility of all samples is low and increases while decreasing temperature, as shown in figure 73d. All samples, except for the 50 nm one, exhibit a temperature-dependent behavior following $T^{-\alpha}$ with $\alpha > 1.5$ ($T^{-1.9}$ for 2 µm, $T^{-1.8}$ for 500 nm and $T^{-1.7}$ for 100 nm), which is consistent with semi-insulating semiconductor characteristics. For the thinnest sample, however, a $T^{-1.4}$ dependence is detected, indicating a degradation of the transport conditions due to the surface roughness induced by the large interconnected domains. Finally, the 2 µm and 500 nm-thick samples show high hole mobilities of 20 700 $cm^2V^{-1}s^{-1}$ and 1 680 $cm^2V^{-1}s^{-1}$ at 22 K, respectively. These values are in good agreement with those mentioned in other works on BiSb alloys[143,156,157]. In [143], a mobility of 28 000 $cm^2V^{-1}s^{-1}$ is measured in a $Bi_{0.85}Sb_{0.15}$ layer at 5K, which is also expected in our cases if we try to extend our curve to this temperature. The mobilities of both samples decrease with temperature, following a trend described by a negative power law: $T^{-1.7}$ for the 2µm-thick sample for temperatures below 75K and $T^{-1.3}$ for the 500 nm thick sample. These results confirm the TI behavior of the BiSb layers integrated on GaAs(111)A.



*<u>Figure 73:</u> Hall effect measurements on the BiSb layers. **(a)** Evolution of the Hall coefficient R_H, **(b)** the Hall carrier concentration C_H, **(c)** the Hall sheet concentration N_H and **(d)** the Hall mobility μ_H as a function of the temperature. The inset in **(d)** shows the Hall mobility as function of the temperature, in logarithm scales, along with the $T^{-\alpha}$ dependencies, in dotted lines.*

3.6 Conclusions of Chapter 3

In this third chapter, we developed the integration of the BiSb topological insulator on GaAs substrates. A careful study of the growth conditions and specially the surface preparation allowed to synthetize high quality 2D layers[126,127]. On (001) substrates, an axiotaxiale crystalline relationship between the BiSb layer and the GaAs substrate is found around the [1-10] direction, which allows the integration of the hexagonal BiSb(0001) crystal on the cubic GaAs(001) substrates. On the other hand, the integration on (111)A substrates leads to the growth of twin related grains, that can be eliminated by the deposition of an antimony bilayer[137,138]. One question remains about the change of the transport properties of the heterostructure due to the presence of this metallic bi-layer. It is reported in literature that the use of bismuth instead of antimony on Si(111) substrates can indeed create a parallel channel that reduce the surface contribution to the overall transport[158]. This is not the case for Sb terminated Si(111) surfaces, and we expect the same behavior on GaAs(111) surfaces. Finally, both, electrical and ARPES measurements confirmed the presence of the topologically protected surface states on the 2D BiSb layers.

Now that the proof of concept of epitaxially integrating high quality TI layers on industrial substrates is reported, the next step will be to reduce the layer thickness and increase the transition temperature in order to limit the leaking currents into the bulk and maximize the surface transport. Concerning the realization of hybrid interfaces with superconductors, one bottleneck for epitaxial integration of Aluminum layers on BiSb is the necessity to grow these materials at cryogenic temperatures without oxidizing the TI surface[159]. Finally, a new opportunity arises from the development of this new materials: the integration of ferroelectric layers on top of the TI in order to build a new type of Magnetic Random Access Memory based on Spin Orbit Torques (SOT-MRAM)[160]. These different possibilities are presented in the next chapter.

Chapter 4:
Perspectives

My research activities continue to evolve in both direction: the synthesis of new hybrid interfaces combining semiconductors, topological insulators, ferroelectric materials and superconductors and the fabrication of devices for quantum and spintronic applications. This was also made possible thanks to the creation of the Epicentre common laboratory between LAAS-CNRS and Riber SA (see **Annexes**). Growers are highly dependent on the growth reactors available in their environment. This collaboration brought a fully customized system in the LAAS cleanroom including a C21DZ cluster for growing III-V-VI semiconductors and topological insulators, and a prototype for epitaxy of superconductors at cryogenic temperatures. The system will be completed in July 2024 by a glovebox for preparing and transferring samples, without oxidation, between deposition tools. Overall, a perfect environment is being created for realization of highly clean hybrid interfaces, studying their fundamental properties and integrating them into quantum and spintronic devices. This platform is quite unique world-wide, only comparable to few development units present in Microsoft Copenhagen and University of California Santa Barbara. Perspectives proposed in the following are priorities that will be developed in the lab in the coming years.

4.1 Vertically integrated GAA-FET devices

Lot of attention has been given to the optimization of self-catalyzed III-V nanowires integrated on silicon but no working GAA-FET device has been fabricated yet with these nanostructures. Benefiting from the long experience of Dr. Guilhem Larrieu for building top-down GAA-FET in LAAS, we propose to optimize the developed stacks for bottom up nanowire arrays[161] (**figure 74**). This integration still requires lot of process optimizations between growth and device fabrication. Indeed, III-V surfaces are quickly oxidized in air and wet etching of nanowire arrays results generally in their unwanted electrostatic merging. Moreover, the quality of the interface between the high-K oxide and the III-V nanowire is a key parameter in order to improve the device performances. Here we propose to deposit thin gate oxide (5nm) of HfO_2 or Al_2O_3 dielectrics thanks to atomic layer deposition and optimize their permittivity. Another key parameter for efficient devices is the access resistances of the source and drain contracts. Standard AuGe stacks developed for 2D III-V structures are generally not ohmic or present high contact resistances in the case of 3D nanowire arrays. Pt-based contact developed for silicon nanowires might be a solution that should be explored for III-V GAA-FETs. Alternative Ti- and Ni- based metallic contact[162] are also considered in order to reduce source/drain contact resistances and complex Ni/Ge/Au/Ni/Au stacking structures proposed in reference [11] might be developed if necessary. Finally, a direct comparison between top-down and bottom-up GAA-FET device performances will help to access the potential of this technology.

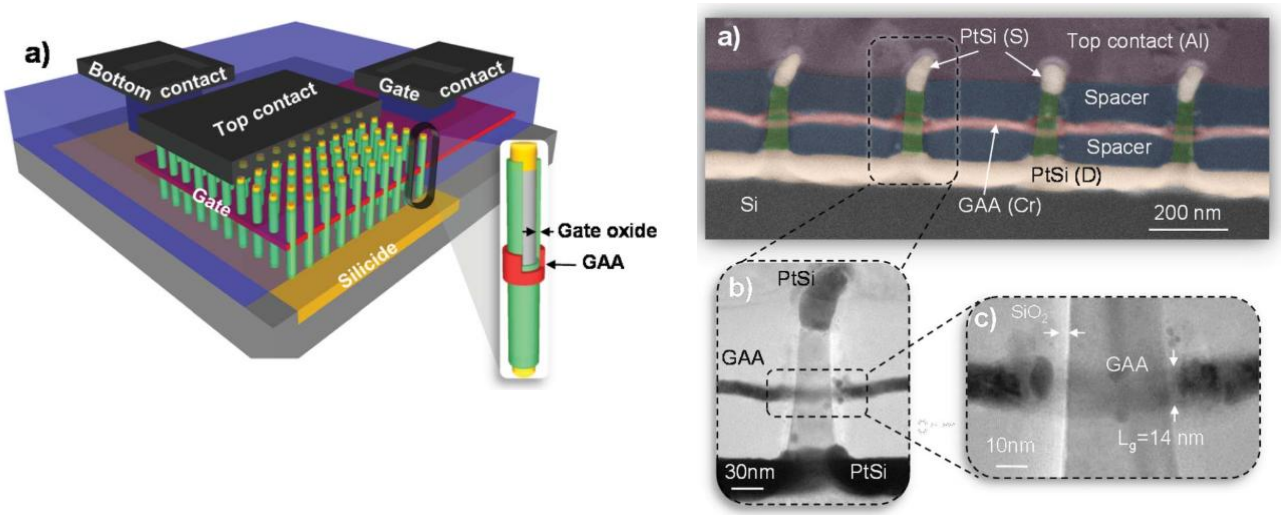


Figure 74: *On left: artistic view of a vertical nanowire array-based field effect transistor. On right: Transmission electron micrographs of the vertical nanowire array transistor.* ***(a)*** *TEM cross-section in tilted view with false color of the device with a gate surrounding each nanowire, a symmetrical silicided S/D (PtSi) contacts and 60 nm low k (2.7) dielectric spacers separating the S/D contacts to the gate,* ***(b)*** *a zoom of the TEM crosssection with a nice planarity of the stacked layers and* ***(c)*** *a zoom of the GAA region with the 5 nm SiO2 gate oxide and the 14 nm gate length.*

4.2 Hybrid semiconductors / superconductor interfaces

As presented in **chapter 2**, hybrid semiconductor / superconductor interfaces are of prime interest for the realization of qubits. Beyond the MZM technologies presented previously, Josephson junction field-effect transistors (JJ-FET) are a key technology broadly used to implement qubits in devices (**figure 75**)[163].

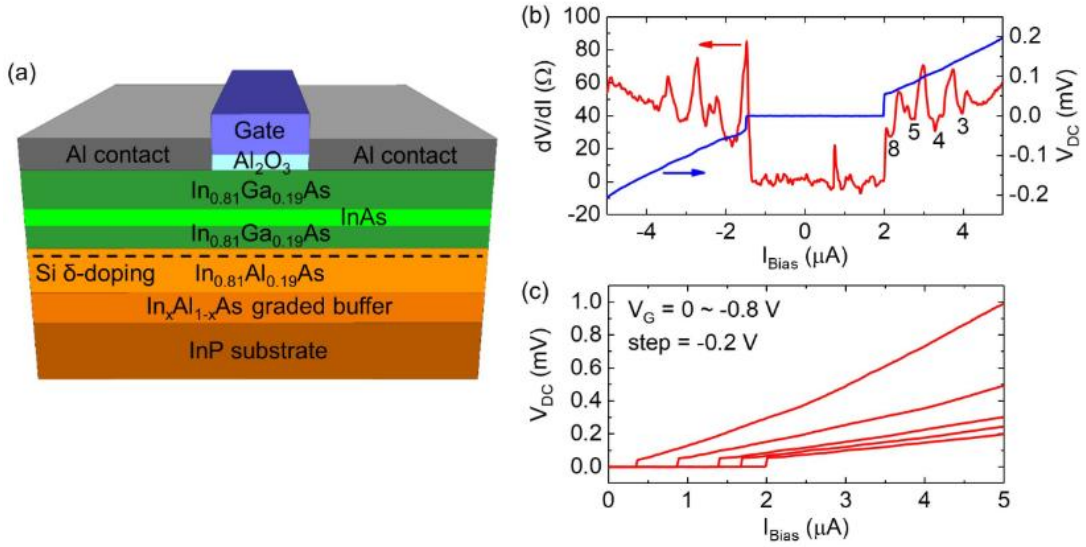


Figure 75: ***(a)*** *Schematic of a JJ-FET, and the InAs quantum well heterostructure platform.* ***(b)*** *dV/dI versus I_{Bias} and V_{dc} versus I_{Bias} measured at V_G = 0 V, shown with red and blue lines and corresponding to the left and right y-axes, respectively. The Andreev reflection dV/dI minima are indicated.* ***(c)*** *I_{Bias} versus V_{dc} at different V_G, where a larger I_C corresponds to a larger V_G value.*

Key metrics to probe their quality are the error rate and the coherence time, both limited by material imperfections. If quantum error correction (QEC) is used to protect quantum information, its implementation requires multiple physical qubits or control systems that strongly limit scaling up. Thus, any improvement of the material quality will have a direct impact on the qubit performances. Actual technologies, for fabricating JJ-FET devices, generally involve ex-situ sputtering processes, yielding to the deposition of polycrystalline superconductors (generally Aluminum). The distribution in the superconducting grain sizes induces a spread in the superconducting gaps and hence in the JJ-FETs behavior. Moreover, the interface transparency between the superconductor and the semiconductor is also of great importance, and any defect will impact the coherence time of devices. An alternative option for fabricating such interfaces is to epitaxially integrate the superconductor at cryogenic temperature in the MBE chamber, as already reported for InAs nanowires[97], which strongly improves the interface transparency. Benefiting from the EpiCentre environment, we have the unique possibility in France to combine both materials in our MBE cluster, and thus to improve further these interfaces. In this context, my research activity will focus on the growth of Al-, Sn-, Pb-superconductors -InAs, -InSb semiconductor interfaces in both configurations: 2D layers and nanowires, as illustrated in figure 76.

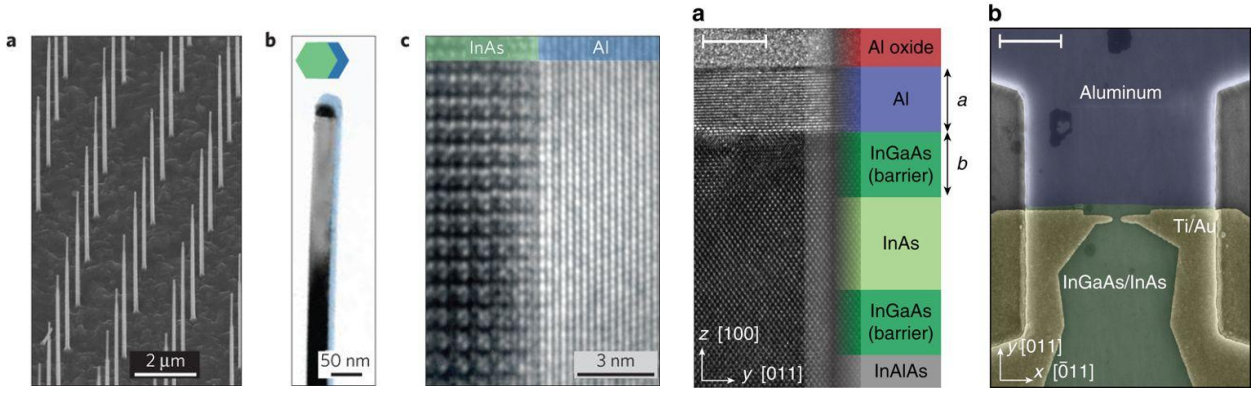


Figure 76: *Examples of hybrid superconductor-semiconductor interfaces. On left: The Al-InAs nanowire geometry. On right, the 2D Al-InAs integration.*

Aluminum is a type I superconductor with a critical temperature of $T_c = 1.2K$ and a critical magnetic field of $H_c = 0,01T$. It is the most used superconductor in quantum devices and will constitute a benchmark to compare the cryo-epitaxial Al-semiconductor interfaces with standard sputtered junctions and demonstrate the improved interface transparency. Other superconductors will be tested including Sn and Pb. Tin is a type I superconductor with a T_c *of 3.72K* and a H_c of *0,03T*. It can be epitaxially integrated on InSb and is compatible with microelectronic industrial processes. Importantly, β-Sn displays a large and robust superconducting gap, with enhanced magnetic fields resilience, and large critical currents. β-Sn-based JJ-FETs have thus high potential for qubits manipulation. Finally, Lead is a type II superconductor with a T_c *of 7.19K* and a H_c of *0,08T.* In this context, Pb has the best fundamental properties, epitaxial integration of InSb is reported, but its compatibility with standard industrial processes is more limited. Nevertheless, the three superconductors will be studied and integrated on both InAs and InSb nanostructures (2D and nanowires).

4.3 The growth of BSTS topological insulators

As discussed in **section 3.1**, our strategy was to first integrate BiSb TI layers on GaAs substrates. With the arrival of the EpiCentre MBE cluster in LAAS designed to grow topological materials, new options are available. Owing to the Bismuth features, many theoretical and experimental studies have focused on the $Bi_{2-x}Sb_xTe_{3-y}Se_y$ (BSTS) materials since it should allow to compensate donors and acceptors in the bulk materials[164] and increase the bandgap up to 0,45eV[165], which is more than 10 times larger than that of $Bi_{1-x}Sb_x$. This is of fundamental importance since the transition temperature between a semiconductor and a TI behavior depends directly on the bulk bandgap and the density of carriers[166] (**figure 77**). If the topologically protected surface states are present at room temperature, they are generally overwhelmed by the bulk transport for low bandgap TIs since their carrier density is several orders of magnitude higher. Applying the Mott criterion to BSTS (**figure 77**), the intrinsic carrier density of 10^{15} cm^{-3} is reached around 300K, which makes it an ideal TI candidate for room temperature applications. Nevertheless, such a high temperature transition has never been observed to our knowledge due to the difficulty to grow single crystalline intrinsic BSTS layers.

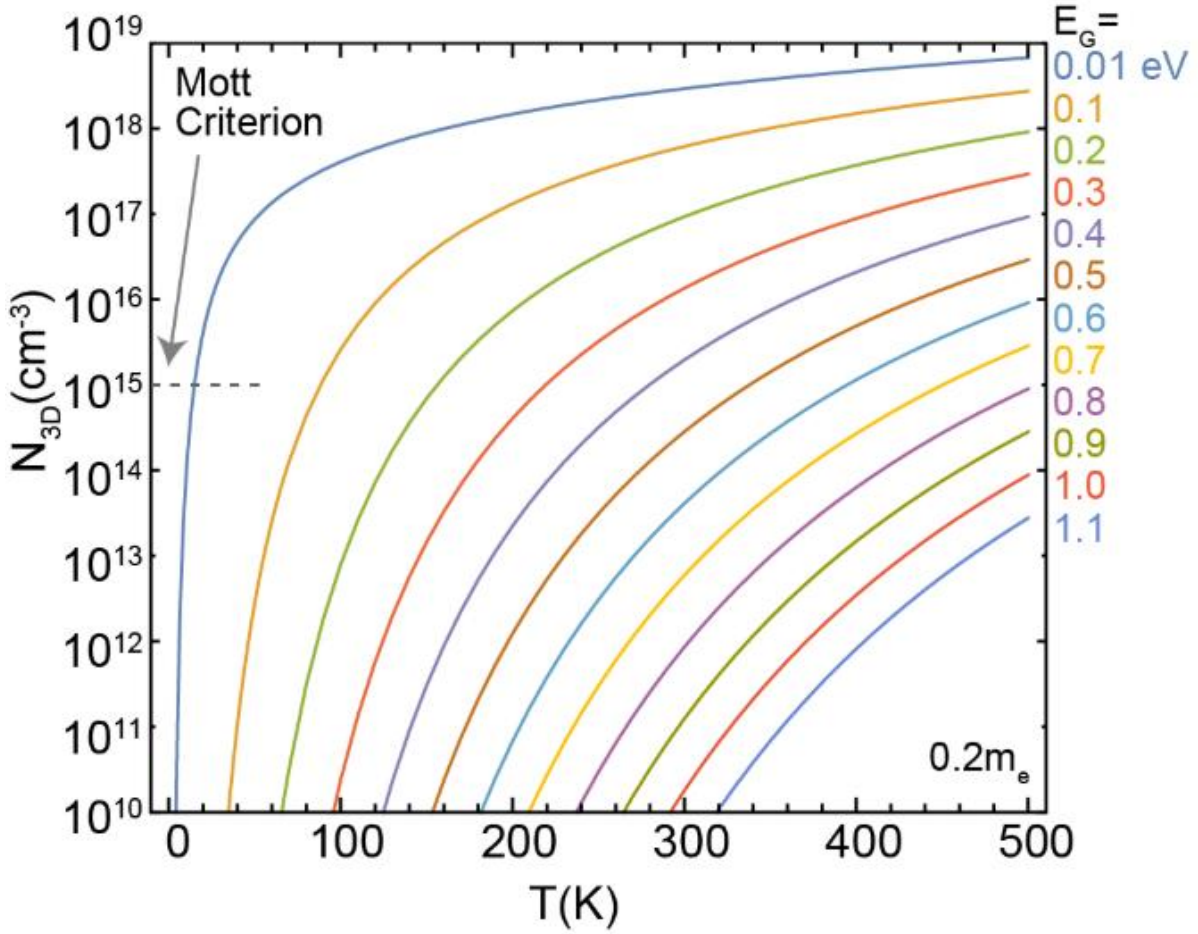


Figure 77: *Temperature dependence of the carrier density for various bandgaps with m* = 0,2 m_e for intrinsic materials and illustration of the Mott criterion.*

We recently studied the integration of BiSbTe (BST) layers on GaAs and measured a bulk bandgap of about 280 meV (**figure 78**). A transition from the semiconductor behavior to the TI one is measured around 220K, which roughly corresponds to the Mott criterion. This demonstrates the possibility to observe topological properties at room temperature for BSTS materials. One of the research axes in the coming years will thus be to optimize these growths.

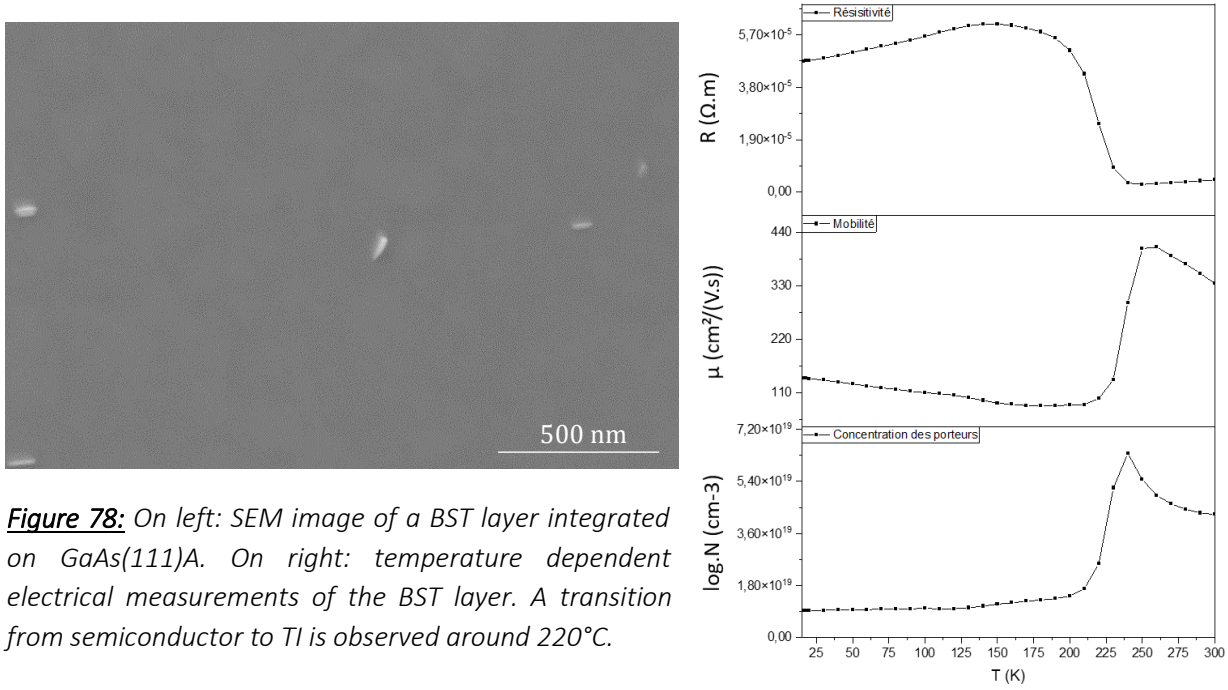


Figure 78: *On left: SEM image of a BST layer integrated on GaAs(111)A. On right: temperature dependent electrical measurements of the BST layer. A transition from semiconductor to TI is observed around 220°C.*

4.4 Selective area growth and topological insulator / superconductor interfaces

The transition from semiconductor to topological insulators, in hybrid interfaces with superconductors, is a logical step toward topological qubits. Indeed, the conclusive evidence for MZMs and their non-Abelian statistics requires sophisticated manipulation and measurement protocols, meaning that the integration of TI into advanced quantum circuits is highly desirable for enhancing coherence times. Nevertheless, the manipulation of quantum information is generally performed using circuit quantum electrodynamics architectures composed of Josephson junctions (JJ)[167], which creates additional demands on the microwave compatibility as the environment needs to have low dielectric losses. TI need thus to be locally integrated on compatible substrates such as Si or sapphire. In a recent study, we demonstrated the possibility to locally integrate BiSbTe materials on *Si(111)-(√3x√3)R30°-Sb* reconstructed surfaces (**figure 79**).

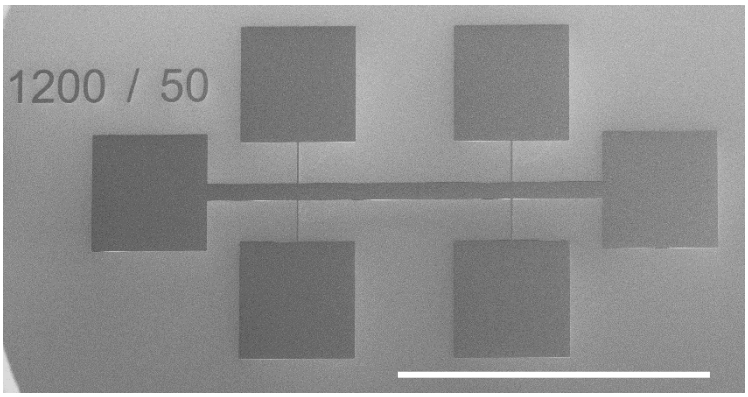


Figure 79: *Example of the selective area growth of a 100nm thick BiSbTe layer on Si(111). Scale bar 1mm.*

After SAG growth of the TI layer in the III-V-VI MBE chamber, samples can be transferred into the superconductor MBE prototype for epitaxy at cryogenic temperature. A complete ultra-high vacuum fabrication process is thus possible, protecting the crucial TI surface and allowing fabrication of complex architectures as reported in figure 80.

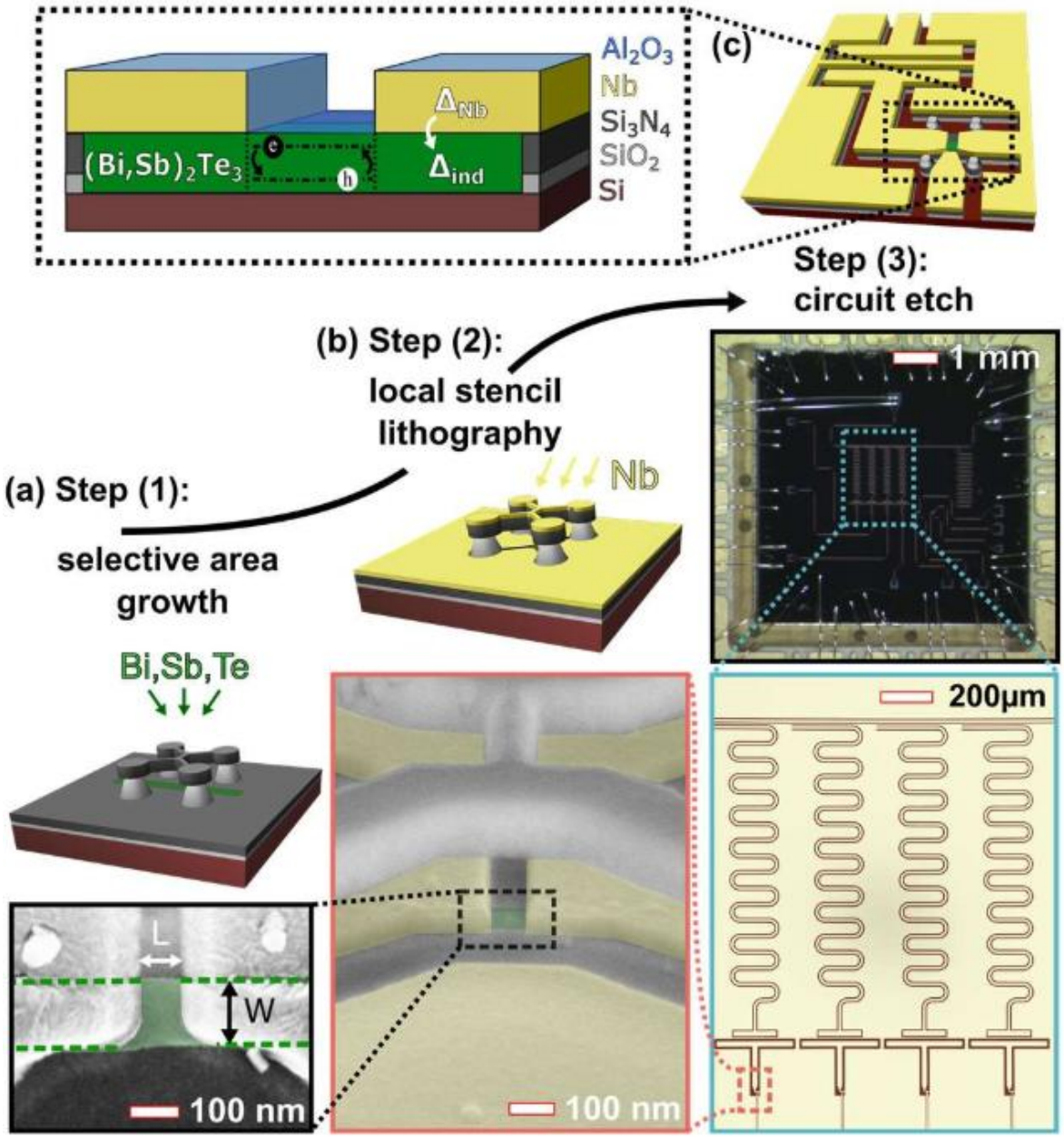


Figure 80: Integration of TI Josephson junctions in superconducting quantum circuits[168]. **(a)** Schematic illustrates SAG of BST in a trench with sample rotation [step (1)]. Bottom false-colored SEM shows a BST nanoribbon (green) of width W. Two Nb electrodes deposited in step (2) are separated by length L. **(b)** Schematic depicts the Nb (yellow) deposition from a fixed angle [step (2)]. False-colored SEM at an angle shows the JJ and the stencil mask used to shadow a part of the BST nanoribbon from the Nb (bottom). **(c)** Top right schematic illustrates the transmon circuitry produced by etching the Nb [step (3)]. Inset (top left) depicts the stack structure in the JJ region, the induced superconductivity in the TI under the Nb electrodes and transport in the JJ via Andreev bound states. Optical micrograph (middle) shows a wire-bonded chip and a false-colored SEM (bottom) the four qubits and readout cavities.

4.5 Ferroelectric / topological insulator interfaces for SOT-MRAMs

Random Access Memories (RAM) are a type of data storage that have been used in computers since their inception and allow a quick access to the stored data. With 300 million computers sold in 2020, Dynamic or Static Random-Access Memories (DRAM or SRAM) are crucial for the microelectronics industry. However, even if these memories have a fast access time, their storage capacity is not great, and they are volatile, which combined to refresh energy of DRAM and leakage current of SRAM are major sources of power dissipation in modern electronics. Implementing non-volatility at the processor level impose the development of an electrically addressable non-volatile memory that combines processor speed (GHz), large endurance, better-than-SRAM density and compatibility with CMOS voltages. Magnetic random-access memories (MRAM) are non-volatile memories that best meet these constraints. They are based on a magnetic tunnel junctions (MTJ), where the magnetic anisotropy energy is used to retain information and on the principle of magnetoresistance to retrieve it[169]. Concerning "writing", a significant attention is given to Spin Transfer Torque (STT) by industry, and STT-MRAMs are now commercially available at major nanoelectronic foundries for e-Flash-like applications. However, their two-terminal configuration, which is excellent for density, has to compromise the writing speed to ~20ns to avoid device degradation and to maintain large endurance (**figure 81**). On the contrary, the Spin Orbit Torque (SOT) based writing is a three terminal device that combines sub-ns high speed with large endurance. Here, switching of the magnetization is achieved thanks to materials exhibiting strong spin orbit interactions and by using either the Rashba or the Spin Hall effect[170–172].

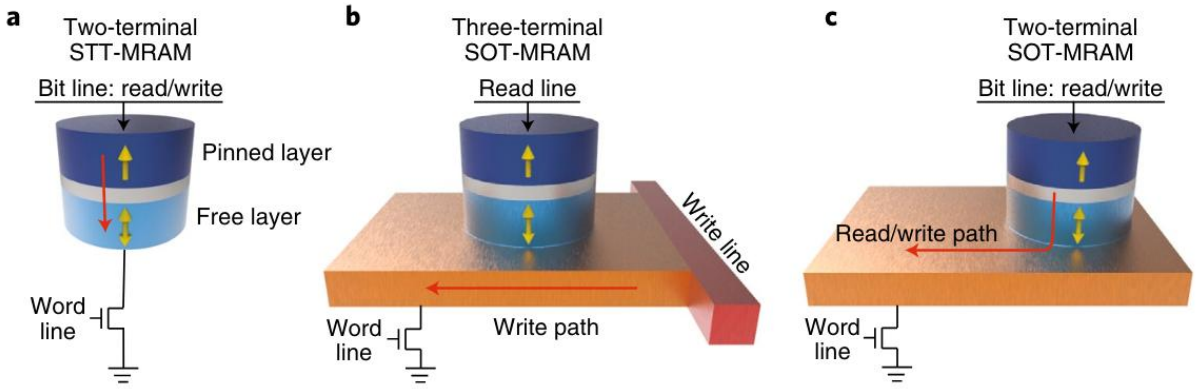


Figure 81: *Three types of MRAM cell structure.* ***(a)****, Schematic of a conventional MRAM cell driven by STT. An out-of-plane current (red arrow) is applied to switch the magnetization of the free layer (bottom layer) through the STT effect. The grey layer is the non-magnetic tunnel barrier, and the yellow arrows indicate magnetization.* ***(b)****, Schematic of a three-terminal SOT-MRAM cell. An in-plane current is applied to switch the magnetization of the free layer through a SOT effect with the assistance of an external magnetic field.* ***(c)****, Schematic of a two-terminal SOT-MRAM cell. A current with both in-plane and out-of-plane components is applied to switch the magnetization of the free layer. The SOT generated by the in-plane component of the current is the dominant mechanism in the switching.*

A typical SOT structure is presented in **figure 81** and consists in a MTJ placed on a heavy metal channel (orange layer). The resistance of the MTJ is dependent of the magnetization of the reference (RL) and the free layers (FL) in a parallel or antiparallel configuration. While SOT-MRAM developments are making great progress, writing current by SOT is still too high and must be reduced by a factor of at least three. Along with the reduction of power consumption of the memory, reducing current is also critical to minimize cell footprint by enabling a minimum size on the addressing transistors. Taking advantage of spin currents present at the TI surfaces, together with Dr. Corentin Durand in LAAS and collaborators from Spintec, we propose to replace the heavy metal in this structure by a TI in order to generate the spin orbit torques at its surface and switch the ferromagnet (FM) magnetization. One of the most challenging steps is the integration of the MTJ on the TI. Indeed, in order to decrease the writing current in a SOT-MRAM, the thickness of the TI material should be reduced as much as possible. This generally induces a surface roughness due to a Volmer-Weber or a Stranski–Krastanov growth mode, depending of the substrate orientation, as reported previously. This roughness can influence the MTJ stacking homogeneity and thus the magnetization of the free layer. The addition of a buffer layer (Ti, Pt, Cr) before deposition of the magnetic material could then solve several issues: improving the FM homogeneity, minimizing the intermixing at the interface and favoring a particular magnetization direction. Preliminary results obtained in LAAS (**figure 82**), demonstrate the integration of a Cobalt magnetic layer on BiSb having an in-plane magnetization. Achieving a perpendicular magnetization of this magnetic layer requires a fine tuning of the interface and a perfect control of its thickness. It should also improve the stability of the FL and thus the reliability of the SOT-MRAM structure. To go beyond this first proof-of-concept, we propose to build a full MTJ stacks on either optimized BiSb of BSTS layers, fabricate micrometer-sized Hall bar (electron beam lithography) and quantify the switching efficiency.

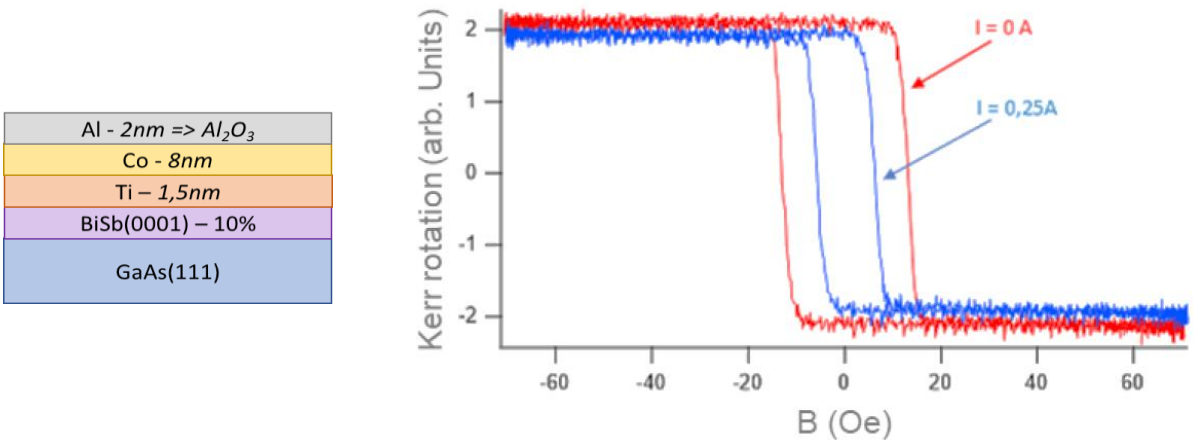


Figure 82: *On left: example of a Co magnetic layer deposited on a TI. On right: Magneto-Optical Kerr effect (MOKE) hysteresis showing in-plane magnetization of 8nm Co layer deposited on BiSb (red hysteresis). Adding a current in the BiSb layer reduces the coercivity H_C (blue hysteresis).*

The typical structure of modern SOT-MTJ consists of a Substrate/SOT/FL/MgO/RL/SAF stack, where the SAF is a synthetic antiferromagnet, and the free layer (FL) (storage) and the reference layer (RL) are made of CoFeB to ensure a high tunnel magnetoresistance (TMR) ratio. Typical TMR reported in SOT-MTJ are on the order of 100-150 % for out-of-plane MTJ. Most studied SOT layer consist of 5d heavy metals such as Pt, Ta, and W, as these materials are already part of MRAM manufacturing. They typically exhibit efficiencies $|\xi_{DL}|$ ranging from 0.1 to 0.5, where ξ is the ratio between the spin current effectively converted into a torque and the charge current used to produce the spin current. In order to ensure its fixed direction, the RL is ferromagnetically pinned to a hard SAF layer by a thin nonmagnetic metal layer such as W or Ta. This metal insertion is equally important to decouple the hard layer texture, usually (111), to the (100) CoFe texture. The SAF relies on strong Ruderman–Kittel–Kasuya–Yosida (RKKY) antiferromagnetic coupling between two ferromagnetic layers separated by thin nonmagnetic spacers. In addition to stabilizing the RL, the role of the SAF is to minimize the dipolar field of the RL radiated on the FL, such as maintaining the hysteresis loop of the FL centered around zero-field. Since we aim at addressing TI-based SOT-MTJs, one should focus on developments using CoFeB material as a FL in order to be compatible with a MTJ-stack, and at least sustaining 300°C thermal budget to obtain large TMR. Another essential point of MRAM technology is the use of perpendicularly magnetized stacks, as they have better scalability and a smaller footprint than their in-plane magnetized counterparts. Interfacial perpendicular magnetization anisotropy (PMA) originates from the spin-orbit interaction and electronic hybridization effects between the FL and the SOT underlayer and/or MgO. Hence, introducing complex materials in the stack, such as TI, can hamper the growth of PMA by intermixing and roughness.

Addressing above challenges, we will deploy and combine two strategies. Firstly, we will study the insertion of a buffer layer X (X-BL) before deposition of the FL, e.g. using Ti, Pt, Cr or Mo, in order to minimize intermixing and to favor a perpendicular magnetization direction. This approach was proven efficient to induce PMA in a magnetic layer deposited on top of TI materials[173]. However, the nature of this buffer layer and the impact of thermal budget on PMA and SOT efficiency remains poorly studied. To accelerate the preliminary developments and to accommodate for available magnetic materials in different tools, other materials like Co could be used to screen the TI/X-BL/FM SOT properties and to narrow down the most promising material TI/X-BL systems to be implemented in SOT-MTJ stack. To leverage the need of CoFeB layer, additional methods can be investigated. For example, the deposition of Boron-getter layers next to the CoFeB FL is known to help the diffusion of B away from it, which in turn provides the local epitaxial order between CoFe and MgO lattices that is required for large TMR and large PMA. We can employ this approach to induce or improve PMA, as successfully achieved recently in Spintec in a different system. Finally, the concept of a hybrid FL, i.e., a FL composed of a reading CoFeB-based layer coupled to a magnetic layer or multilayer with stronger PMA was recently demonstrated[174] and could be used in the frame of TI-based developments.

Annexes

5.1 Curriculum Vitae

Sébastien Plissard

Born the 29th November 1980 in Lons Le Saunier (39)

Education:

2003-2007: **Ph.D. in Physics in the Grenoble Institute of Technology (GIT or INPG).**
Specialization: **Micro et Nano Electronic.**

2002-2003: **Master of Science in Physics (INPG)**
Specialization: **Optics, Optoelectronics and Microwaves**

2000-2003: French engineering school **ENSPG** (currently Phelma)
Specialization: **Instrumentation for Physics**

Professional Experience:

Since 12/2013 **Chargé de Recherche** at **LAAS-CNRS**

10/2010 – 12/2013 **Post-Docs** in the Eindhoven / Delft University of Technology
Collaboration with the group of ***Prof. Erik Bakkers at TU/e***
Collaboration with the group of ***Prof. Leo Kouwenhoven at TU/D***

10/2008 – 09/2010 **Post-Doc** at **IEMN-CNRS**, Lille
Collaboration with the ***Epiphy*** *group*

09/2003 – 09/2007 **Ph.D.** at **CEA-LETI**, Grenoble.
"Study of the p-type doping of the HgCdTe grown by MBE."

Teachings:

2016 – 2021 Lectures at **INSA** -Toulouse (Engineer School) about:
"1D, 2D, 3D growth of nanoscale materials for opto- and nano- electronics"

5.2 Citations, Awards, Administration of science

Citation Report: *(2024/06)*

	Web of Science	*Google Scholar*
H-index	*39*	*40*
Sum of the times cited	*7 900*	*11 280*

Patents (pending)	*0 (2)*
Peer-reviewed articles (submitted)	*65 (2)*
Oral presentations in Conferences (Invited)	*28 (14)*

Awards and Honors:

2012 **Newcomb Cleveland Prize**
AAAS Awards for the best paper of the year published in Science.
"Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices"
V. Mourik, K. Zuo, S.M. Frolov, S.R. Plissard, E.P.A.M. Bakkers, L.P. Kouwenhoven
Science **2012**, 336(6084), 1003-1007, DOI:10.1126/science.1222360

2012 **Majorana Fermions – Top 10 breakthroughs in Physics for 2012**
Awarded by www.physicsworld.com & www.sciencemag.org

2015 **Diana Car**
Award for the Best Student Presentation at the 2015 MRS Spring Meeting, Symposium S.

Administration of science:

Since 2023 Member of the Scientific Committee of the **GdR MatEpi**

Since 2021 Head of the **MPN** team at **LAAS-CNRS** (7 permanent researchers, total ~25)
Chief Scientific Officer of the **Epicentre** laboratory (LAAS – Riber SA)
Member of the **steering committee** and of the **supervisory board** of **EpiCentre**

Since 2018 Member of the Scientific Committee of the **GdR Pulse**

2014 - 2022 Main contact for the **GdR Nanofils**
Organization of a workshop every 18 months.

5.3 Peer-reviewed articles

[67]. **Dense dislocation network in epitaxial $Bi_{1-x}Sb_x$ TIs revealed by wet-etching and TEM**
L. Cancellara, M.A. Khaled, R.Daubriac, S. Fekraoui, A. Arnoult, C. Durand, S.R. Plissard
Just submitted

[66]. **Aligning liquid crystals on self-organized GaAs nanostructures: towards monolithic LC-tunable photonic devices**
H. Villanti, J.-B. Doucet, S. Plissard, A. Arnoult, B. Reig, L. Dupont, V Bardinal
Just submitted

[65]. Large-Scale Epitaxial Integration of Single-Crystalline BiSb Topological Insulator on GaAs (111)A
M.A. Khaled, L. Cancellara, S. Fekraoui, R. Daubriac, F. Bertran, C. Bigi, Q. Gravelier, R. Monflier, A. Arnoult, C. Durand, S.R. Plissard
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D.S. Dhungana, N. Mallet, P.-F. Fazzini, G. Larrieu, F. Cristiano, S. Plissard
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[57]. Ubiquitous Non-Majorana Zero-Bias Conductance Peaks in Nanowire Devices
J. Chen, B.D. Woods, P. Yu, M. Hocevar, D. Car, S.R. Plissard, E.P.A.M. Bakkers, T.D. Stanescu, S.M. Frolov
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5.4 Conferences

Co-organized conferences:

5. *Co-organizer of the MP3 mini-colloquium at the* ***Journées de la Matière Condensée***
   Matériaux fonctionnels pour la spintronique
   Marseille, France, October 28-31, **2024.**
4. *Co-organizer of the MMPS20 mini-colloquium at the* ***Journées de la Matière Condensée***
   Hybrid superconductor-semiconductor nanostructures
   Rennes, France, Augustus 24-27, **2021.**
3. *Co-organizer,* ***MRS Fall 2015, Symposium P***
   Synthesis and Applications of Nanowires and Hybrid 1D-0D/2D/3D Semiconductor Nanostructures
   Boston, USA, November-December 29-4, **2015.**
2. *Organizer,* ***GDR Pulse and GDR Nanofils in Toulouse***
   Toulouse, France, September-October 29-04, **2014.**
1. *Co-organizer,* ***ESPS-NIS 2012***
   Epitaxial Semiconductors on Patterned Substrates and Novel Index Surfaces
   Eindhoven, The Netherlands, May 7-11, **2012.**

Invited talks in conferences:

IT11 *S. Plissard - Defect-free and composition controlled BiSb nanostructures for quantum computing,* **2018 Conference on Materials for Quantum Computing,** Pittsburgh, USA, October 30-November 2**, 2018.**

IT10 *S. Plissard - Nanoscale Topological Insulators for Quantum Computing*
French-American Workshop, Grenoble, France, June 21-22**, 2018.**

IT9 *S. Plissard - Préparation des substrats pour la croissance VLS de nanofils*
GdR Pulse - Atelier Nucléation, Lille, France, Mai 22-24**, 2018.**

IT8 *S. Plissard - Growth of 1D, 2D, 3D materials for opto- and nano-electronics*
IEEE-NMDC Summer School, Toulouse, France, July 10-14, **2017.**

IT7 *S. Plissard - From random to controlled nanowire networks*
Journée Surfaces et Interfaces, Toulouse, France, January 28-30, **2015.**

IT6 *S. Plissard - From random to controlled nanowire networks*
MRS Fall 2014, Symposium LL, Boston, USA, November-December 30-5, **2014.**

IT5 *S. Plissard - From random to controlled nanowire networks*
Optical properties of individual nanowires and quantum dots in high magnetic field, Toulouse, France, September 24-26, **2014.**

IT4 *S. Plissard - InSb nanowire networks*
ESPS-NIS 2014, Traunkirchen, Austria, July 20-23, **2014.**

IT3 *S. Plissard - InSb nanowire railtracks for Majoranas*
MRS Spring 2014, Symposium UU, San Francisco, USA, April 20-24, **2014.**

IT2 *S. Plissard - High quality InSb nanowires for Majorana detection*
6th Nanowire Growth Workshop, St. Petersburg, Russia, June 4-6, **2012.**

IT1 *S. Plissard - Nano-patterned substrates to figure out the growth mechanisms of III-V NWs*
Sigma Symposium, Nijmegen, The Netherlands, April 13, **2012.**

Invited Colloquia:

CL4 *S. Plissard - Molecular beam epitaxy at cryogenic temperature*
RT Vide, Toulouse, France, June 19-22, 2023.

CL3 *S. Plissard - From random to controlled nanowire networks*
Institut Néel, Grenoble, France, March 3, 2015.

CL2 *S. Plissard -InSb nanowires for Majorana devices*
CNRS-INL, Lyon, France, September 6, 2012.

CL1 *S. Plissard III-V nanowires : from growth to applications*
CNRS-LAAS, Toulouse, France, June 18, 2012.

International conferences:

IC54 *S. Plissard –*
Wafer Scale Epitaxial Integration of Single Crystalline BiSb Topological Insulator on GaAs(111)A
ICMBE 2024, Matsue, Japan, September 8-13, 2024.

IC53 *S. Fekraoui, M.A. Khaled, R. Daubriac, L. Cancellara, Q. Gravelier, R. Monflier, A. Arnoult, C. Durand, S. Plissard - Characterization of epitaxial $Bi_{1-x}Sb_x$ topological insulator thin films on GaAs(111) substrates,* JMC 2024, Colloquium MP2, Marseille, France, October 28-31 2024.

IC52 *M.A. Khaled, D.P.G. Nyoma, S. Fekraoui, L. Cancellara, R. Daubriac, T. Blon, B. Lassagne, J.-F. Bobo, F. Bertran, C. Bigi, Q. Gravelier, A. Arnoult, C. Durand, S. Plissard - Epitaxial Topological Insulator Bi1-xSbx films on GaAs substrates for Spintronic applications,* JMC 2024, Colloquium MP2, Marseille, France, October 28-31 2024.

IC51 *M.A. Khaled, R. Daubriac, L. Cancellara, Q. Gravelier, T. Blon, J.-F. Bobo, A. Arnoult, C. Durand, S. Plissard - Topological insulator $Bi_{1-x}Sb_x$ films on GaAs substrates as current-induced Spin-Orbit Torques generators,* 2023 E-MRS Fall Meeting, Warsaw, Poland, September 2023.

IC50 *S. Plissard - Structural and electrical characterizations of BiSb TI layers epitaxially integrated on GaAs,* ICMBE 2022, Sheffield, UK, September 4-9, 2022.

IC49 *S. Plissard - Materials developments for future quantum computers,*
Quantum Technologies Workshop, Toulouse, France, March 10, 2021.

IC48 *S. Plissard - Full CMOS compatibility of InAs nanowires on Silicon,*
J2N 2019, Lyon, France, November 13-15, 2019.

IC47 *Y. Jiang, Z. Yang, D. Car, S. Gazibegovic, B. Ghada, R. Op het Veld, S. Plissard, E. Bakkers, V. Pribiag, S. Frolov - Ferromagnetic Contacts to InSb nanowires,* APS March Meeting, Boston, Massachusetts, USA, March 4-8, 2019.

IC46 *P. Yu, J. Chen, M. Hocevar, G. Badawy, S. Gazibegovic, R. Op Het Veld, S. Plissard, E. Bakkers, S. Frolov - De-localized states in three-terminal InSb nanowire devices,* APS March Meeting, Boston, Massachusetts, USA, March 4-8, 2019.

IC45 *P. Zhang, H. Wu, Z. Su, R. Zitko, E. Lee, D. Car, S. Plissard, M. Hocevar, S. Gazibegovic, R. Op Het Veld, G. Badawy, E. Bakkers, S. Frolov - Erasing odd-parity states in a semiconductor quantum dot coupled to a superconductor,* APS March Meeting, Boston, Massachusetts, USA, March 4-8, 2019.

IC44 *P. Yu, J. Chen, M. Hocevar, D. Car, S. Plissard, E. Bakkers, S. Frolov - Comparing Majorana ZBP with trivial Andreev bound states and super hard superconducting gap in InSb nanowire hybrid devices,* APS March Meeting, Los Angeles, California, USA, March 5-9, 2018.

IC43 *A. Zarassi, Z. Su, J.-F. Hsu, P. San-Jose, E. Prada, R. Aguado, E.J.H. Lee, D. Car, S. Gazibegovic, R. Op het Veld, S. Plissard, J. Logan, M. Pendharkar, D. Pennachio, J. Sue Lee, M. Hocevar, C. Palmstrom, E.P.A.M. Bakkers, S. Frolov - Replicas of Andreev spectra in InSb nanowires,* APS March Meeting, Los Angeles, California, USA, March 5-9, 2018.

IC42 *P. Ebert, P. Capiod, T. Xu, A. Díaz Álvarez, X. Han, D. Troadec, J.-P. Nys, M. Berthe, L. Lymperakis, J. Neugebauer, I. Lefebvre, S. Plissard, P. Caroff, R. Dunin-Borkowski B. Grandidier - How can band offsets in III-V nanowires be determined correctly by scanning tunneling spectroscopy?,* 45th Conference on the Physics and Chemistry of Surfaces and Interfaces (PCSI-45), Kona, Hawai, USA, January 14-18, 2018.

IC41 *S. Plissard - Defect-free $Bi_{1-x}Sb_x$ nanowires on Si by MBE* J2N 2017, Grenoble, France, November 13-15, 2017.

IC40 *Z. Su, H. Wu, M. Hocevar, D. Car, S. Plissard, E. Bakkers, S. Frolov - Kitaev model with quantum dot chains I: zero bias peaks,* APS March Meeting, New Orleans, Louisiana, USA, March 13-17, 2017.

IC39 *H. Wu, Z. Su, M. Hocevar, D. Car, S. Plissard, E. Bakkers, S. Frolov - Kitaev model with quantum dot chains II: zero bias peaks,* APS March Meeting, New Orleans, Louisiana, USA, March 13-17, 2017.

IC38 *V. Mourik, K. Zuo, D. Szombati, D. Pikulin, B. Nijholt, V. Ostroukh, A. Akhmerov, D. van Woerkom, A. Geresdi, D. Car, S. Plissard, E. Bakkers, L. Kouwenhoven, S. Frolov - Magnetic field and gate tunable supercurrent fluctuations in multimode semiconductor nanowires,* APS March Meeting, New Orleans, Louisiana, USA, March 13-17, 2017.

IC37 *P. Yu, J. Chen, M. Hocevar, D. Car, S. Plissard, E. Bakkers, S. Frolov - Zero-bias peaks in InSb nanowire hybrid devices: magnetic field anisotropy, peak splittings and phase diagrams,* APS March Meeting, New Orleans, Louisiana, USA, March 13-17, 2017.

IC36 *D.S. Dhungana, N. Sartori, N. Mallet, F. Cristiano, G. Larrieu, A. Hemeryck, S.R. Plissard - Controlling nanowire nucleation for integration on silicon,* IEEE Photonics Society Summer Topical Meeting Series (SUM), Newport Beach, California, USA, July 11-13, 2016.

IC35 *Z. Yang, A. Surrente, K. Galkowski, G. Tutuncuoglu, H. Potts, M. Friedl, J.B. Leran, A. Fontcuberta i Morral, F. Cristiano, D.K. Maude, S.R. Plissard, P. Plochocka – Optical properties of GaAsSb nanowire networks and GaAs nanomembranes,* 11th IEEE Nanotechnology Materials and Devices Conference (NMDC), Toulouse, France, October 9-12, 2016.

IC34 *Z. Su, J. Chen, P. Yu, M. Hocervar, S. Plissard, D. Car, A. Tacla, A. Daley, D.Pekker, E. Bakkers, S. Frolov - Spins of Andreev states in double quantum dots,* APS March Meeting, Baltimore, Maryland, USA, March 14-18, 2016.

IC33 *J. Chen, P. Yu, M. Hocevar, S. Plissard, D. Car, E. Bakkers, S. Frolov - Super-Hard induced gap in InSb nanowires,* APS March Meeting, Baltimore, Maryland, USA, March 14-18, 2016.

IC32 *P. Yu, J. Chen, M. Hocevar, S. Plissard, D. Car, E. Bakkers, S. Frolov - Superconducting gap closing and Zero-bias peak in InSb nanowire,* APS March Meeting, Baltimore, Maryland, USA, March 14-18, 2016.

IC31 *P. Yu, J. Chen, M. Hocevar, S. Plissard, D. Car, E. Bakkers, S. Frolov - Zero-bias peak in InSb nanowires,* APS March Meeting, San Antonio, Texas, USA, March 2-6, 2015.

IC30 *J. Chen, P. Yu, M. Hocevar, S. Plissard, D. Car, E. Bakkers, S. Frolov - Zero-bias peak splitting in InSb nanowires,* APS March Meeting, San Antonio, Texas, USA, March 2-6, 2015.

IC29 *S. Assali, D. Kriegner, I. Zardo, S. Plissard, M.A. Verheijen, J. Stangl, J.E.M. Haverkort, E.P.A.M. Bakkers - Direct band gap wurtzite GaP nanowires for LEDs and quantum devices,* **Conference on Nanoepitaxy - Materials and Devices VI,** *San Diego, California, USA, August 19-21,* **2014.**

IC28 *M. Cassidy, J. Kammhuber, D. Car, S. Plissard, E. Bakkers, L. DiCarlo, L. Kouwenhoven - Coupling InSb quantum dots to a superconducting microwave resonator*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC27 *M. Cassidy, J. Kammhuber, D. Car, S. Plissard, E. Bakkers, L. DiCarlo, L. Kouwenhoven - Coupling InSb quantum dots to a superconducting microwave resonator*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC26 *F. Pei, M. Cassidy, S. Plissard, D. Car, E. Bakkers, L. Kouwenhoven - Probing the local environment of a superconductor-proximitized nanowire using single electron transistors*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC25 *J. Chen, P. Yu, S. Plissard, D. Car, V. Mourik, K. Zuo, D. van Woerkom, D. Szombati, L. Kouwenhoven, E. Bakkers, S. Frolov - Supercurrents in InSb nanowire Josephson junctions*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC24 *A. Geresdi, D.B. Szombati, L.J. Cornelissen, D. Car, S. Plissard, E. Bakkers, L. Kouwenhoven - Anomalous oscillations of the Josephson supercurrent in InSb nanowires*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC23 *K. Zuo, V. Mourik, D. van Woerkom, F. de Vries, S. Plissard, E. Bakkers, L. Kouwenhoven - Majorana fermions in hybrid superconductor-semiconductor nanowire devices*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC22 *I. van Weperen, D. Eeltink, B. Tarasinski, M. Wimmer, S. Plissard, E. Bakkers, L. Kouwenhoven - Large spin-orbit quantum interference effects in a dual-gated InSb nanowire device*, APS March Meeting, Denver, Colorado, USA, March 3-7, 2014.

IC21 *S. Assali, I. Zardo, S. Plissard, M.A. Verheijen, J.E.M. Haverkort, E.P.A.M. Bakkers, - Wurtzite Gallium Phosphide has a Direct-Band Gap,* ICON 2013, Annecy, France, November 23-26, 2013.

IC20 *Y. Cui, S. Plissard, J. Wang, T.T.T. Vu, E. Smalbrugge, E.J. Geluk, T. de Vries, J. Bolk, M. Trainor, M.A. Verheijen, J.E.M. Haverkort, E.P.A.M. Bakkers*
InP nanowire array solar cell with cleaned sidewalls, 2013 International Conference on Indium, Phosphide and Relaetd Materials (IPRM), Kobe, Japan, May 19-23, 2013.

IC19 *V. Mourik, K. Zuo, D. van Woerkom, S. Frolov, S. Plissard, E. Bakkers, L. Kouwenhoven - Majorana fermions in hybrid superconductor-semiconductor nanowire devices,* APS March Meeting, Baltimore, Maryland, USA, March 18-22, 2013.

IC18 *S. Plissard - InSb branched nanowires for Majorana fermion manipulations*
MRS Fall 2012, Boston, USA, November 25-30, 2012.

IC17 *S. Plissard - InSb nanowire structures for Majorana fermion manipulations*
Nanowire 2012, Berlin, Germany, September 19-21, 2012.

IC16 *S. Nadj-Perge, J. van den Berg, S. Frolov, V. Pribiag, S. Plissard, E. Bakkers, L. Kouwenhoven - Coherent manipulation of spin-orbit quantum bits in InSb nanowires*, APS March Meeting, Boston, MA, USA, February 27-March 2, 2012.

IC15 *V. Pribiag, S. Nadj-Perge, Stevan, J. van den Berg, S. Frolov, S.Plissard, E. Bakkers, L. Kouwenhoven - Electrical control of single hole spins in InSb nanowire quantum dots*, APS March Meeting, Boston, MA, USA, February 27-March 2, 2012.

IC14 *S. Frolov, S. Nadj-Perge, V. Pribiag, J. van den Berg, S. Plissard, E. Bakkers, L. Kouwenhoven - Electric dipole spin resonance measurement of spin-orbit anisotropy in InSb nanowire quantum dots*, APS March Meeting, Boston, MA, USA, February 27-March 2, 2012.

IC13 *S. Plissard - Study of the InSb nanowire growth mechanisms*
GDR Nanofils, Porquerolles, France, October 17-21, 2011.

IC12 *P. Caroff, T. Xu, K.A. Dick, S.R. Plissard, T.H. Nguyen, B. Grandidier, X. Wallart - Growth of antimony-containing heterostructure nanowires by molecular beam epitaxy : crystal phase control, surfaces and interfaces,* MRS Spring 2011, Symposium EE : Semiconductor nanowires - From fundamentals to applications, San Francisco, California, USA, 2011.

IC11 *P. Caroff, J. Bolinsson, S.R. Plissard, X. Wallart, K.A. Dick - Controlled axial polytypism in single binary and ternary III-V nanowires,* 6th International Conference on Materials for Advanced Technologies, ICMAT 2011, Symposium I : Semiconductor nanowires and heterostructures : synthesis, properties and multifunctions, City of Singapore, Singapore, June 2011.

IC10 *P. Caroff, K.A. Dick, C. Thelander, S.R. Plissard, X. Wallart - Growth of antimony-containing nanowires.* Thematic Days on Nanowires and Applications, Villeneuve d'Ascq, France, 2011.

IC9 *P. Caroff, C. Thelander, S.R. Plissard, X. Wallart, K.A. Dick - Growth by MBE and characterization of antimonide III-V nanowires,* 473rd Wilhelm and Else Heraeus Seminar, Bad Honnef, Germany, 2011.

IC8 *S. Plissard, P. Caroff, K.D. Thelander, X. Wallart - Direct Integration of GaAs/GaAsSb NWs Grown by MBE on Si without Extrinsic Metal Particle*
MRS Spring 2010, San Francisco, CA, April 5-9, 2010.

IC7 *X. Wallart, C. Coinon, S.R. Plissard, S. Godey, O. Offranc, V. Magnin, J.-F. Lampin - Low temperature grown GaAsSb as photoconductive material near 1.06 µm.* 22nd IEEE Conference on Indium Phosphide and Related Materials (IPRM), Kagawa, Japan, 2010.

IC6 *L. Desplanque, D. Vignaud, S. Godey, S.R. Plissard, E. Cadio, X. Wallart, P. Liu, H, Sellier - $Al_{0.56}In_{0.44}Sb/Ga_{0.5}In_{0.5}Sb$ heterostructures for high speed and low power consumption electronic devices,* 16th International Conference on Molecular Beam Epitaxy, Berlin, Germany, 2010.

IC5 *S.R. Plissard, K.A. Dick, X. Wallart, P. Caroff - Direct integration of gold-free GaAs/GaAsSb nanowires on Si by MBE,* 16th International Conference on Molecular Beam Epitaxy, Berlin, Germany, 2010.

IC4 *X. Wallart, C. Coinon, S.R. Plissard, S. Godey, O. Offranc, V. Magnin, J.-F. Lampin - Characterization of low temperature grown $GaAs_{1-x}Sb_x$ with x ~ 0.15*. 16th International Conference on Molecular Beam Epitaxy, Berlin, Germany, 2010.

IC3 *S.R. Plissard, G. Larrieu, X. Wallart, P. Caroff - Growth of aligned self-catalysed GaAs nanowires on Si(111) using a VLS mechanism*. 5th Nanowire Growth Workshop, Rome, Italy, 2010.

IC2 *P. Caroff, S.R. Plissard, X. Wallart, K.A. Dick, C. Thelander - Growth of antimony-containing nanowires by MBE.* 5th Nanowire Growth Workshop, Rome, Italy, 2010.

IC1 *S. Plissard, P-type doping of HgCdTe grown by molecular beam epitaxy*
The 2006 U.S. workshop on the physics and chemistry of II-VI materials,
Newport Beach, CA, October 10-12, 2006.

5.5 Supervision of research

PhD Students:

- Salima Fekraoui (2023-2026) – Université de Toulouse - LAAS-CNRS – 100%
  Growth of the BSTS topological insulator
- Dima Sadek (2018-2022) – Université de Toulouse - LAAS-CNRS – 100%
  Integration of the BiSb topological insulator on industrial substrate: from structural to electrical characterizations
- Daya Sagar Dhungana (2015-2018) – Université de Toulouse - LAAS-CNRS – 100%
  Growth of InAs and $Bi_{1-x}Sb_x$ nanowires on silicon for nanoelectronics and topological qubits by molecular beam epitaxy
- Diana Car (2012-2016) – TU Eindhoven – 50%
  Synthesis of InSb nanowire architectures: building blocks for Majorana devices
- Jia Wang (2010-2014) – TU Eindhoven – 50%
  Controlling nanowire growth direction

Postdoctoral researchers:

- Mohamed Ali Khaled (2024-2025) – Université de Toulouse - LAAS-CNRS – 100%
  Topological Materials for Magnetic Memories
- Richard Daubriac (2023-2024) – Université de Toulouse - LAAS-CNRS – 100%
  Cryogenic molecular beam epitaxy of Superconductors
- Leonardo Cancellara (2023-2024) – Université de Toulouse - LAAS-CNRS – 50%
  Investigation of materials and nanostructures for electronics by TEM

Master students:

- Salima Fekraoui (2023) – 100%
  Growth of the $Bi_{1-x}Sb_x$ TI by MBE
- Abdourahman Khaireh Walieh (2021) – 50%
  Deep learning based RHEED image recognition for crystal growth automation and Characterization
- Grégoire Chevrier (2020) – 100%
  Growth of Al layers on III-V semiconductors
- Wouter de Jong (2018) – 100%
  Controlling compositions in the Nanoscale $Bi_{1-x}Sb_x$ Topological Insulator
- Nicolò Sartori (2016) – 100%
  Nucleation and first steps of nanowire growth

Participation in PhD committees:

- Diana She (2024) – Examiner
  Molecular beam epitaxy growth of the BiSb/MnGa heterostructures for the charge current to spin current conversion study
- Thomas Dussarp (2022) – Examiner
  GaAs nanowires: crystal phase engineering and applications for water photoelectrolysis
- Anjali Harikumar (2022) – Examiner
  Development of AlGaN nanostructures for the fabrication of electron-pumped UV emitters
- Romaric de Lépinau (2020) – Examiner
  GaAs-on-Si solar cells based on nanowire arrays grown by molecular beam epitaxy
- Marco Vettori (2019) – Examiner
  Growth optimization and characterization of regular arrays of GaAs/AlGaAs core/shell nanowires for tandem solar cells on silicon
- Giacomo Priante (2016) – Examiner
  Formation mechanisms of heterostructures and polytypes in III-V nanowires
- Adrián Díaz Álvarez (2016) – Examiner
  Surface characterization of III-V semiconductor nanowires: Morphological, structural and electronic properties
- Jean-Baptiste Barakat (2015) – Reviewer
  Micro- et nanofils de Ga(In)N et GaAs par épitaxie en phase vapeur par la méthode
- Pierre-marie Coulon (2014) – Examiner
  Croissance et Caractérisation de Nanofils/Microfils de GaN
- Geoffrey Avit (2014) – Examiner
  Micro- et nanofils de Ga(In)N et GaAs par épitaxie en phase vapeur par la méthode

5.6 Reviewing activities

I regularly participate in the review of projects for the following agencies:

- Agence Nationale de la recherche (ANR) for the annual call (~1 per year) – CE09
- ANR for the PEPR Electronic call (2023)
- HCERES for evaluation of the IM2NP evaluation (2023)
- Swiss National Science Foundation (SNSF) for the annual call

I regularly review studies in the following journals:

- Advanced Materials (Wiley)
- Nature Communications (NPG)
- Scientific reports (NPG)
- Nano Letters (ACS)
- Nanotechnology (IOP)
- Applied Physics Letters (AIP)
- Journal of Applied Physics (AIP)

Since 2023, I am Associate Editor at the European Physical Journal Applied Physics (EPJ AP).

5.7 Research funding

Year	Acronym	Details	Agency	Role	Collaborators	Funding
2024	M3TI	Magnetism and Transport with Topological Insulators	Quantum Technologies in Occitanie	Co-PI	LAAS	24 000€
2023	TopMemo	Topological materials for Magnetic Memories	ANR-PRC-C09	PI	SPINTEC	242 000€
2023	TOPOSOT	Topological insulators as Spin-Orbit Torque source materials for the manipulation of perpendicularly magnetized thin films	NanoX	Co-PI	LPCNO CEMES	90 000€
2023	CryoSup	Cryogenic molecular beam epitaxy of Superconductors	Quantum Technologies in Occitanie	PI	LPCNO	80 000€
2022	SPINMAT	Glovebox Auger spectrometer	PEPR SPIN		LAAS	100 000€
2022	HyTop	Hybrid interfaces with Topological Insulators	Quantum Technologies in Occitanie	Co-PI	CEMES	80 000€
2021	EpiCentre	Common laboratory between LAAS-CNRS and Riber SA	Chief Scientific Officer Member of the Steering Comity Member of the Supervision Board			9 000 000€
2017	HYBRID	Hybrid materials for quantum science and engineering	ANR-PIRE		Néel-CNRS Pittsburgh Uni UCSB	220 000€
2015	NanOnSi	Integration of high mobility III-V nanowires on silicon	MESR	PI		220 000€
2014	WireOnSi	"Bottom up" integration of high mobility III-V nanowires on silicon	IDEX Emergence	PI		100 000€

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